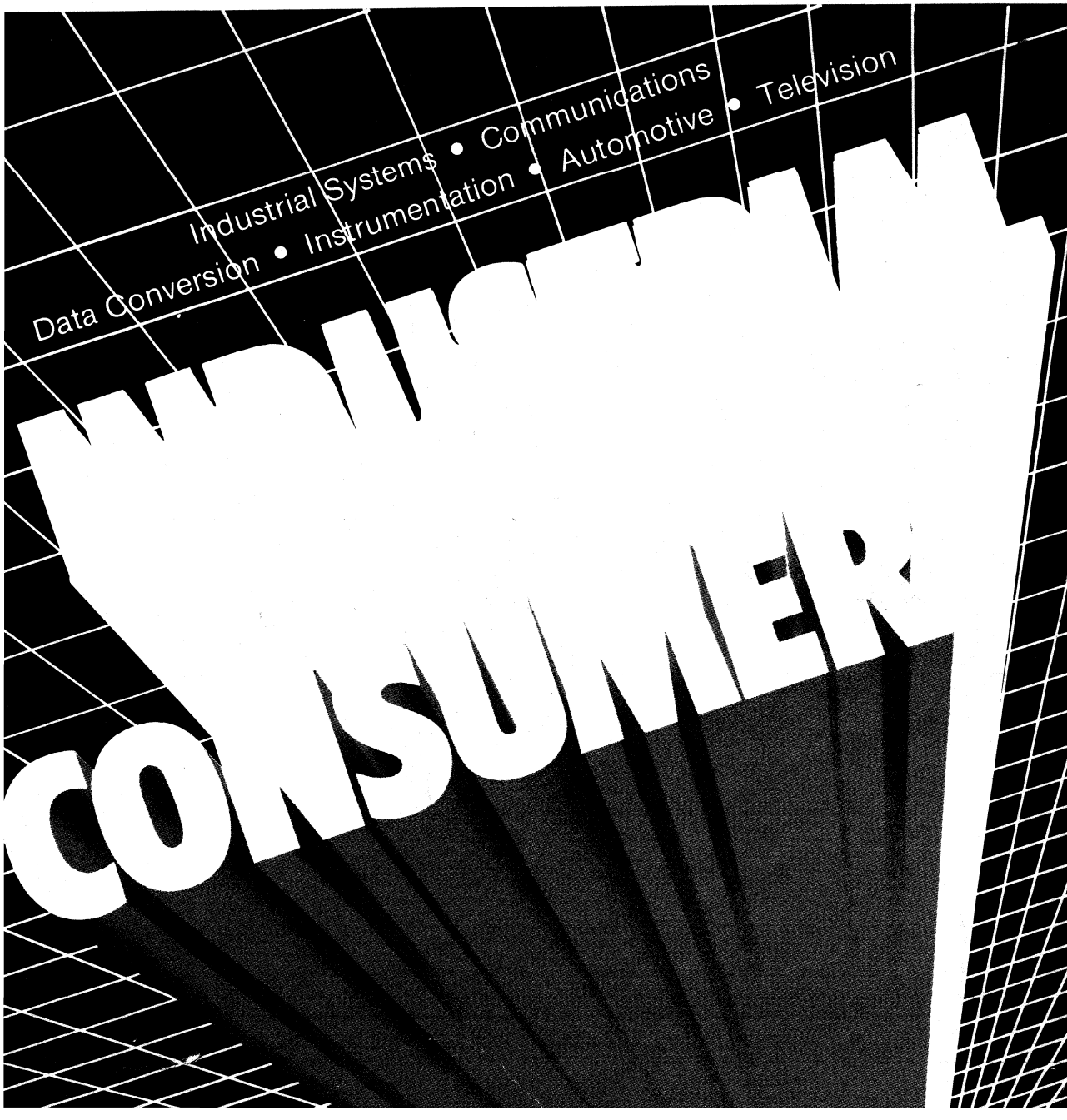
RCA Solid State

Linear Integrated Circuits
and MOS/FET's



RCA Linear Integrated Circuits
and MOS/FET's

This DATABOOK contains detailed technical information on the full line of linear integrated circuits and the low-power line of metal-oxide-semiconductor field-effect transistors (MOS/FET's) currently available from RCA Solid State Division. This broad spectrum of products includes many highly diverse types intended for a wide range of circuit functions in industrial and/or consumer applications.

The first section, a general over-all guide to available products, contains a complete index of types, photographs of the wide variety of package options, product classification and selection guides, recommended operating and handling procedures, a list of special terms and symbols, and a cross-reference listing that shows the recommended RCA replacement types for many popular industry devices. This general section is followed by technical data on individual types grouped into eleven broad product categories, including: Operational Amplifiers, Voltage Comparators, Data-Conversion Circuits, Arrays, Power Control Circuits, Differential Amplifiers, Special-Function Circuits, Audio Circuits, Radio Circuits, and MOS/FET's. The first page of each data section lists all the types included in the section grouped according to specific circuit functions together with a reference to the page that contains the technical data for each type.

The final section of the DATABOOK lists high-reliability types supplied for military, aerospace, and critical industrial applications and defines the screening levels to which each of them are supplied, shows dimensional outlines for all package types, and lists, together with a brief abstract, current RCA application notes on linear integrated circuits and MOS/FET's.

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The device data shown for some types are indicated as preliminary. **Preliminary data** are intended for guidance purposes in evaluating devices for equipment design. Such data are shown for types currently being designed for inclusion in our standard line of commercially available products. For current information on the status of preliminary programs, please contact your local RCA sales office.

Printed in USA/1-84

General Guide to Linear Integrated Circuits

1

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CA3050	†	—	—	—	—	—	361	410
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CA3183	E	H	—	—	—	—	532	459
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CA3600	E	—	—	—	—	—	619	479
CA6078A	T	S	—	—	—	—	592	79
CA6741	T	S	—	—	—	—	592	79

■ No designated suffix letter for this type in TO-5 style package

‡‡ No designated suffix letter for this type of ceramic flat package

• No designated suffix letter for this type in dual-in-line plastic package

† No designated suffix letter for this type in dual-in-line ceramic package

Δ No designated suffix letter for this type in quad-in-line plastic package

* In 8-lead dual-in-line Mini-DIP package

§ In 14-lead dual-in-line plastic package

★ No designated suffix letter for this type in TO-220-style package with vertical-mount lead form.

Packages

RCA linear device packages are identified by letters as indicated in the following chart. When ordering a Linear device, it is important that the appropriate suffix letter(s) be affixed to the type number of the device.

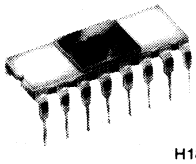
Package	Suffix Letter
Dual-In-Line Welded-Seal Ceramic Package	D
Dual-In-Line Plastic Package	E
Dual-In-Line Frit-Seal Ceramic Package	F
Chip	H
Dual-In-Line Plastic Package with "Power Slab"	P
Modified Dual-In-Line Plastic Package with "Power Slab"	EM
Modified Quad-In-Line Plastic Package	QM
Quad-In-Line Plastic Package	Q
TO-5 Style Package with Dual-In-Line Formed Leads (DIL-CAN)	S
TO-5 Style Package with Straight Leads	T
TO-220 Style Package with Horizontal-Mount Lead Form	M
TO-5 Style Package with Radial Formed Leads	V1
Staggered Quad-In-Line Plastic Package	W
Ceramic Flat Package	K

Notes:

1. Some types may have an additional "M" suffix following the package designation suffix, i.e., CA3134EM. The additional "M" suffix simply indicates that the device is a mechanical variant of the basic package type.

2. RCA linear integrated circuits are provided in chip form to allow customer design of special and complex circuits to suit individual needs. Linear chips are electrically identical to and offer the features of their counterparts, sealed in ceramic, TO-5, and plastic packages. The package-options charts shown with the functional diagrams for each generic type of RCA linear integrated circuit indicate those types for which chip versions are available.

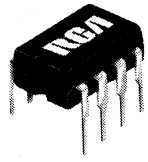
D Suffix
Dual-In-Line Welded-Seal Ceramic Package



H1844

14 and 16-lead versions

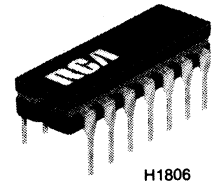
E Suffix
Dual-In-Line Plastic Package



H1817

8, 14, 16, 18, 22, 24 and 28-lead versions

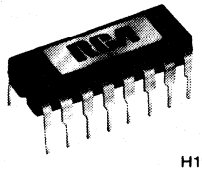
F Suffix
Dual-In-Line Frit-Seal Ceramic Package



H1806

14 and 16-lead versions

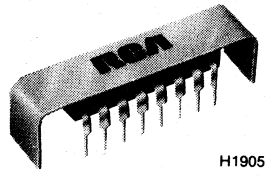
P Suffix
"Power Slab" Plastic Dual-In-Line Package



H1902

CA3136P only

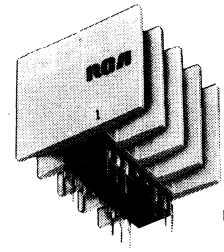
EM Suffix
Modified 16-lead Dual-In-Line Plastic Package with "Power Slab"



H1905

CA3134EM only

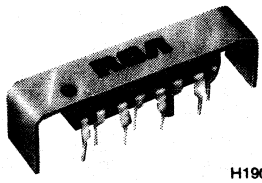
EM Suffix
Modified 16-lead Dual-In-Line Plastic Package with "Power Slab"



H1827

Packages (Cont'd)

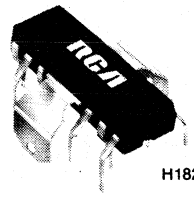
QM Suffix
Quad-In-Line Plastic Package (QUIP) with "Power Slab"



H1906

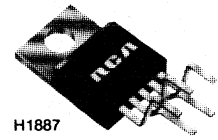
16-lead version

Q Suffix
Modified 16-lead QUIP



H1825

VERSA-V and VERSA-V1 TO-220 Style Plastic Package with Vertical-Mount Lead Form



H1887

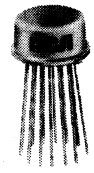
(Versions with horizontal-mount lead form are also available).

S Suffix
TO-5 Style Package with Dual-In-Line Formed Leads (DIL-CAN)

H1787

8-lead version

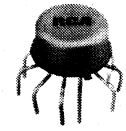
T Suffix
TO-5 Style Package with Straight Leads



H1463

8, 10, and 12-lead versions

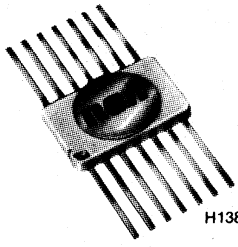
V1 Suffix
TO-5 Style Package with Radial Formed Leads



H1561

8, 10, and 12-lead versions

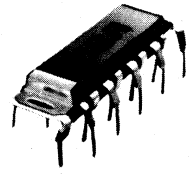
K Suffix
Ceramic Flat Package



H1383R1

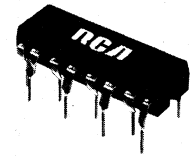
14-lead version

Shielded 20-lead Quad-In-Line Plastic Package



H1704

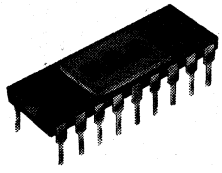
W Suffix
Staggered Quad-In-Line Plastic Package



H1885.

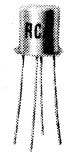
14 and 16-lead versions

D Suffix
18-lead Dual-In-Line Side-Brazed Ceramic Package



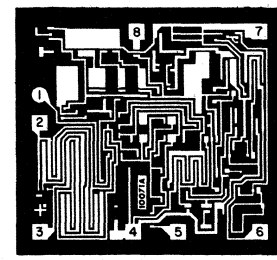
H1910

JEDEC TO-72



H1299

H Suffix
Chip



92CM-32235

Product Classification Chart

Industrial Circuits

OPERATIONAL AMPLIFIERS

General Purpose

Single Unit	Dual Unit
CA101	CA082*
CA201	CA083*
CA301A	CA158
CA307	CA258
CA741	CA358
CA748	CA747
CA3105	CA1458
CA3152*	CA1558
CA3193*	CA2904
CA3420*	Quad Unit
CA3493*	CA084*
CA6741•	CA124
	CA224
	CA324
	CA3401

General Purpose Wideband

Single Unit
CA080*
CA081*
CA3008
CA3010
CA3015
CA3016
CA3029
CA3030
CA3037
CA3038
CA3100*
CA3130*
CA3140*
CA3160*
Dual Unit
CA3240*
CA3260*

Variable

High Current
CA3094
Micropower
CA3060
CA3078
CA3080
CA3440*
CA6078A•
Dual Unit
CA3280

DIFFERENTIAL AMPLIFIERS

CA3000
CA3001
CA3004
CA3005
CA3006
CA3007
CA3026
CA3028
CA3040
CA3049
CA3050
CA3051
CA3053
CA3054
CA3102

ARRAYS

Amplifier/Diode

Amplifier
CA3026
CA3035
CA3048
CA3049
CA3052
CA3054
CA3060
CA3102
Diode
CA3019
CA3039
CA3141

Transistor

CA1724	CA3096
CA1725	CA3097
CA3018	CA3118
CA3036	CA3127
CA3045	CA3128
CA3046	CA3138
CA3050	CA3146
CA3051	CA3183
CA3081	CA3227
CA3082	CA3246
CA3083	▲CA3600
CA3084	
CA3086	
CA3093	

POWER CONTROL CIRCUITS

Voltage Regulators	Solenoid & Motor Drivers
CA723	CA3169
CA1524	CA3219
CA2524	
CA3085	Power Amplifiers
CA3524	CA3020
	CA3105
Zero-Voltage Switches	
CA3058	Automotive Ignition Switch
CA3059	CA3165
CA3079	
Programmable Schmitt Triggers	Universal Controller
CA3098	CA3228
CA3099	

DATA CONVERSION

A/D Converters	
CA3162	
CA3300	
CA3308	
Display Drivers	
CA3161	CA3081
CA3168	CA3082
CA3207*	
CA3208*	

VOLTAGE COMPARATORS

Single Unit
CA311
CA3098+
CA3099+
Dual Unit
CA3290*
Quad Unit
CA139
CA239
CA339

SPECIAL FUNCTION CIRCUITS

Timer	Automotive Circuits	Broadband (Video) Amplifiers
CA555	CA3105	CA080*
	CA3130*	CA081*
Four Quadrant Multiplier	CA3160*	CA082*
CA3091	CA3161	CA083*
	CA3165	CA084*
Single-Chip Detector Alarm	CA3168	CA3001
Systems	CA3169	CA3002
CA3164*	**CA3207***	CA3020
	CA3208*	CA3021
Prescalers	CA3219	CA3022
CA3179	CA3228	CA3023
CA3199	CA3260*	CA3040
CA3211	CA3290*	CA3071
		CA3100*
		CA3130*
		CA3140*
		CA3160*
		CA3240*
		CA3260*

MOS/FET's

Single Gate		Dual Gate		Dual Gate Protected	
3N128	3N153	3N140	40600	3N187	40673
3N138	3N154	3N141	40601	3N200	40819
3N139	40467A	3N159	40602	3N204	40820
3N142	40468A		40603	3N205	40821
3N143	40559A		40604	3N206	40822
3N152				3N211	40823
				3N212	40841
				3N213	

•Low-noise versions of CA741 and CA3078 *BiMOS types ▲CMOS types +Programmable

Product Classification Chart

Consumer Circuits

AUDIO CIRCUITS	RADIO CIRCUITS		MOS/FET's		
Drivers	AM/FM Com-	FM IF	Single Gate	Dual Gate	Dual Gate
CA3094	munications	Circuits	3N128	3N140	Protected
	Circuits	Gain Blocks	3N138	3N141	3N187
Power	CA3075	CA3076	3N139	3N159	3N200
Amplifiers	CA3076		3N142	40600	3N204
CA2002	CA3088	Subsystems	3N143	40601	3N205
CA2004	CA3089	CA3075	3N152	40602	3N206
	CA3123	CA3089	3N153	40603	3N211
Preamplifiers	CA3143	CA3189	3N154	40604	3N212
CA3036	CA3179	CA3209	40467A		3N213
CA3048	CA3189		40468A		40673
CA3052	CA3199		40559A		40819
	CA3209				40820
					40821
					40822
					40823
					40841

Operating and Handling Considerations

Solid state devices are being designed into an increasing variety of electronic equipment because of their high standards of reliability and performance. However, it is essential that equipment designers be mindful of good engineering practices in the use of these devices to achieve the desired performance.

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of linear integrated circuits and MOS field-effect transistors.

The ratings included in RCA data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

The design flexibility provided by integrated circuits and MOS/FET's makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of these devices provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

MOUNTING

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with gold or nickel plated Kovar leads.* It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress. The aluminum-foil-lined cardboard "sandwich pack" employed for static protection of the flat-pack also provides some additional protection against lead corrosion, and it is recommended that the devices be stored in this package until used.

When integrated circuits are welded onto printed circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

MOS FIELD-EFFECT TRANSISTORS

Insulated-Gate Metal Oxide-Semiconductor Field-Effect Transistors (MOS FETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in an MOS FET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applica-

* MIL-38510A, paragraph 3.5.6.1(a), lead material.

tions, with virtually no problems of damage due to electrostatic discharge.

In some MOS FETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOS FETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

*Trade Mark: Emerson and Cumming, Inc.

Operating and Handling Considerations

SOLID STATE CHIPS

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

Terms and Symbols

A	closed-loop voltage gain
A_{AF}	audio amplifier gain
A_{DIFF}	differential voltage gain
ACC	automatic chroma control
AFC	automatic frequency control
AFT	automatic fine tuning
AGC	automatic gain control
AMR	am rejection
A_{OL}	open-loop voltage gain
A_V	amplifier voltage gain
b_{fs}	small-signal, common-source, forward transfer susceptance (imaginary part of corresponding admittance; see y_{fs})
b_{is}	small-signal, common-source, input susceptance (imaginary part of corresponding admittance; see y_{is})
b_{os}	small-signal, common-source, output susceptance (imaginary part of corresponding admittance, see y_{os})
b_{rs}	small-signal, common-source, reverse transfer susceptance (imaginary part of corresponding admittance, see y_{rs})
BW	bandwidth (unity gain)
BW_{OL}	open-loop bandwidth
C_{BI}	base-to-substrate capacitance
C_{CB}	collector-to-base capacitance
C_{EB}	emitter-to-base capacitance
C_{EXT}	external capacitance
C_{FB}	feedback capacitance
C_I	input capacitance
C_{ios}	small-signal output capacitance
C_{is}	small-signal input capacitance
C_{iss}	small-signal, common-source short-circuit input capacitance
C_{I-O}	input-to-output capacitance; data in/out capacitance
CMMR	common-mode rejection ratio
C_O	output capacitance
C_{os}	feedthrough capacitance
C_{oss}	small-signal, common-source short-circuit output capacitance
C_{QP}	charge-pump capacitance
C_{rss}	small-signal, common-source short-circuit, reverse transfer capacitance
e_i	input sensitivity
E_N	I/F noise voltage
e_N	low-frequency noise voltage; equivalent short-circuit input noise voltage ($\mu V\sqrt{Hz}$)
$e_{N(total)}$	wideband noise voltage referenced to input
e_{O1}/e_{O2}	channel separation
E_{ON}	broadband output noise voltage
f_{CL}	clock input frequency
f_{max}	maximum operating frequency
f_p	charge-pump input-pulse frequency
f_t	unity-gain crossover frequency; gain-bandwidth product
f_ϕ	input-pulse frequency
G_p	power gain
G_m	forward transconductance (large-signal)
h_{FE}	static forward-current transfer ratio (beta)
h_{fe}	small-signal forward-current transfer ratio
I^+	dc supply current
I^-	dc supply current
I_A	amplifier supply current
I_{ABC}	amplifier bias current
I_{AGC}	AGC source current
I_B	base current
I_C	collector current
I_{CBO}	collector cutoff current
I_{CEO}	collector cutoff current
$I_{CE(OFF)}$	output leakage current
I_D	drain current
$I_{D(ON)}$	dc on-state drain current
I_{DARK}	dark current
I_{DF}	diode forward current
I_{DDO}	supply current for drain supply voltage (V_{DD})
I_{DS}	zero-gate (bias) drain current (dual-gate types)
I_{DSS}	zero-gate (bias) drain current (single-gate types)
I_F	forward current
I_G	channel (input) gate lead current
I_{GR}	channel (input) gate reverse current
I_{GS}	gate terminal current (single-gate types)
I_{G1S}	gate-No.1 terminal current dual-gate types
I_{G2S}	gate-No. 2 terminal current dual-gate types
I_{GSSF}	gate-to-source forward leakage current, all other terminals shorted to source (dual-gate types).
I_{G1SSF}	gate-No.1 source forward leakage current, all other terminals shorted to source (dual-gate types).
I_{G2SSF}	gate-No. 2-to-source forward leakage current, all other terminals shorted to source (dual-gate types).
I_{GSSR}	gate-to-source reverse leakage current, all other terminals shorted to source (single-gate types).
I_{G1SSR}	gate-No. 1-to-source reverse leakage current, all other terminals shorted to source (dual-gate types).
I_{G2SSR}	gate-No.2-to-source reverse leakage current, all other terminals shorted to source (dual-gate types).
I_{GT}	gate trigger current; gate terminal current
I_I	input current
I_{IB}	input bias current
I_{IBC}	internal bias current
I_{IO}	input offset current
αI_{IO}	average temperature coefficient of input offset current
$\Delta I_{IO}/\Delta T$	temperature coefficient of input offset current (drift)
I_{LIM}	short-circuit limiting current
I_{MTR}	current-mirror transfer ratio
I_N	I/F noise current
i_N	equivalent open-circuit noise current ($pA/\sqrt{Hz}$)
I_O	output current
$I_{O(DIFF)}$	differential output current (sink)
I_{OO}	output offset current
I_{OL}	output leakage current, low
I_{OM}	peak output current
$\lvert I_{OM}\rvert$	magnitude of peak output current
I_{OM}^+	maximum output current (source)
I_{OM}^-	maximum output current (sink)
I_p	photo current
I_{p-p}	peak-to-peak output current
I_Q	total quiescent current
I_{QPL}	charge-pump input current
I_R	dc reverse (leakage) current
I_{REFO}	supply current for reference supply voltage
I_{SSO}	strobe load current voltage (V_{SS})
I_{SXO}	supply current for supply voltage
I_{TH}	threshold current
I_{TOTAL}	total supply current
k_N	normalized factor ($k_N = k/k_r$)
MAG	maximum available power gain
MUG	maximum useable power gain (unneutralized)
NF	noise factor
P_O	power output
P_D	device dissipation
P_{SRR}	power supply rejection ratio
$r_{ds(off)}$	small-signal drain-to-source off-state resistance
$r_{ds(on)}$	static drain-to-source on-state resistance
R_{GS}	gate leakage-current resistance
R_O	output resistance
R_o	low-frequency output resistanc
r_o	small-signal output resistance
r_{oss}	small-signal, short-circuit, common-source output resistance
R_I	differential input resistance
r_i	small-signal input resistance
r_{iss}	small-signal, short-circuit, common-source input resistanc
R_i	low-frequency input resistance
R_{ON}	ON resistance; the ON-state resistance of an analog switch at specified input and load conditions.
ΔR_{ON}	ΔON resistance; the difference in ON-state resistance between any 2 analog switches at specified input and load conditions.
S/N	signal-to-noise ratio
SR	slew rate
T_A	ambient temperature
t_d	delay time
t_{DR}	differential recovery time
t_f	fall time
$t_{f\phi}$	input-pulse rise time
THD	total harmonic distortion
t_{off}	turn-off time
t_{on}	turn-on time
t_r	rise time
$t_{R\phi}$	input-pulse rise time
t_{rr}	reverse recovery time
t_S	setup time
t_{STG}	storage time
t_W	pulse width
V^+	DC positive supply voltage
V^-	DC negative supply voltage
V_{ABC}	amplifier bias voltage
V_{BB}	substrate voltage
V_{BE}	base-to-emitter voltage

Terms and Symbols

$V_{BE(sat)}$	base-to-emitter saturation voltage
$V_{(BR)CBO}$	collector-to-base breakdown voltage
$V_{(BR)CES}$	collector-to-emitter breakdown voltage
$V_{(BR)DI}$	dc breakdown voltage between diode and substrate
$V_{(BR)R}$	dc reverse breakdown voltage
$V_{(BR)EBO}$	emitter-to-base breakdown voltage
$V_{(BR)GSSF}$	dc gate-to-source forward breakdown voltage, all other terminals shorted to source (single-gate types)
$V_{(BR)G1SSF}$	dc gate-No.1-to-source forward breakdown voltage, all other terminals shorted to source (dual-gate types)
$V_{(BR)G2SSF}$	dc gate No.2-to-source forward breakdown voltage, all other terminals shorted to source (dual-gate types)
$V_{(BR)GSSR}$	dc gate-to-source reverse breakdown voltage, all other terminals shorted to source (single-gate types)
$V_{(BR)G2SSR}$	dc gate-No.2-to-source reverse breakdown voltage, all other terminals shorted to source (dual-gate types)
V_{CBO}	collector-to-base voltage
V_{CC}	drain supply voltage used as a second positive supply voltage. It is $\leqslant V_{DD}$ and referenced to V_{SS}
VCO	voltage controlled oscillator
V_{CEO}	collector-to-emitter voltage
$V_{CEO(sus)}$	collector-to-emitter sustaining voltage
V_{CIO}	collector-to-substrate voltage
V_{CP}	charge pump voltage
V_{DD}	drain supply voltage (the most positive supply voltage; always referenced to ground)
V_{DG}	drain-to-gate voltage (single-gate types)
V_{DG1}	drain-to-gate-No.1 voltage (dual-gate types)
V_{DG2}	drain-to-gate-No.2 voltage (single-gate types)
V_{DIO}	diode-to-substrate voltage
V_{DR}	diode reverse voltage
V_{DS}	drain-to-source voltage
V_{EE}	source voltage (the most negative supply voltage in a 3-supply voltage system)
V_F	dc forward voltage
$\Delta V_F/\Delta T$	temperature coefficient of forward voltage drop
V_{GH}	channel gate input voltage, high level
V_{GL}	channel gate input voltage, low level
V_{GS}	gate-to-source voltage
$V_{GS}(TH)$	gate-to-source threshold voltage
$V_{GS}(Off)$	gate-to-source cutoff voltage (single-gate types)
V_{G1S}	gate-No.1-to-source voltage (dual-gate type)
$V_{G1S}(Off)$	gate-No.1-to-source cutoff voltage (dual-gate types)
V_{G2S}	gate-No.2-to-source voltage (dual-gate types)
$V_{G2S}(off)$	gate-No.2-to-source cutoff voltage (dual-gate types)
V_I	input voltage
$V_{I(Lim)}$	input limiting voltage
V_{ICR}	common-mode input voltage range
V_{IL}	input-voltage, low level
V_{IH}	input-voltage, high level
V_{IO}	input offset voltage
$\lvert V_{IO}\rvert$	magnitude of input offset voltage
$\Delta V_{IO}/\Delta T$	temperature coefficient of magnitude of input offset voltage
$\Delta V_{IO}/\Delta T$	temperature coefficient of input offset voltage drift
$\Delta V_{IO}/\Delta V^+$	positive input-offset-voltage sensitivity
$\Delta V_{IO}/\Delta V^-$	negative input-offset-voltage sensitivity
αV_{IO}	average temperature coefficient of input-offset voltage
$V_{i(Lim)}$	input limiting voltage (knee)
V_{knee}	protective diode knee voltage (protected gate types)
V_N	output noise voltage
V_O	output voltage
$\Delta V_O/\Delta V^-$	dc supply voltage sensitivity
$\Delta V_O/\Delta V^+$	dc supply voltage sensitivity
$V_{O(rms)}$	open-loop output voltage swing
ΔV_O	output voltage temperature coefficient
$V_{Op\text{-}p}$	output voltage swing
$V_{O(af)}$	recovered af voltage
V_{OL}	output voltage, low level; the voltage level at an output when the input logic conditions have been set to establish logic LOW output.
V_{OO}	output offset voltage
V_{OH}	output voltage, high level; the voltage level at an output when the input logic conditions have been set to establish a logic HIGH output.
V_{OM}^+	maximum output voltage
V_{OM}^-	maximum output voltage
V_{QP}	charge pump voltage
V_{QPL}	charge pump input voltage, low level
V_{QPH}	charge-pump input voltage, high level
V_{REF}	reference voltage
V_{REG}	regulated supply voltage
V_{RR}	supply voltage rejection ratio
V_{TH}	input threshold voltage
V_Z	zener voltage
Y_{fs}	magnitude of small-signal, common-source, short-circuit forward transfer admittance (transadmittance)
Y_{is}	small-signal, common-source, short-circuit, input-admittance (conductance, real part of admittance; susceptance, imaginary part of admittance)
Y_{os}	small-signal, common-source, short-circuit, output admittance
$\lvert Y_{rs}\rvert$	magnitude of small-signal, common-source, short-circuit, reverse transadmittance
$<Y_{rs}$	phase angle of small-signal, common-source, short-circuit, reverse transadmittance
$(-)_{rs}$	angle of reverse transadmittance, common-source circuit
Z_1	input impedance
Z_O	output impedance
Z_Z	zener impedance
ϕ	phase angle
ϕ	phase margin
η	efficiency
ϕL	open-loop phase lag

Cross-Reference Directory for Linear Integrated Circuits

Industry Type	RCA Replacement Type
AD301AH	CA301AT,LM301AH
AD301AN	CA301AE,LM301AN
AD741H	CA741T,LM741H
AD741N	CA741E,LM741N
AD741CH	CA741CT,LM741CH
AD741CN	CA741CE,LM741CN
AD2020	CA3162E
AMLM301AH	CA301AT,LM301AH
AMLM301H	CA301T,LM301AH
AMLM307H	CA307T,LM307H
AMLM311H	CA311T,LM311H
AM723HC	CA723CT,LM723CH
AM723HM	CA723T,LM723H
AM741HC	CA741CT,LM741CH
AM741HM	CA741T,LM741H
AM747HC	CA747CT
AM747HM	CA747T
AM748HC	CA748CT, LM748CH
AM1458H	CA1458T,LM1458H
AM1558H	CA1558T,LM1558H
HA1-2630	CA3020
HA1-2650	LM1558A, CA1558E
HA1-2655	LM1458H, CA1458E
HA1-2720	CA6078
HA2-2311-5	CA311T,LM311H
HA2-2520	CA3100T
HA2-2650	CA1558T,LM1558H
HA2-2655	CA1458T,LM1458H
HA2-2720	CA3078E
ITT1352N	CA1352E
ITT3064C	CA3064T
ITT3064N	CA3064E
ITT3065N	CA3065E
LF156H	CA081T
LF356H	CA081CT
LF356J	CA081E
LM100	CA3085E
LM124N	CA124E
LM139J	CA139F
LM139AN	CA139AE
LM139AJ	CA139AF
LM139N	CA139E
LM158AH	CA158AT
LM158AN	CA158AE
LM158AT	CA158AT
LM158N	CA158E
LM158P	CA158E
LM158T	CA158T
LM201AN	CA201AE
LM201AP	CA201AE
LM201AV	CA201AE
LM201H	CA201T
LM201N	CA201E
LM201T	CA201T
LM224N	CA224E
LM239AD	CA239AF
LM239AF	CA239AF
LM239AJ	CA239AF
LM239AN	CA239AE
LM239D	CA239F
LM239F	CA239F
LM239J	CA239F
LM239N	CA239E
LM258AH	CA258AT
LM258AN	CA258AE
LM258AT	CA258AT
LM258H	CA258T
LM258L	CA258T
LM258N	CA258E
LM258P	CA258E
LM258T	CA258T
LM301AH	CA301AT,LM301AH
LM301AL	CA301AT,LM301AH
LM301AN	CA301AE,LM301AN
LM301AP	CA301AE,LM301AN
LM301AT	CA301AT,LM301AH
LM301AV	CA301AE,LM301AN
LM307H	CA307T,LM307H
LM307N	CA307E,LM307N
LM307T	CA307T,LM307H
LM311H	CA311T,LM311H
LM311L	CA311T,LM311H
LM311N	CA311E,LM311N
LM311P	CA311E,LM311N
LM311T	CA311T,LM311H
LM324N	CA324E,LM324N
LM339AJ	CA339AF
LM339AN	CA339AE,LM339AN
LM339D	CA339F
LM339F	CA339F
LM339J	CA339F
LM339N	CA339E,LM339N
LM358AH	CA358AT
LM358AN	CA358AE
LM358AT	CA358AT
LM358H	CA358T
LM358L	CA358T
LM358N	CA358E
LM358P	CA358E
LM358T	CA358T
LM393N	CA3290E
LM555CH	CA555CT,LM555CH
LM555CN	CA555CE,LM555CN
LM555H	CA555T
LM555N	CA555E,LM555N
LM723CH	CA723CT,LM723CH
LM723CN	CA723CE,LM723CN
LM723H	CA723T,LM723H
LM723N	CA723E,LM723N
LM741CH	CA741CT,LM741CH
LM741CN	CA741CE,LM741CN
LM741H	CA741T,LM741H
LM741N	CA741E,LM741N
LM746N	CA3072
LM747CH	CA747CT
LM747CN	CA747CE
LM747H	CA747T
LM748CH	CA748CT,LM748CH
LM748CN	CA748CE,LM748CN
LM748H	CA748T,LM748H
LM1310N	CA1310E
LM1391N	CA1391E
LM1394N	CA1394E
LM1458H	CA1458T,LM1458H
LM1458N	CA1458E,LM1458N
LM1558H	CA1558T,LM1558H
LM1558N	CA1558E
LM1800N	CA758E
LM1820N	CA3123E
LM1845N	CA3120E
LM2111N	CA2111AE
LM2901J	CA2901F
LM2901N	LM2901N
LM2902N	LM2902N
LM2904N	CA2904E,LM2904N
LM2904P	CA2904E,LM2904N
LM3011H	CA3011
LM3018H	CA3018
LM3018AH	CA3018A
LM3019H	CA3019
LM3026H	CA3026
LM3028AH	CA3028A
LM3028B	CA3028B
LM3039H	CA3039
LM3045D	CA3045,CA3045F
LM3046N	CA3046
LM3053H	CA3053
LM3054N	CA3054
LM3064H	CA3064
LM3064N	CA3064E
LM3065N	CA3065
LM3066N	CA3066
LM3067N	CA3067
LM3070N	CA3070
LM3071N	CA3071
LM3075N	CA3075
LM3086N	CA3086
LM3089N	CA3089E, CA3189E
LM3126N	CA3126E
LM3146AN	CA3146AE
LM3302J	LM3302F
LM3302	LM3302N
LM3401N	CA3401E
M5141T	CA741CT,LM741CH
MC1310P	CA1310E
MC1352P	CA1352E
MC1357P	CA2111AE
MC1357PQ	CA2111AQ
MC1358P	CA3065
MC1364G	CA3064T
MC1364P	CA3064E
MC1370P	CA3070
MC1371P	CA3071
MC1375P	CA3075
MC1389P	CA3089E, CA3189E
MC1391P	CA1391E
MC1394P	CA1394E
MC1398P	CA1398E
MC1455G	CA555CT,LM555CH
MC1455P1	CA555CE,LM555CN
MC1458G	CA1458T,LM1458H
MC1458P1	CA1458E,LM1458N
MC1458T	CA1458T,LM1458H
MC1555G	CA555T
MC1555P1	CA555CE,LM555CN
MC1558G	CA1558T,LM1558H
MC1558P1	CA1558E
MC1558T	CA1558T,LM1558H
MC1723CG	CA723CT,LM723CH
MC1723CP	CA723CE,LM723CN
MC1723G	CA723T,LM723H
MC1741CG	CA741CT,LM741CH
MC1741CP1	CA741CE, LM741CN
MC1741G	CA741T,LM741H

Cross-Reference Directory for Linear Integrated Circuits

Industry Type	RCA Replacement Type
MC1747CG	CA747CT
MC1747G	CA747T
MC1748CG	CA748CT,LM748CH
MC1748CP1	CA748CE,LM748CN
MC1748G	CA748T,LM748H
MC3346P	CA3046
MC3386P	CA3086
MC34001BP	CA081AE
MC34001P	CA081E
MC34002BP	CA082AE
MC34002P	CA082E
MC3401P	CA3401E
NE555P	CA555CE,LM555CN
NE555L	CA555CT,LM555CH
NE555T	CA555CT,LM555CH
NE555V	CA555CE,LM555CN
PM741J	CA741T,LM741H
PM741CJ	CA741CT,LM741CH
PM747K	CA747T
PM747CK	CA747CT
RC555NB	CA555CE,LM555CN
RC555T	CA555CT,LM555CH
RC723CN	LM723CN
RC723DB	CA723CE,LM723CN
RC723T	CA723CT,LM723CH
RC1458NB	CA1458E,LM1458N
RC1458T	CA1458T,LM1458T
RC3401DB	CA3401E
RC741DB	CA741CE,LM741CN
RC741NB	CA741CE,LM741CN
RC741T	CA741T,LM741H
RC747DB	CA747CE
RC747T	CA747T
RM555T	CA555T,LM555H
RM723T	CA723T, LM723H
RM741T	CA741T,LM741H
RM747T	CA747T
RM1558T	CA1558T, LM1558H
SE555L	CA555T
SE555N	CA555E
SE555P	CA555E
SE555T	CA555T
SFC2301A	CA301AT,LM301AH
SFC2301ADC	CA301AE,LM301AN
SFC2307	CA307T,LM307H
SFC2311	CA311T,LM311H
SFC2741C	CA741CT,LM741CH
SFC2741M	CA741T,LM741H
SFC2748DC	CA748CE,LM748CN
SFC2748C	CA748CT,LM748CH
SG301AN	CA301AE,LM301AN
SG301AT	CA301AT,LM301AH
SG307N	CA307E,LM307N
SG307T	CA307T,LM307H
SG311M	CA311E,LM311N
SG311T	CA311T,LM311H
SG723CN	CA723CE,LM723CN
SG723CT	CA723CT,LM723CH
SG723T	CA723T,LM723H
SG741CN	CA741CE,LM741CN
SG741CT	CA741CT,LM741CH
SG741T	CA741T,LM741H
SG747CN	CA747CE
SG747CT	CA747CT
SG747T	CA747T
SG748CN	CA748CE,LM748CN
SG748CT	CA748CT,LM748CH

Industry Type	RCA Replacement Type
SG748T	CA748T,LM748H
SG1458M	CA1458E,LM1458N
SG1458T	CA1458T,LM1458H
SG1558T	CA1558T
SG2524N	CA2524E
SG3018T	CA3018
SG3018AT	CA3018A
SG3058J	CA3058
SG3059J	CA3059
SG3079J	CA3079
SG3081N	CA3081
SG3081J	CA3081F
SG3082N	CA3082
SG3082J	CA3082F
SG3083J	CA3083F
SG3401N	CA3401E
SG3524N	CA3524E
SN76115N	CA1310E
SN76116N	CA758E
SN76242N	CA3070
SN76243AN	CA3071
SN76264N	CA3072
SN76267N	CA3067
SN76298N	CA1398E
SN76564N	CA3064
SN76565N	CA3064E
SN76635N	CA3123E
SN76650N	CA1352E
SN76666N	CA3065
SN76675N	CA3075
SN76676P	CA3076
SN76689N	CA3089E, CA3189E
SSS301AJ	CA301AT,LM301AH
SSS301AP	CA301AE,LM301AN
SSS741CJ	CA741CT,LM741CH
SSS1458J	CA1458T,LM1458H
SSS1558J	CA1558T,LM1558H
TDA2002V	CA2002
TDA2002H	CA2002M
TBB0747	CA747CT
TBB0748	CA748CT,LM748CH
TBB0748B	CA748CE,LM748CN
TBB1458B	CA1458E,LM1458N
TBC0747	CA747T
TCA270	CA270
TDA3081N	CA3081
TDA3082N	CA3082
TDA3083N	CA3083
TDA7607	CA7607E
TDA7611	CA7611E
TDB0723	CA723CT,LM723CH
TDB0723A	CA723CE,LM723CN
TDC0723	CA723T,LM723H
TL080ML	CA080T
TL080AML	CA080AT
TL080CL	CA080CT
TL080CP	CA080E
TL080ACP	CA080AE, CA080BE
TL081ML	CA081T
TL081AML	CA081AT
TL081CL	CA081CT
TL081CP	CA081E
TL081ACP	CA081AE
TL081BCP	CA081BE
TL082ML	CA082T
TL082	CA082CT

Industry Type	RCA Replacement Type
TL082CP	CA082E
TL082ACP	CA082AE
TL082BCP	CA082BE
TL083CN	CA083E
TL083ACN	CA083AE
TL084ACN	CA084AE
TL084CN	CA084E
TL084BCN	CA084BE
U5B7741312	CA741T,LM741H
U5B7741393	CA741CT,LM741CH
U5B7748312	CA748T,LM748H
U5B7748393	CA748CT,LM748CH
U5R7723312	CA723T,LM723H
U5R7723393	CA723CT
U6A7723393	CA723CE,LM723CN
U9T7741393	CA741CE,LM741CN
ULN2111A	CA2111AE
ULN2111N	CA2111AQ
ULN2114A	CA3072
ULN2124A	CA3070
ULN2125A	CA3120E
ULN2127A	CA3071
ULN2129A	CA3075
ULN2137A	CA3123E
ULN2165A	CA3065
ULN2210A	CA1310E
ULN2212B	CA3012
ULN2262A	CA3126Q
ULN2264A	CA3064
ULN2267A	CA3067
ULN2269A	CA3121E
ULN2289A	CA3089E, CA3189E
ULN2298A	CA1398E
ULX2244A	CA758E
μA301AH	CA301AT,LM301AH
μA307H	CA307T,LM307H
μA307T	CA307E,LM307N
μA301AT	CA301AE,LM301AN
μA311H	CA311T, LM311H
μA311T	CA311E,LM311N
μA555HC	CA555CT,LM555CH
μA555HM	CA555T
μA555TC	CA555CE,LM555CN
μA720PC	CA3123E
μA723CA	CA723CE,LM723CN
μA723CL	CA723CT,LM723CH
μA723CN	CA723CE,LM723CN
μA723HC	CA723CT,LM723CH
μA723HM	CA723T,LM723H
μA723MN	CA723E,LM723N
μA723ML	CA723T,LM723H
μA723PC	CA723CE,LM723CN
μA741CN	CA741CE,LM741CN
μA741CL	CA741CT,LM741CH
μA741CP	CA741CE,LM741CN
μA741CT	CA741CE,LM741CN
μA741HC	CA741CT,LM741CH
μA741HM	CA741T,LM741H
μA741ML	CA741T,LM741H
μA741MN	CA741E,LM741N
μA741MP	CA741E,LM741N
μA741PC	CA741CE,LM741CN
μA746PC	CA3072
μA747CA	CA747CE
μA747CL	CA747CT
μA747CN	CA747CE

Cross-Reference Directory for Linear Integrated Circuits

Industry Type	RCA Replacement Type
μA747HC	CA747CT
μA747HM	CA747T
μA747ML	CA747T
μA747MN	CA747E
μA747PC	CA747CE
μA747A	CA747E
μA748CL	CA748CT,LM748CH
μA748CN	CA748CE,LM748CN
μA748CP	CA748CE,LM748CN
μA748CT	CA748CT,LM748CH
μA748HC	CA748CT,LM748CH
μA748HM	CA748T,LM748H
μA748ML	CA748T,LM748H
μA748MN	CA748E,LM748N
μA748MP	CA748E,LM748N
μA748T	CA748E,LM748N
μA748TC	CA748CE,LM748CN
μA758PC	CA758E
μA780PC	CA3070
μA781PC	CA3071
μA787PC	CA3126Q
μA1391T	CA1391E
μA1394T	CA1394E
μA1458HC	CA1458T,LM1458H
μA1458TC	CA1458E,LM1458N
μA1558HM	CA1558T
μA3018HM	CA3018
μA3018AHM	CA3018A

Industry Type	RCA Replacement Type
μA3019HM	CA3019
μA3026HM	CA3026
μA3036HM	CA3036
μA3039HM	CA3039
μA3045DM	CA3045,CA3045F
μA3046DC	CA3046
μA3054PC	CA3054
μA3064HC	CA3064
μA3064PC	CA3064E
μA3065PC	CA3065
μA3066PC	CA3066
μA3075PC	CA3075
μA3086DC	CA3086F
μA3089E	CA3089E, CA3189E
μA3401P	CA3401E
μPC151A	CA741CT,LM741CH
μPC151C	CA741CE,LM741CN
μPC157A	CA301AT,LM301AH
μPC157C	CA301AE,LM301AN
μPC251A	CA747CT
μPC251C	CA747CE
μPC301AC	CA301AE,LM301AN
μPC311C	CA311E,LM311N
μPC324C	CA324E,LM324N
μPC339C	CA339E,LM339N
μPC741C	CA741CE,LM741CN
μPC1458C	CA1458E,LM1458N

LM Branded Linear IC's

RCA supplies the following Linear IC's branded with the industry standard "LM" Brand. Technical Data on LM Branded types is identical to the corresponding CA Branded types. See chart below.

Type	Equivalent CA Type	Data Bulletin File No.	Page
LM1458H	CA1458T	531	38
LM1458N	CA1458E	531	38
LM1558H	CA1558T	531	38
LM201H	CA201T	786	28
LM2901N	*		
LM2902N	*		
LM2904N	CA2904E	1019	38
LM301AH	CA301AT	786	28
LM301AN	CA301AE	786	28
LM307H	CA307T	785	34
LM307N	CA307E	785	34
LM311H	CA311T	797	270
LM311N	CA311E	797	270
LM324N	CA324E	796	104
LM3302N	*		
LM339AN	CA339AE	795	301

Type	Equivalent CA Type	Data Bulletin File No.	Page
LM339N	CA339E	795	301
LM358N	CA358E	1019	98
LM555CH	CA555CT	834	653
LM555CN	CA555CE	834	653
LM723CH	CA723CT	788	520
LM723CN	CA723CE	788	520
LM723H	CA723T	788	520
LM723N	CA723E	788	520
LM741CH	CA741CT	531	38
LM741CN	CA741CE	531	38
LM741H	CA741T	531	38
LM741N	CA741E	531	38
LM748CH	CA748CT	531	38
LM748CN	CA748CE	531	38
LM748H	CA748T	531	38
LM748N	CA748E	531	38

*No CA Branded part type conforms to industry standard data

The EVP option

For systems designers, the key to cost-effective device procurement is often found in determining the right level of reliability. How much reliability? At what cost?

For semiconductor manufacturer and user alike, the answer has always been the same. As much reliability as the application requires at the lowest practical cost.

The screening programs of RCA employ this philosophy to achieve Linear IC reliability goals in both standard product and military high-reliability product.

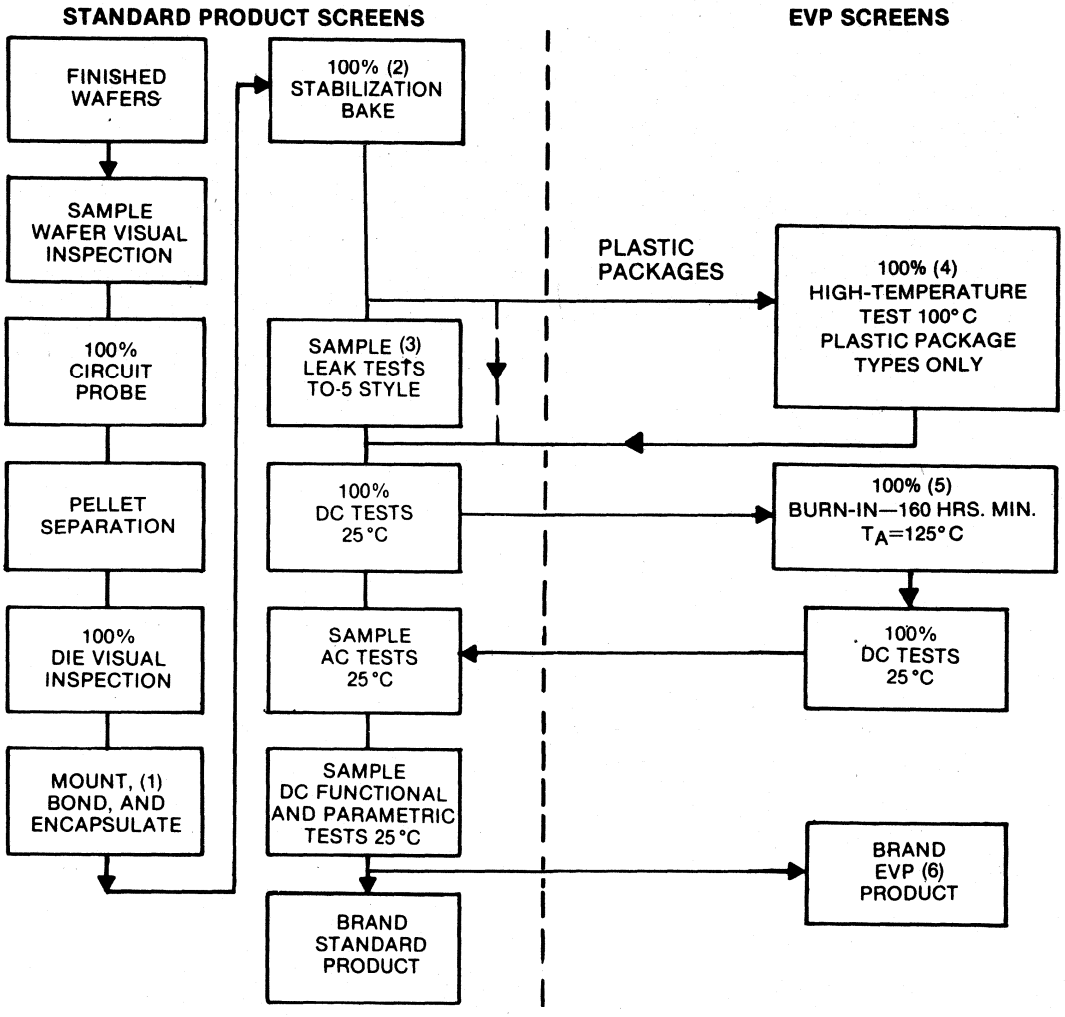
As both integrated circuits and their application become more complex, an increasing number of linear IC users find the cost-effective answer to reliability requirements in a new level of reliability screening. One which for the intended use, is more effective than standard product but does not involve the higher costs required to achieve military reliability levels.

This new cost-effective approach to enhanced commercial reliability is provided by the RCA Extra Value Program.

The Extra Value Program adds a burn-in and additional testing to the comprehensive real-time controls and test procedures carried out on standard plastic and TO-5-style product. The enhanced product of the Extra Value Program achieves AQL levels as shown in the chart below.

TEST	EVP PRODUCT
100% High-Temperature Continuity or Functional Test at 100 °C	Plastic-package types only
Sample Leak Test	TO-5-style package types only; Gross leak rate = $1x10^{-5}$ Atm.cc/sec. max.; Fine leak rate = $5x10^{-8}$ Atm.cc/sec. max.
100% Burn-In	160 Hrs. Min. at 125 °C per MIL-STD-883A Method 1015.1
AQL DC Parametric Tests	0.25% Max.
AQL DC Functional Tests	0.15% Max.
Marking	Standard Part No. with Blue Dot

PROCESS FLOW CHART



(1) Epoxy mount and cure; ultrasonic aluminum wire bond on TO-5-style or thermosonic gold-wire bond on plastic types; encapsulate in TO-5-style or plastic dual-in-line package.

(2) Stabilization bake 6 hours at 175 °C for plastic-package types, 16 hours at 200 °C for TO-5-style types.

(3) Gross leak rate of $1x10^{-5}$ Atm.cc/sec max. and fine leak rate of $5x10^{-8}$ Atm.cc/sec max.

(4) High-temperature (i.e., heat-pipe, hot-rail) test
   (a) automatic test for continuity on each terminal at 100 °C for array types.
   (b) continuity or functional gain test at 100 °C for op-amps, comparators, and voltage regulators.

(5) 100% dc test before and after burn-in per MIL-STD-883A Method 1015.1

(6) Brand EVP product surviving both Enhancement Screens with Standard Type Number plus blue dot.

The extra value of burn-in

Quality relates to the percentage of defective units at "time zero". It is a measure of devices dead-on-arrival (DOA). While the total absence of even a single defective unit in any lot of devices received from the semiconductor manufacturer may be the ideal goal, it is an impractical one.

Testing experience and a complete understanding of failure mechanisms tell us that every increment of improvement over the standard 0.65% AQL carries a price tag which becomes disproportionately high relative to the number of line rejects it will eliminate.

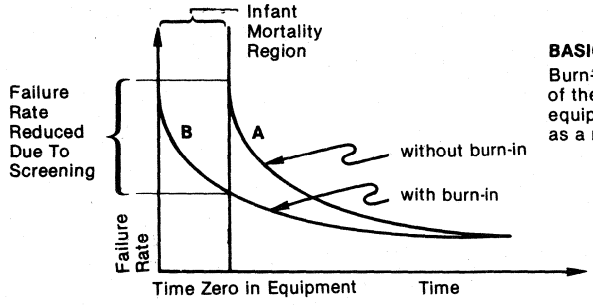
Application experience shows that the simple reduction of AQL does in no way guarantee an improvement in field-failure rates.

Reliability, in contrast to the zero-time aspects of quality, is a measure of the maintenance of quality through time in actual system environment.

Component burn-in is effective in screening out temperature- and time-dependent mechanisms that would normally escape detection under a 100% final electrical test.

Thus, the Extra Value Program offers greater cost effectiveness in achieving field reliability than any program which relies solely on reduced outgoing or incoming inspection levels.

The basic theory of burn-in and the type of improvement which can be expected through reduced device infant mortality is depicted in the chart below.



BASIC THEORY OF SCREENING

Burn-in and screening eliminate a major percentage of the infant mortality. Component life in equipment is translated from curve A to curve B as a result of burn-in

EVP SCREENING	ORDERING INFORMATION		
	Package Type	Standard Type No.	Extra Value Type No.
Burn-In Time — 160 Hrs. Min. Burn-In Temperature — 125 °C Hot Continuity Test Temperature — 100 °C	Plastic Dual-In-Line	CA741E	CA741EX
	TO-5 Style	CA3140T	CA3140TX

Operational Amplifiers
Technical Data

General Purpose

General Purpose Wideband

Variable

*BiMOS types
•Low-noise versions of CA741 and CA3078

Op Amp, Comparator, and OTA

Selection Chart ..... Pages 24 — 27

Op-Amp, Comparator, and OTA Selection Chart

Type #	Description	Basic Ratings			Input Characteristics @ 25°C				
		Compens. Internal External	V^+, V^- Max. V	I_S Max. nA	V_{IO} Max. mV	I_B Max. nA	I_{IO} Max. nA	V_{ICR} (Plus) V	V_{ICR} (Minus) V
CA080E	Single BiMOS Op-Amp with High Slew Rate	E	±18	2.8	15	.050	.030	10	10
CA080T-S		E	±18	2.8	6	.040	.020	12	12
CA080AE		E	±18	2.8	6	.040	.020	12	12
CA080AT-S		E	±18	2.8	3	.040	.020	12	12
CA080BE		E	±18	2.8	3	.030	.010	12	12
CA080CT-S		E	±18	2.8	15	.050	.030	10	10
CA081E	Single BiMOS Op-Amp with High Slew Rate	I, E	±18	2.8	15	.050	.030	10	10
CA081T-S		I, E	±18	2.8	6	.040	.020	12	12
CA081AE		I, E	±18	2.8	6	.040	.020	12	12
CA081AT-S		I, E	±18	2.8	3	.040	.020	12	12
CA081BE		I, E	±18	2.8	3	.030	.010	12	12
CA081CT-S		I, E	±18	2.8	15	.050	.030	10	10
CA082E	Dual BiMOS Op-Amp with High Slew Rate	I	±18	5.6	15	.050	.030	10	10
CA082T-S		I	±18	5.6	6	.040	.020	12	12
CA082AE		I	±18	5.6	6	.040	.020	12	12
CA082AT-S		I	±18	5.6	3	.040	.020	12	12
CA082BE		I	±18	5.6	3	.030	.010	12	12
CA082CT-S		I	±18	5.6	15	.050	.030	10	10
CA083E	Dual BiMOS Op-Amp with High Slew Rate	I	±18	5.6	15	.050	.030	10	10
CA083AE		I	±18	5.6	6	.040	.020	12	12
CA083BE		I	±18	5.6	3	.030	.010	12	12
CA084E	Quad BiMOS Op-Amp with High Slew Rate	I	±18	11.2	15	.050	.030	10	10
CA084AE		I	±18	11.2	6	.040	.020	12	12
CA084BE		I	±18	11.2	3	.030	.010	12	12
CA101	General Purpose Op-Amp	E	±22	3.0	5.0	500	200	12	12
CA124[11]	Quad Op-Amp	I	±16	8	5	150	30	V^+–1.5	0
CA139[11]	Quad Volt Comparator	NA	±18	8	5	100	25	V^+–1.5	0
CA139A[11]	Quad Volt-Comparator	NA	±18	8	2	100	25	V^+–1.5	0
CA158[11]	Dual Op-Amp-General Purpose	E	±16	3	5	150	30	V^+–1.5	0
CA158A[11]	Dual Op-Amp-General Purpose	E	±16	3	2	50	10	V^+–1.5	0
CA201	General Purpose Op-Amp	E	±22	3	7.5	1,500	500	12	12
CA224[11]	Quad Op Amp	I	±16	8	7	250	50	V^+–1.5	0
CA239[11]	Quad Volt Comparator	NA	±18	8	5	250	50	V^+–1.5	0
CA258[11]	Dual Op-Amp-General Purpose	E	±16	3	5	150	30	V^+–1.5	0
CA258A[11]	Dual Op-Amp-General Purpose	E	±16	3	3	80	15	V^+–1.5	0
CA301A	General Purpose Op-Amp	E	±18	3	7.5	250	50	12	12
CA307	General Purpose Op-Amp	I	±18	3	7.5	300	50	12	12
CA311	Single Volt Comparator	NA	±18	8	7.5	250	50	14	14
CA324[11]	Quad Op-Amp	I	±16	8	7	250	50	V^+–1.5	0
CA339[11]	Quad Voltage Comparator	NA	±18	8	5	250	50	V^+–1.5	0
CA339A[11]	Quad Voltage Comparator	NA	±18	8	2	250	50	V^+–1.5	0
CA358[11]	Dual Op-Amp General Purpose	E	±16	3	7	250	50	V^+–1.5	0
CA358A[11]	Dual Op-Amp General Purpose	E	±16	3	3	100	30	V^+–1.5	0
CA741	Single-General Purpose Op-Amp	I	±22	2.8	5	500	200	12	12
CA741C	Single-General Purpose Op-Amp	I	±18	2.8	6	500	200	12	12
CA747	Dual 741	I	±22	5.6	5	500	200	12	12
CA747C	Dual 741	I	±18	5.6	6	500	200	12	12
CA748	Single-General Purpose Op-Amp	E	±22	2.8	5	500	200	12	12
CA748C	Single-General Purpose Op-Amp	E	±18	2.8	6	500	200	12	12
CA1458	Dual 748	I	±18	5.6	6	500	200	12	12
CA1558	Dual 748	I	±22	5.6	5	500	200	12	12
CA3008	General Purpose Op-Amp	E	±8	9	5	12,000	5,000	.50	4
CA3008A	General Purpose Op-Amp	E	±8	9	2	4,000	1,500	.50	4
CA3010	General Purpose Op-Amp	E	±8	9	5	12,000	5,000	.50	4
CA3010A	General Purpose Op-Amp	E	±8	9	2	4,000	5,000	.50	4
CA3015	General Purpose Op-Amp	E	±16	21	5	24,000	5,000	.65	8
CA3016	General Purpose Op-Amp	E	±16	21	5	24,000	5,000	.65	8
CA3029	General Purpose Op-Amp	E	±8	9	5	12,000	5,000	.50	4
CA3029A	General Purpose Op-Amp	E	±8	9	2	4,000	1,500	.50	4
CA3030	General Purpose Op-Amp	E	±16	21	5	24,000	5,000	.65	8
CA3030A	General Purpose Op-Amp	E	±16	21	2	6,000	1,600	.65	8
CA3037	General Purpose Op-Amp	E	±8	9	5	12,000	5,000	.50	4
CA3037A	General Purpose Op-Amp	E	±16	9	2	4,000	1,500	.50	4
CA3038	General Purpose Op-Amp	E	±16	21	5	24,000	5,000	.65	8
CA3038A	General Purpose Op-Amp	E	±16	21	2	6,000	1,600	.65	8
CA3060D	OTA - Triple Amplifier and Array	E	±7	3.6	5	5,000	1,000	4.3	5
CA3060AD		E	±18	3.6	5	5,000	1,000	12	12
CA3060BD	I_{ABC} = 100 μA	E	±18	3.6	5	5,000	1,000	12	12
CA3060E	I_{ABC} = 100 μA	E	±18	3.6	5	5,000	1,000	12	12

Output Characteristics				AC Characteristics @ 25°C			Package Characteristics[4]		Page #
V_{OUT} +[5] Min. V	V_{OUT}−[5] Min. V	R_L for V_{OUT} OHMS	AOL[1] Min V/V	BW[2] Typ MHz	Slew Rate[2] Typ V/μs	Temp[3] Range IMC	Plastic Ceramic	TO5 Metal CAN	
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C	8E		
24 V_{pp}	24 V_{pp}	10K	50K	5	13	M		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	8E		83
24 V_{pp}	24 V_{pp}	10K	50K	5	13	M	8E		
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C	8E		
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	50K	5	13	M		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	8E		83
24 V_{pp}	24 V_{pp}	10K	50K	5	13	M		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	8E		
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C	8E		
24 V_{pp}	24 V_{pp}	10K	50K	5	13	M		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	8E		83
24 V_{pp}	24 V_{pp}	10K	50K	5	13	M		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	8E		
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C	14E		
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	14E		83
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	14E		
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C	14E		
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	14E		83
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	14E		
10	10	2K	50K	1.0	10 non comp	M	8E	8T, 8S	28
V^+−1.5V	0	2K	50K	1.0	.5	M	14E		104
V_{SAT} = .5V		5.1K	50K	t_r = 300 ns	t_f = 1.3 μs	M	14E		301
V_{SAT} = .5V		5.1K	50K	t_r = 300 ns	t_f = 1.3 μs	M	14E		
V^+−1.5V	0	2K	50K	1.0	.5	M	8E	8T, 8S	93
V^+−1.5V	0	2K	50K	1.0	.5	M	8E	8T, 8S	
+10	+10	2K	20K	1.0	10 non comp	C	8E	8T, 8S	28
V^+−1.5V	0	2K	25K	1.0	.5	I	14E		104
V_{SAT} = .5V		2K	50K	t_r = 300 ns	t_f = 1.3 μs	I	14E		301
V^+−1.5V	0	2K	50K	1.0	.5	I	8E	8T, 8S	93
V^+−1.5V	0	2K	50K	1.0	.5	I	8E	8T, 8S	
+10	−10	2K	25K	1.0	10 non comp	C	8E	8T, 8S	28
+10	−10	2K	25K	2	.5	C	8E	8T, 8S	34
V_{SAT} = 1.5V		5K	200K	Response time 200 ns		C	8E	8T, 8S	270
V^+−1.5V	0	2K	25K	1.0	.5	C	14E		104
V_{SAT} = .5V		2K	50K	t_r = 300 ns	t_f = 1.3 μs	C	14E		301
V_{SAT} = .5V		2K	50K	t_r = 300 ns	t_f = 1.3 μs	C	14E		
V^+−1.5V	0	2K	25K	1.0	.5	C	8E	8T, 8S	93
V^+−1.5V	0	2K	25K	1.0	.5	C	8E	8T, 8S	
10	−10	2K	50K	1.0	.5	M	8E	8T, 8S	38
10	−10	2K	20K	1.0	.5	C	8E	8T, 8S	
10	−10	2K	50K	1.0	.5	M	14E	10T	38
10	−10	2K	20K	1.0	.5	C	14E	10T	
10	−10	2K	50K	1.0	.5	M	8E	8T, 8S	38
10	−10	2K	20K	1.0	.5	C	8E	8T, 8S	
10	−10	2K	20K	1.0	.5	C	8E	8T, 8S	38
10	−10	2K	50K	1.0	.5	M	8E	8T, 8S	38
2	−2	2K	.7K	.20[10]	3	M	14K		114
2	−2	2K	.7K	.20[10]	3	M	14K		121
2	−2	2K	.7K	.20[10]	3	M		12T	114
2	−2	2K	.7K	.20[10]	3	M		12T	121
6	−6	2K	2K	.20[10]	3	M		12T	114
6	−6	2K	2K	.20[10]	3	M	14K		114
2	−2	2K	.7K	.20[10]	7	M	14E		114
2	−2	2K	.7K	.20[10]	7	C	14E		121
6	−6	2K	2K	.20[10]	3	C	14E		114
6	−6	2K	2K	.20[10]	3	C	14E		121
2	−2	2K	.7K	.20[10]	7	C	14D		114
2	−2	2K	.7K	.20[10]	7	M	14D		121
6	−6	2K	2K	.20[10]	3	M	14D		114
6	−6	2K	2K	.20[10]	3	M	14D		121
4.6	−5.8	∞	gm=30μmho	.110	8	M	16D		
12	−12	∞	gm=30μmho	.110	8	M	16D		224
12	−12	∞	gm=30μmho	.110	8	M	16D		
12	−12	∞	gm=30μmho	.110	8	I	16E		

Op-Amp, Comparator, and OTA Selection Chart

Type #	Description	Basic Ratings			Input Characteristics @ 25°C				
		Compens. Internal External	V^+, V^- Max. V	I_S Max. nA	V_{IO} Max. mV	I_B Max. nA	I_{IO} Max. nA	V_{ICR} (Plus) V	V_{ICR} (Minus) V
CA3078	Micropower Op Amp	E	±7	.130	4.5	170	32	5	5
CA3078A	Micropower Op-Amp	E	±18	.025	3.5	12	2.5	5	5
CA3080	High Slew Rate OTA	E	±18	1.2	5	5,000	600	12	12
CA3080A	High Slew Rate OTA	E	±18	1.2	2	5,000	600	12	12
CA3094	Programmable	E	±12	.4	5	5,000	2,000	12	14
CA3094A	Power Switch/Amplifier	E	±18	.4	5	5,000	2,000	12	14
CA3094B	(OTA)	E	±22	.4	5	5,000	2,000	12	14
CA3100	Wideband BiMOS Op-Amp	E, I	±18	10.5	5	2,000	400	12	12
CA3130[11]	BiMOS Op-Amp with	E	±8	15	15	.050	.030	10	0
CA3130A[11]	MOS Input and	E	±8	15	5	.030	.020	10	0
CA3130B[11]	MOS Output	E	±8	15	2	.020	.010	10	0
CA3140	BiMOS Op-Amp with	I	±18	6	15	.050	.030	11	15
CA3140A	MOS Input and	I	±18	6	5	.030	.020	12	15
CA3140B	Bipolar Output	I	±22	6	2	.020	.010	12	15
CA3160[11]	BiMOS Op-Amp with	I, E	±8	15	15	.050	.030	10	0
CA3160A[11]	MOS Input and	I, E	±8	15	5	.030	.020	10	0
CA3160B[11]	MOS Output	I, E	±8	15	2	.020	.010	10	0
CA3193[8]	Precision - 5μV/°C, Neg. Null	I	±18	3.5	.500	40	10	10	12
CA3193A[8]	Precision - 3μV/°C, Neg. Null	I	±18	3.5	.200	20	5	10	12
CA3193B[8]	Precision — 2 μV/°C Neg. Null	I	±22	3.5	.075	15	3	10	12
CA3240	Dual BiMOS Op-Amp	I	±18	12	15	.050	.030	11	15
CA3240A	With MOS Input and Bipolar Output	I	±18	12	5	.040	.020	12	15
CA3260[11]	Dual BiMOS Op Amp	I	±8	15.5	15	.050	.030	10	0
CA3260A[11]	With MOS Input	I	±8	15.5	5	.030	.020	10	0
CA3260B[11]	and MOS Output	I	±8	15.5	2	.020	.010	10	0
CA3280[12]	Dual OTA	E	±18	4.8	3.0	5,000	700	13	13
CA3280A[12]	Dual OTA	E	±18	4.8	0.5	5,000	700	13	13
CA3290	Dual BiMOS	NA	±18	3	20	.050	.030	V^+–3.8V	V^-
CA3290A	Comparator with	NA	±18	3	10	.040	.025	V^+–3.8V	V^-
CA3290B	MOS Input & Bipolar Output	NA	±22	3	6	.030	.020	V^+–3.8V	V^-
CA3401	Quad Single Supply Op-Amp (Norton)	I	±18	14	NA	300	NA	NA	NA
CA3420	Low-Supply Voltage	I	±11	.550	10	.003	.0020	NS	NS
CA3420A	Low Current BiMOS	I	±11	.550	5	.003	.0020	.2	1.0
CA3420B	Op-Amp (±1V Operation)	I	±11	.550	2	.001	.0007	.2	1.0
CA3420	Low-Supply Voltage	I	±11	.700	10	.003	.0020	8.5	10
CA3420A	Low-Current BiMOS	I	±11	.700	5	.003	.0020	9.0	10
CA3420B	Op-Amp (±10V Operation)	I	±11	.700	2	.001	.0007	9.0	10
CA3440[7]	Nano Power	I	±12.5	.017	10	.050	.030	3.5	5.0
CA3440A[7]	BiMOS Op-Amps	I	±12.5	.017	5	.040	.020	3.5	5.0
CA3440B[7]		I	±12.5	.017	2	.030	.010	3.5	5.0
CA3493[8]	Precision - 5μV/°C - Pos. Null	I	±18	3.5	.500	40	10	10	12
CA3493A[8]	Precision - 3 μV°C - Pos. Null	I	±18	3.5	.200	20	5	10	12
CA3493B[8]	Precision - 2 μV/°C - Pos. Null	I	±22	3.5	.075	15	3	10	12
CA6078A[9, 10]	Low Burst Noise Micropower Op-Amp	E	±18	.025	3.5	12	3.5	14	14
CA6741[9]	Low Burst Noise General Purpose Op-Amp	I	±22	2.8	5.0	500	200	12	12

NOTES:

1. A_{OL} value is for a load resistor as specified in the output characteristics chart. If the load is different it will be displayed under the A_{OL} value.
   For OTA's the A_{OL} value is replaced by gm.
2. Slew rate values on externally compensated amplifiers will differ with compensation.
   For comparator circuits the slew rate and BW values are replaced by response times.
3. Temperature range's are defined as:
   C = 0°C to 70°C
   I = 40°C to 85°C
   M = –55°C to 125°C
4. Package suffix's are defined as:
   T = TO-5
   E = Plastic
   K = Ceramic Flat Pak
   D = Ceramic — Dual in Line
   S = TO-5 formed for 8 or 12 Lead Plastic
5. Output characteristics are defined for load resistors as defined in the chart. If there are characteristics for two load resistors they will be displayed by a slanted line.
6. CA3100 AC Characteristics:
   Slew rate characteristics in the chart is for C_c = 10 pf Av = 1, V_o = 10 V (pulse)
   For C_c = 0pf, A_V = 10, SR = 70 V/μs typ., 50 V/μs min.

Output Characteristics				AC Characteristics @ 25°C			Package Characteristics[4]		Page #
V_{OUT} +[5] Min. V	V_{OUT}−[5] Min. V	R_L for V_{OUT} OHMS	AOL[1] Min V/V	BW[2] Typ MHz	Slew Rate[2] Typ V/μs	Temp[3] Range IMC	Plastic Ceramic	TO5 Metal CAN	
5.1	−5.1	10K	25K	.002	1.5	C	8E	8T, 8S	237
5.1	−5.1	10K	40K	.0003	0.5	M	8E	8T, 8S	
12	12	∞	gm = 9.6 μmho	2	50	C	8E	8T, 8S	245
12	12	∞	gm = 9.6 μmho	2	50	M	8E	8T, 8S	
14.95	14.2	2K	20K	30	50	M	8E	8T, 8S	213
14.95	14.2	2K	20K	30	50	M	8E	8T, 8S	
14.95	14.2	2K	20K	30	50	M	8E	8T, 8S	
9	−9	2K	630	38	25[6]	M	8E	8T, 8S	135
14.99/12	.001	∞/2K	50K	15/C_c= 0	30/C_c = 0	M	8E	8T, 8S	141
14.99/12	.001	∞/2K	50K	15/C_c = 0	30/C_c = 0	M	8E	8T, 8S	
14.99/12	.001	∞/2K	100K	15/C_c = 0	30/C_c = 0	M	8E	8T, 8S	
12	−14	2K	20K	4.5	9	M	8E	8T, 8S	156
12	−14	2K	20K	4.5	9	M	8E	8T, 8S	
12	−14	2K	50K	4.5	9	M	8E	8T, 8S	
14.99/12	.001	∞/2K	50K	4	10	M	8E	8T, 8S	176
14.99/12	.001	∞/2K	50K	4	10	M	8E	8T, 8S	
14.99/12	.001	∞/2K	100K	4	10	M	8E	8T, 8S	
13	−13	2K	100K	1.2	.25	C	8E	8T, 8S	52
13	−13	2K	316K	1.2	.25	I	8E	8T, 8S	
13	−13	2K	1000K	1.2	.25	M	8E	8T, 8S	
12	−14	2K	20K	4.5	9	M	8E, 14E1	8T, 8S	193
12	−14	2K	20K	4.5	9	M	8E, 14E1	8T, 8S	
14.99/11	.001	∞/2K	50K	4	10	M	8E	8T, 8S	208
14.99/11	.001	∞/2K	50K	4	10	M	8E	8T, 8S	
14.99/11	.001	∞/2K	100M	4	10	M	8E	8T, 8S	
12	−12	∞	50K/∞	9	125	M	16E		260
12.5	−13.3	∞	50K/∞	9	125	M	16E		
V_{SAT} = .4V		(4mA)	25K	t_r = 1.2 μs	t_f = 200 ns	M	8E, 14E1	8T, 8S	291
V_{SAT} = .4V		(4mA)	25K	t_r = 1.2 μs	t_f = 200 ns	M	8E, 14E1	8T, 8S	
V_{SAT} = .4V		(4mA)	50K	t_r = 1.2 μs	t_f = 200 ns	M	8E, 14E1	8T, 8S	
13.5	.10	10K	1K	5	.6	M	14E		110
.90	−.85	∞	10K/10KΩ	.5	.5	M	8E	8T, 8S	63
.90	−.85	∞	20K/10KΩ	.5	.5	M	8E	8T, 8S	
.90	−.95	∞	20K/10KΩ	.5	.5	M	8E	8T, 8S	
9.7	−9.7	∞	10K/10KΩ	.5	.5	M	8E	8T, 8S	63
9.7	−9.7	∞	20K/10KΩ	.5	.5	M	8E	8T, 8S	
9.7	−9.7	∞	20K/10KΩ	.5	.5	M	8E	8T, 8S	
3	−3	10K	10K	.063	.03	M	8E	8T, 8S	254
3	−3	10K	10K	.063	.03	M	8E	8T, 8S	
3	−3	10K	32K	.063	.03	M	8E	8T, 8S	
13	−13	2K	100K	1.2	.25	C	8E	8T, 8S	68
13	−13	2K	316K	1.2	.25	I	8E	8T, 8S	
13	−13	2K	1000K	1.2	.25	M	8E	8T, 8S	
13.7	−13.7	10K	40K	.0003	1.5	M		8T, 8S	79
12	−12	2K	50K	1.0	.50	M		8T, 8S	79

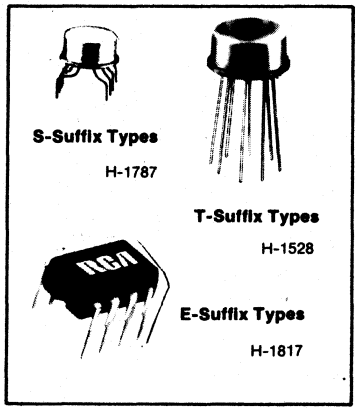
NOTES (cont'd):

7. For CA3440 series R_{SET} = 10 MΩ.
8. CA3493 is equivalent to CA3193 with the exception of nulling & pin out. CA3493 is pos nulling with pinout equivalent μA725. CA3193 has CA741 pinout.
   Temp COEFF = $\Delta V_{IO}/\Delta T$

	Typ	Max	
CA3193/CA3493	1.0	5	μV/° C
CA3193A/CA3493A	1.0	3	μV/° C
CA3193B/CA3493B	.60	2	μV/° C

9. CA6078T and CA6741T are for applications where low noise (burst + I/f) is a prime requirement.
10. −3 db BW
11. Characteristics shown are for single supply operation.
12. CA3280 characteristics @ I_{ABC} = 500 μA except V_{IO}, I_B, I_{IO} which are at I_{ABC} = 1 mA.

CA101, CA201, CA301A Types



Operational Amplifiers

For Commercial, Industrial, and Military Applications

Features:

- *Short-circuit protection and latch-free operation*
- *Unity-gain phase compensation with a single 30-pF capacitor*
- *Replacement for industry types 101, 201, 301A*
- *CA301A Slew Rate (Summing ampl.) 10 V/μs*

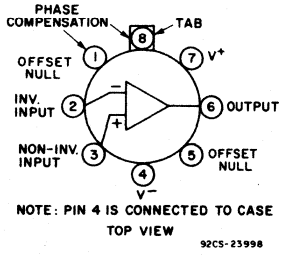
The RCA-CA101, CA201, and CA301A are general-purpose, high-gain operational amplifiers for use in military, industrial, and commerical applications.

These types, which are externally phase compensated, permit a choice of operation for optimum high-frequency performance at a selected gain; unity-gain compensation can be obtained with a single 30-pF capacitor.

All types are available in 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads ("DIL-CAN", S suffix). The CA301A is also available in the 8-lead dual-in-line plastic package ("MINI-DIP"), E suffix), and in chip form (H suffix).

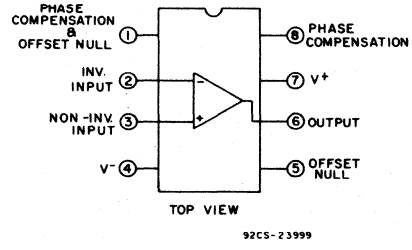
Applications:

- *Long-interval integrator*
- *Timers*
- *Sample-and-hold circuits*
- *Summing amplifiers*
- *Multivibrators*
- *Comparators*
- *Instrumentation*
- *AC/DC converters*
- *Inverting amplifiers*
- *Sine- & square-wave generators*
- *Capacitance multipliers & simulated inductors*



a — TO-5 Style package for all types

T-Suffix
S-Suffix



b — Plastic package for CA301A

E-Suffix

Fig. 1 - Functional diagrams.

Maximum Ratings, *Absolute Maximum Values at T_A = 25° C:*

DC SUPPLY VOLTAGE (Between V+ and V⁻ Terminals):
- CA101, CA201 ..... 44 V
- CA301A ..... 36 V

DC INPUT VOLTAGE ..... ±15 V
(For supply voltages less than ±15 V, the Input Voltage rating is equal to the DC Supply Voltage)
DIFFERENTIAL INPUT VOLTAGE ..... ±30 V
OUTPUT SHORT-CIRCUIT DURATION ..... Indefinite*
DEVICE DISSIPATION:
- UP TO T_A = 75° C ..... 500 mW
- Above T_A = 75° C Derate linearly at ..... 6.67 mW/° C

AMBIENT TEMPERATURE RANGE:
- Operating —
  - CA101 ..... -55 to +125° C
  - CA201, CA301A ..... 0 to +70° C
- Storage (All types) ..... -65 to +150° C

LEAD TEMPERATURE (During Soldering):
- At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265° C

* At $T_A \leq 70°$ C and $T_C \leq 125°$ C (CA101); $T_A \leq 55°$ C and $T_C \leq 70°$ C (CA201, CA301A).

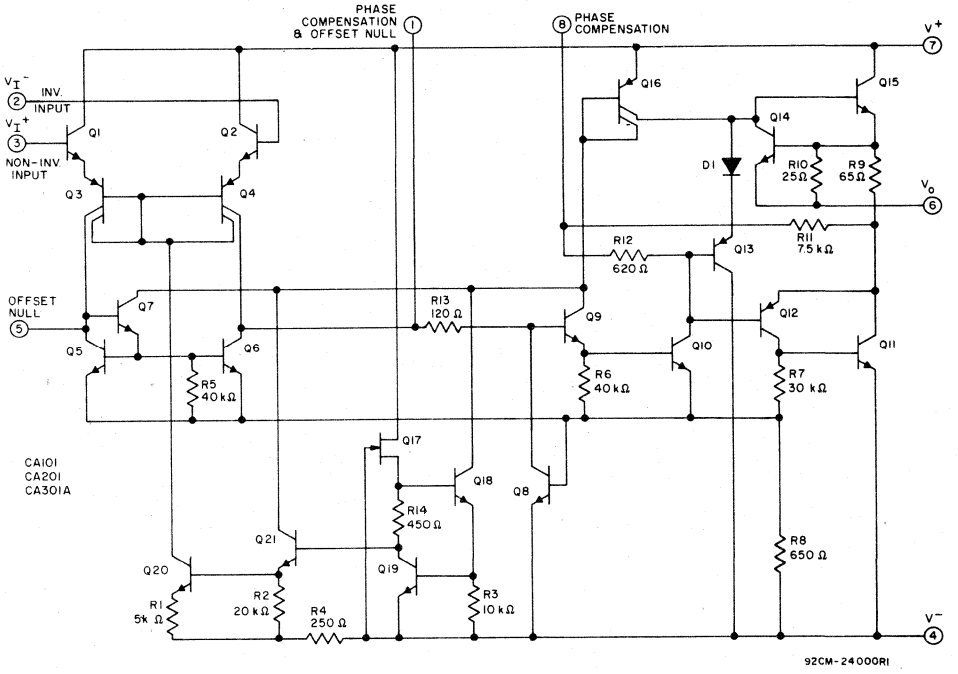


Fig. 2 - Schematic diagram.

CA101, CA201, CA301A Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	TEST CONDITIONS Δ	LIMITS									UNITS
	Supply Voltage (V±) = 5 to 15 V	CA101			CA201			CA301A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage V_{IO}	T_A=25°C $R_S \leq 10k\Omega$	—	1	5	—	2	7.5	—	—	—	mV
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	—	2	7.5	
	$R_S \leq 10k\Omega$	—	—	6	—	—	10	—	—	—	
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	—	—	10	
Average Temperature Coefficient of Input Offset Voltage αV_{IO}	$R_S \leq 10k\Omega$	—	6	—	—	10	—	—	—	—	μV/°C
	$R_S \leq 50\Omega$	—	3	—	—	6	—	—	—	—	
		—	—	—	—	—	—	—	6	30	
Average Temperature Coefficient of Input Offset Current αI_{IO}	-55°C to +25°C	—	—	—	—	—	—	—	—	—	nA/°C
	0°C to +25°C	—	—	—	—	—	—	—	0.02	0.6	
	+25°C to +70°C	—	—	—	—	—	—	—	0.01	0.3	
	+25°C to +125°C	—	—	—	—	—	—	—	—	—	
Input Offset Current I_{IO}	T_A = 0°C	—	—	—	—	150	750	—	—	—	nA
	T_A = 25°C	—	40	200	—	100	500	—	3	50	
	T_A = 70°C	—	—	—	—	50	400	—	—	—	
	T_A = 125°C	—	10	200	—	—	—	—	—	—	
		—	—	—	—	—	—	—	—	70	
	T_A = -55°C	—	100	500	—	—	—	—	—	—	
Input Bias Current I_{IB}	T_A = -55°C	—	0.28	1.5	—	—	—	—	—	—	μA
	T_A = 0°C	—	—	—	—	0.32	2	—	—	—	
	T_A = 25°C	—	0.12	0.5	—	0.25	1.5	—	0.07	0.25	
		—	—	—	—	—	—	—	—	0.3	
Supply Current $I_\pm$	T_A=25°C $V_\pm$=15V	—	—	—	—	—	—	—	1.8	3	mA
	$V_\pm$=20V	—	1.8	3	—	1.8	3	—	—	—	
	T_A=125°C $V_\pm$=20V	—	1.2	2.5	—	—	—	—	—	—	
Open-Loop Differential Voltage Gain A_{OL}	T_A=25°C $V_\pm$=15V V_O=±10V $R_L \geq 2k\Omega$	50	160	—	20	150	—	25	160	—	V/mW
	$V_\pm$=15V V_O=±10V $R_L \geq 2k\Omega$	25	—	—	15	—	—	15	—	—	
Input Resistance R_I	T_A=25°C	0.3	0.8	—	0.1	0.4	—	0.5	2	—	MΩ
Output Voltage Swing V_{OPP}	$V_\pm$=15V R_L=10kΩ	±12	±14	—	±12	±14	—	±12	±14	—	V
	$V_\pm$=15V R_L=2kΩ	±10	±13	—	±10	±13	—	±10	±13	—	
Common-Mode Input-Voltage Range V_{ICR}	$V_\pm$=15V	±12	—	—	±12	—	—	±12	—	—	V
	$V_\pm$=20V	—	—	—	—	—	—	—	—	—	
Common-Mode Rejection Ratio CMRR	$R_S \leq 10k\Omega$	70	90	—	65	90	—	—	—	—	dB
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	70	90	—	
Supply-Voltage Rejection Ratio PSRR	$R_S \leq 10k\Omega$	70	90	—	70	90	—	—	—	—	dB
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	70	90	—	

Δ Characteristics applicable over operating temperature range (T_A) as shown below, unless otherwise specified:
CA101: -55 to +125°C; CA201, CA301A: 0 to 70°C

TYPICAL STATIC CHARACTERISTICS

TYPE CA101

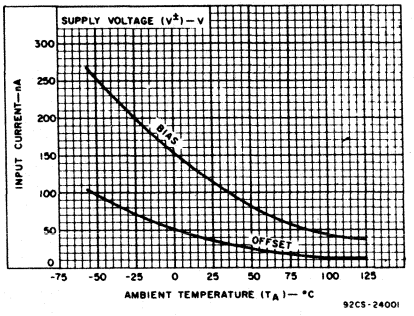


Fig. 3 - Input current (I_{IO}, I_{IB}) vs. temperature.

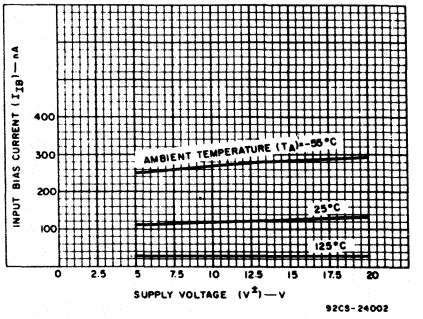


Fig. 4 - Input bias current vs. supply voltage.

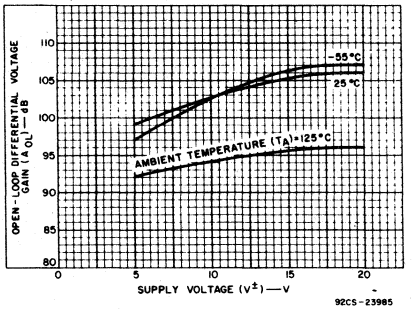


Fig. 5 - Voltage gain vs. supply voltage.

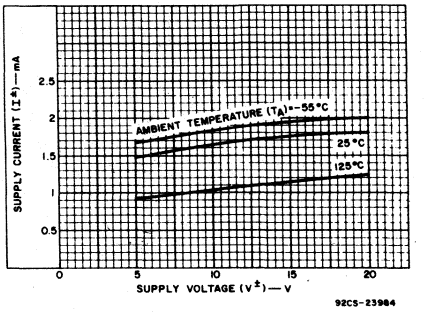


Fig. 6 - Supply characteristics.

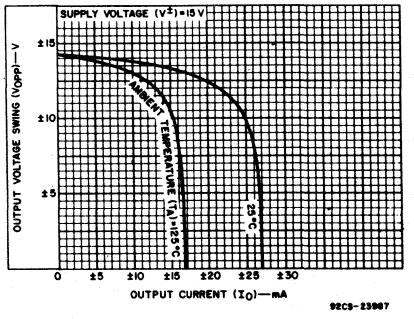


Fig. 7 - Output characteristics.

TYPE CA201

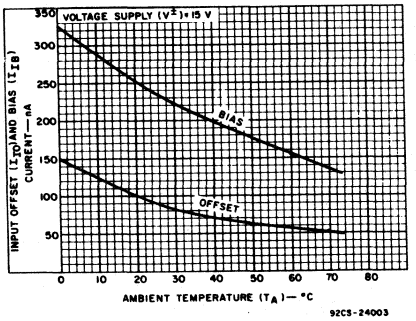


Fig. 8 - Input current (I_{IO}, I_{IB}) vs. temperature.

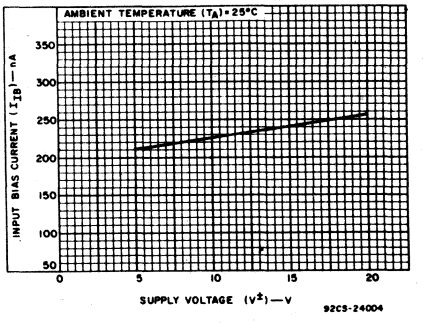


Fig. 9 - Input bias current (I_{IB}) vs. supply voltage.

CA101, CA201, CA301A Types

TYPICAL STATIC CHARACTERISTICS (Cont'd)

TYPE CA201

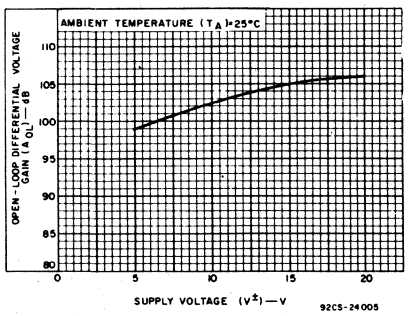


Fig. 10 - Voltage gain vs. supply voltage.

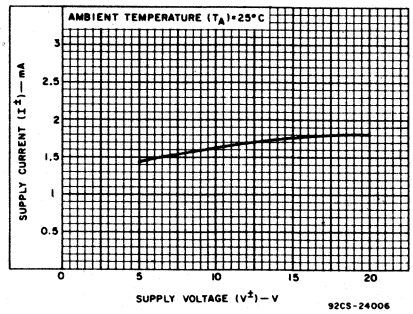


Fig. 11 - Supply characteristics.

TYPE CA301A

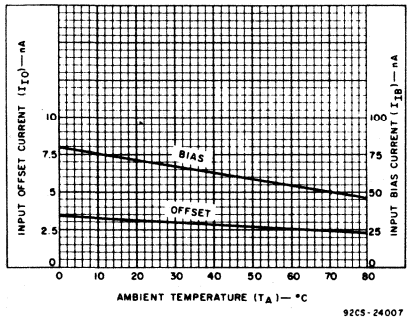


Fig. 12 - Input current (I_{IO}, I_{IB}) vs. temperature.

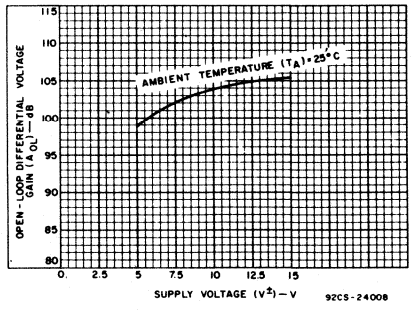


Fig. 13 - Voltage gain vs. supply voltage.

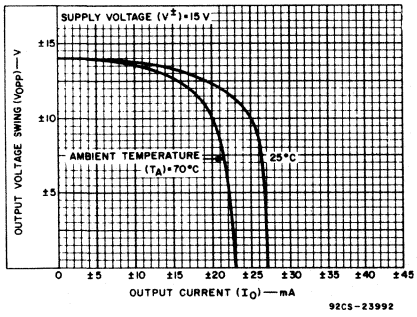


Fig. 14 - Output characteristics.

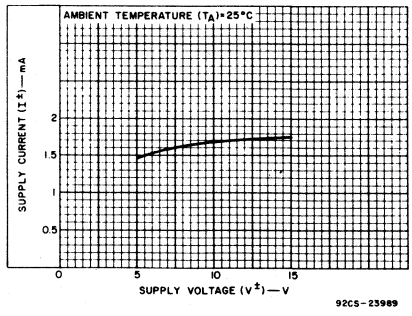


Fig. 15 - Supply characteristics.

TYPICAL DYNAMIC CHARACTERISTICS
TYPES CA101, CA201, CA301A

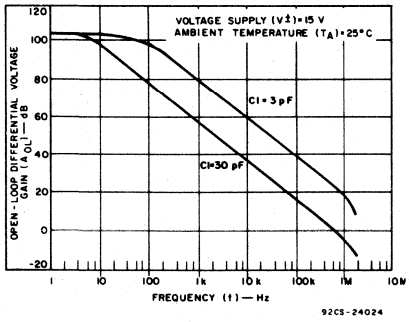


Fig. 16 - Voltage gain vs. frequency.

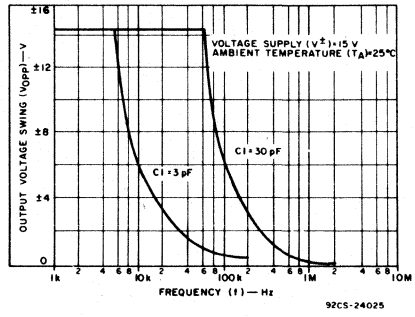


Fig. 17 - Output voltage swing vs. frequency.

TYPICAL DYNAMIC CHARACTERISTICS (Cont'd) FOR TYPES CA101, CA201 AND CA301A

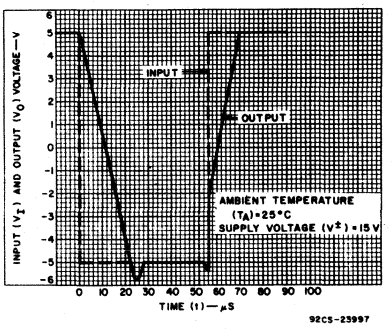


Fig. 18 - Voltage follower pulse response.

TYPE CA301A

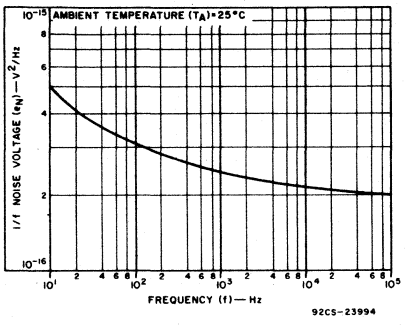


Fig. 19 - 1/f noise voltage vs. frequency.

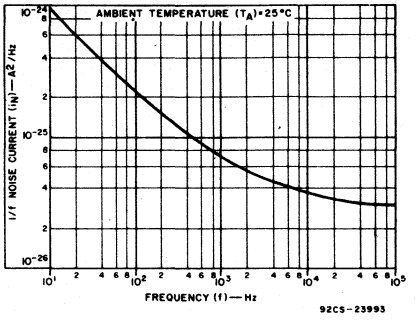
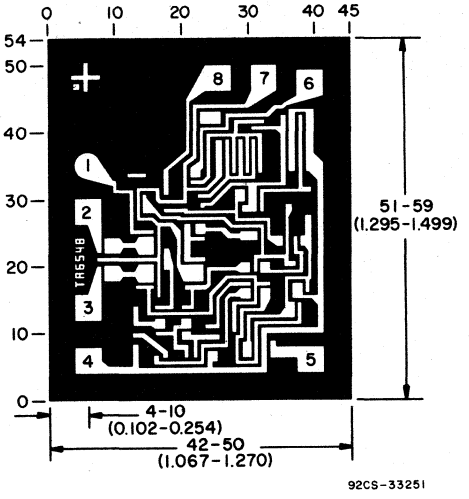


Fig. 20 - 1/f noise current vs. frequency.



Dimensions and pad layout for CA301H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

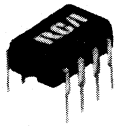
CA307

S-Suffix Types
(DIL-CAN)

H-1787

T-Suffix Types
(TO-5 Style)

H-1528



G-Suffix Types
E-Suffix Types
(Mini-DIP)

H-1817

Operational Amplifier

For Military, Industrial, and Commerical Applications

Applications:

- *Long-interval integrators*
- *Timers*
- *Sample-and-hold circuits*
- *Summing amplifiers*
- *Multivibrators*

The RCA CA307 is a general-purpose operational amplifier intended for use in military, industrial, and commerical applications. A 30-pF on-chip capacitor provides internal frequency compensation.

The CA307 is available in 8-lead TO-5 style packages with standard leads (T suffix), with dual-in-line formed leads ("DIL-CAN", S suffix), in the 8-lead dual-in-line plastic package ("MINI-DIP", E suffix), and in chip form (H suffix).

The CA307 is a direct replacement for industry type 307 in packages with similiar terminal arrangements.

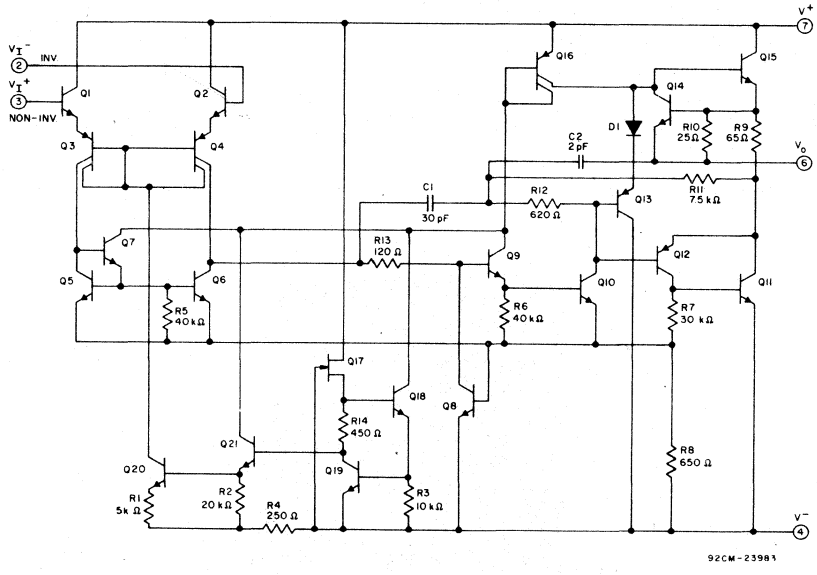


Fig. 1 - Schematic diagram of CA307.

Maximum Ratings, *Absolute Maximum Values at T_A = 25° C:*

DC SUPPLY VOLTAGE (Between V+ and V⁻ Terminals):
CA307 ..... 36 V
DC INPUT VOLTAGE ..... ±15 V
(For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage)
DIFFERENTIAL INPUT VOLTAGE ..... ±30 V
OUTPUT SHORT-CIRCUIT DURATION* ..... Indefinite
DEVICE DISSIPATION UP TO T_A = 70° C ..... 500 mW
Above T_A = 70° C Derate linearly at ..... 6.67 mW/° C
AMBIENT TEMPERATURE RANGE:
Operating ..... 0° C to +70° C†
Storage ..... -65° C to +150° C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265° C

*For type CA307 continuous short circuit is allowed for Case Temperature to +70° C and ambient temperature to +55° C.
†Types CA307 E, S, and T can be operated over the temperature range of -55 to +125° C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70° C.

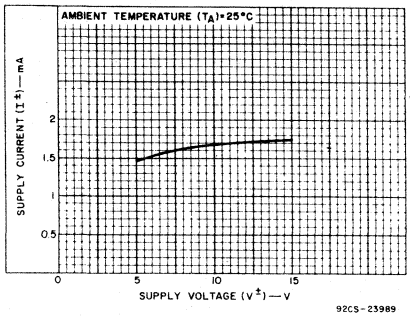


Fig. 2 - Supply current vs. supply voltage.

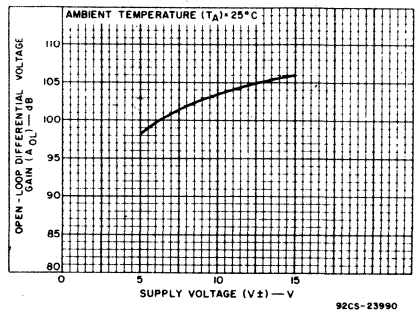


Fig. 3 - Open-loop differential voltage gain vs. supply voltage.

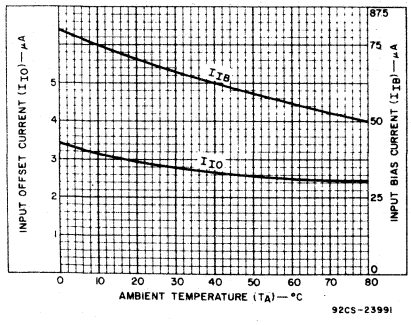


Fig. 4 - Input offset and input bias current vs. ambient temperature.

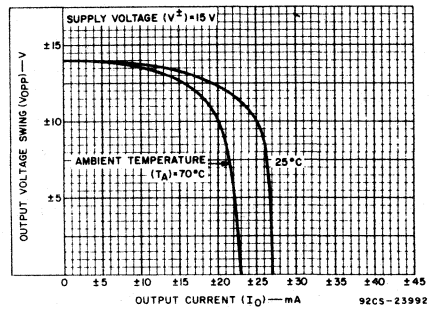


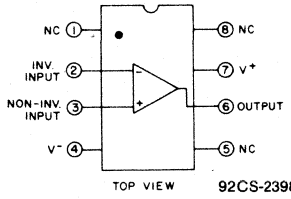
Fig. 5 - Output voltage swing vs. output current.

CA307

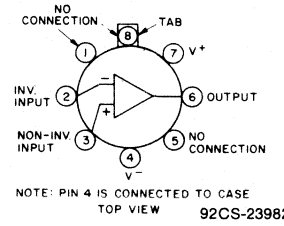
ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS△	LIMITS			UNITS
		Supply Voltage (V±) = 5 V to 15 V	CA307			
			Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	T_A = 25° C, $R_S \leq$ 50 kΩ	—	2	7.5	mV
		$R_S \leq$ 50 kΩ	—	—	10	
Average Temperature Coefficient of Input Offset Voltage	αV_{IO}		—	6	30	μV/° C
Input Offset Current	I_{IO}		—	—	70	nA
		T_A = 25° C	—	3	50	
Average Temperature Coefficient of Input Offset Current	αI_{IO}	+25 to 70° C	—	0.01	0.3	nA/° C
		0 to +25° C	—	0.02	0.6	
Input Bias Current	I_{IB}		—	—	300	nA
		T_A = 25° C	—	70	250	
Supply Current	I±	T_A = +125° C, V± = 20 V	—	—	—	mA
		T_A = 25° C, V± = 15 V	—	1.8	3	
Open-Loop Differential Voltage Gain	A_{OL}	V± = 15 V, V_O = ±10V, $R_L \geq$ 2kΩ	15	—	—	V/mV
		V±=15V, V_O=±10 V, R_L≥2kΩ,T_A=25° C	25	160	—	
Input Resistance	R_I	T_A = 25° C	0.5	2	—	MΩ
Output Voltage Swing	V_{OPP}	V± = 15 V, R_L = 10 kΩ	±12	±14	—	V
		V± = 15 V, R_L = 2 kΩ	±10	±13	—	
Input Voltage Range	V_{ICR}	V± = 15 V	±12	—	—	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq$ 50 kΩ	70	90	—	dB
Supply-Voltage Rejection Ratio	PSRR	$R_S \leq$ 50 kΩ	70	96	—	dB

△Characteristics applicable over operating temperature range T_A = 0 to 70° C unless otherwise specified.



FUNCTIONAL DIAGRAM FOR PLASTIC PACKAGE



FUNCTIONAL DIAGRAM FOR TO-5 STYLE PACKAGES

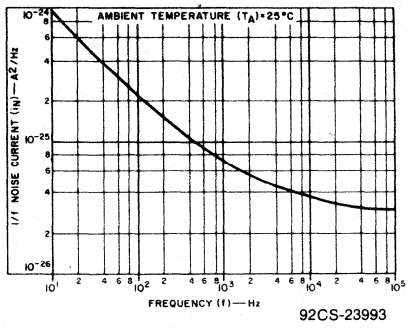


Fig. 6 - 1/f noise current vs. frequency.

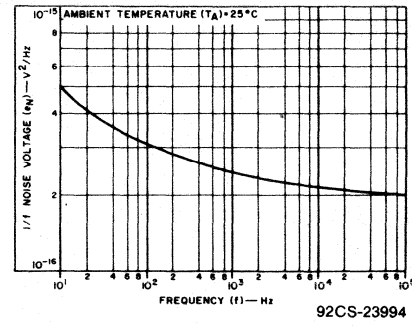


Fig. 7 - 1/f noise voltage vs. frequency.

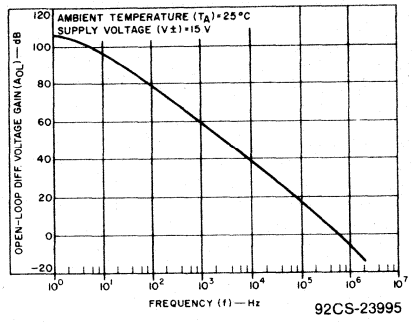


Fig. 8 - Open-loop differential voltage gain vs. frequency.

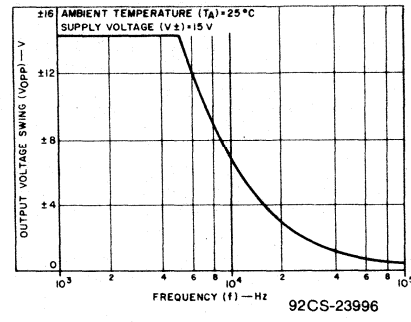


Fig. 9 - Output voltage swing vs. frequency.

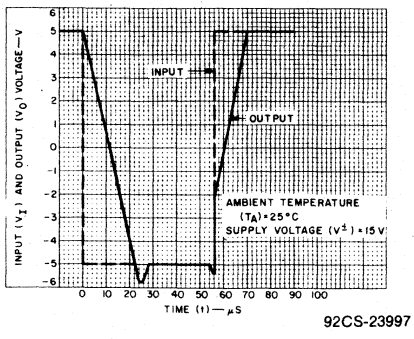
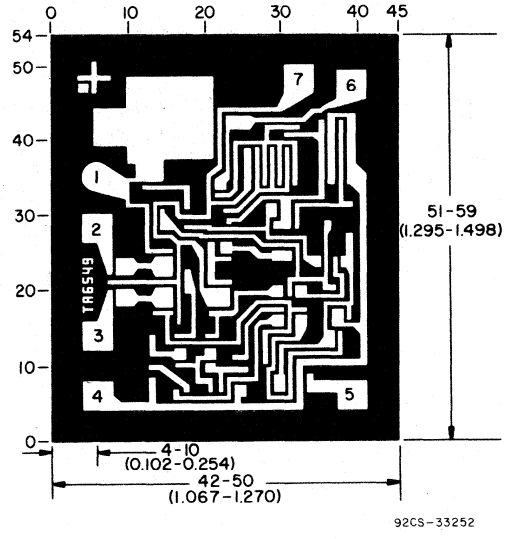


Fig. 10 - Input and output voltage vs. time.

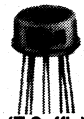


Dimensions and pad layout for CA307H.

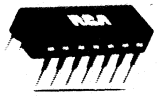
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA741, CA747, CA748, CA1458, CA1558 Types

(E Suffix)
8-LEAD DIP
(MINI-DIP)
H-1817



(T Suffix)
8-LEAD
TO-5
H-1528



(E Suffix)
14-LEAD DIP
H-1517

(S Suffix)
8-LEAD
TO-5
(DIL-CAN)
H-1787

Operational Amplifiers

High-Gain Single and Dual Operational Amplifiers
For Military, Industrial and Commerical Applications

Features:

- *Input bias current (all types):*
  500 nA max.
- *Input offset current (all types):*
  200 nA max.

Applications:

- *Comparator*
- *DC amplifier*
- *Integrator or differentiator*
- *Multivibrator*
- *Narrow-band or band-pass filter*
- *Summing amplifier*

The RCA-CA1458, CA1558 (dual types); CA741C, CA741 (single-types); CA747C, CA747 (dual types); and CA748C, CA748 (single types) are general-purpose, high-gain operational amplifiers for use in military, industrial, and commercial applications.

These monolithic silicon integrated-circuit devices provide output short-circuit protection and latch-free operation. These types also feature wide common-mode and differential-mode signal ranges and have low-offset voltage nulling capability when used with an appropriately valued potentiometer. A 5-megohm potentiometer is used for offset nulling types CA748C, CA748 (See Fig. 10); a 10-kilohm potentiometer is used for offset nulling types CA741C, CA741, CA747CE, CA747E (See Fig. 9); and types CA1458, CA1558, CA747CT, have no specific terminals for offset nulling. Each type consists of a differential-input amplifier that effectively drives a gain and level-shifting stage having a complementary emitter-follower output.

This operational amplifier line also offers the circuit designer the option of operation with internal or external phase compensation.

Types CA748C and CA748, which are externally phase compensated (terminals 1 and 8) permit a choice of operation for improved bandwidth and slew-rate capabilities. Unity gain with external phase compensation can be obtained with a single 30-pF capacitor. All the other types are internally phase-compensated.

RCA's manufacturing process make it possible to produce IC operational amplifiers with low-burst ("popcorn") noise characteristics. Type CA6741, a low-noise version of the CA741, gives limit specifications for burst noise in the data bulletin, File No. 530. Contact your RCA Sales Representative for information pertinent to other operational amplifier types that meet low-burst noise specifications.

RCA Type No.	No. of Ampl.	Phase Comp.	Offset Voltage Null	Min. A_{OL}	Max. V_{IO} (mV)	Operating-Temperature Range (°C)
CA1458	dual	int.	no	20k	6	0 to +70▲
CA1558	dual	int.	no	50k	5	−55 to +125
CA741C	single	int.	yes	20k	6	0 to +70▲
CA741	single	int.	yes	50k	5	−55 to +125
CA747C	dual	int.	yes*	20k	6	0 to +70▲
CA747	dual	int.	yes*	50k	5	−55 to +125
CA748C	single	ext.	yes	20k	6	0 to +70▲
CA748	single	ext.	yes	50k	5	−55 to +125

*In the 14-lead dual-in-line plastic package only.

▲All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

CA741, CA747, CA748, CA1458, CA1558 Types

ORDERING INFORMATION

When ordering any of these types, it is important that the appropriate suffix letter for the package required be affixed to the type number. For example: If a CA1458 in a straight-lead TO-5 style package is desired, order CA1458T.

TYPE NO.	PACKAGE TYPE AND SUFFIX LETTER							FIG. NO.
	TO-5 STYLE			PLASTIC		CHIP	BEAM-LEAD	
	8L	10L	DIL-CAN	8L	14L			
CA1458	T		S	E		H		1d, 1h
CA1558	T		S	E				1d, 1h
CA741C	T		S	E		H		1a, 1e
CA741	T		S	E			L	1a, 1e
CA747C		T			E	H		1b, 1f
CA747		T			E			1b, 1f
CA748C	T		S	E		H		1c, 1g
CA748	T		S	E				1c, 1g

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^\circ C$:

DC Supply Voltage (between V^+ and V^- terminals):
- CA741C, CA747C▲, CA748C, CA1458▲ . . . . . 36 V
- CA741, CA747▲, CA748, CA1558▲ . . . . . 44 V

Differential Input Voltage . . . . . ±30 V
DC Input Voltage* . . . . . ±15 V
Output Short-Circuit Duration . . . . . Indefinite
Device Dissipation:
- Up to 70°C (CA741C, CA748C) . . . . . 500 mW
- Up to 75°C (CA741, CA748) . . . . . 500 mW
- Up to 30°C (CA747) . . . . . 800 mW
- Up to 25°C (CA747C) . . . . . 800 mW
- Up to 30°C (CA1558) . . . . . 680 mW
- Up to 25°C (CA1458) . . . . . 680 mW

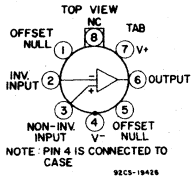
For Temperatures Indicated Above . . . . . Derate linearly 6.67 mW/°C
Voltage between Offset Null and V^- (CA741C, CA741, CA747CE) . . . . . ±0.5 V
Ambient Temperature Range:
- Operating – CA741, CA747E, CA748, CA1558 . . . . . −55 to +125 °C
- CA741C, CA747C, CA748C, CA1458 . . . . . 0 to +70 °C†
- Storage . . . . . −65 to +150 °C

Lead Temperature (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . 265 °C

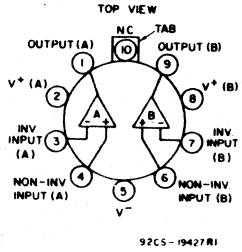
* If Supply Voltage is less than ± 15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

▲ Voltage values apply for each of the dual operational amplifiers.

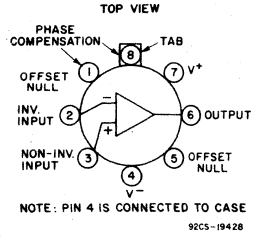
† All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.



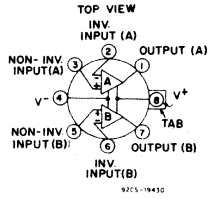
1a.–CA741CS,CA741CT,CA741S, & CA741T with internal phase compensation.



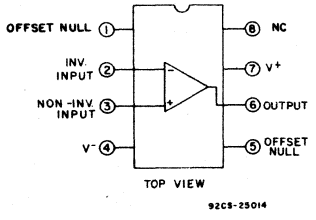
1b.–CA747CT and CA747T with internal phase compensation.



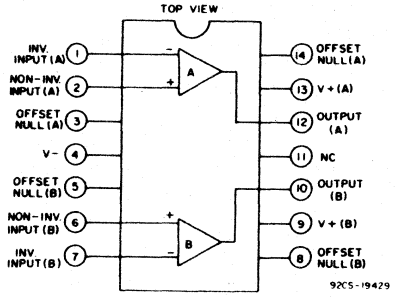
1c.–CA748CS, CA748CT,CA748S, and CA748T with external phase compensation.



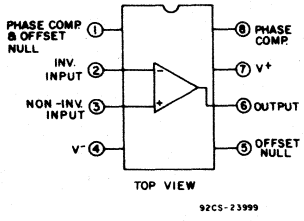
1d.–CA1458S,CA1458T,CA1558S, and CA1558T and internal phase compensation.



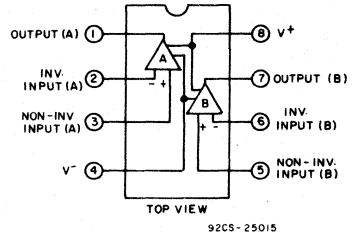
1e.–CA741C and CA741E with internal phase compensation.



1f.–CA747CE and CA747E with internal phase compensation.



1g.–CA748CE and CA748E with external phase compensation.



1h.–CA1458E and CA1558E with internal phase compensation.

Fig. 1 – Functional diagrams.

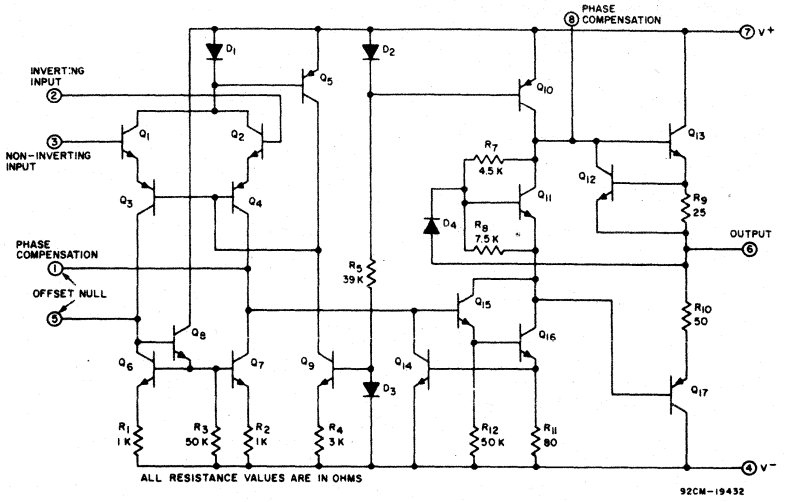


Fig.2—Schematic diagram of operational amplifier with external phase compensation for CA748C and CA748.

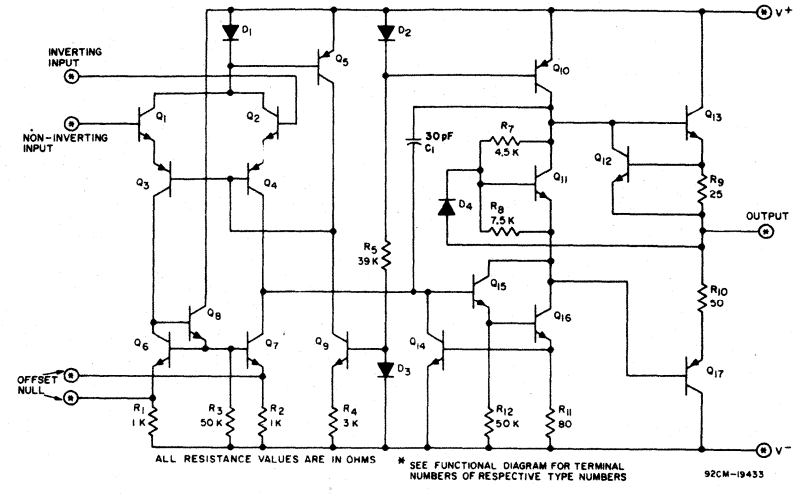


Fig.3—Schematic diagram of operational amplifiers with internal phase compensation for CA741C, CA741, and for each amplifier of the CA747C, CA747, CA1458, and CA1558.

CA741, CA747, CA748, CA1458, CA1558 Types

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	TEST CONDITIONS V± = ±15 V •	TYP. VALUES ALL TYPES	UNITS
Input Capacitance, C_I		1.4	pF
Offset Voltage Adjustment Range		±15	mV
Output Resistance, R_O		75	Ω
Output Short-Circuit Current		25	mA
Transient Response: Rise Time, t_r	Unity gain, V_I = 20 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF	0.3	μs
Transient Response: Overshoot		5	%
Slew Rate, SR: Closed-loop	$R_L \geq$ 2 kΩ	0.5	V/μs
Slew Rate, SR: Open-loop▲		40	

▲ Open-loop slew rate applies only for types CA748C and CA748.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, V^+ = 15 V, V^- = −15 V	Ambient Temperature, T_A	LIMITS CA741C CA747C* CA748C CA1458* Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S \leq$ 10 kΩ	25 °C	–	2	6	mV
		0 to 70 °C	–	–	7.5	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		0 to 70 °C	–	–	300	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		0 to 70 °C	–	–	800	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V_O = ±10 V	25 °C	20,000	200,000	–	
		0 to 70 °C	15,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		25 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq$ 10 kΩ	25 °C	70	90	–	dB
Supply-Voltage Rejection Ratio, PSRR	$R_S \leq$ 10 kΩ	25 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq$ 10 kΩ	25 °C	±12	±14	–	V
	$R_L \geq$ 2 kΩ	25 °C	±10	±13	–	
		0 to 70 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
Device Dissipation, P_D		25 °C	–	50	85	mW

* Values apply for each section of the dual amplifiers.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, $V^+ = 15$ V, $V^- = -15$ V	Ambient Temperature, T_A	LIMITS CA741 CA747* CA748 CA1558* Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S = \leq 10\,k\Omega$	25 °C	–	1	5	mV
		−55 to +125 °C	–	1	6	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		−55 °C	–	85	500	
		+125 °C	–	7	200	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		−55 °C	–	300	1500	
		+125 °C	–	30	500	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq 2\,k\Omega$ $V_O = \pm 10$ V	25 °C	50,000	200,000	–	
		−55 to +125 °C	25,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		−55 to +125 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq 10\,k\Omega$	−55 to +125 °C	70	90	–	dB
Supply Voltage Rejection Ratio, PSRR	$R_S \leq 10\,k\Omega$	−55 to +125 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq 10\,k\Omega$	−55 to +125 °C	±12	±14	–	V
	$R_L \geq 2\,k\Omega$	−55 to +125 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
		−55 °C	–	2	3.3	
		+125 °C	–	1.5	2.5	
Device Dissipation, P_D		25 °C	–	50	85	mW
		−55 °C	–	60	100	
		+125 °C	–	45	75	

* Values apply for each section of the dual amplifiers.

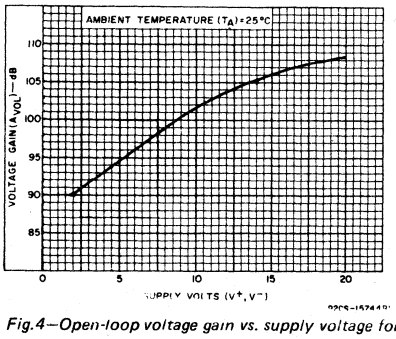


Fig.4—Open-loop voltage gain vs. supply voltage for all types except CA748 and CA748C.

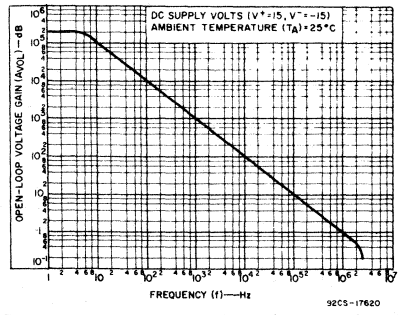


Fig.5—Open-loop voltage gain vs. frequency for all types except CA748 and CA748C.

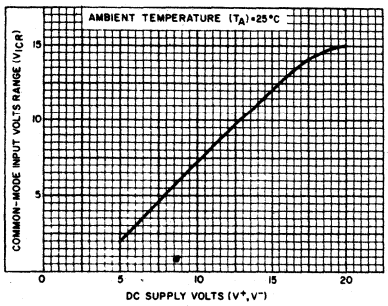


Fig.6—Common-mode input voltage range vs. supply voltage for all types.

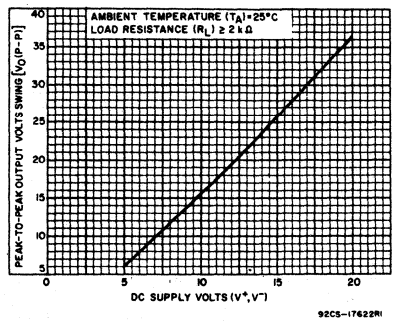


Fig.7—Peak-to-peak output voltage vs. supply voltage for all types except CA748 and CA748C.

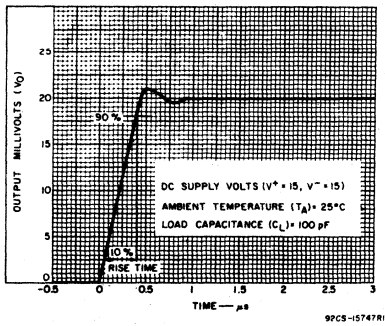


Fig.8—Output voltage vs. transient response time for CA741C and CA741.

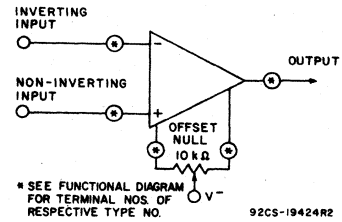


Fig.9—Voltage offset null circuit for CA741C, CA741, CA747CE, and CA747E.

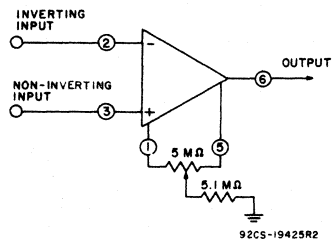


Fig.10—Voltage-offset null circuit for CA748C and CA748.

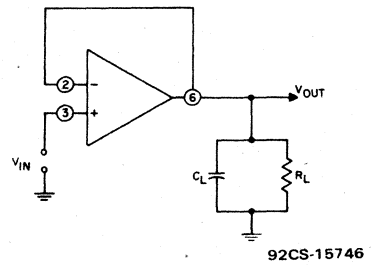


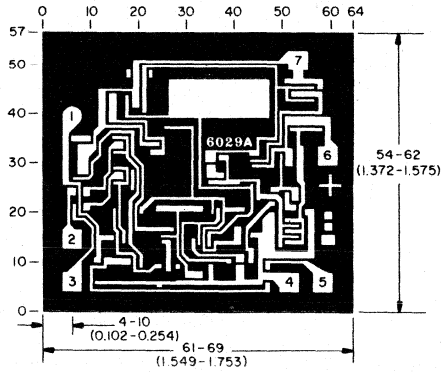
Fig.11—Transient response test circuit for all types.

CA741, CA747, CA748, CA1458, CA1558 Types

CHIP PHOTOS

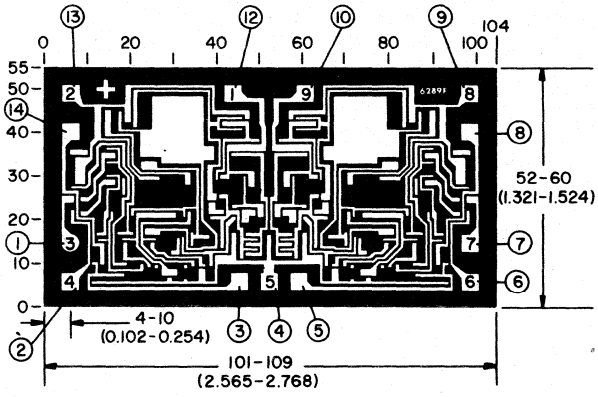
Dimensions and Pad Layouts

CA741CH



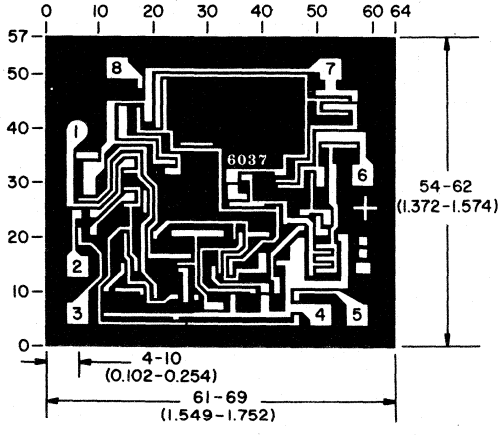
92CS-33259

CA747CH



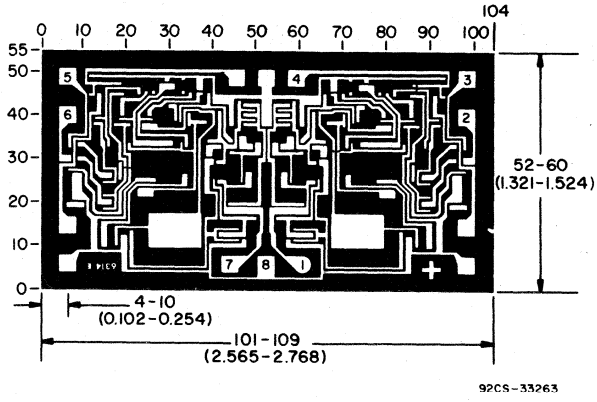
NOTE: NOS. IN PADS ARE FOR 10-LEAD TO-5
NOS. OUTSIDE OF CHIP ARE FOR 14-LEAD DIP

92CM-33260



92CS-33261

CA748CH

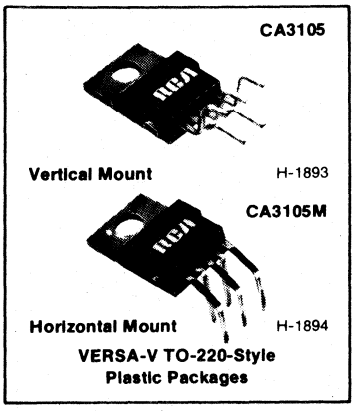


92CS-33263

CA1458H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3105, CA3105M



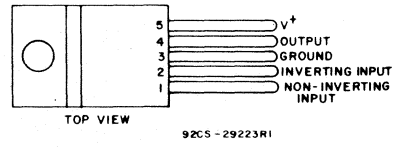
High-Power Operational Amplifier

Features

- *Output short circuit and thermal overload protection*
- *Load dump voltage surge protection*
- *Output current capability of up to 3.5 A*
- *Compensated for gains > 30*
- *VERSA-V power transistor package–requires no electrical insulation*

The RCA-CA3105 is a monolithic silicon operational amplifier designed for driving loads as low as 1.6 ohms. It provides a high output current capability (up to 3.5 A), and rapid settling time. It is ideal for use in ac or dc servo amplifiers, deflection yoke drivers, programmable power supplies, power multivibrators, power dump flashers, etc.

The CA3105 is supplied in a 5-lead plastic TO-220-style VERSA-V package. All leads (except terminal 3) are electrically insulated from the mounting flange, eliminating the need for insulating hardware. The VERSA-V package is available with two lead configurations. The CA3105 has a vertical mount lead form, and the CA3105M has a horizontal mount lead form.



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE	28 V
OPERATING SUPPLY VOLTAGE	18 V
OUTPUT PEAK CURRENT:	
REPETITIVE	3.5 A
NON-REPETITIVE	4.5 A
POWER DISSIPATION, P_D @ T_A=90°C	15 W
THERMAL RESISTANCE, JUNCTION-TO-CASE	4°C/W
AMBIENT-TEMPERATURE RANGE:	
OPERATING	0 to +125°C
STORAGE	−40 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 12 s max.	260°C

ELECTRICAL CHARACTERISTICS @ T_A = 25° C, V_S = +10 V Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}		—	1.3	5.0	mV
Input Bias Current, I_B	$T_A \leq T_{MAX}$	24	30	35	nA
Input Offset Current, I_{IO}	V_{CM} = 0	—	2.6	7	nA
Voltage Gain, A_{OL}		76	80	84	dB
Output Voltage Swing, V_O	A_V = +1 R_L = 100 Ω	±8	±8.5	±8.8	V
	R_L=50 KΩ	±8	±8.7	±9	V
Common Mode Rejection Ratio, CMRR		64	65	67	dB
Power Supply Rejection Ratio, PSRR		53	55	60	dB
Quiescent Supply Current, I_S		65	85	100	mA
Input Capacitance, C_{in}	f = 1 MHz	—	5	—	pF
Slew Rate, SR	R_L = 100 Ω, A_V = +1	—	5	—	V/μs
Gain Bandwidth Product	A_{VL} = 0 dB, R_L = 100 Ω C_L = 100 pF, V_{IN} = 20, f = 1 kHz	—	5	—	MHz

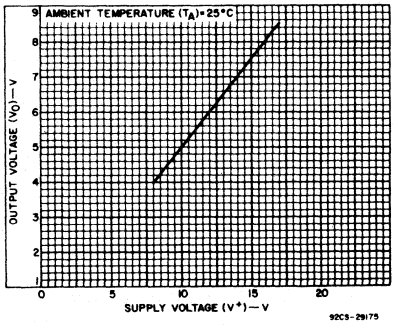


Fig. 1 - Typical quiescent output voltage as a function of supply voltage.

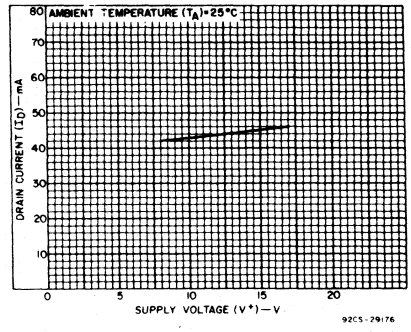


Fig. 2 - Typical quiescent drain current as a function of supply voltage.

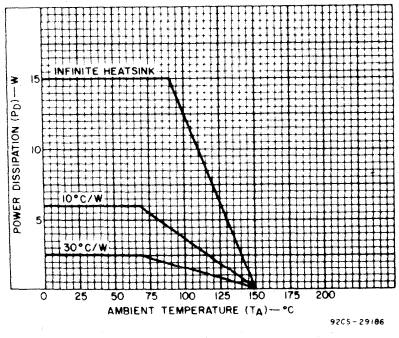


Fig. 3 - Maximum allowable power dissipation as a function of ambient temperature.

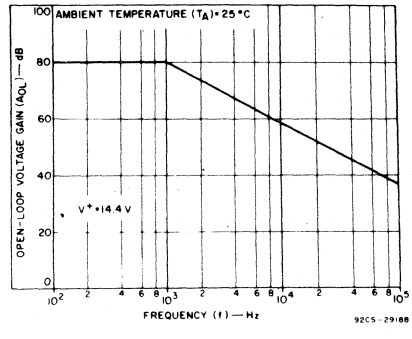
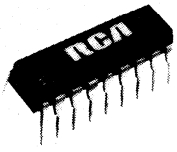


Fig. 4 - Open-loop voltage gain as a function of frequency.

CA3152E



H-1899

E-SUFFIX
18-Lead Dual-In-Line
Plastic Package

BiMOS Input Op-Amp, Frequency Band-Select Switch, and Quad Comparator

For Television Tuning Interfacing

Features:

- *Input op-amp: high impedance PMOS input transistors and internal reference bias*
- *Low input bias current and internal diode protection at op-amp inputs*
- *High op-amp output voltage swing (0.7-28.0 V dc) with 3-mA source or sink capability*
- *Three op-amp output voltage logic-controlled clamp levels*
- *Logic-controlled bandswitching with four separate outputs*
- *Two bandswitch output current sinks*
- *Two bandswitch current-limited output current sources*
- *Internally referenced quad comparator*
- *Low drive current input requirement*
- *Low output leakage*
- *High output current sink capability*
- *Bipolar and PMOS processes on a single chip*

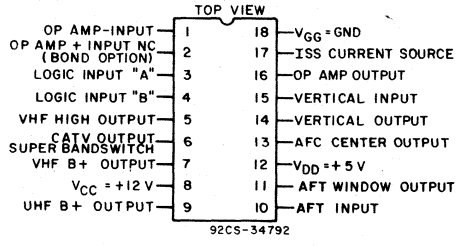
The RCA CA3152E* linear integrated circuit has three major sections for interfacing television tuning systems: an input op-amp, a band-select switch, and an internally referenced quad-comparator.

The op-amp output voltage has a wide dynamic range with a 3-mA source or sink capability and can be clamped to three discrete levels in response to logic inputs. The op-amp also has internal bias reference and phase compensation. High impedance PMOS input transistors are protected by input limiting diode clippers.

The band-select switch has two logic inputs controlling four outputs: VHF B+, VHF HIGH, SUPERBAND CATV, AND UHF B+. The VHF B+ and UHF B+ outputs are current sources which are short-circuit protected by current limiting. VHF HIGH and SUPERBAND CATV outputs are current sinks with low off-state leakage.

The quad comparator features internal reference bias, low output leakage, and 6-mA current sinking capability. The outputs of two of the comparators are internally connected to form a window comparator.

The CA3152E is supplied in an 18-lead dual-in-line plastic package.



TERMINAL ASSIGNMENT

*Formerly RCA Dev. Type No. TA10702

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_A=25° C)

SUPPLY CURRENT (I_{SS})	20 mA
SUPPLY VOLTAGE (V_{CC}) (PIN 8)	+18 V dc
SUPPLY VOLTAGE (V_{DD}) (PIN 12)	+8 V dc
DEVICE DISSIPATION PER PACKAGE (P_D):	
UP TO 55° C	750 mW
ABOVE 55° C (Derate Linearly)	7.9 mW/° C
AMBIENT TEMPERATURE RANGE:	
OPERATING (T_A)	0 to +70 °C
STORAGE (T_{stg})	−55 to +150 °C

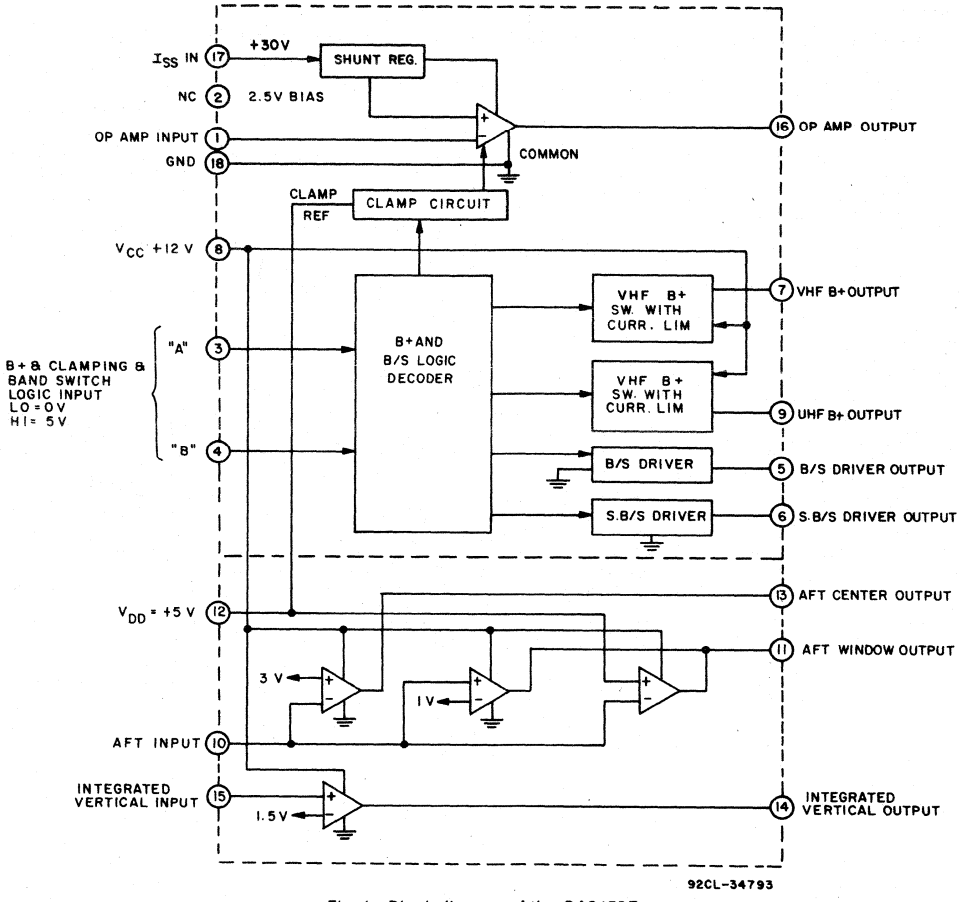


Fig. 1 - Block diagram of the CA3152E.

LOGIC TABLE FOR BANDSWITCH AND OP-AMP OUTPUTS

Inputs				Outputs					
Op-Amp Pin 1	V_A Pin 3	V_B Pin 4	BAND	VHF B+ Source Pin 7	UHF B+ Source Pin 9	VHF High Sink Pin 5	Super Bandswitch CATV Sink Pin 6	Pin 16 Voltage Min.	Pin 16 Voltage Max.
1	0	0	Low VHF	ON	OFF	OFF	OFF	0.7 V	1.1 V
1	0	1	High VHF Midband CATV	ON	OFF	ON	OFF	1.6 V	2.1 V
1	1	0	Superband CATV	ON	OFF	ON	ON	4.9 V	5.75 V
1	1	1	UHF	OFF	ON	ON	OFF	0.7 V	1.1 V
0	0	0		ON	OFF	OFF	OFF	28 V	34 V
0	0	1		ON	OFF	ON	OFF	28 V	34 V
0	1	0		ON	OFF	ON	ON	28 V	34 V
0	1	1		OFF	ON	ON	OFF	28 V	34 V

Logic 1=5 V
Logic 0=0 V

CA3152E

COMMON SECTION

ELECTRICAL CHARACTERISTICS @ T_A=25°C; I_{SS}=9 mA, V_{DD}=+5 V dc, V_{CC}=+12 V dc

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		Min.	Max.	
I_{CC} Supply Current, I_8	All Outputs Open	0.1	2	mA
I_{DD} Supply Current, I_{12}	All Outputs Open	0.1	1.5	mA
Tuning Voltage Supply Regulator, V_{17}	I_{SS}=9 mA	29	35	V dc
V_{17} Regulation, ΔV_{17}	V_1=V_{17} @ I_{SS}=6 mA, V_2=V_{17} @ I_{SS}=12 mA, ΔV_{17}=$\lvert V_1-V_2 \rvert$	0	0.8	V dc

OP-AMP SECTION

ELECTRICAL CHARACTERISTICS @ T_A=25°C; I_{SS}=9 mA, V_{DD}=+5 V dc, V_{CC}=+12 V dc
V_H=2.4 V Min., V_L=0.8 V Max., V_A=Pin 3, V_B=Pin 4

CHARACTERISTIC	V_A	V_B	TEST CONDITIONS	LIMITS		UNITS
				Min.	Max.	
Bias Voltage, V_1 Bias	V_L	V_L	Pin 1 through 10 KΩ to Pin 16	2.35	2.65	V dc
Bias Current, I_1 Bias	V_L	V_L	Pin 1 to Ground	—	100	pA
Output Source Current, I_{16} Source	V_L	V_L	V_1=0 V, V_{16}=17.5 V dc	−3	—	mA
Output Sink Current, I_{16} Sink	V_L	V_L	V_1=5 V dc, V_{16}=17.5 V dc	3	—	mA
Open Loop Voltage Gain, V_{16} A_{OL}	V_L	V_L	I_{SS}=10 mA, R_L=10 KΩ, V_1=2.5 V dc, V_{16}=17.5 V dc	1	—	V/mV
High Clamp Output Voltage, V_{16} HCL	V_L	V_L	V_1=0 V dc	28	34	V dc
Low Clamp Output Voltage, V_{16} CL1	V_L	V_L	V_1=5 V dc	0.7	1.1	V dc
Low Clamp Output Voltage, V_{16} CL2	V_L	V_H	V_1=5 V dc	1.6	2.1	V dc
Low Clamp Output Voltage, V_{16} CL3	V_H	V_L	V_1=5 V dc	4.9	5.75	V dc

BANDSWITCH SECTION

ELECTRICAL CHARACTERISTICS @ T_A=25°C; I_{SS}=9 mA, V_{DD}=+5 V dc, V_{CC}=+12 V dc
V_H=2.4 V Min., V_L=0.8 V Max., V_A=Pin 3, V_B=Pin 4, V_I=5 V

CHARACTERISTIC	V_A	V_B	TEST CONDITIONS	LIMITS		UNITS
				Min.	Max.	
Pin 7 ON (VHF ON)	V_H	V_L	I_7=−15 mA	11.3	—	V dc
Pin 9 ON (UHF ON)	V_H	V_H	I_9=−15 mA	11.3	—	V dc
Pin 7 OFF (VHF OFF)	V_H	V_H	I_7=1 mA	—	1.5	V dc
Pin 9 OFF (UHF OFF)	V_H	V_L	I_9=1 mA	—	1.5	V dc
VHF Short Circuit Current, I_7 SC	V_L	V_L	—	20	45	mA
UHF Short Circuit Current, I_9 SC	V_H	V_H	—	20	45	mA
V5 Saturation Voltage, V_5 SAT	V_H	V_L	I_5=2.5 mA	—	0.5	V dc
V6 Saturation Voltage, V_6 SAT	V_H	V_L	I_6=2.5 mA	—	0.5	V dc
Bandswitch Leakage Current, I_5 L	V_L	V_L	V_5=15 V dc	−0.2	1	μA
Superbandswitch Leakage Current, I_6 L	V_L	V_L	V_6=15 V dc	−0.2	1	μA
Logic Input Low Input Current, I_3 L	—	—	V_A=0 V dc, V_B=5 V dc	0	−30	μA
Logic Input Low Input Current, I_4 L	—	—	V_A=5 V dc, V_B=0 V dc	0	−30	μA
Logic Input High Input Current, I_3 H	—	—	V_A=5 V dc, V_B=0 V dc	—	1	μA
Logic Input High Input Current, I_4 H	—	—	V_A=0 V dc, V_B=5 V dc	—	1	μA

DC COMPARATOR SECTION
ELECTRICAL CHARACTERISTICS @ T_A=25° C; I_{SS}=9 mA, V_{DD}=+5 V dc, V_{CC}=+12 V dc

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		Min.	Max.	
Input Bias Current, I_{10} BIAS L	V_{10}=0 V dc	—	−750	nA
Input Bias Current, I_{10} BIAS H	V_{10}=6 V dc	+1	−0.450	mA
Input Bias Current, I_{15} BIAS L	V_{15}=0 V dc	0	−250	nA
Input Bias Current, I_{15} BIAS H	V_{15}=6 V dc	+1	−0.160	mA
Output Sink Current, I_{11} Sink	V_{10}=0 V dc, V_{11}=1.5 V dc	6	—	mA
Output Sink Current, I_{11} Sink	V_{10}=6 V dc, V_{11}=1.5 V dc	6	—	mA
Output Saturation Voltage, V_{11} SAT1	V_{10}=0 V dc, I_{11} SINK=4 mA	100	700	mV
Output Saturation Voltage, V_{11} SAT2	V_{10}=6 V dc, I_{11} SINK=4 mA	100	700	mV
Output Leakage Current, I_{11} LEAKAGE	V_{10}=2.25 V dc, V_{11}=12 V dc	−0.2	1.0	μA
Output Sink Current, I_{13} SINK	V_{10}=6 V dc, V_{13}=1.5 V dc	6	—	mA
Output Saturation Voltage, V_{13} SAT	V_{10}=6 V dc, I_{13} SINK=4 mA	100	700	mV
Output Leakage Current, I_{13} LEAKAGE	V_{10}=2.25 V dc, V_{13}=12 V dc	−0.2	1.0	μA
Output Sink Current, I_{14} SINK	V_{15}=0 V dc, V_{14}=1.5 V dc	6	—	mA
Output Saturation Voltage, V_{14} SAT	V_{15}=0 V dc, I_{14} SINK=4 mA	100	700	mV
Output Leakage Current, I_{14} LEAKAGE	V_{15}=2.25 V dc, V_{14}=12 V dc	−0.2	1.0	μA
AFT Center Reference Voltage, V_{13} REF	(See Fig. 2)	2.8	3.2	V dc
AFT Window Reference Voltage Low, V_{11} REF LOW	(See Fig. 2)	0.8	1.2	V dc
AFT Window Reference Voltage High, V_{11} REF HIGH	(See Fig. 2)	4.95	5.05	V dc
Vertical Output Reference, V_{14} REF	(See Fig. 2)	1.3	1.7	V dc

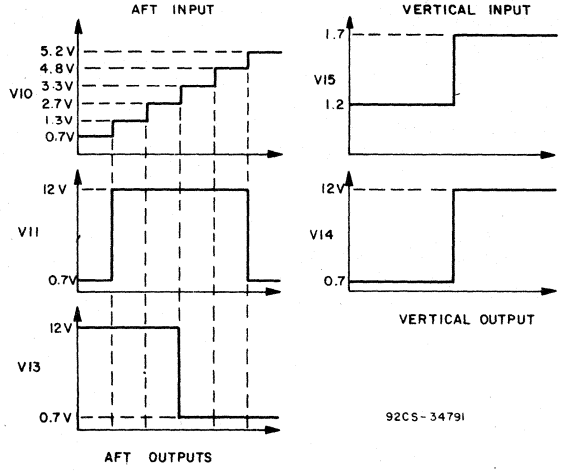
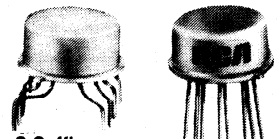


Fig. 2 - Quad comparator action.

CA3193, CA3193A, CA3193B Types



S Suffix
8-LEAD TO-5
with Dual-In-Line
Formed Leads
"DIL-CAN"
H-1787

T Suffix
8-LEAD TO-5
H-1528

E Suffix
8-LEAD Dual-
In-Line Plastic
Package "Mini-DIP"
H-1817

BiMOS Precision Operational Amplifier

FEATURES:

- *Low V_{IO}: 75 μV max. (CA3193B)*
  200 μV max. (CA3193A)
  500 μV max. (CA3193)
- *Low $\Delta V_{IO}/\Delta T$: 2 μV/° C max. (CA3193B)*
  3 μV/° C max. (CA3193A)
  5 μV/° C max. (CA3193)
- *Low I_{IO} and I_I*
- *Low $\Delta I_{IO}/\Delta T$: 50 pA/° C max. (CA3193B)*
  150 pA/° C max. (CA3193)
- *Low $\Delta I_I/\Delta T$: 0.5 nA/° C max. (CA3193B)*
  3.7 nA/° C max. (CA3193)
- *Extremely high gain:*
  120 dB min. (CA3193B)
  110 dB min. (CA3193A)
  100 dB min. (CA3193)
- *Low VIO vs. time*
- *High CMRR and PSRR*
- *Internally compensated: 1.2-MHz gain-bandwidth product*
- *Low input noise: 0.1 Hz to 10 Hz*
  Noise voltage: 0.36 μVp-p typ.
  Noise current: 12 pAp-p typ.

APPLICATIONS

- *Thermocouple preamplifiers*
- *Strain-gauge bridge amplifiers*
- *Summing amplifiers*
- *Differential amplifiers*
- *Bilateral current sources*
- *Log amplifiers*
- *Differential voltmeters*
- *Precision voltage references*
- *Active filters*
- *Buffers*
- *Integrators*
- *Sample-and-hold circuits*
- *Low frequency filters*

The CA3193B, CA3193A and CA3193 are ultra-stable, precision-instrumentation, operational amplifiers that employ both PMOS and bipolar transistors on a single monolithic chip. The CA3193-series amplifiers are internally phase-compensated and provide a gain-bandwidth product of 1.2 MHz. They are pin-compatible with the industry 741 series and many other IC op amps, and may be used as replacements for 741-series types in most applications.

The CA3193 series can also be used as functional replacements for op-amp types 725, 108A, OP-5, OP-7, LM11 and LM714 in many applications where nulling is not employed. Because of their low offset voltage and low offset voltage-versus-temperature coefficient, the CA3193-series amplifiers have a wider range of applications than most op amps and are particularly well suited for use as thermocouple amplifiers, high-gain filters, buffers, strain-gauge bridge amplifiers and precision voltage references.

The three types in the CA3193 series are functionally identical. The CA3193B, however, operates from supply voltages of ±3.5 V to ± 22 V and has an operating temperature range of -55° C to +125° C. The CA3193 and CA3193A operate from supply voltages of ± 3.5 V to ± 18 V and have operating temperature ranges of -25° C to +85° C and 0° C to +70° C, respectively.

The CA3193-series types are supplied in standard 8-lead TO-5-style (T suffix), 8-lead dual-in-line formed lead TO-5-style (DIL-CAN—S suffix) and 8-lead dual-in-line plastic (Mini-DIP—E suffix) packages.

Circuit Description
The block diagram of the CA3193 amplifier, Fig. 2, shows the voltage gain and supply current for each of its four amplifier stages. Simplified and complete schematic diagrams of the CA3193 amplifier are shown in Figs. 3 and 4, respectively.

Absolute-Maximum Ratings, *Absolute-Maximum Values at $T_A = 25°C$*

	CA3193	CA3193A	CA3193B	
DC Supply Voltage	±18	±18	±22	V
Differential-Mode Input Voltage	±5	±5	±5	V
Common-Mode DC Input Voltage	(V+ −4), V−	(V+ −4), V−	(V+ −4), V−	V
Input Terminal Current	1	1	1	mA
Device Dissipation				
Without Heat Sink				
Up to 55 °C	630	630	630	mW
Above 55 °C	Derate Linearly 6.67			mW/°C
Temperature Range	0 to 70	−25 to 85	−55 to 125	°C
Output Short-Circuit Duration*	Indefinite	Indefinite	Indefinite	
Lead Temperature (During Soldering) at distance of 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	±265	±265	±265	°C

*Short circuit may be applied to ground or to either supply.

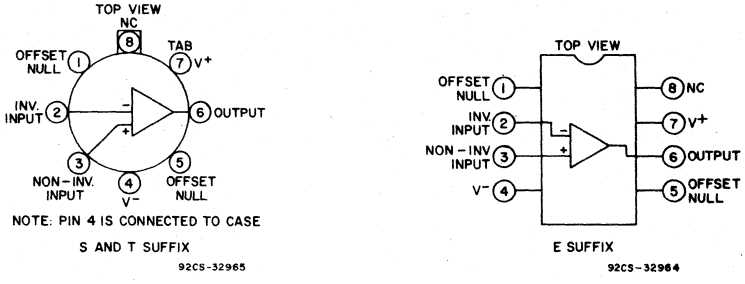


Fig. 1 — Functional diagram of CA3193 series.

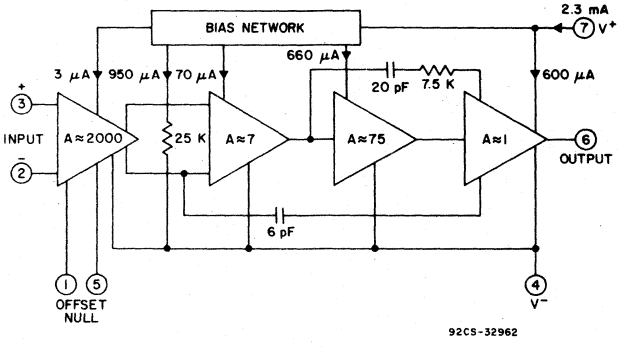


Fig. 2 — Block diagram of CA3193 series.

Circuit Description (cont'd)

A quad of physically cross-connected n-p-n transistors comprise the input-stage differential pair (Q1,Q2 in Figs. 3 and 4); this arrangement contributes to the low input offset-voltage characteristics of the amplifier. The ultra-high gain provided in the first stage ensures that subsequent stages cannot significantly influence the overall offset-voltage characteristics of the amplifier. High load impedances for the input-stage differential pair (Q1,Q2) are provided by the cascode-connected p-n-p transistors Q3,Q5 and Q4,Q6, thereby contributing to the high gain developed in the stage.

The second stage of the amplifier consists of a differential amplifier employing PMOS/FETs (Q7,Q8 in Figs. 3 and 4) with

CA3193, CA3193A, CA3193B Types

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 15$ V and $V^- = 15$ V unless otherwise specified.

CHARACTERISTIC	LIMITS									UNITS
	CA3193B			CA3193A			CA3193			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	40	75	—	140	200	—	300	500	μV
V_{IO} @ Max.Temp.	—	—	275	—	—	380	—	—	725	μV
Input Offset Voltage Temp.Coefficient, $\Delta V_{IO}/\Delta T$ (Over specified temperature range for each device)	—	0.60	2	—	1	3	—	1	5	μV/°C
Input Offset Current, I_{IO}	—	1	3	—	3	5	—	5	10	nA
$\|I_{IO}\|$ @ Max.Temp.	—	—	8	—	—	11	—	—	17	nA
Input Offset Current Temp. Coefficient, $\Delta I_{IO}/\Delta T$ (Over specified temperature range for each device)	—	0.01	0.05	—	0.03	0.10	—	0.04	0.15	nA/°C
Input Bias Current, I_I	—	6	15	—	10	20	—	20	40	nA
$\|I_B\|$ @ Max.Temp.	—	—	60	—	—	83	—	—	207	nA
Input Bias Current Temp. Coefficient, $\Delta I_I/\Delta T$	—	0.08	0.50	—	0.10	1.18	—	0.15	3.70	nA/°C
Input Noise Voltage, e_n p-p (0.1 to 10 Hz)	—	0.36	0.60	—	0.36	—	—	0.36	—	μV p-p
Input Noise Voltage Density, e_n										
$f_O = 10$ Hz	—	25	50	—	25	—	—	25	—	
$f_O = 100$ Hz	—	25	45	—	25	—	—	25	—	
$f_O = 1000$ Hz	—	24	45	—	24	—	—	24	—	nV/$\sqrt{\text{Hz}}$
$f_O = 10$ kHz	—	24	45	—	24	—	—	24	—	
$f_O = 100$ kHz	—	22	40	—	22	—	—	22	—	
Input Noise Current, i_n p-p (0.1 to 10 Hz)	—	12	20	—	12	20	—	12	20	pA p-p
Input Noise Current Density, i_n										
$f_O = 10$ Hz	—	0.83	2.30	—	0.83	—	—	0.83	—	
$f_O = 100$ Hz	—	0.80	1.20	—	0.80	—	—	0.80	—	
$f_O = 1000$ Hz	—	0.75	1.00	—	0.75	—	—	0.75	—	pA/$\sqrt{\text{Hz}}$
$f_O = 10$ kHz	—	0.72	0.80	—	0.72	—	—	0.72	—	
$f_O = 100$ kHz	—	0.60	0.80	—	0.60	—	—	0.60	—	

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V+ = 15$ V and $V- = 15$ V (Cont'd) unless otherwise specified.

CHARACTERISTIC	LIMITS									UNITS
	CA3193B			CA3193A			CA3193			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Common-Mode Input Voltage Range, V_{ICR}	−12	−13.5 to 11.5	10	−12	−13.5 to 11.5	10	−12	−13.5 to 11.5	10	V
Common-Mode Rejection Ratio, ($V_{CM} = V_{ICR}$)	120	130	—	110	115	—	100	110	—	dB
		0.316	1		1.78	3.16		3.16	10	μV/V
Power Supply Rejection Ratio, PSRR, $\Delta V_{IO}/\Delta V\pm$	110	130	—	100	130	—	100	130	—	dB
		0.316	3.16		0.316	10		0.316	10	μV/V
Maximum Output Voltage Swing ($R_L \geq 2$ KΩ)	±13.0	±13.5	—	±13.0	±13.5	—	±13.0	±13.5	—	V
Large-Signal Voltage Gain ($V_O = \pm 10$)										
$R_L \geq 1$ KΩ	—	115	—	—	—	—	—	—	—	
$R_L \geq 2$ KΩ	120	125	—	110	115	—	100	110	—	dB
$R_L \geq 10$ KΩ	—	130	—	—	125	—	—	115	—	
Short-Circuit Output Current to the Opposite Rail, $I_{OM}+$, $I_{OM}-$	−25	±7	25	−25	±7	25	−25	±7	25	mA
Slew Rate, SR ($R_L \geq 2$ KΩ; Unity Gain Voltage Follower)	—	0.25	—	—	0.25	—	—	0.25	—	V/μs
Gain-Bandwidth Product, f_t $A_{OL} = 0$ dB $R_L = 2$ kΩ $C_L = 100$ pF $V_{IN} = 20$ f = 1 kHz	—	1.20	—	—	1.20	—	—	1.20	—	MHz
Small-Signal Transient Response, t_r (V_{IN} = 20 mV p-p, f = 1 kHz	—	0.29	—	—	0.29	—	—	0.29	—	μs
Supply Current, $R_L = \infty$ $V+ = 15$, $V- = -15$	—	2.3	3.5	—	2.3	3.5	—	2.3	3.5	mA
Temperature Range	−55	—	125	−25	—	85	0	—	70	°C

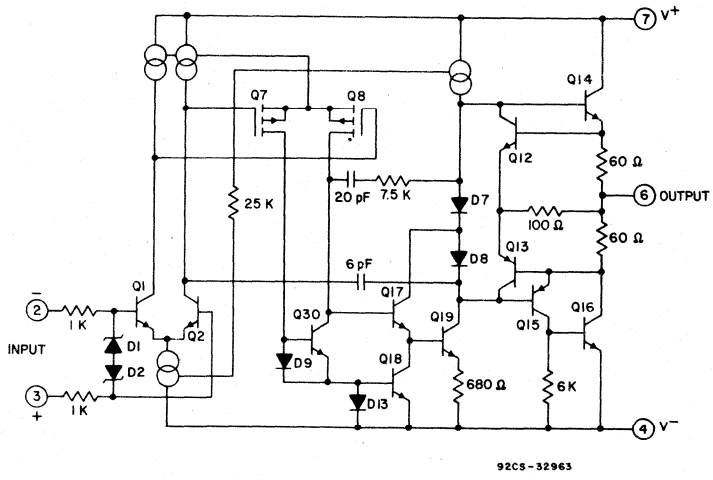


Fig. 3 — CA3193 simplified schematic diagram.

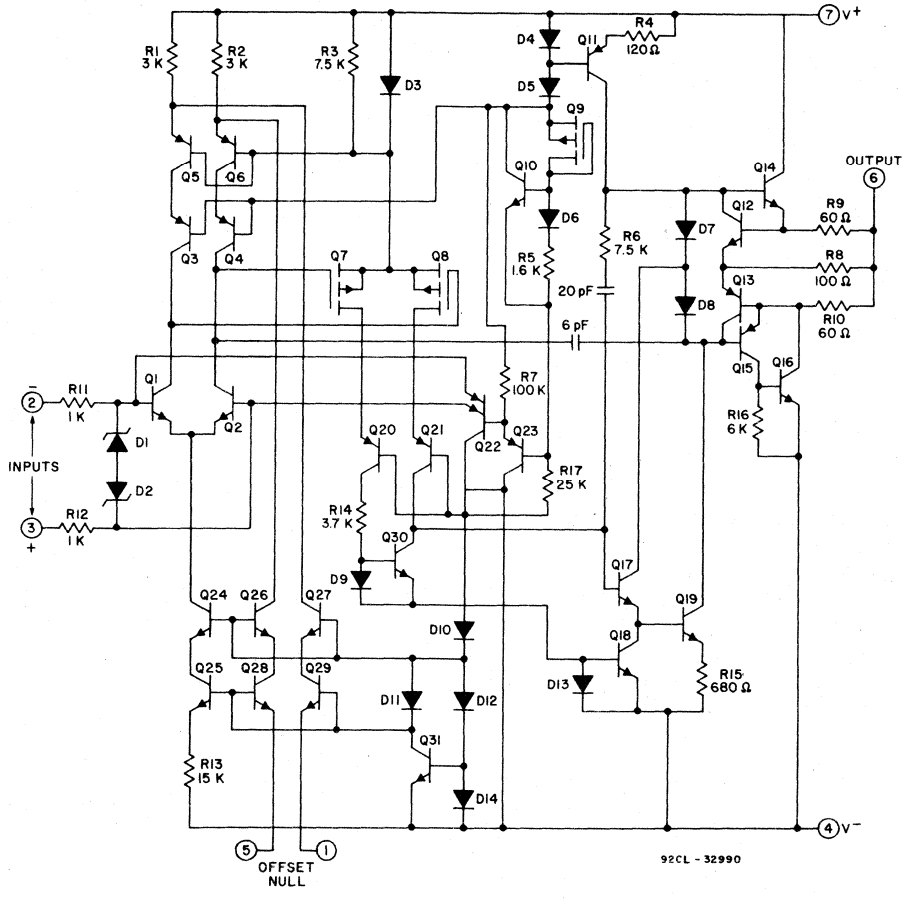


Fig. 4 — Schematic diagram of CA3193 series.

Circuit Description (cont'd)

appropriate drain loading. Since Q7 and Q8 are MOS/FETs, their loading on the first stage is quite low, thereby making an additional contribution to the high gain developed in the first stage. The second stage is also configured to convert its differential signal to a single-ended output signal by means of current mirror D9,Q30 (Figs. 3 and 4) to drive subsequent gain stage.

The third stage of the amplifier consists of Darlington-connected n-p-n transistors (Q17,Q19 in Figs. 3 and 4), driving the quasi-complementary Class AB output stage (Q14 and Q15,Q16 in Figs. 3 and 4). Output-stage short-circuit protection is activated by voltage drops developed across the 60-ohm resistors adjacent to the output terminal (R9 and R10, Fig. 4). When the voltage drop developed across either of these resistors reaches a potential equal to 1 V_{be}, the respective protective transistor (Q12 or Q13) is activated and shunts the base drive from the bases of the output stage transistors (Q14 and Q15,Q16).

Internal frequency compensation for the CA3193 amplifier is provided by two internal networks, a 6-pF capacitor connected between the input-stage transistor collectors and the node between the third and output stages and a second network, consisting of a 20-pF capacitor in series with a 7.5-KΩ resistor connected between the input and output nodes of the third stage.

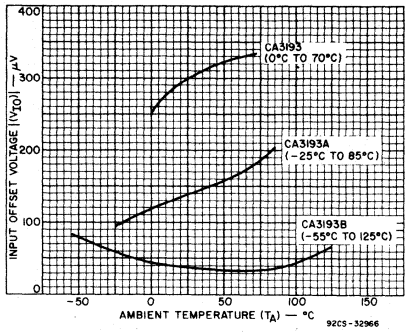


Fig. 5 — Typical input offset-voltage temperature characteristic for CA3193 series.

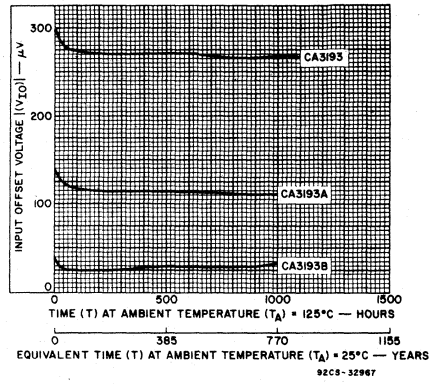


Fig. 6 — Input offset voltage vs. time.

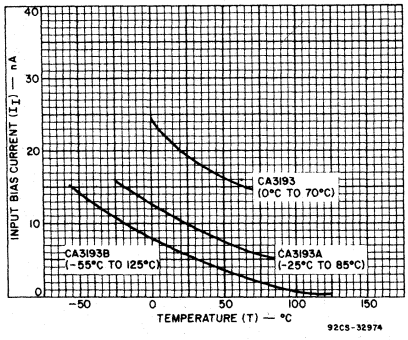


Fig. 7 — Typical input bias current vs. temperature

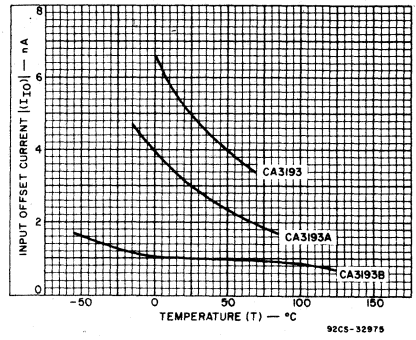


Fig. 8 — Typical input offset current vs. temperature.

CA3193, CA3193A, CA3193B Types

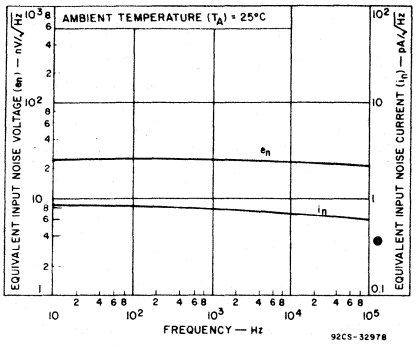


Fig. 9 — Input noise voltage and current density vs. frequency.

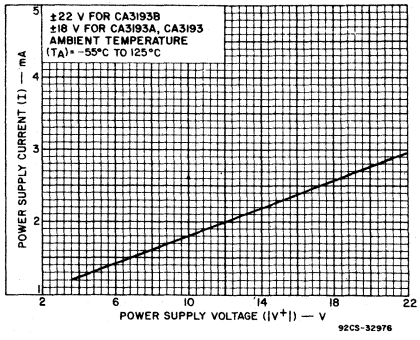


Fig. 10 — Power supply voltage (V+, V−) vs. supply current.

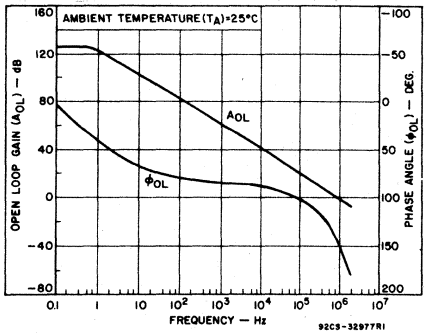


Fig. 11 — Open-loop gain and phase-shift response for CA3193B.

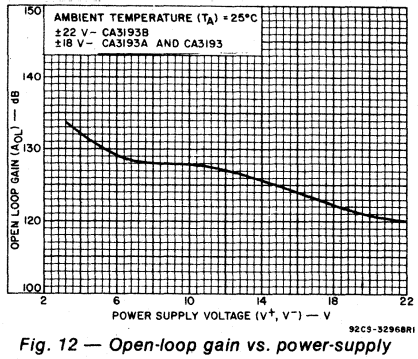


Fig. 12 — Open-loop gain vs. power-supply voltage.

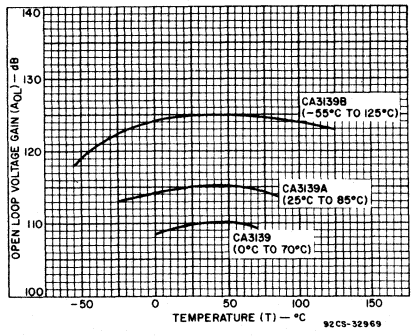
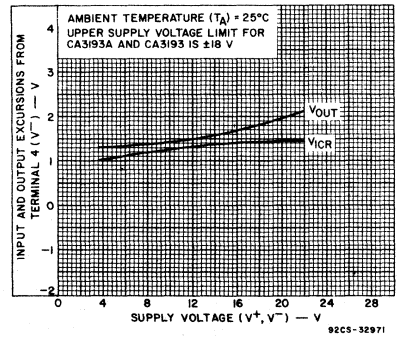


Fig. 13 — Open-loop gain vs. temperature for CA3193 series.



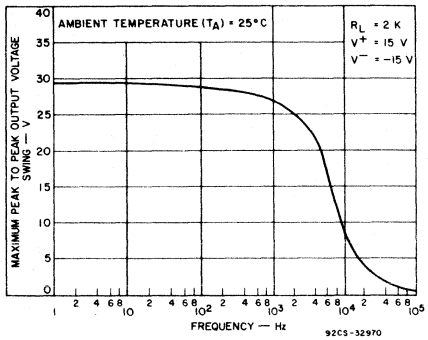


Fig. 14 — Maximum undistorted output voltage vs. frequency.

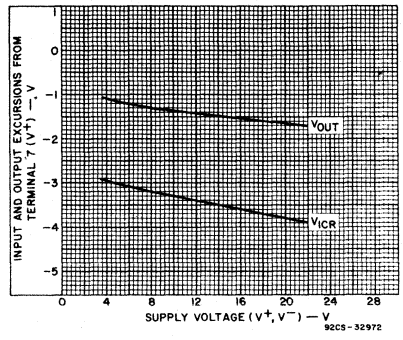


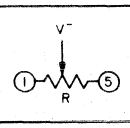
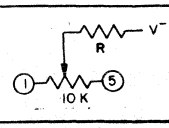
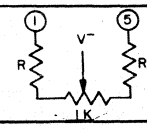
Fig. 15 — Output-voltage-swing capability and common-mode input-voltage vs. supply voltage.

Offset Voltage Nulling

The input offset voltage can be nulled to zero by any of the three methods shown in the table below. A 10K potentiometer between terminals 1 and 5, with its wiper returned to V⁻, will provide a gross nulling for all types. For finer nulling, either of the other two circuits shown below may be used, thus providing simpler improved resolution for all types.

CAUTION: The CA3193 amplifiers will be damaged if they are plugged into op-amp circuits employing nulling with respect to the V+ supply bus.

Offset Voltage Nulling

Offset Nulling Circuits			
Type	**Resistor R Value**	**Resistor R Value**	**Resistor R Value**
CA3193B CA3193A CA3193	10K 10K 10K	100K 50K 20K	20K 10K 5K
	Gross Offset Adjustment	Finer Offset Adjustments	

Test Circuits

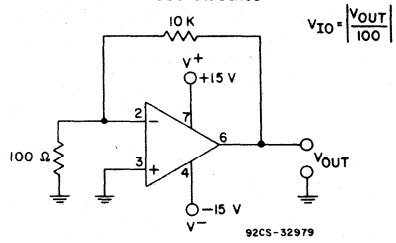
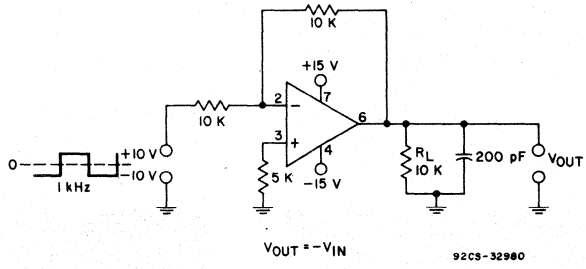
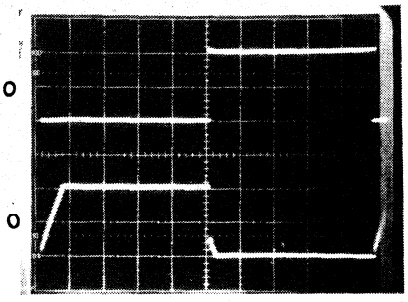


Fig. 16 - Input offset voltage test circuit.



a



TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

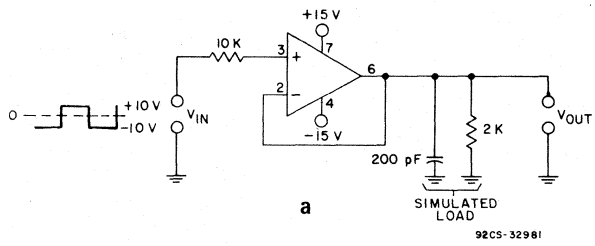
VERT.: $\frac{10\,V}{DIV}$ $V^+ = 15\,V$ $V^- = -15\,V$

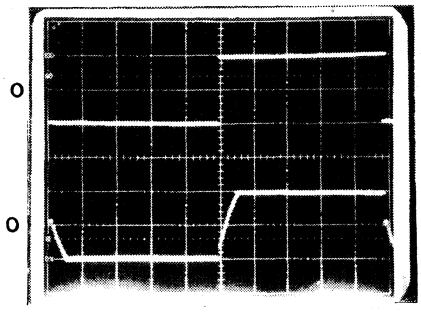
HOR.: $\frac{.1\,ms}{DIV}$ $R_L = 10\,K$

92CS-32989

b

Fig. 17 - Inverting amplifier (a) test circuit (b) response to 1-kHz, 20-V p-p square wave.





TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT: 10 V / DIV

HOR : .1 ms / DIV

V+ = 15 V

V⁻ = 15 V

R_L = 2K

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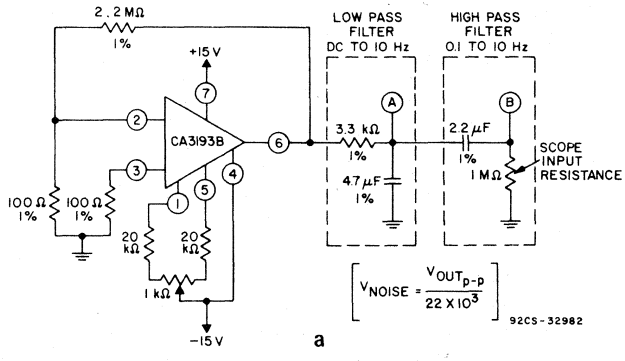
Fig. 18 - Voltage follower (a) test circuit (b) response to 20-V p-p, 1-kHz square-wave input.



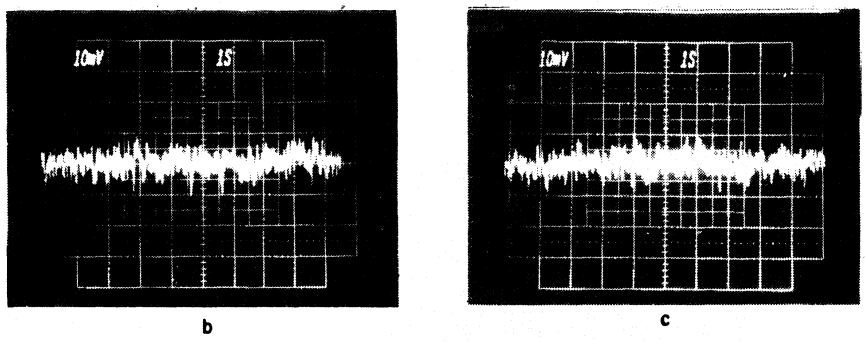
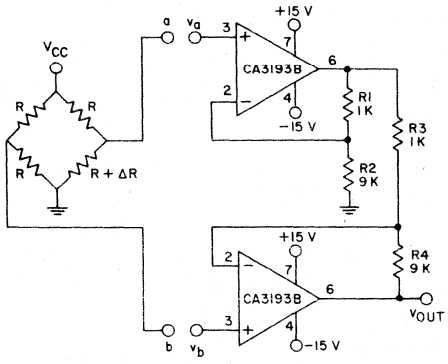


Fig. 19 - Low frequency noise (a) test circuit—0.1 to 10 Hz (b) output A waveform—0 to 10 Hz noise (c) output B waveform—0 to 10 Hz noise.

Application Circuits



$$V_{OUT} = -V_a\left(\frac{R2}{R1}+1\right)\frac{R4}{R3} + V_b\left(\frac{R4}{R3}+1\right)$$

FOR IDEAL RESISTORS WITH $\frac{R1}{R2} = \frac{R3}{R4}$

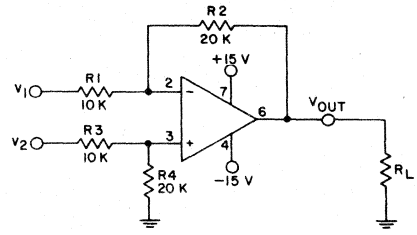
$$V_{OUT} = V_b - V_a\left(\frac{R4}{R3}+1\right)$$

$$A = \frac{V_{OUT}}{V_b - V_a} = \left(\frac{R4}{R3}+1\right)$$

FOR VALUES ABOVE $V_{OUT} = (V_b - V_a)(10)$

92CS-32984

Fig. 20 - Typical two-op amp bridge-type differential amplifier.



$$V_{OUT} = V_2\left(\frac{R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right) - V_1\left(\frac{R2}{R1}\right)$$

IF R4 = R2, R3 = R1 AND $\frac{R2}{R1} = \frac{R4}{R3}$

THEN $V_{OUT} = (V_2 - V_1)\left(\frac{R2}{R1}\right)$

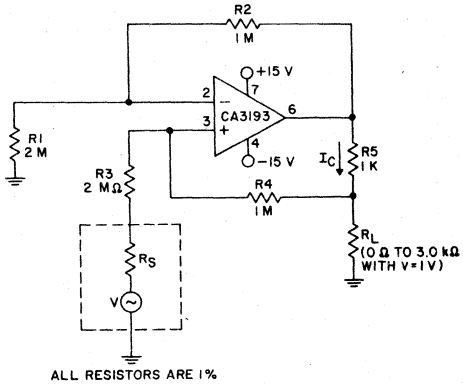
FOR VALUES ABOVE $V_{OUT} = 2(V_2 - V_1)$

IF A_V IS TO BE MADE 1 AND IF R1 = R3 = R4 = R WITH R2 = 0.999 R (0.1% MISMATCH IN R2)

THEN $V_{OCM} = 0.0005\ V_{IN}$ OR CMRR = 66 dB
THUS, THE CMRR OF THIS CIRCUIT IS LIMITED BY THE MATCHING OR MISMATCHING OF THIS NETWORK RATHER THAN THE AMPLIFIER.

92CS-32983

Fig. 21 - Differential amplifier (simple subtractor) using CA3193B.



ALL RESISTORS ARE 1%

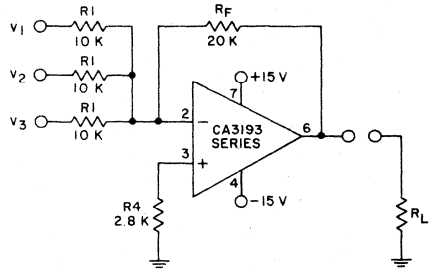
IF R1 = R3 AND R2 ≈ R4 + R5 THEN

I_L IS INDEPENDENT OF VARIATIONS IN R_L FOR R_L VALUES OF 0 Ω TO 3 kΩ WITH V = 1 V

$$I_L = \frac{V}{R3\,R5} = \frac{V}{(2\,M)(1K)} = \frac{V}{2\,K} = 500\ \mu A$$

92CS-32985

Fig. 22 - Using CA3193B as a bilateral current source.



$$V_{OUT} = -\left(\frac{R_F}{R1}V_1 + \frac{R_F}{R1}V_2 + \frac{R_F}{R1}V_3\right)$$

$$V_{OUT} = -(2V_1 + 2V_2 + 2V_3)$$

92CS-32973

Fig. 23 - Typical summing amplifier application.

CA3193, CA3193A, CA3193B Types

The CA3193B is an excellent choice for use with thermocouples. In Fig. 24, the CA3193B amplifies the signal generated 500 times. The three 22-megohm resistors will provide full-scale output if the thermocouple opens.

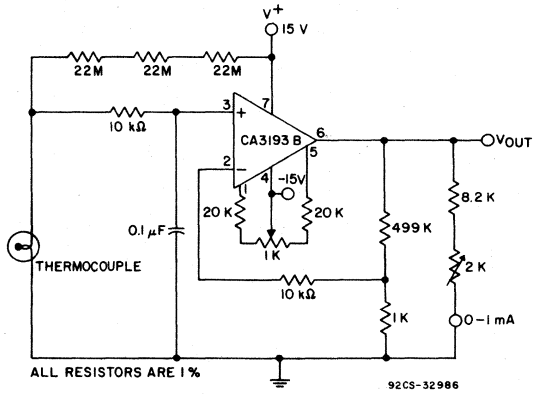
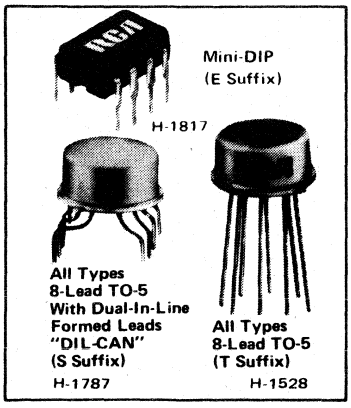


Fig. 24 - The CA3193B used in a thermocouple circuit.



Low-Supply Voltage, Low-Input Current BiMOS OP-AMPS

Features:

- *2 V Supply at 300 μA Supply Current*
- *1 pA (typ) Input Current (Essentially Constant to 85° C)*
- *Rail-to-Rail Output Swing (Drive ±2 mA into 1 KΩ Load)*
- *Pin Compatible with 741 Op-Amp*
- *Low Cost 8-Lead Minidip, TO-5*

Applications:

- *pH Probe Amplifiers*
- *Picoammeters*
- *Electrometer (High Z) instruments*
- *Portable Equipment*
- *Inaccessible Field Equipment*
- *Battery Dependent Equipment (Medical and Military)*

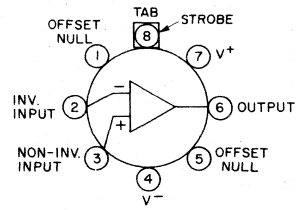
The RCA-CA3420B, CA3420A, and CA3420• are integrated-circuit operational amplifiers that combine PMOS transistors and BiPolar transistors on a single monolithic chip. The CA3420B, CA3420A, and CA3420 BIMOS operational amplifiers feature gate-protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 1 pA). The internal bootstrapping network features a unique guard-banding technique for reducing the doubling of leakage current for every 10° C increase in temperature. The CA3420 series operates at total supply voltages from 2 to 20 volts either single or dual supply. These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Additionally, they have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.45 volt below the negative supply terminal, an important attribute for single-supply application. The output stage uses a feedback OTA type amplifier that can swing essentially from rail-to-rail. The output driving current of 1.5 mA MIN is provided by using non-linear current mirrors.

The CA3420-series has the same 8-lead pin-out used for the industry standard 741. They are supplied in the standard 8-lead TO-5 style package (S suffix, and T suffix); in the standard 8-lead dual-in-line plastic package (Minidip - E suffix), and are also available in chip form (H suffix).

• **Formerly Dev. Type No. TA10841**

TERMINAL ASSIGNMENTS

TOP VIEW

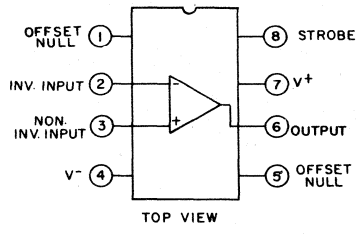


NOTE: PIN 4 IS CONNECTED TO CASE

92CS-33997

S AND T SUFFIXES

TOP VIEW



TOP VIEW

92CS-29086

E SUFFIX

CA3420, CA3420A, CA3420B

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25° C):

DC Supply Voltage
(Between V^+ and V^- Terminals) ..... 22 V
Differntial-Mode
Input Voltage ..... ±15 V
Common-Mode DC
Input Voltage ..... (V^+ + 8 V) to (V^- -0.5 V)
Input-Terminal Current ..... 1 mA
Device Dissipation:
Without Heat Sink —
Up to 55° C ..... 630 mW
Above 55° C ..... Derate linearly 6.67 mW/° C
With Heat Sink -
Up to 110° C ..... 630 mW
Above 110° C ..... Derate linearly 16.7 mW° C

Temperature Range:
Operating (All Types) ..... -55 to +125° C
Storage (All Types) ..... -65 to +150° C
Output Short-Circuit
Duration* ..... Indefinite
Lead Temperature
(During Soldering):
At Distance 1/16 ± 1/32 Inch
(1.59 ± 0.79 mm) from case
For 10 seconds max. ..... +265° C

*Short circuit may be applied to ground or to either supply.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

Characteristic		Test Conditions V+ = +10V; V- = -10V TA = 25° C		CA3420B (T,S)	CA3420A (T,S,E)	CA3420 (T,S,E)	Units
Input Resistance	R_I			150	150	150	TΩ
Input Capacitance	C_I			4.9	4.9	4.9	pF
Output Resistance	R_O			300	300	300	Ω
Equivalent Input Noise Voltage	e_n	f = 1 KHz	R_S 100 Ω	62	62	62	nV/ Hz
		f = 10 KHz		38	38	38	
Short-Circuit Current Source Source IOM+				2.6	2.6	2.6	mA
To Opposite Supply Sink IOM-				2.4	2.4	2.4	mA
Gain-Bandwidth Product	f_T			0.5	0.5	0.5	MHz
Slew Rate	SR			0.5	0.5	0.5	V/μs
Transient Response Rise Time tr		R_L = 2 K Ω		0.7	0.7	0.7	μs
Overshoot		C_L = 100 pF		15	15	15	%
Current from Terminal 8 To V-	I_{8+}			20	20	20	μA
Current from Terminal 8 To V+	I_{8-}			2	2	2	mA

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V+ = 1V, V- = -1V, TA = 25°C unless otherwise specified

Characteristic	Limits									Units
	CA3420B			CA3420A			CA3420			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $\|V_{IO}\|$	—	0.8	2	—	2	5	—	5	10	mV
Input Offset Current $\|I_{IO}\|$ *	—	0.01	4.0	—	0.01	4	—	0.01	4	pA
Input Current $\|I_I\|$ *	—	0.02	5	—	0.02	5	—	1	5	pA
Large-Signal Voltage Gain	20K	100K	—	20K	100K	—	10K	100K	—	V/V
AOL (R_L = 10 KΩ)	86	100	—	86	100	—	80	100	—	dB
Common-Mode	—	320	560	—	560	1000		560	1800	μV/V
Rejection Ratio CMRR	65	70	—	60	65	—	55	65	—	dB
Common-Mode Input VICR +	+0.2	+0.5	—	+0.2	+0.5	—	+0.2	+0.5	—	V
Voltage Range VICR -	-1	-1.3	—	-1	-1.3	—		-1.3	—	V
Power Supply Rejection	—	20	180	—	32	320	—	100	1000	μV/V
Ratio PSRR ΔVIO/ΔV	75	94	—	70	90	—	60	80	—	dB
Max Output Voltage VOM +	+0.90	+0.95	—	+0.90	+0.95	—	+0.90	+0.95	—	V
RL = 00 VOM -	-0.85	-0.91	—	-0.85	-0.91	—	-0.85	-0.91	—	V
Supply Current I+	—	350	650	—	350	650	—	350	650	μA
Device Dissipation P_D	—	0.7	1.1	—	0.7	1.1	—	0.7	1.1	mW
Input Offset Voltage Temp. Drift ΔVIO/ΔT	—	4	—	—	4	—	—	4	—	μV/°C

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V+ = 10V, V- = -10V, TA = 25°C unless otherwise specified

Characteristic	Limits									Units
	CA3420B			CA3420A			CA3420			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $\|V_{IO}\|$	—	0.8	2	—	2	5	—	5	10	mV
Input Offset Current $\|I_{IO}\|$ *	—	0.03	4	—	0.03	4	—	0.03	4	pA
Input Current $\|I_I\|$ *	—	0.05	5	—	0.05	5	—	0.05	5	pA
Large-Signal Voltage Gain	20K	100K	—	20K	100K	—	10K	100K	—	V/V
AQL (R_L = 10K Ω)	86	100	—	86	100	—	80	100	—	dB
Common-Mode	—	32	100	—	100	320	—	100	320	μV/V
Rejection Ratio CMRR	80	90	—	70	80	—	70	80	—	dB
Common-Mode Input VICR +	+9.0	+9.3	—	+9.0	+9.3	—	+8.5	+9.3	—	V
Voltage Range VICR -	-10	-10.3	—	-10	-10.3	—	-10	-10.3	—	V
Power Supply Rejection	—	20	180	—	32	320	—	32	320	μV/V
Ratio PSRR ΔVIO/ΔV	75	94	—	70	90	—	70	90	—	dB
Max Output Voltage VOM +	+9.7	+9.9	—	+9.7	+9.9	—	+9.7	+9.9	—	V
RL = 00 VOM -	-9.7	-9.85	—	-9.7	-9.85	—	-9.7	-9.85	—	V
Supply Current I+	—	450	1000	—	450	1000	—	450	1000	μA
Device Dissipation P_D	—	9	14	—	9	14	—	9	14	mW
Input Offset Voltage Temp. Drift ΔVIO/ΔT	—	4	—	—	4	—	—	4	—	μV/°C

* The maximum limit represents the levels obtainable on high speed automatic test equipment. Typical values are obtained under laboratory conditions.

CA3420, CA3420A, CA3420B

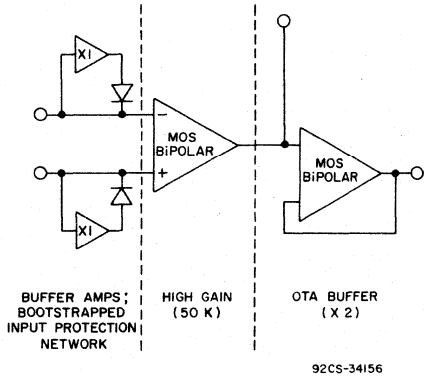


Fig. 1 - Functional diagram for CA3420.

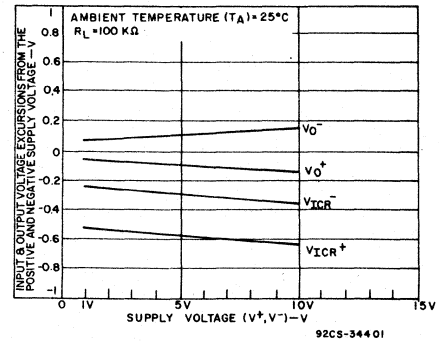


Fig. 2 - Output-voltage-swing and common-mode input-voltage range versus supply voltage.

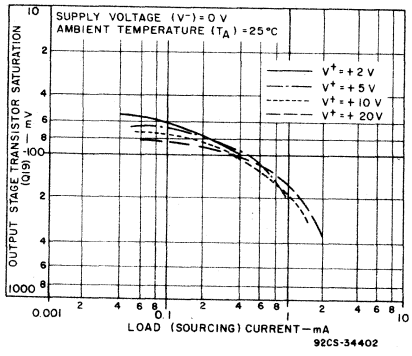


Fig. 3 - Output voltage versus load sourcing current.

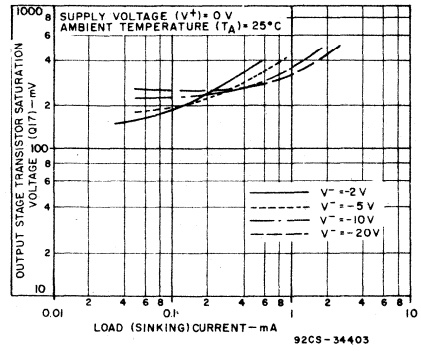


Fig. 4 - Output voltage versus load sinking current.

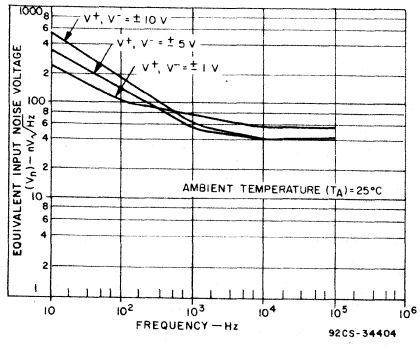


Fig. 5 - Input noise voltage versus frequency.

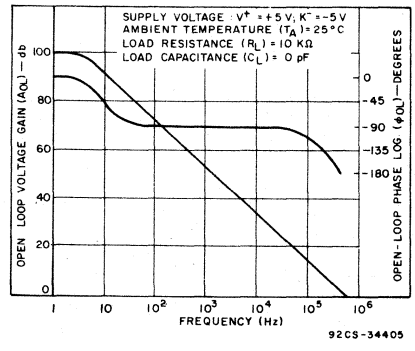


Fig. 6 - Open-loop gain and phase-shift response.

Application Circuits

Picoameter Circuit

The exceptionally low input current (typically 0.2 pA) makes the CA3420 highly suited for use in a picoameter circuit. With only a single 10K megohm resistor, this circuit covers the range from ±1.5 pA. Higher current ranges are possible with suitable switching techniques and current scaling resistors. Input transient protection is provided by the 1-megohm resistor in series with the input. Higher current ranges require that this resistor be reduced. The 10-megohm resistor connected to pin 2 of the CA3420 decouples the potentially high input capacitance often associated with lower current circuits and reduces the tendency for the circuit to oscillate under these conditions.

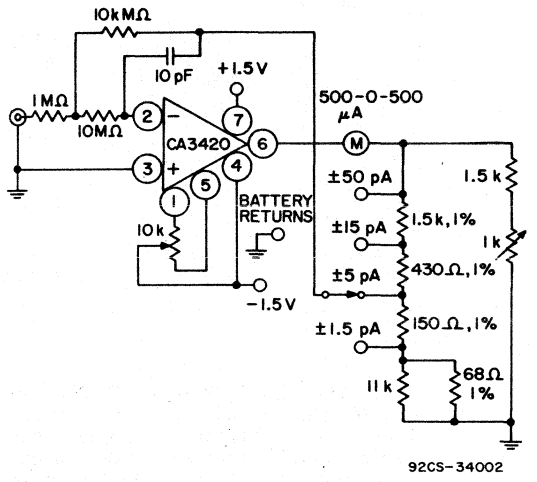


Fig. 7 - Picoameter circuit.

High-Input-Resistance Voltmeter

Advantage is taken of the high input impedance of the CA3420 in a high-input-resistance dc voltmeter. Only two 1.5 V "AA" type penlite batteries power this exceedingly high-input resistance (>1,000,000-megohms) dc voltmeter. Full-scale deflection is ±500 mV, ±150 mV, and ±15 mV. Higher voltage ranges are easily added with external input voltage attenuator networks.

The meter is placed in series with the gain network, thus eliminating the meter temperature coefficient error term.

Supply current in the standby position with the meter undeflected is 300 μA. At full-scale deflection this current rises to 800 μA. Carbon-zinc battery life should be in excess of 1,000 hours.

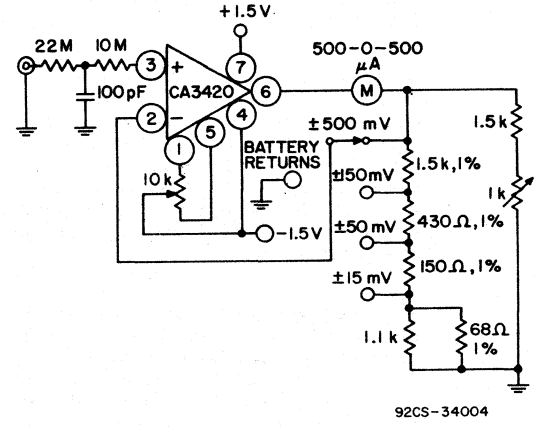
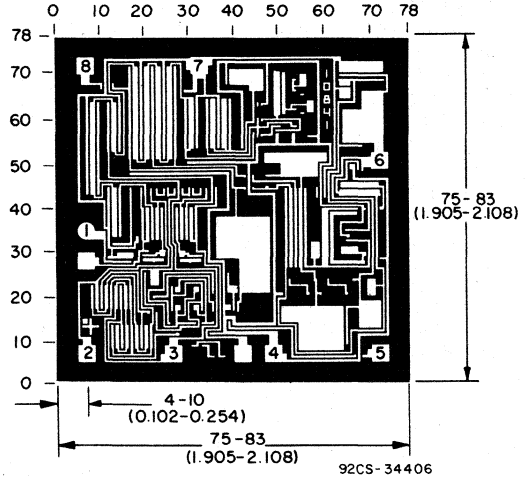


Fig. 8 - High input resistance voltmeter.

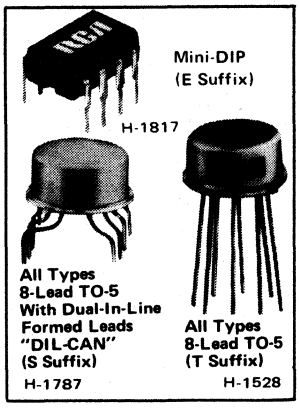


The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CA3420H.

CA3493, CA3493A, CA3493B



BiMOS Precision Operational Amplifier

Features

- *Low V_{IO}: 75 μV max. (CA3493B)*
  200 μV max. (CA3493A)
  500 μV max. (CA3493)
- *Low $\Delta V_{IO}/\Delta T$: 2 μV/°C max. (CA3493B)*
  3 μV/°C max. (CA3493A)
  5 μV/°C max. (CA3493)
- *Low I_{IO} and I_I*
- *Low $\Delta I_{IO}/\Delta T$: 50 pA/°C max. (CA3493B)*
  150 pA/°C max. (CA3493)
- *Low $\Delta I_I/\Delta T$: 0.5 nA/°C max. (CA3493B)*
  3.7 nA/°C max. (CA3493)
- *Extremely high gain:*
  120 dB min. (CA3493B)
  110 dB min. (CA3493A)
  100 dB min. (CA3493)
- *Low V_{IO} vs. time*
- *High CMRR and PSRR*
- *Internally compensated: 1.2-MHz gain-bandwidth product*
- *Low input noise: 0.1 Hz to 10 Hz*
  Noise voltage: 0.36 μV_{p-p} typ.
  Noise current: 12 pA_{p-p} typ.

Applications

- *Thermocouple preamplifiers*
- *Strain-gauge bridge amplifiers*
- *Summing amplifiers*
- *Differential amplifiers*
- *Bilateral current sources*
- *Log amplifiers*
- *Differential voltmeters*
- *Precision voltage references*
- *Active filters*
- *Buffers*
- *Integrators*
- *Sample-and-hold circuits*
- *Low frequency filters*

The CA3493B, CA3493A and CA3493 are ultra-stable, precision-instrumentation, operational amplifiers that employ both PMOS and bipolar transistors on a single monolithic chip. The CA3493-series amplifiers are internally phase-compensated and provide a gain-bandwidth product of 1.2 MHz. They are pin-compatible with many industrial types such as 725, 108A, OP-5, OP-7, LM11 and LM714 where positive nulling is employed.

Because of their low offset voltage and low offset voltage-versus-temperature coefficient, the CA3493-series amplifiers have a wider range of applications than most op amps and are particularly well suited for use as thermocouple amplifiers, high-gain filters, buffers, strain-gauge bridge amplifiers and precision voltage references.

The three types in the CA3493 series are functionally identical. The CA3493B, however, operates from supply voltages of ±3.5 V to ±22 V and has an operating temperature range of −55 °C to +125 °C. The CA3493 and CA3493A operate from supply voltages of ±3.5 V to ±18 V and have operating temperature ranges of −25 °C to +85 °C and 0 °C to +70 °C, respectively.

The CA3493-series types are supplied in standard 8-lead TO-5-style (T suffix), 8-lead dual-in-line formed lead TO-5-style (DIL-CAN—S suffix) and 8-lead dual-in-line plastic (Mini-DIP—E suffix) packages.

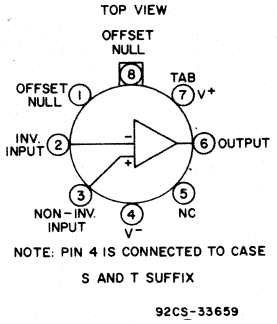
Circuit Description

The block diagram of the CA3493 amplifier, Fig. 2, shows the voltage gain and supply current for each of its four amplifier stages. Simplified and complete schematic diagrams of the CA3493 amplifier are shown in Figs. 3 and 4, respectively.

Absolute-Maximum Ratings, *Absolute-Maximum Values at $T_A = 25°C$*

	CA3493B	CA3493A	CA3493	
DC Supply Voltage	±22	±18	±18	V
Differential-Mode Input Voltage	±5	±5	±5	V
Common-Mode DC Input Voltage	(V+ −4), V−	(V+ −4), V−	(V+ −4), V−	V
Input Terminal Current	1	1	1	mA
Device Dissipation				
Without Heat Sink				
Up to 55°C	630	630	630	mW
Above 55°C		Derate Linearly 6.67		mW/°C
Temperature Range	−55 to 125	−25 to 85	0 to 70	°C
Output Short-Circuit Duration*	Indefinite	Indefinite	Indefinite	
Lead Temperature (During Soldering) at distance of 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	±265	±265	±265	°C

*Short circuit may be applied to ground or to either supply.



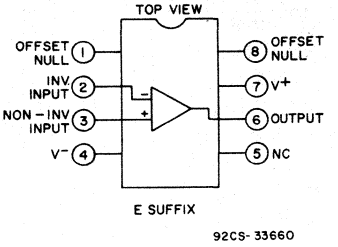


Fig. 1 - Functional diagram of CA3493 series.

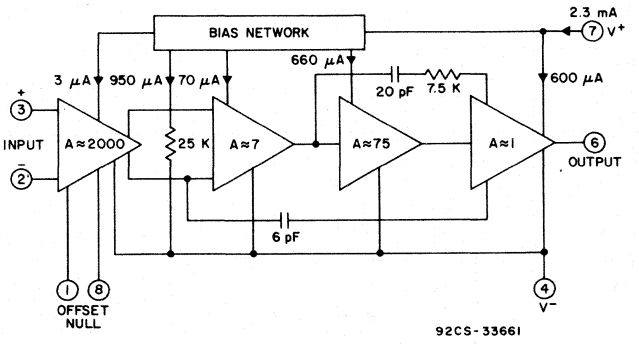


Fig. 2 - Block diagram of CA3493 series.

Circuit Description (cont'd)

A quad of physically cross-connected n-p-n transistors comprise the input-stage differential pair (Q1,Q2 in Figs. 3 and 4); this arrangement contributes to the low input offset-voltage characteristics of the amplifier. The ultra-high gain provided in the first stage ensures that subsequent stages cannot significantly influence the overall offset-voltage characteristics of the amplifier. High load impedances for the input-stage differential pair (Q1,Q2) are provided by the cascode-connected p-n-p transistors Q3,Q5 and Q4,Q6, thereby contributing to the high gain developed in the stage.

The second stage of the amplifier consists of a differential amplifier employing PMOS/FETs (Q7,Q8 in Figs. 3 and 4) with

CA3493, CA3493A, CA3493B

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 15$ V and $V^- = 15$ V unless otherwise specified.

CHARACTERISTIC	LIMITS									UNITS
	CA3493B			CA3493A			CA3493			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	40	75	—	140	200	—	300	500	μV
V_{IO} @ Max.Temp.	—	—	275	—	—	380	—	—	725	μV
Input Offset Voltage Temp.Coefficient, $\Delta V_{IO}/\Delta T$ (Over specified temperature range for each device)	—	0.60	2	—	1	3	—	1	5	μV/°C
Input Offset Current, I_{IO}	—	1	3	—	3	5	—	5	10	nA
$\|I_{IO}\|$ @ Max.Temp.	—	—	8	—	—	11	—	—	17	nA
Input Offset Current Temp. Coefficient, $\Delta I_{IO}/\Delta T$ (Over specified temperature range for each device)	—	0.01	0.05	—	0.03	0.10	—	0.04	0.15	nA/°C
Input Bias Current, I_I	—	6	15	—	10	20	—	20	40	nA
$\|I_B\|$ @ Max.Temp.	—	—	60	—	—	83	—	—	207	nA
Input Bias Current Temp. Coefficient, $\Delta I_I/\Delta T$	—	0.08	0.50	—	0.10	1.18	—	0.15	3.70	nA/°C
Input Noise Voltage, $e_{n\ p\text{-}p}$ (0.1 to 10 Hz)	—	0.36	0.60	—	0.36	—	—	0.36	—	μV p-p
Input Noise Voltage Density, e_n										
$f_O = 10$ Hz	—	25	50	—	25	—	—	25	—	
$f_O = 100$ Hz	—	25	45	—	25	—	—	25	—	
$f_O = 1000$ Hz	—	24	45	—	24	—	—	24	—	nV/
$f_O = 10$ kHz	—	24	45	—	24	—	—	24	—	$\sqrt{Hz}$
$f_O = 100$ kHz	—	22	40	—	22	—	—	22	—	
Input Noise Current, $i_{n\ p\text{-}p}$ (0.1 to 10 Hz)	—	12	20	—	12	20	—	12	20	pA p-p
Input Noise Current Density, i_n										
$f_O = 10$ Hz	—	0.83	2.30	—	0.83	—	—	0.83	—	
$f_O = 100$ Hz	—	0.80	1.20	—	0.80	—	—	0.80	—	
$f_O = 1000$ Hz	—	0.75	1.00	—	0.75	—	—	0.75	—	pA/
$f_O = 10$ kHz	—	0.72	0.80	—	0.72	—	—	0.72	—	$\sqrt{Hz}$
$f_O = 100$ kHz	—	0.60	0.80	—	0.60	—	—	0.60	—	

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 15$ V and $V^- = 15$ V (Cont'd) unless otherwise specified.

CHARACTERISTIC	LIMITS									UNITS
	CA3493B			CA3493A			CA3493			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Common-Mode Input Voltage Range, V_{ICR}	−12	−13.5 to 11.5	10	−12	−13.5 to 11.5	10	−12	−13.5 to 11.5	10	V
Common-Mode Rejection Ratio, ($V_{CM} = V_{ICR}$)	120	130	—	110	115	—	100	110	—	dB
		0.316	1		1.78	3.16		3.16	10	μV/V
Power Supply Rejection Ratio, PSRR, $\Delta V_{IO}/\Delta V \pm$	110	130	—	100	130	—	100	130	—	dB
		0.316	3.16		0.316	10		0.316	10	μV/V
Maximum Output Voltage Swing ($R_L \geq 2$ KΩ)	±13.0	±13.5	—	±13.0	±13.5	—	±13.0	±13.5	—	V
Large-Signal Voltage Gain ($V_O = \pm 10$)										
$R_L \geq 1$ KΩ	—	115	—	—	—	—	—	—	—	
$R_L \geq 2$ KΩ	120	125	—	110	115	—	100	110	—	dB
$R_L \geq 10$ KΩ	—	130	—	—	125	—	—	115	—	
Short-Circuit Output Current to the Opposite Rail, I_{OM}^+, I_{OM}^-	−25	±7	25	−25	±7	25	−25	±7	25	mA
Slew Rate, SR ($R_L \geq 2$ KΩ; Unity Gain Voltage Follower)	—	0.25	—	—	0.25	—	—	0.25	—	V/μs
Gain-Bandwidth Product, f_t $A_{OL} = 0$ dB $R_L = 2$ kΩ $C_L = 100$ pF $V_{IN} = 20$ f = 1 kHz	—	1.20	—	—	1.20	—	—	1.20	—	MHz
Small-Signal Transient Response, t_r ($V_{IN} = 20$ mV p-p, f = 1 kHz	—	0.29	—	—	0.29	—	—	0.29	—	μs
Supply Current, $R_L = \infty$ $V^+ = 15$, $V^- = -15$	—	2.3	3.5	—	2.3	3.5	—	2.3	3.5	mA
Temperature Range	−55	—	125	−25	—	85	0	—	70	°C

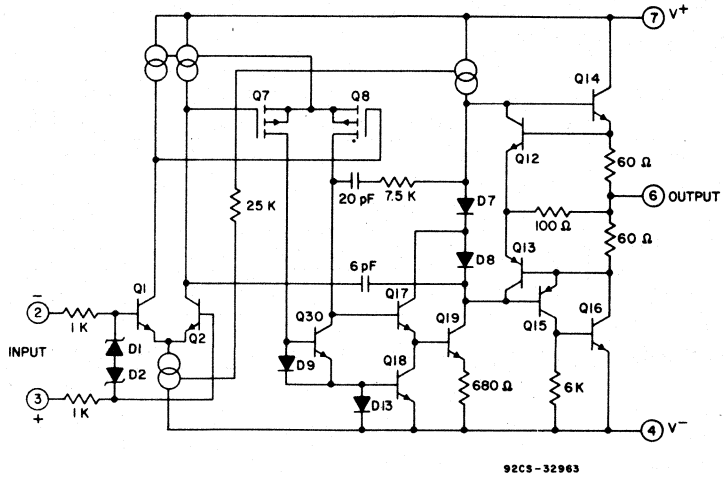


Fig. 3 - CA3493 simplified schematic diagram.

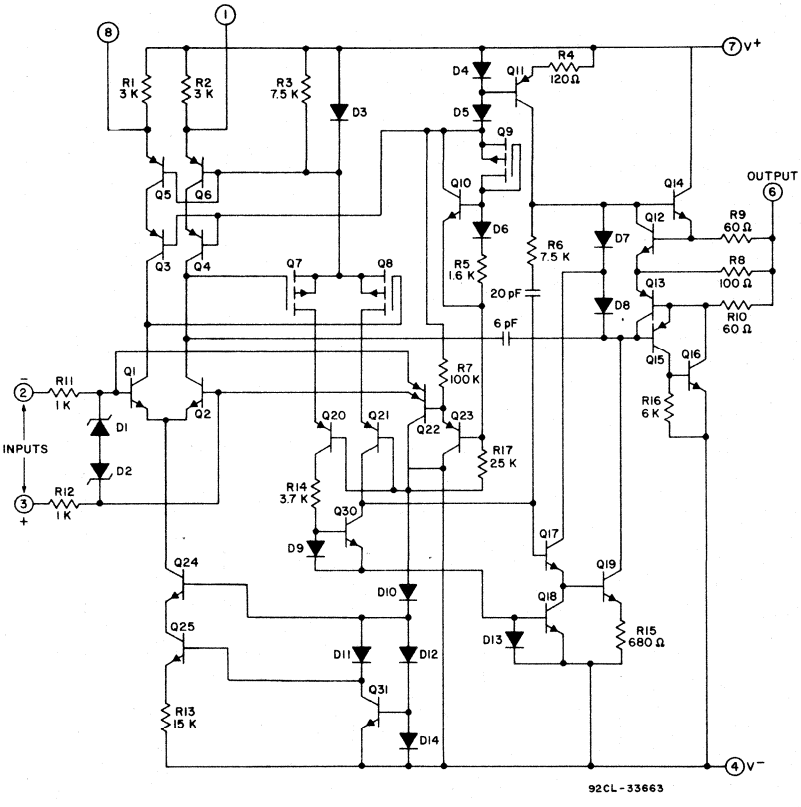


Fig. 4 - Schematic diagram of CA3493 series.

Circuit Description (cont'd)

appropriate drain loading. Since Q7 and Q8 are MOS/FETs, their loading on the first stage is quite low, thereby making an additional contribution to the high gain developed in the first stage. The second stage is also configured to convert its differential signal to a single-ended output signal by means of current mirror D9,Q30 (Figs. 3 and 4) to drive subsequent gain stage.

The third stage of the amplifier consists of Darlington-connected n-p-n transistors (Q17,Q19 in Figs. 3 and 4), driving the quasi-complementary Class AB output stage (Q14 and Q15,Q16 in Figs. 3 and 4). Output-stage short-circuit protection is activated by voltage drops developed across the 60-ohm resistors adjacent to the output terminal (R9 and R10, Fig. 4). When the voltage drop developed across either of these resistors reaches a potential equal to 1 V_{be}, the respective protective transistor (Q12 or Q13) is activated and shunts the base drive from the bases of the output stage transistors (Q14 and Q15,Q16).

Internal frequency compensation for the CA3493 amplifier is provided by two internal networks, a 6-pF capacitor connected between the input-stage transistor collectors and the node between the third and output stages and a second network, consisting of a 20-pF capacitor in series with a 7.5-KΩ resistor connected between the input and output nodes of the third stage.

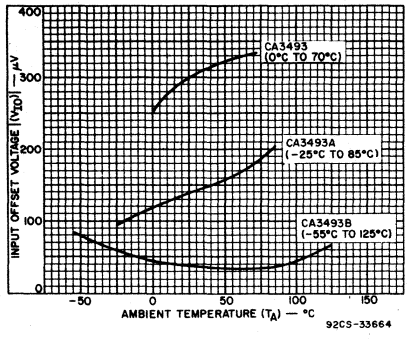


Fig. 5 — Typical input offset-voltage temperature characteristic for CA3493 series.

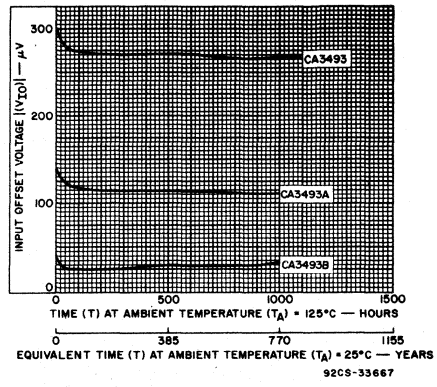


Fig. 6 — Input offset voltage vs. time.

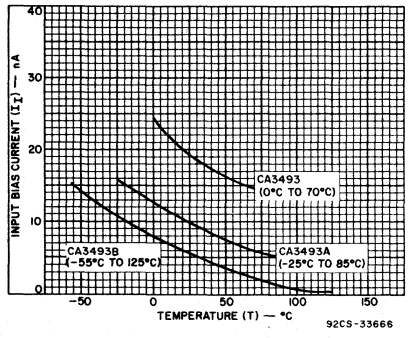


Fig. 7 — Typical input bias current vs. temperature

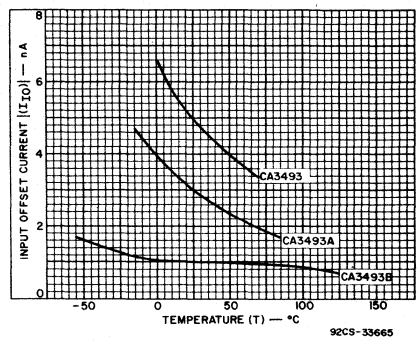


Fig. 8 — Typical input offset current vs. temperature.

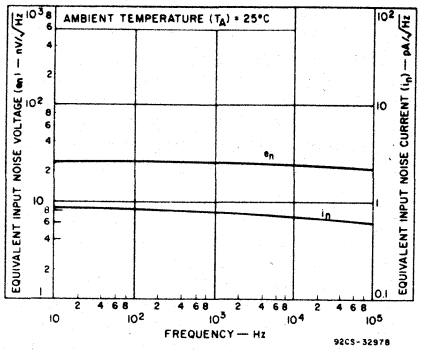


Fig. 9 — Input noise voltage and current density vs. frequency.

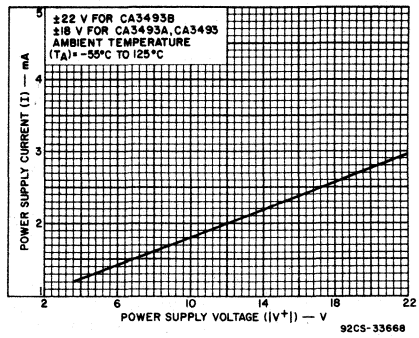


Fig. 10 — Power supply voltage (V+, V−) vs. supply current.

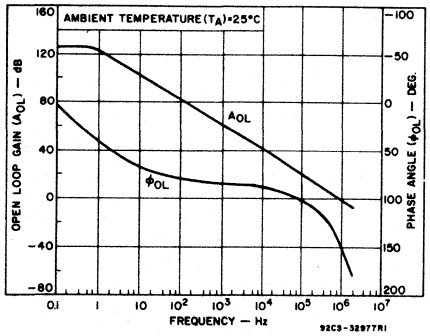


Fig. 11 — Open-loop gain and phase-shift response for CA3493B.

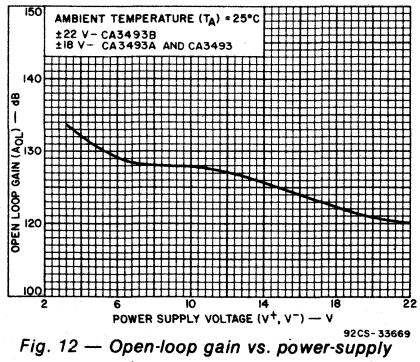


Fig. 12 — Open-loop gain vs. power-supply voltage.

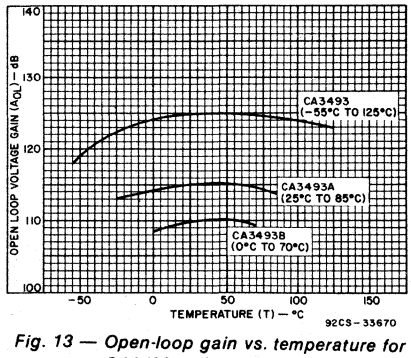


Fig. 13 — Open-loop gain vs. temperature for CA3493 series.

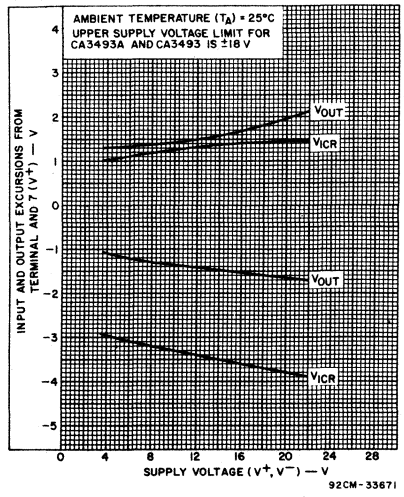


Fig. 15 — Output-voltage-swing capability and common-mode input-voltage vs. supply voltage.

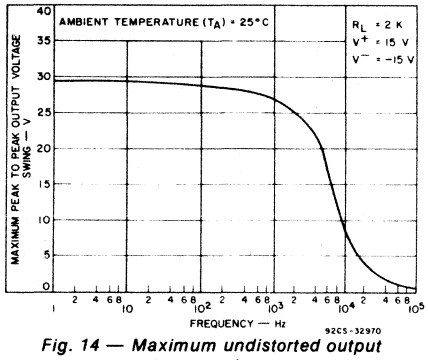


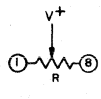
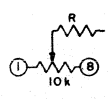
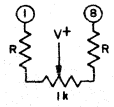
Fig. 14 — Maximum undistorted output voltage vs. frequency.

Offset Voltage Nulling

The input offset voltage can be nulled to zero by any of the three methods shown in the table below. A 10K potentiometer between terminals 1 and 8, with its wiper returned to V^+, will provide a gross nulling for all types. For finer nulling, either of the other two circuits shown below may be used, thus providing simpler improved resolution for all types.

CAUTION: The CA3493 amplifiers will be damaged if they are plugged into op-amp circuits employing nulling with respect to the V^- supply bus.

Offset Voltage Nulling

Offset Nulling Circuits			
Type	**Resistor R Value**	**Resistor R Value**	**Resistor R Value**
CA3493B CA3493A CA3493	10K 10K 10K	100K 50K 20K	20K 10K 5K
	Gross Offset Adjustment	Finer Offset Adjustments	

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Test Circuits

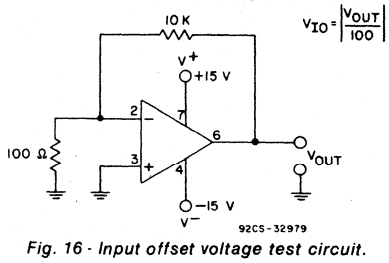
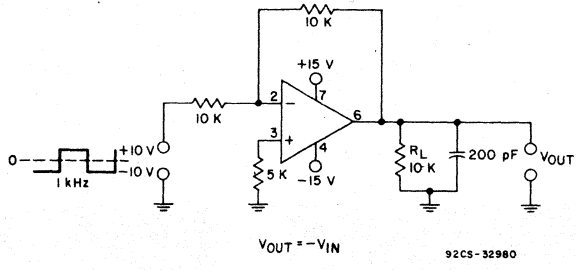
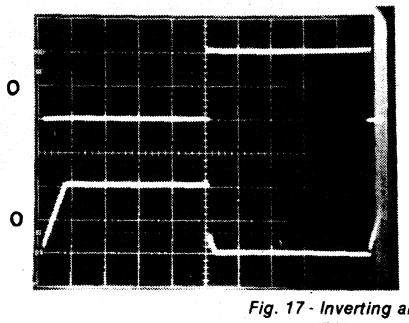


Fig. 16 - Input offset voltage test circuit.



a



TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT. : $\frac{10V}{DIV}$ $V^+ = 15V$ $V^- = -15V$

HOR. : $\frac{.1ms}{DIV}$ $R_L = 10K$

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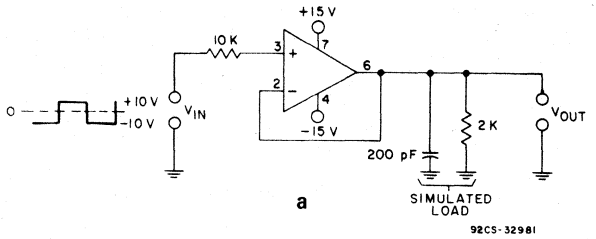
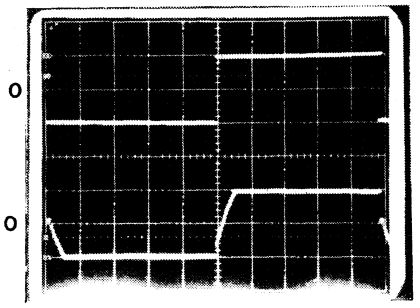
b

Fig. 17 - Inverting amplifier (a) test circuit (b) response to 1-kHz, 20-V p-p square wave.





TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT: $\frac{10\ V}{DIV}$

HOR : $\frac{.1\ ms}{DIV}$

$V^+ = 15\ V$

$V^- = 15\ V$

$R_L = 2K$

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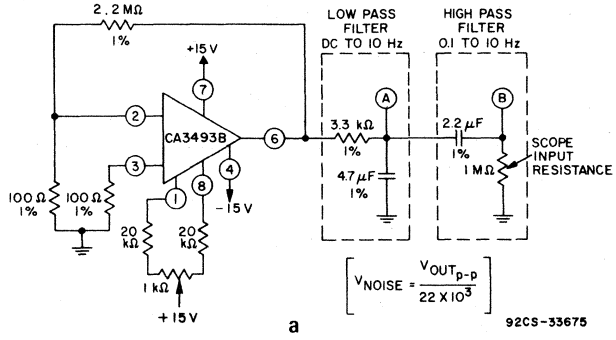
Fig. 18 - Voltage follower (a) test circuit (b) response to 20-V p-p, 1-kHz square-wave input.



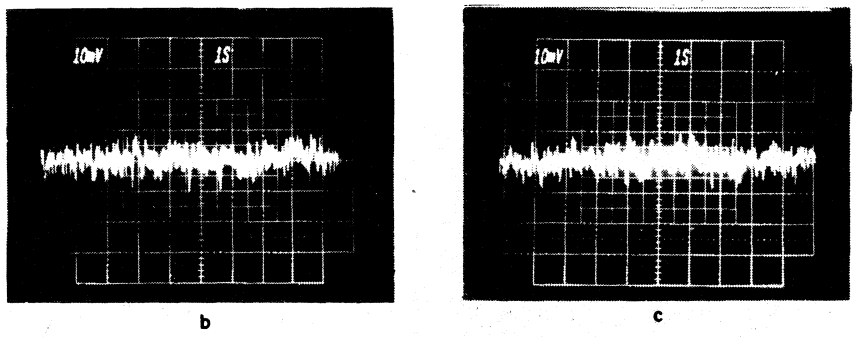
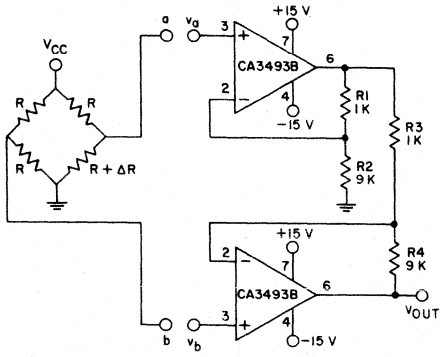


Fig. 19 - Low frequency noise (a) test circuit—0.1 to 10 Hz (b) output A waveform—0 to 10 Hz noise (c) output B waveform—0 to 10 Hz noise.

Application Circuits



$$V_{OUT} = -V_a\left(\frac{R2}{R1}+1\right)\frac{R4}{R3} + V_b\left(\frac{R4}{R3}+1\right)$$

FOR IDEAL RESISTORS WITH $\frac{R1}{R2} = \frac{R3}{R4}$

$$V_{OUT} = V_b - V_a\left(\frac{R4}{R3}+1\right)$$

$$A = \frac{V_{OUT}}{V_b - V_a} = \left(\frac{R4}{R3}+1\right)$$

FOR VALUES ABOVE $V_{OUT} = (V_b - V_a)(10)$

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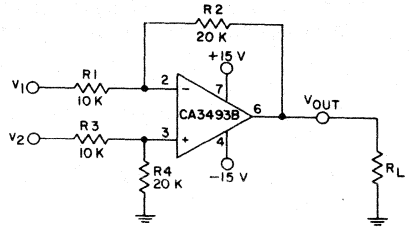
Fig. 20 - Typical two-op amp bridge-type differential amplifier.



$$V_{OUT} = V_2\left(\frac{R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right) - V_1\left(\frac{R2}{R1}\right)$$

IF R4 = R2, R3 = R1 AND $\frac{R2}{R1} = \frac{R4}{R3}$

THEN $V_{OUT} = (V_2 - V_1)\left(\frac{R2}{R1}\right)$

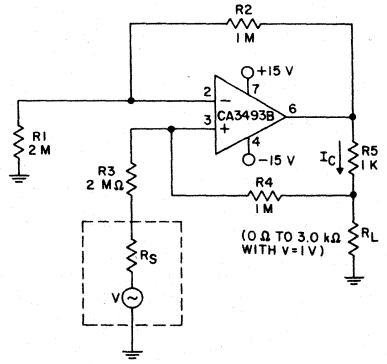
FOR VALUES ABOVE $V_{OUT} = 2(V_2 - V_1)$

IF A_V IS TO BE MADE 1 AND IF R1 = R3 = R4 = R
WITH R2 = 0.999 R (0.1% MISMATCH IN R2)

THEN V_{OCM} = 0.0005 V_{IN} OR CMRR = 66 dB
THUS, THE CMRR OF THIS CIRCUIT IS LIMITED BY THE MATCHING OR MISMATCHING OF THIS NETWORK RATHER THAN THE AMPLIFIER.

92CS-33677

Fig. 21 - Differential amplifier (simple subtractor) using CA3493B.



ALL RESISTORS ARE 1%

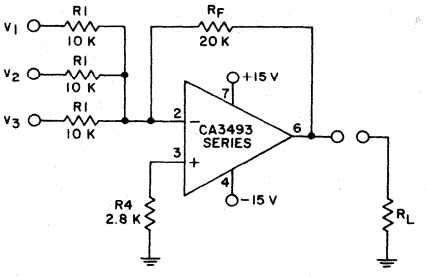
IF R1 = R3 AND R2 ≈ R4 + R5 THEN

I_L IS INDEPENDENT OF VARIATIONS IN R_L
FOR R_L VALUES OF 0 Ω TO 3 kΩ WITH V = 1 V

$$I_L = \frac{V}{R3}\frac{R4}{R5} = \frac{V}{(2\,M)(1K)} = \frac{V}{2\,K} = 500\ \mu A$$

92CS-33678

Fig. 22 - Using CA3493B as a bilateral current source.



$$V_{OUT} = -\left(\frac{R_F}{R1}V_1 + \frac{R_F}{R1}V_2 + \frac{R_F}{R1}V_3\right)$$

$$V_{OUT} = -(2V_1 + 2V_2 + 2V_3)$$

92CS-33679

Fig. 23 - Typical summing amplifier application.

CA3493, CA3493A, CA3493B

The CA3493B is an excellent choice for use with thermocouples. In Fig. 24, the CA3493B amplifies the signal generated 500 times. The three 22-megohm resistors will provide full-scale output if the thermocouple opens.

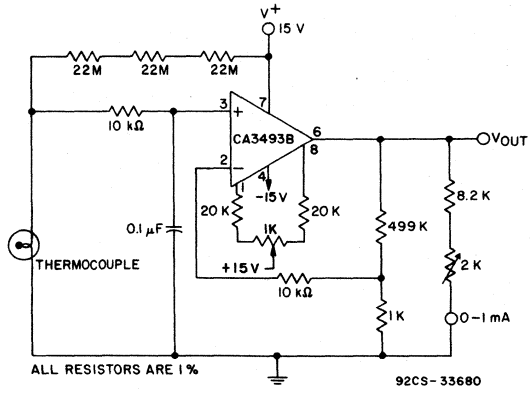
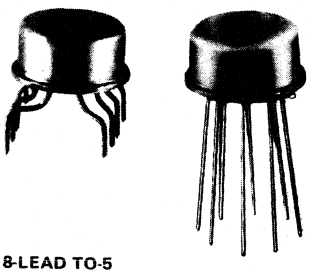


Fig. 24 - The CA3493B used in a thermocouple circuit.



8-LEAD TO-5 with Dual-In-Line Formed Leads H-1787

8-LEAD TO-5 H-1528

Operational Amplifiers

CA6078AT – Micropower Type
CA6741T – General-Purpose Type

For Applications where Low Noise (Burst + 1/f) is a Prime Requirement

Virtually free from "popcorn" (burst) noise: device rejected if any noise burst exceeds 20 μV (peak), referred to input over a 30-second time period.

RCA CA6078AT and CA6741T* are low-noise linear IC operational amplifiers that are virtually free of "popcorn" (burst) noise.

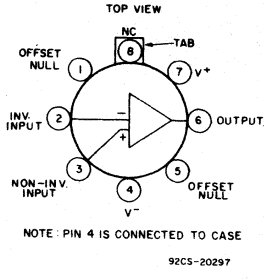
These low-noise versions of the CA3078AT and CA3741T are a result of improved processing developments and rigid burst-noise inspection criteria. A highly selective test circuit (See Fig. 2) assures that each type meets the rigid low-noise standards shown in the data section. This low-burst-noise property also assures excellent performance throughout the 1/f noise spectrum.

In addition the CA6078AT and CA6741T offer the same features incorporated in the CA3078AT and CA3741T respectively, including output short-circuit protection, latch-free operation, wide common-mode and differential-mode signal ranges, and low-offset nulling capability.

For detailed data, characteristics curves, schematic diagram, dimensional outline, and test circuits, refer to the Operational Amplifier Data Bulletins File No. 531 and 535. In addition, for details of considerations in burst-noise measurements, refer to Application Note, ICAN-6732, "Measurement of Burst ("Popcorn") Noise in Linear IC's".

The CA6078AT and CA6741T utilize the hermetically sealed 8-lead TO-5 type package. The CA6078AT and the CA6741T can also be supplied on request with dual-in-line formed leads. These types are identified as the CA6078AS and CA6741S. This formed-lead configuration conforms to that of the 8-lead dual-in-line (Mini–Dip) package. For terminal arrangements, see page 4.

*Formerly Dev. No. TA5807X and TA6029 respectively.



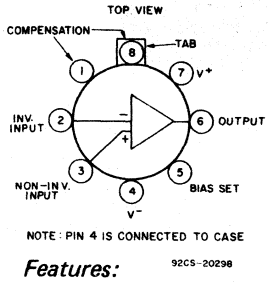
CA6741T

Applications:

- **Low-noise AC amplifier**
- **Narrow-band or band-pass filter**
- **Integrator or differentiator**
- **DC amplifier**
- **Summing amplifier**

Features:

- **Internal phase compensation**
- **Input bias current: 500 nA max.**
- **Input offset current: 200 nA max.**
- **Open-loop voltage gain: 50,000 (94 dB) min.**
- **Input offset voltage: 5 mV max.**



CA6078AT

Applications:

- **Portable electronics**
- **Medical electronics**
- **DC amplifier**
- **Narrow-band or band-pass filter**
- **Integrator or differentiator**
- **Instrumentation**
- **Telemetry**
- **Summing amplifier**

Features:

- **Open-loop voltage gain: 40,000 (92 dB) min.**
- **Input offset voltage:3.5 mV max.**
- **Operates with low total supply voltage: 1.5 V min. (± 0.75 V)**
- **Low quiescent operating current: adjustable for application optimization**
- **Input bias current: adjustable to below 1 nA**

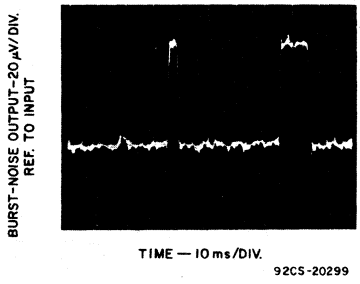
CA6078, CA6741

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

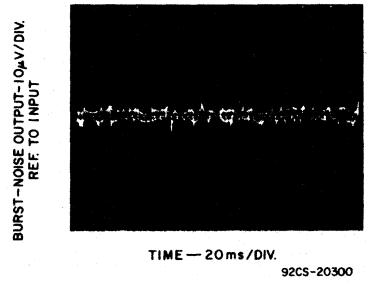
	CA6741T	CA6078AT
DC Supply Voltage (between V^+ and V^- terminals)	44 V	36 V
Differential-Mode Input Voltage	±30 V	±6 V
Common-Mode DC Input Voltage▲	±15 V	V^+ to V^-
Device Dissipation:		
Up to 75°C (CA6741T), Up to 125° (CA6078AT)	500 mW	250 mW
Above 75°C	Derate linearly 5 mW/°C	–
Temperature Range:		
Operating	−55 to +125 °C	−55 to +125 °C
Storage	−65 to +150 °C	−65 to +150 °C
Output Short-Circuit Duration●	No limitation	No limitation
Lead Temperature (During soldering):		
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm)		
from case for 10 seconds max.	300 °C	300 °C

▲If Supply Voltage is less than ±15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

●Short circuit may be applied to ground or to either supply.



a. Typ. device with high-burst-noise characteristic.



b. Typ. device controlled for burst noise.

Fig.1—Typ. waveforms of type with high burst noise and type controlled for burst noise.

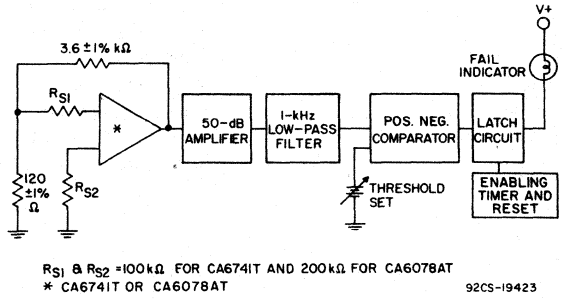


Fig.2—Block diagram of burst-noise "popcorn" test equipment.

ELECTRICAL CHARACTERISTICS – CA6078AT, *For Equipment Design.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Supply Volts: $V^+ = 6$, $V^- = -6$ $T_A = 25^oC$, $I_Q = 20\ \mu A$	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz $R_{S1} = R_{S2} = 200\ k\Omega$	Device is rejected if the total noise voltage (burst + $1/f$), referred to input, exceeds 20 μV peak, during a 30-sec. test period.			
Principal Characteristics (For detailed Electrical Characteristics refer to CA3078AT Data Bulletin, File No. 535.)						
Input Offset Voltage	V_{IO}	$R_S \leq 10\ k\Omega$	–	0.7	3.5	mV
Input Offset Current	I_{IO}		–	0.5	2.5	nA
Input Bias Current	I_{IB}		–	7	12	nA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 10\ k\Omega$	40,000	100,000	–	
		$V_O = \pm 4V$	92	100	–	dB
Common-Mode Input Voltage Range	V_{ICR}	$V^+ = V^- = 15$ V	±14	–	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\Omega$	80	115	–	dB
Output Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10\ \Omega$	±13.7	±14.1	–	V
		$R_L \geq 2\ k\Omega$	–	±14	–	
Supply Current	I_Q		–	20	25	μA

ELECTRICAL CHARACTERISTICS – CA6741T, *For Equipment Design.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Supply Volts; $V^+ = 15$, $V^- = -15$ $T_A = 25^oC$	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz $R_{S1} = R_{S2} = 100\ k\Omega$	Device is rejected if the total noise voltage (burst + $1/f$), referred to input, exceeds 20 μV peak, during a 30-sec. test period.			
Principal Characteristics (For detailed Electrical Characteristics refer to CA3741T Data Bulletin, File No. 531.)						
Input Offset Voltage	V_{IO}	$R_S \leq 10\ k\Omega$	–	1	5	mV
Input Offset Current	I_{IO}		–	20	200	nA
Input Bias Current	I_{IB}		–	80	500	nA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 2\ k\Omega$	50,000	200,000	–	
		$V_O = \pm 10$ V	94	106	–	dB
Common-Mode Input Voltage Range	V_{ICR}		±12	±13	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\Omega$	70	90	–	dB
Output Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10\ k\Omega$	±12	±14	–	V
		$R_L \geq 2\ k\Omega$	±10	±13		
Supply Current	I_Q		–	1.7	2.8	mA

CA6078, CA6741

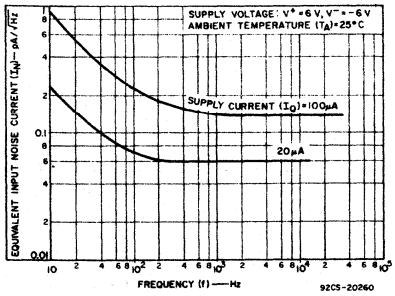


Fig.3—I_N vs. Frequency for CA6078AT.

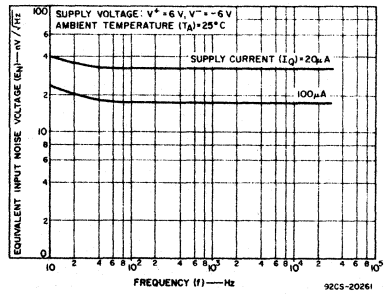


Fig.4—E_N vs. Frequency for CA6078AT.

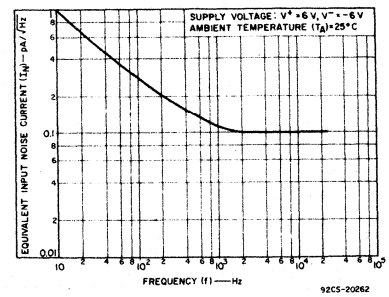


Fig.5—I_N vs. Frequency for CA6741T.

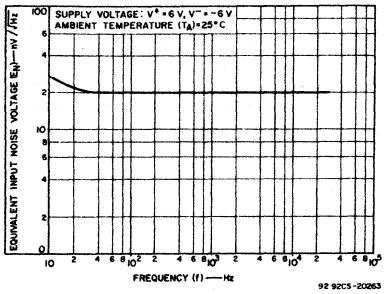


Fig.6—E_N vs. Frequency for CA6741T.

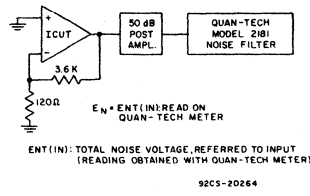


Fig.7—Test block diagram for E_N.

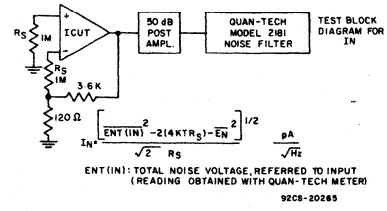
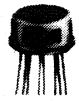
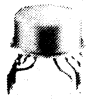


Fig.8—Test block diagram for I_N.


(E Suffix)
8-LEAD
(MINI-DIP)
H-1517


(T Suffix)
8-LEAD
TO-5 H-1528


(E Suffix)
14-LEAD DIP
H-1817


(S Suffix)
8-LEAD
TO-5
(DIL-CAN)
H-1787

BiMOS Operational Amplifiers

With MOS/FET Input, Composite Bipolar/MOS Output

Single Amplifier: CA080, CA081
Dual Amplifier: CA082, CA083
Quad Amplifier: CA084

Features:

- *Very low input bias and offset currents*
- *Input impedance typically 1.5 x 10^{12} Ω*
- *Low input offset voltage*
- *Wide common-mode input voltage range*
- *Low power consumption*
- *Fast slew rate*
- *Unity-gain bandwidth = 5 MHz (typ.)*
- *Wide output voltage swing*
- *Low distortion*
- *Continuous short circuit protection*
- *Direct replacement for industry type TL080 series in most applications*

The RCA-CA080, CA081, CA082, CA083, and CA084 BiMOS operational amplifiers combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOS/FET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range. The bipolar and MOS output transistors allow a wide output voltage swing and provide a high output current capability.

Package Selection Chart

Type No.	Package Type & Suffix			
	8L TO-5	DIL-CAN	Mini-DIP	14L DIP
CA080	T	S	E	
CA080A	T	S	E	
CA080B			E	
CA080C	T	S		
CA081	T	S	E	
CA081A	T	S	E	
CA081B			E	
CA081C	T	S		
CA082	T	S	E	
CA082A	T	S	E	
CA082B			E	
CA082C	T	S		
CA083				E
CA083A				E
CA083B				E
CA084				E
CA084A				E
CA084B				E

Applications:

- *Inverters*
- *High-Q notch filters*
- *IC preamplifiers*
- *Unity Gain Absolute Value Amplifiers*
- *Sample and hold amplifiers*
- *Active filters*

The CA080 is externally phase-compensated, and the CA081, CA082, CA083, and CA084 are internally phase-compensated. All types except the CA082 have provisions for external offset nulling.

The CA080, CA081, CA082, CA083, and CA084 are available in chip form (H Suffix).

Operating Temperature Ranges:

-55 to +125° C	0 to +70° C
CA080T, CA080S	CA080CT, CA080CS
CA080AT, CA080AS	CA080BE
CA081T, CA081S	CA081CT, CA081CS
CA081AT, CA081AS	CA081BE
CA082T, CA082S	CA082CT, CA082CS
CA082AT, CA082AS	CA082BE
	CA083BE, CA083AE
	CA083BE
	CA084, CA084AE
	CA084BE

CA080, CA081, CA082, CA083, CA084 Series

MAXIMUM RATINGS, *Absolute Maximum Values:*

DC SUPPLY VOLTAGE V± ..... ±18 V
DIFFERENTIAL INPUT VOLTAGE ..... ±16 V
INPUT VOLTAGE RANGE ..... ± 15 V
INPUT CURRENT ..... 1 mA
OUTPUT SHORT-CIRCUIT DURATION ..... UNLIMITED*
POWER DISSIPATION, PD:
At TA = 25°C:
E Suffix ..... 625 mW
T Suffix ..... 680 mW
Derating Factors:
Mini-DIP ..... Derate linearly at 6.67 mW/°C above 56°C
14-Lead DIP ..... Derate linearly at 6.67 mW/°C above 56°C
TO-5 ..... Derate linearly at 6.67 mW/°C above 56°C
AMBIENT TEMPERATURE RANGE:
CT, CS, E, Suffixes ..... 0 to +70°C
T, S, Suffixes ..... -55 to +125°C
STORAGE TEMPERATURE RANGE, ALL TYPES ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

* The output may be shorted to ground or either supply if the maximum temperature and dissipation ratings are observed.

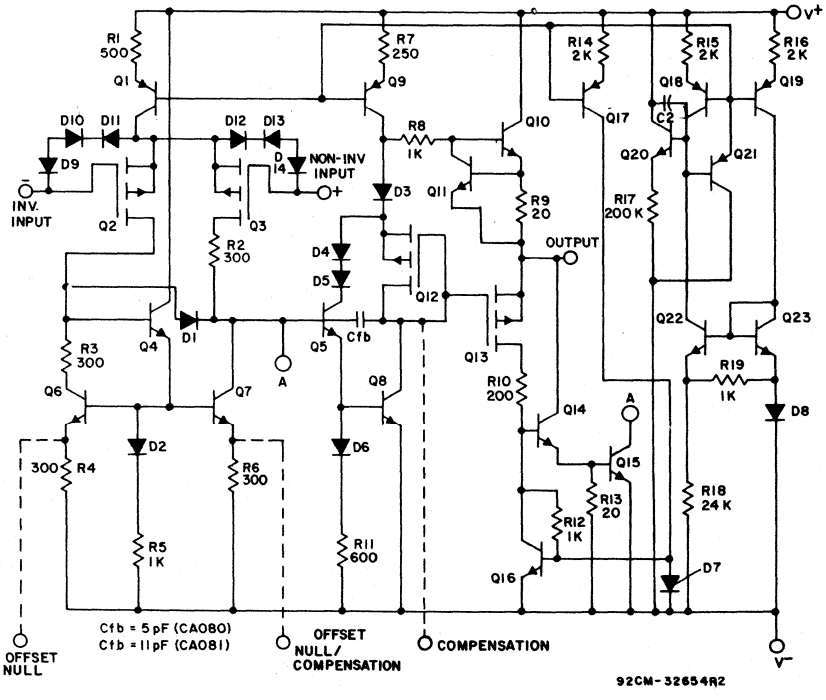
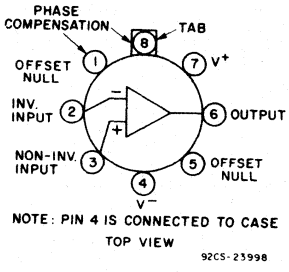


Fig. 1 - Schematic diagram of the CA080, CA081, CA082, CA083, and CA084.

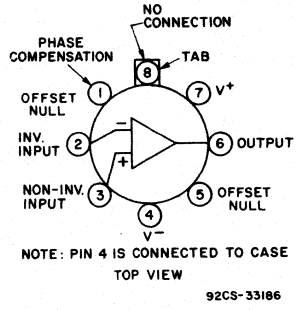
CA080, CA081, CA082, CA083, CA084 Series

Texas Instruments-to-RCA Package Suffix Cross Reference Chart

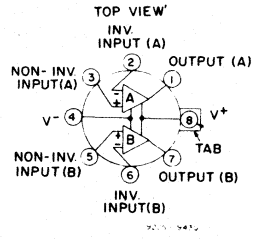
Texas Instruments		RCA	
Suffix	**Description**	**Suffix**	**Description**
ACJG	Ceramic DIL	AS	DILCAN TO-5
ACL	TO-5	AT	TO-5
ACN	Plastic DIL	AE	Plastic DIL
ACP	Plastic DIL	AE	Plastic DIL
CJG	Ceramic DIL	CS	DILCAN TO-5
CL	TO-5	CT	TO-5
CN	Plastic DIL	E	Plastic DIL
CP	Plastic DIL	E	Plastic DIL
IJG	Ceramic DIL	S	DILCAN TO-5
IL	TO-5	T	TO-5
IP	Plastic DIL	E	DILCAN TO-5
MJG	Ceramic DIL	S	DILCAN TO-5
ML	TO-5	T	TO-5
AML	TO-5	AT	TO-5
BCP	Plastic DIL	BE	Plastic DIL



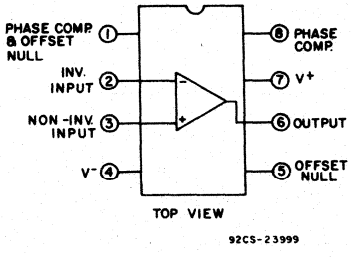
CA080
T, S Suffixes



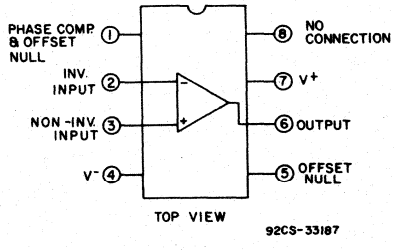
CA081
T, S Suffixes



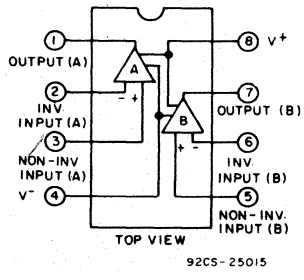
CA082
T, S Suffixes



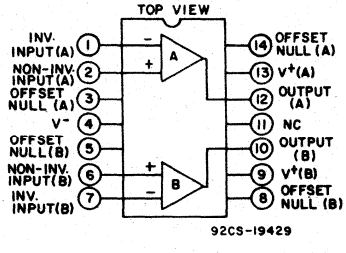
CA080
E Suffix



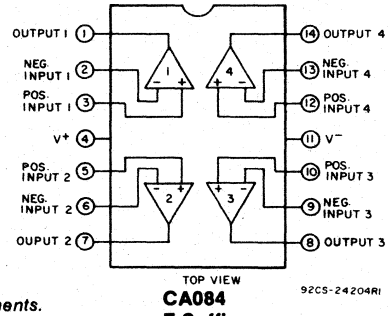
CA081
E Suffix



CA082
E Suffix



CA083
E Suffix



CA084
E Suffix

Fig. 2 - Terminal assignments.

CA080, CA081, CA082, CA083, CA084 Series

TYPICAL OPERATING CHARACTERISTICS at $V\pm = 15$ V, $T_A = 25°C$

CHARACTERISTIC	TEST CONDITIONS	VALUE	UNITS
Slew Rate at Unity Gain, SR	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, A_{VD} = 1	13	V/μs
Rise Time, t_r	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, A_{VD} = 1	0.1	μs
Overshoot Factor		10	%
Equivalent Input Noise Voltage, e_n	R_S = 100 Ω, f = 1 kHz	40	nV/√Hz

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ and $T_A = -55$ to $+125°C$ for types supplied in TO-5 style packages (T, S Suffixes). $V^+ = \pm 15$ V

This does not include CA080C, CA081C, or CA082C. These types are supplied in TO-5 packages, but they are specified over the range of 0 to 70°C, and their limits are the same as those for the CA080, CA081, CA082, and CA083 in plastic packages over the range 0 to 70°C.

CHARACTERISTIC	TEST CONDITIONS	−55 to +125°C	+25°C	LIMITS: CA080T, S CA081T, S CA082T, S Min.	Typ.	Max.	LIMITS: CA080AT, S CA081AT, S CA082AT, S Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	R_S = 50Ω	X		—	3	6	—	2	3	mV
			X	—	—	9	—	—	5	
Temperature Coefficient of Input Offset Voltage, $\propto V_{IO}$	R_S = 50 Ω		X	—	10	—	—	10	—	μV/°C
Input Offset Current, I_{IO}		X		—	5	20	—	5	20	pA
			X	—	—	4	—	—	2	nA
Input Current		X		—	15	40	—	15	40	pA
			X	—	—	10	—	—	5	nA
Common-Mode Input Voltage Range, V_{ICR}		X		±12	—	—	±12	—	—	V
Maximum Output Voltage Swing, V_{OP-P}	R_L = 10 kΩ	X		24	27	—	24	27	—	V
	$R_L \geq 10$ kΩ		X	24	—	—	24	—	—	
	$R_L \geq 2$ kΩ		X	20	24	—	20	24	—	
Large-Signal Differential Voltage Gain, A_{VD}	$R_L \geq 2$ kΩ, $V_O = \pm 10$V	X		50	200	—	50	200	—	V/mV
			X	25	—	—	25	—	—	
Unity-Gain Bandwidth		X		—	5	—	—	5	—	MHz
Input Resistance, R_I		X		—	1.5	—	—	1.5	—	TΩ
Common-Mode Rejection Ratio, CMRR	$R_S \leq 10$ kΩ	X		80	86	—	80	86	—	dB
Power Supply Rejection Ratio, PSRR ($\Delta V^+ / \pm \Delta V_{IO}$)	$R_S \leq 10$ kΩ	X		80	86	—	80	86	—	dB
Supply Current, I^+ (per amp., CA082, CA083)	No load, No Signal	X		—	1.4	2.8	—	1.4	2.8	mA
Channel Separation, V_{O1}/V_{O2} (between amps., CA082, CA083)	A_{VD} = 100	X		—	120	—	—	120	—	dB

ELECTRICAL CHARACTERISTICS at T_A = 25°C, T_A = 0 to +70°C for types supplied in plastic dual-in-line packages (E Suffix). V^+ = ±15 V

CHARACTERISTIC	TEST CONDITIONS	0 to 70°C	+25°C	LIMITS CA080BE CA081BE CA082BE CA083BE CA084BE Min.	Typ.	Max.	LIMITS CA080AE CA081AE CA082AE CA083AE CA084AE Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	R_S = 50Ω	X		—	2	3	—	3	6	mV
			X	—	—	5	—	—	7.5	
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 50 Ω		X	—	10	—	—	10	—	μV/°C
Input Offset Current, I_{IO}		X		—	5	10	—	5	20	pA
			X	—	—	0.4	—	—	0.6	nA
Input Current		X		—	15	30	—	15	40	pA
			X	—	—	0.7	—	—	1	nA
Common-Mode Input Voltage Range, V_{ICR}		X		±12	—	—	±12	—	—	V
Maximum Output Voltage Swing, V_{OP-P}	R_L = 10 kΩ	X		24	27	—	24	27	—	V
	R_L ≥ 10 kΩ		X	24	—	—	24	—	—	
	R_L ≥ 2 kΩ		X	20	24	—	20	24	—	
Large-Signal Differential Voltage Gain, A_{VD}	R_L ≥ 2 kΩ,	X		50	200	—	50	200	—	V/mV
	V_O = ±10V		X	—	—	—	—	—	—	
Unity-Gain Bandwidth		X		—	5	—	—	5	—	MHz
Input Resistance, R_I		X		—	1.5	—	—	1.5	—	TΩ
Common-Mode Rejection Ratio, CMRR	R_S ≤ 10 kΩ	X		80	86	—	80	86	—	dB
Power Supply Rejection Ratio, PSRR ($\Delta V^+/\pm\Delta V_{IO}$)	R_S ≤ 10 kΩ	X		80	86	—	80	86	—	dB
Supply Current, I^+ (per amp., CA082, CA083, CA084)	No load, No Signal	X		—	1.4	2.8	—	1.4	2.8	mA
Channel Separation, V_{O1}/V_{O2} (between amps.,CA082, CA083)	A_{VD} = 100	X		—	120	—	—	120	—	dB

CA080, CA081, CA082, CA083, CA084 Series

ELECTRICAL CHARACTERISTICS at T_A = 25°C, T_A = 0 to 70°C for types supplied in plastic dual-in-line packages (E Suffix). V^+ = ±15 V

The limits for the CA080C, CA081C, and CA082C in TO-5 packages are the same as those for the types in this chart.

CHARACTERISTIC	TEST CONDITIONS	0 to 70°C	+25°C	LIMITS CA080E, T CA081E, T CA082E, T CA083E CA084E Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	R_S = 50Ω	X		—	5	15	mV
			X	—	—	20	
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 50 Ω		X	—	10	—	μV/°C
Input Offset Current, I_{IO}		X		—	5	30	pA
			X	—	—	1	nA
Input Current		X		—	15	50	pA
			X	—	—	2	nA
Common-Mode Input Voltage Range, V_{ICR}		X		±10	—	—	V
Maximum Output Voltage Swing, V_{OP-P}	R_L = 10 kΩ	X		24	27	—	V
	$R_L \geq$ 10 kΩ		X	24	—	—	
	$R_L \geq$ 2 kΩ		X	20	24	—	
Large-Signal Differential Voltage Gain, A_{VD}	$R_L \geq$ 2 kΩ, V_O = ±10V	X		25	200	—	V/mV
			X	—	—	—	
Unity-Gain Bandwidth		X		—	5	—	MHz
Input Resistance, R_I		X		—	1.5	—	TΩ
Common-Mode Rejection Ratio, CMRR	$R_S \leq$ 10 kΩ	X		70	76	—	dB
Power Supply Rejection Ratio, PSRR ($\Delta V^+ / \pm \Delta V_{IO}$)	$R_S \leq$ 10 kΩ	X		70	76	—	dB
Supply Current, I^+ (per amp., CA082, CA083)	No load, No Signal	X		—	1.4	2.8	mA
Channel Separation, V_{O1}/V_{O2} (between amps., CA082, CA083)	A_{VD} = 100	X		—	120	—	dB

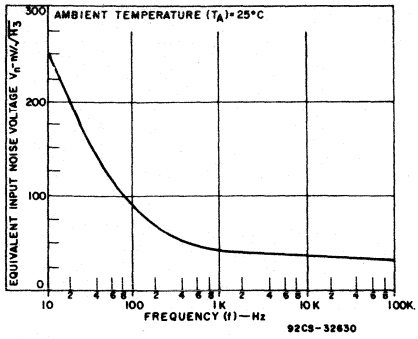


Fig. 3 - Noise voltage as a function of frequency.

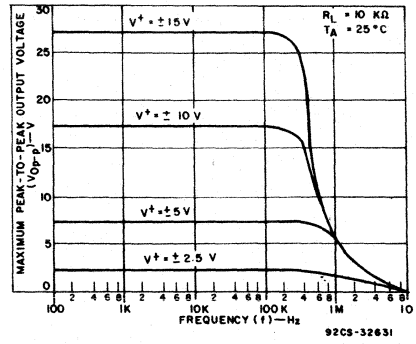


Fig. 4 - Output voltage as a function of frequency.

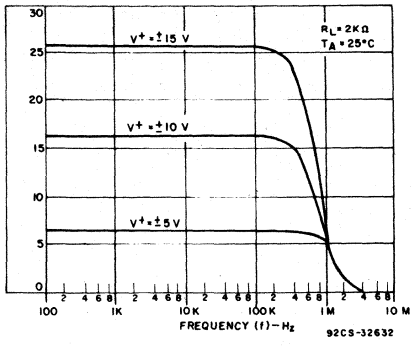


Fig. 5 - Output voltage as a function of frequency.

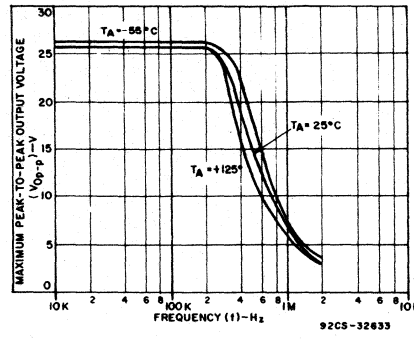


Fig. 6 - Output voltage as a function of frequency.

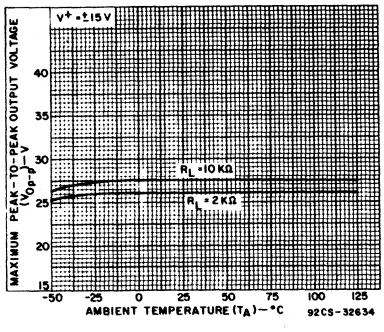


Fig. 7 - Output voltage as a function of ambient temperature.

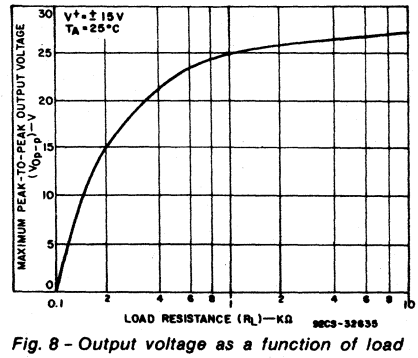


Fig. 8 - Output voltage as a function of load resistance.

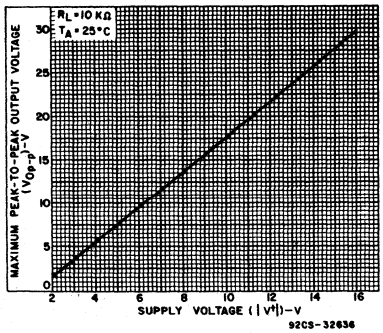


Fig. 9 - Output voltage as a function of supply voltage.

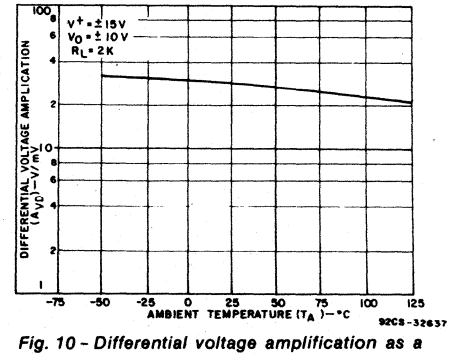


Fig. 10 - Differential voltage amplification as a function of ambient temperature.

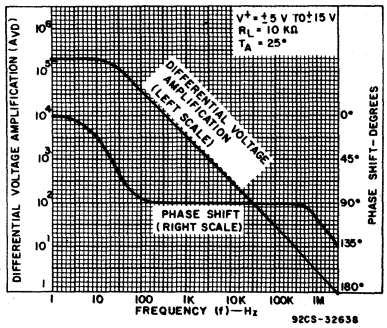


Fig. 11 - Differential voltage amplification as a function of frequency.

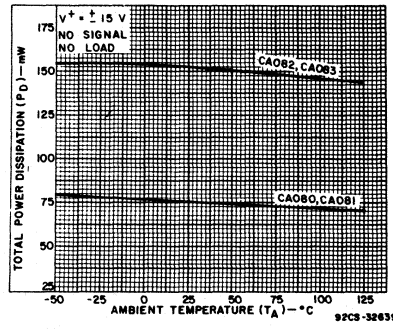


Fig. 12 - Total power dissipation as a function of ambient temperature.

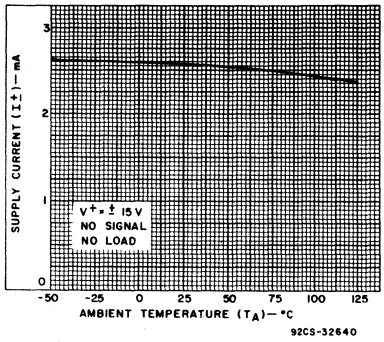


Fig. 13 - Supply current as a function of ambient temperature.

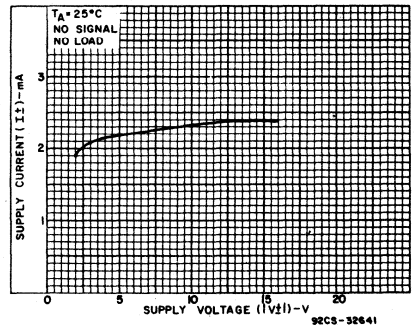


Fig. 14 - Supply current as a function of supply voltage.

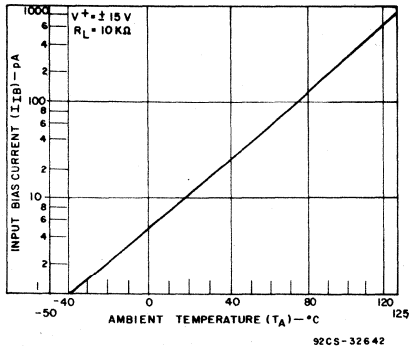


Fig. 15 - Input bias current as a function of ambient temperature.

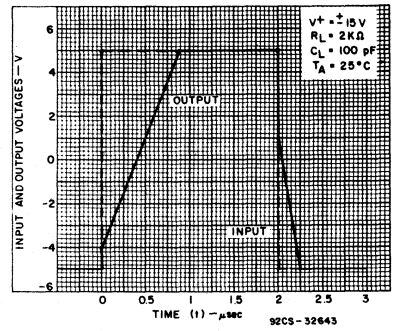


Fig. 16 - Voltage follower large-signal pulse response.

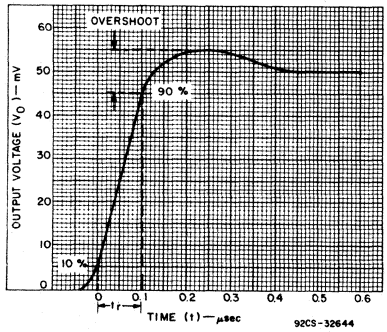


Fig. 17 - Output voltage as a function of elapsed time.

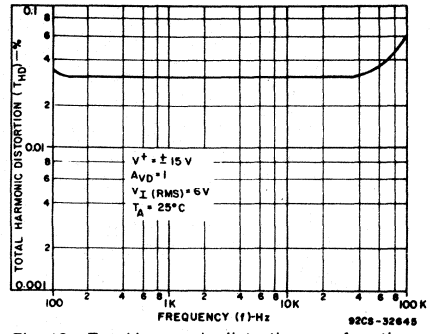


Fig. 18 - Total harmonic distortion as a function of frequency.

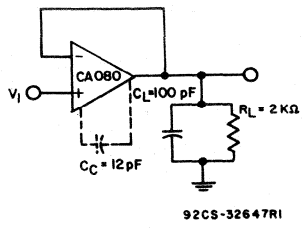


Fig. 19 - Unity-gain amplifier.

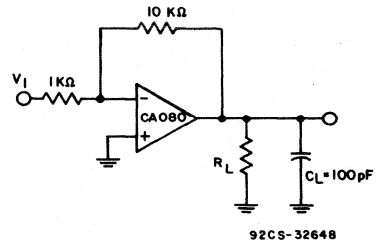


Fig. 20 - 10X inverting amplifier.

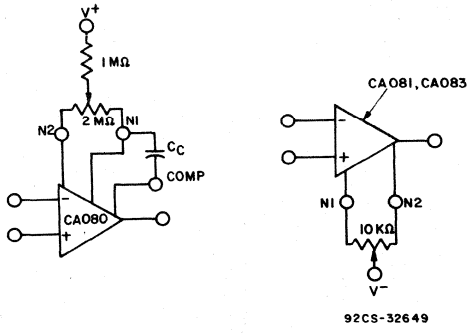


Fig. 21 - Input-offset voltage null circuits.

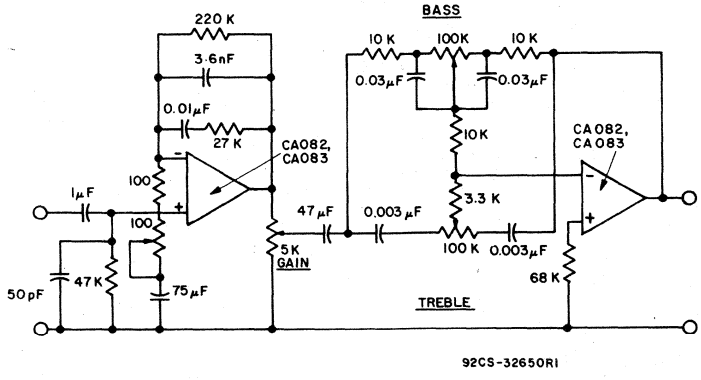


Fig. 22 - IC preamplifier.

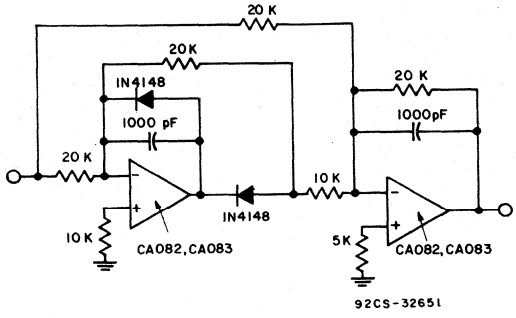


Fig. 23 - Unity-gain absolute-value amplifier.

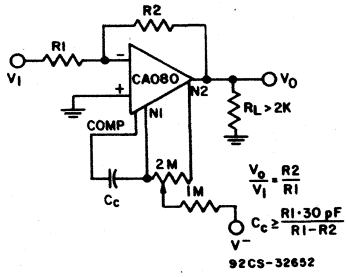


Fig. 24 - Inverting amplifier with single-pole compensation and offset adjustment.

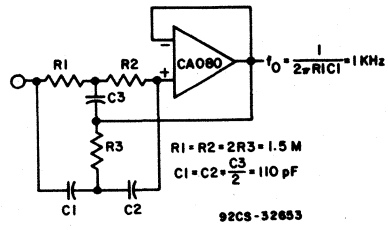


Fig. 25 - High Q notch filter.

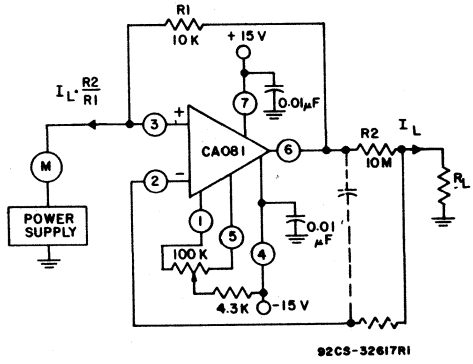


Fig. 26 - Basic current amplifier for low-current measurement systems.

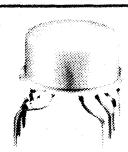
CURRENT AMPLIFIER

The low input-terminal current needed to drive the CA081 makes it ideal for use in current-amplifier applications such as the one shown in Fig.26. In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R2/R1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100 nA, with values shown, the load current presented to the supply will be 100 μA; a much easier current to measure in many systems.

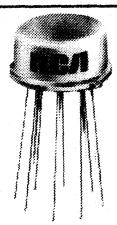
Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output-load capacitance and the potential oscillation in this situation. Essentially, the necessary high-frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types



S-Suffix Types
(DIL-CAN)
H-1787



T-Suffix Types
(TO-5 Style)
H-1528

E-Suffix Types
(Mini-DIP)
H-1817

Dual Operational Amplifiers

For Commerical, Industrial, and Military Applications

Features:

- *Internal frequency compensation for unity gain*
- *High dc voltage gain - 100 dB typ.*
- *Wide bandwidth at unity gain - 1 MHz typ.*
- *Wide power supply range:*
  Single supply 3 to 30 V
  Dual supplies ± 1.5 to ± 15 V
- *Low supply current - 1.5 mA typ.*
- *Low input bias current*
- *Low input offset voltage and current*
- *Input common-mode voltage range includes ground*
- *Differental input voltage range equal to V+ range*
- *Large output voltage swing - 0 to V+ -1.5 V*

The RCA-CA158, CA158A, CA258, CA258A, CA358, CA358A and CA2904 types consist of two independent, high gain, internally frequency compensated operational amplifiers which are designed specifically to operate from a single power supply over a wide range of voltages. They may also be operated from split power supplies. The supply current is basically independent of the supply voltage over the recommended voltage range.

These devices are particularly useful in interface circuits with digital systems and can be operated from the single common 5 Vdc power supply. They are also intended for transducer amplifiers, dc gain blocks and many other conventional op amp circuits which can benefit from the single power supply capability.

The CA158, CA158A, CA258, CA258A, CA358, CA358A, and CA2904 types are supplied in 8-lead dual-in-line plastic packages (MINI-DIP, E suffix), 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads (DIL-CAN, S suffix). The CA358 is also supplied in chip form (H suffix).

The CA158, CA158A, CA258, CA258A, CA358, CA358A, and CA2904 types are an equivalent to or a replacement for the industry types 158, 158A, 258, 258A, 358, 358A, and CA2904.

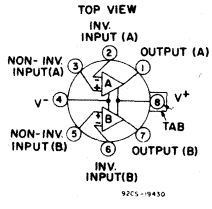


Fig. 1 - Functional diagram for CA158, CA258, and CA358 S- and T-suffix types.

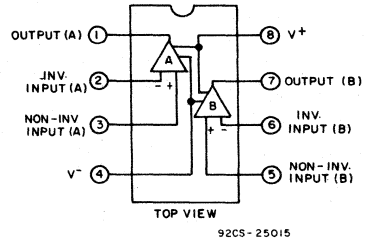


Fig. 2 - Functional diagram for CA158, CA258, CA358, and CA2904 E-suffix types.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

SUPPLY VOLTAGE, V^+:	
CA2904	26 V or ± 13 V
Other Types	32 V or ± 16 V
DIFFERENTIAL INPUT VOLTAGE:	
All Types	± 32 V
INPUT VOLTAGE	−0.3 V to V^+ V
INPUT CURRENT ($V_I < -0.3$ V) +	50 mA
OUTPUT SHORT CIRCUIT TO GROUND ($V^+ \leq 15$ V)*	Continuous
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	630 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to + 125°C
Storage	−65 to + 150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+ 300 °C

+ This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V dc.

* The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

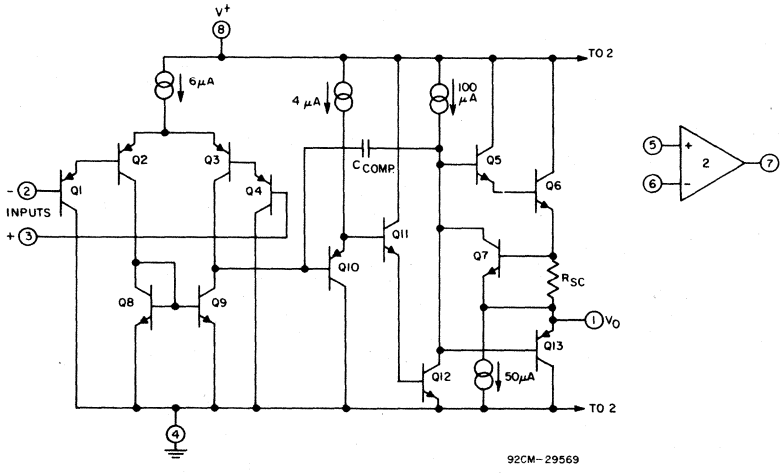


Fig.3 – Schematic diagram – one of two operational amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply For Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA158A (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
T_A = 25°C					
Input Offset Voltage, V_{IO}	Note 3	–	1	2	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	2	10	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	20	50	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
T_A = –55 to +125°C					
Input Offset Voltage, V_{IO}	Note 3	–	–	4	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	15	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	30	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	200	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	100	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA258A (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
T_A = 25°C					
Input Offset Voltage, V_{IO}	Note 3	–	1	3	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	2	15	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	40	80	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
T_A = –25 to +85°C					
Input Offset Voltage, V_{IO}	Note 3	–	–	4	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_s = 0	–	7	15	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	30	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	200	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	100	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA358A (E. T. S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	3	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	100	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	25	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	65	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = 0 to +70°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	5	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	20	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	75	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	300	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	200	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of thedevice. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA158 (E, T, S) CA258 (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
T_A = 25°C					
Input Offset Voltage, V_{IO}	Note 3	–	2	5	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	3	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	150	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
T_A = –55 to + 125°C (CA158); T_A = –25 to +85°C (CA258)					
Input Offset Voltage, V_{IO}	Note 3	–	–	7	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	100	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	300	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA358 (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	25	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	65	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = 0 to +70°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	9	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	150	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	500	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ \geq$ 15 V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA2904E			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
T_A = 25°C					
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	R_L = 10 kΩ .	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	—	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	50	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	50	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
T_A = -40 to +85°C					
Input Offset Voltage, V_{IO}	Note 3	–	–	10	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	45	200	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	500	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of thedevice. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

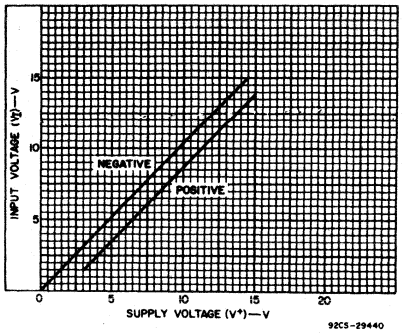


Fig.4 – Input voltage range as a function of supply voltage.

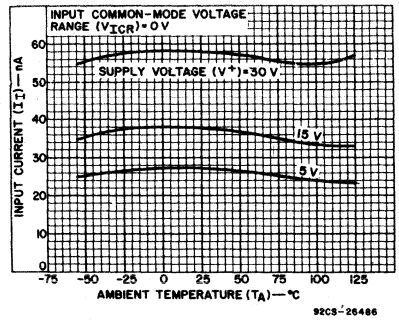


Fig.5 – Input current as a function of ambient temperature.

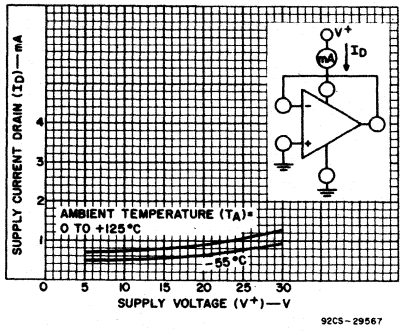


Fig.6 – Supply current drain as a function of supply voltage.

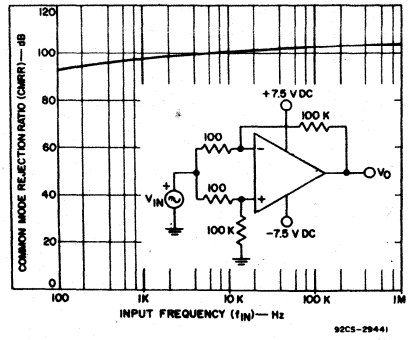


Fig.7 – Common mode rejection ratio as a function of input frequency.

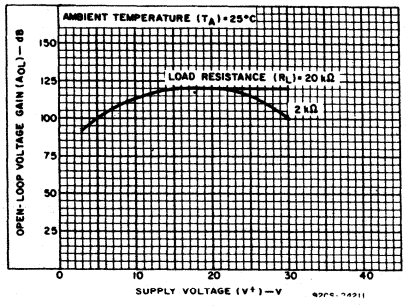


Fig.8 – Voltage gain as a function of supply voltage.

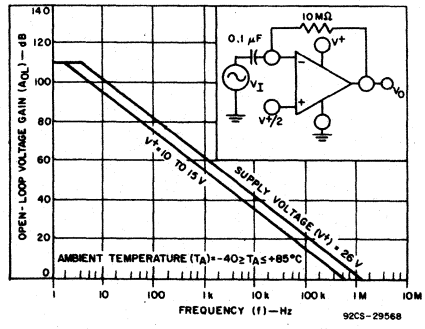


Fig.9 – Open-loop frequency response.

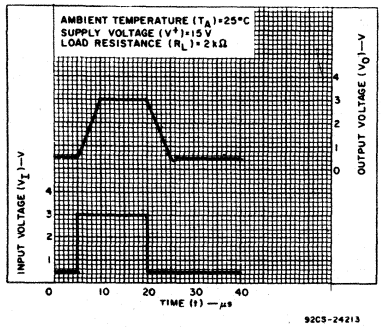


Fig.10 – Voltage follower pulse response.

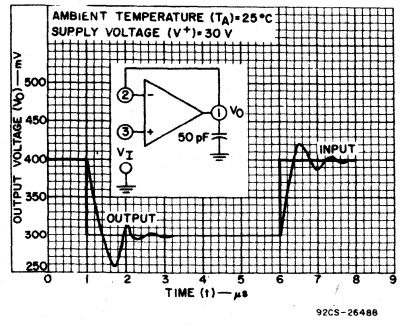


Fig.11 – Voltage follower pulse response (small signal).

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

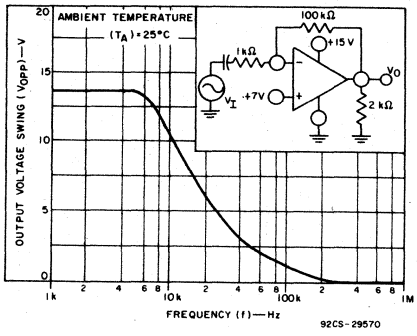


Fig.12 – Large-signal frequency response.

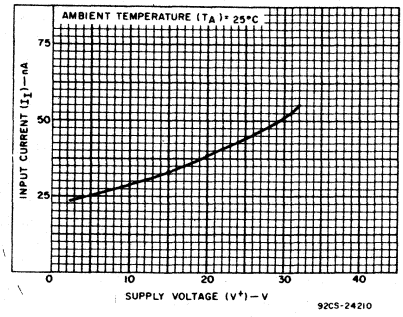


Fig.13 – Input current as a function of supply voltage.

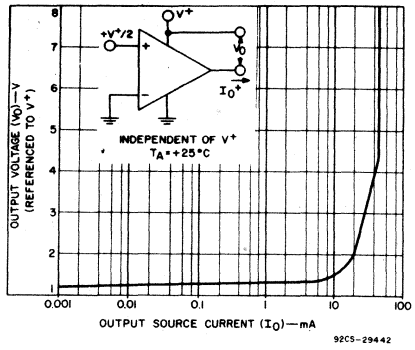


Fig.14 – Output source current characteristics.

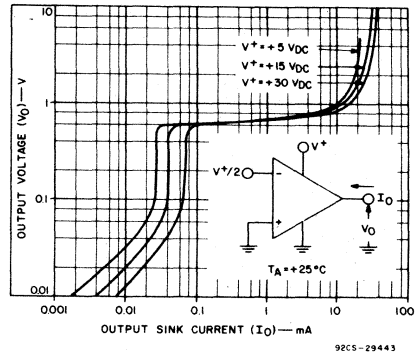


Fig.15 – Output sink current characteristics.

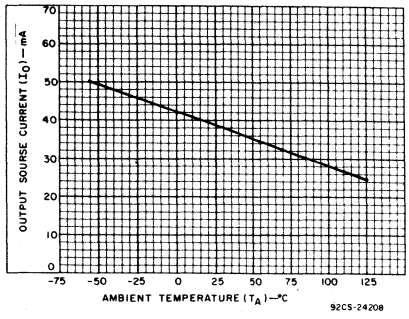


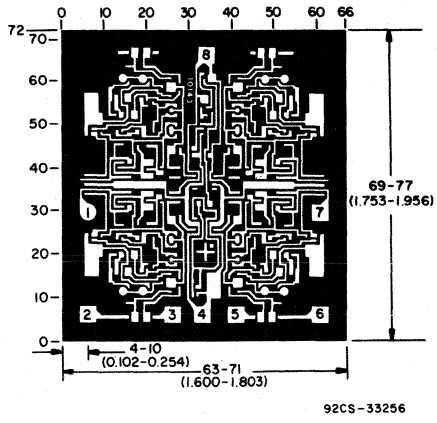
Fig.16 – Output current as a function of ambient temperature.

ORDERING INFORMATION

These packages are identified by Suffix Letters indicated in the chart shown below. When ordering these devices, it is important that the appropriate suffix letter be affixed to the type number of the device required.

PACKAGE	SUFFIX LETTERS	TYPES
8-Lead Dual-In-Line Plastic with	E	CA158, A CA258, A CA358, A CA2904
8-Lead TO-5 Style with Standard Leads	T	CA158, A CA258, A CA358, A
8-Lead TO-5 Style with Dual-In-Line Formed Leads	S	

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

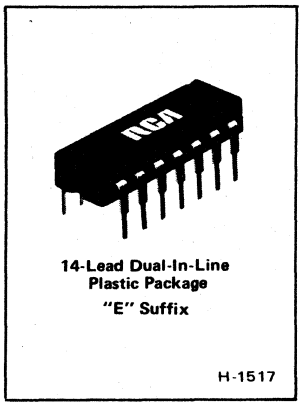


Dimensions and pad layout for CA358H..

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA124, CA224, CA324 Types



14-Lead Dual-In-Line Plastic Package "E" Suffix

H-1517

Quad Operational Amplifiers

For Commercial, Industrial, and Military Applications

Features:

- Operation from single or dual supplies
- Unity-gain bandwidth . . . . . 1 MHz (typ.)
- DC voltage gain . . . . . 100 dB (typ.)
- Input bias current . . . . . 45 nA (typ.)
- Input offset voltage . . . . . 2 mV (typ.)
- Input offset current . . . . . 5 nA (typ.) for CA224, CA324
  . . . . . 3 nA (typ.) for CA124
- Replacement for industry types 124, 224, 324

The RCA-CA124, -CA224, and -CA324 consist of four independent, high-gain operational amplifiers on a single monolithic substrate. An on-chip capacitor in each of the amplifiers provides frequency compensation for unity gain. These devices are designed specifically to operate from either single or dual supplies, and the differential voltage range is equal to the power-supply voltage. Low power drain and an input common-mode voltage range of from 0 V to $V^+ - 1.5$ V (single-supply operation) make the CA124, CA224, and CA324 suitable for battery operation.

Applications

- Summing amplifiers
- Multivibrators
- Oscillators
- Transducer amplifiers
- DC gain blocks

The CA124, CA224, and CA324 are supplied in a 14-lead dual-in-line plastic package (E suffix). The CA324 is also available in chip form (H suffix).

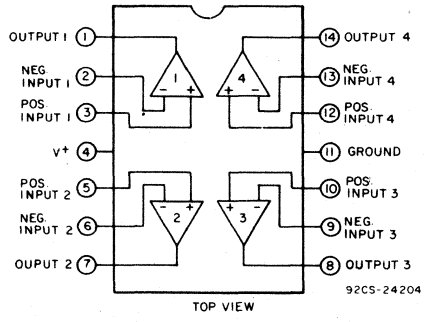


Fig. 1 – Functional diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

SUPPLY VOLTAGE	32 V or ±16 V
DIFFERENTIAL INPUT VOLTAGE	±32 V
INPUT VOLTAGE	−0.3 V to +32 V
INPUT CURRENT ($V_I < -0.3$ V)†	50 mA
OUTPUT SHORT CIRCUIT TO GROUND ($V^+ \leq 15$ V)*	Continuous
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

*The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device.

†This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V dc.

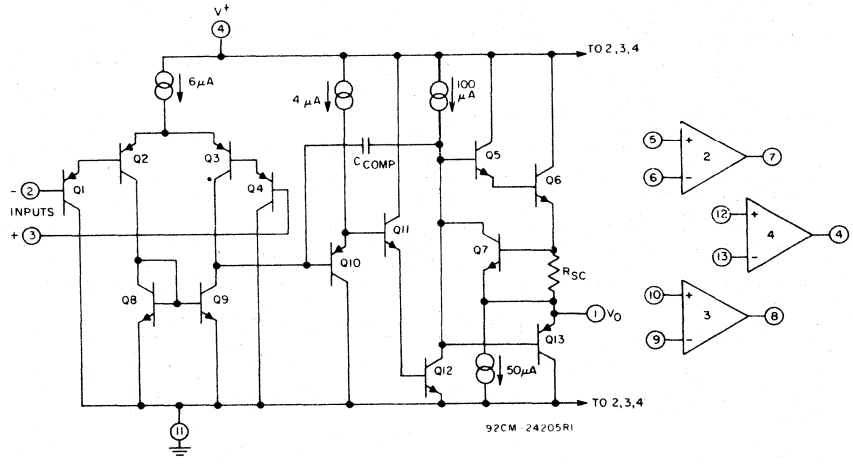


Fig. 2—Schematic diagram—one of four operational amplifiers.

CA124, CA224, CA324 Types

ELECTRICAL CHARACTERISTICS (Values Apply For Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	CA124 LIMITS			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	5	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+–1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+=30 V	0	–	V^+–1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	3	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	150	nA
Output Current (Source), I_O	V_I^+=+1 V, V_I^-=0 V, V^+=15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+=0 V, V_I^-=1 V, V^+=15 V	10	20	–	mA
	V_I^+=0 V, V_I^-=1 V, V_O=200 mV	12	50	–	μA
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	94	100	–	dB
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f=1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = –55 to +125°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	7	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	100	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	–	300	nA
Supply Current, I^+	$R_L = \infty$ On All Ampl.	–	0.8	2	mA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V	0	–	V^+–2	V
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	88	–	–	dB
Output Voltage Swing: High-Level, V_{OH}	R_L=2 kΩ, V^+=30 V	26	–	–	V
	R_L=10 kΩ	27	28	–	
Low-Level, V_{OL}	R_L=10 kΩ	–	5	20	mV
Output Current: Source, I_O	V_I^+=1 V_{DC}, V_I^-=0, V^+=15 V	10	20	–	mA
Sink, I_O	V_I^-=1 V_{DC}, V_I^+=0, V^+=15 V	5	8	–	mA
Differential Input Voltage	Note 2	–	–	V^+	V

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go to +32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

ELECTRICAL CHARACTERISTICS (Values apply for each operational amplifier)

CHARACTERISTIC	TEST CONDITIONS	CA224, CA324 LIMITS			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+–1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+= 30 V	0	–	V^+–1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	V_I^+=+1 V, V_I^-=0 V, V^+=15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+=0 V, V_I^-=1 V, V^+=15 V	10	20	–	mA
	V_I^+=0 V, V_I^-=1 V, V_O=200 mV	12	50	–	μA
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	88	100	–	dB
Common-Mode Rejection Ratio, CMRR	DC	65	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = –40 to +85°C (CA224), T_A = 0 to 70°C (CA324)				
Input Offset Voltage, V_{IO}	Note 3	–	–	9	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_s = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	150	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	–	500	nA
Supply Current, I^+	R_L =∞ On All Ampl.	–	0.8	2	mA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V	0	–	V^+–2	V
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	83	–	–	dB
Output Voltage Swing: High-Level, V_{OH}	R_L = 2 kΩ, V^+ = 30 V	26	–	–	V
	R_L = 10 kΩ	27	28	–	
Low-Level, V_{OL}	R_L = 10 kΩ	–	5	20	mV
Output Current: Source, I_O	V_I^+=1 V_{DC}, V_I^-=0, V^+=15 V	10	20	–	mA
Sink, I_O	V_I^-=1 V_{DC}, V_I^+=0, V^+=15 V	5	8	–	mA
Differential Input Voltage	Note 2	–	–	V^+	V

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go to +32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

CA124, CA224, CA324 Types

TYPICAL CHARACTERISTICS CURVES

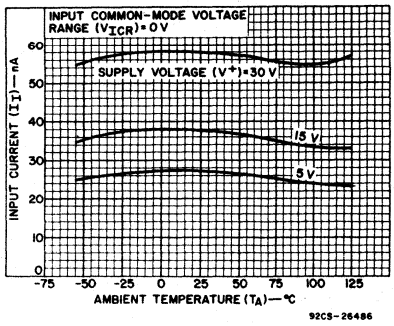


Fig. 3—Input current vs. ambient temperature.

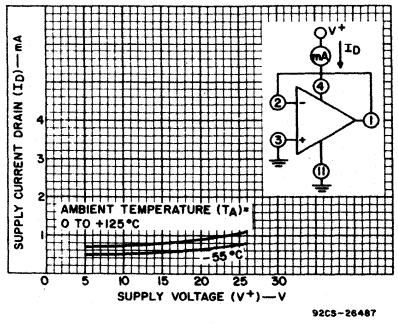


Fig. 4—Supply current drain vs. supply voltage.

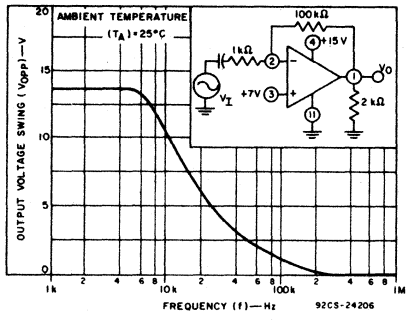


Fig. 5—Large-signal frequency response.

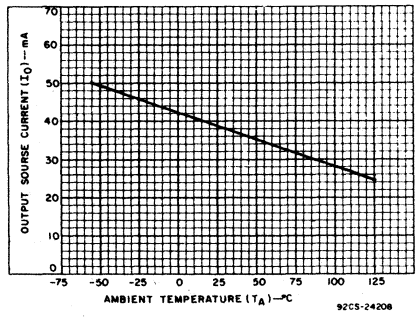


Fig. 6—Output current vs. ambient temperature.

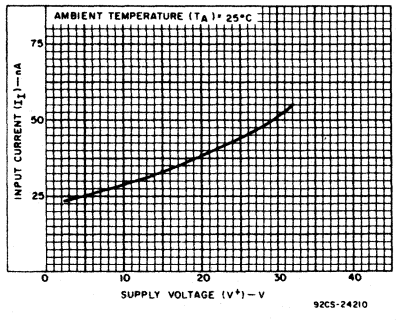


Fig. 7—Input current vs. supply voltage.

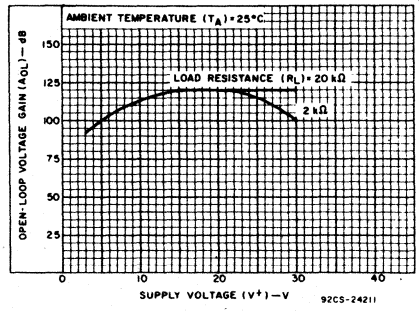


Fig. 8—Voltage gain vs. supply voltage.

TYPICAL CHARACTERISTICS CURVES (CONT'D)

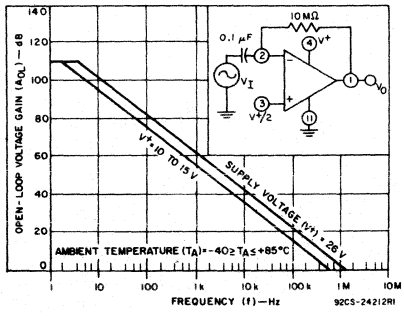


Fig. 9—Open-loop frequency response.

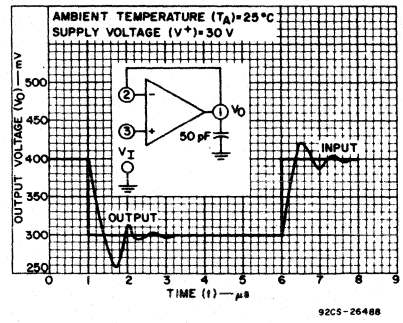


Fig. 10—Voltage follower pulse response (small signal).

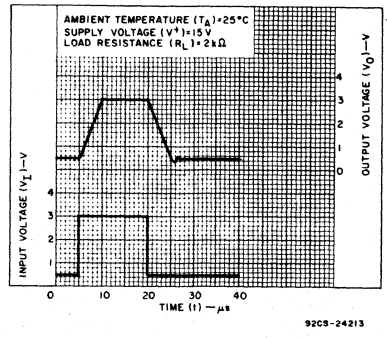
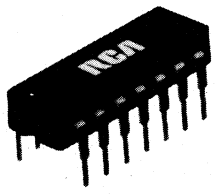


Fig. 11—Voltage follower pulse response.

CA3401E



14-Lead Dual-In-Line
Plastic Package
(E-Suffix Type)

H-1517

Quad Single-Supply Operational Amplifier

For Automotive Electronics and Industrial Control Systems

"E" Suffix Types — Standard Dual-In-Line Plastic Package

Features:
- *Single-supply operation - +5 V to +18 Vdc*
- *Internally compensated*
- *Wide unity-gain bandwidth - 5 MHz typ.*
- *Low input bias current - 50 nA typ.*
- *High open-loop gain - 2000 V/V typ.*

Applications:
- *Automotive*
- *Constant-Current Sources*
- *Multivibrators*
- *Sample and Hold*
- *Square-Wave Generator*
- *Oscillators*
- *Tachometers*
- *Active Filters*
- *Multi-Channel Amplifiers*
- *Summing Amplifiers*

The RCA-3401 is a high-gain monolithic quad operational amplifier designed specifically for applications using a single positive power supply. No external compensation is necessary. Closed-loop stability in each of the four independent amplifiers is maintained by a 3-pF on-chip capacitor. The CA3401 is ideally suited for applications in industrial control systems, automotive electronics, and general purpose amplifiers, e.g. oscillators, tachometers, active filters, and multichannel amplifiers.

The CA3401 is supplied in a 14-lead dual-in-line plastic package (E suffix), and is also available in chip form (H suffix). It is a direct replacement for the Motorola MC3401P, and is pin-compatible with the Motorola MC3301P and the National Semi-conductor LM3900N. The CA3401 can be operated over the temperature range of -55 to +125°C, although the limit values of certain specified electrical characteristics apply only over the range of 0 to +75°C.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DC SUPPLY VOLTAGE	+18 V
INPUT SIGNAL CURRENT	5 mA
DEVICE DISSIPATION:	
Up to T_A = 25°C	625 mW
Above T_A = 25°C	Derate lineary 5 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	-55 to + 125°C
Storage	-65 to + 150°C
LEAD TEMPERATURE (During soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	300°C

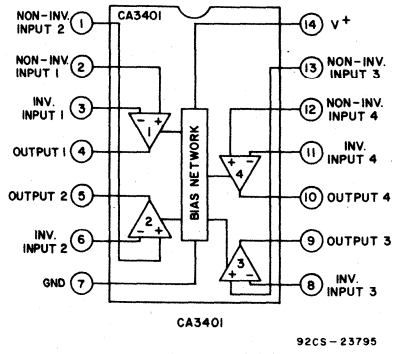


Fig. 1 - Block diagram of CA3401.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V^+ = 15 V (Unless Indicated Otherwise)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
STATIC					
Output Voltage:					
High, V_{OH}		13.5	14.2	–	V
Low, V_{OL}		–	0.03	0.1	
Max. Undistorted Output Swing, V_{OP-P}	0°C<T_A<75°C	10	13.5	–	
Output Current:					
Source, I_{SOURCE}		5	10	–	mA
Sink, I_{SINK}		0.5	1	–	
Total Quiescent Current: I_Q					
Noninverting inputs open		–	6.9	10	mA
Noninverting inputs grounded		–	7.8	14	
Input Bias Current, I_{IB}	R_L = ∞ T_A = 25°C	–	50	300	nA
	R_L = ∞ 0°C ≤T_A≤75°C	–	–	500	
DYNAMIC					
Open-Loop Voltage Gain, A_{OL}	T_A = 25°C	1000	2000	–	V/V
	0°C≤T_A≤75°C	800	–	–	
Input Resistance, R_I		0.1	1	–	MΩ
Slew Rate, SR	C_L = 100 pF, R_L = 5 kΩ	–	0.6	–	V/μs
Unity Gain Gandwidth, BW		–	5	–	MHz
Phase Margin, ϕ		–	70	–	Degrees
Power Supply Rejection	f = 100 Hz	–	55	–	dB
Channel Separation, e_{01}/e_{02}	f = 1 kHz	–	65	–	dB

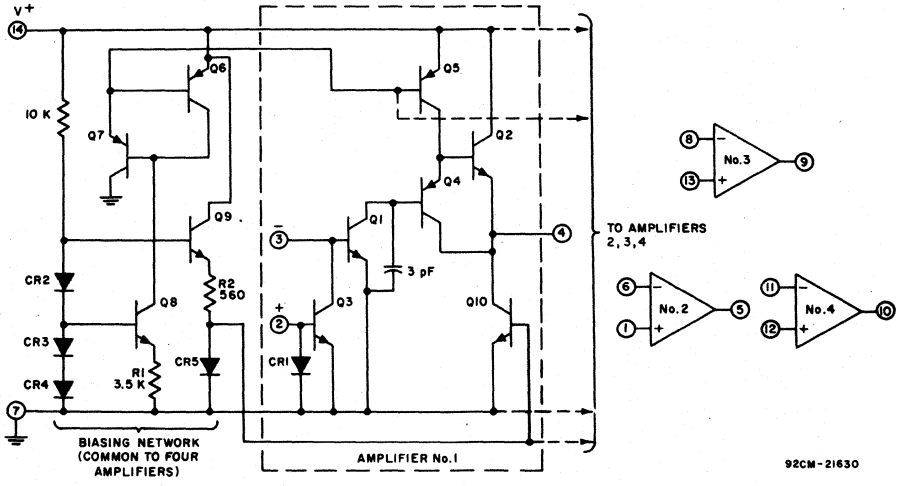


Fig.2 – Schematic diagram of CA3401.

CA3401E

TEST CIRCUITS

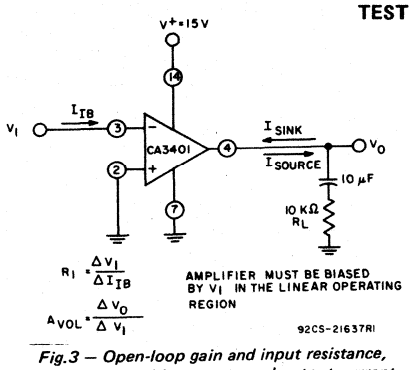


Fig.3 – Open-loop gain and input resistance, input bias current and output current test circuit.

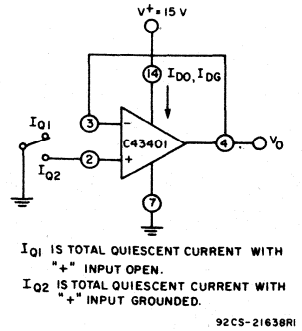


Fig.4 – Quiescent power supply current test circuit.

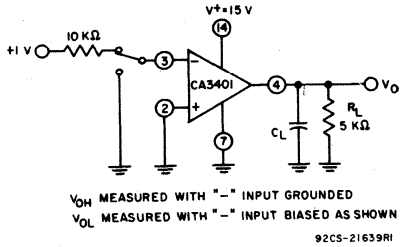


Fig.5 – Output voltage swing test circuit.

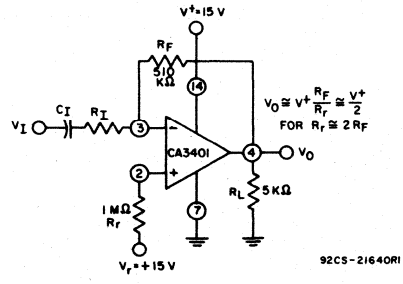


Fig.6 – Peak-to-peak output voltage test circuit.

TYPICAL CHARACTERISTIC CURVES

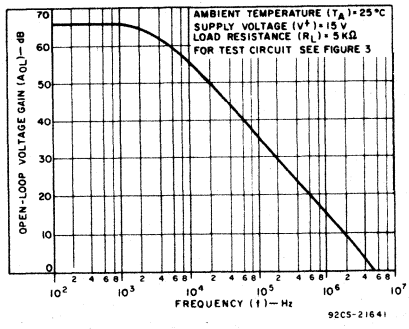


Fig.7 – Open-loop voltage gain vs. frequency.

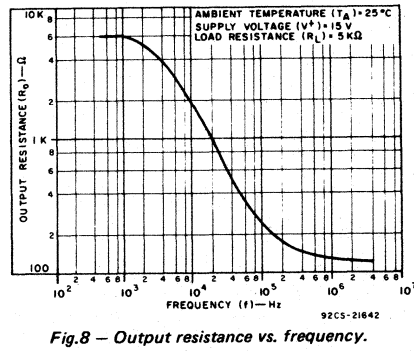


Fig.8 – Output resistance vs. frequency.

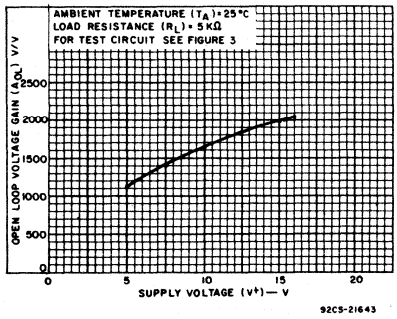


Fig.9 – Open-loop voltage gain vs. supply voltage.

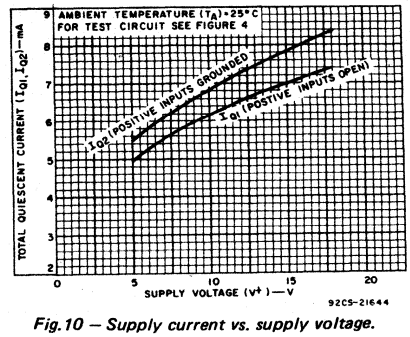


Fig.10 – Supply current vs. supply voltage.

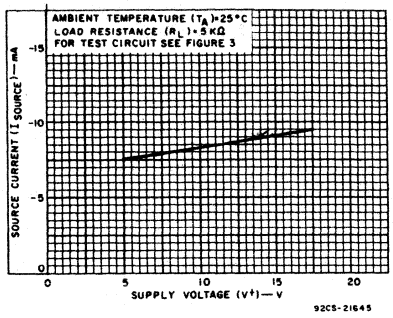


Fig. 11 – Source current vs. supply voltage.

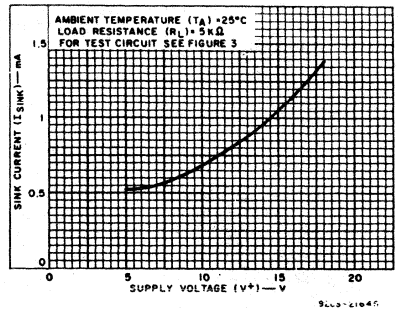
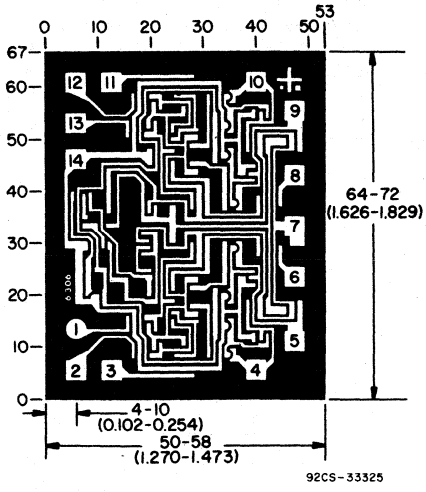


Fig. 12 – Sink current vs. supply voltage.

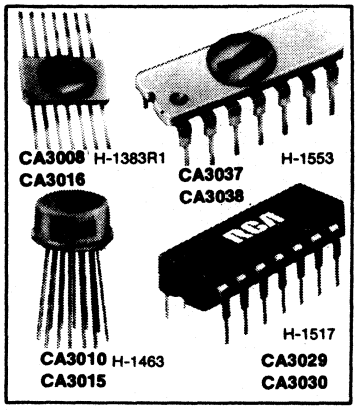


Dimensions and pad layout for CA3401H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038



Operational Amplifiers

Features:

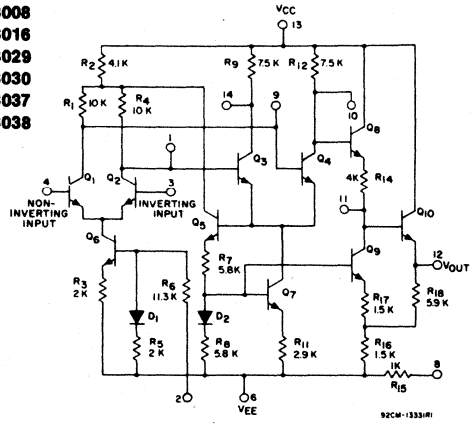
- *All types are electrically identical within their voltage groups*
- *For use in telemetry, data-processing, instrumentation, and communication equipment*
- *Built-in temperature stability from −55°C to +125°C for flat pack, TO-5 style, and ceramic dual-in-line packages; 0°C to +70°C for plastic dual-in-line packages*

6-Volt Types	12-Volt Types	Package
CA3008	CA3016	14-Lead Flat Pack
CA3010	CA3015	12-Lead TO-5 Style
CA3029	CA3030	14-Lead Plastic Dual-In-Line (TO-116)
CA3037	CA3038	14-Lead Ceramic Dual-In-Line (TO-116)

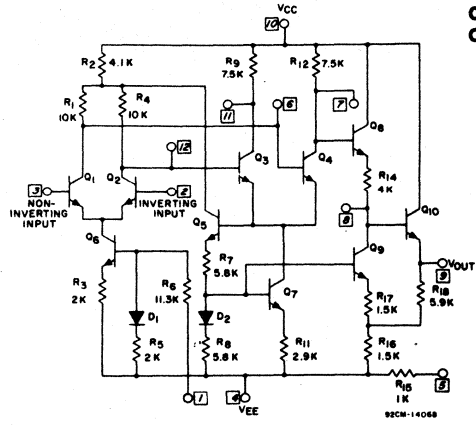
Applications:

- *Narrow-band and band-pass amplifier*
- *Operational functions*
- *Feedback amplifier*
- *DC and video amplifier*
- *Multivibrator*
- *Oscillator*
- *Comparator*
- *Servo driver*
- *Scaling adder*
- *Balanced modulator-driver*

CA3008
CA3016
CA3029
CA3030
CA3037
CA3038



CA3010
CA3015



Schematic diagrams.

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010	CA3008 CA3029 CA3037	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010	CA3008 CA3029 CA3037	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 (CA3008, CA3029, CA3037) 4 & 9 (CA3010)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.6, CA3008, CA3029, CA3037 No.4, CA3010 (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015	CA3016 CA3030 CA3038	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015	CA3016 CA3030 CA3038	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 (CA3016, CA3030, CA3038) 4 & 9 (CA3015)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.6, CA3016, CA3030, CA3038 No.4, CA3015 (Substrate) DO NOT GROUND				

	CA3008 CA3016 CA3037 CA3010 CA3015 CA3038	CA3029 CA3030
OPERATING TEMPERATURE RANGE	-55°C to +125°C	0°C to +70°C
STORAGE TEMPERATURE RANGE	-65°C to +200°C	-25°C to +85°C

	CA3016 CA3030 CA3015 CA3038	CA3008 CA3029 CA3010 CA3037
MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V	-4 V to +1 V
MAXIMUM DEVICE DISSIPATION	600 mW	300 mW

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 (CA3008, CA3016, CA3029, CA3030, CA3037, CA3038) Terminal No.5 (CA3010, CA3015) Not Connected Unless Otherwise Specified	Test Circuit	CA3008 CA3010 CA3029 CA3037			CA3016 CA3015 CA3030 CA3038			Units	Typical Characteristic Curves
			Fig.	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	1.08 -	5 -	- -	- 1.37	- 5	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.54 -	5 -	- -	- 1.07	- 5	μA	2
Input Bias Current	I_I	= +6V = -6V = +12V = -12V	5	- -	5.3 -	12 -	- -	- 9.6	- 24	μA	3
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_T	= +6 V = -6 V = +12V = -12V	4	- -	30 -	- -	- -	- 175	- -	mW	none
		[5] shorted to [9] V_{CC} = +6V, V_{EE} = -6V		-	102	-	-	-	-		
		8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	500	-		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Common-Mode Rejection Ratio	CMR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	4 -	6.75 -	- -	- 12	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	10 -	14 -	- -	- 5	- 7.8	- -	kΩ	13
Output Impedance	Z_{OUT}	= +6V = -6V = +12V = -12V	15	- -	200 -	- -	- -	- 92	- -	Ω	16
Common-Mode Input-Voltage Range	V_{CMR}	= +6V = -6V = +12V = -12V	11	- -	+0.5 -4 -	- -	- -	- +0.65 -8	- -	V	none

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038; Italic Numbers in Square Boxes are for CA3010, CA3015

INPUT OFFSET VOLTAGE AND CURRENT

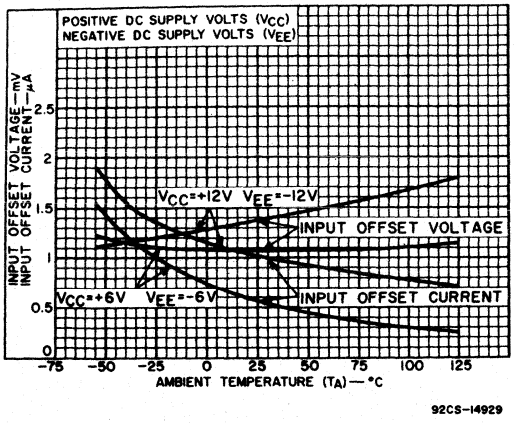


Fig.2

INPUT BIAS CURRENT

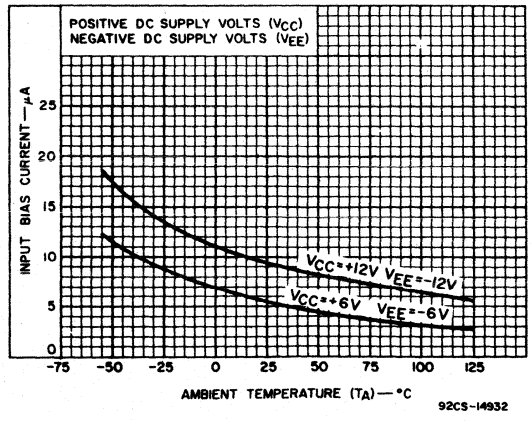


Fig.3

INPUT OFFSET VOLTAGE, INPUT OFFSET VOLTAGE SENSITIVITY, AND DEVICE DISSIPATION TEST CIRCUIT

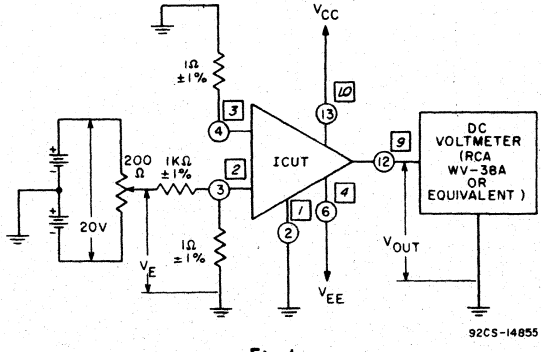


Fig.4

INPUT OFFSET CURRENT AND INPUT BIAS CURRENT TEST CIRCUIT

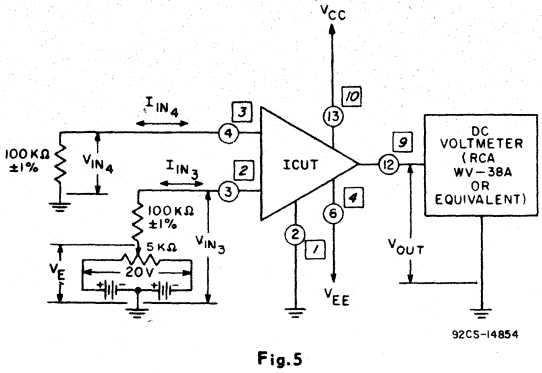


Fig.5

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the diference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\ (\text{Step 2}) - V_{OUT}\ (\text{Step 3})}{2\ \text{volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$

I_C = Direct Current into Terminal (13) or [10]

I_E = Direct Current out of Terminal (6) or [4]

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN_4}.
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN_4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038; Italic Numbers in Square Boxes are for CA3010, CA3015

OPEN-LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3008, CA3010, CA3015, CA3016, CA3037, CA3038

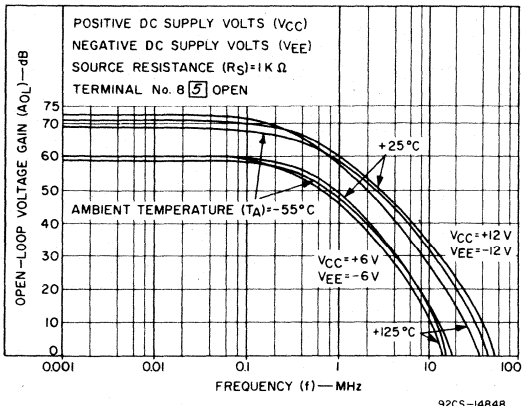


Fig.6

OPEN-LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3029 AND CA3030

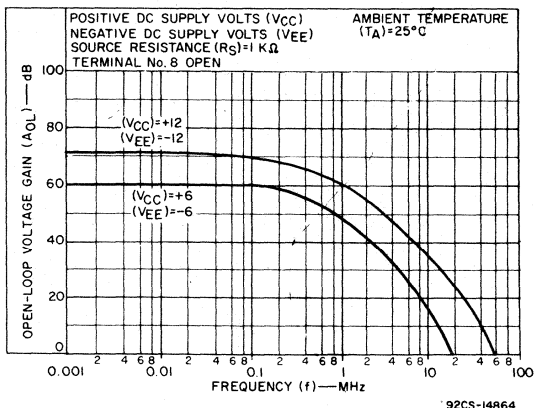
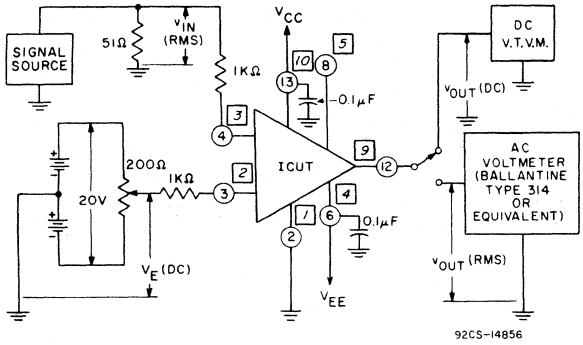


Fig.7

OPEN-LOOP DIFFERENTIAL VOLTAGE GAIN, MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE, AND OPEN-LOOP BANDWIDTH AT -3 dB POINT TEST CIRCUIT



Procedure:

1. Adjust V_E for V_{OUT} = ±0.1 V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at f = 1 kHz.

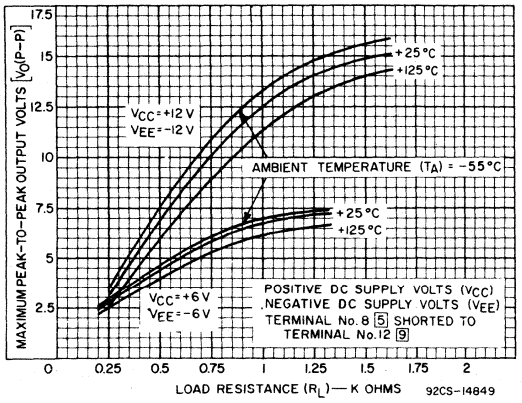
$$A_{OL} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

3. Measure Maximum Peak-to-Peak Output Voltage at f = 1 kHz.
4. Measure Open-Loop Bandwidth at -3 dB Point.

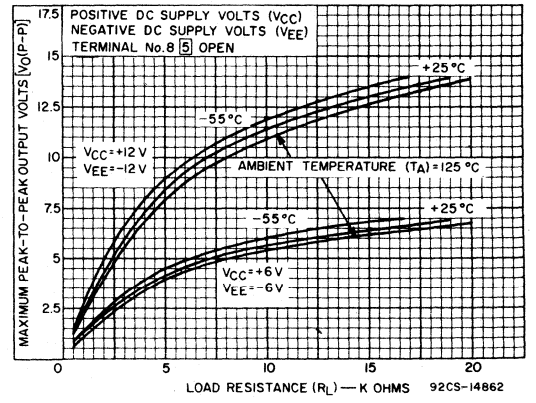
Reference Level = A_{OL} at 1 kHz.

Fig.8

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3008, CA3010, CA3015, CA3016, CA3037, CA3038



(a)



(b)

Fig.9

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038; Italic Numbers in Square Boxes are for CA3010, CA3015

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3029 AND CA3030

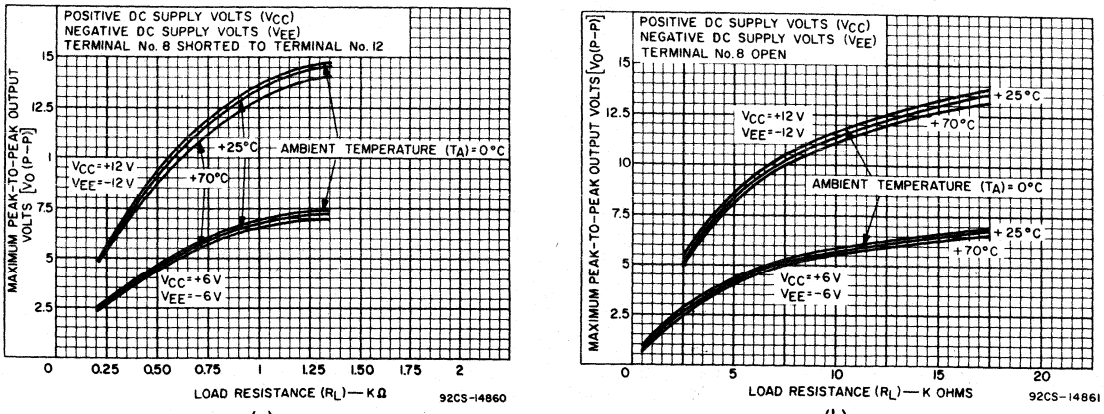
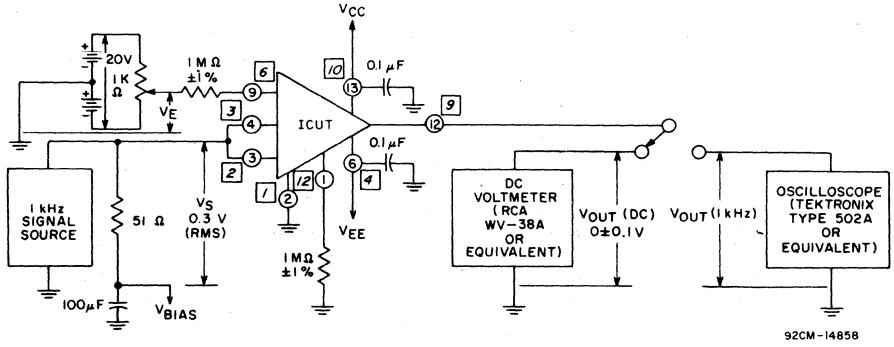


Fig.10

COMMON-MODE REJECTION RATIO AND COMMON-MODE INPUT-VOLTAGE-RANGE TEST CIRCUIT



Procedures:

Common-Mode Rejection Ratio:

1. Set V_{BIAS} = 0. Adjust V_E for V_{OUT}(DC) = 0 ± 0.1 V.
2. Apply 1-kHz sinusodial input signal and adjust for V_S = 0.3 V (RMS).
3. Measure and record the RMS value of V_{OUT}. An oscilloscope is used for this measurement so that the output signal may be visually separated.from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT}/V_S$$

$$A_{CM} \text{ in dB} = -20 \log_{10} V_S/V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$CMR \text{ in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB}.$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

Fig.11

COMMON-MODE REJECTION RATIO vs. FREQUENCY

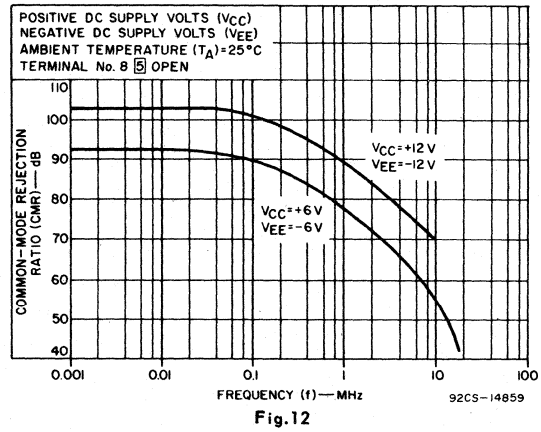


Fig.12

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038; Italic Numbers in Square Boxes are for CA3010, CA3015

SINGLE-ENDED INPUT IMPEDANCE vs. TEMPERATURE

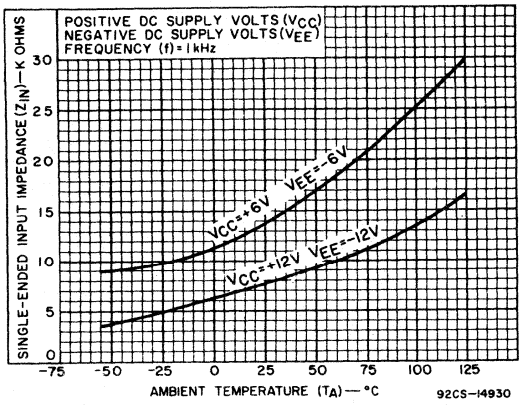


Fig.13

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

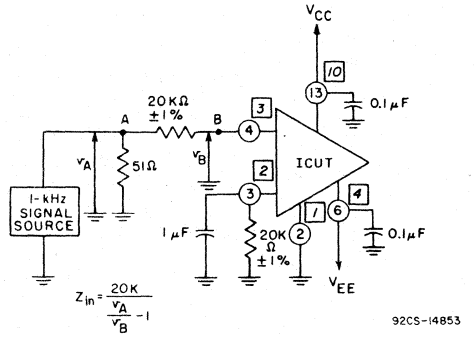


Fig.14

OUTPUT IMPEDANCE TEST CIRCUIT

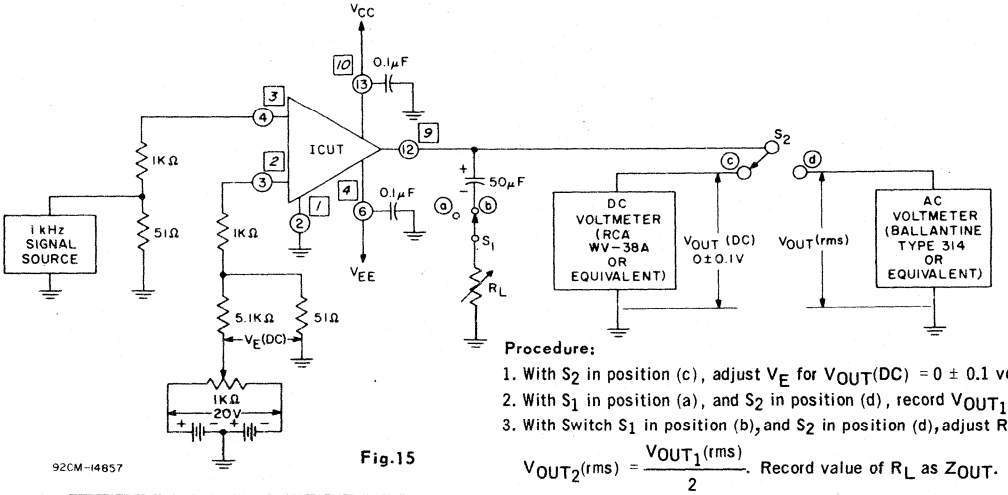
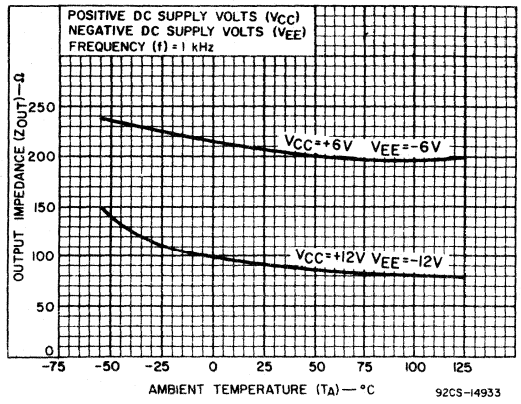


Fig.15

Procedure:

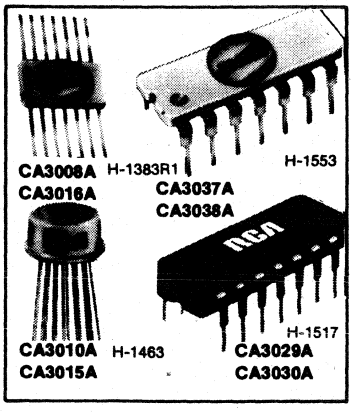
1. With S_2 in position (c), adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ volt.
2. With S_1 in position (a), and S_2 in position (d), record $V_{OUT_1}(rms)$.
3. With Switch S_1 in position (b), and S_2 in position (d), adjust R_L until $V_{OUT_2}(rms) = \frac{V_{OUT_1}(rms)}{2}$. Record value of R_L as Z_{OUT}.



OUTPUT IMPEDANCE vs. TEMPERATURE

Fig.16

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A



Operational Amplifiers

Features:

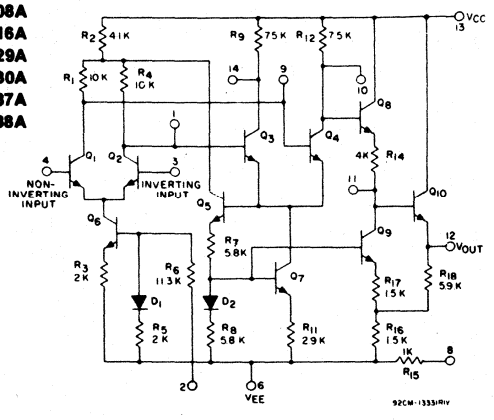
- *These new types have all the desirable features and characteristics of their prototypes plus lower noise figures and improved input characteristics for offset voltage, offset current, bias current, and impedance*
- *All types are electrically identical within their voltage groups*
- *For use in telemetry, data-processing, instrumentation, and communication equipment*
- *Built-in temperature stability from −55°C to +125°C for flat pack, TO-5 style, and ceramic dual-in-line packages; 0°C to +70°C for plastic dual-in-line packages*

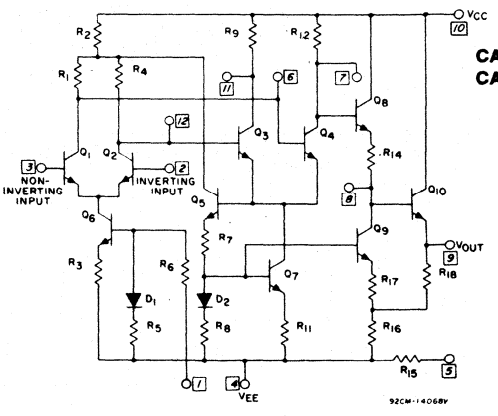
6-Volt Types	12-Volt Types	Package
CA3008A	CA3016A	14-Lead Flat Pack
CA3010A	CA3015A	12-Lead TO-5 Style
CA3029A	CA3030A	14-Lead Plastic Dual-In-Line (TO-116)
CA3037A	CA3038A	14-Lead Ceramic Dual-In-Line (TO-116)

Applications:

- *Narrow-band and band-pass amplifier*
- *Operational functions*
- *Feedback amplifier*
- *DC and video amplifier*
- *Multivibrator*
- *Oscillator*
- *Comparator*
- *Servo driver*
- *Scaling adder*
- *Balanced modulator-driver*

CA3008A
CA3016A
CA3029A
CA3030A
CA3037A
CA3038A





Schematic diagrams.

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010A	CA3008A CA3029A CA3037A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010A	CA3008A CA3029A CA3037A	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
-	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 (CA3008A, CA3029A, CA3037A) 4 & 9 (CA3010A)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.6, CA3008A, CA3029A, CA3037A No.4, CA3010A (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015A	CA3016A CA3030A CA3038A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015A	CA3016A CA3030A CA3038A	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
-	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 (CA3016A, CA3030A, CA3038A) 4 & 9 (CA3015A)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.6, CA3016A, CA3030A, CA3038A No.4, CA3015A (Substrate) DO NOT GROUND				

	CA3008A CA3010A CA3016A CA3015A CA3037A CA3038A	CA3029A CA3030A
OPERATING TEMPERATURE RANGE	-55°C to +125°C	0°C to +70°C
STORAGE TEMPERATURE RANGE	-65°C to +200°C	-25°C to +85°C

	CA3016A CA3015A CA3030A CA3038A	CA3008A CA3029A
MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V	-4 V to +1 V
MAXIMUM DEVICE DISSIPATION	600 mW	300 mW

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 (CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A), Terminal No.5 (CA3010A, CA3015A) Not Connected Unless Otherwise Specified	Test Circuit Fig.	CA3008A CA3010A CA3029A CA3037A Min.	Typ.	Max.	CA3016A CA3015A CA3030A CA3038A Min.	Typ.	Max.	Units	Typical Characteristic Curves Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	0.9 -	2 -	- -	- 1	- 2	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.3 -	1.5 -	- -	- 0.5	- 1.6	μA	2
Input Bias Current	I_I	= +6V = -6V = +12V = -12V	5	- -	2.5 -	4 -	- -	- 4.7	- 6	μA	3
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_T	= +6 V = -6 V = +12V = -12V	4	- -	40 -	- -	- -	- 175	- -	mW	none
		[5] shorted to [9] V_{CC} = +6V, V_{EE} = -6V		-	102	-	-	-	-		
		8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	500	-		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Slew Rate	SR	V_{CC} = +6V V_{EE} = -6V R_S = 1 kΩ = +12V = -12V	none	- -	3 -	- -	- -	- 7	- -	V/μs	none
Common-Mode Rejection Ratio	CMR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	- -	6.75 -	- -	- -	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	15 -	20 -	- -	- 7.5	- 10	- -	kΩ	13
Output Impedance	Z_{OUT}	= 6V = -6V = +12V = -12V	15	- -	160 -	- -	- -	- 85	- -	Ω	16
Common-Mode Input-Voltage Range	V_{CMR}	= +6V = -6V = +12V = -12V	11	- -	+0.5 -4 -	- -	- -	- +0.65 -8	- -	V	none
Noise Figure	NF	V_{CC} = +3V, V_{EE} = -3V R_S = 1 kΩ = +6V = -6V = +9V = -9V = +12V = -12V	18	- - - -	6.3 8.3 - -	9 12 - -	- - - -	6.3 8.3 10 11	9 12 14 16	dB	17

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A; Italic Numbers in Square Boxes are for CA3010A, CA3015A

INPUT OFFSET VOLTAGE AND CURRENT

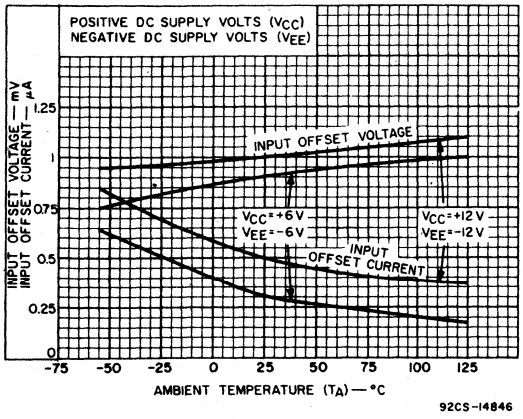


Fig.2

INPUT BIAS CURRENT

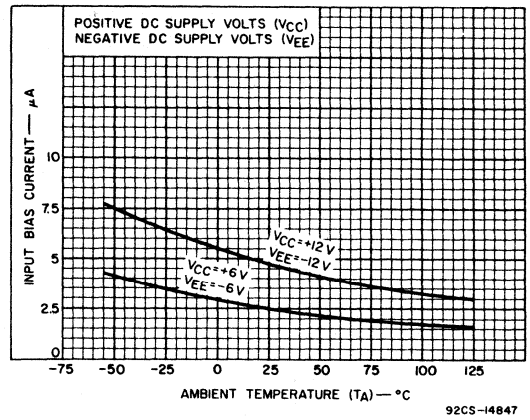


Fig.3

INPUT OFFSET VOLTAGE, INPUT OFFSET VOLTAGE SENSITIVITY, AND DEVICE DISSIPATION TEST CIRCUIT

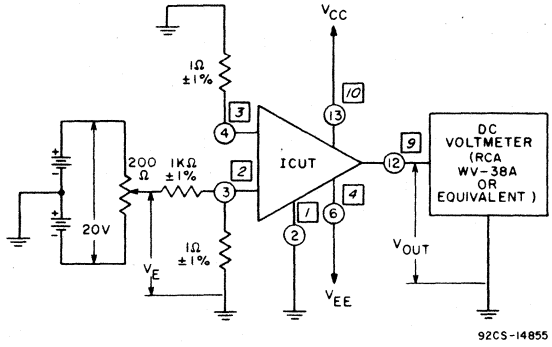


Fig.4

INPUT OFFSET CURRENT AND INPUT BIAS CURRENT TEST CIRCUIT

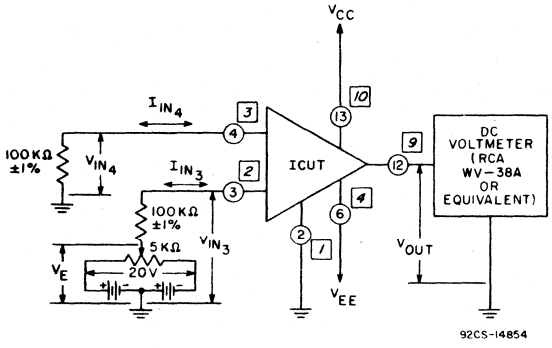


Fig.5

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the diference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\ (\text{Step 2}) - V_{OUT}\ (\text{Step 3})}{2\ \text{volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$

I_C = Direct Current into Terminal 13 or *10*

I_E = Direct Current out of Terminal 6 or *4*

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN4}
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A; Italic Numbers in Square Boxes are for CA3010A, CA3015A

OPEN LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3008A, CA3010A, CA3015A, CA3016A, CA3037A, CA3038A

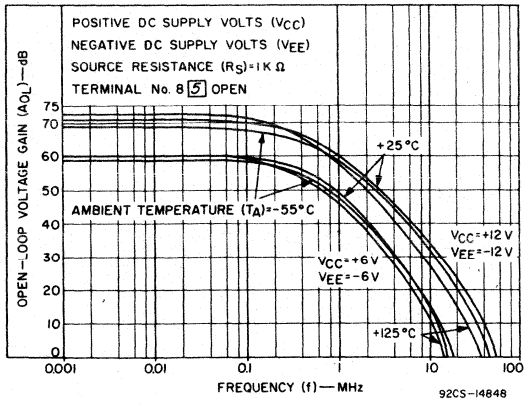


Fig.6

OPEN LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3029A AND CA3030A.

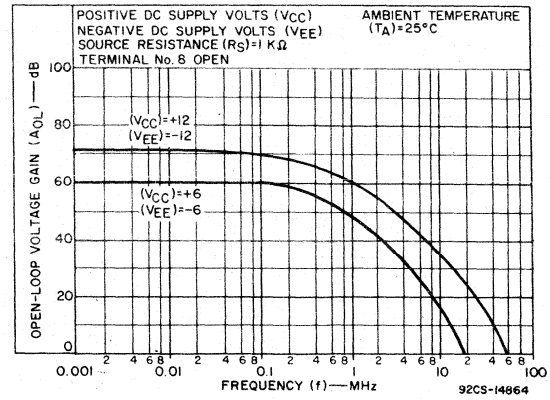
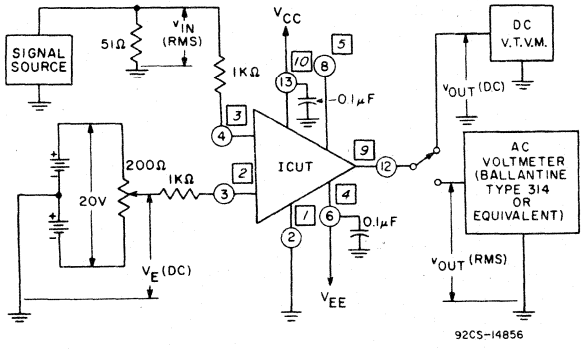


Fig.7

OPEN-LOOP DIFFERENTIAL VOLTAGE GAIN, MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE, AND OPEN-LOOP BANDWIDTH AT -3 POINT TEST CIRCUIT



Procedure:

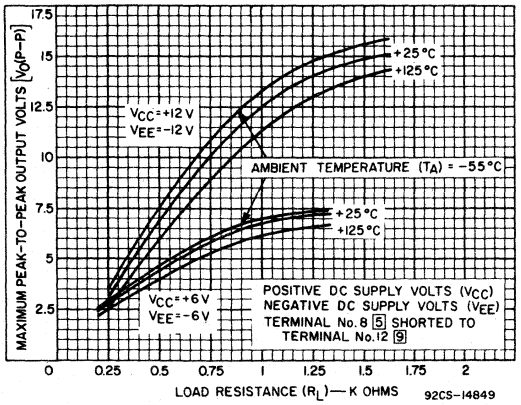
1. Adjust V_E for V_{OUT} = ±0.1 V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at f = 1 kHz

$$A_{OL} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

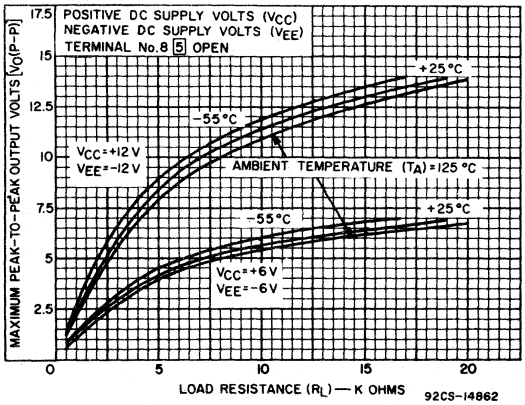
3. Measure Maximum Peak-to-Peak Output Voltage at f = 1 kHz
4. Measure Open-Loop Bandwidth at -3 dB Point
   Reference Level = A_{OL} at 1 kHz

Fig.8

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3008A, CA3010A, CA3015A, CA3016A, CA3037A, CA3038A



(a)



(b)

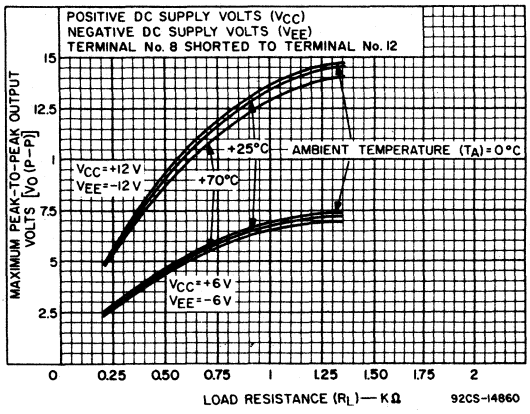
Fig.9

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

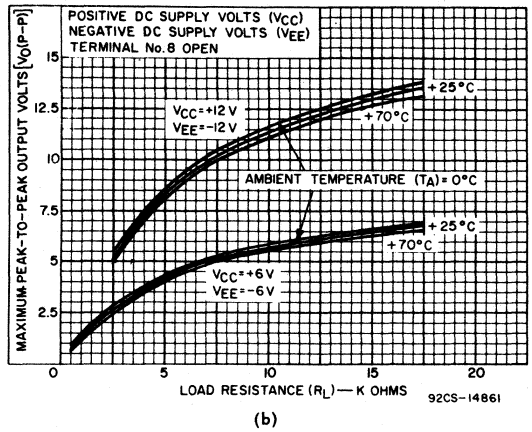
TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A; Italic Numbers in Square Boxes are for CA3010A, CA3015A

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3029A AND CA3030A



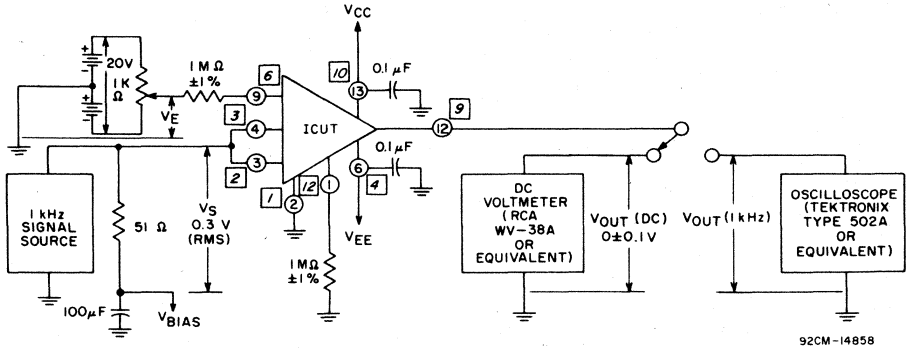
(a)



(b)

Fig.10

COMMON-MODE REJECTION RATIO AND COMMON-MODE INPUT-VOLTAGE-RANGE TEST CIRCUIT



Procedures:

Common-Mode Rejection Ratio:

1. Set V_{BIAS} = 0. Adjust V_E for V_{OUT}(DC) = 0 ± 0.1 V.
2. Apply 1-kHz sinusodial input signal and adjust for V_S = 0.3 V (RMS).
3. Measure and record the RMS value of V_{OUT}. An oscilloscope is used for this measurement so that the output signal may be visually separated.from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT}/V_S$$

$$A_{CM} \text{ in dB} = -20 \log_{10} V_S/V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$CMR \text{ in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB}.$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

Fig.11

COMMON-MODE REJECTION RATIO vs. FREQUENCY

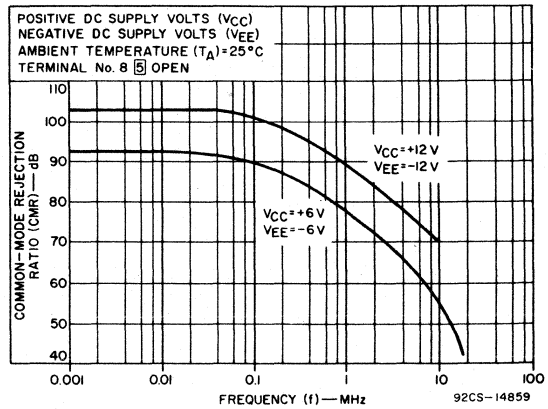


Fig.12

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A; Italic Numbers in Square Boxes are for CA3010A, CA3015A

SINGLE-ENDED INPUT IMPEDANCE vs. TEMPERATURE

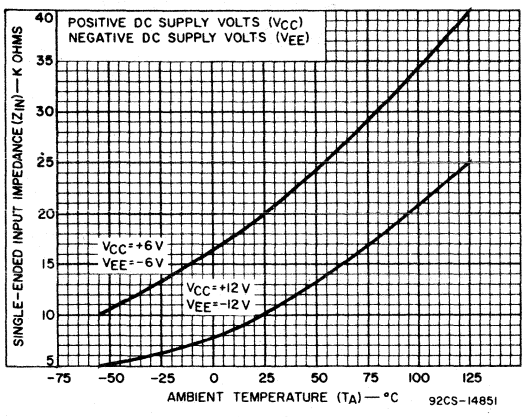


Fig.13

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

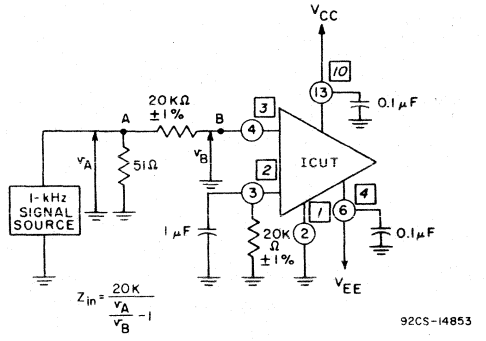


Fig.14

OUTPUT IMPEDANCE TEST CIRCUIT

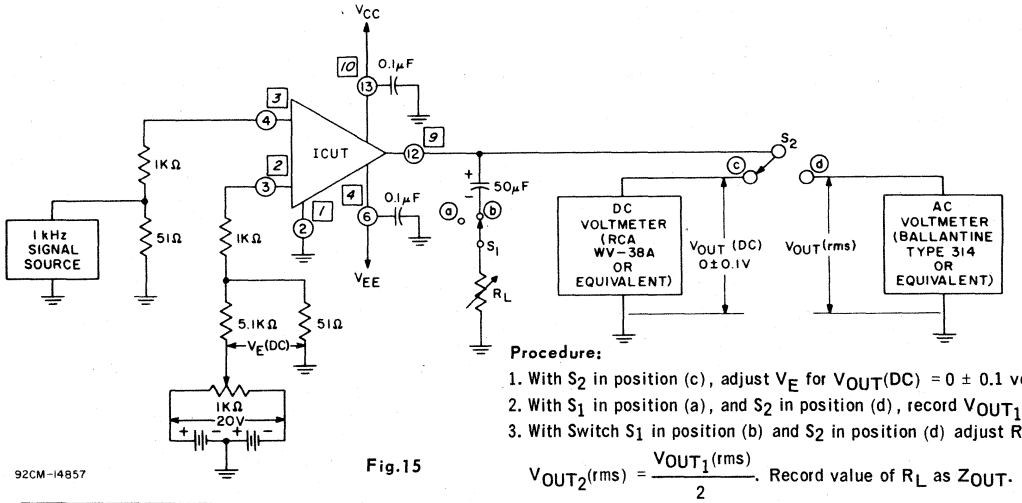
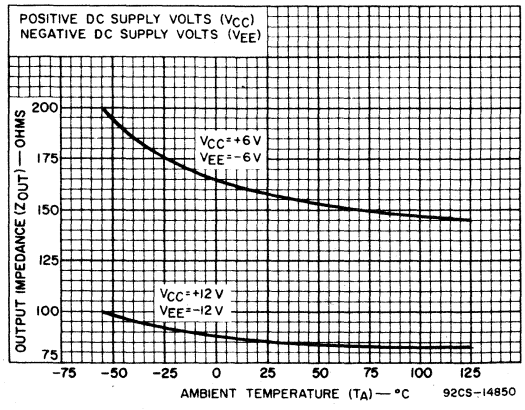


Fig.15

Procedure:

1. With S_2 in position (c), adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ volt.
2. With S_1 in position (a), and S_2 in position (d), record $V_{OUT_1}(rms)$.
3. With Switch S_1 in position (b) and S_2 in position (d) adjust R_L until $V_{OUT_2}(rms) = \frac{V_{OUT_1}(rms)}{2}$. Record value of R_L as Z_{OUT}.



OUTPUT IMPEDANCE vs. TEMPERATURE

Fig.16

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

NOISE FIGURE vs. FREQUENCY

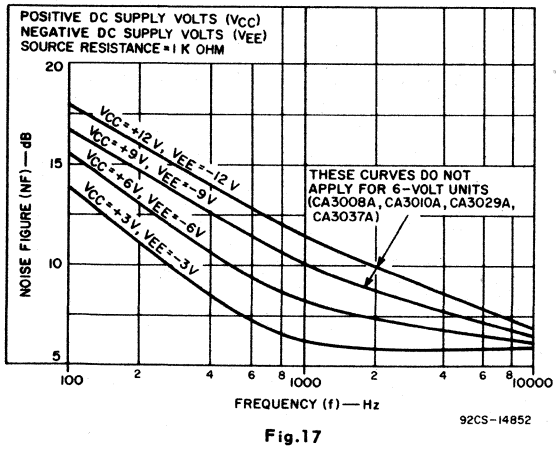


Fig.17

NOISE FIGURE TEST CIRCUIT

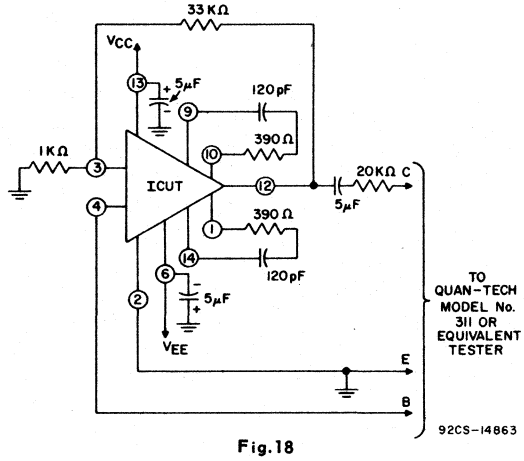


Fig.18

12-Lead TO-5

H-1463

Low-Power Wideband Amplifiers

Features:

- *Lower DC Power Drain:*
  P_T { *CA3021 = 4 mW typ.*; *CA3022 = 12.5 mW typ.*; *CA3023 = 35 mW tp.* } *at V_{CC} = 6 V*
- *Excellent frequency response:*
  -3dB BW { *CA3021 = 2.4 MHz typ.*; *CA3022 = 7.5 MHz typ.*; *CA3023 = 16 MHz typ.* }
- *High Voltage Gain:*
  A { *CA3021 = 56 dB typ. at 0.5 MHz*; *CA3022 = 57 dB typ. at 2.5 MHz*; *CA3023 = 53 dB typ. at 5 MHz* }
- *Wide AGC Range: 33 dB typ.*
- *Only one power supply (4.5 to 12 V) required*
- *Hermetically sealed 12-lead TO-5-style package*
- *Operation from −55° C to +125° C*

Applications:

- *Gain-controlled linear amplifiers*
- *AM/FM IF amplifiers*
- *Video amplifiers*
- *Limiters*

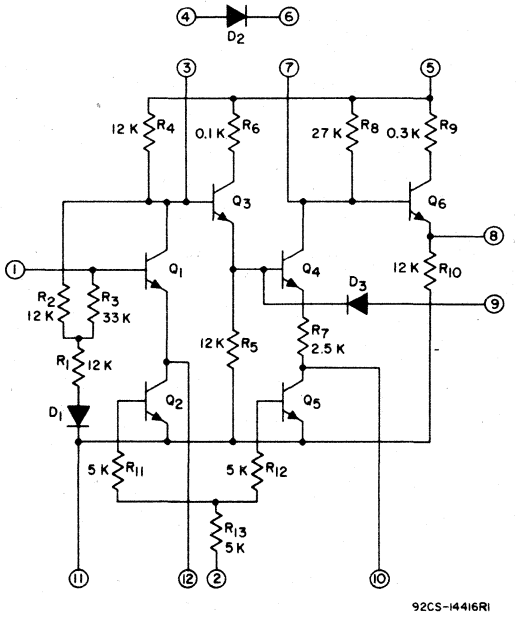


Fig. 1 - Schematic diagram for CA3021, CA3022, and CA3023.

CA3021, CA3022, CA3023

ABSOLUTE-MAXIMUM RATINGS:

OPERATING-TEMPERATURE RANGE	-55°C to +125°C	
STORAGE-TEMPERATURE RANGE	-65°C to +150°C	
LEAD TEMPERATURE (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C	
DEVICE DISSIPATION, P_T	120 max.	mW
INPUT-SIGNAL VOLTAGE	-3, +3 max.	V
DC VOLTAGES AND CURRENTS	See Table Below	

	VOLTAGE OR CURRENT LIMITS		CIRCUIT CONDITIONS	
TERMINAL	NEGATIVE	POSITIVE	TERMINAL	CONDITIONS
1	-3V	+3V	1	Connected to Voltage Source through 100Ω Resistor
			5	+12V
			10, 11, 12	Ground
2	-3V	+12V	5	+12V
			10, 11, 12	Ground
3	0V	+12V	5	+12V
			10, 11, 12	Ground
4	-12V	+12V	6, 11	Ground
	10 max. mA			
5	0V	+18V	10, 11, 12	Ground
6	-12V	+12V	5, 11	Ground
	10 max. mA			

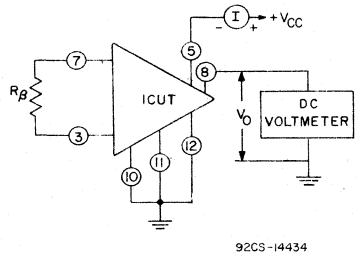
	VOLTAGE OR CURRENT LIMITS		CIRCUIT CONDITIONS	
TERMINAL	NEGATIVE	POSITIVE	TERMINAL	CONDITIONS
7	0V	+12V	5	+12V
			10, 11, 12	Ground
8	20 max. mA		5	+12V
			10, 11, 12	Ground
9	-0.5V	+3V	5	+12V
			10, 11, 12	Ground
10	0V	+4V	2,5	+12V
			11	Ground
11	-6V	+12V	2	Ground
			5	+12V
12	0V	+4V	2,5	+12V
			11	Ground

ELECTRICAL CHARACTERISTICS, at $T_A = 25^oC$, $V_{CC} = +6V$, unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS										
		TEST SETUP AND PROCEDURE	FEEDBACK RESISTANCE (R_β) BETWEEN TERMINALS 3 AND 7	FREQUENCY f	CA3021 (TA5219)			CA3022 (TA5236)			CA3023 (TA5218)			UNITS	TYPICAL CHARACTERISTIC CURVE
		Fig.	Ω	MHz	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units	Fig.
Device Dissipation	P_T	2	∞	-	1	4	8	–	–	–	–	–	–	mW	3a,d
			∞	–	–	–	–	5	12.5	24	–	–	–	mW	3b,d
			∞	–	–	–	–	–	–	–	24	35	48	mW	3c,d
Quiescent Output Voltage	V_O	2	39k	–	–	2.2	–	–	–	–	–	–	–	V	–
			10k	–	–	–	–	–	1.9	–	–	–	–	V	
			4.7k	–	–	–	–	–	–	–	–	1.3	–	V	
AGC Source Current	I_{AGC}	4	V_{AGC} =+6V		–	0.8	–	–	0.8	–	–	0.8	–	mA	–
Voltage Gain	A	5	560k	0.5	50	56	–	–	–	–	–	–	–	dB	6a
			39k	0.8	40	46	–	–	–	–	–	–	–	dB	6a,d
			39k	2.5	–	–	–	50	57	–	–	–	–	dB	6b
			10k	3	–	–	–	40	44	–	–	–	–	dB	6b,d
			18k	5	–	–	–	–	–	–	50	53	–	dB	6c
			4.7k	10	–	–	–	–	–	–	40	44	–	dB	6c,d
Bandwidth at -3 dB Point	BW	5	39k	–	0.8	2.4	–	–	–	–	–	–	–	MHz	6a
			10k	–	–	–	–	3	7.5	–	–	–	–	MHz	6b
			4.7k	–	–	–	–	–	–	–	10	16	–	MHz	6c
Input-Impedance Components: Input Resistance	R_{IN}	7	39k	1	–	4000	–	–	–	–	–	–	–	Ω	–
			10k	5	–	–	–	–	1300	–	–	–	–	Ω	
			4.7k	10	–	–	–	–	–	–	–	300	–	Ω	
Input-Impedance Components: Input Capacitance	C_{IN}	7	39k	1	–	11	–	–	–	–	–	–	–	pF	–
			10k	5	–	–	–	–	18	–	–	–	–	pF	
			4.7k	10	–	–	–	–	–	–	–	13	–	pF	
Output Resistance	R_{OUT}	8	39k	1	–	300	–	–	–	–	–	–	–	Ω	–
			10k	5	–	–	–	–	120	–	–	–	–	Ω	
			4.7k	10	–	–	–	–	–	–	–	100	–	Ω	
Noise Figure	NF	9	39k	1	–	4.2	8.5	–	–	–	–	–	–	dB	–
			10k	1	–	–	–	–	4.4	8.5	–	–	–	dB	
			4.7k	1	–	–	–	–	–	–	–	6.5	8.5	dB	
AGC Range	AGC	10	–	1	–	33	–	–	–	–	–	–	–	dB	–
			–	5	–	–	–	–	33	–	–	–	–	dB	
			–	10	–	–	–	–	–	–	–	33	–	dB	
Maximum Output Voltage (RMS Value)	v_{out}	5	39k	1	–	0.6	–	–	–	–	–	–	–	V(rms)	–
			10k	5	–	–	–	–	0.7	–	–	–	–	V(rms)	
			4.7k	10	–	–	–	–	–	–	–	0.5	–	V(rms)	

CA3021, CA3022, CA3023

TEST SETUP FOR MEASUREMENT OF DEVICE DISSIPATION AND QUIESCENT OUTPUT VOLTAGE



$P_T = V_{CC}(I)$

Fig.2

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3022

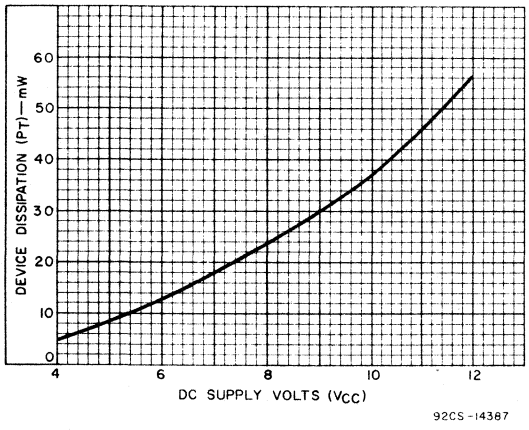


Fig.3(b)

DEVICE DISSIPATION VS TEMPERATURE FOR CA3021, CA3022, AND CA3023

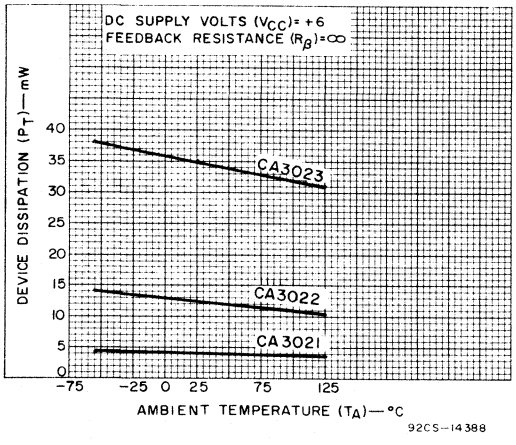


Fig.3(d)

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3021

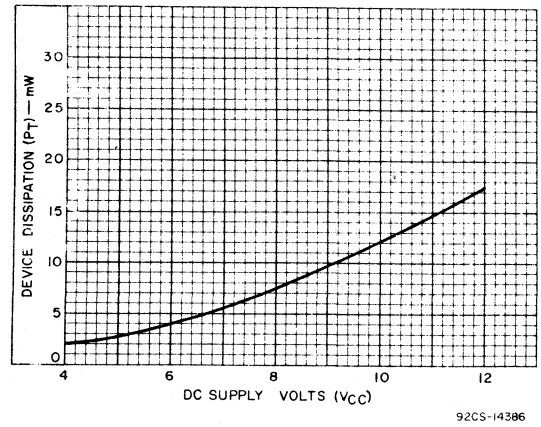


Fig.3(a)

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3023

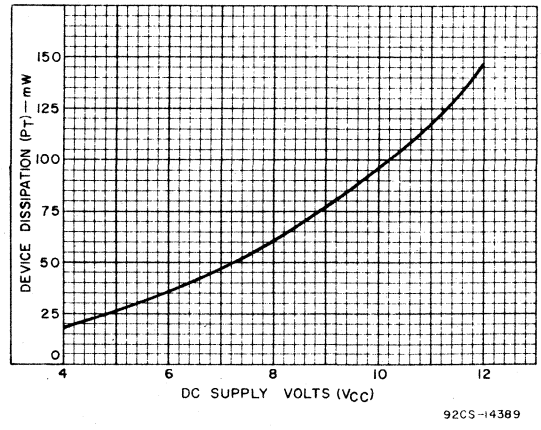
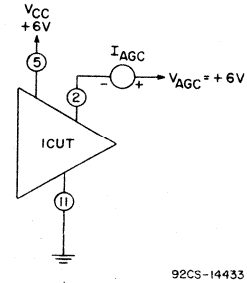


Fig.3(c)

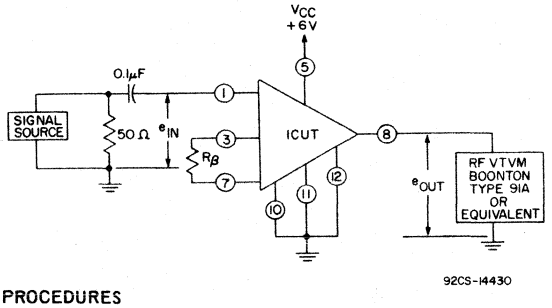
TEST SETUP FOR MEASUREMENT OF AGC SOURCE CURRENT



I_{AGC} IS THE CURRENT FLOWING INTO TERMINAL 2.

Fig.4

TEST SETUP FOR MEASUREMENTS OF VOLTAGE-GAIN, -3dB BANDWIDTH, AND MAXIMUM OUTPUT VOLTAGE



PROCEDURES

Voltage Gain:

(a) Set e_{in} = 0.5 mVat frequency specified, read e_{out} Voltage Gain

(A) = $20 \log_{10} \frac{e_{out}}{e_{in}}$

Bandwidth:

(a) Set e_{out} to a convenient reference voltage at f = 100 kHz and record corresponding value of e_{in}.

(b) Increase the frequency, keeping e_{in} constant until e_{out} drops 3-dB. Record Bandwidth.

Fig.5

VOLTAGE GAIN VS FREQUENCY FOR CA3021

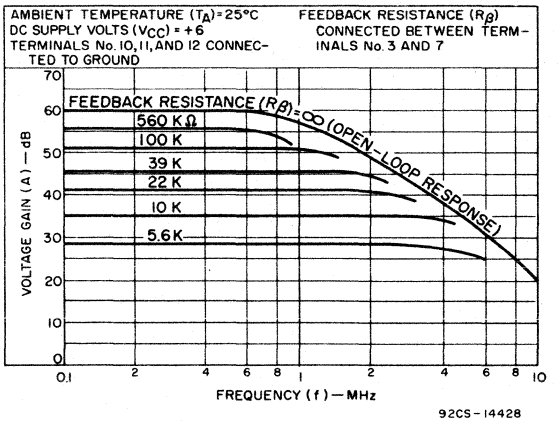


Fig.6(a)

VOLTAGE GAIN VS FREQUENCY FOR CA3022

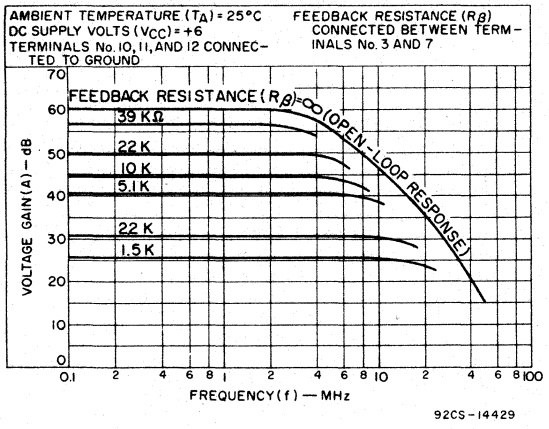


Fig.6(b)

VOLTAGE GAIN VS FREQUENCY FOR CA3023

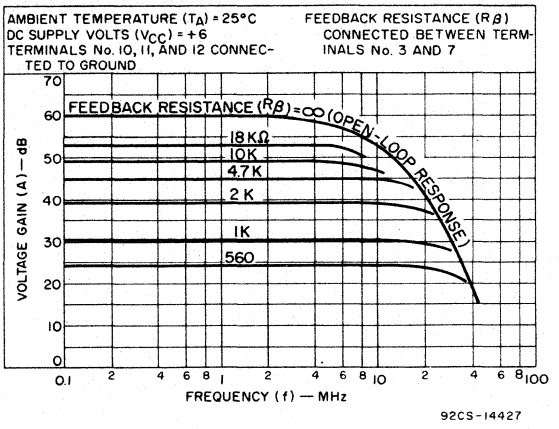


Fig.6(c)

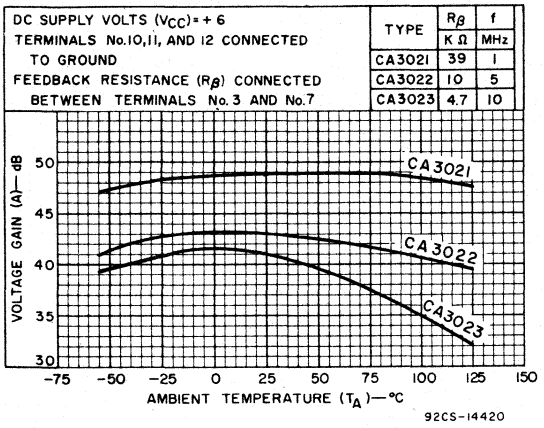
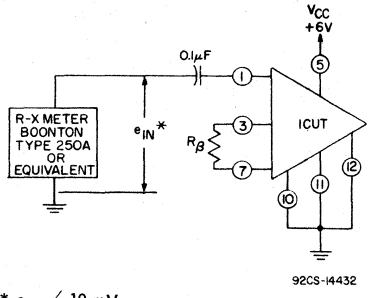


Fig.6(d)

VOLTAGE GAIN VS TEMPERATURE FOR CA3021, CA3022, AND CA3023

CA3021, CA3022, CA3023

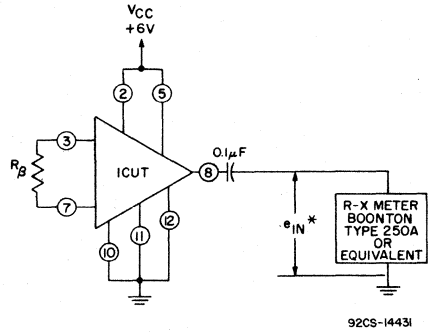
TEST SETUP FOR MEASUREMENT OF INPUT-IMPEDANCE COMPONENTS



* $e_{in} \leq 10$ mV

Fig.7

TEST SETUP FOR MEASUREMENT OF OUTPUT RESISTANCE

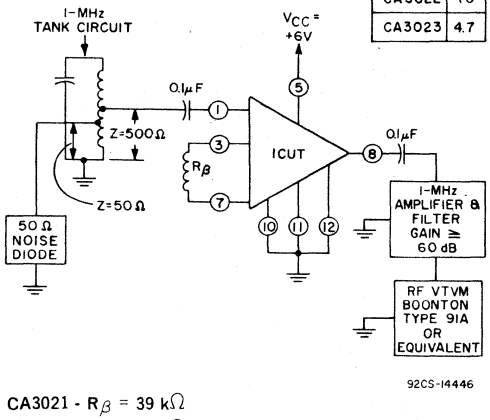


* $e_{in} \leq 10$ mV

Fig.8

TEST SETUP FOR MEASUREMENT OF NOISE FIGURE

ICUT	Rβ KΩ
CA3021	39
CA3022	10
CA3023	4.7

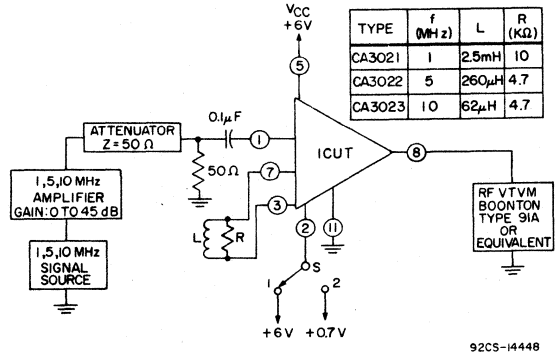


CA3021 - R_β = 39 kΩ
CA3022 - R_β = 10 kΩ
CA3023 - R_β = 4.7 kΩ

Fig.9

TEST SETUP FOR MEASUREMENT OF AGC RANGE

TYPE	f (MHz)	L	R (KΩ)
CA3021	1	2.5mH	10
CA3022	5	260μH	4.7
CA3023	10	62μH	4.7



$$\text{AGC RANGE} = 20 \log_{10} \frac{\text{A WITH S IN POSITION 1}}{\text{A WITH S IN POSITION 2}}$$

(A = VOLTAGE GAIN)

	f MHz
CA3021	1
CA3022	5
CA3023	10

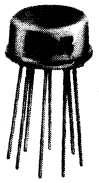
Fig. 10

CA3100 Types

Wideband Operational Amplifier

Mini-DIP
(E Suffix)
1-1817

8-Lead TO-5
With Dual-In-Line
Formed Leads
"DIL-CAN"
(S Suffix)
H-1787



8-Lead TO-5
(T Suffix)
H-1528

Features:

- *High open-loop gain at video frequencies - 42 dB typ. at 1 MHz*
- *High unity-gain crossover frequency (f_T) - 38 MHz typ.*
- *Wide power bandwidth - V_O = 18 Vp-p typ. at 1.2 MHz*
- *High slew rate - 70 V/μs [typ.] in 20 dB amplifier*
  25 V/μs [typ.] in unity-gain amplifier
- *Fast settling time - 0.6 μs typ.*
- *High output current - ±15 mA min.*
- *LM118, 748/LM101 pin compatibility*
- *Single capacitor compensation*
- *Offset null terminals*

Applications:

- *Video amplifiers*
- *Fast peak detectors*
- *Meter-driver amplifiers*
- *High-frequency feedback amplifiers*
- *Video pre-drivers*
- *Oscillators*
- *Multivibrators*
- *Voltage-controlled oscillator*
- *Fast comparators*

RCA-CA3100S, CA3100T is a large-signal wideband, high-speed operational amplifier which has a unity gain crossover frequency (f_T) of approximately 38 MHz and an open-loop, 3 dB corner frequency of approximately 110 kHz. It can operate at a total supply voltage of from 14 to 36 volts (±7 to ±18 volts when using split supplies) and can provide at least 18 Vp-p and 30 mA p-p at the output when operating from ±15 volt supplies. The CA3100 can be compensated with a single external capacitor and has dc offset adjust terminals for those applications requiring offset null. (See Fig. 15).

The CA3100 circuit contains both bipolar and P-MOS transistors on a single monolithic chip.

The CA3100 is supplied in either the standard 8-lead TO-5 package ("T" suffix), or in the 8-lead TO-5 dual-in-line formed-lead "DIL'CAN" package ("S" suffix).

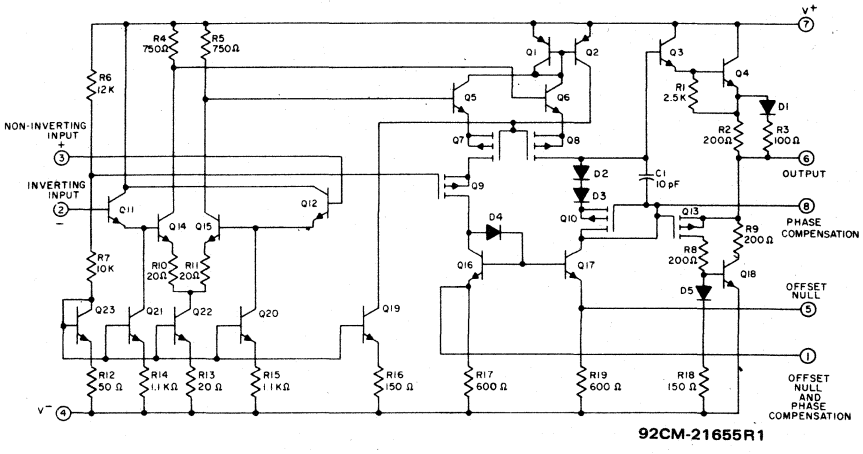


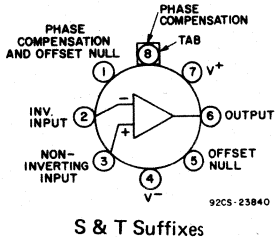
Fig. 1 — Schematic diagram for CA3100.

CA3100 Types

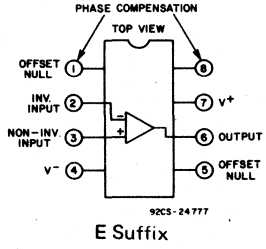
ELECTRICAL CHARACTERISTICS, *At T_A = 25°C:*

CHARACTERISTICS	TEST CONDITIONS SUPPLY VOLTAGE (V^+,V^-)=15 V UNLESS OTHERWISE SPECIFIED	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
STATIC					
Input Offset Voltage, V_{IO}	V_O = 0 ± 0.1 V	–	±1	±5	mV
Input Bias Current, I_{IB}	V_O = 0 ± 1 V	–	0.7	2	μA
Input Offset Current, I_{IO}	V_O = 0 ± 1 V	–	±0.05	±0.4	μA
Low-Frequency Open-Loop Voltage Gain, A_{OL}●	V_O = ± 1 V Peak, F = 1 kHz	56	61	–	dB
Common-Mode Input Voltage Range, V_{ICR}	CMRR ≥ 76 dB	±12	+14 −13	–	V
Common-Mode Rejection Ratio, CMRR	V_I Common Mode = ± 12 V	76	90	–	dB
Maximum Output Voltage: Positive, V_{OM}^+	Differential Input Voltage = 0 ± 0.1 V, R_L = 2 KΩ	+9	+11	–	V
Maximum Output Voltage: Negative, V_{OM}^-	Differential Input Voltage = 0 ± 0.1 V, R_L = 2 KΩ	−9	−11	–	V
Maximum Output Current: Positive, I_{OM}^+	Differential Input Voltage = 0 ± 0.1 V, R_L = 250 Ω	+15	+30	–	mA
Maximum Output Current: Negative, I_{OM}^-	Differential Input Voltage = 0 ± 0.1 V, R_L = 250 Ω	−15	−30	–	mA
Supply Current, I^+	V_O = 0 ± 0.1 V, R_L ≥ 10 KΩ	–	8.5	10.5	mA
Power-Supply Rejection Ratio, PSRR	ΔV^+ = ± 1 V, ΔV^- = ± 1 V	60	70	–	dB
DYNAMIC					
Unity-Gain Crossover Frequency, f_T	C_C = 0, V_O = 0.3 V (P-P)	–	38	–	MHz
1-MHz Open-Loop Voltage Gain, A_{OL}	f = 1 MHz, C_C = 0, V_O = 10 V (P-P)	36	42	–	dB
Slew Rate, SR: 20-dB Amplifier	A_V = 10, C_C = 0, V_I = 1 V (Pulse)	50	70	–	V/μs
Slew Rate, SR: Follower Mode	A_V = 1, C_C = 10 pF, V_I = 10 V (Pulse)	–	25	–	V/μs
Power Bandwidth, PBW▲: 20-dB Amplifier	A_V = 10, C_C = 0, V_O = 18 V (P-P)	0.8	1.2	–	MHz
Power Bandwidth, PBW▲: Follower Mode	A_V = 1, C_C = 10 pF, V_O = 18 V (P-P)	–	0.4	–	MHz
Open-Loop Differential Input Impedance, Z_I	F = 1 MHz	–	30	–	KΩ
Open-Loop Output Impedance, Z_O	F = 1 MHz	–	110	–	Ω
Wideband Noise Voltage Referred to Input, e_N(Total)	BW = 1 MHz, R_S = 1 KΩ	–	8	–	μV_{RMS}
Settling Time, t_s To Within ± 50 mV of 9 V Output Swing	R_L = 2 KΩ, C_L = 20 pF	–	0.6	–	μs

▲ Power Bandwidth = $\frac{\text{Slew Rate}}{\pi V_O \text{ (P-P)}}$ ● Low-frequency dynamic characteristic



S & T Suffixes



E Suffix

TERMINAL ASSIGNMENTS

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Supply Voltage (between V+ and V⁻ terminals)	36	V
Differential Input Voltage	±12	V
Input Voltage to Ground*	±15	V
Offset Terminal to V⁻ Terminal Voltage	±0.5	V
Output Current	50	mA•
Device Dissipation:		
Up to T_A = 55°C	630	mW
Above T_A = 55°C	6.67	mW/°C
Ambient Temperature Range:		
Operating:		
E Type	−40 to +85	°C
S and T Types	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

* If the supply voltage is less than ±15 volts, the maximum input voltage to ground is equal to the supply voltage.

• CA3100S, CA3100T does not contain circuitry to protect against short circuits in the output.

TYPICAL CHARACTERISTIC CURVES

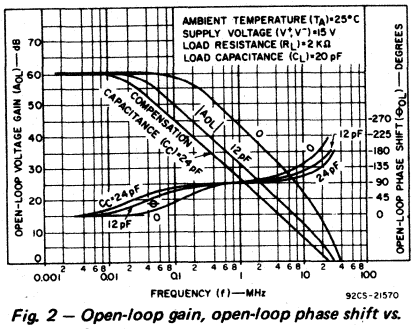


Fig. 2 – Open-loop gain, open-loop phase shift vs. frequency.

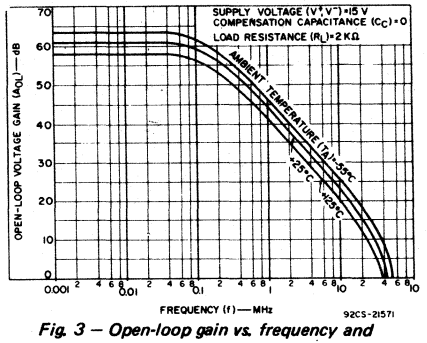


Fig. 3 – Open-loop gain vs. frequency and temperature.

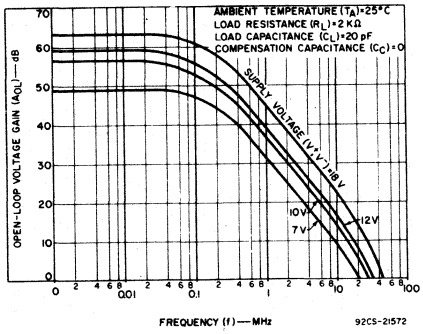


Fig. 4 – Open-loop gain vs. frequency and supply voltage.

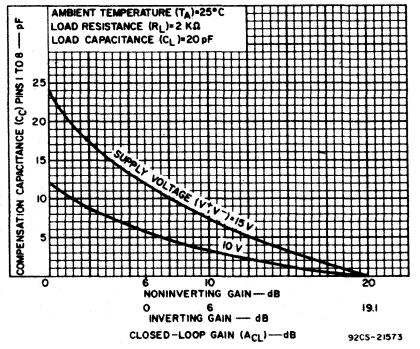


Fig. 5 – Required compensation capacitance vs. closed-loop gain.

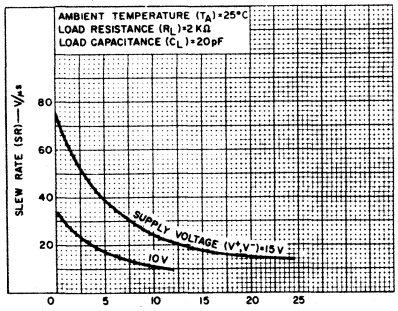


Fig. 6 – Slew rate vs. compensation capacitance.

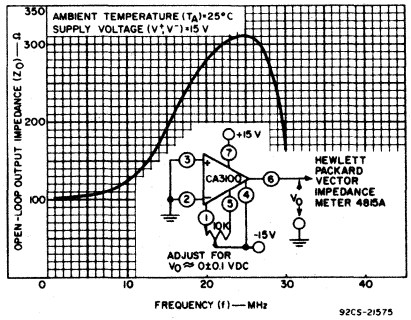


Fig. 7 – Typical open-loop output impedance vs. frequency.

TYPICAL CHARACTERISTIC CURVES (Cont'd)

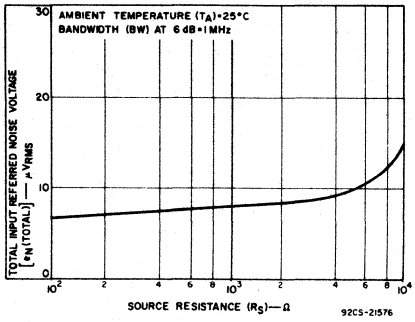


Fig. 8 – Wideband input noise voltage vs. source resistance.

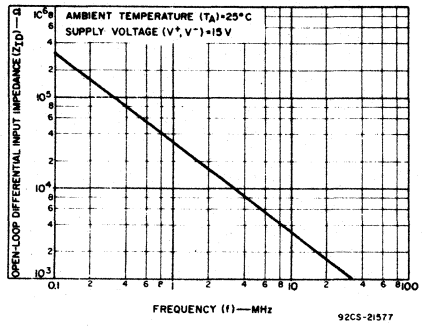


Fig. 9 – Typical open-loop differential input impedance vs. frequency.

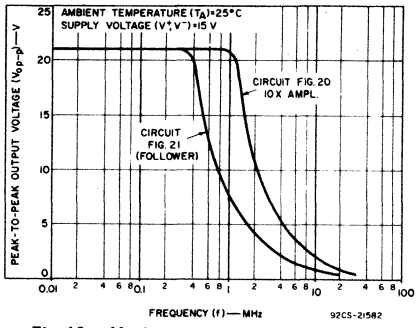


Fig. 10 – Maximum output voltage swing vs. frequency.

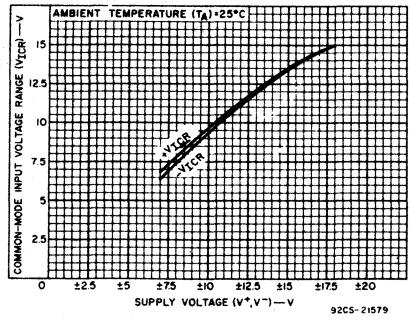


Fig. 11 – Common-mode input voltage range vs. supply voltage.

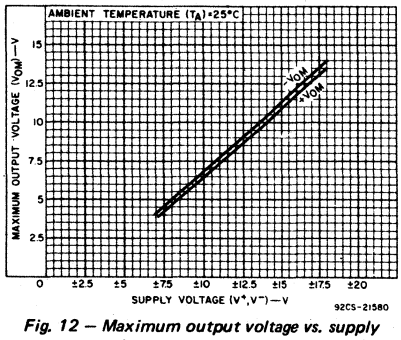


Fig. 12 – Maximum output voltage vs. supply voltage.

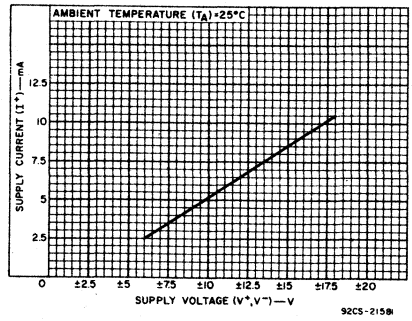


Fig. 13 – Supply current vs. supply voltage.

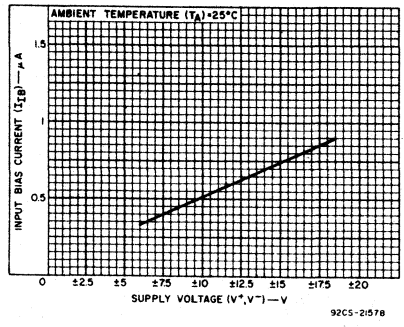


Fig. 14 – Input bias current vs. supply voltage.

TEST CIRCUITS

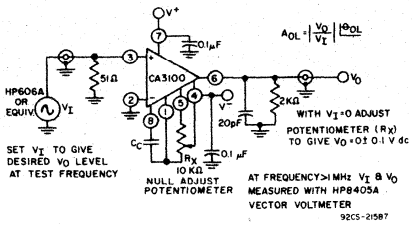


Fig. 15 – Open-loop voltage gain test circuit.

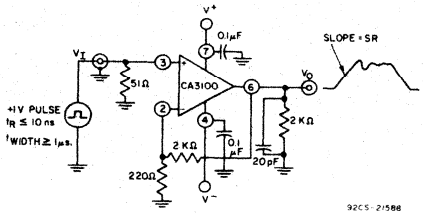


Fig. 16 – Slew rate in 10X amplifier test circuit.

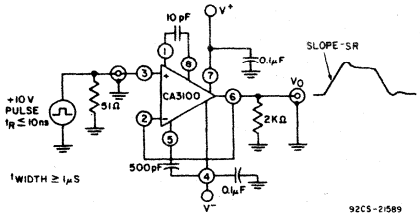


Fig. 17 – Follower slew rate test circuit.

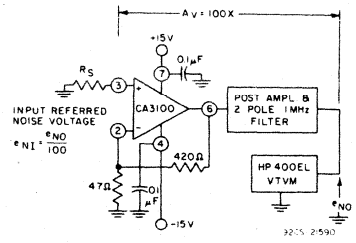


Fig. 18 – Wideband input noise voltage test circuit.

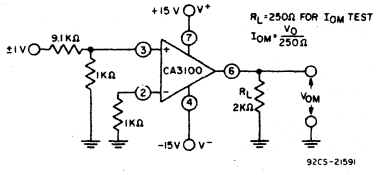


Fig. 19 – Output voltage swing (V_{OM}), output current swing (I_{OM}) test circuit.

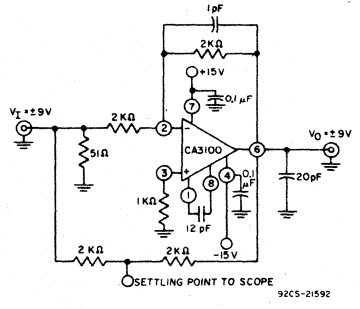


Fig. 20 – Settling time test circuit.

TYPICAL APPLICATIONS

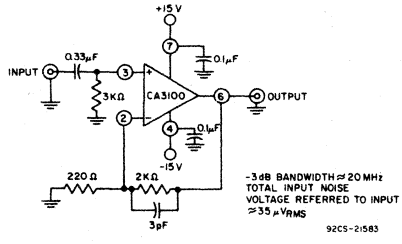


Fig. 21 – 20 dB video amplifier.

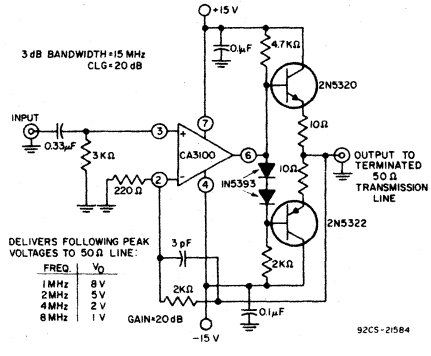


Fig. 22 – 20 dB video line driver.

TYPICAL APPLICATIONS (Cont'd)

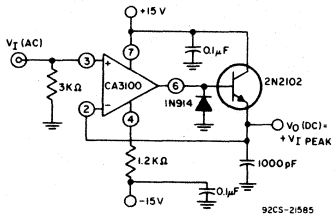


Fig. 23 – Fast positive peak detector.

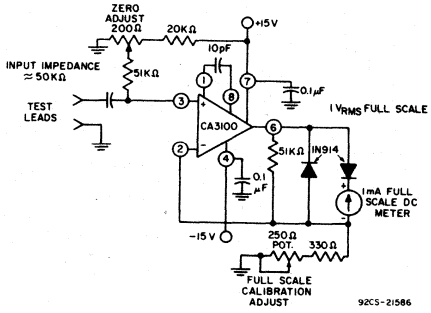
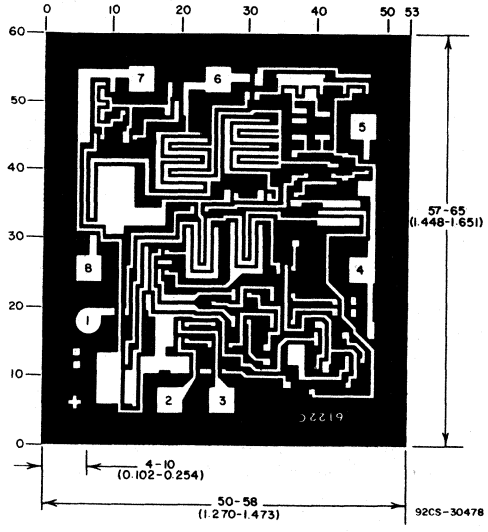


Fig. 24 – 1 MHz meter-driver amplifier.

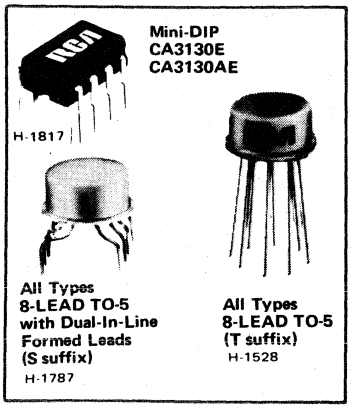
Chip Dimensions and Pad Layout



CA3100H Chip

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



BiMOS Operational Amplifiers

With MOS/FET Input/ COS/MOS Output

FEATURES:

- *MOS/FET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 × 10^{12}Ω) typ.
  very low II = 5 pA typ. at 15-V operation
  2 pA typ. at 5-V operation
- *Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *COS/MOS output stage permits signal swing to either (or both) supply rails*

} *Ideal for single-supply applications*

RCA-CA3130T, CA3130E, CA3130S, CA-3130AT, CA 3130AS, CA3130AE, CA3130BT, and CA3130BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3130 Series is supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA3130 is available in chip form (H suffix). The CA3130 and CA3130A are also available in the Mini-DIP 8-lead dual-in-line plastic package (E suffix). All types operate over the full military-temperature range of -55°C to +125°C. The CA3130B is intended for applications requiring premium-grade specifications. The CA3130A offers superior input characteristics over those of the CA3130.

- *Low V_{IO}: 2 mV max. (CA3130B)*
- *Wide BW: 15 MHz typ. (unity-gain crossover)*
- *High SR: 10 V/μs typ. (unity-gain follower)*
- *High output current (I_O): 20 mA typ.*
- *High A_{OL}: 320,000 (110 dB) typ.*
- *Compensation with single external capacitor*

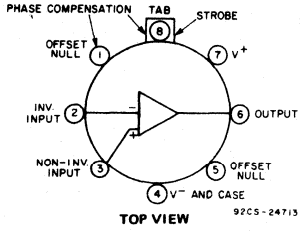
APPLICATIONS:

- *Ground-referenced single-supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *High-input-impedance comparators (ideal interface with digital COS/MOS)*
- *High-input-impedance wideband amplifiers*
- *Voltage followers (e.g., follower for single-supply D/A converter)*
- *Voltage regulators (permits control of output voltage down to zero volts)*
- *Peak detectors*
- *Single-supply full-wave precision rectifiers*
- *Photo-diode sensor amplifiers*

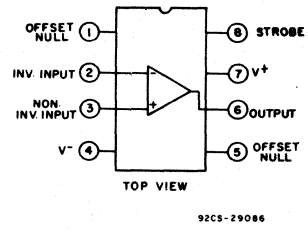
CA3130, CA3130A, CA3130B

ELECTRICAL CHARACTERISTICS at T_A=25°C, V^+=15 V, V^- = 0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS									Units
	CA3130B (T,S)			CA3130A (T,S,E)			CA3130 (T,S,E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.8	2	–	2	5	–	8	15	mV
Input Offset Current, $\|I_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	–	5	20	–	5	30	–	5	50	pA
Large-Signal Voltage Gain, A_{OL}	100 k	320 k	–	50 k	320 k	–	50 k	320 k	–	V/V
V_O=10 V_{p-p}, R_L=2 kΩ	100	110	–	94	110	–	94	110	–	dB
Common-Mode Rejection Ratio, CMRR	86	100	–	80	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR}	0	−0.5 to 12	10	0	−0.5 to 12	10	0	−0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	–	32	100	–	32	150	–	32	320	μV/V
Maximum Output Voltage:										
At R_L=2 kΩ V_{OM}^+	12	13.3	–	12	13.3	–	12	13.3	–	V
V_{OM}^-	–	0.002	0.01	–	0.002	0.01	–	0.002	0.01	
At R_L=∞ V_{OM}^+	14.99	15	–	14.99	15	–	14.99	15	–	
V_{OM}^-	–	0	0.01	–	0	0.01	–	0	0.01	
Maximum Output Current: I_{OM}^+ (Source) @ V_O = 0 V	12	22	45	12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O = 15 V	12	20	45	12	20	45	12	20	45	
Supply Current, I^+: V_O=7.5 V, R_L=∞	–	10	15	–	10	15	–	10	15	mA
V_O = 0 V, R_L = ∞	–	2	3	–	2	3	–	2	3	
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$*	–	5	–	–	10	–	–	10	–	μV/°C



S and T Suffixes



E Suffix

Fig.1 – Functional diagrams for the CA3130 series.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS ($V^+ = +7.5$ V, $V^- = -7.5$ V, $T_A = 25^oC$ (Unless Otherwise Specified))	CA3130B (T,S)	CA3130A (T,S,E)	CA3130 (T,S,E)	UNITS
Input Offset Voltage Adjustment Range	10 kΩ across Terms. 4 and 5 or 4 and 1	±22	±22	±22	mV
Input Resistance, R_I		1.5	1.5	1.5	TΩ
Input Capacitance, C_I	f = 1 MHz	4.3	4.3	4.3	pF
Equivalent Input Noise Voltage, e_n	BW = 0.2 MHz, R_S = 1 MΩ*	23	23	23	μV
Unity Gain Crossover Frequency, f_T	$C_C = 0$	15	15	15	MHz
	C_C = 47 pF	4	4	4	
Slew Rate, SR: Open Loop	$C_C = 0$	30	30	30	V/μs
Closed Loop	C_C = 56 pF	10	10	10	
Transient Response: Rise Time, t_r	C_C = 56 pF, C_L = 25 pF, R_L = 2 kΩ (Voltage Follower)	0.09	0.09	0.09	μs
Overshoot		10	10	10	%
Settling Time (4 V_{p-p} Input to <0.1%)		1.2	1.2	1.2	μs

* Although a 1-MΩ source is used for this test, the equivalent input noise remains constant for values of R_S up to 10 MΩ.

CHARACTERISTIC	TEST CONDITIONS ($V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$ (Unless Otherwise Specified))	CA3130B (T,S)	CA3130A (T,S,E)	CA3130 (T,S,E)	UNITS
Input Offset Voltage, V_{IO}		1	2	8	mV
Input Offset Current, I_{IO}		0.1	0.1	0.1	pA
Input Current, I_I		2	2	2	pA
Common-Mode Rejection Ratio, CMRR		100	90	80	dB
Large-Signal Voltage Gain, A_{OL}	V_O = 4 V_{p-p}, R_L = 5 kΩ	100 k	100 k	100 k	V/V
		100	100	100	dB
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.8	0 to 2.8	0 to 2.8	V
Supply Current, I^+	V_O = 5 V, $R_L = \infty$	300	300	300	μA
	V_O = 2.5 V, $R_L = \infty$	500	500	500	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	200	μV/V

CA3130, CA3130A, CA3130B

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC
INPUT VOLTAGE... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK −
UP TO 55°C ..... 630 mW
ABOVE 55°C .... Derate linearly 6.67 mW/°C
WITH HEAT SINK −
UP TO 90°C ..... 1 W
ABOVE 90°C ... Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:
OPERATING (all types) ..... −55 to + 125°C
STORAGE (all types) ..... −65 to + 150°C
OUTPUT SHORT-CIRCUIT
DURATION* ..... INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH
(1.59 ± 0.79 mm) FROM CASE
FOR 10 SECONDS MAX. ..... +265°C

*Short circuit may be applied to ground or to either supply.

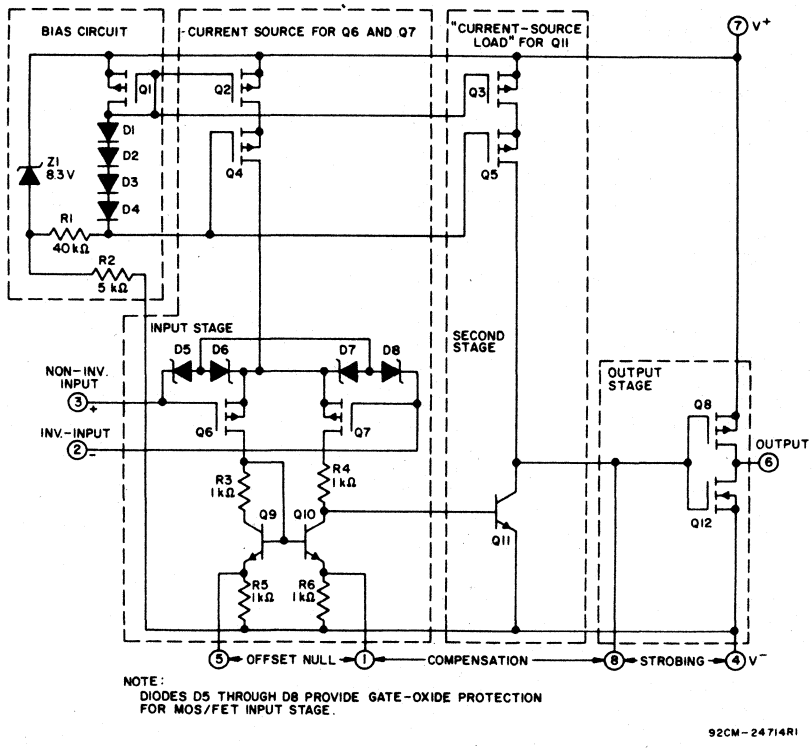


Fig. 2 – Schematic diagram of the CA3130 Series.

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3130 Series COS/MOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive COS/MOS digital circuits in comparator applications).

Input Stages—The circuit of the CA3130 is shown in Fig. 2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

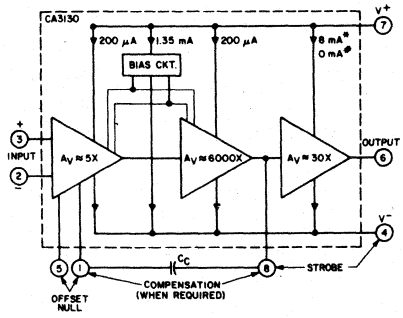
Second-Stage—Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit—At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes nonconductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage, Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage—The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are nonlinear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

†For general information on the characteristics of COS/MOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "COS/MOS Transistor Array".



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15 V
* WITH INPUT TERMINALS BIASED SO THAT TERM. 6 POTENTIAL IS +7.5 V ABOVE TERM. 4.
* WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.

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Fig. 3 – Block diagram of the CA3130 Series.

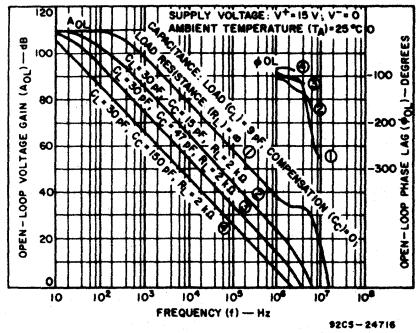

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Fig. 4 – Open-loop voltage gain and phase shift vs. frequency for various values of C_L, C_C, and R_L.

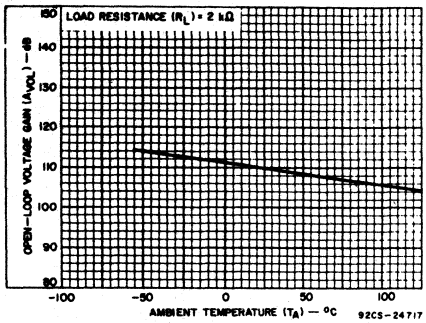


Fig. 5 – Open-loop gain vs. temperature.

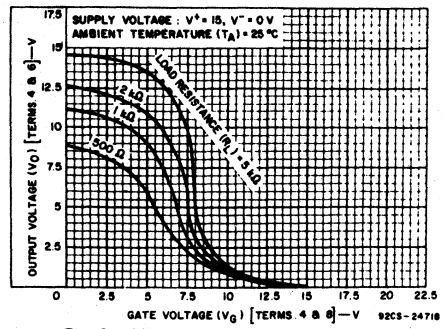


Fig. 6 – Voltage transfer characteristics of COS/MOS output stage.

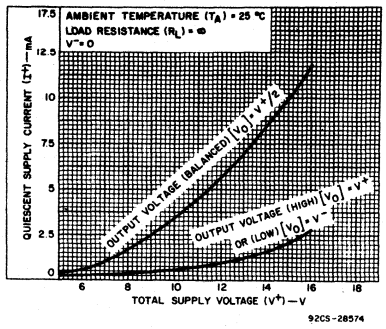


Fig. 7 – Quiescent supply current vs. supply voltage.

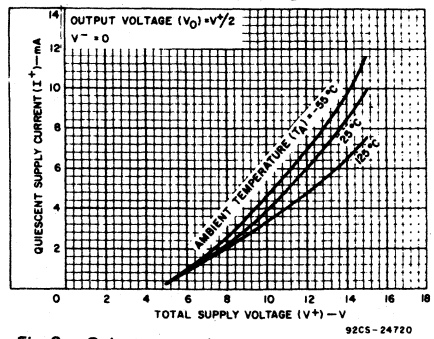


Fig. 8 – Quiescent supply current vs. supply voltage at several temperatures.

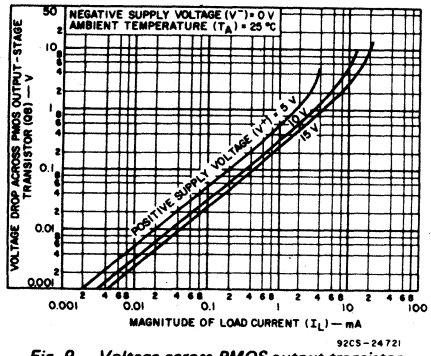


Fig. 9 – Voltage across PMOS output transistor (Q8) vs. load current.

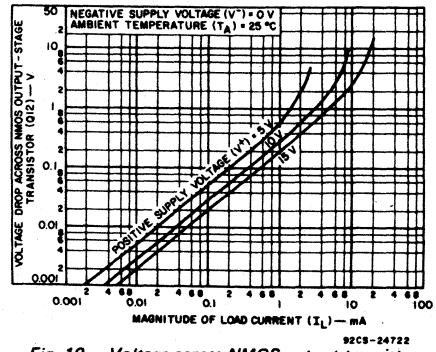


Fig. 10 – Voltage across NMOS output transistor (Q12) vs. load current.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3130 Series Op-Amps is typically 5 pA at T_A=25°C when terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig.11 contains data showing the variation of input current as a function of common-mode input voltage at T_A = 25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied

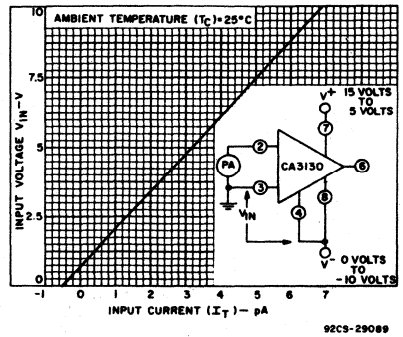


Fig.11 – Input current vs. common-mode voltage.

voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3130 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig.12 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

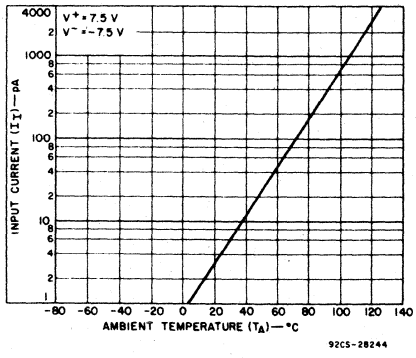


Fig.12 – Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terms. 2 and 3. Fig.13 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices (TO-5 package) during life testing. At lower temperatures (TO-5 and plastic), for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

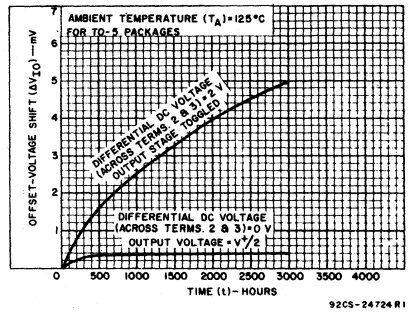


Fig.13 – Typical incremental offset-voltage shift vs. operating life.

Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 14a and 14b show the CA3130 connected for both dual- and single-supply operation.

Dual-supply operation: When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e.,

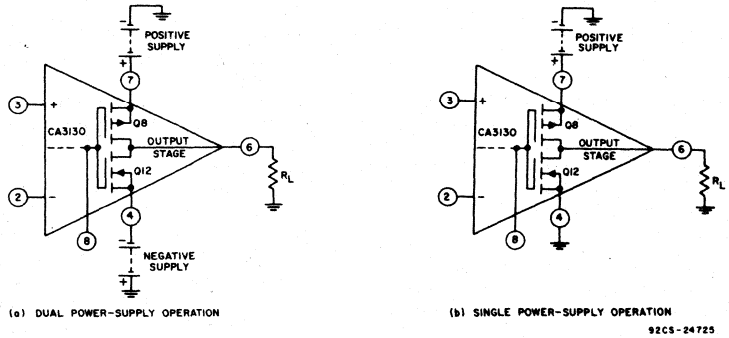


Fig.14 – CA3130 output stage in dual and single power-supply operation.

the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 14a shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L=\infty$, by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Fig.14b. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is a $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply-voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 23 μV when the test-circuit amplifier of Fig. 15 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

TYPICAL APPLICATIONS

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Fig. 16 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Fig. 17, together with related waveforms. This follower circuit is

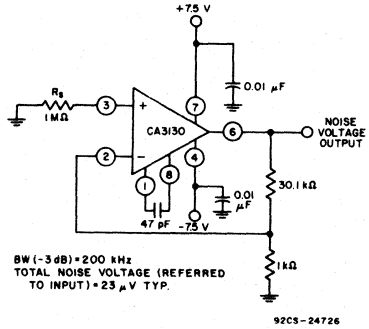
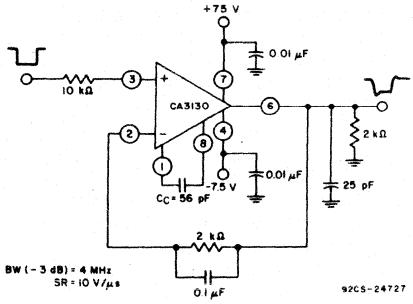
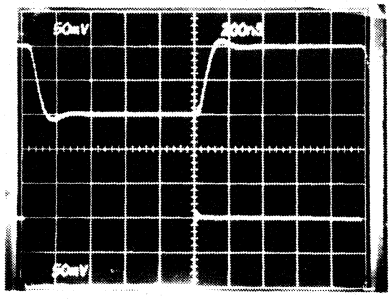
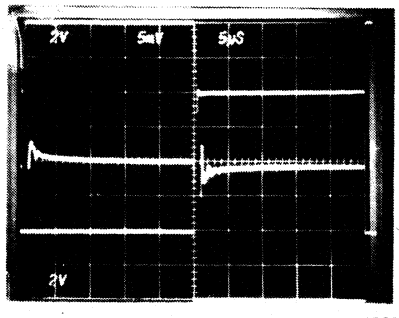


Fig.15 – Test-circuit amplifier (30-dB gain) used for wideband noise measurements.





Top Trace: Output
Bottom Trace: Input
(a) Small-signal response (50 mV/div. and 200 ns/div.)



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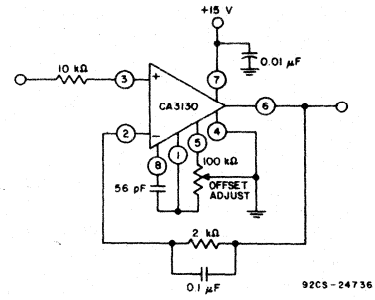
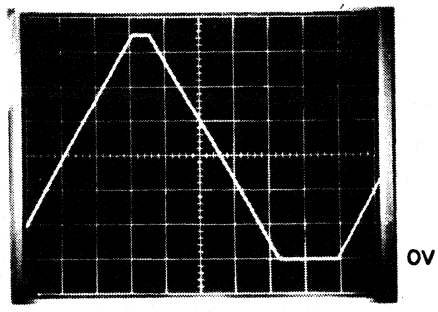
Top Trace: Output signal (2 V/div. and 5 μs/div.)
Center Trace: Difference signal (5 mV/div. and 5 μs/div.)
Bottom Trace: Input signal (2 V/div. and 5 μs/div.)
(b) Input-output difference signal showing settling time (Measurement made with Tektronix 7A13 differential amplifier)

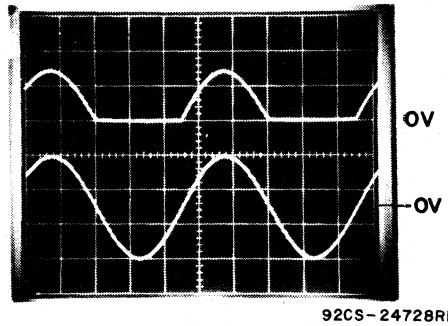
Fig. 16 – Split-supply voltage follower with associated waveforms.

linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 17a, with input-signal ramping. The waveforms in Fig. 17b show that the follower does not lose its input-to-output phase-sense, even though the input is





(a) Output-waveform with input-signal ramping (2 V/div. and 500 μs/div.)



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Top Trace: Output (5 V/div. and 200 μs/div.)
Bottom Trace: Input (5 V/div. and 200 μs/div.)
(b) Output-waveform with ground-reference sine-wave input

Fig. 17 – Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig. 9 in ICAN-6080).

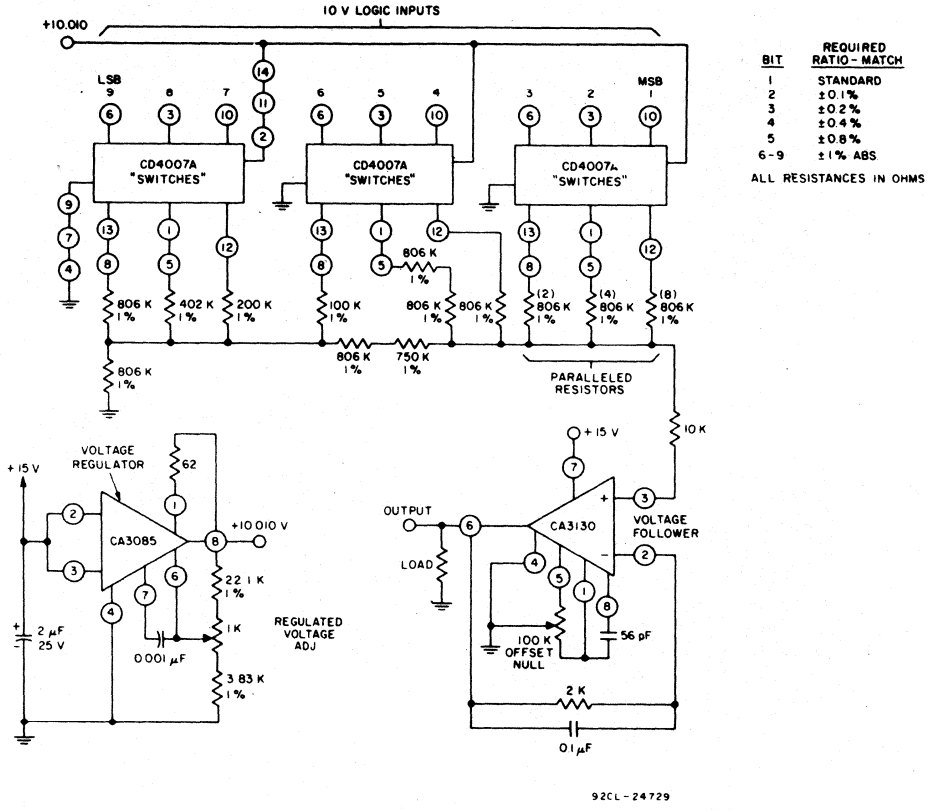
being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 17b also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.

9-Bit COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig.18 This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with COS/MOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig.18.

of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with varia-



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS

ALL RESISTANCES IN OHMS

Fig.18 – 9-bit DAC using COS/MOS digital switches and CA3130.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly

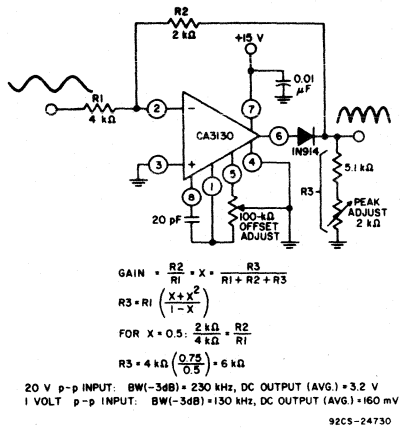
tions of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

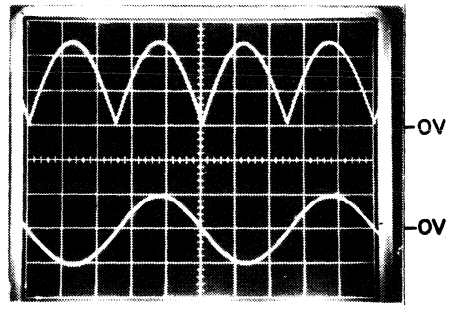
Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

The absolute-value circuit using the CA3130 is shown in Fig. 19. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a

*"Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC", Application Note ICAN-6080.

negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to −R2/R1. When the equality of the two equations shown in Fig. 19 is satisfied, the full-wave output is symmetrical.





Top Trace: Output signal (2 V/div.)
Bottom Trace: Input signal (10 V/div.)
Time base on both traces: 0.2 ms/div.

Fig. 19 — Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.

Peak Detectors

Peak-detector circuits are easily implemented with the CA3130, as illustrated in Fig. 20 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in an active "pull-down" mode so that the intrinsic capacitance can be discharged more expeditiously.

Error-Amplifier in Regulated-Power Supplies

The CA3130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero. Fig. 21 shows the schematic diagram of a 40-mA power supply capable of providing regulated output voltage by continuous adjustment over the range from 0 to 13 volts. Q3 and Q4 in IC2 (a CA3086 transistor-array IC) function as zeners to provide supply-voltage for the CA3130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier. Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q5 in IC3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R2.

Fig. 22 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous ad-

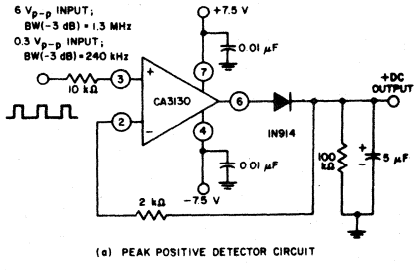


Fig. 20 — Peak-detector circuits.

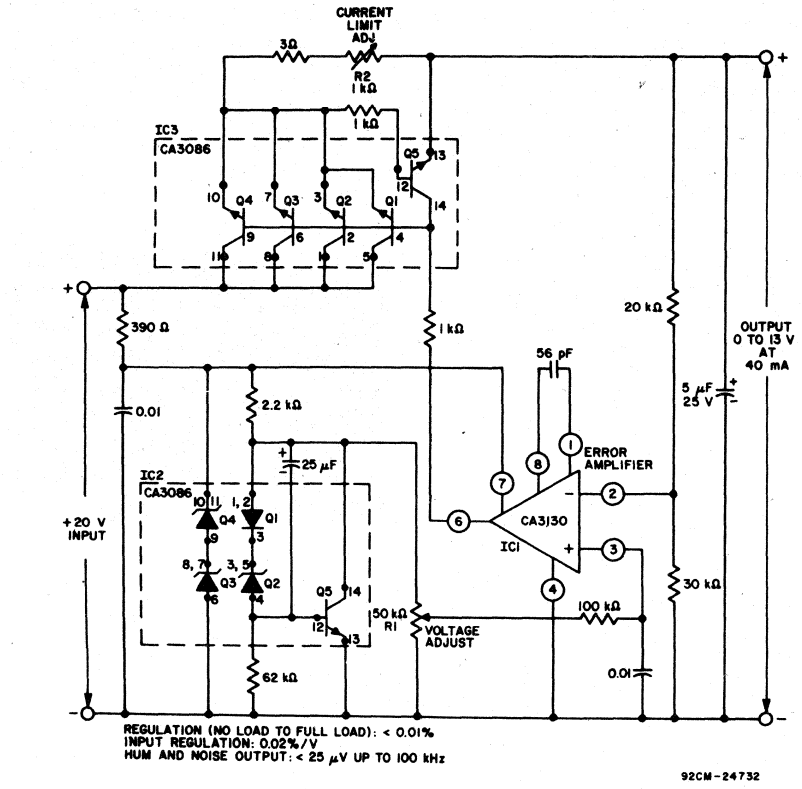


Fig.21 – Voltage regulator circuit (0 to 13 V at 40 ma).

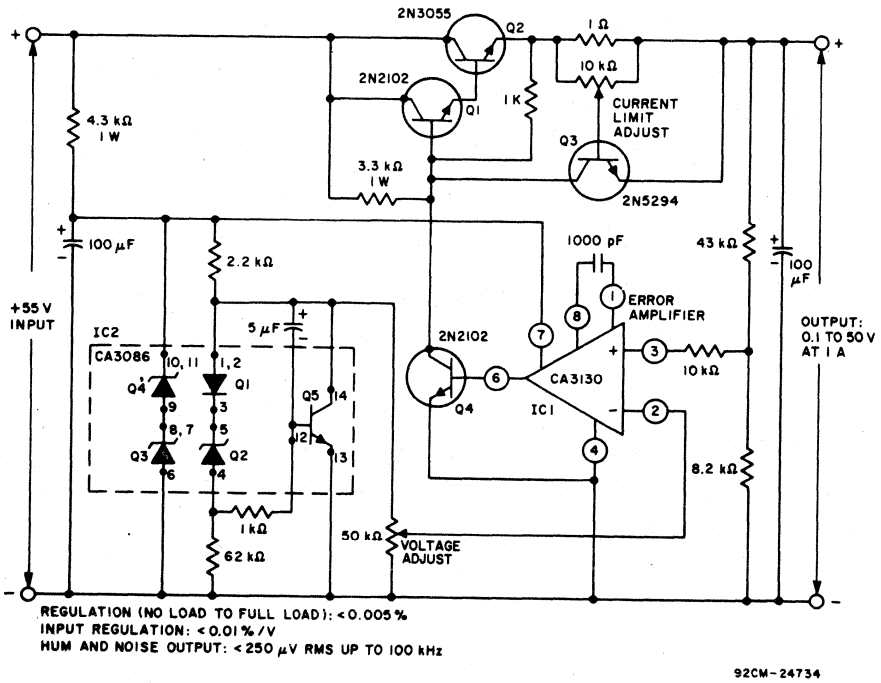


Fig.22 – Voltage regulator circuit (0.1 to 50 V at 1 A).

justment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Fig. 23. Resistors R1 and R2 are used to bias the CA3130 to the mid-point of the supply-voltage and R3 is the feedback resistor. The pulse repetition rate is selected by positioning S1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

Function Generator

Fig. 24 contains a schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)*, IC1, operated as a voltage-controlled current-source. The output, I_O, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA3130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

*See File No. 475 and ICAN-6668.

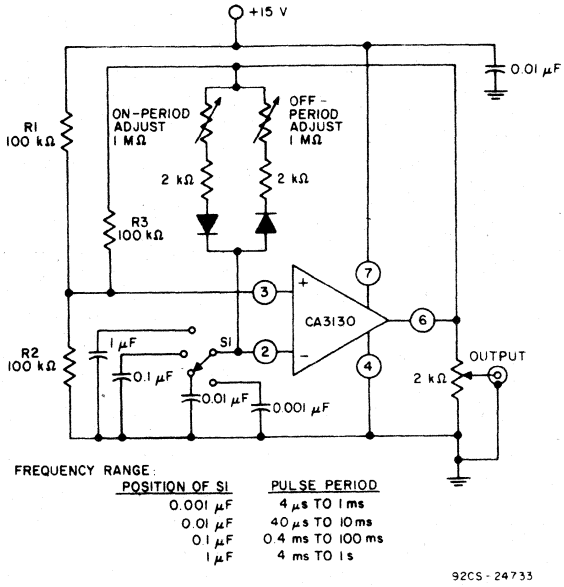


Fig.23 — Pulse generator (astable multivibrator) with provisions for independent control of "ON" and "OFF" periods.

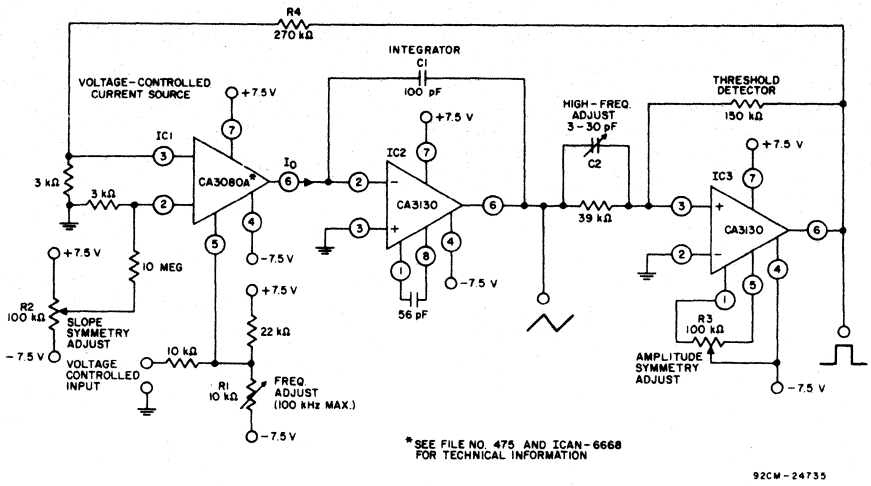


Fig. 24 — Function generator (frequency can be varied 1,000,000/1 with a single control).

Operation with Output-Stage Power-Booster

The current-sourcing and -sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 25, three COS/MOS transistor-pairs in a single CA3600E* IC array are shown parallel connected with the output stage in the CA3130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA3130 output stage by about 2.5X.

The amplifier circuit in Fig. 25 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (−3 dB) is 50 kHz.

*See File No. 619 for technical information.

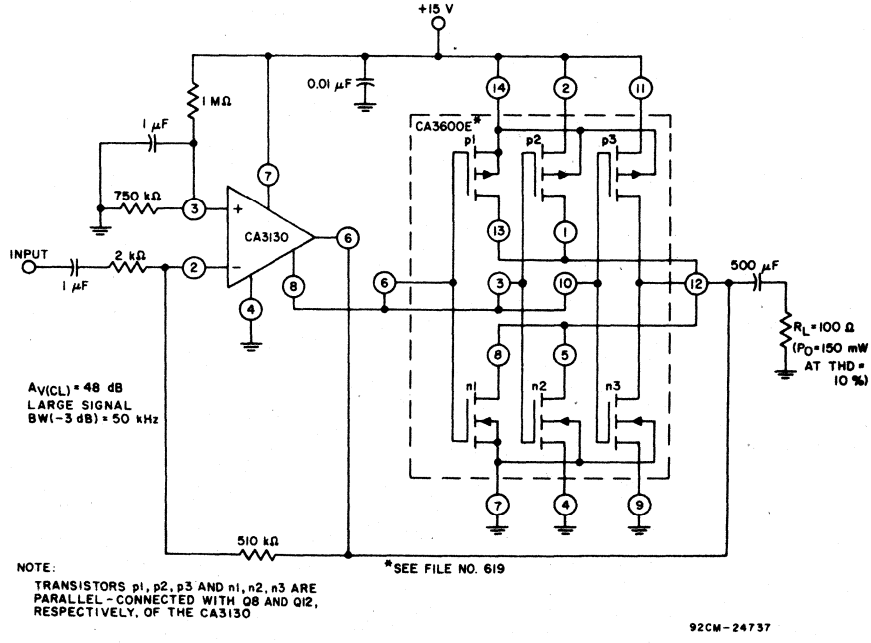
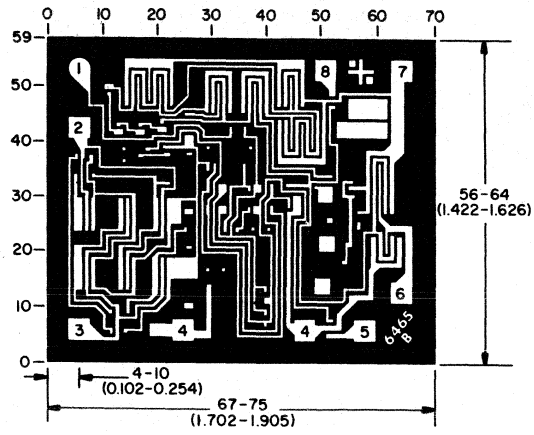


Fig. 25 — COS/MOS transistor array (CA3600E) connected as power-booster in the output stage of the CA3130.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and Pad Layout for CA3130H.

CA3140, CA3140A, CA3140B Types

BiMOS Operational Amplifiers

With MOS/FET Input/Bipolar Output

FEATURES:

- *MOS/FET Input Stage*
  - *(a) Very high input impedance (Z_{IN}) — 1.5 TΩ typ.*
  - *(b) Very low input current (I_I) — 10 pA typ. at ± 15 V*
  - *(c) Low input-offset voltage (V_{IO}) — to 2 mV max.*
  - *(d) Wide common-mode input-voltage range (V_{ICR})— can be swung 0.5 volt below negative supply-voltage rail*
  - *(e) Output swing complements input common-mode range*
  - *(f) Rugged input stage — bipolar diode protected*
- *Directly replaces industry type 741 in most applications*
- *Includes numerous industry operational amplifier categories such as general-purpose, FET input, wideband (high slew rate)*
- *Operation from 4-to-44 volts Single or Dual supplies*
- *Internally compensated*
- *Characterized for ± 15-volt operation and for TTL supply systems with operation down to 4 volts*
- *Wide bandwidth — 4.5 MHz unity gain at ± 15 V or 30 V; 3.7 MHz at 5 V*
- *High voltage-follower slew rate — 9 V/μs*
- *Fast setting time — 1.4 μs typ. to 10 mV with a 10-V_{p-p} signal*
- *Output swings to within 0.2 volt of negative supply*
- *Strobable output stage*

APPLICATIONS:

- *Ground-referenced single-supply amplifiers in automobile and portable instrumentation*
- *Sample and hold amplifiers*
- *Long-duration timers/multivibrators (microseconds—minutes—hours)*
- *Photocurrent instrumentation*
- *Peak detectors* ■ *Active filters*
- *Comparators*
- *Interface in 5 V TTL systems & other low-supply voltage systems*
- *All standard operational amplifier applications*
- *Function generators* ■ *Tone controls*
- *Power supplies* ■ *Portable instruments*
- *Intrusion alarm systems*

The CA3140B, CA3140A, and CA3140 are integrated-circuit operational amplifiers that combine the advantages of high-voltage PMOS transistors with high-voltage bipolar transistors on a single monolithic chip. Because of this unique combination of technologies, this device can now provide designers, for the first time, with the special performance features of the CA3130 COS/MOS operational amplifiers and the versatility of the 741 series of industry-standard operational amplifiers.

The CA3140, CA3140A, and CA3140 BiMOS operational amplifiers feature gate-protected MOS/FET (PMOS) transistors in the input circuit to provide very-high-input impedance, very-low-input current, and high-speed performance. The CA3140B operates at supply voltages from 4 to 44 volts; the CA3140A and CA3140 from 4 to 36 volts (either single or dual supply). These operational amplifiers are internally phase-compensated to achieve stable operation in unity-gain follower operation, and, additionally, have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset-voltage nulling. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load-terminal short-circuiting to either supply-rail or to ground.

The CA3140 Series has the same 8-lead terminal pin-out used for the "741" and other industry-standard operational amplifiers. They are supplied in either the standard 8-lead TO-5 style package (T suffix), or in the 8-lead dual-in-line formed-lead TO-5 style package "DIL-CAN" (S suffix). The CA3140 is available in chip form (H suffix). The CA3140A and CA3140 are also available in an 8-lead dual-in-line

plastic package (Mini-DIP-E suffix). The CA3140B is intended for operation at supply voltages ranging from 4 to 44 volts, for applications requiring premium-grade specifications. The CA3140A and CA3140 are for operation at supply voltages up to 36 volts (±18 volts). All types can be operated safely over the temperature range from -55°C to +125°C.

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS $V^+ = +15$ V, $V^- = -15$ V, $T_A = 25°C$	CA3140B (T,S)	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage Adjustment Resistor		Typ. Value of Resistor Between Term. 4 and 5 or 4 and 1 to Adjust Max. V_{IO}	43	18	4.7	kΩ
Input Resistance	R_I		1.5	1.5	1.5	TΩ
Input Capacitance	C_I		4	4	4	pF
Output Resistance	R_O		60	60	60	Ω
Equivalent Wideband Input Noise Voltage (See Fig. 39)	e_n	BW = 140 kHz, R_S = 1 MΩ	48	48	48	μV
Equivalent Input Noise Voltage (See Fig.10)	e_n	f = 1 kHz, R_S = 100 Ω	40	40	40	$nV/\sqrt{Hz}$
		f = 10 kHz, R_S = 100 Ω	12	12	12	$nV/\sqrt{Hz}$
Short-Circuit Current to Opposite Supply Source	I_{OM^+}		40	40	40	mA
Sink	I_{OM^-}		18	18	18	mA
Gain-Bandwidth Product, (See Figs. 5 &18)	f_T		4.5	4.5	4.5	MHz
Slew Rate, (See Fig.6)	SR		9	9	9	V/μs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low			220	220	220	μA
Transient Response: Rise Time	t_r	R_L = 2 kΩ, C_L = 100 pF	0.08	0.08	0.08	μs
Overshoot (See Fig. 37)	t_r	R_L = 2 kΩ, C_L = 100 pF	10	10	10	%
Settling Time at 10 V_{p-p}, (See Fig.17)	1 mV / 10 mV t_s	R_L = 2 kΩ, C_L = 100 pF, Voltage Follower	4.5	4.5	4.5	μs
	1 mV / 10 mV t_s	R_L = 2 kΩ, C_L = 100 pF, Voltage Follower	1.4	1.4	1.4	μs

CA3140, CA3140A, CA3140B Types

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At $V^+ = 15$ V, $V^- = 15$ V, $T_A = 25^oC$ Unless Otherwise Specified

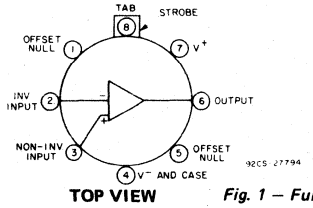
CHARACTERISTIC	LIMITS									UNITS
	CA3140B			CA3140A			CA3140			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	–	0.8	2	–	2	5	–	5	15	mV
Input Offset Current, $\|I_{IO}\|$	–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I	–	10	30	–	10	40	–	10	50	pA
Large-Signal Voltage Gain, A_{OL}● (See Figs. 4,18)	50 k	100 k	–	20 k	100 k	–	20 k	100 k	–	V/V
	94	100	–	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR (See Fig.9)	–	20	50	–	32	320	–	32	320	μV/V
	86	94	–	70	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR} (See Fig.20)	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	11	V
Power-Supply Rejection Ratio, PSRR $\Delta V_{IO}/\Delta V$ (See Fig.11)	–	32	100	–	100	150	–	100	150	μV/V
	80	90	–	76	80	–	76	80	–	dB
Max. Output Voltage■ V_{OM}^+ (See Figs.13,20) V_{OM}^-	+12	13	–	+12	13	–	+12	13	–	V
	−14	−14.4	–	−14	−14.4	–	−14	−14.4	–	
Supply Current, I^+ (See Fig.7)	–	4	6	–	4	6	–	4	6	mA
Device Dissipation, P_D	–	120	180	–	120	180	–	120	180	mW
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$	–	5	–	–	6	–	–	8	–	μV/°C
Max. Output Voltage,★ V_{OM}^+ V_{OM}^-	+19	+19.5	–	–	–	–	–	–	–	V
	−21	−21.4	–	–	–	–	–	–	–	
Large-Signal Voltage Gain, A_{OL}♦★	20 k	50 k	–	–	–	–	–	–	–	V/V
	86	94	–	–	–	–	–	–	–	dB

● At $V_O = 26V_{p\text{-}p}$, +12V, −14V and $R_L = 2\ k\Omega$.

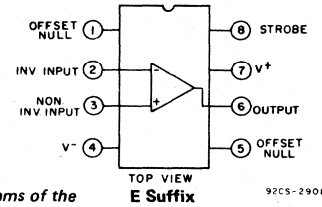
■ At $R_L = 2\ k\Omega$.

♦ At $V_O = +19$ V, −21 V, and $R_L = 2\ k\Omega$.

★ At $V^+ = 22$ V, $V^- = 22$ V.



TOP VIEW
S and T Suffixes



E Suffix

Fig. 1 – Functional diagrams of the CA3140 series.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3140, CA3140A	CA3140B
DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V	44 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±8 V	±8 V
COMMON-MODE DC INPUT VOLTAGE	(V^+ +8 V) to (V^- −0.5 V)	
INPUT-TERMINAL CURRENT	1 mA	
DEVICE DISSIPATION:		
WITHOUT HEAT SINK —		
UP TO 55°C	630 mW	
ABOVE 55°C	Derate linearly 6.67 mW/°C	
WITH HEAT SINK —		
Up to 55°C	1 W	
Above 55°C	Derate linearly 16.7 mW/°C	
TEMPERATURE RANGE:		
OPERATING (ALL TYPES)	−55 to + 125°C	
STORAGE (ALL TYPES)	−65 to +150°C	
OUTPUT SHORT-CIRCUIT DURATION*	INDEFINITE	
LEAD TEMPERATURE (DURING SOLDERING):		
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	+265°C	

* Short circuit may be applied to ground or to either supply.

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE

At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25°C$

CHARACTERISTIC		CA3140B (T,S)	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage	$\lvert V_{IO}\rvert$	0.8	2	5	mV
Input Offset Current	$\lvert I_{IO}\rvert$	0.1	0.1	0.1	pA
Input Current	I_I	2	2	2	pA
Input Resistance		1	1	1	TΩ
Large-Signal Voltage Gain (See Figs.4,18)	A_{OL}	100 k	100 k	100 k	V/V
		100	100	100	dB
Common-Mode Rejection Ratio,	CMRR	20	32	32	μV/V
		94	90	90	dB
Common-Mode Input-Voltage Range (See Fig.20)	V_{ICR}	−0.5	−0.5	−0.5	V
		2.6	2.6	2.6	
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$	32	100	100	μV/V
		90	80	80	dB
Maximum Output Voltage (See Figs.13,20)	V_{OM}^+	3	3	3	V
	V_{OM}^-	0.13	0.13	0.13	
Maximum Output Current: Source	I_{OM}^+	10	10	10	mA
Sink	I_{OM}^-	1	1	1	
Slew Rate (See Fig.6)		7	7	7	V/μs
Gain-Bandwidth Product (See Fig.5)	f_T	3.7	3.7	3.7	MHz
Supply Current (See Fig.7)	I^+	1.6	1.6	1.6	mA
Device Dissipation	P_D	8	8	8	mW
Sink Current from Term. 8 to Term. 4 to Swing Output Low		200	200	200	μA

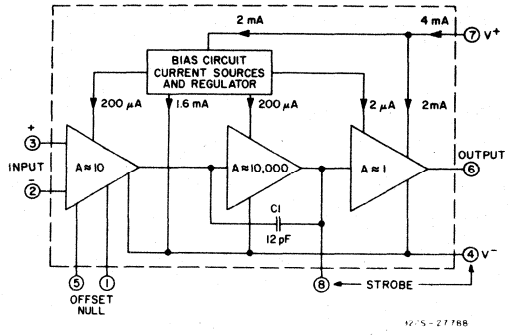


Fig.2 – Block diagram of CA3140 series.

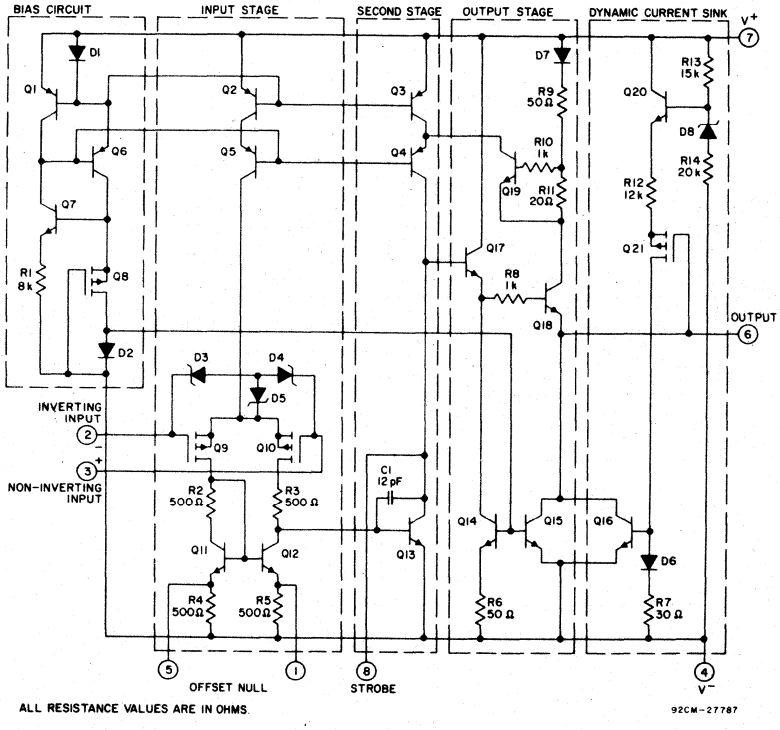


Fig.3 – Schematic diagram of CA3140 series.

CIRCUIT DESCRIPTION

Fig.2 is a block diagram of the CA3140 Series PMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant-current flow circuits in the first and second stages. The CA3140 includes an on-chip phase-compensating capacitor that is sufficient for the unity gain voltage-follower configuration.

Input Stages – The schematic circuit diagram of the CA3140 is shown in Fig.3. It consists of a differential-input stage using PMOS field-effect transistors (Q9, Q10) working into a mirror pair of bipolar transistors (Q11, Q12) functioning as load resistors together with resistors R2 through R5. The mirror-pair transistors also function as a differen-

tial-to-single-ended converter to provide base-current drive to the second-stage bipolar transistor (Q13). Offset nulling, when desired, can be effected with a 10-kΩ potentiometer connected across terminals 1 and 5 and with its slider arm connected to terminal 4. Cascode-connected bipolar transistors Q2, Q5 are the constant-current source for the input stage. The base-biasing circuit for the constant-current source is described subsequently. The small diodes D3, D4, D5 provide gate-oxide protection against high-voltage transients, e.g., static electricity.

Second Stage — Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q13 and its cascode-connected load resistance provided by bipolar transistors Q3, Q4. On-chip phase compensation, sufficient for a majority of the applications is provided by C1. Additional Miller-Effect compensation (roll-off) can be accomplished, when desired, by simply connecting a small capacitor between terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (terminal 4) by mechanical or electrical means, the output terminal 6 swings low, i.e., approximately to terminal 4 potential.

Output Stage — The CA3140 Series circuits employ a broadband output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q17, Q18) is established by transistors (Q14, Q15) whose base-currents are "mirrored" to current flowing through diode D2 in the bias circuit section. When the CA3140 is operating such that output terminal 6 is sourcing current, transistor Q18 functions as an emitter-follower to source current from the V+ bus (terminal 7), via D7, R9, and R11. Under these conditions, the collector potential of Q13 is sufficiently high to permit the necessary flow of base current to emitter follower Q17 which, in turn, drives Q18.

When the CA3140 is operating such that output terminal 6 is sinking current to the V− bus, transistor Q16 is the current-sinking element. Transistor Q16 is mirror-connected to D6, R7, with current fed by way of Q21, R12, and Q20. Transistor Q20, in turn, is biased by current-flow through R13, zener D8, and R14. The dynamic current-sink is controlled by voltage-level sensing. For purposes of explanation, it is assumed that output terminal 6 is quiescently established at the potential mid-point between the V+ and V− supply rails. When output-current sinking-mode operation is required, the collector potential of transistor Q13 is driven below its quiescent level, thereby causing Q17, Q18 to decrease the output voltage at terminal 6. Thus, the gate terminal of PMOS transistor Q21 is displaced toward the V− bus, thereby reducing the channel resistance of Q21. As a consequence, there is an incremental increase in current flow through Q20, R12, Q21, D6, R7, and the base of Q16. As a result, Q16 sinks current from terminal 6 in direct response to the incremental change in output voltage caused by Q18. This sink current flows regardless of load; any excess current is internally supplied by the emitter-follower Q18. Short-circuit protection of the output circuit is provided by Q19, which is driven into conduction by the high voltage drop developed across R11 under output short-circuit conditions. Under these conditions, the collector of Q19 diverts current from Q4 so as to reduce the base-current drive from Q17, thereby limiting current flow in Q18 to the short-circuited load terminal.

Bias Circuit — Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R1. The function of the bias circuit is to establish and maintain constant-current flow through D1, Q6, Q8 and D2. D1 is a diode-connected transistor mirror-connected in parallel with the base-emitter junctions of Q1, Q2, and Q3. D1 may be considered as a current-sampling diode that senses the emitter current of Q6 and automatically adjusts the base current of Q6 (via Q1) to maintain a constant current through Q6, Q8, D2. The base-currents in Q2, Q3 are also determined by constant-current flow D1. Furthermore, current in diode-connected transistor D2 establishes the currents in transistors Q14 and Q15.

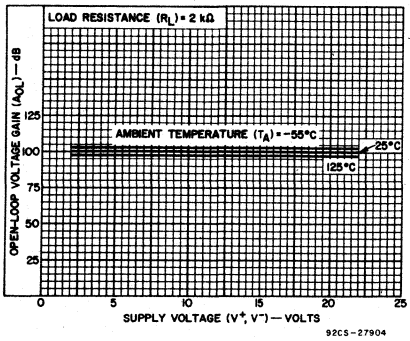


Fig.4 — Open-loop voltage gain vs supply voltage and temperature.

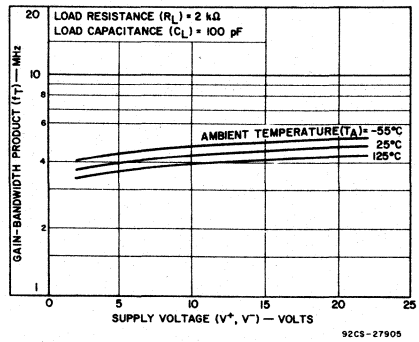


Fig.5 — Gain-bandwidth product vs supply voltage and temperature.

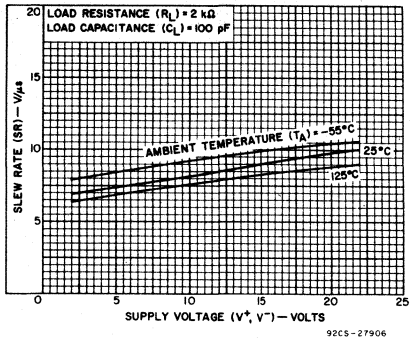


Fig.6 — Slew rate vs supply voltage andtemperature.

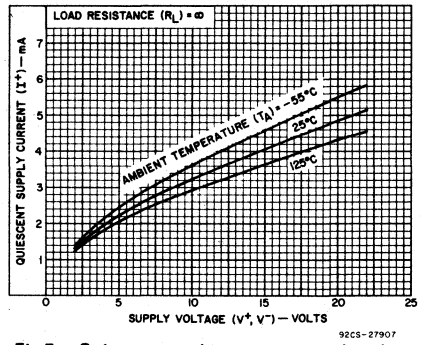


Fig.7 — Quiescent supply current vs supply voltage and temperature.

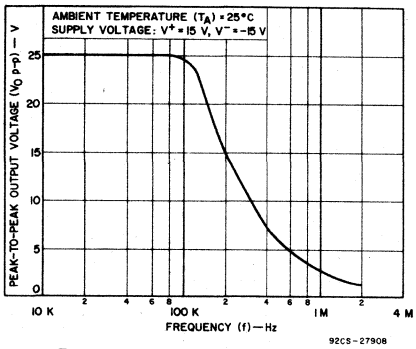


Fig.8 — Maximum output voltage swing vs frequency.

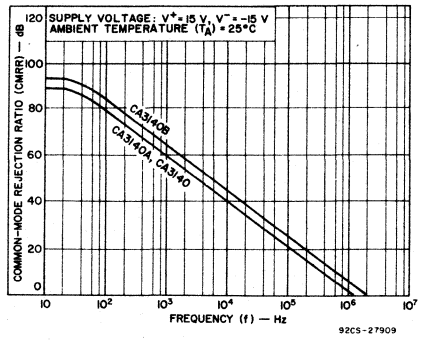


Fig.9 — Common-mode rejection ratio vs frequency.

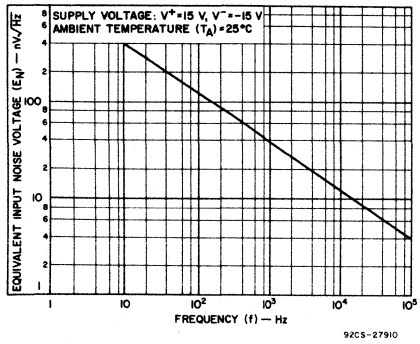


Fig.10 — Equivalent input noise voltage vs frequency.

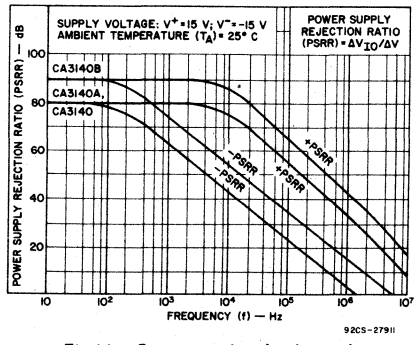


Fig.11 — Power supply rejection ratio vs frequency.

APPLICATIONS CONSIDERATIONS

Wide dynamic range of input and output characteristics with the most desirable high input-impedance characteristic is achieved in the CA3140 by the use of an unique design based upon the PMOS-Bipolar process. Input-common-mode voltage range and output-swing capabilities are complementary, allowing operation with the single supply down to four volts.

The wide dynamic range of these parameters also means that this device is suitable for many single-supply applications, such as, for example, where one input is driven below the potential of terminal 4 and the phase sense of the output signal must be maintained — a most important consideration in comparator applications.

OUTPUT CIRCUIT CONSIDERATIONS

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2-volt zener diode connected to terminal 8 as shown in Fig.12. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the CA3140. These voltages are independent of the operating supply voltage.

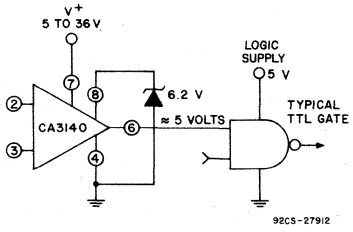


Fig.12 — Zener clamping diode connected to terminals 8 and 4 to limit CA3140 output swing to TTL levels.

Fig.13 shows output current-sinking capabilities of the CA3140 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

Fig.16 show some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

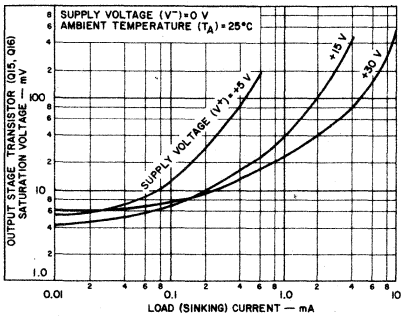


Fig.13 — Voltage across output transistors Q15 and Q16 vs load current.

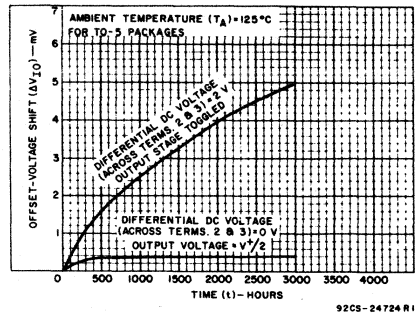


Fig.14 — Typical incremental offset-voltage shift vs operating life.

OFFSET-VOLTAGE NULLING

The input-offset voltage can be nulled by connecting a 10-kΩ potentiometer between terminals 1 and 5 and returning its wiper arm to terminal 4, see Fig.15a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig.15b, to optimize its utilization range are given in the table "Typical Electrical Characteristics" shown in this bulletin.

An alternate system is shown in Fig.15c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

LOW-VOLTAGE OPERATION

Operation at total supply voltages as low as 4 volts is possible with the CA3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low-voltage limitation occurs when the upper extreme of the input common-mode voltage range extends down to the voltage at terminal 4. This limit is reached at a total

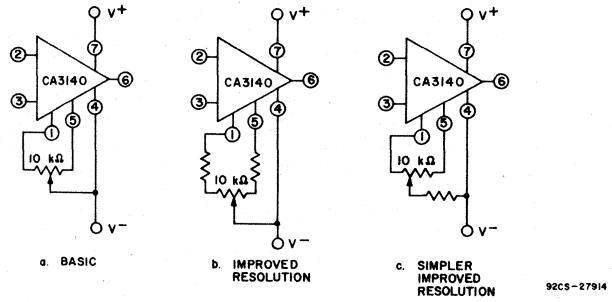
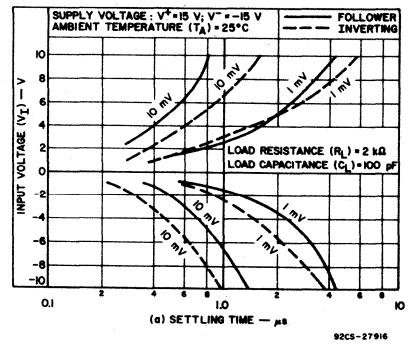


Fig.15 – Three offset-voltage nulling methods.

supply voltage just below 4 volts. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Fig.20 shows these characteristics and shows that with 2-volt dual supplies, the lower extreme of the input common-mode voltage range is below ground potential.



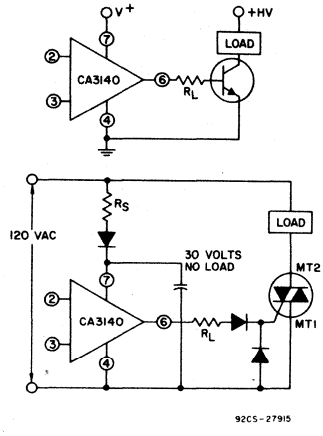
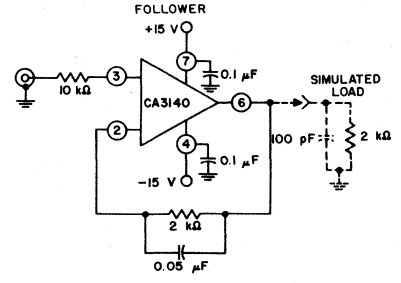


Fig.16 – Methods of utilizing the $V_{CE(sat)}$ sinking-current capability of the CA3140 series.



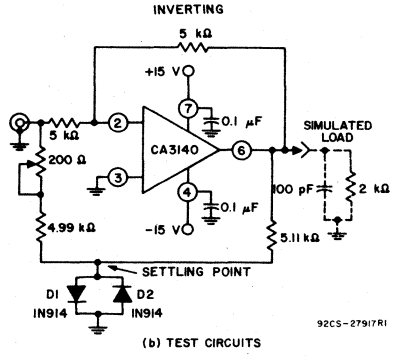


Fig.17 – Input voltage vs settling time.

BANDWIDTH AND SLEW RATE

For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between terminals 1 and 8 can reduce the open-loop −3 dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Fig.17 shows the typical settling time required to reach 1 mV or 10 mV of the final value for various levels of large signal inputs for the voltage-follower and inverting unity-gain amplifiers. The exceptionally fast setting time characteristics are largely due to the high combination of high gain and wide bandwidth of the CA3140; as shown in Fig. 18.

INPUT CIRCUIT CONSIDERATIONS

As mentioned previously, the amplifier inputs can be driven below the terminal 4 potential, but a series current-limiting re-

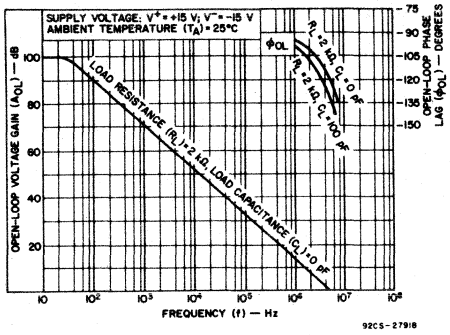


Fig.18 — Open-loop voltage gain and phase lag vs frequency.

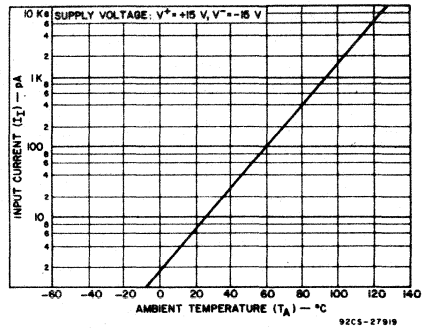


Fig.19 — Input current vs ambient temperature.

sistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3140 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig.19 shows typical input-terminal current versus ambient temperature for the CA3140.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Fig.14 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of 125°C (for TO-5); at lower temperatures (TO-5 and plastic), for example, at 85°C, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetircal, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar a transistor input stage.

SUPER SWEEP FUNCTION GENERATOR

A function generator having a wide tuning range is shown in Fig.21. The 1,000,000/1

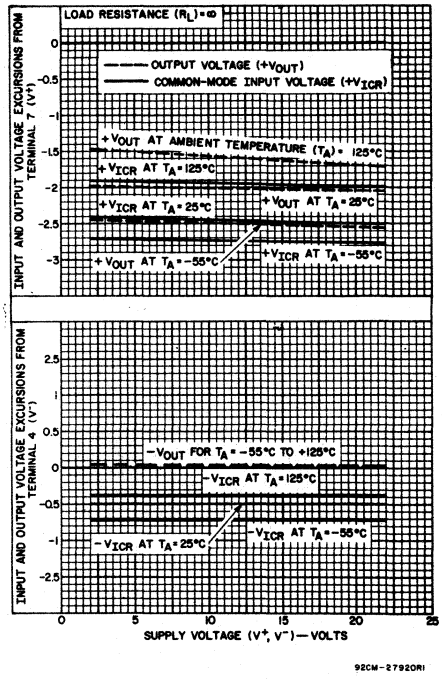


Fig.20 — Output-voltage-swing capability and common-mode input-voltage range vs supply voltage and temperature.

adjustment range is accomplished by a single variable potentiometer or by an auxiliary sweeping signal. The CA3140 functions as a non-inverting read-out amplifier of the triangular signal developed across the integrating capacitor network connected to the output of the CA3080A current source.

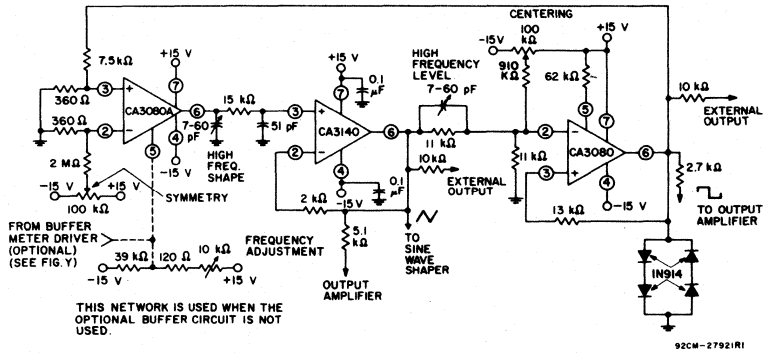
Buffered triangular output signals are then applied to a second CA3080 functioning as a high-speed hysteresis switch. Output from the switch is returned directly back to the

input of the CA3080A current source, thereby, completing the positive feedback loop.

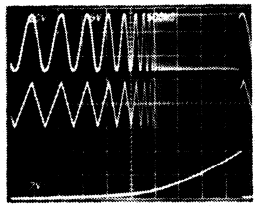
The triangular output level is determined by the four 1N914 level-limiting diodes of the second CA3080 and the resistor-divider network connected to terminal No.2 (input) of the CA3080. These diodes establish the input trip level to this switching stage and, therefore, indirectly determine the amplitude of the output triangle.

Compensation for propagation delays around the entire loop is provided by one adjustment on the input of the CA3080. This adjustment, which provides for a constant generator amplitude output, is most easily made while the generator is sweeping. High-frequency ramp linearity is adjusted by the single 7-to-60 pF capacitor in the output of the CA3080A.

It must be emphasized that only the CA-3080A is characterized for maximum output linearity in the current-generator function.



(a) Circuit



TOP TRACE: OUTPUT AT JUNCTION OF 2.7 Ω AND 51 Ω RESISTORS 5 V/DIV AND 500 ms/DIV
CENTER TRACE: EXTERNAL OUTPUT OF TRIANGULAR FUNCTION GENERATOR 2 V/DIV AND 500 ms/DIV
BOTTOM TRACE: OUTPUT OF "LOG" GENERATOR 10 V/DIV AND 500 ms/DIV

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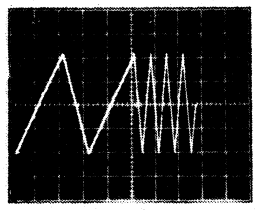
(b1) Function generator sweeping



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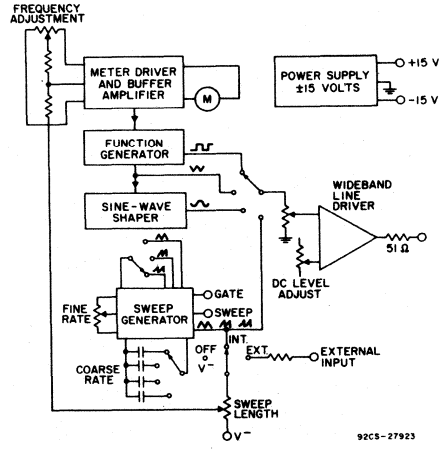
(b2) Function generator with fixed frequencies



(c) Interconnections

1V/DIV and 1 sec/DIV

Three tone test signals, highest frequency ⩾ 0.5 MHz. Note the slight assymmetry at the three-second/cycle signal. This assymmetry is due to slightly different positive and negative integration from the CA3080A and from the pc board and component leakages at the 100-pA level.

Fig.21 – Function generator.

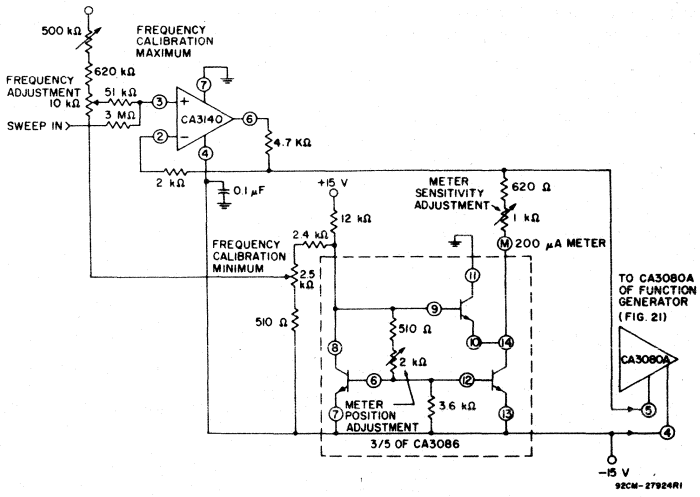


Fig. 22 – Meter driver and buffer amplifier.

METER DRIVER AND BUFFER AMPLIFIER

Fig. 22 shows the CA3140 connected as a meter driver and buffer amplifier. Low driving impedance is required of the CA-3080A current source to assure smooth operation of the Frequency Adjustment Control. This low-driving impedance requirement is easily met by using a CA3140 connected as a voltage follower. Moreover, a meter may be placed across the input to the CA3080A to give a logarithmic analog indication of the function generators frequency.

Analog frequency readout is readily accomplished by the means described above because the output current of the CA3080A varies approximately one decade for each 60-mV change in the applied voltage, V_{ABC} (voltage between terminals 5 and 4 of the CA3080A of the function generator). Therefore, six decades represent 360-mV change in V_{ABC}.

Now, only the reference voltage must be established to set the lower limit on the meter. The three remaining transistors from the CA3086 Array used in the sweep generator are used for this reference voltage. In addition, this reference generator arrangement tends to track ambient temperature variations, and thus compensates for the effects of the normal negative temperature coefficient of the CA3080A V_{ABC} terminal voltage.

Another output voltage from the reference generator is used to insure temperature tracking of the lower end of the Frequency Adjustment Potentiometer. A large series resistance simulates a current source, assuring similar temperature coefficients at both ends of the Frequency Adjustment Control.

To calibrate this circuit, set the Frequency Adjustment Potentiometer at its low end. Then adjust the Minimum Frequency Calibration Control for the lowest frequency. To establish the upper frequency limit, set the Frequency Adjustment Potentiometer to its upper end and then adjust the Maximum Frequency Calibration Control for the maximum frequency. Because there is interaction among these controls, repetition of the adjustment procedure may be necesary.

Two adjustments are used for the meter. The meter sensitivity control sets the meter-scale width of each decade, while the meter position control adjusts the pointer on the scale with negligible effect on the sensitivity adjustment. Thus, the meter sensitivity adjustment control calibrates the meter so that it deflects 1/6 of full scale for each decade change in frequency.

SINE-WAVE SHAPER

The circuit shown in Fig. 23 uses a CA3140 as a voltage follower in combination with diodes from the CA3019 Array to convert the triangular signal from the function generator to a sine-wave output signal having typically less than 2% THD. The basic zero-crossing slope is established by the 10-kΩ potentiometer connected between terminals 2 and 6 of the CA3140 and the 9.1-kΩ resistor and 10-kΩ potentiometer from terminal 2 to ground. Two break points are established by diodes D_1 through D_4. Positive feedback via D_5 and D_6 establishes the zero slope at the maximum and minimum levels of the sine wave. This technique is necessary because the voltage-follower configuration approaches unity gain rather than the zero gain required to shape the sine wave at the two extremes.

CA3140, CA3140A, CA3140B Types

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine-wave generator. The initial slope is adjusted with the potentiometer R_1, followed by an adjustment of R_2. The final slope is established by adjusting R_3, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessarv

SWEEPING GENERATOR

Fig. 24 shows a sweeping generator. Three CA3140's are used in this circuit. One CA3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third CA3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

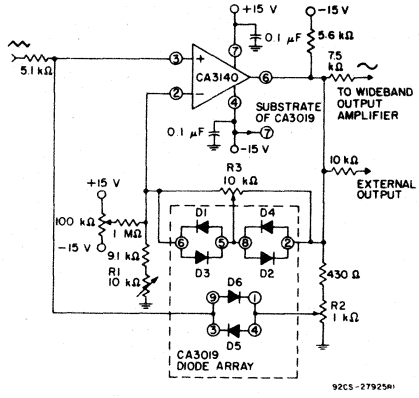


Fig. 23 – Sine-wave shaper.

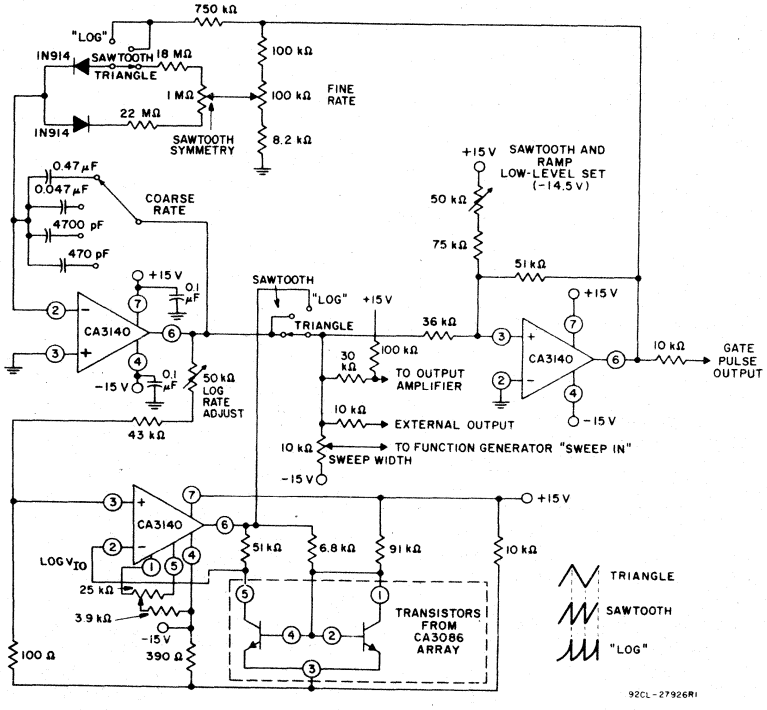


Fig. 24 – Sweeping generator.

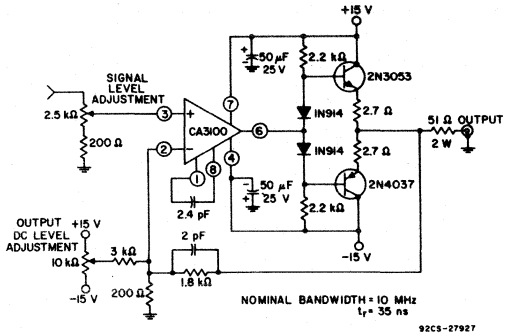


Fig. 25 – Wideband output amplifier.

WIDEBAND OUTPUT AMPLIFIER

Fig. 25 shows a high-slew-rate, wideband amplifier suitable for use as a 50-ohm transmission-line driver. This circuit, when used in conjunction with the function generator and sine-wave shaper circuits shown in Figs. 21 and 23 provides 18 volts peak-to-peak output open-circuited, or 9 volts peak-to-peak output when terminated in 50 ohms. The slew rate required of this amplifier is 28 volts/μs (18 volts peak-to-peak x π x 0.5 MHz).

POWER SUPPLIES

High input-impedance, common-mode capability down to the negative supply and high output-drive current capability are key factors in the design of wide-range output-voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0 to 24 volts.

Unlike many regulator systems using comparators having a bipolar transistor-input stage, a high-impedance reference-voltage divider from a single supply can be used in connection with the CA3140 (see Fig. 26).

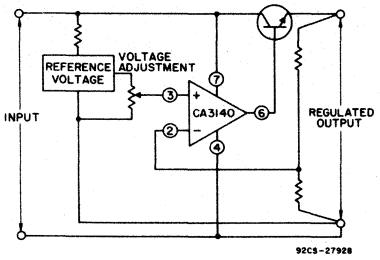


Fig. 26 – Basic single-supply voltage regulator showing voltage-follower configuration.

Essentially, the regulators, shown in Figs. 27 and 28, are connected as non-inverting power operational amplifiers with a gain of 3.2. An 8-volt reference input yields a maximum output voltage slightly greater than 25 volts. As a voltage follower, when the reference input goes to 0 volts the output will be 0 volts. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high I_{CBO} levels will also prevent the output voltage from reaching zero because there is a finite voltage drop (V_{CE}sat) across the output of the CA3140 (see Fig.13). This saturation voltage level may indeed set the lowest voltage obtainable.

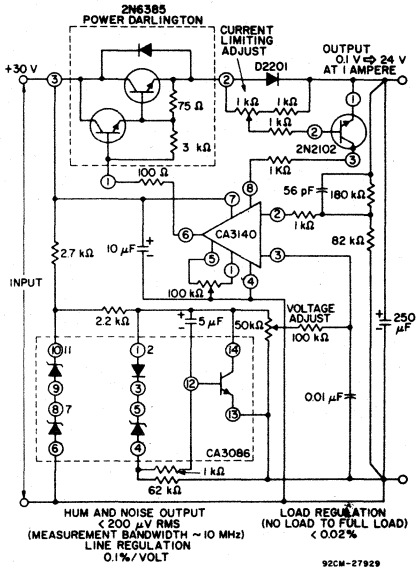


Fig. 27 – Regulated power supply.

The high impedance presented by terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the CA3140 in the event of unusual input or output transients on the supply-rail.

Figs. 27 and 28, show circuits in which a D2201 high-speed diode is used for the current sensor. This diode was chosen for its slightly higher forward-voltage drop characteristic thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1 ampere at 1 volt forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small-signal reference amplifier in the proximity of the current-sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode. In spite of those limitations, the current limiting point can easily be adjusted over the range from 10 mA to 1 ampere with a single adjustment potentiometer. If the temperature stability of the current-limiting system is a serious consideration, the more usual current-sampling resistor-type of circuitry should be employed.

A power Darlington transistor (in a heat sink TO-3 case), is used as the series-pass element for the conventional current-limiting system, Fig. 27, because high-power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat-sink VERSAWATT transistor is used as the series-pass element in the foldback current system, Fig.28, since dissipation levels will only approach 10 watts. In this system, the D2201 diode is used for current sampling. Foldback is provided by the 3 kΩ and 100 kΩ divider network connected to the base of the current-sensing transistor.

Both regulators, Figs. 27 and 28, provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200 μV as read with a meter having a 10-MHz bandwidth.

Fig.31 (a) shows the turn ON and turn OFF characteristics of both regulators. The slow turn-on rise is due to the slow rate of rise of the reference voltage. Fig. 29 (b) shows the transient response of the regulator with the switching of a 20-Ω load at 20 volts output.

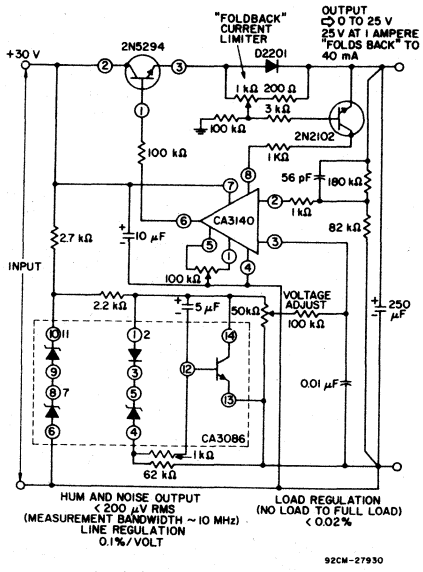
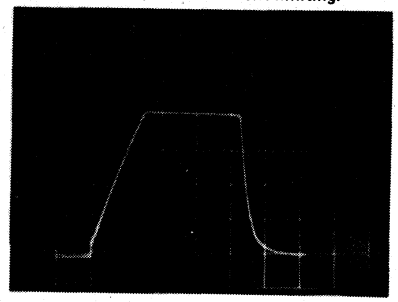
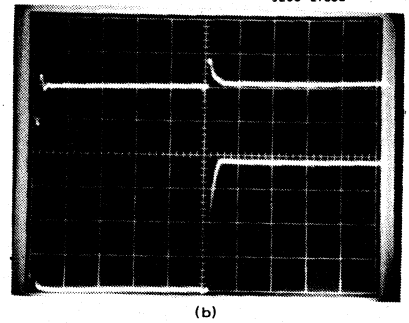


Fig. 28 – Regulated power supply with "foldback" current limiting.



(a)

SUPPLY TURN-ON AND TURN-OFF CHARACTERISTICS
(5 VOLTS / DIV. AND 1 s/DIV.)
92CS-27882



(b)

TRANSIENT RESPONSE
TOP TRACE : OUTPUT VOLTAGE
(200 mV/DIV AND 5 μs/DIV)
BOTTOM TRACE : COLLECTOR OF LOAD SWITCHING TRANSISTOR,
LOAD = 1 AMPERE
(5 VOLTS/DIV AND 5 μs/DIV)
92CS-27881

Fig. 29 – Waveforms of dynamic characteristics of power supply currents shown in Figs. 29 and 30.

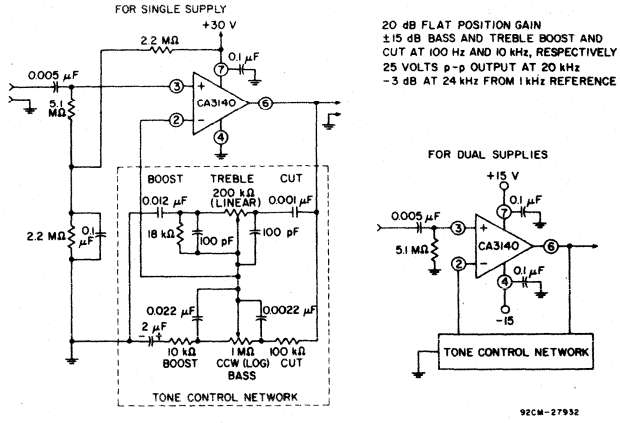


Fig. 30 – Tone control circuit using CA3130 series (20-dB midband gain).

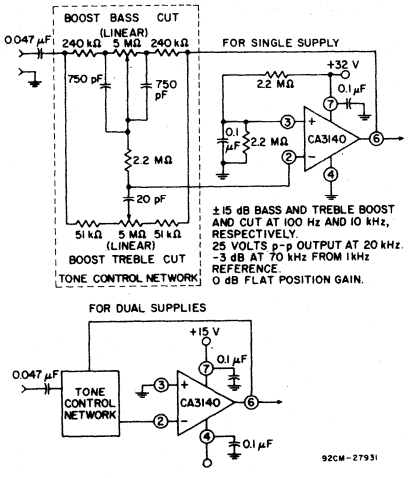


Fig. 31 – Baxandall tone control circuit using CA3140 series.

TONE CONTROL CIRCUITS

High-slew-rate, wide-bandwidth, high-output voltage capability and high input impedance are all characteristics required of tone-control amplifiers. Two tone control circuits that exploit these characteristics of the CA3140 are shown in Figs. 30 and 31.

The first circuit, shown in Fig. 31, is the Baxandall tone-control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the CA3140 makes possible the use of low-cost, low-value, small-size capacitors, as well as reduced load of the driving stage.

Bass treble boost and cut are ± 15 dB at 100 Hz and 10 kHz, respectively. Full peak-to-peak output is available up to at least 20 kHz due to the high slew rate of the CA3140. The amplifier gain is –3 dB down from its "flat" position at 70 kHz.

Fig. 30 shows another tone-control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20-dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from terminal No.3 to ground. A detailed analysis of this circuit is given in "An IC Operational Transconductance Amplifier (OTA) With Power Capability" by L, Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No.3, August, 1972.

WIEN BRIDGE OSCILLATOR

Another application of the CA3140 that makes excellent use of its high input-impedance, high-slew-rate, and high-voltage qualities is the Wien Bridge sine-wave oscillator. A basic Wien Bridge oscillator is shown in Fig. 32. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency equation reduces to the familiar $f = 1/2\pi RC$ and the gain required for oscillation, A_{OSC} is equal to 3. Note that if C_2 is increased by a factor of four and R_2 is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus per-

mitting a potentially higher operating frequency closer to the gain-bandwidth product of the CA3140.

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, R_S, is commonly replaced with some variable resistance element. Thus, through some control means, the value of R_S is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance is made to increase as the output amplitude is increased are a few of the elements often utilized.

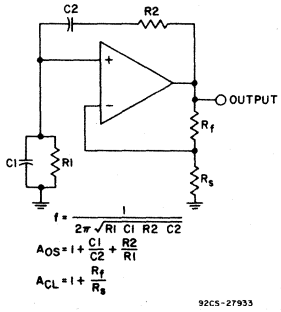


Fig. 32 – Basic Wien bridge oscillator circuit using an operational amplifier.

Fig. 33 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor (R_f of Fig. 32). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1-μF polycarbonate capacitors and 22 MΩ for the frequency determining network, the operating frequency is 0.007 Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of 180 kHz will reach a slew rate of approximately 9 volts/μs when its amplitude is 16 volts peak-to-peak.

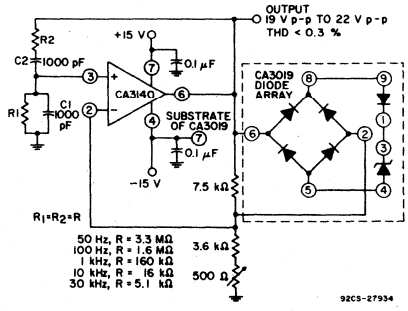


Fig. 33 – Wien bridge oscillator circuit using CA3140 series.

SIMPLE SAMPLE-AND-HOLD SYSTEM

Fig. 34 shows a very simple sample-and-hold system using the CA3140 as the readout amplifier for the storage capacitor. The CA3080A serves as both input buffer amplifier and low feed-through transmission switch.* System offset nulling is accomplished with the CA3140 via its offset nulling terminals. A typical simulated load of 2 kΩ and 30 pF is shown in the schematic.

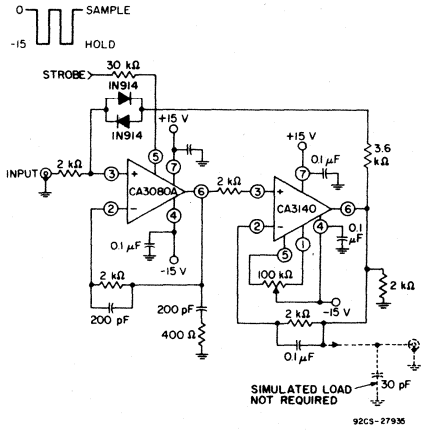
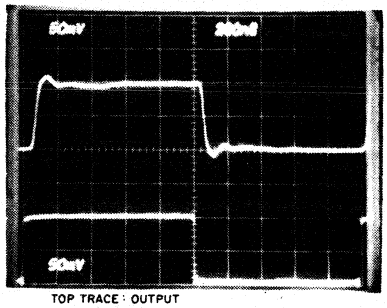


Fig. 34 – Sample- and hold circuit.

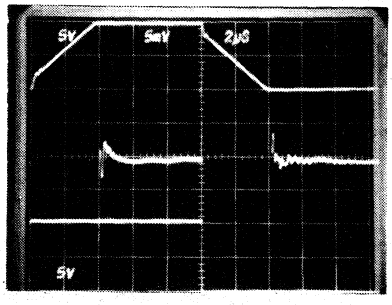
In this circuit, the storage compensation capacitance (C_1) is only 200 pF. Larger value capacitors provide longer "hold" periods but with slower slew rates. The slew rate $\frac{dv}{dt} = \frac{i}{c} = 0.5$ mA/200 pF = 2.5 V/μs.

* ICAN-6668 "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

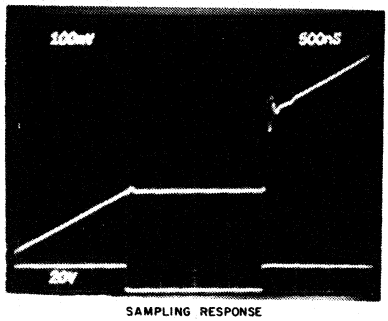
Pulse "droop" during the hold interval is 170 pA/200 pF which is = 0.85 μV/μs; (i.e., 170 pA/200 pF). In this case, 170 pA represents the typical leakage current of the CA3080A when strobed off. If C_1 were increased to 2000 pF, the "hold-droop" rate will decrease to 0.085 μV/μs, but the slew rate would decrease to 0.25 V/μs. The parallel diode network connected between terminal 3 of the CA3080A and terminal 6 of the CA3140 prevents large input-signal feed-through across the input terminals of the CA3080A to the 200 pF storage capacitor when the CA3080A is strobed off. Fig. 35 shows dynamic characteristic waveforms of this sample-and-hold system.



TOP TRACE: OUTPUT
(50 mV/DIV. AND 200 ns/DIV.)
BOTTOM TRACE: INPUT
(50 mV/DIV. AND 200 ns/DIV.)
92CS-27883



LARGE-SIGNAL RESPONSE AND SETTLING TIME
TOP TRACE: OUTPUT SIGNAL
(5 V/DIV. AND 2 μs/DIV.)
BOTTOM TRACE: INPUT SIGNAL
(5 V/DIV. AND 2 μs/DIV.)
CENTER TRACE: DIFFERENCE OF INPUT AND OUTPUT SIGNALS THROUGH TEKTRONIX AMPLIFIER 7A13
(5 mV/DIV. AND 2 μs/DIV.) 92CS-27884



SAMPLING RESPONSE
TOP TRACE: SYSTEM OUTPUT
(100 mV/DIV. AND 500 ns/DIV.)
BOTTOM TRACE: SAMPLING SIGNAL
(20 V/DIV. AND 500 ns/DIV.)
92CS-27885

Fig. 35 – Sample- and hold system dynamic characteristics waveforms.

CURRENT AMPLIFIER

The low input-terminal current needed to drive the CA3140 makes it ideal for use in current-amplifier applications such as the one shown in Fig. 36.● In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R2/R1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100 nA, with values shown, the load current presented to the supply will be 100 μA; a much easier current to measure in many systems.

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output-load capacitance and the potential oscillation in this situation. Essentially, the necessary high-frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

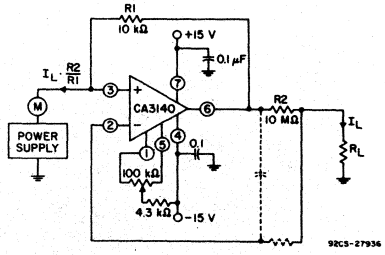


Fig. 36 – Basic current amplifier for low-current measurement systems.

Fig. 37 shows a single-supply, absolute-value, ideal full-wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No.6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3140 functions as a normal inverting amplifier with a gain equal to −R2/R1. When the equality of the two equations shown in Fig. 37 is satisfied, the full-wave output is symmetrical.

● "Operational Amplifiers Design and Applications", J. G. Graeme, McGraw-Hill Book Company, page 308 – "Negative Immittance Converter Circuits".

CA3140, CA3140A, CA3140B Types

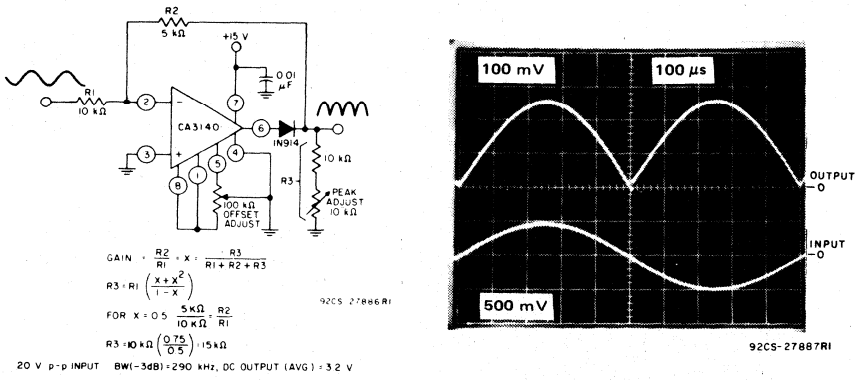


Fig. 37 – Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.

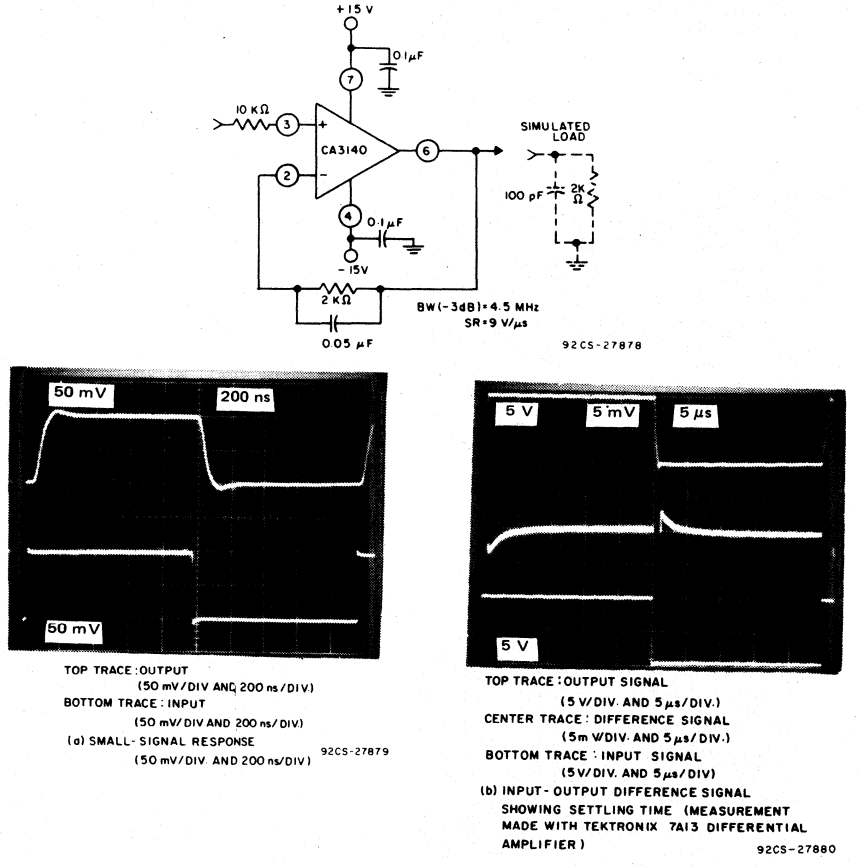


Fig. 38 – Split-supply voltage-follower test circuit and associated waveforms.

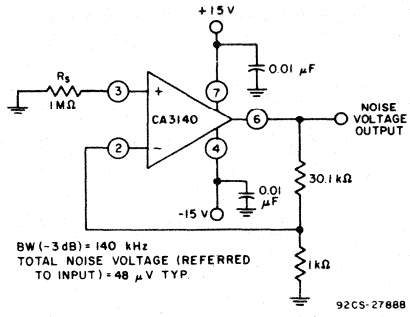
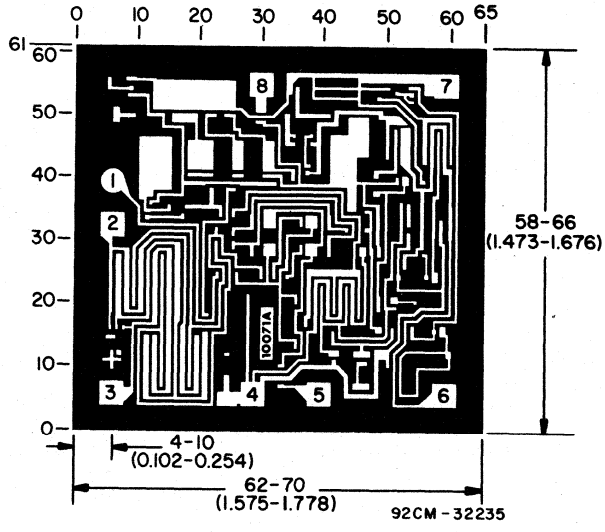


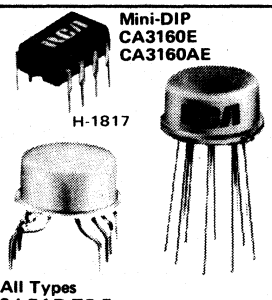
Fig. 39 – Test circuit amplifier (30-dB gain) used for wideband noise measurement.



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3160, CA3160A, CA3160B Types



BiMOS Operational Amplifiers

With MOS/FET Input, COS/MOS Output

FEATURES:

- *Similar to CA3130 but has internal compensation*
- *MOS/FET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 × 10^{12}Ω) typ.
  very low I_I = 5 pA typ. at 15-V operation
  2 pA typ. at 5-V operation
- *Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *COS/MOS output stage permits signal swing to either (or both) supply rails*

} *Ideal for single-supply applications*

The RCA-CA3160T, CA3160S, CA3160E; CA3160AT, CA3160AS, CA3160AE; and CA3160BT, CA3160BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip. The CA3160 series circuits are frequency-compensated versions of the popular CA3130 series.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3160 Series circuits operate at supply voltages ranging from 5 to 16 volts, or +2.5 to +8 volts when using split supplies, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3160 series is supplied in standard 8-lead TO-5 style packages (T suffix) and 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" packages (S suffix). The CA3160 is available in chip form (H suffix).

- *Low V_{IO}: 2 mV max. (CA3160B)*
- *Wide BW: 4 MHz typ. (unity-gain crossover)*
- *High SR: 10 V/μs typ. (unity-gain follower)*
- *High output current (I_O): 20 mA typ.*
- *High A_{OL}: 320,000 (110 dB) typ.*
- *Internal phase compensation for unity gain (With terminal access for supplementary external phase compensation network if desired)*

APPLICATIONS:

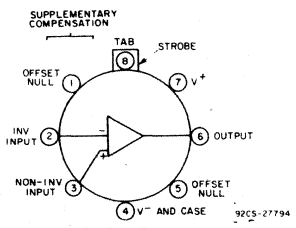
- *Ground-referenced single-supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *Ideal interface with digital COS/MOS*
- *High-input-impedance wideband amplifiers*
- *Voltage followers (e.g., follower for single-supply D/A converter)*
- *Wien-Bridge oscillators*
- *Voltage-controlled oscillators*
- *Photo-diode sensor amplifiers*

The CA3160A and CA3160 are also available in the 8-lead dual-in-line plastic package (Mini-DIP-E suffix). All types operate over the full military-temperature range of -55° C to +125° C. The CA3160B is intended for applications requiring premium-grade specifications. The CA3160A offers superior input characteristics over those of the CA3160.

CA3160, CA3160A, CA3160B Types

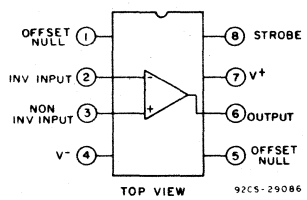
ELECTRICAL CHARACTERISTICS at T_A=25°C, V^+=15 V, V^- = 0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS									Units
	CA3160B (T, S)			CA3160A (T, S, E)			CA3160 (T, S, E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.8	2	–	2	5	–	6	15	mV
Input Offset Current, $\|I_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	–	5	20	–	5	30	–	5	50	pA
Large-Signal Voltage Gain, A_{OL}	100 k	320 k	–	50 k	320 k	–	50 k	320 k	–	V/V
V_O=10 V_{p-p}, R_L=2 kΩ	100	110	–	94	110	–	94	110	–	dB
Common-Mode Rejection Ratio, CMRR	86	100	–	80	95	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR}	0	−0.5 to 12	10	0	−0.5 to 12	10	0	−0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	–	32	100	–	32	150	–	32	320	μV/V
Maximum Output Voltage:										
At R_L=2 kΩ V_{OM}^+	12	13.3	–	12	13.3	–	12	13.3	–	V
At R_L=2 kΩ V_{OM}^-	–	0.002	0.01	–	0.002	0.01	–	0.002	0.01	V
At R_L=∞ V_{OM}^+	14.99	15	–	14.99	15	–	14.99	15	–	V
At R_L=∞ V_{OM}^-	–	0	0.01	–	0	0.01	–	0	0.01	V
Maximum Output Current: I_{OM}^+ (Source) @ V_O = 0 V	12	22	45	12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O = 15 V	12	20	45	12	20	45	12	20	45	mA
Supply Current, I^+: V_O=7.5 V, R_L=∞	–	10	15	–	10	15	–	10	15	mA
V_O = 0 V, R_L = ∞	–	2	3	–	2	3	–	2	3	mA
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$*	–	5	–	–	6	–	–	8	–	μV/°C



TOP VIEW

S and T Suffixes



E Suffix

CA3160 Series devices have an on-chip frequency-compensation network. Supplementary phase-compensation or frequency roll-off (if desired) can be connected externally between terminals 1 and 8.

Fig. 1 – Functional diagrams of the CA3160 Series.

CA3160, CA3160A, CA3160B Types

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS		CA3160B (T, S)	CA3160A (T, S, E)	CA3160 (T, S, E)	UNITS
	$V^+ = +7.5$ V, $V^- = -7.5$ V, $T_A = 25^oC$ (Unless Otherwise Specified)					
Input Offset Voltage Adjustment Range	10 kΩ across Terms. 4 and 5 or 4 and 1		±22	±22	±22	mV
Input Resistance, R_I			1.5	1.5	1.5	TΩ
Input Capacitance, C_I	f = 1 MHz		4.3	4.3	4.3	pF
Equivalent Input Noise Voltage, e_n	BW= 0.2 MHz	R_S=1 MΩ	40	40	40	μV
		R_S=10MΩ	50	50	50	
Equivalent Input Noise Voltage, e_n	R_S= 100 Ω	1 kHz	72	72	72	$nV\sqrt{Hz}$
		10 kHz	30	30	30	
Unity Gain Crossover Frequency, f_T			4	4	4	MHz
Slew Rate, SR:			10	10	10	V/μs
Transient Response: Rise Time, t_r	C_L = 25 pF, R_L = 2 kΩ (Voltage Follower)		0.09	0.09	0.09	μs
Overshoot			10	10	10	%
Settling Time (4 V_{p-p} Input to <0.1%)			1.8	1.8	1.8	μs

CHARACTERISTIC	TEST CONDITIONS	CA3160B (T, S)	CA3160A (T, S, E)	CA3160 (T, S, E)	UNITS
	$V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$ (Unless Otherwise Specified)				
Input Offset Voltage, V_{IO}		1	2	6	mV
Input Offset Current, I_{IO}		0.1	0.1	0.1	pA
Input Current, I_I		2	2	2	pA
Common-Mode Rejection Ratio, CMRR		100	90	80	dB
Large-Signal Voltage Gain, A_{OL}	$V_O = 4\ V_{p-p}$, R_L = 5 kΩ	100 k	100 k	100 k	V/V
		100	100	100	dB
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.8	0 to 2.8	0 to 2.8	V
Supply Current, I^+	V_O = 5 V, $R_L = \infty$	300	300	300	μA
	V_O = 2.5 V, $R_L = \infty$	500	500	500	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	200	μV/V

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC
INPUT VOLTAGE... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK −
UP TO 55°C ..... 630 mW
ABOVE 55°C .... Derate linearly 6.67 mW/°C
WITH HEAT SINK −
UP TO 90°C ..... 1 W
ABOVE 90°C ... Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:
OPERATING (All Types).... −55 to +125°C
STORAGE (All Types) ..... −65 to +150°C
OUTPUT SHORT-CIRCUIT
DURATION* ..... INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH
(1.59 ± 0.79 MM) FROM CASE
FOR 10 SECONDS MAX. ..... +265°C

*Short circuit may be applied to ground or to either supply.

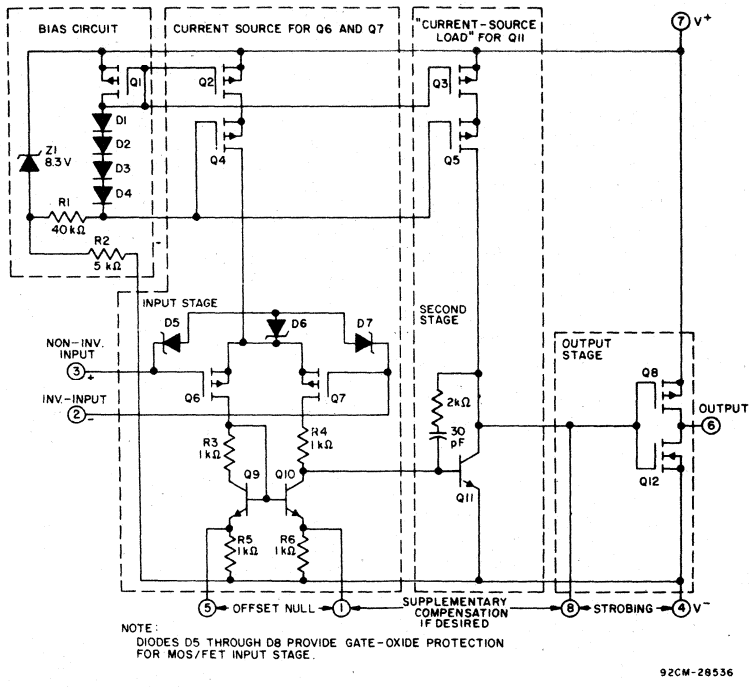


Fig.2 – Schematic diagram of the CA3160 Series.

CIRCUIT DESCRIPTION

Fig.3 is a block diagram of the CA3160 series COS/MOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3160 series circuits are ideal for single-supply operation. Three class A amplifier stages, having the individual gain capability and current consumption shown in Fig.3, provide the total gain of the CA3160. A biasing circuit provides two potentials for common use in the first and second stages. Terminals 8 and 1 can be used to supplement the internal phase compensation network if additional phase compensation or frequency roll-off is desired. Terminals 8 and 4 can also be used to strobe the output stage into a low quiescent current state. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply-rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive COS/MOS digital circuits in comparator applications).

CA3160, CA3160A, CA3160B Types

Input Stages – The circuit of the CA3160 is shown in Fig.2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4, are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D7 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

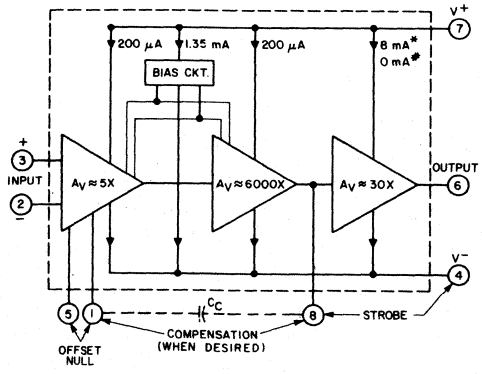
Second-Stage – Most of the voltage gain in the CA3160 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is described later. Miller Effect compensation (roll off) is accomplished by means of the 30-pF capacitor and 2-kΩ resistor connected between the base and collector of transistor Q11. These internal components provide sufficient compensation for unity gain operation in most applications. However, additional compensation, if desired, may be used between Terminals 1 and 8.

Bias-Source Circuit – At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Terminal 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage – The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig.6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

† For general information on the characteristics of COS/MOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "COS/MOS Transistor Array".



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15 V
* WITH INPUT TERMINALS BIASED SO THAT TERM. 6 POTENTIAL IS +7.5 V ABOVE TERM. 4.
* WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.

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Fig. 3 – Block diagram of the CA3160 Series.

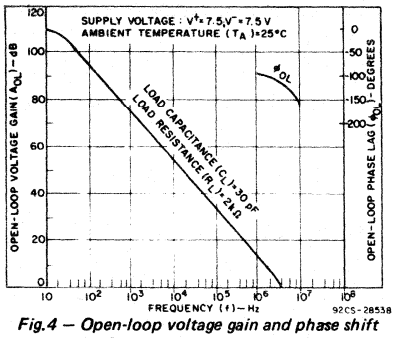


Fig.4 – Open-loop voltage gain and phase shift vs. frequency.

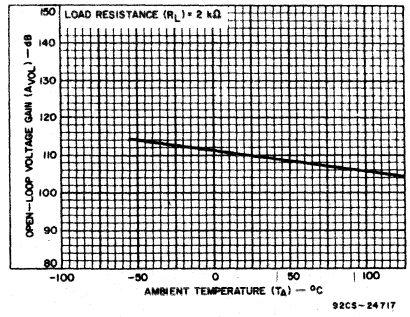


Fig.5 – Open-loop gain vs. temperature.

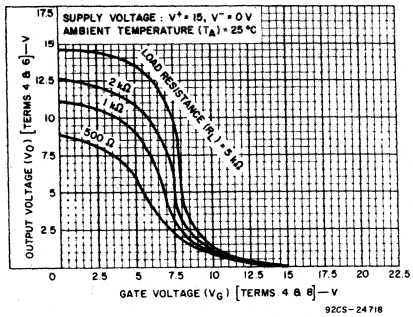


Fig.6 – Voltage transfer characteristics of COS/MOS output stage.

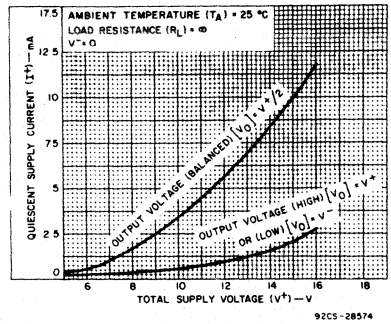


Fig.7 – Quiescent supply current vs. supply voltage.

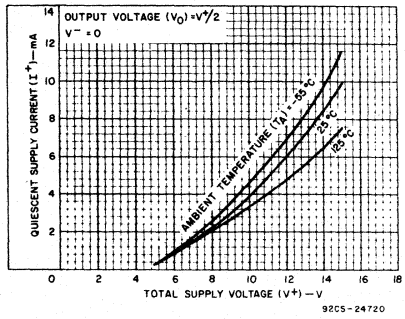


Fig.8 – Quiescent supply current vs. supply voltage at several temperatures.

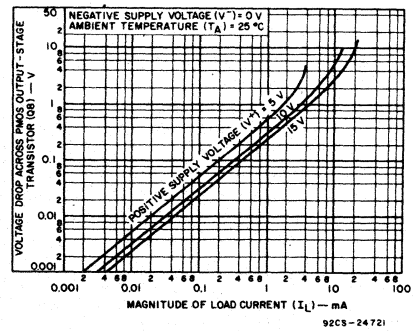


Fig.9 – Voltage across PMOS output transistor (Q8) vs. load current.

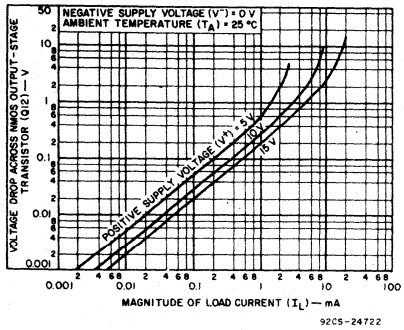


Fig.10 – Voltage across NMOS output transistor (Q12) vs. load current.

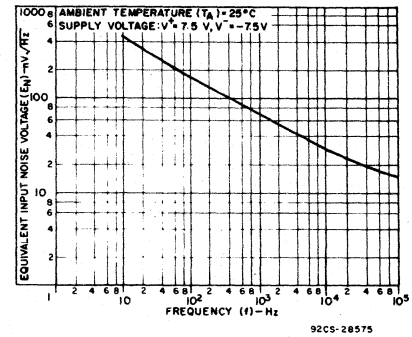


Fig.11 – Equivalent noise voltage vs. frequency.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3160 Series Op-Amps is typically 5 pA at T_A=25°C when Terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig. 12 contains

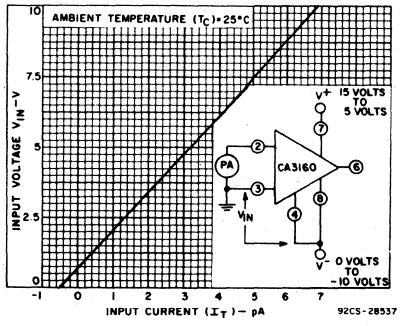


Fig. 12 – Input current vs. common-mode voltage.

data showing the variation of input current as a function of common-mode input voltage at T_A=25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3160 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Input-Current Variation with Temperature

The input current of the CA3160 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig. 13 provides data on the typical variation of input bias current as a function of temperature in the CA3160.

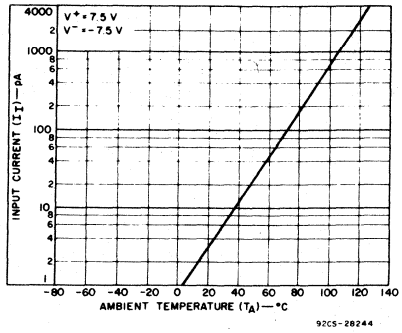


Fig. 13 – Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3160. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3160 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terminals 2 and 3. Fig. 14 shows typical data pertinent to shifts in offset voltage encountered with CA3160 devices in TO-5 packages during life testing. At lower temperatures (TO-5 and plastic) for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those en-

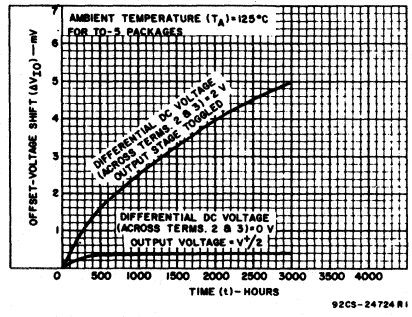
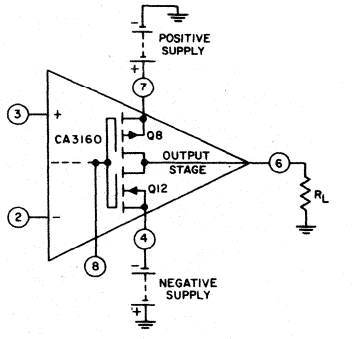


Fig. 14 – Typical incremental offset-voltage shift vs. operating life.

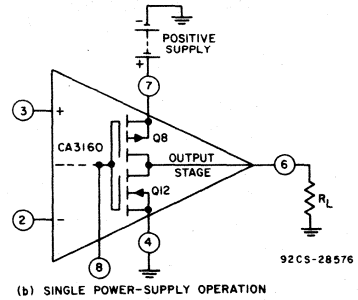
countered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output state is "toggled", e.g., as in comparator applications.

Power-Supply Considerations

Because the CA3160 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 15(a) and 15(b) show the CA3160 connected for both dual- and single-supply operation.



(a) DUAL POWER-SUPPLY OPERATION



(b) SINGLE POWER-SUPPLY OPERATION

Fig. 15 – CA3160 output stage in dual and single power-supply operation.

Dual-supply operation: When the output voltage at Terminal 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3160 operated under these conditions.

Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3160, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 15(a) shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L=\infty$, by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Terminal 6 and ground in the circuit of Fig. 15(b). Let it further be assumed again that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is a $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3160 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 40 μV when the test-circuit amplifier of Fig.16 is operated at a total supply voltage of 15 volts. This value of

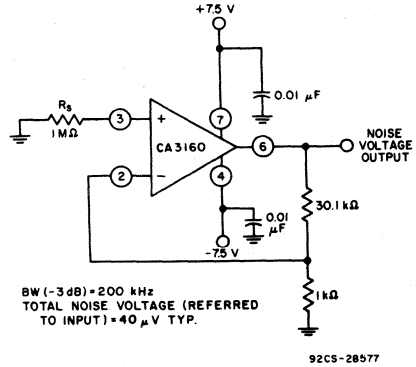
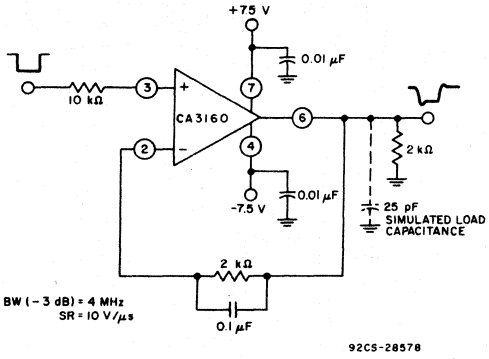
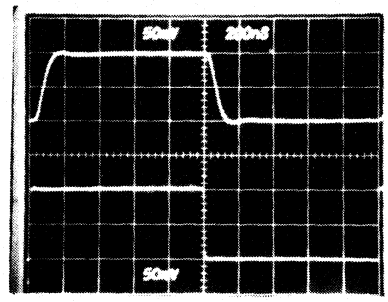


Fig. 16 – Test-circuit amplifier (30-dB gain) used for wideband noise measurements.

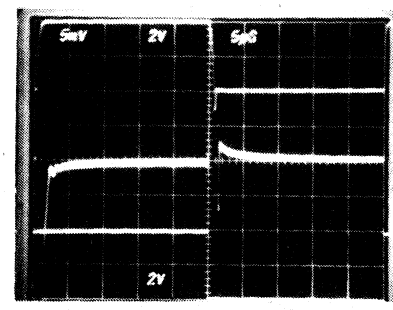
total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.



(a)



(b) *Small Signal Response*
Top Trace: Output
Bottom Trace: Input



(c) *Input-Output Difference Signal Showing Settling Time*
Top Trace: Output Signal
Center Trace: Difference Signal 5 mV/div
Bottom Trace: Input Signal

Fig. 17 – Split-supply voltage follower with associated waveforms.

TYPICAL APPLICATIONS

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3160, are particularly suited to service as voltage followers. Fig.17 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3160 in a split-supply configuration.

A voltage follower, operated from a single-supply, is shown in Fig.18 together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig.18b with input-signal ramping. The waveforms in Fig.18c show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig.18c also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3160 in a single-supply voltage-follower application.

9-Bit COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig.19. This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3160 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with COS/MOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig.19.

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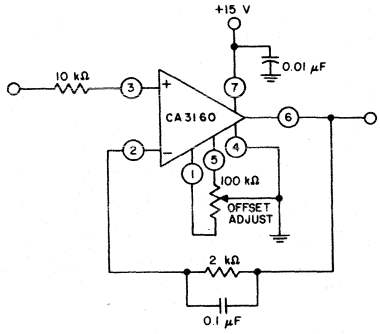
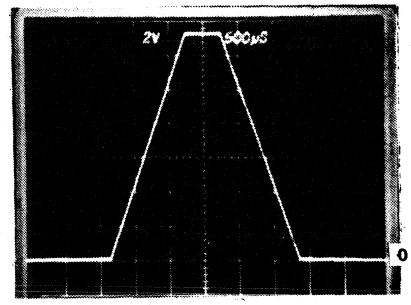
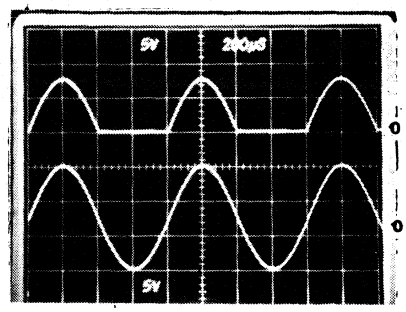
* "Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC", Application Note ICAN-6080.



(a)



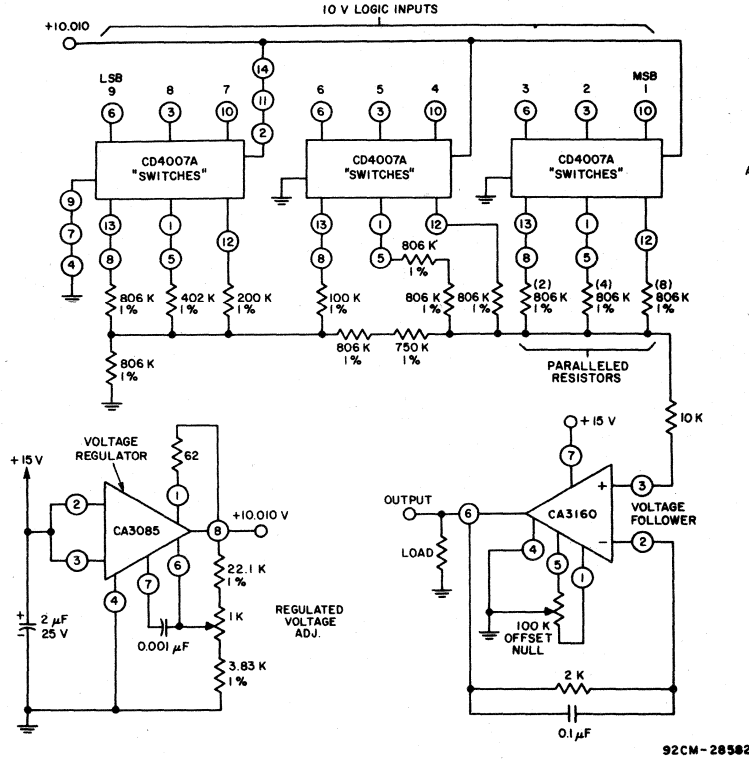
(b) Output signal with input-signal ramping.



92CS-28581R1

(c) Output-Waveform with Ground-Reference Sine-Wave Input
Top Trace: Output
Bottom Trace: Input

Fig.18 – Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig.9 in ICAN-6080.)



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS.

ALL RESISTANCES IN OHMS

Fig.19 – 9-bit DAC using COS/MOS digital switches and CA3160.

The circuit uses an R/2R voltage-ladder network, with the output-potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3160 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

Error-Amplifier in Regulated Power Supplies

The CA3160 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero.

The circuit shown in Fig.20 uses a CA3160 as an error amplifier in a continuously adjustable 1-ampere power supply. One of the key features of this circuit is its ability to regulate down to the vicinity of zero volts with only one dc power supply input.

An RC network, connected between the base of the output drive transistor and the input voltage, prevents "turn-on overshoot", a condition typical of many operational-amplifier regulator circuits. As the amplifier becomes operational, this RC network ceases to have any influence on the regulator performance.

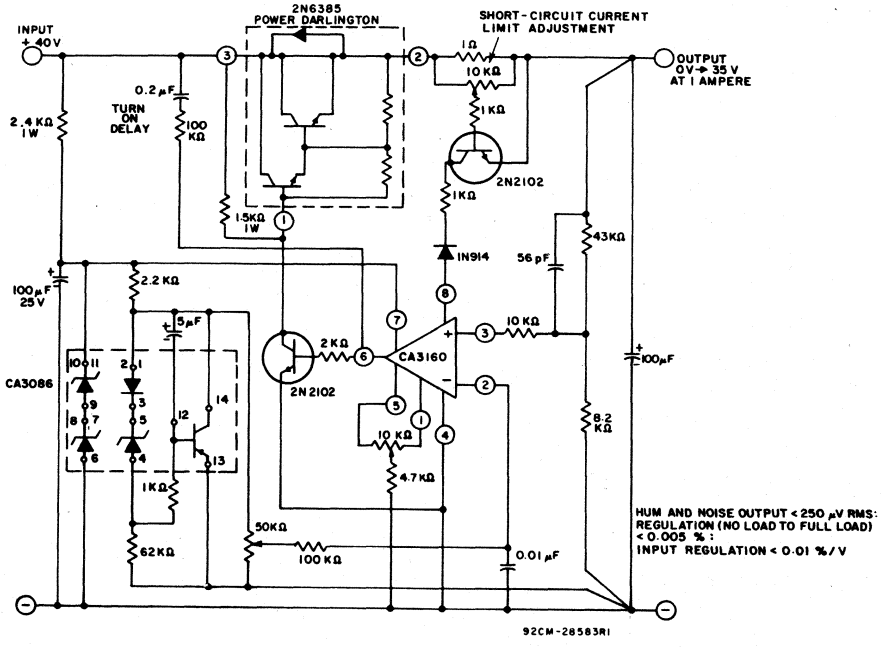


Fig.20 – Voltage regulator circuit (0.1 to 35 V at 1 A).

Precision Voltage-Controlled Oscillator

The circuit diagram of a precision voltage-controlled oscillator is shown in Fig.21. The oscillator operates with a tracking error in the order of 0.02 percent and a temperature coefficient of 0.01%/°C. A multivibrator (A_1) generates pulses of constant amplitude (V) and width (T_2). Since the output (terminal 6) of A_1 (a CA3130) can swing within about 10 millivolts of either supply-rail, the output pulse amplitude (V) is essentially equal to V+. The average output voltage ($E_{avg} = V\ T_2/T_1$) is applied to the non-inverting input terminal of comparator A_2 via an integrating network R_3, C_2. Comparator A_2 operates to establish circuit conditions such that $E_{avg} = V1$. This circuit condition is accomplished by feeding an output signal from terminal 6 of A_2 through R_4, D_4 to the inverting terminal (terminal 2) of A_1, thereby adjusting the multivibrator interval, T_3.

Voltmeter With High Input Resistance

The voltmeter circuit shown in Fig.22 illustrates an application in which a number of the CA3160 characteristics are exploited. Range-switch SW1 is ganged between input and output circuitry to permit selection of the proper output voltage for feedback to Terminal 2 via 10 KΩ current-limiting resistor. The circuit is powered by a single 8.4-volt mercury battery. With zero input signal, the circuit consumes somewhat less than 500 microamperes plus the meter current required to indicate a given voltage. Thus, at full-scale input, the total supply current rises to slightly more than 1500 microamperes.

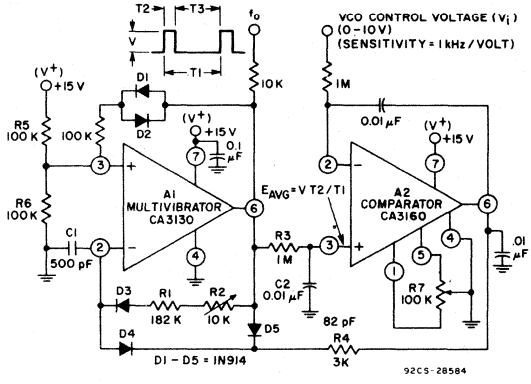


Fig.21 – Voltage-controlled oscillator.

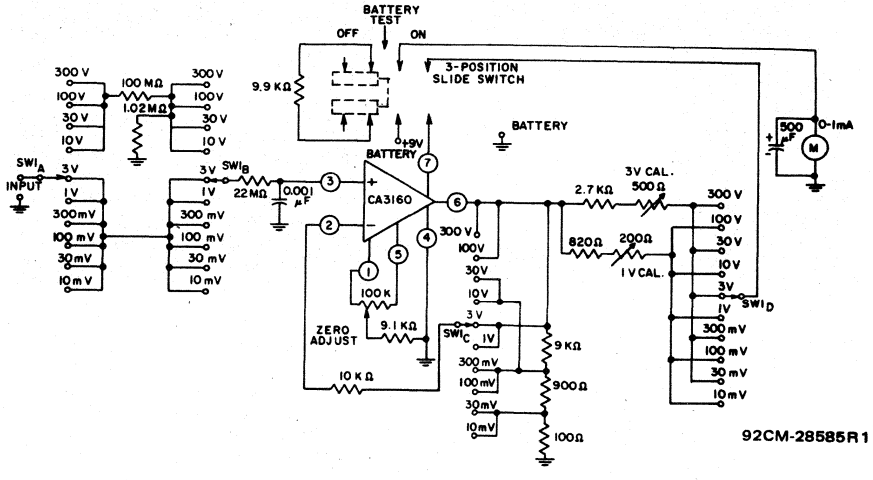


Fig.22 – High-input-resistance DC voltmeter.

CA3160, CA3160A, CA3160B Types

Function Generator

A function generator having a wide tuning range is shown in Fig.23. The adjustment range, in excess of 1,000,000/1, is accomplished by a single potentiometer. Three operational amplifiers are utilized: a CA3160 as a voltage follower, a CA3080 as a high-speed comparator, and a second CA3080A as a programmable current source. Three variable capacitors C1, C2, and C3 shape the triangular signal between 500 kHz and 1 MHz. Capacitors C4, C5, and the trimmer potentiometer in series with C5 maintain essentially constant (±10%) amplitude up to 1 MHz.

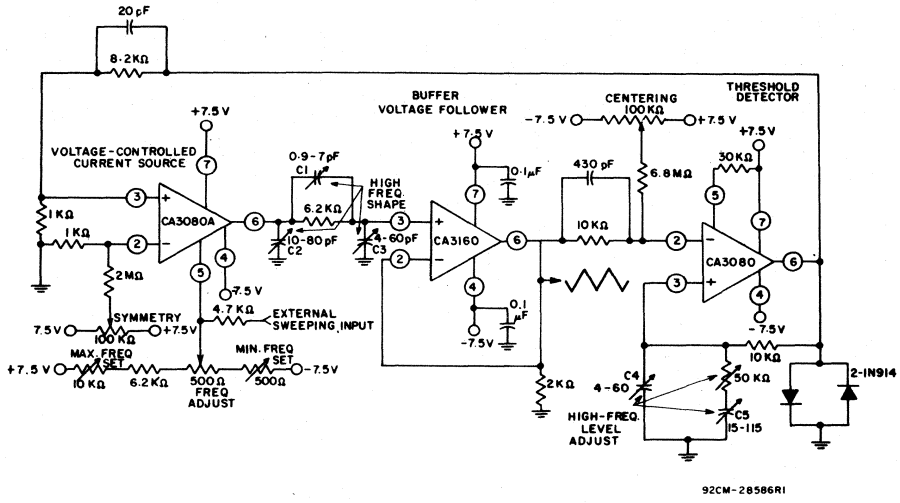
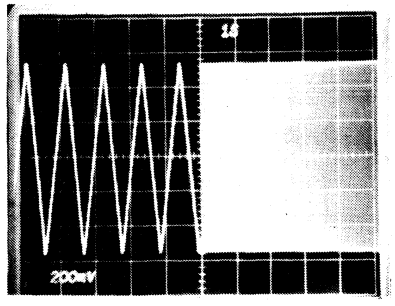
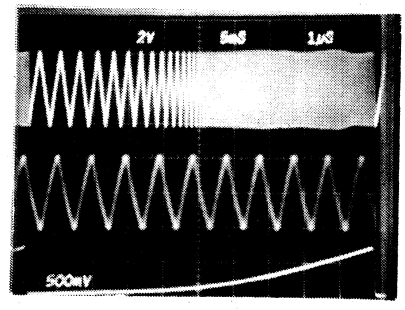


Fig.23(a) – 1,000,000/1 single-control function generator – 1 MHz to 1 Hz.



(b) – Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.

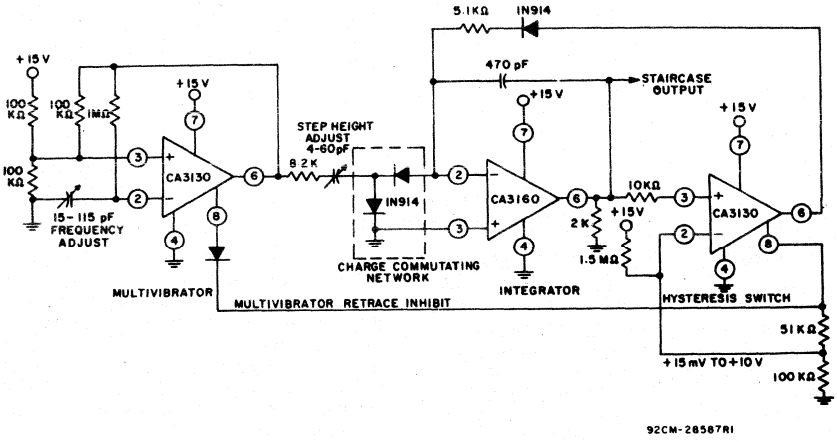


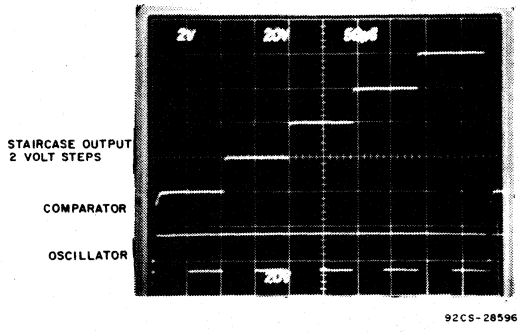
92CS-28588

(c) – Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

Staircase Generator

Fig.24 shows a staircase generator circuit utilizing three COS/MOS operational amplifiers. Two CA3130's are used; one as a multivibrator, the other as a hysteresis switch. The third amplifier, a CA3160, is used as a linear staircase generator.





(b) – Staircase Generator Waveform
Top Trace: Staircase Output
2 Volt Steps
Center Trace: Comparator
Bottom Trace: Oscillator

Picoammeter Circuit

Fig. 25 is a current-to-voltage converter configuration utilizing a CA3160 and CA3140 to provide a picoampere meter for ±3 pA full-scale meter deflection. By placing Terminals 2 and 4 of the CA3160 at ground potential, the CA3160 input is operated in the "guarded mode". Under this operating condition, even slight leakage resistance present between Terminals 3 and 2 or between Terminals 3 and 4 would result in zero voltage across this leakage resistance, thus substantially reducing the leakage current.

If the CA3160 is operated with the same voltage on input Terminals 3 and 2 as on Terminal 4, a further reduction in the input current to the less than one picoampere level can be achieved as shown in Fig. 12.

To further enhance the stability of this circuit, the CA3160 can be operated with its output (Terminal 6) near ground, thus markedly reducing the dissipation by reducing the supply current to the device.

The CA3140 stage serves as a X100 gain stage to provide the required plus and minus output swing for the meter and feedback network. A 100-to-1 voltage divider network consisting of a 9.9-KΩ resistor in series with a 100-ohm resistor sets the voltage at the 10-KMΩ resistor (in series with Terminal 3) to ±30 mV full-scale deflection. This 30-mV signal results from ±3 volts appearing at the top of the voltage divider network which also drives the meter circuitry.

By utilizing a switching technique in the meter circuit and in the 9.9 KΩ and 100-ohm network similar to that used in voltmeter circuit shown in Fig. 22, a current range of 3 pA to 1 nA full scale can be handled with the single 10-KMΩ resistor.

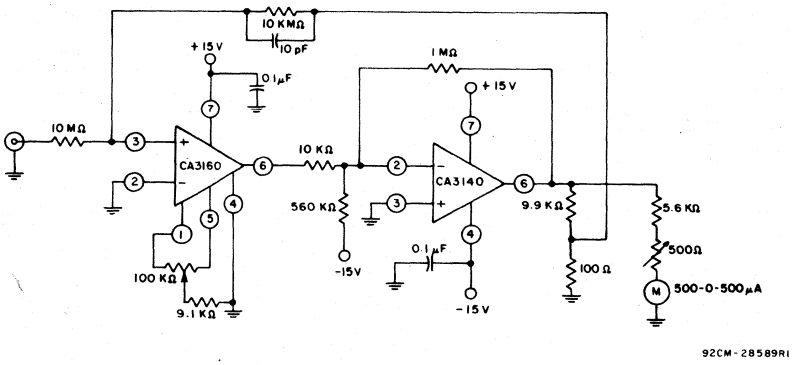


Fig.25 – Current-to-voltage converter to provide a picoammeter with ± 3 pA full-scale deflection.

Single-Supply Sample-and-Hold System

Fig. 26 shows a single-supply sample-and-hold system using a CA3160 to provide a high input impedance and an input-voltage range of 0 to 10 volts. The output from the input buffer integrator network is coupled to a CA3080A. The CA3080A functions as a strobeable current source for the CA3140 output integrator and storage capacitor. The CA3140 was chosen because of its low output impedance and constant gain-bandwidth product. Pulse "droop" during the hold interval can be reduced to zero by adjusting the 100-KΩ bias-voltage potentiometer on the positive input of the CA3140. This zero adjustment sets the CA3080A output voltage at its zero current position. In this sample-and-hold circuit it is essential that the amplifier bias current be reduced to zero to minimize output signal current during the hold mode. Even with 320 mV at the amplifier bias circuit terminal (5) at least ± 100 pA of output current will be available.

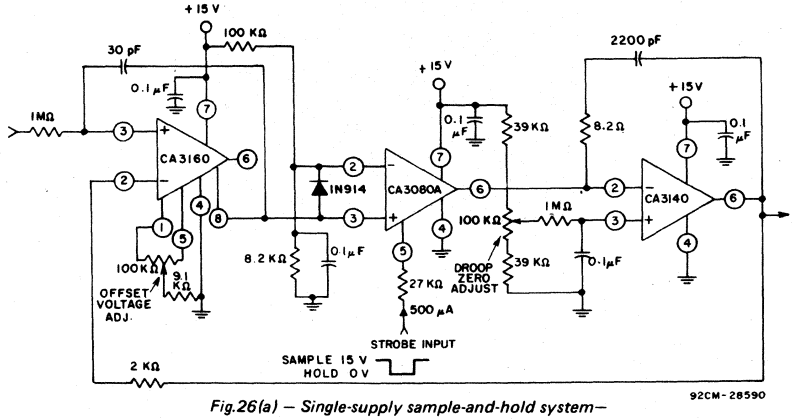
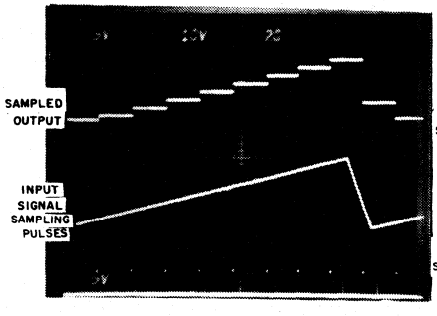
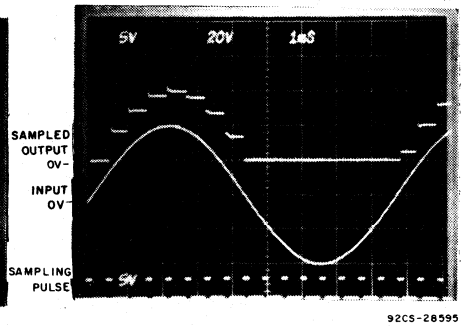


Fig.26(a) – Single-supply sample-and-hold system– input 0-to-10 volts.



(b) – Sample-and-hold waveform.
Top Trace: Sampled Output
Center Trace: Input Signal
Bottom Trace: Sampling Pulses



(c) – Sample-and-hold waveform.
Top Trace: Sampled Output
Center Trace: Input
Bottom Trace: Sampling Pulse

Wien Bridge Oscillator

A simple, single-supply Wien Bridge oscillator using a CA3160 is shown in Fig. 27. A pair of parallel-connected 1N914 diodes comprise the gain-setting network which standardizes the output voltage at approximately 1.1 volts. The 500-ohm potentiometer is adjusted so that the oscillator will always start and the oscillation will be maintained. Increasing the amplitude of the voltage may lower the threshold level for starting and for sustaining the oscillation, but will introduce more distortion.

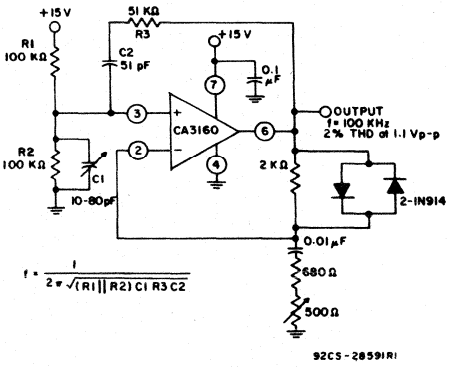


Fig.27 – Single-supply Wien Bridge oscillator.

Operation with Output-Stage Power-Booster

The current sourcing and sinking capability of the CA3160 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig.28, three COS/MOS transistor-pairs in a single CA3600 IC array are shown parallel-connected with the output stage in the CA3160. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA3160 output stage by about 2.5X.

The amplifier circuit in Fig. 28 employs feedback to establish a closed-loop gain of 20 dB. The typical large-signal-bandwidth (−3 dB) is 190 kHz.

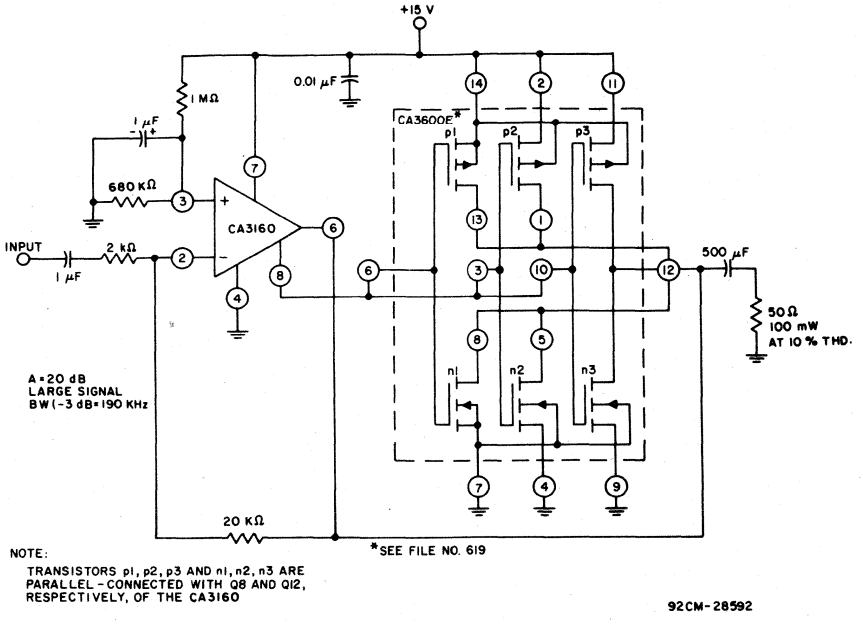
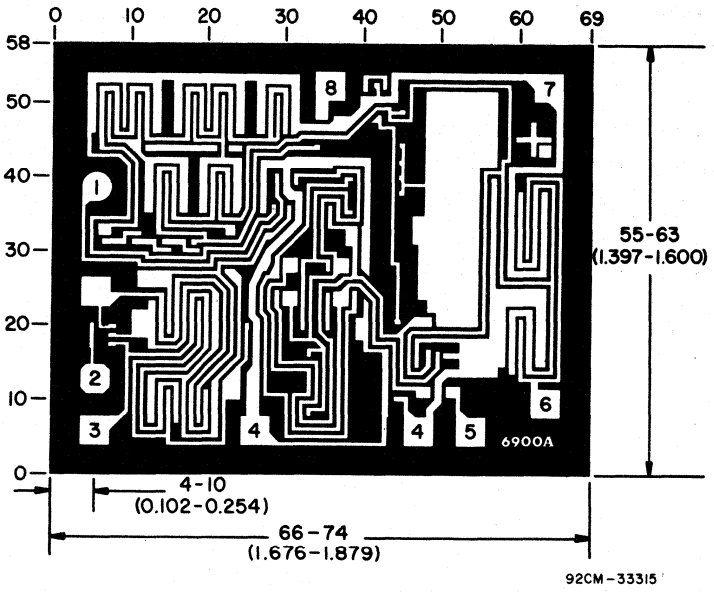


Fig.28 – COS/MOS transistor array (CA3600E) connected as power booster in the output stage of the CA3160.

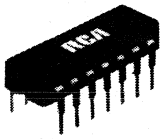
CA3160, CA3160A, CA3160B Types



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photograph and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips the cleavage angles are 57^{o} instead of 90^{o} with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.


Mini-DIP
(E Suffix)
H-1817


14-Lead DIP
(E1 Suffix)
H-1517

Dual BiMOS Operational Amplifiers

With MOS/FET Input, Bipolar Output

Features:

- *Dual version of CA3140*
- *Internally compensated*
- *MOS/FET input stage*
  - (a) *Very high input impedance (Z_{IN}) - 1.5 TΩ typ.*
  - (b) *Very low input current (I_I) - 10 pA typ. at ± 15 V*
  - (c) *Wide common-mode input-voltage range (V_{ICR}) - can be swung 0.5 volt below negative supply-voltage rail*
  - (d) *Rugged input stage - bipolar diode protected*
- *Directly replaces industry types 747 and 1458 in most applications*
- *Operation from 4-to-36 volts single or dual supplies*
- *Characterized for ± 15-volt operation and for TTL supply systems with operation down to 4 volts*
- *Wide bandwidth - 4.5 MHz unity gain at ± 15 V or 30 V*
- *High voltage-follower slew rate - 9/Vμs*
- *Output swings to within 0.5 volt of negative supply at $V^+ = 5$ V, $V^- = 0$*

Applications:

- *Ground-referenced single-supply amplifiers in automobile and portable instrumentation*
- *Sample and hold amplifiers*
- *Long-duration timers/multivibrators (microseconds - minutes - hours)*
- *Photocurrent instrumentation*
- *Active filters*
- *Intrusion alarm systems*
- *Comparators*
- *Instrumentation amplifiers*
- *Function generators*
- *Power supplies*

The RCA-CA3240A and CA3240 are dual versions of the popular CA3140-series integrated circuit operational amplifiers. They combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOS/FET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range (typically to 0.5 V below the negative supply rail). The bipolar output transistors allow a wide output voltage swing and provide a high output current capability.

The CA3240A and CA3240 are supplied in the 8-lead dual-in-line plastic package (Mini-DIP, E suffix), and in the 14-lead dual-in-line plastic package (E1 suffix). They are pin-compatible with the industry standard 747 and 1458 operational amplifiers in similar packages. The CA3240A and CA3240 have an operating-temperature range of −40 to +85° C. The offset null feature is available only when these types are supplied in the 14-lead dual-in-line plastic package (E1 suffix). The CA3240 is also available in chip form (H suffix).

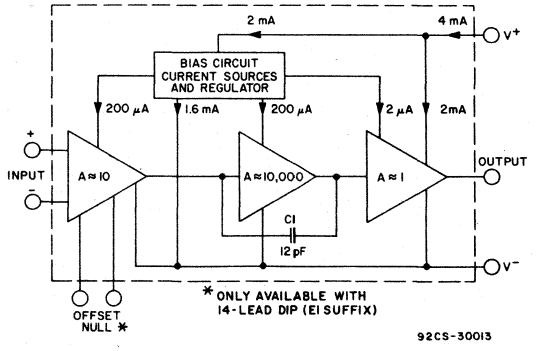


Fig. 1 — Block diagram of one-half CA3240 series.

CA3240, CA3240A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V
OPERATING VOLTAGE RANGE	4 to 36 V or ±2 to ±18 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±8 V
COMMON-MODE DC INPUT VOLTAGE	(V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT	1 mA
DEVICE DISSIPATION:	
UP TO 55°C	630 mW
ABOVE 55°C	Derate linearly 6.67 mW/°C
TEMPERATURE RANGE:	
OPERATING	−40 to +85°C
STORAGE	−65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION●	UNLIMITED
LEAD TEMPERATURE (DURING SOLDERING):	
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	+265°C

● Short circuit may be applied to ground or to either supply. Temperatures and/or supply voltages must be limited to keep dissipation within maximum rating.

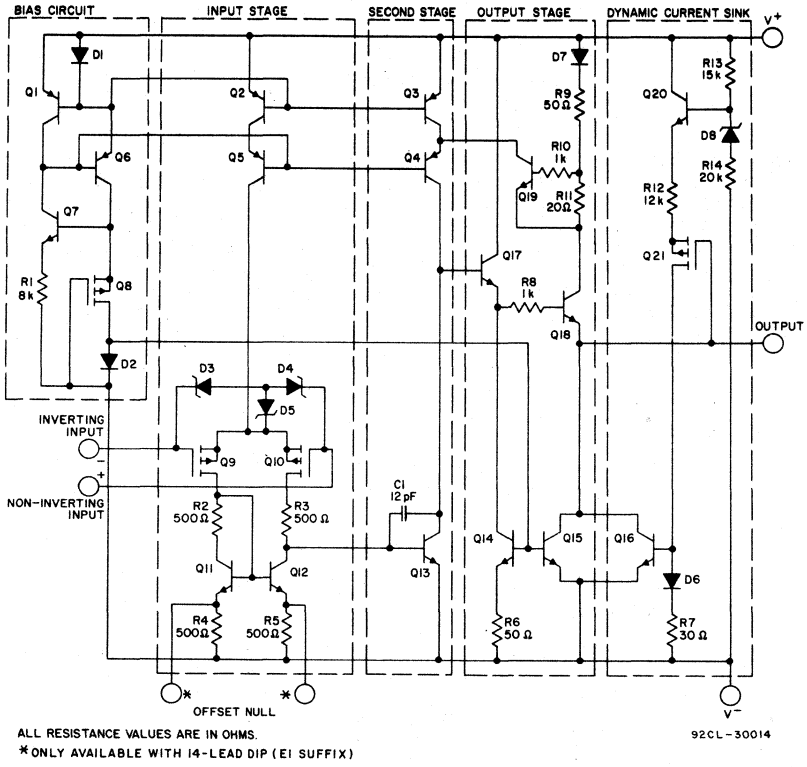


Fig. 2 – Schematic diagram of one-half CA3240 series.

Circuit Description

The schematic diagram of one amplifier section of the CA3240 is shown in Fig. 2. It consists of a differential amplifier stage using PMOS transistors Q9 and Q10 with gate-to-source protection against static discharge damage provided by zener diodes D3, D4, and D5. Constant current bias is applied to the differential amplifier from transistors Q2 and Q5 connected as a constant-current source. This assures a high common-mode rejection ratio. The output of the differential amplifier is coupled to the base of gain stage transistor Q13 by means of an n-p-n current mirror that supplies the required differential-to-single-ended conversion. Provision for offset null for types in the 14-lead plastic package (E1 suffix) is provided through the use of this current mirror.

The gain stage transistor Q13 has a high-impedance active load (Q3 and Q4) to provide maximum open-loop gain. The collector of Q13 directly drives the base of the compound emitter-follower output stage. Pull-down for the output stage is provided by two independent circuits: (1) constant-current-connected transistors Q14 and Q15 and (2) dynamic current-sink transistor Q16 and its associated circuitry. *The level of pull-down current is constant at about 1 mA for Q15 and varies from 0 to 18 mA for Q16 depending on the magnitude of the voltage between the output terminal and V^+.* The dynamic current sink becomes active whenever the output terminal is more negative than V^+ by about 15 V. When this condition exists, transistors Q21 and Q16 are turned on causing Q16 to sink current from the output terminal to V^-. This current always flows when the output is in the linear region, either from the load resistor or from the emitter of Q18 if no load resistor is present. The purpose of this dynamic sink is to permit the output to go within 0.2 V (V_{CE}(sat)) of V^- with a 2-kΩ load to ground. *When the load is returned to V^+, it may be necessary to supplement the 1 mA of current from Q15 in order to turn on the dynamic current sink (Q16).* This may be accomplished by placing a resistor (approx. 2 kΩ) between the output and V^-.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At V^+ = 15 V, V^- = 15 V, T_A = 25°C Unless Otherwise Specified

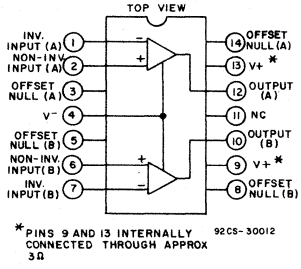
CHARACTERISTIC	LIMITS						UNITS
	CA3240A			CA3240			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	–	2	5	–	5	15	mV
Input Offset Current, $\|I_{IO}\|$	–	0.5	20	–	0.5	30	pA
Input Current, I_I	–	10	40	–	10	50	pA
Large-Signal Voltage Gain, A_{OL}●	20 k	100 k	–	20 k	100 k	–	V/V
(See Figs. 4, 19)	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR	–	32	320	–	32	320	μV/V
(See Fig. 9)	70	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR} (See Fig. 16)	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	11	V
Power-Supply Rejection Ratio, $\frac{\Delta V_{IO}}{\Delta V}$ PSRR	–	100	150	–	100	150	μV/V
(See Fig. 11)	76	80	–	76	80	–	dB
Maximum Output Voltage,■ V_{OM}^+	+12	13	–	+12	13	–	V
(See Figs. 22, 16) V_{OM}^-	−14	−14.4	–	−14	−14.4	–	
Maximum Output Voltage,† V_{OM}^-	0.4	0.13	–	0.4	0.13	–	V
Supply Current, I^+ (See Fig. 7) For Both Amps.	–	8	12	–	8	12	mA
Total Device Dissipation, P_D	–	240	360	–	240	360	mW

● At V_O = 26 V_{p-p}, +12 V, −14 V and R_L = 2 kΩ.
■ At R_L = 2 kΩ.
† At V^+ = 5 V, V^- = GND, I_{Sink} = 200 μA.

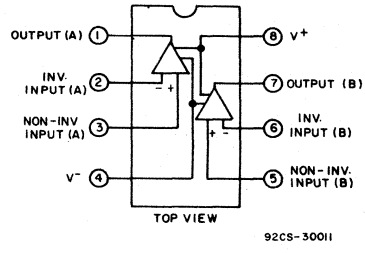
CA3240, CA3240A Types

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS $V^+ = +15$ V, $V^- = -15$ V, $T_A = 25^oC$	TYPICAL VALUES CA3240A	TYPICAL VALUES CA3240	UNITS
Input Offset Voltage Adjustment Resistor (E1 Package Only)		Typ. Value of Resistor Between Terms. 4 and 3(5) or Between 4 and 14(8) to Adjust Max. V_{IO}	18	4.7	kΩ
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I		4	4	pF
Output Resistance	R_O		60	60	Ω
Equivalent Wideband Input Noise Voltage (See Fig. 21)	e_n	BW=140 kHz, R_S = 1 MΩ	48	48	μV
Equivalent Input Noise Voltage (See Fig. 10)	e_n	f= 1 kHz, R_S=	40	40	nV/√Hz
		f=10 kHz, 100 Ω	12	12	
Short-Circuit Current to Opposite Supply Source	I_{OM}^+		40	40	mA
Sink	I_{OM}^-		11	11	
Gain-Bandwidth Product (See Figs. 5 and 19)	f_T		4.5	4.5	MHz
Slew Rate (See Fig. 6)	SR		9	9	V/μs
Transient Response: Rise Time	t_r	R_L=2 kΩ	0.08	0.08	μs
Overshoot (See Fig. 20)		C_L=100 pF	10	10	%
Settling Time at 10 V_{p-p}, (See Fig. 17) 1 mV	t_s	R_L=2 kΩ, C_L=100 pF, Voltage Follower	4.5	4.5	μs
10 mV			1.4	1.4	
Crosstalk		f = 1 kHz	120	120	dB



E1 Suffix
Pin compatible with the industry-standard 747



E Suffix
Pin compatible with the industry-standard 1458

Fig. 3 — Functional diagrams.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V^+ = 15 V, V^- = 15 V, T_A = −40 to +85°C Unless Otherwise Specified

CHARACTERISTIC		TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage,	$\lvert V_{IO}\rvert$	3	10	mV
Input Offset Current,♦	$\lvert I_{IO}\rvert$	32	32	pA
Input Current,♦	I_I	640	640	pA
Large-Signal Voltage Gain, (See Figs. 4, 19)	A_{OL}●	63 k	63 k	V/V
		96	96	dB
Common-Mode Rejection Ratio, (See Fig. 9)	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range, (See Fig. 16)	V_{ICR}	−15 to +12.3	−15 to +12.3	V
Power-Supply Rejection Ratio, (See Fig. 11)	$\Delta V_{IO}/\Delta V$ PSRR	150	150	μV/V
		76	76	dB
Maximum Output Voltage,■ (See Figs. 16, 22)	V_{OM}^+	12.4	12.4	V
	V_{OM}^-	−14.2	−14.2	
Supply Current, (See Fig. 7) For Both Amps.	I^+	8.4	8.4	mA
Total Device Dissipation,	P_D	252	252	mW
Temperature Coefficient of Input Offset Voltage,	$\Delta V_{IO}/\Delta T$	15	15	μV/°C

● At V_O = 26 $V_{p\text{-}p}$, +12 V, −14 V and R_L = 2 kΩ.

■ At R_L = 2 kΩ.

♦ At T_A = 85°C

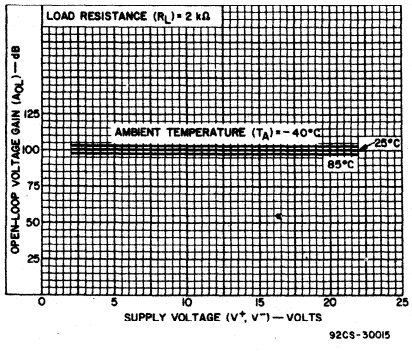


Fig. 4 — Open-loop voltage gain as a function of supply voltage and temperature.

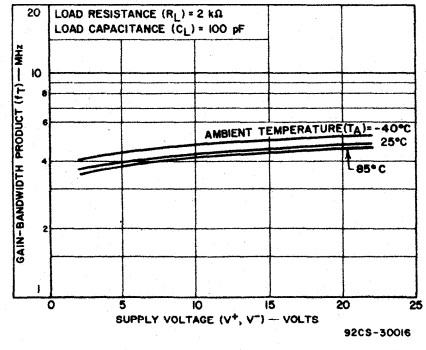


Fig. 5 — Gain-bandwidth product as a function of supply voltage and temperature.

CA3240, CA3240A Types

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE
At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25°C$

CHARACTERISTIC		TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage,	$\|V_{IO}\|$	2	5	mV
Input Offset Current,	$\|I_{IO}\|$	0.1	0.1	pA
Input Current,	I_I	2	2	pA
Input Resistance		1	1	TΩ
Large-Signal Voltage Gain, (See Figs. 4, 19)	A_{OL}	100 k	100 k	V/V
		100	100	dB
Common-Mode Rejection Ratio,	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range, (See Fig. 22)	V_{ICR}	−0.5	−0.5	V
		2.6	2.6	
Power-Supply Rejection Ratio,	PSRR	31.6	31.6	μV/V
		90	90	dB
Maximum Output Voltage, (See Figs. 16,22)	V_{OM}^+	3	3	V
	V_{OM}^-	0.3	0.3	
Maximum Output Current: Source,	I_{OM}^+	20	20	mA
Sink	I_{OM}^-	1	1	
Slew Rate (See Fig. 6)		7	7	V/μs
Gain-Bandwidth Product, (See Fig. 5)	f_T	4.5	4.5	MHz
Supply Current, (See Fig. 7)	I^+	4	4	mA
Device Dissipation,	P_D	20	20	mW

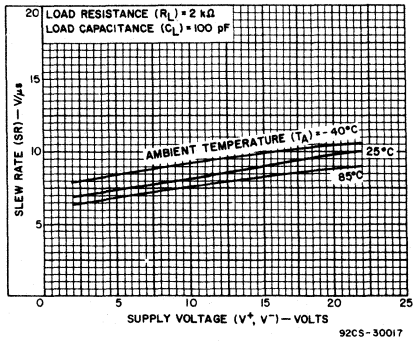


Fig. 6 — Slew rate as a function of supply voltage and temperature.

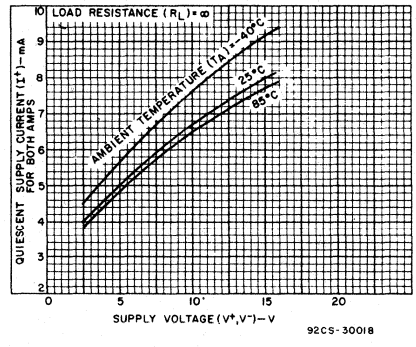


Fig. 7 — Quiescent supply current as a function of supply voltage and temperature.

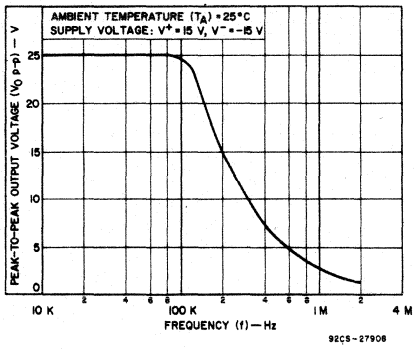


Fig. 8 — Maximum output voltage swing as a function of frequency.

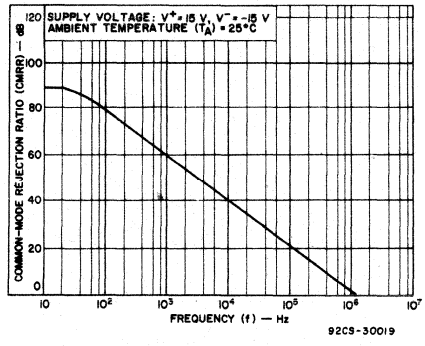


Fig. 9 — Common-mode rejection ratio as a function of frequency.

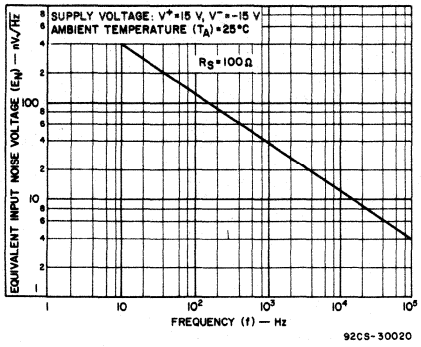


Fig. 10 — Equivalent input noise voltage as a function of frequency.

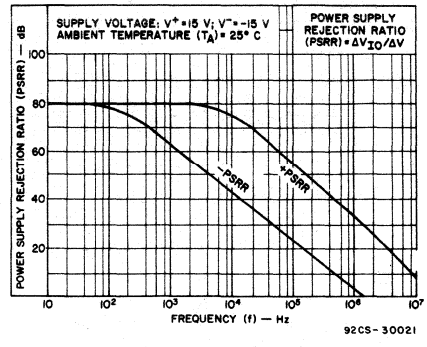


Fig. 11 — Power supply rejection ratio as a function of frequency.

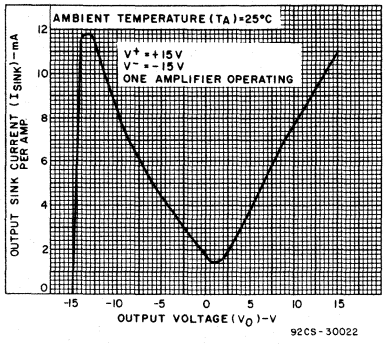


Fig. 12 — Output sink current as a function of output voltage.

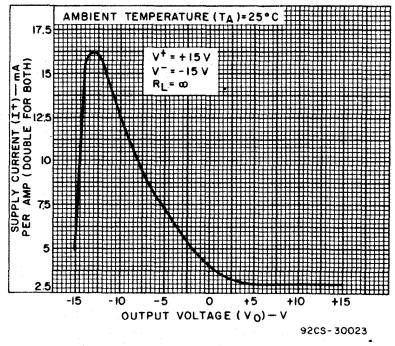


Fig. 13 — Supply current as a function of output voltage.

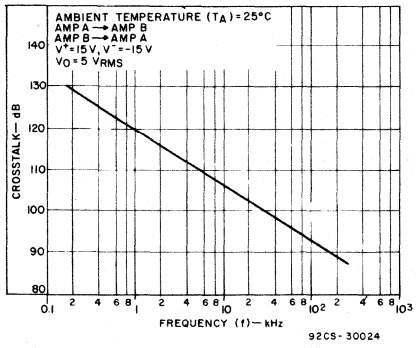


Fig. 14 — Crosstalk as a function of frequency.

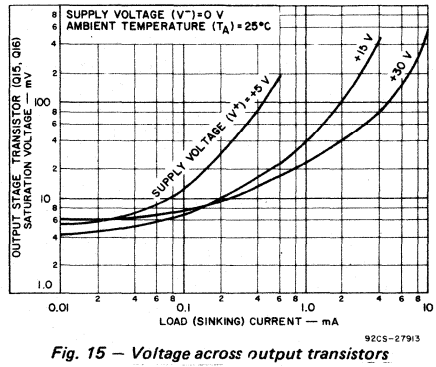


Fig. 15 — Voltage across output transistors Q15 and Q16 as a function of load current.

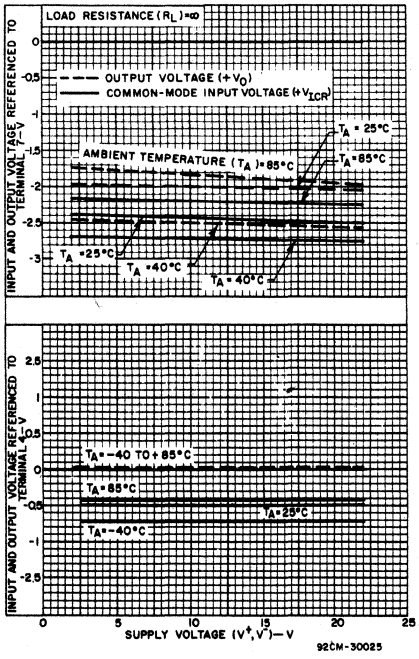


Fig. 16 — Output-voltage-swing capability and common-mode input-voltage range as a function of supply voltage and temperature.

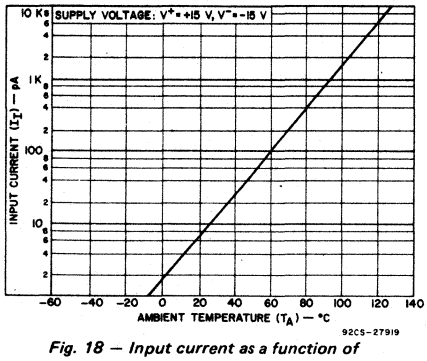
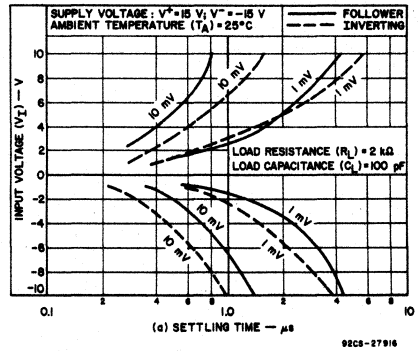


Fig. 18 — Input current as a function of ambient temperature.



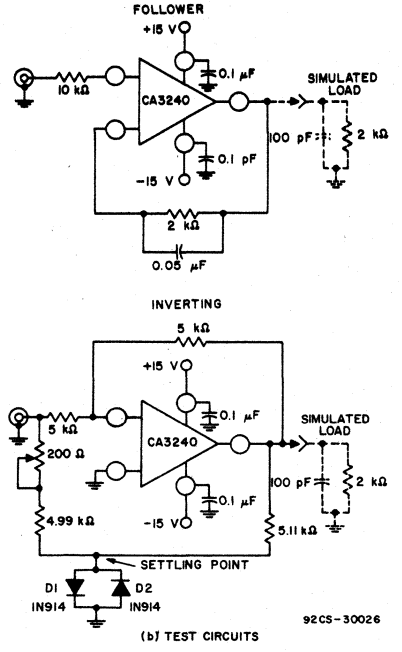


Fig. 17 — Input voltage as a function of settling time.

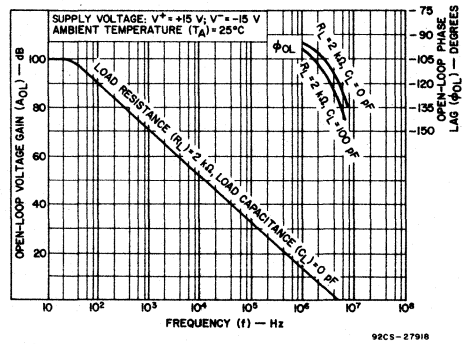
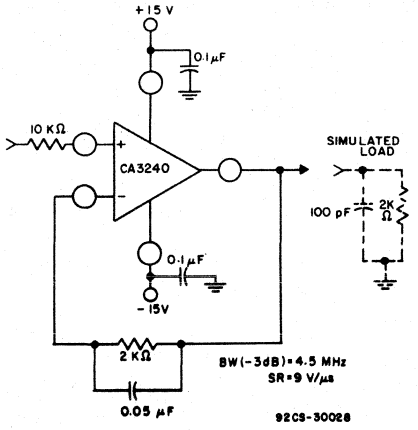
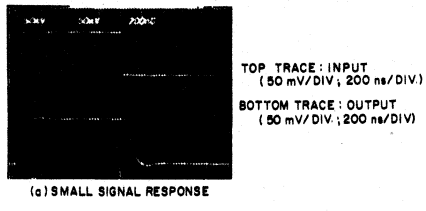


Fig. 19 — Open-loop voltage gain and phase lag as a function of frequency.





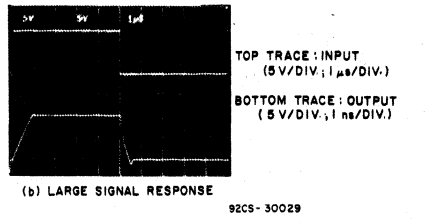


Fig. 20 – Split-supply voltage-follower test circuit and associated waveforms.

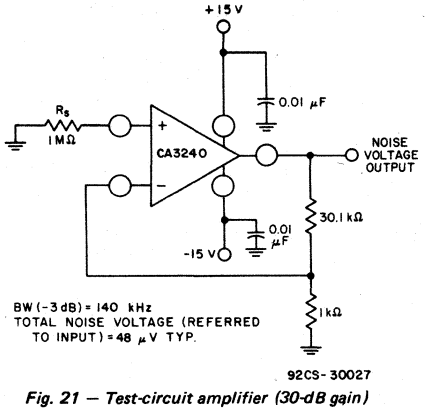


Fig. 21 – Test-circuit amplifier (30-dB gain) used for wideband noise measurement.

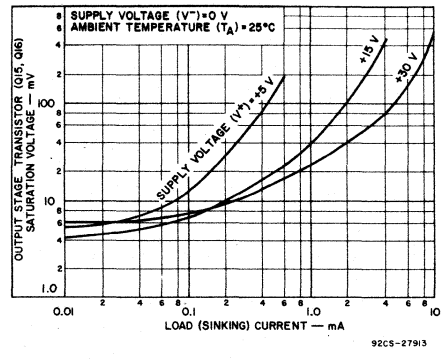


Fig. 22 – Voltage across output transistors Q15 and Q16 as a function of load current.

APPLICATIONS CONSIDERATIONS

Output Circuit Considerations

Fig. 22 shows output current-sinking capabilities of the CA3240 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

Fig. 23 shows some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

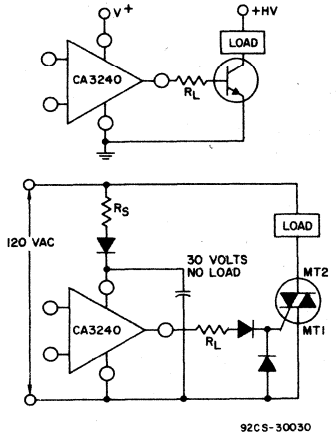


Fig. 23 – Methods of utilizing the $V_{CE}(sat)$ sinking-current capability of the CA3240 series.

Input Circuit Considerations

As indicated by the typical VICR, this device will accept inputs as low as 0.5 V below V^-. However, a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3240 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig. 24 shows typical input-terminal current versus ambient temperature for the CA3240.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

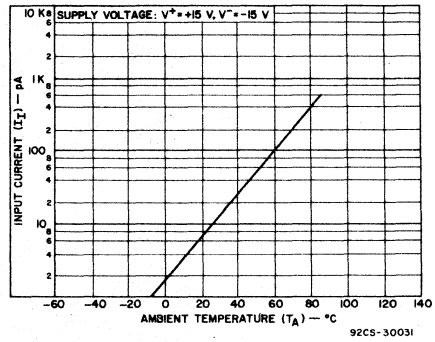


Fig. 24 – Input current as a function of ambient temperature.

Offset-Voltage Nulling

The input-offset voltage of the CA3240AE1 and CA3240E1 can be nulled by connecting a 10-kΩ potentiometer between Terminals 3 and 14 or 5 and 8 and returning its wiper arm to Terminal 4, see Fig. 25a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig. 25b, to optimize its utilization range are given in the table "Electrical Characteristics For Design Guidance" shown in this bulletin.

An alternate system is shown in Fig. 25c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

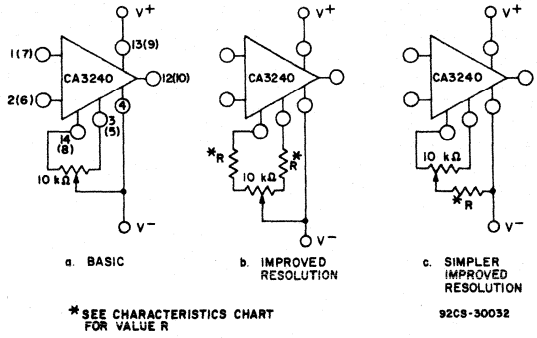


Fig. 25 – Three offset-voltage nulling methods. (CA3240AE1, CA3240E1 only.)

TYPICAL APPLICATIONS

On/Off Touch Switch

The on/off touch switch shown in Fig. 26 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the "on" plate is touched, current flows between the two halves of the grid causing a positive shift in the output voltage (Term. 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing triac driver. When a positive pulse occurs at Terminal 7 of the CA3240E, the triac is turned on and held on by the CA3059 and its associated positive feedback circuitry (51-kΩ resistor and 36-kΩ/42-kΩ voltage divider). When the positive pulse occurs at Terminal 1 (CA3240E), the triac is turned off and held off in a similar manner. Note that power for the CA3240E is supplied by the CA3059 internal power supply.

The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while allowing sufficiently high circuit impedance to provide protection against electrical shock.

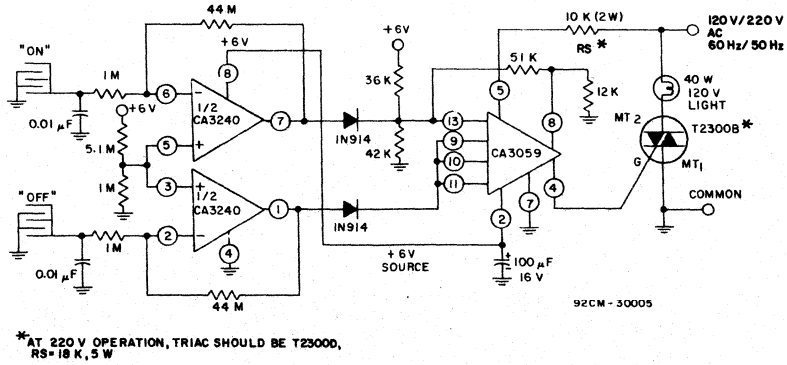


Fig. 26 – On/off touch switch.

CA3240, CA3240A Types

Dual Level Detector (window comparator)

Fig. 27 illustrates a simple dual liquid level detector using the CA3240E as the sensing amplifier. This circuit operates on the principle that most liquids contain enough ions in solution to sustain a small amount of current flow between two electrodes submersed in the liquid. The current, induced by an 0.5-V potential applied between two halves of a PC board grid, is converted to a voltage level by the CA3240E in a circuit similar to that of the on/off touch switch shown in Fig. 26. The changes in voltage for both the upper and lower level sensors are processed by the CA3140 to activate an LED whenever the liquid level is above the upper sensor or below the lower sensor.

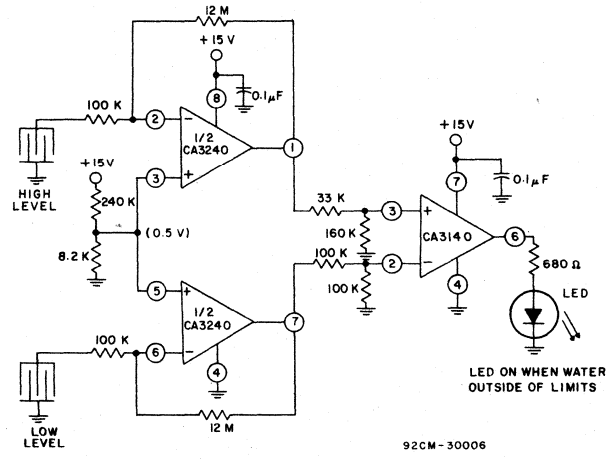


Fig. 27 – Dual level detector.

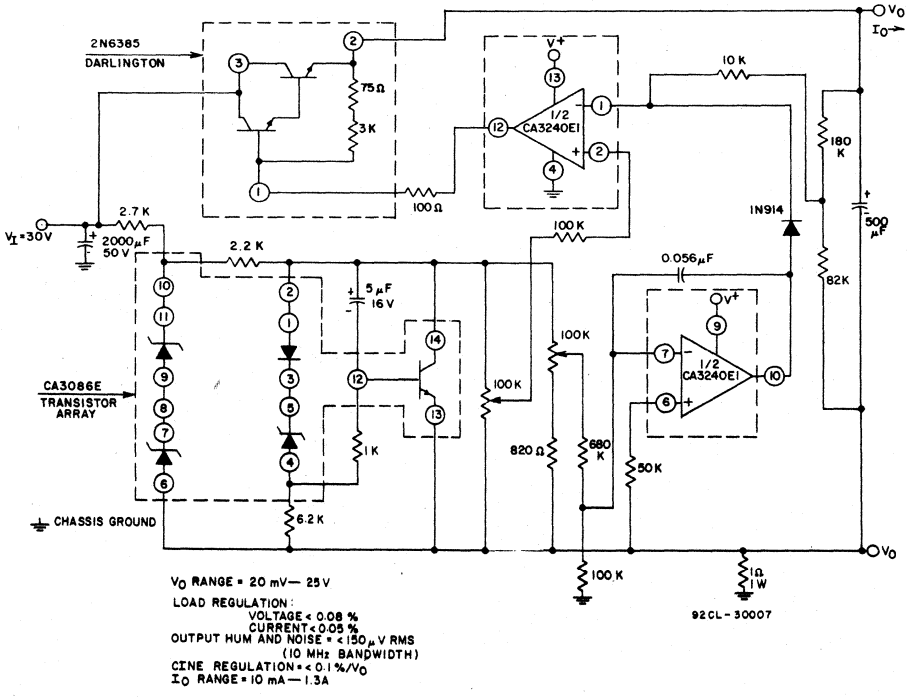


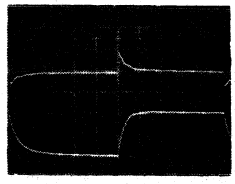
Fig. 28 – Constant-voltage/constant-current power supply.

Constant-Voltage/Constant-Current Power Supply

The constant-voltage/constant-current power supply shown in Fig. 28 uses the CA3240E as a voltage-error and current-sensing amplifier. The CA3240E is ideal for this application because its input common-mode voltage-range includes ground, allowing the supply to adjust from 20 mV to 25 V without requiring an additional negative input voltage. Also, the ground reference capability of the CA-3240E allows it to sense the voltage across the 1-Ω current-sensing resistor in the negative output lead of the power supply. The CA3086 transistor array functions as a reference for both constant-voltage and constant-current limiting. The 2N6385 power Darlington is used as the pass element and may be required to dissipate as much as 40 W. Fig. 29 shows the transient response of the supply during a 100-mA to 1-A load transition.

Precision Differential Amplifier

Fig. 30 shows the CA3240E in the classical precision differential amplifier circuit. The CA3240E is ideally suited for biomedical applications because of its extremely high input impedance. To insure patient safety, an extremely high electrode series resistance is required to limit any current that might result in patient discomfort in the event of a fault condition. In this case, 10-MΩ resistors have been used to limit the current to less than 2 μA without affecting the performance of the circuit. Fig. 31 shows a typical electrocardiogram waveform obtained with this circuit.



TRANSIENT RESPONSE

TOP TRACE : OUTPUT VOLTAGE
(500 mV/cm AND 5 μs/cm)
BOTTOM TRACE : COLLECTOR OF LOAD
SWITCHING TRANSISTOR
LOAD = 100 mA TO 1A
(5 V/cm AND 5 μs/cm)

92CS-30034

Fig. 29 – Transient response.

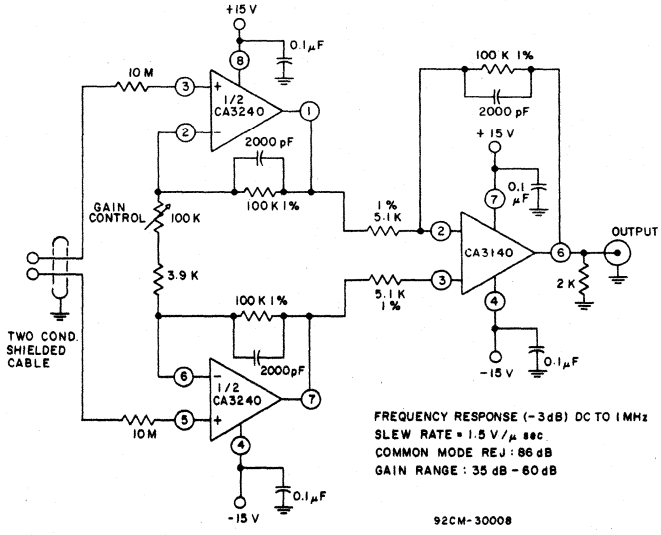
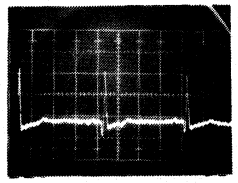


Fig. 30 – Precision differential amplifier.



TYPICAL ELECTROCARDIOGRAM WAVEFORM

VERTICAL : 1.0 mV/DIV.
(AMPLIFIER GAIN = 100 X)
(SCOPE SENSITIVITY = 0.1V/DIV.
HORIZONTAL : > 0.2 SEC/DIV (UNCAL)

92CS-30033

Fig. 31 – Typical electrocardiogram waveform.

Differential Light Detector

In the circuit shown in Fig. 32, the CA3240E converts the current from two photo diodes to voltage, and applies 1 V of reverse bias to the diodes. The voltages from the CA3240E outputs are subtracted in the second stage (CA3140) so that only the difference is amplified. In this manner, the circuit can be used over a wide range of ambient light conditions without circuit component adjustment. Also, when used with a light source, the circuit will not be sensitive to changes in light level as the source ages.

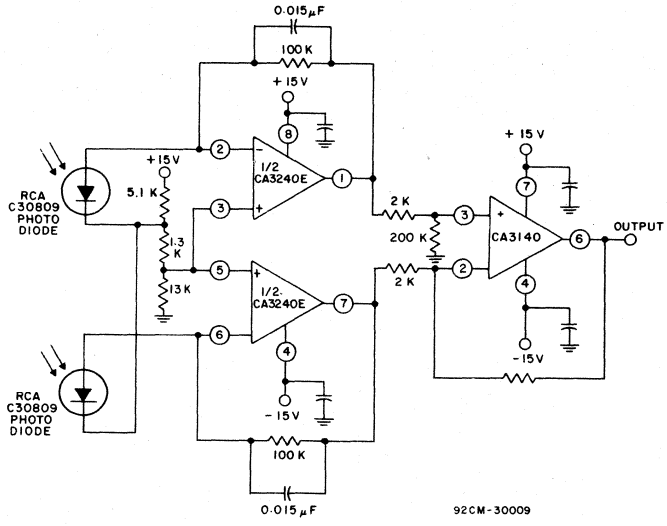
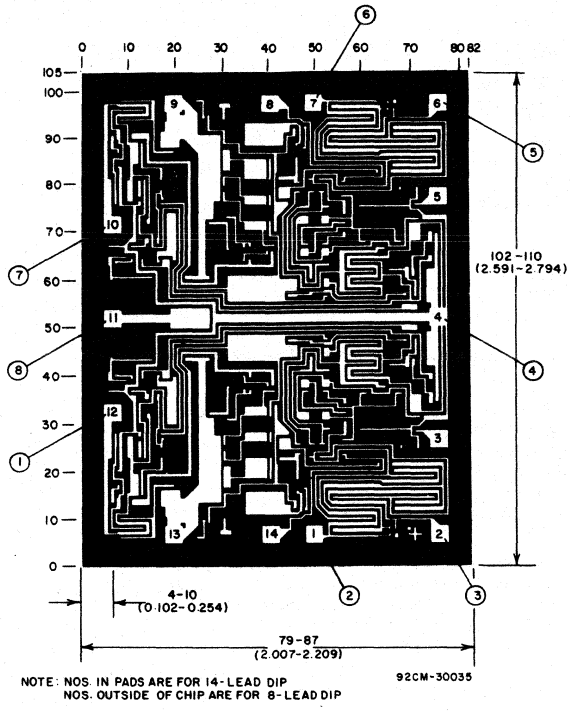


Fig. 32 – Differential light detector.

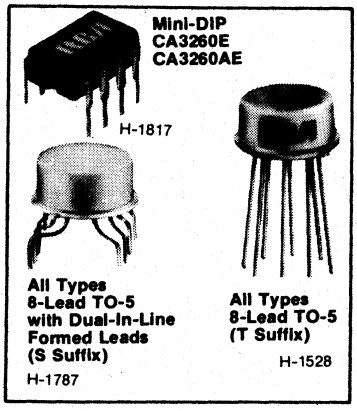
CA3240H Dimensions and Pad Layout



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57^{o} instead of 90^{o} with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3260, CA3260A, CA3260B Types



BiMOS Operational Amplifiers

With MOS/FET Input, COS/MOS Output

FEATURES:

- *Dual version of the CA3160*
- *MOS/FET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 × 10^{12}Ω) typ.
  very low II = 5 pA typ. at 15-V operation
  = 2 pA typ. at 5-V operation
- *Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *COS/MOS output stage permits signal swing to either (or both) supply rails*

} *Ideal for single-supply applications*

- *Low V_{IO}: 2 mV max. (CA3260B)*
  Wide BW: 4 MHz typ. (unity-gain crossover)
  High SR: 10 V/μs typ. (unity-gain follower)
  High output current (I_O): 20 mA typ.
- *High A_{OL}: 320,000 (110 dB) typ.*
- *Internal phase compensation for unity gain.*
- *Same pin-out as CA1458, CA1558*

APPLICATIONS:

- *Ground-referenced single-supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *Ideal interface with digital COS/MOS*
- *High-input-impedance wideband amplifiers*
- *Voltage followers*
  (e.g., follower for single-supply D/A converter)
- *Voltage regulators*
  (permits control of output voltage down to zero volts)
- *Wien-Bridge oscillators*
- *Voltage-controlled oscillators*
- *Photo-diode sensor amplifiers*

The RCA-CA3260T, CA3260S, CA3260E; CA3260AT, CA3260AS, CA3260AE; and CA3260BT, CA3260BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip. The CA3260 series circuits are dual versions of the popular CA3160 series.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3260-series circuits operate at supply voltages ranging from 4 to 16 volts, or ±2 to ±8 volts when using split supplies.

The CA3260 series is supplied in standard 8-lead TO-5-style packages (T suffix) and 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" packages (S suffix). The CA3260 is available in chip form (H suffix).

The CA3260A and CA3260 are also available in the 8-lead dual-in-line plastic package (Mini-DIP E suffix). All types operate over the full military-temperature range of -55° C to +125° C. The CA3260B is intended for applications requiring premium-grade specifications. The CA3260A offers superior input characteristics over those of the CA3260.

ELECTRICAL CHARACTERISTICS for Each Amplifier at T_A=25°C, V^+=15 V, V^-=0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS									UNITS
	CA3260B (T,S)			CA3260A (T,S,E)			CA3260 (T,S,E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\lvert V_{IO} \rvert$, $V^{\pm}$=±7.5 V	—	0.8	2	—	2	5	—	6	15	mV
Input Offset Current, $\lvert I_{IO} \rvert$, $V^{\pm}$=±7.5 V	—	0.5	10	—	0.5	20	—	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	—	5	20	—	5	30	—	5	50	pA
Large-Signal Voltage Gain, A_{OL}	100 k	320 k	—	50 k	320 k	—	50 k	320 k	—	V/V
V_O=10 V_{p-p}, R_L=10 kΩ	100	110	—	94	110	—	94	110	—	dB
Common-Mode Rejection Ratio, CMRR	86	100	—	80	95	—	70	90	—	dB
Common-Mode Input Voltage Range, V_{ICR}	0	0.5 to 12	10	0	0.5 to 12	10	0	0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	—	32	100	—	32	150	—	32	320	μV/V
Maximum Output Voltage:										
At R_L=10 kΩ V_{OM}^+	11	13.3	—	11	13.3	—	11	13.3	—	V
At R_L=10 kΩ V_{OM}^-	—	0.002	0.01	—	0.002	0.01	—	0.002	0.01	V
At R_L=∞ V_{OM}^+	14.99	15	—	14.99	15	—	14.99	15	—	V
At R_L=∞ V_{OM}^-	—	0	0.01	—	0	0.01	—	0	0.01	V
Maximum Output Current, I_{OM}^+ (Source) @ V_O=7.5 V	12	22	45	12	22	45	12	22	45	mA
I_{OM} (Sink) @ V_O=7.5 V	12	20	45	12	20	45	12	20	45	mA
Total Supply Current, I^+ R_L=∞										
V_O(Ampli.A)=V_O (Ampli.B)=7.5 V	—	9	15.5	—	9	15.5	—	9	15.5	mA
V_O (Ampli.A)=V_O (Ampli.B)=0 V	—	1.2	3	—	1.2	3	—	1.2	3	mA
V_O (Ampli.A)=0 V V_O(Ampli.B)=7.5 V	—	5	8.5	—	5	8.5	—	5	8.5	mA
Input Offset Voltage Temp.Drift, $\Delta V_{IO}/\Delta T$	—	5	—	—	6	—	—	8	—	μV/°C
Crosstalk f=1 kHz	—	120	—	—	120	—	—	120	—	dB

CA3260, CA3260A, CA3260B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals)..... 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE..... ±8 V
COMMON-MODE DC
INPUT VOLTAGE..... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK —
UP TO 55°C..... 630 mW
ABOVE 55°C ... Derate linearly 6.67 mW/°C
WITH HEAT SINK —
UP TO 90°C..... 1 W
ABOVE 90°C ... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING (All Types) ..... −55 to +125°C
STORAGE (All Types) ..... −65 to +150°C
OUTPUT SHORT-CIRCUIT
DURATION*..... INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
At distance 1/16 ± 1/32 in.
(1.59 ± 0.79 mm) from case
for 10 s max. ..... +265°C

*Short circuit may be applied to ground or to either supply.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS	CA3260 (T, S)	CA3260 (T, S, E)	CA3260 (T, S, E)	UNITS
V^+=+7.5 V, V^-=−7.5 V, T_A=25°C (Unless Otherwise Specified)					
Input Resistance, R_I		1.5	1.5	1.5	TΩ
Input Capacitance, C_I	f=1 MHz	4.3	4.3	4.3	pF
Unity Gain Crossover Frequency, f_T		4	4	4	MHz
Slew Rate, SR		10	10	10	V/μs
Transient Response: Rise Time, t_r	C_L=25 pF, R_L=2 kΩ (Voltage Follower)	0.09	0.09	0.09	μs
Overshoot		10	10	10	%
Settling Time (4 V_{p-p} Input to < 0.1%)		1.8	1.8	1.8	μs
V^+=5 V, V^-=0 V, T_A=25°C (Unless Otherwise Specified)					
Input Offset Voltage, V_{IO}		1	2	6	mV
Input Offset Current, I_{IO}		0.1	0.1	0.1	pA
Input Current, I_I		2	2	2	pA
Common-Mode Rejection Ratio, CMRR		80	70	60	dB
Large-Signal Voltage Gain, A_{OL}	V_O=4 V_{p-p}, R_L=20 kΩ	100 k 100	100 k 100	100 k 100	V/V dB
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.5	0 to 2.5	0 to 2.5	V
Supply Current, I^+	V_O=5 V, R_L=∞	1	1	1	mA
	V_O=2.5 V, R_L=∞	1.2	1.2	1.2	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	200	μV/V

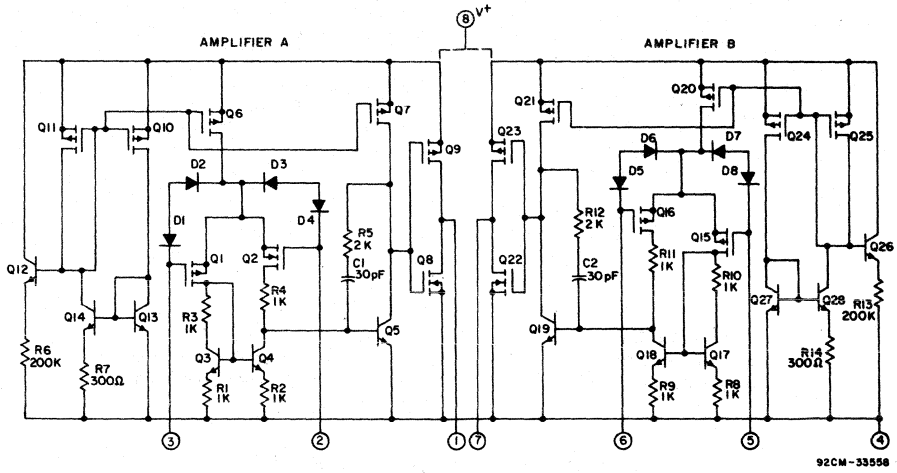
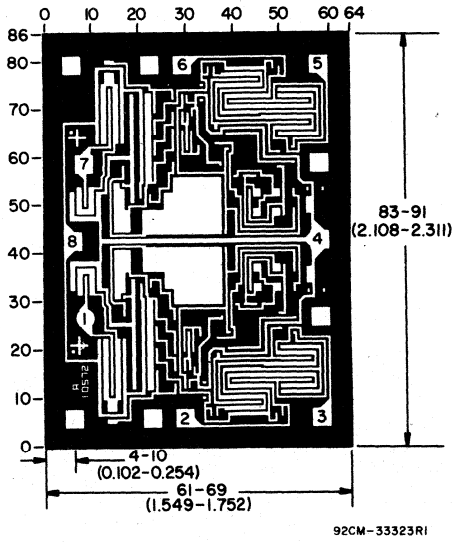


Fig. 1 - Schematic diagram of CA3260 series.

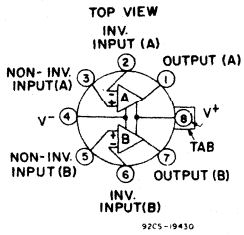


Dimensions and pad layout for CA3260H.

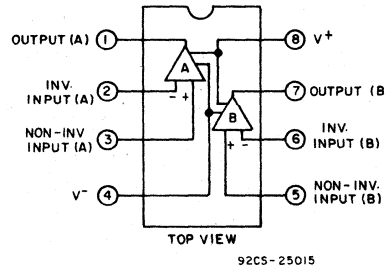
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3260, CA3260A, CA3260B Types



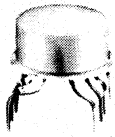
S and T Suffixes
Pin compatible with the industry-standard 1458



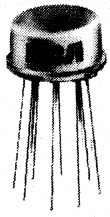
E Suffix
Pin compatible with the industry-standard 1458

Fig. 2 - Functional diagrams for the CA3260 Series.

CA3094, CA3094A, CA3094B Types



S-Suffix Types
8-LEAD TO-5
with Dual-In-Line
Formed Leads
"DIL-CAN"
H-1787



T-Suffix Types
8-LEAD TO-5
H-1528

H-1817

CA3094E
8-LEAD DUAL
IN-LINE PLASTIC
PACKAGE
"MINI-DIP"

Programmable Power Switch/Amplifier

For Control & General-Purpose Applications

CA3094T,S,E:	For Operation Up to 24 Volts
CA3094AT,S,E:	For Operation Up to 36 Volts
CA3094BT,S:	For Operation Up to 44 Volts

Features:

- *Designed for single or dual power supply*
- *Programmable: strobing, gating, squelching, AGC capabilities*
- *Can deliver 3 watts (avg.) or 10 W (peak) to external load (in switching mode)*
- *High-power, single-ended class A amplifier will deliver power output of 0.6 watt [1.6 W device dissipation]*
- *Total harmonic distortion [THD] @ 0.6 W in class A operation - 1.4% typ.*
- *High current-handling capability - 100 mA (avg.), 300 mA (peak)*
- *Sensitivity controlled by varying bias current*
- *Output: "sink" or "drive" capability*

Applications:

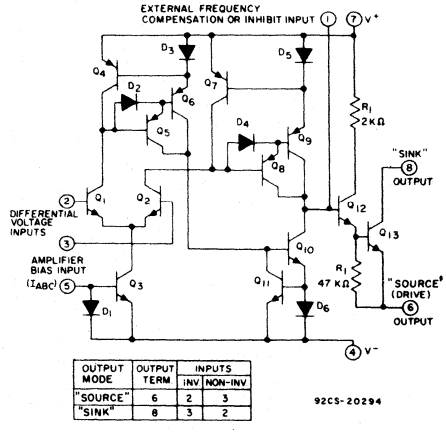
- *Error-signal detector: temperature control with thermistor sensor; speed control for shunt wound dc motor*
- *Over-current, over-voltage, over-temperature protectors*
- *Dual-tracking power supply with RCA-CA3085*
- *Wide-frequency-range oscillator*
- *Analog timer*
- *Level detector*
- *Alarm systems*
- *Voltage follower*
- *Ramp-voltage generator*
- *High-power comparator*
- *Ground-fault interrupter [GFI] circuits*

The CA3094 is a differential-input power-control switch/amplifier with auxiliary circuit features for ease of programmability. For example, an error or unbalance signal can be amplified by the CA3094 to provide an on-off signal or proportional-control output signal up to 100 mA. This signal is sufficient to directly drive high-current thyristors, relays, dc loads, or power transitors. The CA3094 has the generic characteristics of the RCA-CA3080 operational amplifier directly coupled to an integral Darlington power transistor capable of sinking or driving currents up to 100 mA.

The gain of the differential input stage is proportional to the amplifier bias current (I_{ABC}), permitting programmable variation of the integrated circuit sensitivity with either digital and/or analog programming signals. For example, at an I_{ABC} of 100 μA, a one-millivolt change at the input will change the output from 0 to 100 mA (typical).

The CA3094 is intended for operation up to 24 volts and is especially useful for timing circuits, in automotive equipment, and in other applications where operation up to 24 volts is a primary design requirement (see Figs. 28, 29 and 30 in Applications Section). The CA3094A and CA3094B are like the CA3094 but are intended for operation up to 36 and 44 volts, respectively (single or dual supply).

These types are available in 8-lead TO-5 style packages with standard leads ("T" suffix) and with dual-in-line formed leads "DIL-CAN" ("S" suffix). Type CA3094 is also available in an 8-lead dual-in-line plastic package "MINI-DIP" ("E" suffix), and in chip form ("H" suffix).



OUTPUT MODE	OUTPUT TERM	INPUTS	
		INV	NON-INV
"SOURCE"	6	2	3
"SINK"	8	3	2

Fig. 1 — Schematic diagram of CA3094.

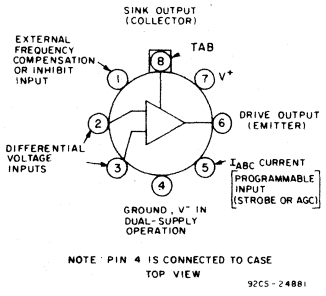
CA3094, CA3094A, CA3094B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

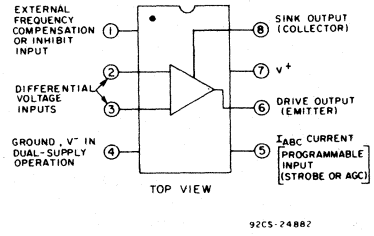
	CA3094	CA3094A	CA3094B	
DC SUPPLY VOLTAGE:				
Dual Supply	± 12 V	± 18 V	± 22 V	V
Single Supply	24 V	36 V	44 V	V
DC DIFFERENTIAL INPUT VOLTAGE (Terminals 2 and 3)	± 5*			V
DC COMMON-MODE INPUT VOLTAGE	Term. 4 ⩽ Term. 2 & 3 ⩽ Term. 7			
PEAK INPUT SIGNAL CURRENT (Terminals 2 and 3)	± 1			mA
PEAK AMPLIFIER BIAS CURRENT (Terminal 5)	2			mA
OUTPUT CURRENT:				
Peak	300			mA
Average	100			mA
DEVICE DISSIPATION:				
Up to T_A = 55°C:				
Without heat sink	630			mW
With heat sink	1.6			W
Above T_A = 55°C:				
Without heat sink derate linearly	6.67			mW/°C
With heat sink derate linearly	16.7			mW/°C
THERMAL RESISTANCE (Junction to Air)	140			°C/W
AMBIENT TEMPERATURE RANGE:				
Operating	−55 to +125			°C
Storage	−65 to +150			°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 300			°C

*Exceeding this voltage rating will not damage the device unless the peak input signal current (1 mA) is also exceeded.

FUNCTIONAL DIAGRAMS



TO-5 Style Package



Plastic Package

TYPICAL CHARACTERISTICS CURVES

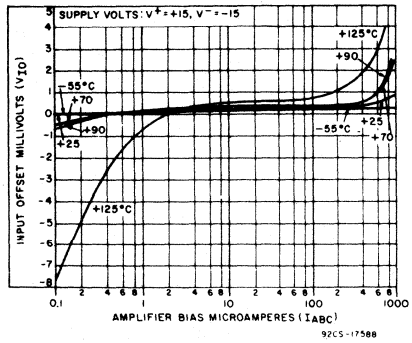


Fig.2 – Input offset voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

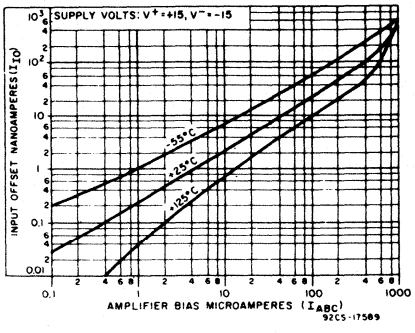


Fig.3 – Input offset current vs. amplifier bias current (I_{ABC}, terminal No.5).

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

CHARACTERISTIC	TEST CONDITIONS: Single Supply V^+ = 30 V, Dual Supply V^+ = 15 V, V^- = 15 V, I_{ABC} = 100 μA Unless Otherwise Specified	LIMITS: Min.	Typ.	Max.	UNITS
INPUT PARAMETERS					
Input Offset Voltage V_{IO}	T_A = 25°C	–	0.4	5	mV
	T_A = 0 to 70°C	–	–	7	mV
Input-Offset-Voltage Change $\lvert\Delta V_{IO}\rvert$	Change in V_{IO} Between I_{ABC} = 100 μA and I_{ABC} = 5 μA	–	1	8	mV
Input Offset Current I_{IO}	T_A = 25°C	–	0.02	0.2	μA
	T_A = 0 to 70°C	–	–	0.3	μA
Input Bias Current I_I	T_A = 25°C	–	0.2	0.50	μA
	T_A = 0 to 70°C	–	–	0.70	μA
Device Dissipation P_D	I_{out} = 0	8	10	12	mW
Common-Mode Rejection Ratio CMRR		70	110	–	dB
Common-Mode Input–Voltage Range V_{ICR}	V^+ = 30 V, High	27	28.8	–	V
	V^+ = 30 V, Low	1.0	0.5	–	V
	V^+ = 15 V	+12	+13.8	–	V
	V^- = 15 V	–14	–14.5	–	V
Unity Gain-Bandwidth	I_C = 7.5 mA, V_{CE} = 15 V, I_{ABC} = 500 μA	–	30	–	MHz
Open-Loop Bandwidth At –3 dB Point BW_{OL}	I_C = 7.5 mA, V_{CE} = 15 V, I_{ABC} = 500 μA	–	4	–	kHz
Total Harmonic Distortion (Class A Operation) THD	P_D = 220 mW	–	0.4	–	%
	P_D = 600 mW	–	1.4	–	
Amplifier Bias Voltage V_{ABC} (Terminal (No.5 to Terminal No.4)		–	0.68	–	V
Input Offset Voltage Temperature Coefficient $\Delta V_{IO}/\Delta T$		–	4	–	μV/°C
Power-Supply Rejection $\Delta V_{IO}/\Delta V$		–	15	150	μV/V
1/F Noise Voltage E_N	f = 10 Hz, I_{ABC} = 50 μA	–	18	–	$\eta V/\sqrt{Hz}$
1/F Noise Current I_N	f = 10 Hz, I_{ABC} = 50 μA	–	1.8	–	$pA/\sqrt{Hz}$
Differential Input Resistance R_I	I_{ABC} = 20 μA	0.50	1	–	MΩ
Differential Input Capacitance C_I	f = 1 MHz, V^+ = 30 V	–	2.6	–	pF

CA3094, CA3094A, CA3094B Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
	Single Supply V^+ = 30 V Dual Supply V^+ = 15 V, V^- = 15 V I_{ABC} = 100 μA Unless Otherwise Specified	Min.	Typ.	Max.	
OUTPUT PARAMETERS (Differential Input Voltage = 1V)					
Peak Output Voltage: (Terminal No. 6) With Q13 "ON" V^+_{OM} With Q13 "OFF" V_{OM}^-	V^+ = 30 V R_L = 2 kΩ to ground	 26 –	 27 0.01	 – 0.05	 V V
Peak Output Voltage: (Terminal No. 6) Positive V^+_{OM} Negative V_{OM}^-	V^+ = +15 V, V^- = -15 V R_L = 2 kΩ to −15 V	 +11 –	 +12 −14.99	0.5 – −14.95	 V V
Peak Output Voltage: (Terminal No. 8) With Q13 "ON" V^+_{OM} With Q13 "OFF" V_{OM}^-	V^+ = 30 V R_L = 2 kΩ to 30 V	 29.95 –	 29.99 0.040	 – –	 V V
Peak Output Voltage: (Terminal No. 8) Positive V^+_{OM} Negative V_{OM}^-	V^+ = 15 V, V^- = − 15 V R_L = 2 kΩ to + 15 V	 +14.95 –	 +14.99 14.96	 – –	 V V
Collector-to-Emitter Saturation Voltage (Terminal No. 8) $V_{CE(sat)}$	V^+ = 30 V I_C = 50 mA Terminal No.6 grounded	–	0.17	0.80	V
Output Leakage Current (Terminal No. 6 to Terminal No. 4)	V^+ = 30 V	–	2	10	μA
Composite Small-Signal Current Transfer Ratio (Beta) (Q_{12} and Q_{13}) h_{fe}	V^+ = 30 V V_{CE} = 5 V I_C = 50 mA	16,000	100,000	–	
Output Capacitance: Terminal No. 6 Terminal No. 8 C_O	f = 1 MHz All Remaining Terminals Tied to Terminal No. 4	 – –	 5.5 17	 – –	 pF pF
TRANSFER PARAMETERS					
Voltage Gain A	V^+ = 30 V I_{ABC} = 100 μA ΔV_{out} = 20 V R_L = 2 kΩ	20,000 86	100,000 100	– –	V/V dB
Forward Transconductance To Terminal No. 1 g_m		1650	2200	2750	μmhos
Slew Rate: Open Loop: Positive Slope Negative Slope	 I_{ABC} = 500 μA R_L = 2 kΩ	 – –	 500 50	 – –	 V/μs V/μs
Unity Gain (Non-Inverting, Compensated)	I_{ABC} = 500 μA R_L = 2 kΩ	–	0.7	–	V/μs

TYPICAL CHARACTERISTICS CURVES (Cont'd)

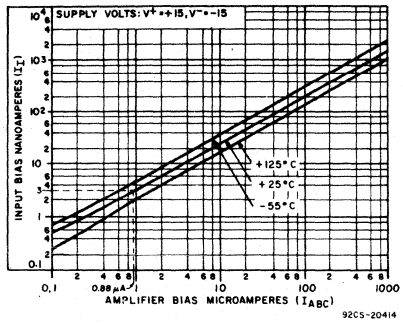


Fig.4 – Input bias current vs. amplifier bias current (I_{ABC}, terminal No.5).

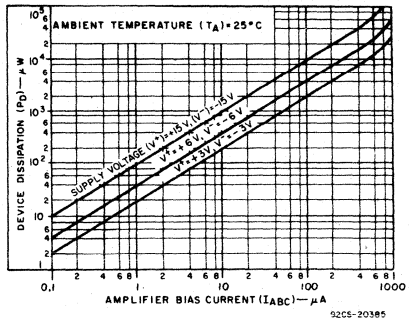


Fig.5 – Device dissipation vs. amplifier bias current (I_{ABC}, terminal No.5).

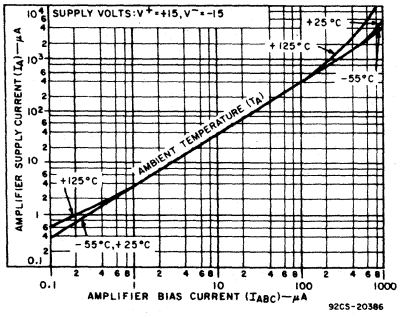


Fig.6 – Amplifier supply current vs. amplifier bias current (I_{ABC}, terminal No.5).

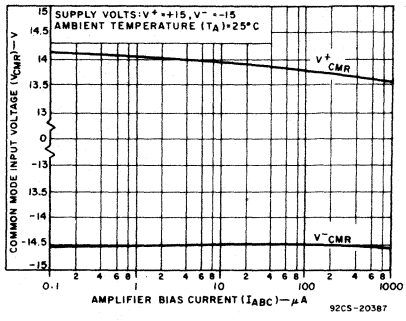


Fig.7 – Common mode input voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

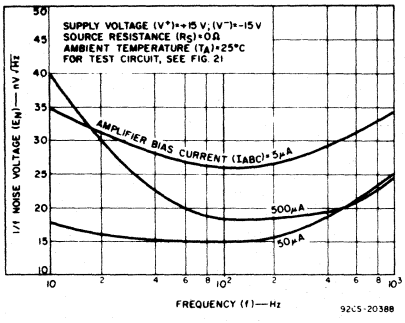


Fig.8 – 1/F Noise voltage vs. frequency.

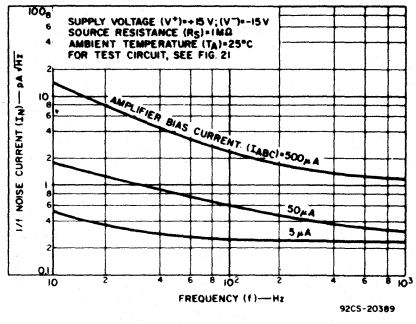


Fig.9 – 1/F Noise current vs. frequency.

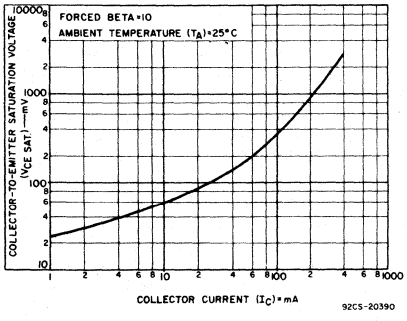


Fig.10 – Collector-emitter saturation voltage vs. collector current of output transistor Q_{13}.

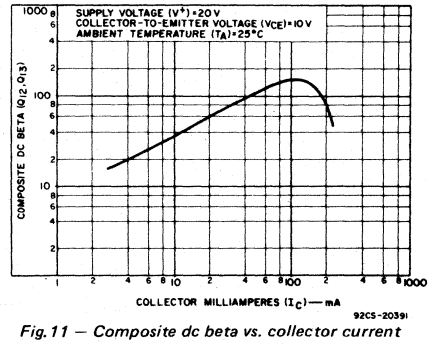


Fig.11 – Composite dc beta vs. collector current of Darlington-connected output transistors (Q_{12}, Q_{13}).

CA3094, CA3094A, CA3094B Types

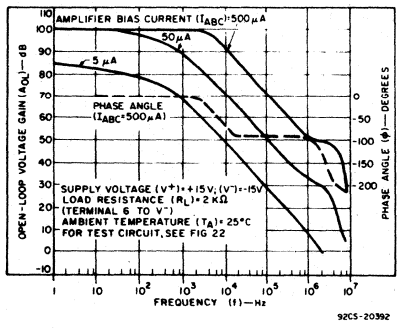


Fig. 12 – Open-loop voltage gain vs. frequency.

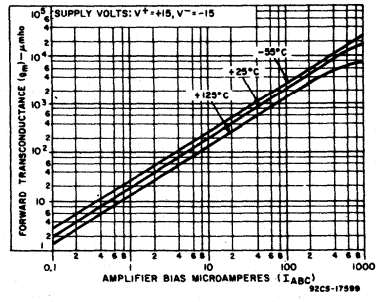


Fig. 13 – Forward transconductance vs amplifier bias current.

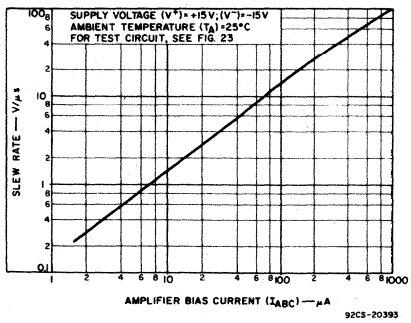


Fig. 14 – Slew rate vs amplifier bias current.

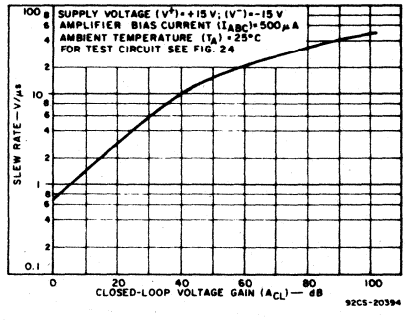


Fig. 15 – Slew rate vs closed-loop voltage gain.

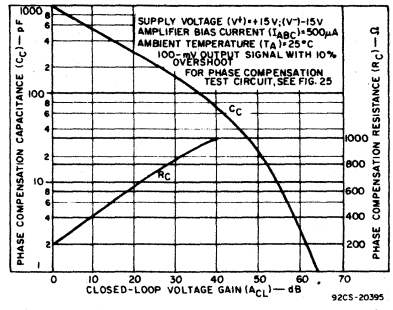


Fig. 16 – Phase compensation capacitance and resistance vs closed-loop voltage gain.

OPERATING CONSIDERATIONS

The "Sink" Output (terminal No.8) and the "Drive" Output (terminal No.6) of the CA3094 are not inherently current (or power) limited. Therefore, if a load is connected between terminal No.6 and terminal No.4 (V^- or ground), it is important to connect a current-limiting resistor between terminal 8 and terminal No.7 (V^+) to protect transistor Q_{13} under shorted load conditions. Similarly, if a load is connected between terminal No.8 and terminal No.7, the current-limiting resistor should be connected between terminal No.6 and terminal No.4 or ground. In circuit applications where the emitter of the output transistor is not connected to the most negative potential in the system, it is recommended that a 100-ohm current-limiting resistor be inserted between terminal No.7 and the V^+ supply.

TEST CIRCUITS

I/F Noise Measurement Circuit

When using the CA3094, A, or B audio amplifier circuits, it is frequently necessary to consider the noise performance of the device. Noise measurements are made in the circuit shown in Fig.21. This circuit is a 30-dB, non-inverting amplifier with emitter-follower output and phase compensation from terminal No.2 to ground. Source resistors (Rs) are set to 0.Ω or 1 MΩ for E noise and I noise measurements, respectively. These measurements are made at frequencies of 10, Hz, 100 Hz, and 1 kHz with a 1-Hz measurement bandwidth. Typical values for 1/f noise at 10 Hz and 50 μA I_{ABC} are E_n = 18 nV/$\sqrt{Hz}$ and I_N = 1.8 pA/$\sqrt{Hz}$.

TEST CIRCUITS

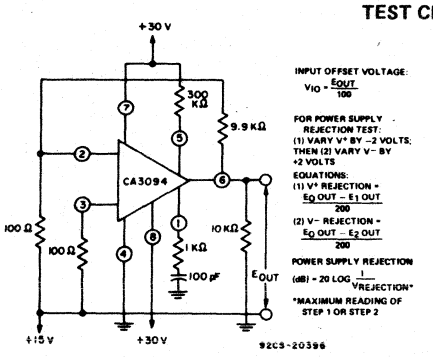


Fig. 17 – Input offset voltage and power-supply rejection test circuit.

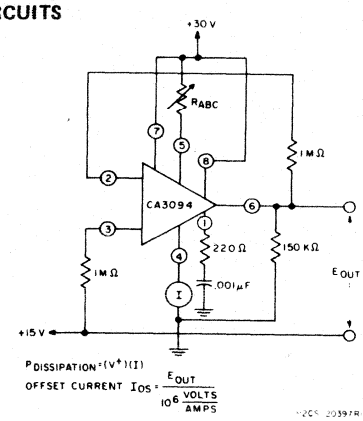


Fig. 18 – Input offset current test circuit.

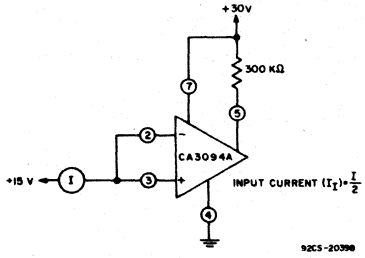


Fig. 19 – Input bias current test circuit.

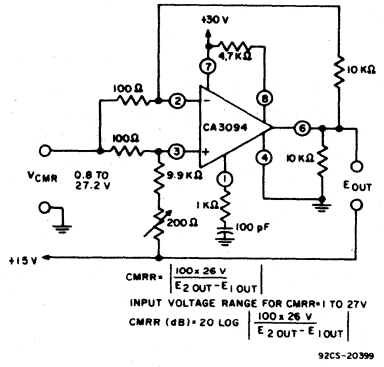


Fig. 20 – Common-mode range and rejection ratio test circuit.

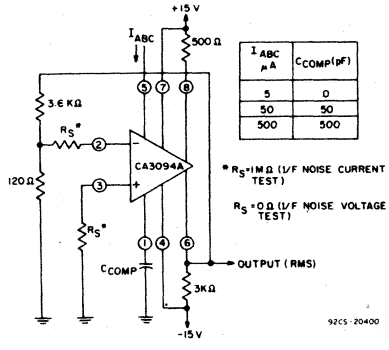


Fig. 21 – 1/F noise test circuit.

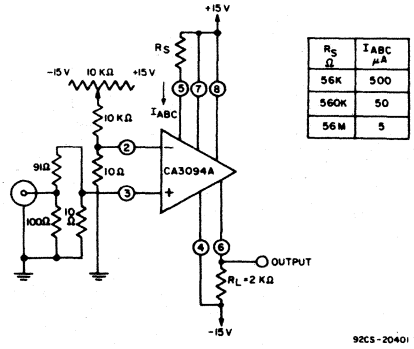


Fig. 22 – Open-loop gain vs frequency test circuit.

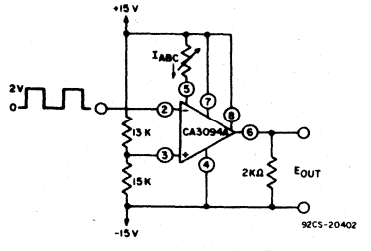


Fig. 23 – Open-loop slew rate vs I_{ABC} test circuit.

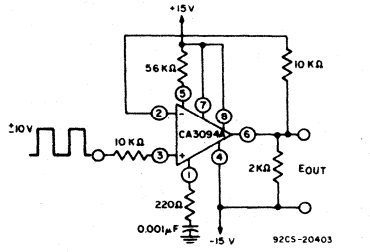
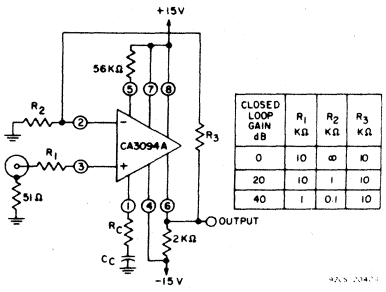


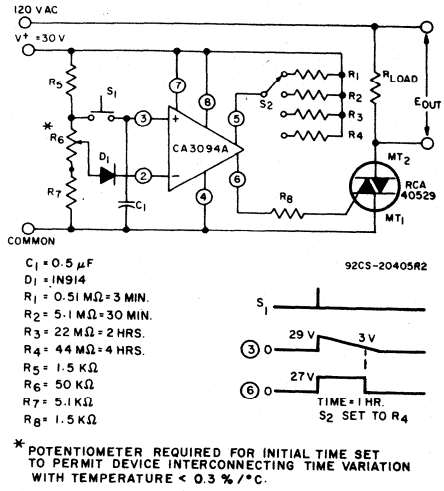
Fig. 24 – Slew rate vs. non-inverting unity gain test circuit.

TEST CIRCUITS (Cont'd)



CLOSED LOOP GAIN dB	R1 KΩ	R2 KΩ	R3 KΩ
0	10	∞	10
20	10	1	10
40	1	0.1	10

Fig.25 – Phase compensation test circuit.



* POTENTIOMETER REQUIRED FOR INITIAL TIME SET TO PERMIT DEVICE INTERCONNECTING TIME VARIATION WITH TEMPERATURE < 0.3 %/°C.

Fig.26 – Presettable analog timer.

TYPICAL APPLICATIONS

For Additional Application Information, refer to Application Note ICAN-6048 "Some Applications of a Programmable Power/ Switch Amplifier IC".

Design Considerations

The selection of the optimum amplifier bias current (I_{ABC}) depends on –

1. The Desired Sensitivity – the higher the I_{ABC}, the higher the sensitivity – i.e., a greater-drive current capability at the output for a specific voltage change at the input.
2. Required Input Resistance – the lower the I_{ABC}, the higher the input resistance.

If the desired sensitivity and requred input resistance are not known and are to be experimentally determined, or the anticipated equipment design is sufficiently flexible to tolerate a wide range of these parameters, it is recommended that the equipment designer begin his calculations with an I_{ABC} of 100 μA, since the CA3094 is characterized at this value of amplifier bias current.

The CA3094 is extremely versatile and can be used in a wide variety of applications.

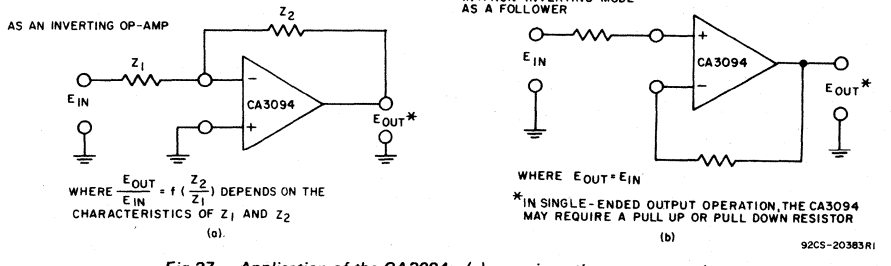
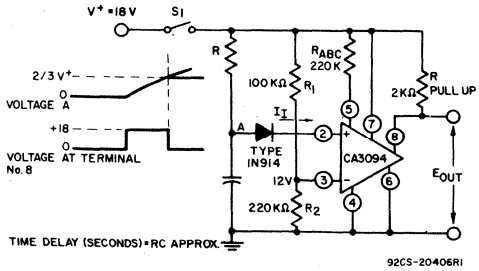


Fig.27 – Application of the CA3094: (a) as an inverting op-amp, and (b) in a non-inverting mode, as a follower.



Problem: To calculate the maximum value of R required to switch a 100-mA output current comparator

Given: $I_{ABC} = 5\ \mu A$, $R_{ABC} = 3.6\ M\Omega \approx \frac{18\ V}{5\ \mu A}$

$I_I = 500$ nA @ $I_{ABC} = 100\ \mu A$ (from Fig.4)

$I_I = 5\ \mu A$ can be determined by drawing a line on Fig.4 through $I_{ABC} = 100\ \mu A$ and $I_B = 500$ nA parallel to the typical $T_A = 25^oC$ curve.

Then: $I_I = 33$ nA @ $I_{ABC} = 5\ \mu A$

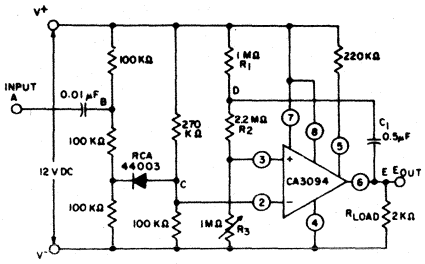
$$R_{max} = \frac{18-12\ volts}{33nA} = 180\ M\Omega\ @\ T_A = 25^oC$$

$$R_{max} = 180\ M\Omega \times 2/3^* = 120\ M\Omega\ @\ T_A = -55^oC$$

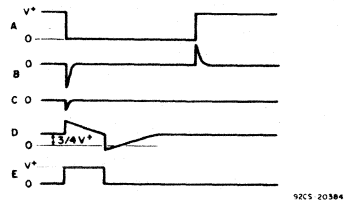
* Ratio of I_I at $T_A = +25^oC$ to I_I at $T_A = -55^oC$ for any given value of I_{ABC}.

Fig.28 – RC timer.

TYPICAL APPLICATIONS (Cont'd)



On a negative-going transient at input (A), a negative pulse at C will turn "on" the CA3094, and the output (E) will go from a low to a high level.



At the end of the time constant determined by C_1, R_1, R_2, R_3, the CA3094 will return to the "off" state and the output will be pulled low by R_{LOAD}. This condition will be independent of the interval when input A returns to a high level.

Fig.29 – RC timer triggered by external negative pulse.

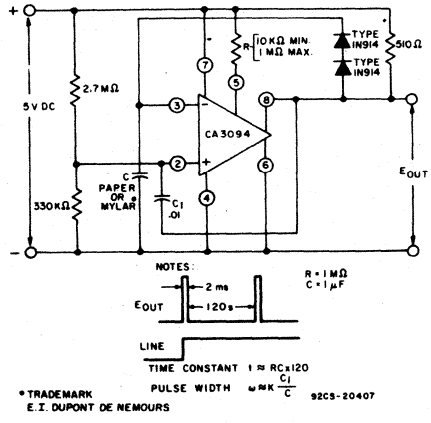


Fig.30 – Free-running pulse generator.

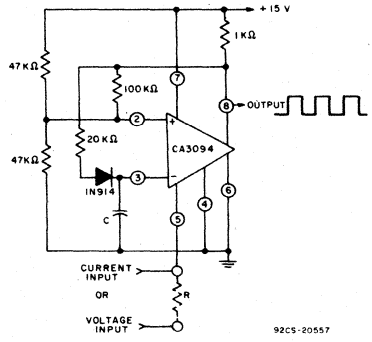


Fig.31 – Current or voltage-controlled oscillator.

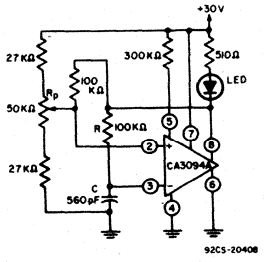


Fig.32 – Single-supply astable multivibrator.

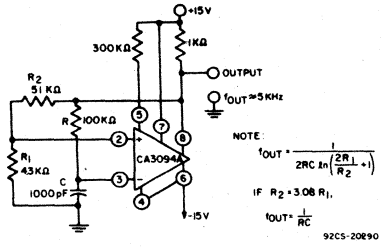
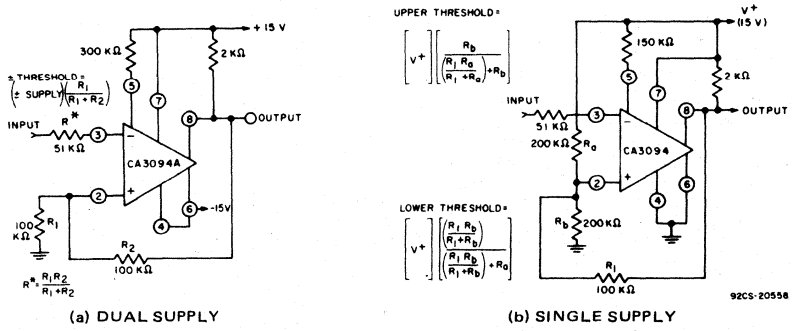


Fig.33 – Dual-supply astable multivibrator.

TYPICAL APPLICATIONS (Cont'd)



(a) DUAL SUPPLY (b) SINGLE SUPPLY

Fig.34 – Comparators (threshold detectors) –dual- and single-supply types.

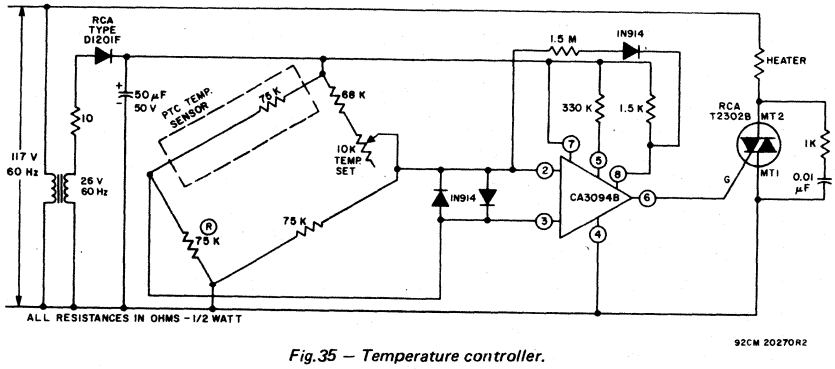


Fig.35 – Temperature controller.

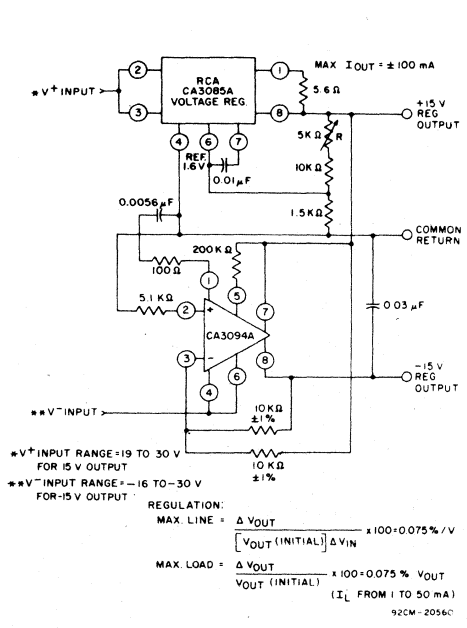


Fig.36 – Dual-voltage tracking regulator.

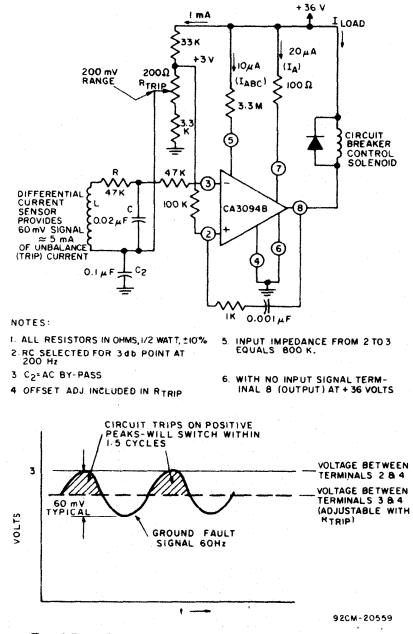
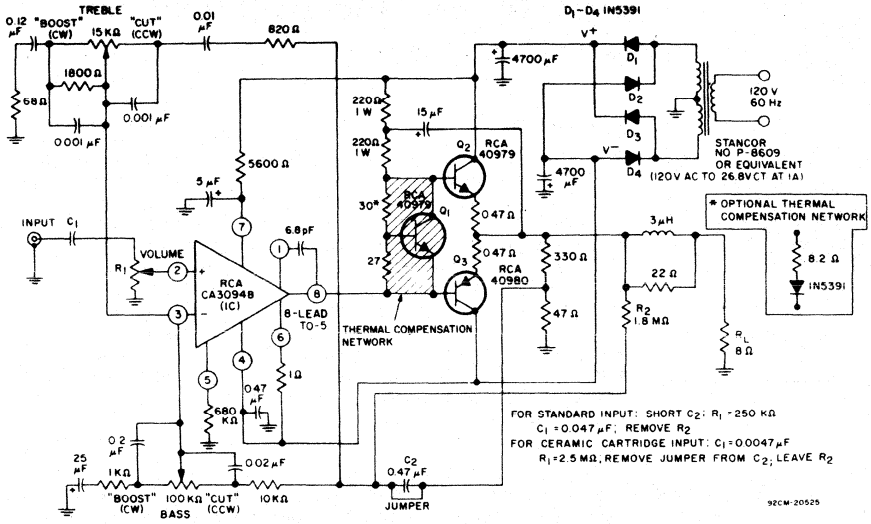


Fig.37 – Ground fault interrupter (GFI) and waveform pertinent to ground fault detector.

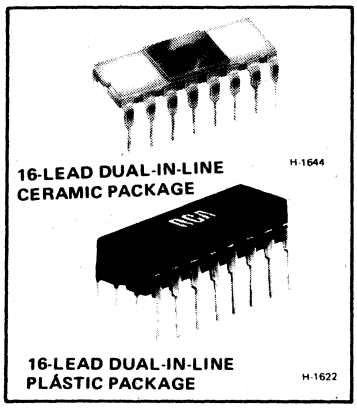


TYPICAL PERFORMANCE DATA
For 12-W Audio Amplifier Circuit

Power Output (8Ω load, Tone Control set at "Flat")		
Music (at 5% THD, regulated supply)	15	W
Continuous (at 0.2% IMD, 60 Hz & 2 kHz mixed in a 4:1 ratio, unregulated supply) See Fig. 8 In ICAN-6048	12	W
Total Harmonic Distoration		
At 1 W, unregulated supply	0.05	%
At 12 W, unregulated supply	0.57	%
Voltage Gain	40	dB
Hum and Noise (Below continuous Power Output)	83	dB
Input Resistance	250	kΩ
Tone Control Range	See Fig. 9 In ICAN-6048	

Fig.38 — 12-watt amplifier circuit featuring true complementary-symmetry output stage with CA3094 in driver stage.

CA3060, CA3060A Types



Operational Transconductance Amplifier Arrays

Features:

- *Low power consumption - as low as 100 μW per amplifier*
- *Independent biasing for each amplifier*
- *High forward transconductance*
- *Programmable range of input characteristics*
- *Low input bias and input offset current*
- *High input and output impedance*
- *No effect on device under output short-circuit conditions*
- *Zener diode bias regulator*

Applications:

- *For low power conventional operational amplifier applications*
- *Active filters*
- *Comparators*
- *Gyrators*
- *Mixers*
- *Modulators*
- *Multiplexers*
- *Multipliers*
- *Strobing and gating functions*
- *Sample and hold functions*

RCA-CA3060AD, CA3060BD, CA3060D, and CA3060E, monolithic integrated circuits, are arrays of three independent Operational Transconductance Amplifiers. This type of amplifier is a new circuit concept that has the generic characteristics of an operational voltage amplifier with the exception that the forward gain characteristic is best described by transconductance rather than voltage gain (open-loop voltage gain is the product of the transconductance and the load resistance, $g_m R_L$). When operated into a suitable load resistor and with provisions for feedback, these amplifiers are well suited for a wide variety of operational-amplifier and related applications. In addition, the extremely high output impedance makes these types particularly well suited for service in active filters.

The three amplifiers in the CA3060 family are identical push-pull Class A types which can be independently biased to achieve a wide range of characteristics for specific application. The electrical characteristics of each amplifier are a function of the amplifier bias current (I_{ABC}). This feature offers the system designer maximum flexibility with regard to output current capability, power consumption, slew rate, input resistance, input bias current, and input offset current. The linear variation of the parameters with respect to bias and the ability to maintain a constant dc level between input and output of each amplifier also makes the CA3060 suitable for a variety of non-linear applications such as mixers, multipliers, and modulators.

In addition; the types in the CA3060 family incorporate a unique Zener diode regulator system that permits current regulation below supply voltages normally associated with such systems.

Generic applications of the OTA are described in ICAN-6668, Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers.

The CA3060AD, CA3060BD, nd CA3060D are supplied in a hermetic 16-lead dual-in-line ceramic package which can be operated over the full military temperature range, −55° C to +125° C. The CA3060E is supplied in a 16-lead dual-in-line plastic package and is operational from −40° C to +85° C.

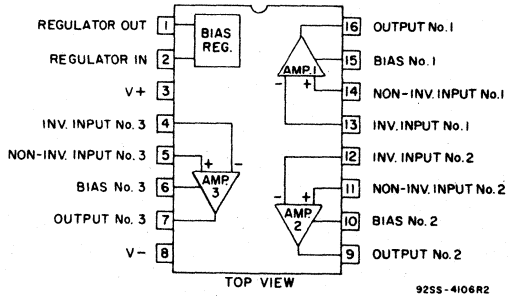


Fig. 1 — Functional block diagram for each type in the CA3060 family.

MAXIMUM RATINGS, *Absolute Maximum Values at T_A = 25°C*

DC Supply Voltage (between V^+ and V^- terminals):
CA3060AD, CA3060BD, CA3060E ..... 36V (±18V)
CA3060D ..... 14 V (±7V)

Differential Input Voltage (each amplifier):
CA3060AD, CA3060BD, CA3060E ..... ±5V
CA3060D ..... ±5V

DC Input Voltage ..... V^+ to V^-

Input Signal Current (each amplifier of each type): ..... ±1 mA

Amplifier Bias Current (each amplifier of each type) ..... 2 mA

Bias Regulator Input Current ..... -5 mA

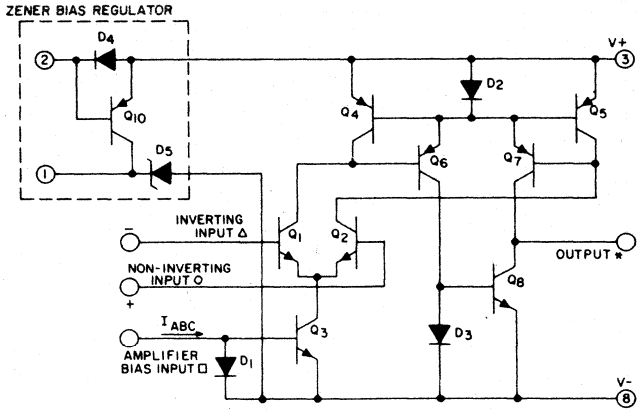
Output Short-Circuit Duration* ..... No limitation

Device Dissipation:
Total Package of each type up to T_A = 75°C ..... 490 mW
Above T_A = 75°C ..... Derate linearly 6.67 mW/°C

Temperature Range:
Operating –
CA3060AD, CA3060BD, CA3060D ..... -55 to +125°C
CA3060E ..... -40 to +85°C
Storage –
CA3060AD, CA3060BD, CA3060D,
CA3060E ..... -65 to +150°C

Lead Temperature (During Soldering):
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm)
from case for 10s max ..... +300°C

*Short circuit may be applied to ground or to either supply.



Δ INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 13, 12 AND 4, RESPECTIVELY
O NON-INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS TERMINAL Nos. 14, 11, AND 5, RESPECTIVELY
* OUTPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 16, 9, AND 7, RESPECTIVELY
□ AMPLIFIER BIAS CURRENT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 15, 10, AND 6, RESPECTIVELY

NOTE: A complete schematic diagram of the OTA is shown on Page 6. 92CS-15860RI

Fig.2—Simplified schematic diagram showing bias regulator and one operational transconductance amplifier for each type of the CA3060 family.

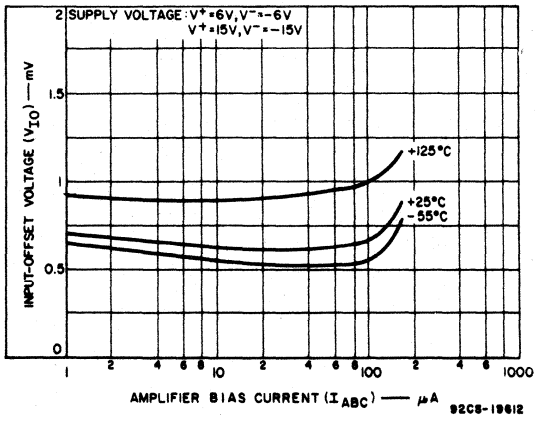


Fig.3—Input offset voltage vs. amplifier bias current.

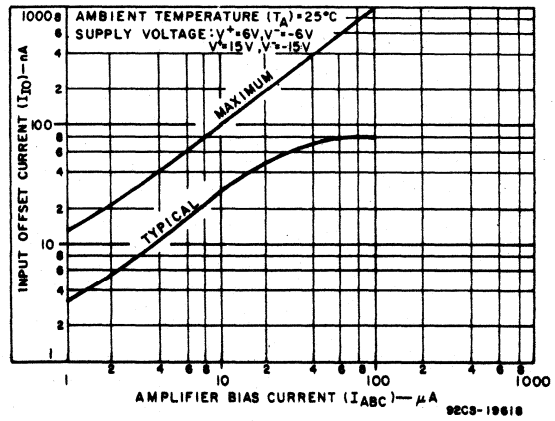


Fig.4—Input offset current vs. amplifier bias current.

CA3060, CA3060A Types

ELECTRICAL CHARACTERISTICS (CA3060D)

For each amplifier at T_A = 25°C, V^+ = 6 V, V^- = -6 V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVES Fig.	LIMITS — Amplifier Bias Current I_{ABC} = 1 μA MIN.	TYP.	MAX.	I_{ABC} = 10 μA MIN.	TYP.	MAX.	I_{ABC} = 100 μA MIN.	TYP.	MAX.	UNITS
STATIC CHARACTERISTICS												
Input Offset Voltage	V_{IO}	3	–	1	5	–	1	5	–	1	5	mV
Input Offset Current	I_{IO}	4	–	3	14	–	30	100	–	250	1000	nA
Input Bias Current	I_{IB}	5a, b	–	33	70	–	300	550	–	2500	5000	nA
Peak Output Current	I_{OM}	6a, b	1.3	2.3	–	15	26	–	150	240	–	μA
Peak Output Voltage: Positive	V_{OM^+}	7	4.6	5	–	4.5	4.8	–	4.5	4.7	–	V
Peak Output Voltage: Negative	V_{OM^-}	7	5.8	5.95	–	5.8	5.95	–	5.7	5.9	–	V
Amplifier Supply Current (each amplifier)	I_A	8a, b	–	8.5	14	–	85	120	–	850	1200	μA
Power Consumption (each amplifier)	P	–	–	0.10	0.17	–	1	1.45	–	10	14.5	mW
Input Offset-Voltage Sensitivity■: Positive	$\Delta V_{IO}/\Delta V^+$	–	–	1.5	120	–	2	120	–	2	120	μV/V
Input Offset-Voltage Sensitivity■: Negative	$\Delta V_{IO}/\Delta V^-$	–	–	20	120	–	20	120	–	30	120	μV/V
Amplifier Bias Voltage*	V_{ABC}	9	–	0.54	–	–	0.60	–	–	0.66	–	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)												
Forward Transconductance (large signal)	g_{21}	10a, b	0.3	1.55	–	3	18	–	30	102	–	mmho
Common-Mode Rejection Ratio	CMRR	–	70	110	–	70	110	–	70	90	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–	4.4 to -5.1 min. 4.7 to -5.3 typ.			4.3 to -5 min. 4.6 to -5.2 typ.			4.3 to -5 min. 4.6 to -5.2 typ.			V
Slew Rate (Test ckt., Fig. 13	SR		–	0.1	–	–	1	–	–	8	–	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	–	20	–	–	45	–	–	110	–	kHz
Input Impedance Components: Resistance	R_I	12	800	1600	–	90	170	–	10	20	–	kΩ
Input Impedance Components: Capacitance at 1 MHz	C_I	–	–	2.7	–	–	2.7	–	–	2.7	–	pF
Output Impedance Components: Resistance	R_O	14	–	200	–	–	20	–	–	2	–	MΩ
Output Impedance Components: Capacitance at 1 MHz	C_O	–	–	4.5	–	–	4.5	–	–	4.5	–	pF
ZENER BIAS REGULATOR CHARACTERISTICS (at T_A = 25°C, I_Z = 0.1 mA)						MIN.	TYP.	MAX.				
Voltage	V_Z	15	Temp. Coeff. = 3 mV/°C			6.2	6.7	7.9				V
Impedance	Z_Z	–					200	300				Ω

* Temperature-Coefficient; -2.2 mV/°C (at V_{ABC} = 0.54 V, I_{ABC} = 1 μA; -2.1 mV/°C (at V_{ABC} = 0.060 V, I_{ABC} = 10 μA); -1.9 mV/°C (at V_{ABC} = 0.66 V, I_{ABC} = 100 μA)

■ Conditions for Input Offset Voltage and Supply Sensitivity:

(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test —

V^+ is reduced to 5 volts for V^+ sensitivity

V^- is reduced to -5 volts for V^- sensitivity

(b) V^+ sensitivity in μV/V = $\frac{\text{Voffset - Voffset for +5 V and -6 V supplies}}{\text{1 volt}}$

V^- sensitivity in μV/V = $\frac{\text{Voffset - Voffset for -5 V and +6 V supplies}}{\text{1 volt}}$

ELECTRICAL CHARACTERISTICS (CA3060AD, CA3060BD, CA3060E)

For each amplifier at T_A = 25°C, V^+ = 15 V, V^- = -15 V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVE Fig.	LIMITS Amplifier Bias Current I_{ABC} = 1 μA MIN.	TYP.	MAX.	I_{ABC} = 10 μA MIN.	TYP.	MAX.	I_{ABC} = 100 μA MIN.	TYP.	MAX.	UNITS
			CA3060BD						CA3060AD CA3060BD CA3060E			
STATIC CHARACTERISTICS												
Input Offset Voltage	V_{IO}	3	–	1	5	–	1	5	–	1	5	mV
Input Offset Current	I_{IO}	4	–	3	14	–	30	100	–	250	1000	nA
Input Bias Current	I_{IB}	5a,b	–	33	70	–	300	550	–	2500	5000	nA
Peak Output Current	I_{OM}	6a,b	1.3	2.3		15	26	–	150	240	–	μA
Peak Output Voltage: Positive	V_{OM^+}	7	12	13.6	–	12	13.6	–	12	13.6	–	V
Negative	V_{OM^-}		12	14.7	–	12	14.7	–	12	14.7	–	
Amplifier Supply Current (each amplifier)	I_A	8a,b	–	8.5	14	–	85	120	–	850	1200	μA
Power Consumption (each amplifier)	P_T	–	–	0.26	0.42	–	2.6	3.6	–	26	36	mW
Input Offset-Voltage Sensitivity■: Positive	$\Delta V_{IO}/\Delta V^+$	--	–	1.5	150	–	2	150	–	2	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	20	150	–	20	150	–	30	150	
Amplifier Bias Voltage*	V_{ABC}	9	–	0.54	–	–	0.60	–	–	0.66	–	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)												
Forward Transconductance (large signal)	g_{21}	10a,b	0.3	1.55	–	3	18	–	30	102	–	mmho
Common-Mode Rejection Ratio	CMRR	–	70	110	–	70	110	–	70	90	–	dB
Common-Mode Input Voltage Range	V_{ICR}	–	+12 to -12 min. +13 to -14 typ.			+12 to -12 min. +13 to -14 typ.			+12 to -12 min. +13 to -14 typ.			V
Slew Rate (Test ckt., Fig. 13)	SR	–	–	0.1	–	–	1	–	–	8	–	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	-	20	–	–	45	–	–	110	–	kHz
Input Impedance Components: Resistance	R_I	12	800	1600	–	90	170	–	10	20	–	kΩ
Capacitance at 1 MHz	C_I	–	–	2.7	–	–	2.7	–	–	2.7	–	pF
Output Impedance Components: Resistance	R_O	14	–	200	–	–	20	–	–	2	–	MΩ
Capacitance at 1 MHz	C_O	–	–	4.5	–	–	4.5	–	–	4.5	–	pF
ZENER BIAS REGULATOR CHARACTERISTICS (at T_A=25°C, I_Z = 0.1 mA)						MIN.	TYP.	MAX.				
Voltage	V_Z	15	Temp. Coeff. = 3 mV/°C			6.2	6.7	7.9				V
Impedance	Z_Z	–					200	300				Ω

* Temperature Coefficient; -2.2 mV/°C (at V_{ABC} = 0.54 V, I_{ABC} = 1 μA; -2.1 mV/°C (at V_{ABC} = 0.060 V, I_{ABC} = 10 μA); -1.9 mV/°C (at V_{ABC} = 0.66 V, I_{ABC} = 100 μA)

■ Conditions for Input Offset Voltage and Supply Sensitivity:

(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test ---

V^+ is reduced to 13 volts for V^+ sensitivity

V^- is reduced to −13 volts for V^- sensitivity

(b) V^+ sensitivity in μV/V = $\frac{\text{Voffset - Voffset for +13 V and −15 V supplies}}{\text{1 volt}}$

V^- sensitivity in μV/V = $\frac{\text{Voffset - Voffset for −13 V and +15 V supplies}}{\text{1 volt}}$

CA3060, CA3060A Types

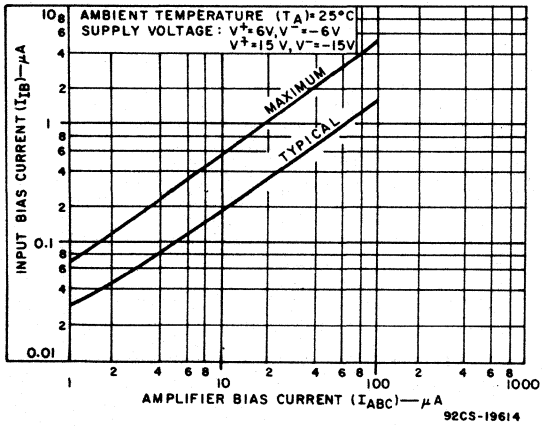


Fig.5a—Input bias current vs. amplifier bias current

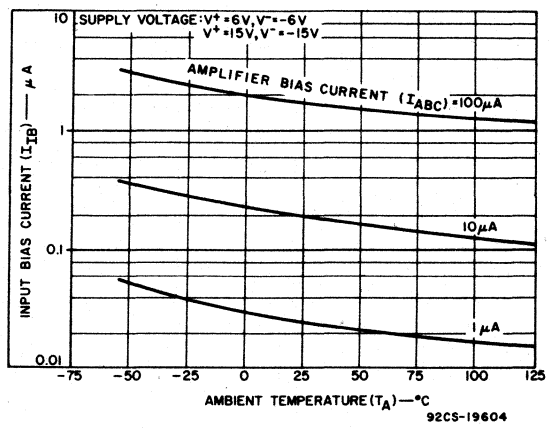


Fig.5b—Input bias current vs. ambient temperature.

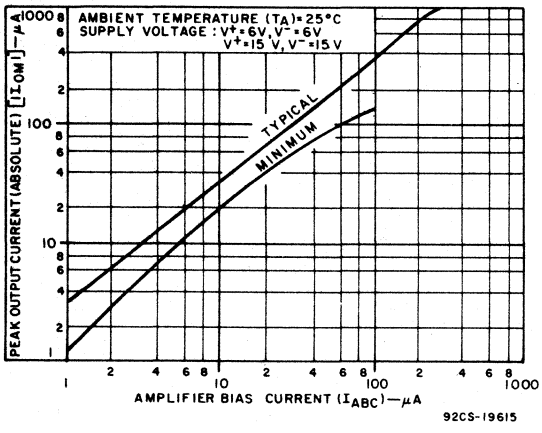


Fig.6a—Peak output current vs. amplifier bias current.

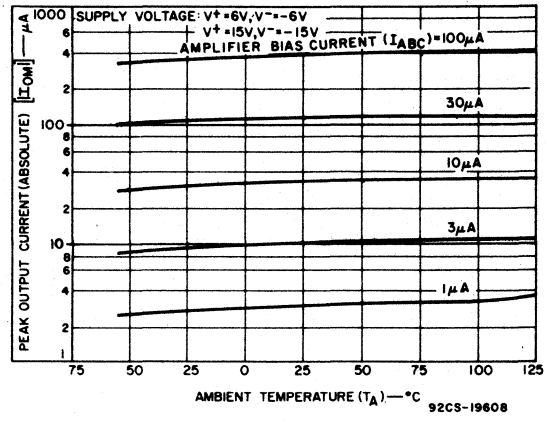


Fig.6b—Peak output current vs. ambient temperature.

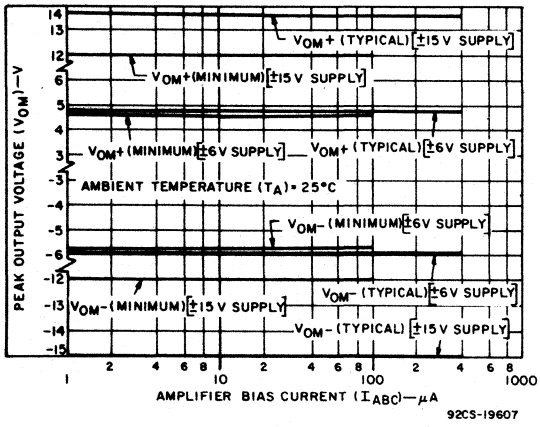


Fig.7—Peak output voltage vs. amplifier bias current.

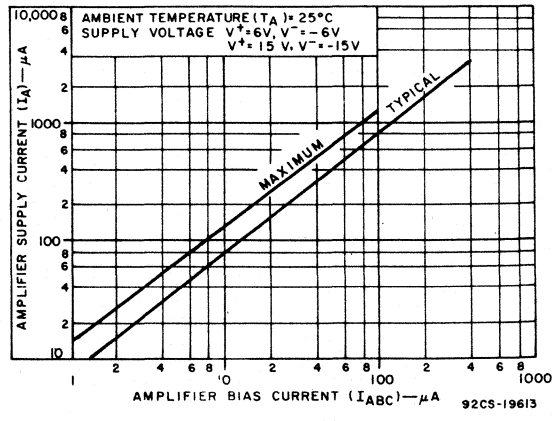


Fig.8a—Amplifier supply current (each amplifier) vs. amplifier bias current.

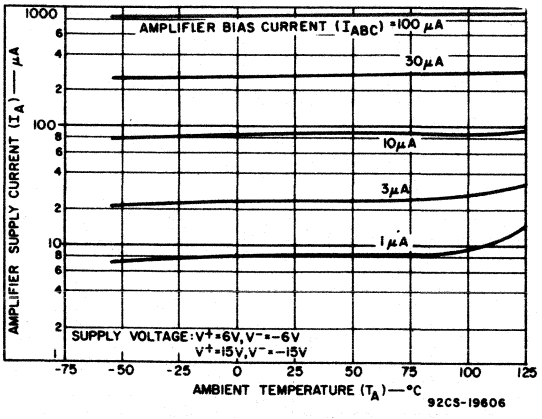


Fig.8b—Amplifier supply current (each amplifier) vs. ambient temperature.

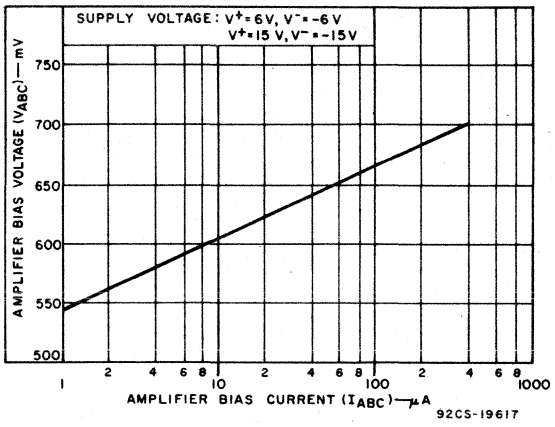


Fig.9—Amplifier bias voltage vs. amplifier bias current.

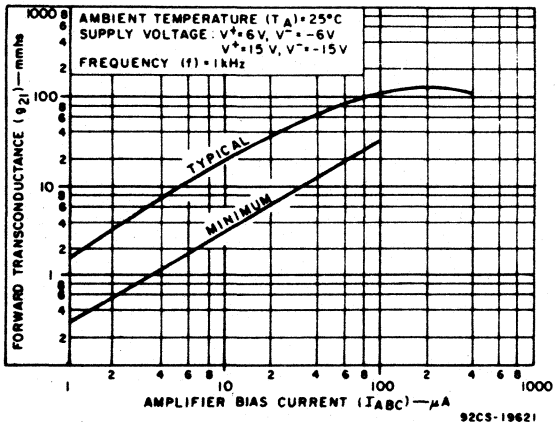


Fig.10a—Forward transconductance vs. amplifier bias current.

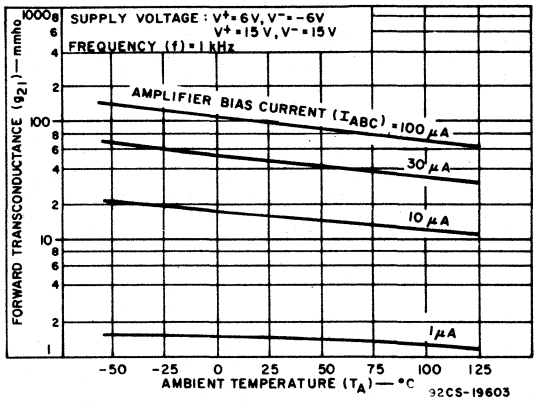


Fig.10b—Forward transconductance vs. ambient temperature.

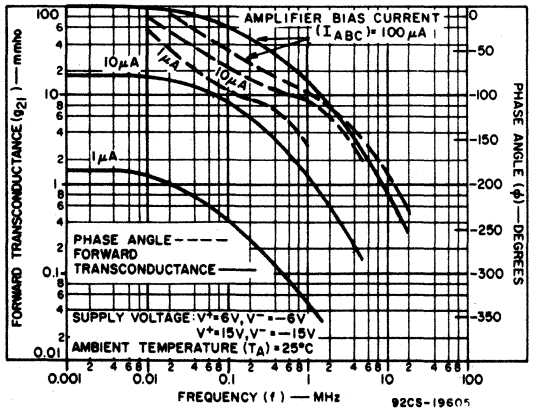


Fig.11—Forward transconductance vs. frequency.

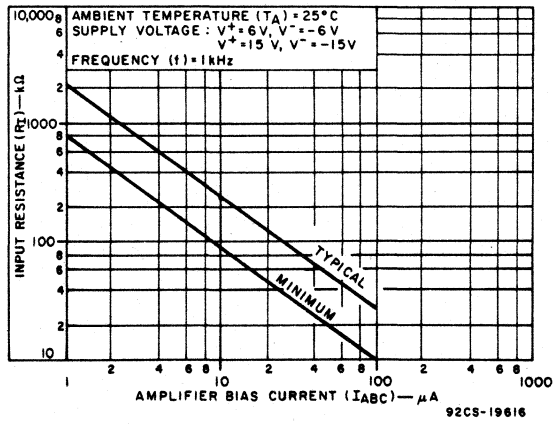
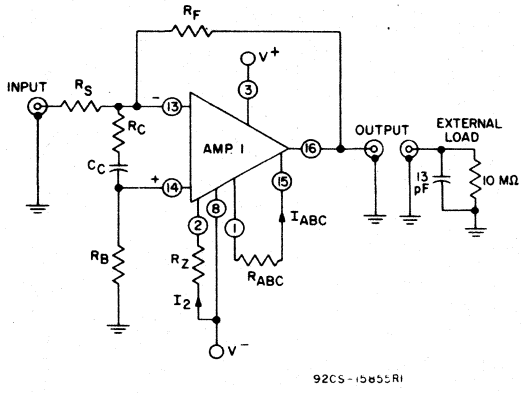


Fig.12—Input resistance vs. amplifier bias current.



V_Z is measured between terminals 1 and 8.

V_{ABC} is measured between terminals 15 and 8.

$$R_Z = \frac{[(V^+)-(V^-)-0.7]}{I_2}, \quad R_{ABC} = \frac{V_Z - V_{ABC}}{I_{ABC}}$$

Supply Voltage: for both ±6 V and ±15 V.

TYPICAL SLEW RATE TEST CIRCUIT PARAMETERS

I_{ABC}	SLEW RATE	I_2	R_{ABC}	R_S	R_F	R_B	R_C	C_C
μA	V/μs	μA	ohms					μF
100	8	200	62 k	100k	100k	51k	100	0.02
10	1	200	620k	1M	1M	510k	1k	0.005
1	0.1	2	6.2M	10M	10M	5.1M	∞	0

Fig. 13—Slew rate test circuit for amplifier No. 1 of CA3060.

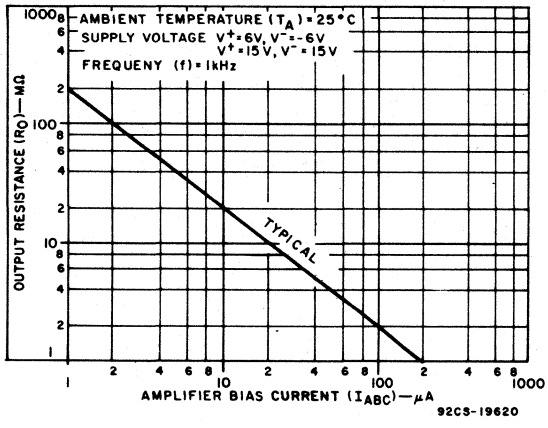


Fig. 14—Output resistance vs. amplifier bias current.

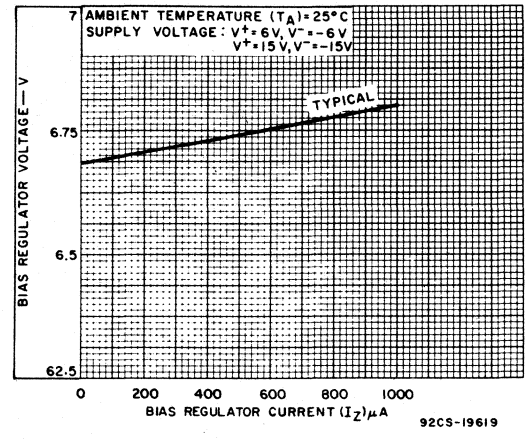


Fig. 15—Bias regulator voltage vs. bias regulator current.

OPERATING CONSIDERATIONS

The CA3060 consists of three operational amplifiers similar in form and application to conventional operational amplifiers but sufficiently different from the standard operational amplifier (op-amp) to justify some explanation of their characteristics. The amplifiers incorporated in the CA3060 are best described by the term Operational Transconductance Amplifier (OTA). The characteristics of an ideal OTA are similar to those of an ideal op-amp except that the OTA has an extremely high output impedance. Because of this inherent characteristic the output signal is best defined in terms of current which is proportional to the difference between the voltages of the two input terminals. Thus, the transfer characteristic is best described in terms of transconductance rather than voltage gain. Other than the difference given above, the characteristics tabulated on pages 3 and 4 of this data bulletin are similar to those of any typical op-amp.

The OTA circuitry incorporated in the CA3060 (See Fig. 16) provides the equipment designer with a wider variety of circuit arrangements than does the standard op-amp; because as the curves in the data bulletin indicate, the user may select the optimum circuit conditions for a specific application simply by varying the bias conditions of each amplifier. If low power consumption, low bias, and low offset current, or high input impedance are primary design requirements, then low current operating conditions may be selected. On the other hand, if operation into a moderate load impedance is the primary consideration, then higher levels of bias may be used.

Bias Considerations for Op-Amp Applications

The operational transconductance amplifiers allow the circuit designer to select and control the operating conditions of the circuit merely by the adjustment of the input bias current I_{ABC}. This enables the designer to have complete control over transconductance, peak output current and total power consumption independent of supply voltage.

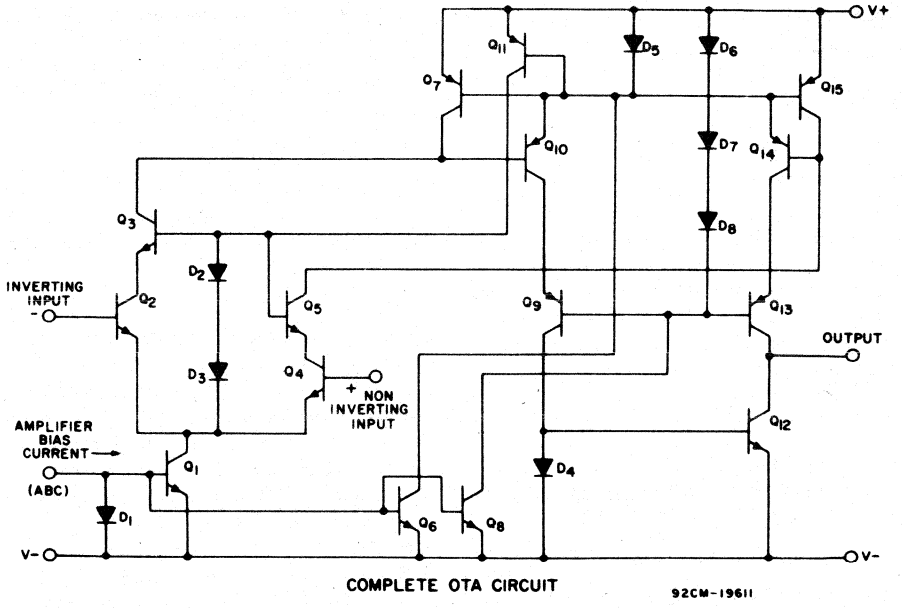


Fig. 16—Complete schematic diagram showing bias regulator and one of the three operational transconductance amplifiers.

In addition, the high output impedance makes these amplifiers ideal for applications where current summing is involved.

The design of a typical operational amplifier circuit (See Fig. 17) would proceed as follows:

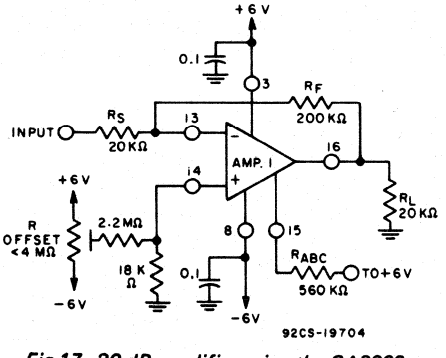


Fig. 17—20-dB amplifier using the CA3060.

Circuit Requirements
Closed loop voltage gain = 10 (20 dB)
Offset voltage adjustable to zero
Current drain as low as possible
Supply voltage = ±6 V
Maximum input voltage = ±50 mV
Input resistance = 20 kΩ
Load resistance = 20 kΩ
Device: CA3060

Calculation

1. Required transconductance g_{21}.
   Assume that the open loop gain A_{OL} must be at least ten times the closed loop gain. Therefore, the forward transconductance required is given by

$$g_{21} = A_{OL}/R_L$$

$$= 100/18\ k\Omega$$

$$\cong 5.5\ mmho$$

(R_L = 20 kΩ in parallel with 200 kΩ

$\cong$ 18 kΩ)

2. Selection of suitable amplifier bias current.
   The amplifier bias current is selected from the minimum value curve of transconductance (Fig. 10a) to assure that the amplifier will provide sufficient gain. For the required g_{21} of 5.5 mmho an amplifier bias current I_{ABC} of 20 μA is suitable.

3. Determination of Output Swing Capability.
   For a loop gain of 10 the output swing is ±0.5 V and the peak load current 25 μA. However, the amplifier must also supply the necessary current through the feedback resistor and for R_S = 20 kΩ than R_F = 200 kΩ if A_{OL} = 10. Therefore, the feedback loading = 0.5/200 kΩ = 2.5 μA.

   The total amplifier current output requirements are, therefore, ±27.5 μA. Referring to the data given in Fig. 6a we see that for an amplifier bias current of 20 μA the amplifier output current is ±40 μA. This is obviously adequate and it is not necessary to change the amplifier bias current I_{ABC}.

4. Calculation of bias resistance.
   For minimum supply current drain the amplifier bias current I_{ABC} should be fed directly from the supplies and not from the bias regulator. The value of the resistor R_{ABC} may be directly calculated using Ohm's law.

$$R_{ABC} = \frac{V_{SUP} - V_{ABC}}{I_{ABC}}$$

$$R_{ABC} = \frac{12 - 0.63}{20 \times 10^{-6}}$$

$$= 568.5\ k\Omega \text{ or } \cong 560\ k\Omega$$

5. Calculation of offset adjustment circuit.
   In order to reduce the loading effect of the offset adjustment circuit on the power supply, the offset control should be arranged to provide the necessary offset current. The source resistance of the non-inverting input is made equal to the source resistance of the inverting input.

i.e. $\frac{20 \times 200 \times 10^6 \text{ ohms}}{220 \times 10^3} \cong 18\ k\Omega$

Because the maximum offset voltage is 5 mV and an additional increment due to the offset current (Fig. 4) flowing through the source resistance

(i.e. $200 \times 10^{-9} \times 18 \times 10^3$ volts), therefore,

the Offset Voltage Range = 5 mV + 3.6 mV = ±8.6 mV

The current necessary to provide this offset is

$$\frac{8.6 \times 10^{-3}}{18 \times 10^3} \text{ or } 0.48\ \mu A$$

With a supply voltage of ±6 V, this current can be provided by a 10 MΩ resistor. However, the stability of such a resistor is often questionable and a more realistic value of 2.2 MΩ was used in the final circuit.

OTHER CONSIDERATIONS

Capacitance Effects

The CA3060 is designed to operate at such low power levels that high impedance circuits must be employed. In designing such circuits, particularly feedback amplifiers, stray circuit capacitance must always be considered because of its adverse effect on frequency response and stability. For example a 10-kΩ load with a stray capacitance of 15 pF has a time constant of 1 MHz. Fig. 18 illustrates how a 10-kΩ 15-pF load modifies the frequency characteristic.

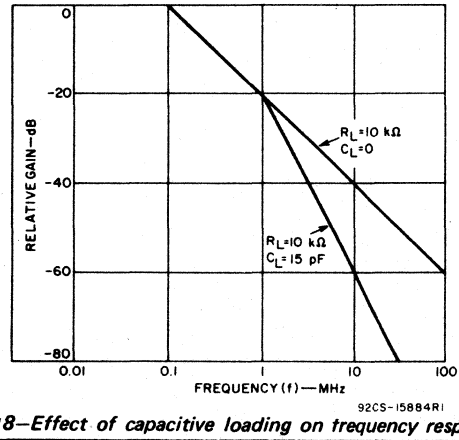


Fig. 18—Effect of capacitive loading on frequency response.

Capacitive loading also has an effect on slew rate; because the peak output current is established by the amplifier bias current, I_{ABC} (see Fig. 6a), the maximum slew rate is limited to the maximum rate at which the capacitance can be charged by the I_{OM}. Therefore,

$$SR = dV/dt = I_{OM}/C_L$$

where C_L is the total load capacitance including strays. This relationship is shown graphically in Fig. 19. When measuring slew rate for this data bulletin, care was taken to keep the total capacitive loading to 13 pF.

Phase Compensation

In many applications phase compensation will not be required for the amplifiers of the CA3060. When needed, compensation may easily be accomplished by a simple RC network at the input of the amplifier as shown in Fig. 13. The values given in Fig. 13 provide stable operation for the critical unity gain condition, assuming that capacitive loading on the output is 13 pF or less. Input phase compensation is recommended in order to maintain the highest possible slew rate.

In applications such as integrators, two OTAs may be cascaded to improve current gain. Compensation is best accomplished in this case with a shunt capacitor at the output of the first amplifier. The high gain following compensation assures a high slew rate.

APPLICATIONS

Having determined the operating points of the CA3060 amplifiers, they can now function in the same manner as conventional op-amps, and thus, are well suited for most op-amp applications, including inverting and non-inverting amplifiers, integrators, differentiators, summing amplifiers etc.

TRI-LEVEL COMPARATOR

Tri-level comparator circuits are an ideal application for the CA3060 since it contains the requisite three amplifiers. A tri-level comparator has three adjustable limits. If either the upper or lower limit is exceeded, the appropriate output is activated until the input signal returns to a selected intermediate limit. Tri-level comparators are particularly suited to many industrial control applications.

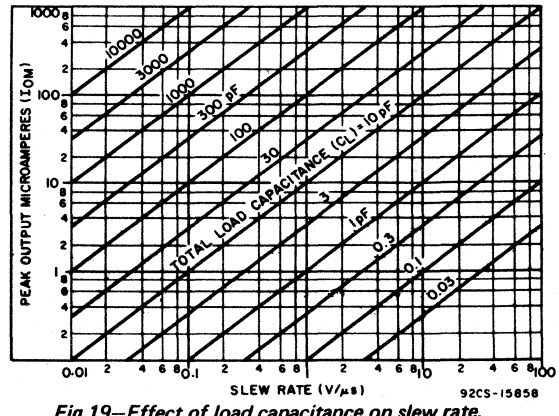


Fig. 19—Effect of load capacitance on slew rate.

Circuit Description

Fig. 20 shows the block diagram of a tri-level comparator using the CA3060. Two of the three amplifiers are used to compare the input signal with the upper-limit and lower-limit reference voltages. The third amplifier is used to compare the input signal with a selected value of intermediate-limit reference voltage. By appropriate selection or resistance ratios this intermediate-limit may be set to any voltage between the upper-limit and lower-limit values. The output of the upper-limit and lower-limit comparator sets the corresponding upper or lower-limit flip-flop. The activated flip-flop retains its state until the third comparator (intermediate-limit) in the CA3060 initiates a reset function, thereby indicating that the signal voltage has returned to the intermediate-limit selected. The flip-flops employ two CA3086 transistor-array IC's, with circuitry to provide separate "SET" and "POSITIVE OUTPUT" terminals.

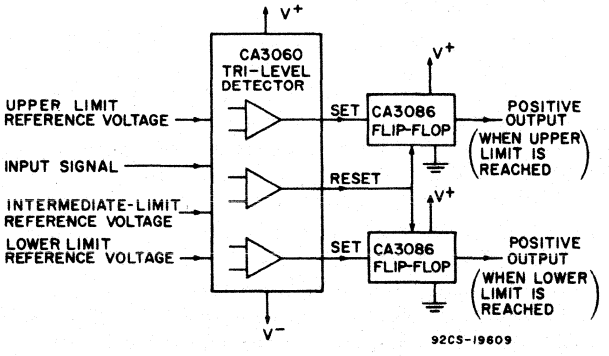


Fig.20—Functional block diagram of a tri-level comparator.

The circuit diagram of a tri-level comparator appears in Fig. 21. Power is provided for the CA3060 via terminals 3 and 8 by ±6-volt supplies and the built-in regulator provides amplifier-bias-current (I_{ABC}) to the three amplifiers via terminal 1. Lower-limit and upper-limit reference voltages are selected by appropriate adjustment of potentiometers R1 and R2, respectively. When resistors R3 and R4 are equal in value (as shown), the intermediate-limit reference voltage is automatically established at a value midway between the lower-limit and upper-limit values. Appropriate variation of resistors R3 and R4 permits selection of other values of intermediate-limit voltages. Input signal (E_S) is applied to the three comparators via terminals 5, 12, and 14. The "SET" output lines trigger the appropriate flip-flop whenever the input signal reaches a limit value. When the input signal returns to an intermediate-value, the common flip-flop "RESET" line is energized. The loads in the circuits, shown in Fig. 21 are 5-V, 25-mA lamps.

Active Filters — Using the CA3060 as a Gyrator

The high output impedance of the OTAs makes the CA3060 ideally suited for use as a gyrator in active filter applications. Fig. 22 shows two OTAs of the CA3060 connected as a gyrator in an active filter circuit. The OTAs in this circuit can make a 3-μF capacitor function as a floating 10-kilohenry inductor across Terminals A and B. The measured Q of 13 (at a frequency of 1 Hz) of this inductor compares favorably with a calculated Q of 16. The 20-kilohm to 2-megohm attenuators in this circuit extend the dynamic range of the OTA by a factor of 100. The 100-kilohm potentiometer, across V+ and V-, tunes the inductor by varying the g_{21} of the OTAs, thereby changing the gyration resistance.

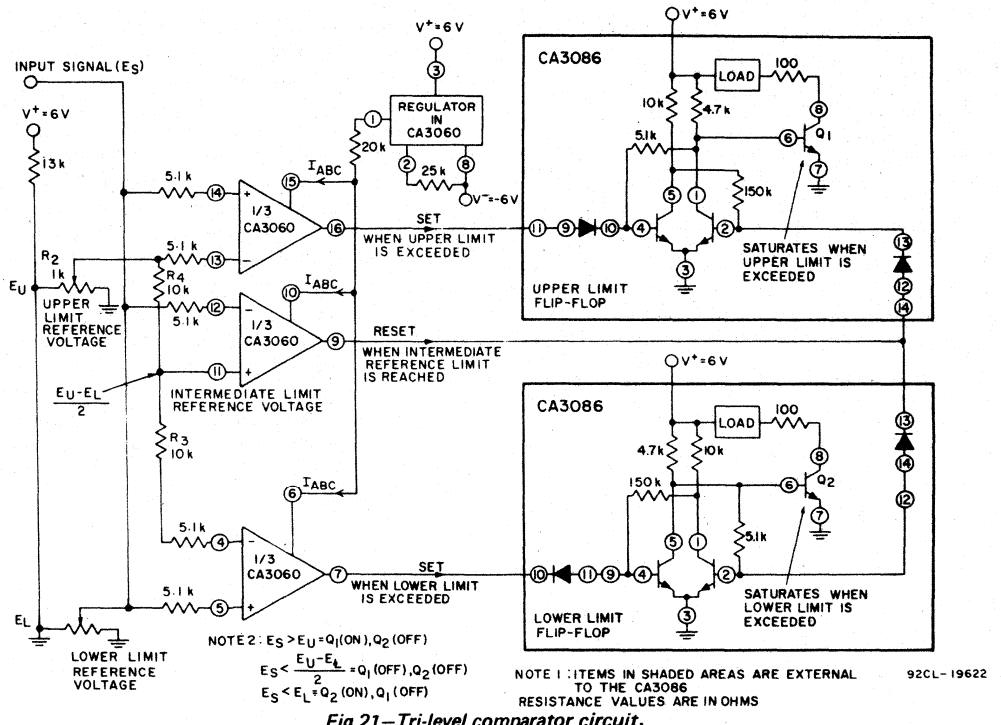


Fig.21—Tri-level comparator circuit.

CA3060, CA3060A Types

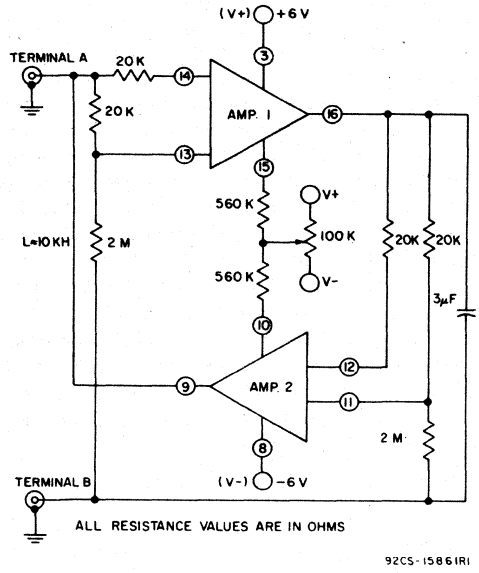


Fig.22—Two operational transconductance amplifiers of the CA3060 connected as a gyrator in an active filter circuit.

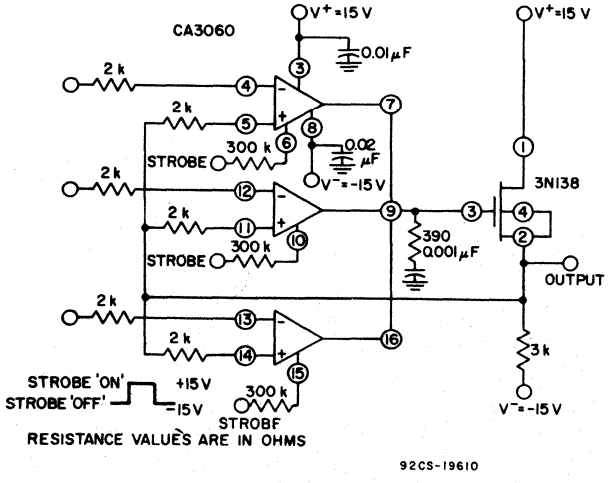


Fig.23—Three-channel multiplexer.

THREE CHANNEL MULTIPLEXER

Fig. 23 shows a schematic of a three channel multiplexer using a single CA3060 and a 3N138 MOS/FET as a buffer and power amplifier.

When the CA3060 is connected as a high-input impedance voltage follower, and strobe "ON," each amplifier is activated and the output swings to the level of the input of that amplifier. The cascade arrangement of each CA3060 amplifier with the MOS/FET provides an open loop voltage gain in excess of 100 dB, thus assuring excellent accuracy in the voltage follower mode with 100% feedback.

Operation at ±6 volts is also possible with several minor changes. First, the resistance in series with amplifier bias current (I_{ABC}) terminal of each amplifier should be decreased to maintain 100 μA of strobe—"ON" current at this lower supply voltage. Second, the drain resistance for the MOS/FET should be decreased to maintain the same value of source current. The low cost dual-gate protected MOS/FET, RCA-40841, may be used when operating at the low supply voltage.

The phase compensation network consists of a single 390Ω resistor and a 1000-pF capacitor, located at the interface of the CA3060 output and the MOS/FET gate. The bandwidth of the system is 1.5 MHz and the slew rate is 0.3 volts/μsec. The system slew rate is directly proportional to the value of the phase compensation capacitor. Thus, with higher gain settings where lower values of phase compensation capacitors are possible, the slew rate is proportionally increased.

NON LINEAR APPLICATIONS

AM Modulator (Two-Quadrant Multiplier)

Fig. 24 shows Amplifier No. 3 of the CA3060 used in an AM modulator or 2-quadrant multiplier circuit. When modulation is applied to the amplifier bias input, Terminal B, and the carrier frequency to the differential input, Terminal A, the waveform, shown in Fig. 24, is obtained. Fig. 24 is a result of adjusting the input offset control to balance the circuit so that no modulation can occur at the output without a carrier input. The linearity of the modulator is indicated by the solid trace of the superimposed modulating frequency. The maximum depth of modulation is determined by the ratio of the peak input modulating voltage to $V_{\bar{}}$.

The two-quadrant multiplier characteristic of this modulator is easily seen if modulation and carrier are reversed as shown in Fig. 24. The polarity of the output must follow that of the differential input; therefore, the output is positive only during, the positive half cycle of the modulation and negative only in the second half cycle. Note, that both the input and output signals are referenced to ground. The output signal is zero when either the differential input or I_{ABC} are zero.

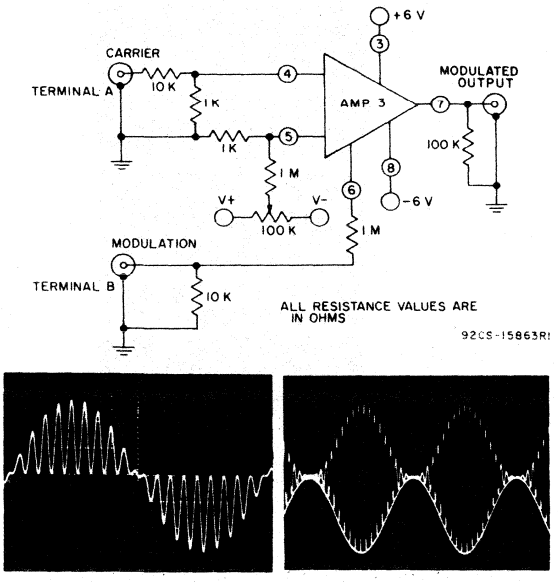


Fig.24—Two-quadrant multiplier circuit using the CA3060 with associated waveforms.

Four-Quadrant Multiplier

The CA3060 is also useful as a four-quadrant multiplier. A block diagram of such a multiplier, utilizing Amplifier Nos. 1, 2, and 3, is shown in Fig. 25 and a typical circuit is shown in Fig. 26. The multiplier consists of a single CA3060 and, as in the two-quadrant multiplier, exhibits no level shift between input and output. In Fig. 25, Amplifier No. 1 is connected as an inverting amplifier for the X-input signal. The output current of Amplifier No. 1 is calculated as follows:

$$I_O(1) = [-V_X]\ [g_{21}(1)] \qquad \text{(Eq.3)}$$

Ampl. No. 2 is a non-inverting amplifier so that

$$I_O(2) = [+V_X]\ [g_{21}(2)] \qquad \text{(Eq. 4)}$$

Because the amplifier output impedances are high, the load current is the sum of the two output currents, for an output voltage

$$V_O = V_X R_L\ [g_{21}(2) - g_{21}(1)] \qquad \text{(Eq. 5)}$$

The transconductance is approximately proportional to the amplifier bias current; therefore, by varying the bias current the g_{21} is also controlled. Amplifier No. 2 bias current is proportional to the Y-input signal and is expressed as

$$I_{ABC(2)} \approx \frac{(V\text{-}) + V_Y}{R_1} \qquad \text{(Eq. 6)}$$

Hence,

$$g_{21}(2) \approx k\ [\ (V\text{-}) + V_Y\ ]. \qquad \text{(Eq. 7)}$$

Bias for Amplifier No. 1 is derived from the output of Amplifier No. 3 which is connected as a unity-gain inverting amplifier. $I_{ABC(1)}$, therefore, varies inversely with V_Y. And by the same reasoning as above

$$g_{21}(1) \approx k\ [(V\text{-}) - V_Y]. \qquad \text{(Eq. 8)}$$

Combining equation 5, 7, and 8 yields:

$$V_O \approx V_X \cdot k \cdot R_L \left|[(V\text{-}) + V_Y] - [(V\text{-}) - V_Y]\right| \quad \text{or}$$

$$V_O \approx 2\,k\,R_L\,V_X\,V_Y$$

Fig. 26 shows the actual circuit including all the adjustments associated with differential input and an adjustment for equalizing the gains of Amplifiers No. 1 and No. 2. Adjustment of the circuit is quite simple. With both the X and Y voltages at zero, connect Terminal 10 to Terminal 8. This procedure disables Amplifier No. 2 and permits adjusting the offset voltage of Amplifier No. 1 to zero by means of the 100-kΩ potentiometer. Next, remove the short between Terminals 10 and 8 and connect Terminal 15 to Terminal 8. This step disables Amplifier No. 1 and permits Amplifier No. 2 to be zeroed with the other potentiometer. With AC signals on both the X and Y input, R3 and R11 are adjusted for symmetrical output signals. Fig. 27 shows the output waveform with the multiplier adjusted. The voltage waveform in Fig. 27a shows suppressed carrier modulation of 1-kHz carrier with a triangular wave.

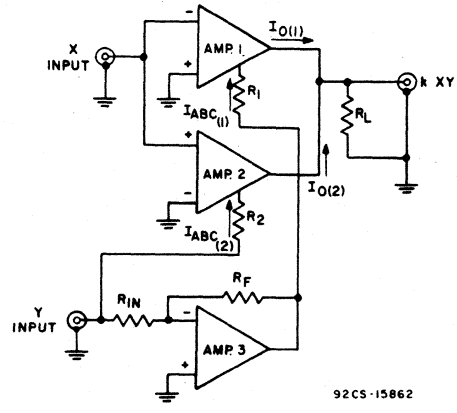


Fig.25—Four-quadrant multiplier using the CA3060.

Figures 27b and 27c, respectively, show the squaring of a triangular wave and a sine wave. Notice that in both cases the outputs are always positive and return to zero after each cycle.

CA3060, CA3060A Types

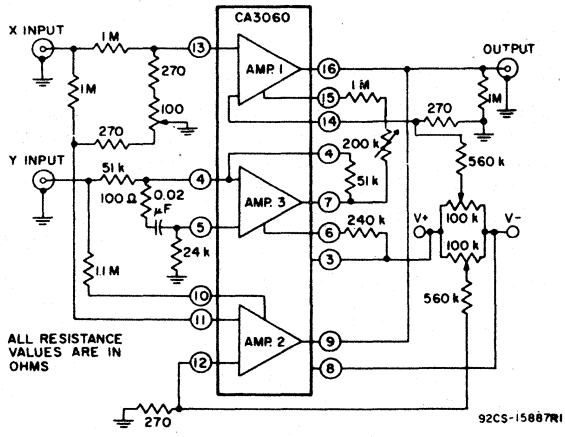


Fig.26—Typical four-quadrant multiplier circuit.

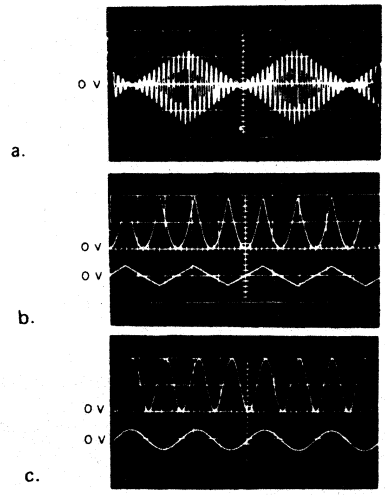
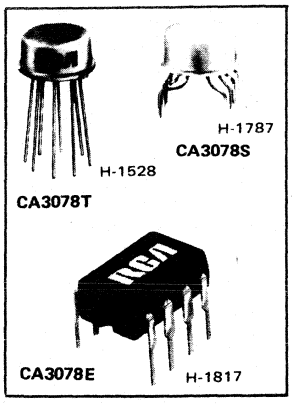


Fig.27—Voltage waveforms of four-quadrant multiplier circuit.



Micropower Operational Amplifier

Features:

- Low standby power: as low as 700 nW
- Wide supply voltage range: ±0.75 to ±15 V
- High peak output current: 6.5 mA min.
- Adjustable quiescent current
- Output short-circuit protection

Applications:

- Portable electronics
- Medical electronics
- Instrumentation
- Telemetry
- Intrusion alarms

The RCA-CA3078 and CA3078A are high-gain monolithic operational amplifiers which can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The CA3078 and CA3078A provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5-volt battery is a practical reality with these devices.

The CA3078A is a preminum device having a supply voltage range of $V^{\pm}$ = 0.75 to $V^{\pm}$ = 15 V and an operating temperature range of −25°C to +125°C. The CA3078 has the same lower supply voltage limit but the upper limit is V^{+} = +6 V and V^{-} = −6 V. The operating temperature range is from 0°C to +70°C.

The CA3078 and CA3078A are supplied in the standard 8-lead TO-5 package ("T" suffix), the 8-lead dual-in-line formed-lead "DIL-CAN" package ("S" suffix), or the 8-lead dual-in-line plastic "MINI-DIP" package ("E" suffix).

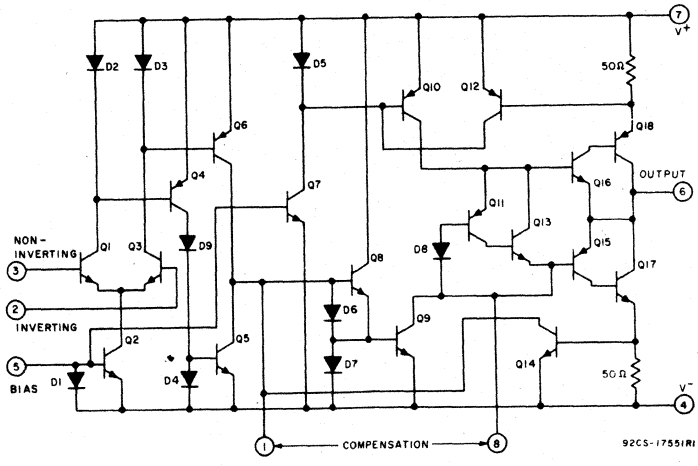


Fig. 1 – Schematic diagram of the CA3078 and CA3078A.

CA3078, CA3078A Types

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25°C$*

	CA3078A	CA3078
DC Supply Voltage (between V^+ and V^- terminal	36 V	14 V
Differential Input Voltage	±6 V	±6 V
DC Input Voltage	V^+ to V^-	V^+ to V^-
Input Signal Current	0.1 mA	0.1 mA
Output Short-Circuit Duration*	No Limitation	No Limitation
Device Dissipation	150 mW (up to 125°C)	500 mW (up to 70°C)
Temperature Range:		
Operating	−55 to +125°C	0 to +70°C
Storage	−65 to +150°C	−65 to +150°C
Lead Temperature (During Soldering):		
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10s max.	+300°C	+300°C

* Short circuit may be applied to ground or to either supply.

ELECTRICAL CHARACTERISTICS For Equipment Design

CHARACTERISTICS SYMBOLS	TEST CONDITIONS			CA3078A LIMITS					CA3078 LIMITS					UNITS
				R_{SET} = 5.1 MΩ, I_Q = 20 μA					R_{SET} = 1 MΩ, I_Q = 100 μA					
				T_A = 25°C			T_A = −55 to 125°C		T_A = 25°C			T_A = 0 to 70°C		
	V^+ & V^- V	R_S kΩ	R_L kΩ	MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
V_{IO}	6	≤10	–	–	0.70	3.5	–	4.5	–	1.3	4.5	–	5	mV
V_{IO}		–	–	–	0.50	2.5	–	5.0	–	6	32	–	40	nA
I_{IB}		–	–	–	7	12	–	50	–	60	170	–	200	nA
A_{OL}		–	≥10	92	100	–	90	–	88	92	–	86	–	dB
I_Q		–	–	–	20	25	–	45	–	100	130	–	150	μA
P_D		–	–	–	240	300	–	540	–	1200	1560	–	1800	μW
V_{OM}		–	≥10	±5.1	±5.3	–	±5	–	±5.1	±5.3	–	±5	–	V
V_{ICR}		≤10	–	–	−5.5 to +5.8	–	−5 to +5	–	–	−5.5 to +5.8	–	−5 to +5	–	V
CMRR		≤10	–	80	115	–	–	–	80	110	–	–	–	dB
I_{OM}^+ or I_{OM}^-		–	–	–	12	–	6.5	30	–	12	–	6.5	30	mA
$\Delta V_{IO}/\Delta V^+$		≤10		76	105	–	–	–	76	93	–	–	–	μV/V
$\Delta V_{IO}/\Delta V^-$			–	76	105	–	–	–	76	93	–	–	–	
				R_{SET} = 13 MΩ, I_Q = 20 μA										
V_{IO}	15	≤10	–	–	1.4	3.5	–	4.5	–	–	–	–	–	mV
A_{OL}		–	≥10	92	100	–	88	–	–	–	–	–	–	dB
I_Q		–	–	–	20	30	–	50	–	–	–	–	–	μA
P_D		–	–	–	600	750	–	1350	–	–	–	–	–	μW
V_{OM}		–	≥10	±13.7	±14.1	–	±13.5	–	–	–	–	–	–	V
CMRR		≤10	–	80	106	–	–	–	–	–	–	–	–	dB
I_{IB}		–	–	–	7	14	–	55	–	–	–	–	–	nA
I_{IO}		–	–	–	0.50	2.7	–	5.5	–	–	–	–	–	nA

ELECTRICAL CHARACTERISTICS, *at $T_A = 25°C$*

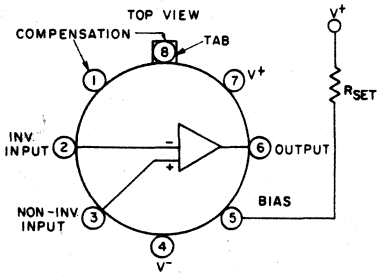
Typical Values Intended Only for Design Guidance

CHARACTERISTICS SYMBOLS	TYPICAL VALUES				UNITS
	CA3078A		CA3078		
	$V^+ = +1.3$ V, $V^- = -1.3$ V $R_{SET} = 2$ MΩ $I_Q = 10$ μA	$V^+ = +0.75$ V, $V^- = -0.75$ V $R_{SET} = 10$ MΩ $I_Q = 1$ μA	$V^+ = +1.3$ V, $V^- = -1.3$ V $R_{SET} = 2$ MΩ $I_Q = 10$ μA	$V^+ = +0.75$ V, $V^- = -0.75$ V $R_{SET} = 10$ MΩ $I_Q = 1$ μA	
V_{IO}	0.7	0.9	1.3	1.5	mV
I_{IO}	0.3	0.054	1.7	0.5	nA
I_{IB}	3.7	0.45	9	1.3	nA
A_{OL}	84	65	80	60	dB
I_Q	10	1	10	1	μA
P_D	26	1.5	26	1.5	μW
V_{OPP}	1.4	0.3	1.4	0.3	V
V_{ICR}	−0.8 to +1.1	−0.2 to +0.5	−0.8 to +1.1	−0.2 to +0.5	V
CMRR	100	90	100	90	dB
$I_{OM}^{\pm}$	12	0.5	12	0.5	mA
$\Delta V_{IO}/\Delta V^{\pm}$	20	50	20	50	μV/V

Typical Values Intended Only for Design Guidance *at $T_A = 25°C$ and $V^+ = +6$ V, $V^- = -6$ V*

CHARACTERISTICS SYMBOLS	TEST CONDITIONS	CA3078A		CA3078	UNITS
		$R_{SET} = 5.1$ MΩ $I_Q = 20$ μA	$R_{SET} = 1$ MΩ $I_Q = 100$ μA	$R_{SET} = 1$ MΩ $I_Q = 100$ μA	
$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10$ kΩ	5	6	6	μV/°C
$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10$ kΩ	6.3	70	70	pA/°C
BW_{OL}	3dB pt.	0.3	2	2	kHz
SR	See Figs. 20, 21	0.027	0.04	0.04	V/μs
		0.5	1.5	1.5	
–	10% to 90% Rise Time	3	2.5	2.5	μs
R_I		7.4	1.7	0.87	MΩ
R_O		1	0.8	0.8	kΩ
e_N (10 Hz)	$R_S = 0$	40	–	25	nV/$\sqrt{Hz}$
i_N (10 Hz)	$R_S = 1$ MΩ	0.25	–	1	pA/$\sqrt{Hz}$

CA3078, CA3078A Types



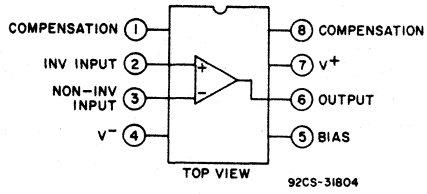


Fig. 2 – Functional diagrams.

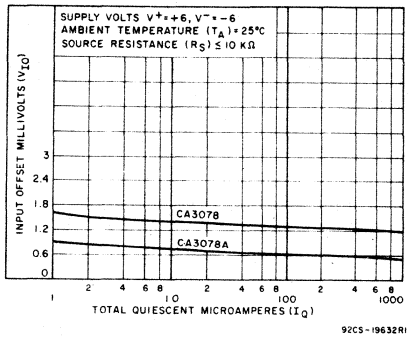


Fig. 3 – Input offset voltage vs. total quiescent current.

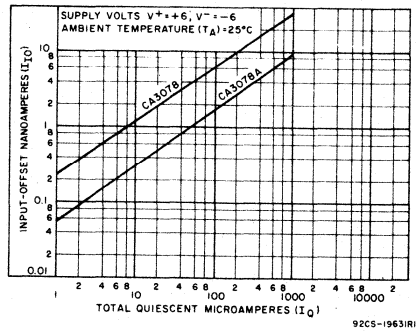


Fig. 4 – Input offset current vs. total quiescent current.

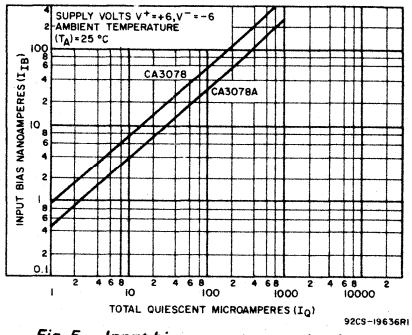


Fig. 5 – Input bias current vs. total quiescent current.

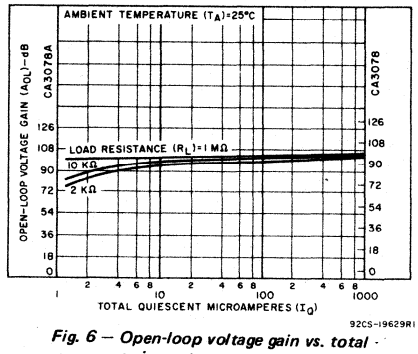


Fig. 6 – Open-loop voltage gain vs. total quiescent current.

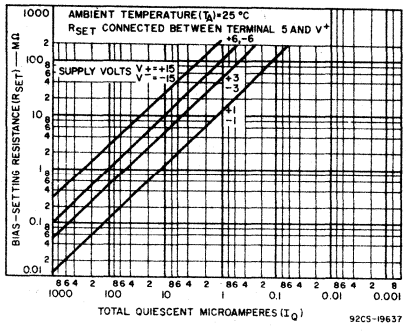


Fig. 7 – Bias-setting resistance vs. total quiescent current.

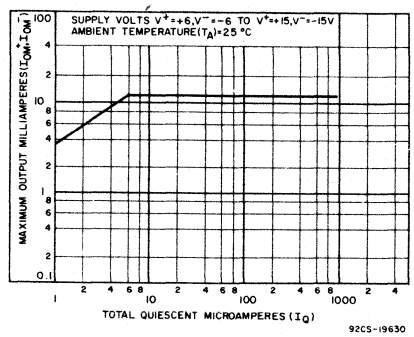


Fig. 8 – Maximum output current vs. total quiescent current.

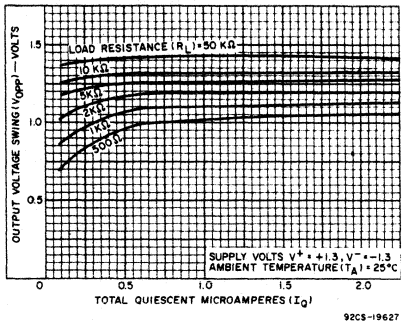


Fig. 9 — Output voltage swing vs. total quiescent current.

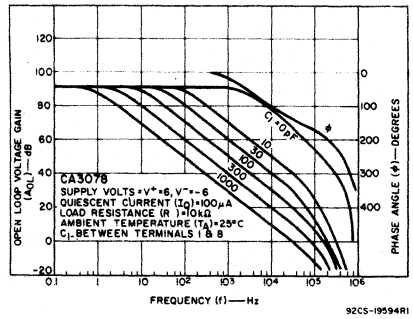


Fig. 10 — Open-loop voltage gain vs. frequency for I_Q = 100 μA — CA3078.

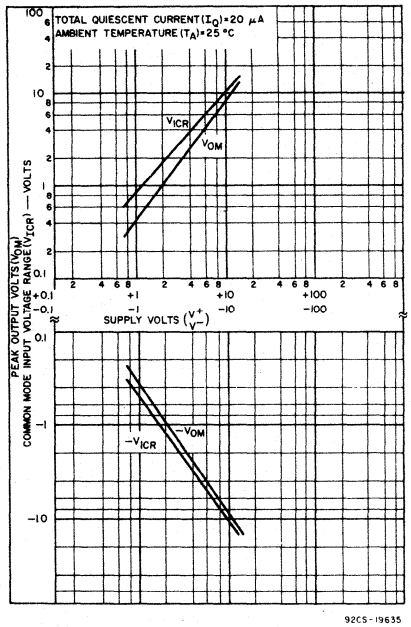


Fig. 11 — Output and common-mode voltage vs. supply voltage.

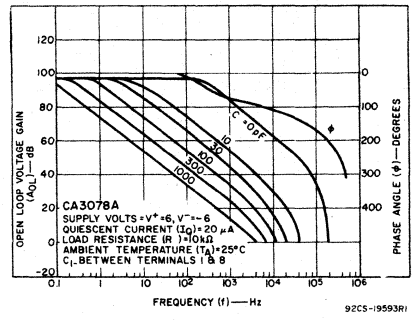


Fig. 12 — Open-loop voltage gain vs. frequency for I_Q = 20 μA — CA3078.

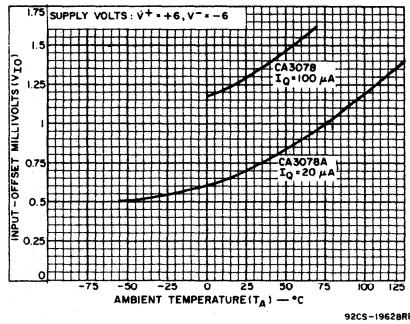


Fig. 13 — Input offset voltage vs. temperature.

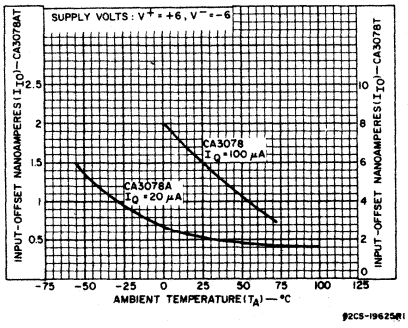


Fig. 14 — Input offset current vs. temperature.

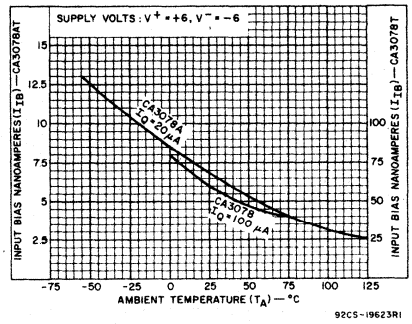


Fig. 15 — Input bias current vs. temperature.

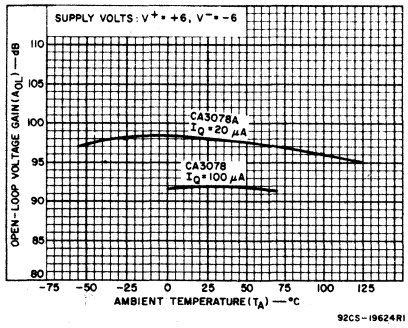


Fig. 16 – Open-loop voltage gain vs. temperature.

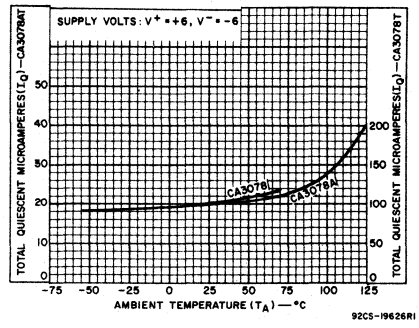


Fig. 17 – Total quiescent current vs. temperature.

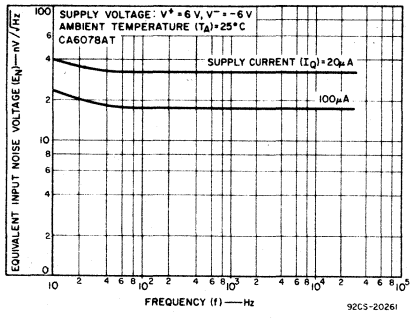


Fig. 18 – Quivalent input noise voltage vs. frequency.

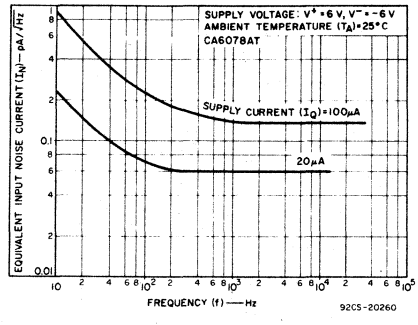


Fig. 19 – Equivalent input noise current vs. frequency.

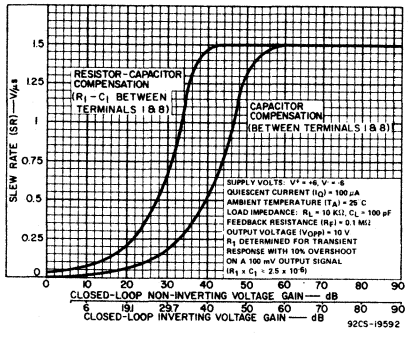


Fig. 20 – Slew rate vs. closed-loop gain for I_Q = 100 μA – CA3078.

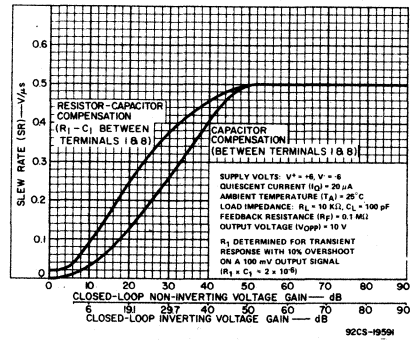


Fig. 21 – Slew rate vs. closed-loop gain for I_Q = 20 μA – CA3078.

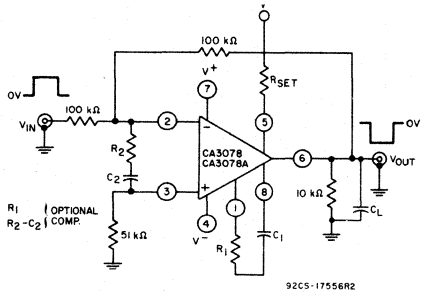


Fig. 22 – Transient response and slew-rate, unity gain (inverting) test circuit.

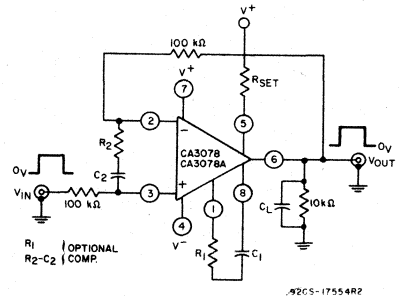


Fig. 23 – Slew-rate, unity gain (non-inverting) test circuit.

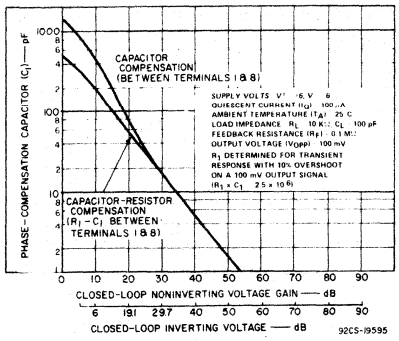


Fig. 24 – Phase compensation capacitance vs. closed-loop gain – CA3078.

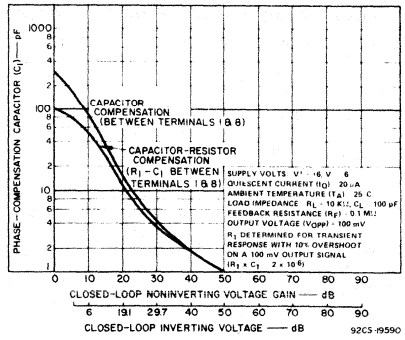


Fig. 25 – Phase compensation capacitance vs. closed-loop gain – CA3078A.

Table I – Unity-gain slew rate vs. compensation – CA3078 and CA3078A

SUPPLY VOLTS: $V^+ = 6$, $V^- = -6$	**TRANSIENT RESPONSE: 10% OVERSHOOT FOR AN OUTPUT VOLTAGE OF 100 mV**
OUTPUT VOLTAGE (V_O) = ±5 V	**AMBIENT TEMPERATURE (T_A) = 25°C**
LOAD RESISTANCE (R_L) = 10 kΩ	

COMPENSATION TECHNIQUE	UNITY GAIN (INVERTING) Fig. 22					UNITY GAIN (NON-INVERTING) Fig. 23				
	R1	C1	R2	C2	SLEW RATE	R1	C1	R2	C2	SLEW RATE
CA3078 – I_Q = 100 μA	kΩ	pF	kΩ	μF	V/μs	kΩ	pF	kΩ	μF	V/μs
Single Capacitor	0	750	∞	0	0.0085	0	1500	∞	0	0.0095
Resistor & Capacitor	3.5	350	∞	0	0.04	5.3	500	∞	0	0.024
Input	∞	0	0.25	0.306	0.67	∞	0	0.311	0.45	0.67
CA3078A – I_Q = 20 μA										
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor & Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	0.4

OPERATING CONSIDERATIONS

Compensation Techniques

The CA3078A and CA3078 can be phase-compensated with one or two external components depending upon the closed-loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from terminal 1 to terminal 8. Values of the resistor and capacitor required for compensation as a function of closed loop gain are shown in Figs. 24 and 25. These curves represent the compensation necessary at quiescent currents of 100 μA and 20 μA, respectively, for a transient response with 10% overshoot. Figs. 20 and 21 show the slew rates that can be obtained with the two different compensation techniques. Higher speeds can be achieved with input compensation, but this increases noise output. Compensation can also be accomplished with a single capacitor connected from terminal 1 to terminal 8, with speed being sacrificed for simplicity. Table I gives an indication of slew rates that can be obtained with various compensation techques at quiescent currents of 100 μA and 20 μA.

Single Supply Operation

The CA3078A and CA3078 can operate from a single supply with a minimum total supply voltage of 1.5 volts. Figs. 27 and 28 show the CA3078A or CA3078 in inverting the non-inverting 20-dB amplifier configurations utilizing a 1.5-volt type "AA" cell for a supply. The total power consumption for

either circuit is approximately 675 nanowatts. The output voltage swing in this configuration is 300 mV p-p with a 20 kΩ load.

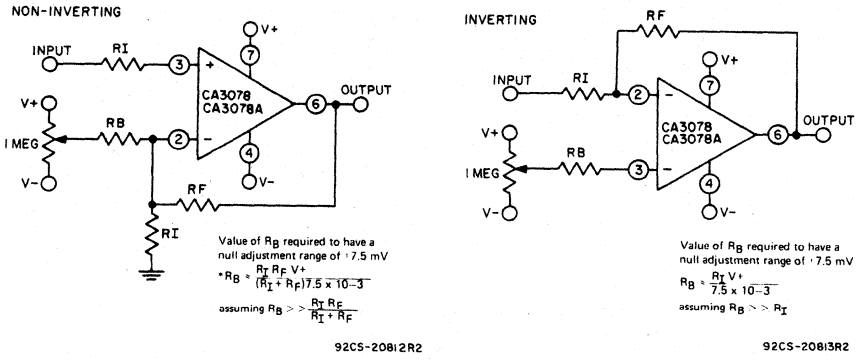


Fig. 26 – Offset voltage null circuits.

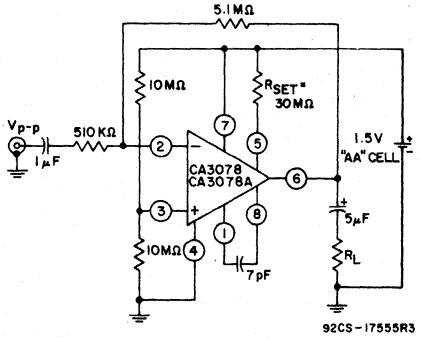


Fig. 27 – Inverting 20-dB amplifier circuit.

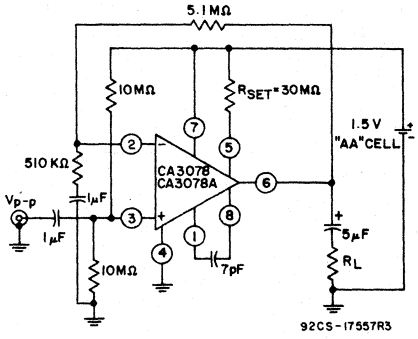
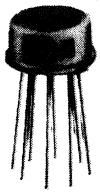
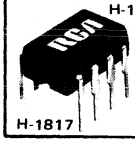


Fig. 28 – Non inverting 20-dB amplifier circuit.

CA3080S
CA3080AS
8-LEAD TO-5
with Dual-In-Line
Formed Leads
"DIL-CAN"
H-1787



CA3080
CA3080A
8-LEAD TO-5
H-1528



H-1817

CA3080E
CA3080AE
8-LEAD Dual-
In-Line Plastic
Package
"MINI-DIP"

Operational Transconductance Amplifiers (OTA's)

Gatable-Gain Blocks

Features:

- Slew rate (unity gain, compensated): 50 V/μs
- Adjustable power consumption: 10μW to 30 mW
- Flexible supply voltage range: ± 2 V to ± 15 V
- Fully adjustable gain: 0 to $g_m R_L$ limit
- Tight g_m spread: CA3080 (2:1), CA3080A (1.6:1)
- Extended g_m linearity: 3 decades

The RCA-CA3080 and CA3080A types are Gatable-Gain Blocks which utilize the unique operational-transconductance-amplifier (OTA) concept described in Application Note ICAN-6668, "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

The CA3080 and CA3080A types have differential input and a single-ended, push-pull, class A output. In addition, these types have an amplifier bias input which may be used either for gating or for linear gain control. These types also have a high output impedance and their transconductance (g_m) is directly proportional to the amplifier bias current (I_{ABC}).

The CA3080 and CA3080A types are notable for their excellent slew rate (50 V/μs), which makes them especially useful for multiplex and fast unity-gain voltage followers. These types are especially applicable for multiplex applications because power is consumed only when the devices are in the "ON" channel state.

The CA3080A is rated for operation over the full military-temperature range (−55 to +125°C) and its characteristics are specifically controlled for applications such as sample-hold, gain-control, multiplex, etc. Operational transconductance amplifiers are also useful in programmable power-switch applications, e.g., as described in Application Note ICAN-6048, "Some Applications of a Programmable Power Switch/Amplifier" (CA3094, CA3094A, CA3094B).

These types are supplied in the 8-lead TO-5-style package (CA3080, CA3080A), and in the 8-lead TO-5-style package with dual-in-line formed leads ("DIL-CAN", CA3080S, CA3080AS). The CA3080 is also supplied in the 8-lead dual-in-line plastic ("MINI-DIP") package (CA3080E, CA3080AE), and in chip form (CA3080H).

Applications:

- **Sample and hold**
- **Multiplex**
- **Voltage follower**
- **Multiplier**
- **Comparator**

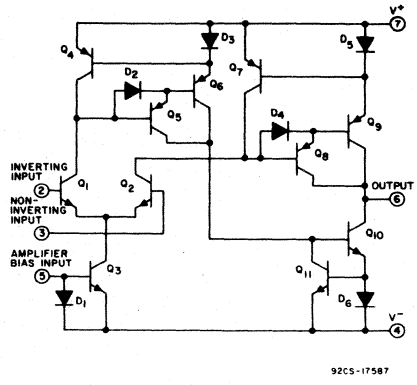


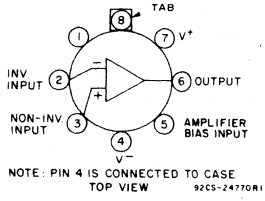
Fig.1 – Schematic diagram for CA3080 and CA3080A.

CA3080, CA3080A Types

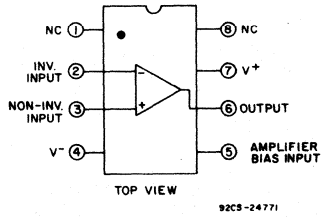
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (Between V^+ and V^- terminals)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE	V^+ to V^-
INPUT SIGNAL CURRENT	1 mA
AMPLIFIER BIAS CURRENT	2 mA
OUTPUT SHORT-CIRCUIT DURATION*	Indefinite
DEVICE DISSIPATION	125 mW
TEMPERATURE RANGE:	
Operating	
CA3080, CA3080E, CA3080S	0 to + 70 °C
CA3080A, CA3080AE, CA3080AS	−55 to + 125 °C
Storage	−65 to + 150 °C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 265 °C

* Short circuit may be applied to ground or to either supply.



TO-5 Style Package



Plastic Package (E Suffix)

Fig.2 – Functional diagrams.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS FOR THE CA3080 AND CA3080A

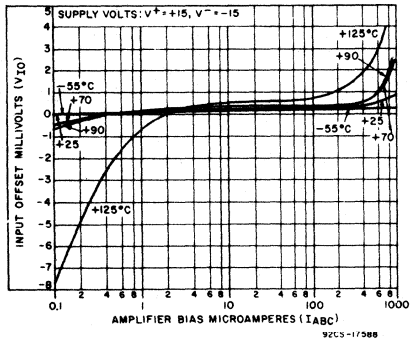


Fig.3 – Input offset voltage as a function of amplifier bias current.

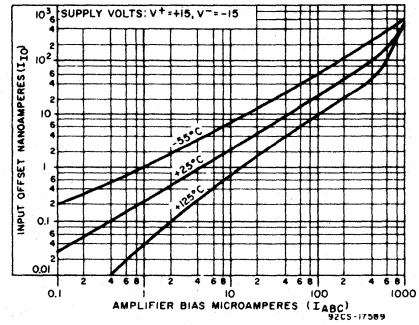


Fig.4 – Input offset current as a function of amplifier bias current.

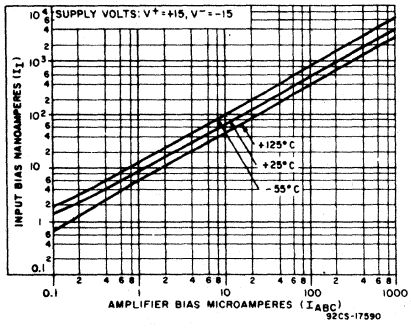


Fig.5 – Input bias current as a function of amplifier bias current.

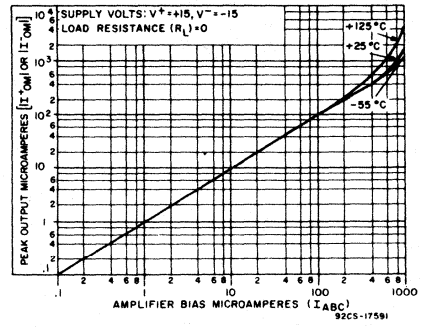


Fig.6 – Peak output current as a function of amplifier bias current.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS: $V^+ = 15$ V, $V^- = -15$ V, $I_{ABC} = 500\ \mu A$, $T_A = 25^oC$ (unless indicated otherwise)	CA3080, CA3080E, CA3080S LIMITS			UNITS
			Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}		–	0.4	5	mV
		$T_A = 0$ to 70^oC	–	–	6	
Input Offset Current	I_{IO}		–	0.12	0.6	μA
Input Bias Current	I_I		–	2	5	μA
		$T_A = 0$ to 70^oC	–	–	7	
Forward Transconductance (large signal)	g_m		6700	9600	13000	μmho
		$T_A = 0$ to 70^oC	5400	–	–	
Peak Output Current	$\lvert I_{OM} \rvert$	$R_L = 0$	350	500	650	μA
		$R_L = 0$, $T_A = 0$ to 70^oC	300	–	–	
Peak Output Voltage:						
Positive	V^+_{OM}	$R_L = \infty$	12	13.5	–	V
Negative	V^-_{OM}		−12	−14.4	–	
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity:						
Positive	$\Delta V_{IO}/\Delta V^+$		–	–	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	–	150	
Common-Mode Rejection Ratio	CMRR		80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}		12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I		10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

			CA3080, CA3080E, CA3080S	
Input Offset Voltage	V_{IO}	$I_{ABC} = 5\ \mu A$	0.3	mV
Input Offset Voltage Change	$\lvert \Delta V_{IO} \rvert$	$I_{ABC} = 500\ \mu A$ to $I_{ABC} = 5\ \mu A$	0.2	mV
Peak Output Current	I_{OM}	$I_{ABC} = 5\ \mu A$	5	μA
Peak Output Voltage:				
Positive	V^+_{OM}	$I_{ABC} = 5\ \mu A$	13.8	V
Negative	V^-_{OM}		−14.5	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	0.08	nA
		$I_{ABC} = 0$, $V_{TP} = 36$ V	0.3	
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4$ V	0.008	nA
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate:				
Maximum (uncompensated)	SR		75	V/μs
Unity Gain (compensated)			50	
Open-Loop Bandwidth	BW_{OL}		2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	f = 1 MHz	0.024	pF
Propagation Delay	t_{PHL}, t_{PLH}	$I_{ABC} = 500\ \mu A$	45	ns

CA3080, CA3080A Types

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS: $V^+ = 15$ V, $V^- = -15$ V, $I_{ABC} = 500\ \mu A$, $T_A = 25^oC$ (unless indicated otherwise)	CA3080A, CA3080AE, CA3080AS LIMITS Min.	Typ.	Max.	UNITS
Input Offset Voltage	V_{IO}	$I_{ABC} = 5\ \mu A$	–	0.3	2	mV
			–	0.4	2	
		$T_A = -55$ to $+125^oC$	–	–	5	
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	$I_{ABC} = 500\ \mu A$ to $I_{ABC} = 5\ \mu A$	–	0.1	3	mV
Input Offset Current	I_{IO}		–	0.12	0.6	μA
Input Bias Current	I_I		–	2	5	μA
		$T_A = -55$ to $+125^oC$	–	–	8	
Forward Transconductance (large signal)	g_m		7700	9600	12000	μmho
		$T_A = -55$ to $+125^oC$	4000	–	–	
Peak Output Current	$\lvert I_{OM}\rvert$	$I_{ABC} = 5\ \mu A$, $R_L = 0$	3	5	7	μA
		$R_L = 0$	350	500	650	
		$R_L = 0$, $T_A = -55$ to $+125^oC$	300	–	–	
Peak Output Voltage:						V
Positive	V^+_{OM}	$I_{ABC} = 5\ \mu A$	12	13.8	–	
Negative	V^-_{OM}	$R_L = \infty$	−12	−14.5	–	
Positive	V^+_{OM}	$R_L = \infty$	12	13.5	–	
Negative	V^-_{OM}		−12	−14.4	–	
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity:						$\mu V/V$
Positive	$\lvert\Delta V_{IO}/\Delta V^+\rvert$		–	–	150	
Negative	$\lvert\Delta V_{IO}/\Delta V^-\rvert$		–	–	150	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	–	0.08	5	nA
		$I_{ABC} = 0$, $V_{TP} = 36$ V	–	0.3	5	
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4$ V	–	0.008	5	nA
Common-Mode Rejection Ratio	CMRR		80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}		12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I		10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

			CA3080A, CA3080AE, CA3080AS	
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate:				V/μs
Maximum (uncompensated)	SR		75	
Unity Gain (compensated)			50	
Open-Loop Bandwidth	BW_{OL}	–	2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		.15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	f = 1 MHz	0.024	pF
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	$I_{ABC} = 100\ \mu A$, $T_A = -55$ to $+125^oC$	3	$\mu V/^oC$
Propagation Delay	t_{PHL}, t_{PLH}	$I_{ABC} = 500\ \mu A$	45	ns

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

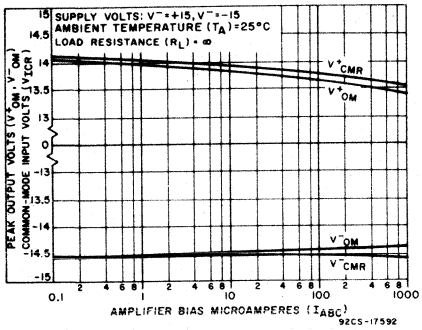


Fig.7 – Peak output voltage as a function of amplifier bias current.

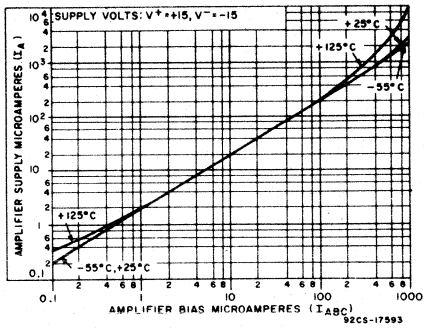


Fig.8 – Amplifier supply current as a function of amplifier bias current.

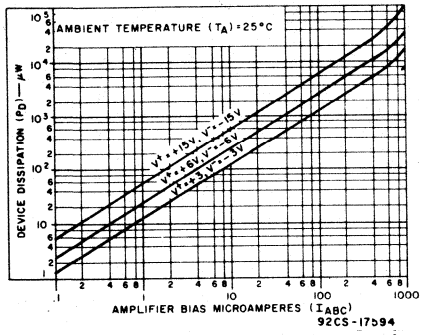


Fig.9 – Total power dissipation as a function of amplifier bias current.

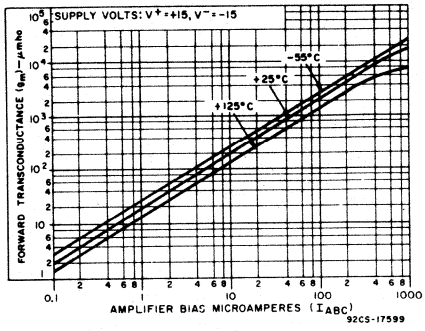


Fig.10 – Transconductance as a function of amplifier bias current.

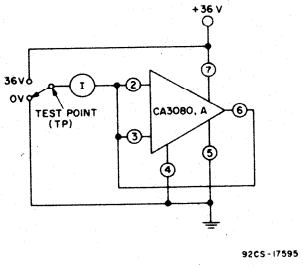


Fig.11 – Leakage current test circuit.

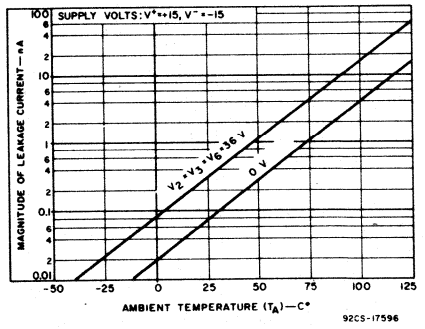


Fig.12 – Leakage current as a function of temperature.

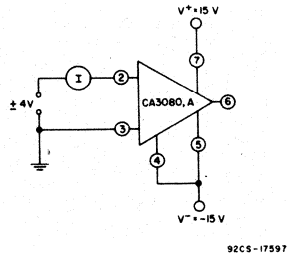


Fig.13 – Differential input current test circuit.

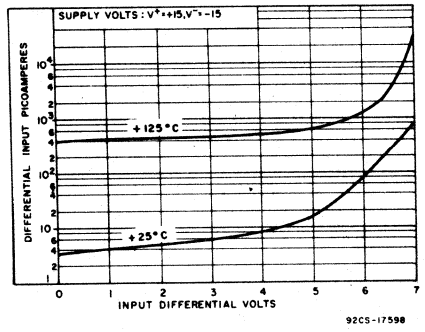


Fig.14 – Input current as a function of input differential voltage.

CA3080, CA3080A Types

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

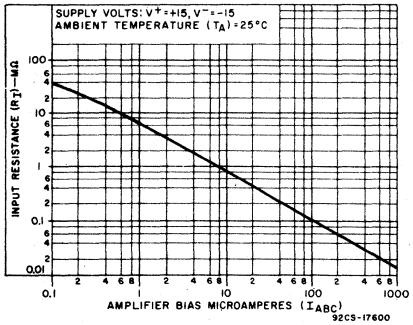


Fig. 15 – Input resistance as a function of amplifier bias current.

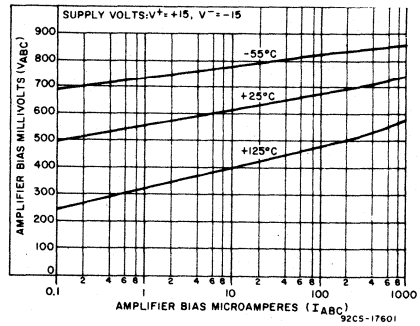


Fig. 16 – Amplifier bias voltage as a function of amplifier bias current.

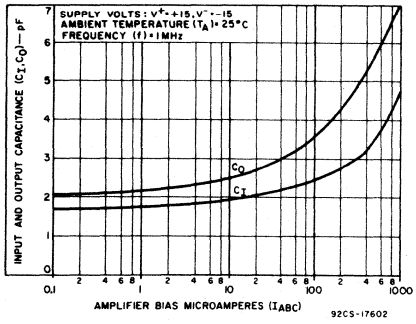


Fig. 17 – Input and output capacitance as a function of amplifier bias current.

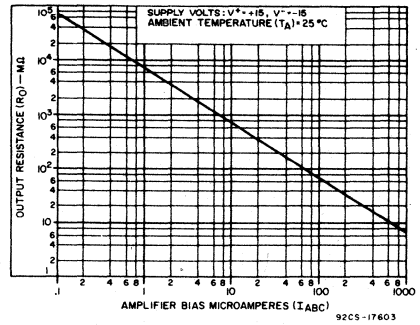


Fig. 18 – Output resistance as a function of amplifier bias current.

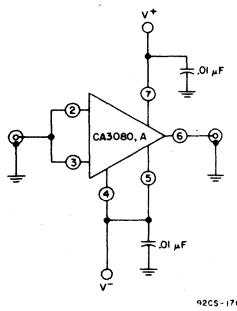


Fig. 19 – Input-to-output capacitance test circuit.

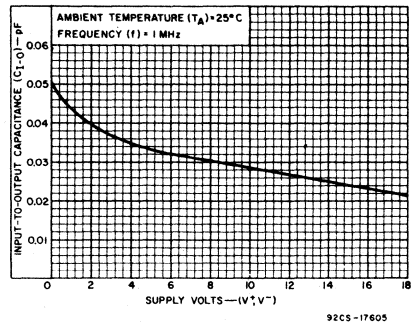
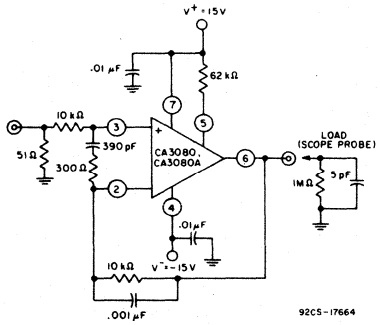


Fig. 20 – Input-to-output capacitance as a function of supply voltage.

APPLICATIONS



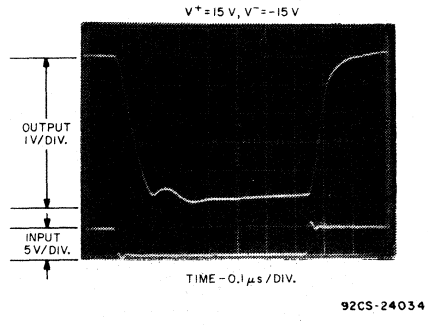


Fig. 21 – Schematic diagram of the CA3080 and CA3080A in a unity-gain voltage follower configuration and associated waveform.

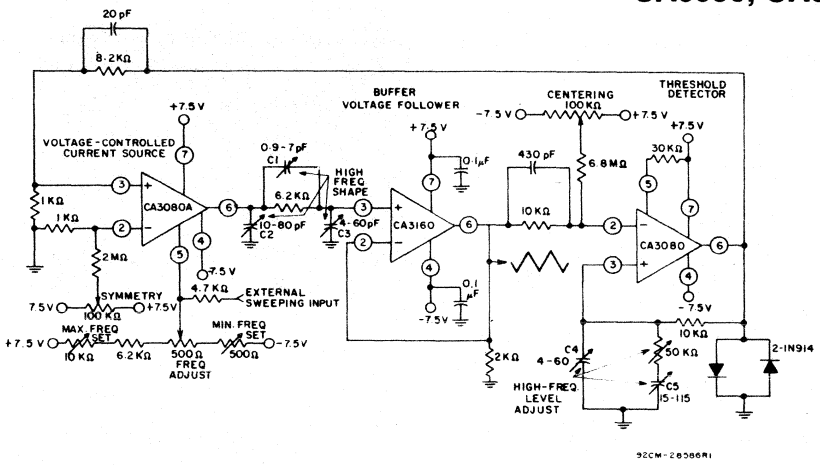
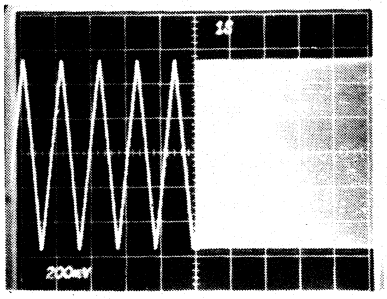
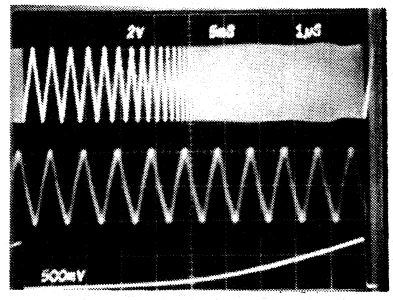


Fig.22 – 1,000,000/1 single-control function generator – 1 MHz to 1 Hz.



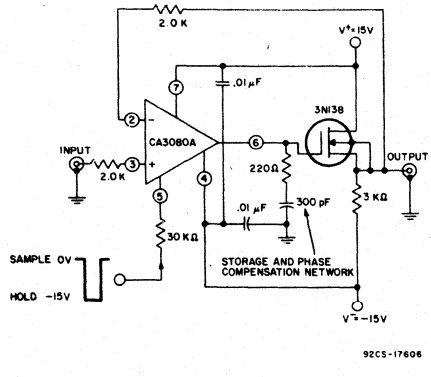
(a) – Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.



92CS-28588

(b) – Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

Fig.23 – Function generator dynamic characteristics waveforms.



SLEW RATE(IN SAMPLE MODE)=1.3 V/μs
ACQUISITION TIME*=3μs

* TIME REQUIRED FOR OUTPUT TO SETTLE WITHIN ±3mV OF A 4-VOLT STEP

Fig.24 – Schematic diagram of the CA3080A in a sample-hold configuration.

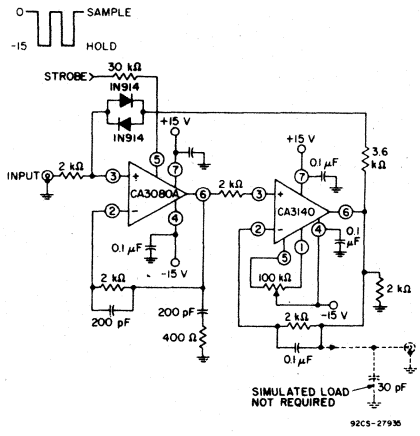
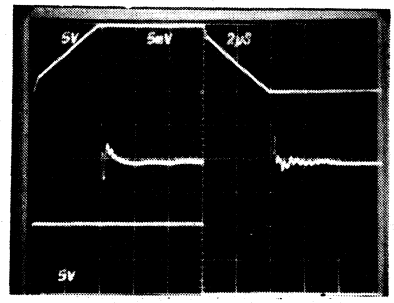


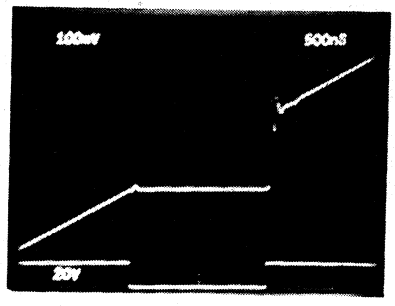
Fig.25 – Sample- and hold circuit.



LARGE-SIGNAL RESPONSE AND SETTLING TIME
TOP TRACE: OUTPUT SIGNAL (5 V/DIV. AND 2 μs/DIV.)
BOTTOM TRACE: INPUT SIGNAL (5 V/DIV. AND 2 μs/DIV.)
CENTER TRACE: DIFFERENCE OF INPUT AND OUTPUT SIGNALS THROUGH TEKTRONIX AMPLIFIER 7A13 (5 mV/DIV. AND 2 μs/DIV.)

92CS-27684

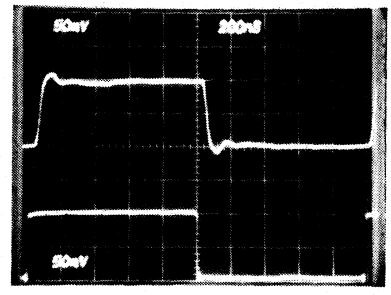
Fig.26 – Large-signal response and settling time for circuit shown in Fig.25.



SAMPLING RESPONSE
TOP TRACE: SYSTEM OUTPUT (100 mV/DIV. AND 500 ns/DIV.)
BOTTOM TRACE: SAMPLING SIGNAL (20 V/DIV. AND 500 ns/DIV.)

92CS-27885

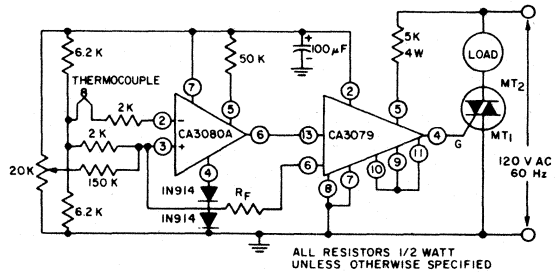
Fig.27 – Sampling response for circuit shown in Fig. 25.



TOP TRACE: OUTPUT (50 mV/DIV. AND 200 ns/DIV.)
BOTTOM TRACE: INPUT (50 mV/DIV. AND 200 ns/DIV.)

92CS-27883

Fig.28 – Input and output response for circuit shown in Fig. 25.



92CS-22619R1

Fig.29 – Thermocouple temperature control with CA3079 zero voltage switch as the output amplifier.

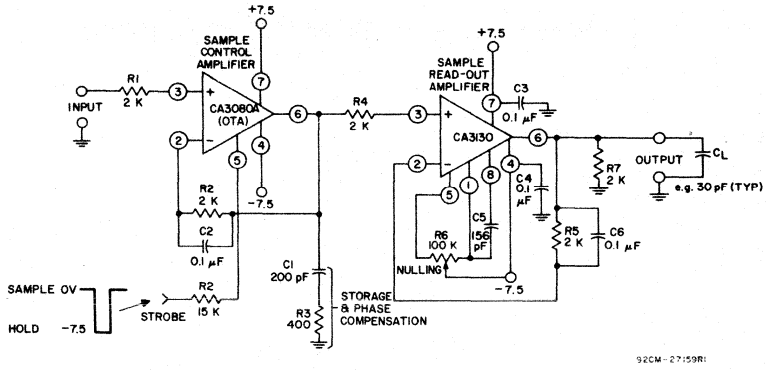
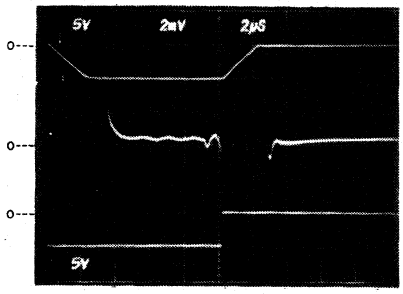
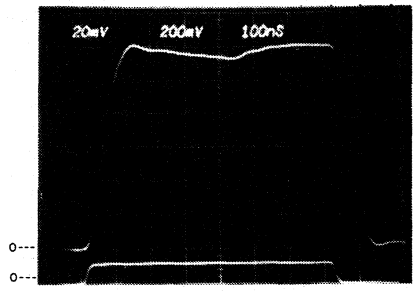


Fig.30 – Schematic diagram of the CA3080A in a sample-hold circuit with BiMos output amplifier.



TOP TRACE: OUTPUT—5 V/DIV. & 2 μs/DIV.
CENTER TRACE: DIFFERENTIAL COMPARISON OF INPUT & OUTPUT—2 mV/DIV. & 2 μs/DIV.
BOTTOM TRACE: INPUT—5 V/DIV. & 2 μs/DIV.
92CS-27161

Fig.31 – Large-signal response for circuit shown in Fig. 30.



TOP TRACE: OUTPUT—20 mV/DIV. & 100 ns/DIV.
BOTTOM TRACE: INPUT—200 mV/DIV. & 100 ns/DIV.
92CS-27160

Fig.32 – Small-signal response for circuit shown in Fig. 30.

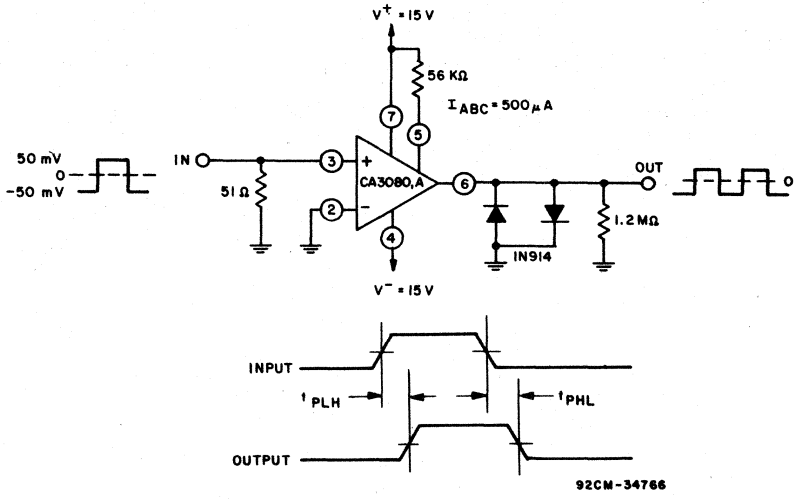
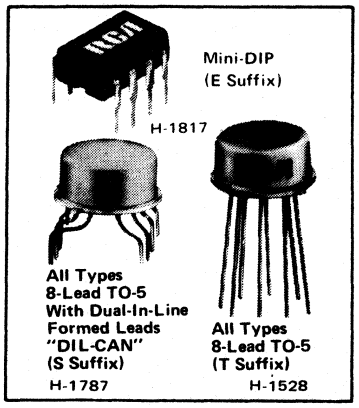


Fig. 33 - Propagation delay test circuit and associated waveforms.

CA3440, CA3440A, CA3440B



Nanopower BiMOS Op Amp

Features:

- *300-nW (typ.) standby power at $V^+ = 5$ V*
- *Supply current, BW, slew rate programmable using external resistor*
- *10-pA (typ.) input current*
- *4.0 to 15-V supply*
- *Output drives typical bipolar-type loads*
- *Low-cost 8-lead Mini-DIP, TO-5*

The RCA-CA3440B, CA3440A, and CA3440* are integrated circuit operational amplifiers that combine the advantages of MOS and bipolar transistors on a single monolithic chip.

The CA3440-series BiMOS Op Amp features gate-protected PMOS transistors in the input circuit to provide very-high-input impedance and very-low-input current (10 pA). These devices operate at total supply voltages from 4 to 15 volts and can be operated over the temperature range from −55°C to +125°C. Their virtues are programmability and very low standby power consumption (300 nW). These operational amplifiers are internally phase-compensated to achieve stable operation in the unity-gain follower configuration. Terminals are also provided for use in applications requiring input offset-voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.5 volts below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses MOS complementary source-follower form which permits moderate load driving capability (10 KΩ) at very low total standby currents (50 nA).

The CA3440-series has the same 8-lead terminal pin-out used for "741" and other industry-standard op amps with two exceptions: terminals one and five must be connected to the negative supply or to a potentiometer if nulling is required. Terminal 8 must be programmed through an external resistor returned to the negative supply.

These devices are supplied in either the standard 8-lead TO-5 style package (T suffix), 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" package (S suffix), or in the 8-lead dual-in-line plastic package "Mini-DIP" (E suffix). They are also available in chip form (H suffix).

* Formerly Dev. Type No. TA10590.

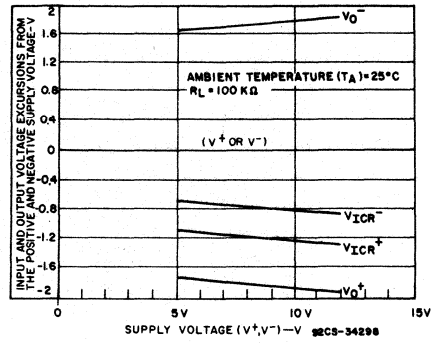


Fig. 1 - Output-voltage-swing and common-mode input-voltage range versus supply voltage.

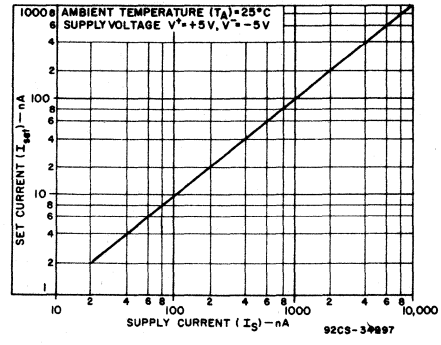


Fig. 2 - Set current versus supply current.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE
(BETWEEN V^+ AND V^- TERMINALS) ..... 25 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±9 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK —
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate linearly 6.67 mW/°C
WITH HEAT SINK —
AT 125°C ..... 418 mW
BELOW 125°C ..... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING ..... −55 to +125°C
STORAGE ..... −65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 IN. (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX. ..... +265°C

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS V^+=+5 V; V^-=-5 V R_{SET}=10 MΩ; T_A=25°C		CA3440B (T,S)	CA3440A	CA3440	UNITS
Input Resistance, R_I			2	2	2	TΩ
Input Capacitance, C_T			3.5	3.5	3.5	pF
Ouput Resistance, R_O			450	450	450	Ω
Equivalent Input Noise Voltage, e_n	f= 1 kHz	R_S=100 Ω	110	110	110	$nV/\sqrt{Hz}$
	f=10 kHz	R_S=100 Ω	110	110	110	$nV/\sqrt{Hz}$
Short-Circuit Current Source IOM^+			15	15	15	mA
To Opposite Supply Sink IOM^-			4.5	4.5	4.5	mA
Gain-Bandwidth Product, f_T			63	63	63	kHz
Slew Rate, SR			0.03	0.03	0.03	V/μs
Transient Response Rise Time, t_r	R_L= 10 kΩ		5.6	5.6	5.6	μs
Overshoot	C_L=100 pF		10	10	10	%

CA3440, CA3440A, CA3440B

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V^+ = +5 V, V^- = -5 V, T_A = 25°C Unless Otherwise Specified, R_{SET}=10 MΩ

CHARACTERISTIC	LIMITS									UNITS
	CA3440B			CA3440A			CA3440			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	0.8	2	—	2	5	—	5	10	mV
Input Offset Current, $\|I_{IO}\|$	—	2.5	10	—	2.5	20	—	2.5	30	pA
Input Current, $\|I_I\|$	—	10	30	—	10	40	—	10	50	pA
Large-Signal Voltage Gain, AOL	32K	100K	—	10K	100K	—	10K	100K	—	V/V
(R_L=10 KΩ)	90	100	—	80	100	—	80	100	—	dB
Common-Mode	—	32	180	—	100	320	—	100	320	μV/V
Rejection Ratio, CMRR	75	90	—	70	80	—	70	80	—	dB
Common-Mode Input Voltage Range, $\overline{VICR}^+$	+3.5	+3.7	—	+3.5	+3.7	—	+3.5	+3.7	—	V
$\overline{VICR}^-$	−5.0	−5.3	—	−5.0	−5.3	—	−5.0	−5.3	—	V
Power Supply Rejection Ratio, $\Delta VIO/\Delta V$	—	20	180	—	32	320	—	32	320	μV/V
PSRR	75	94	—	70	90	—	70	90	—	dB
Maximum Output Voltage, V_{OM}^+	+3	+3.2	—	+3	+3.2	—	+3	+3.2	—	V
V_{OM}^-	−3	−3.2	—	−3	−3.2	—	−3	−3.2	—	V
Supply Current, I^+	—	10	17	—	10	17	—	10	17	μA
Device Dissipation, P_D	—	100	170	—	100	170	—	100	170	μW
Input Offset Voltage Temperature Drift, $\Delta VIO/\Delta T$	—	4	—	—	4	—	—	4	—	μV/°C

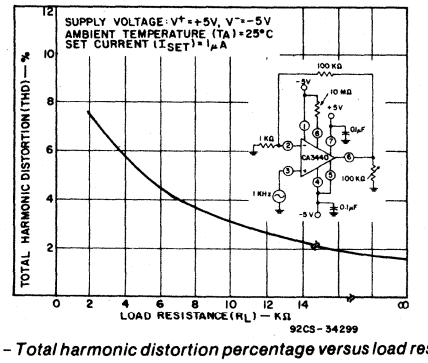


Fig. 3 - Total harmonic distortion percentage versus load resistance.

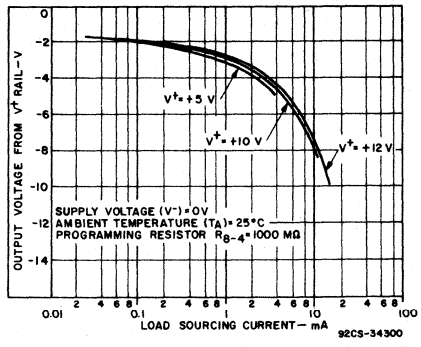


Fig. 4 - Output voltage versus sourcing load current.

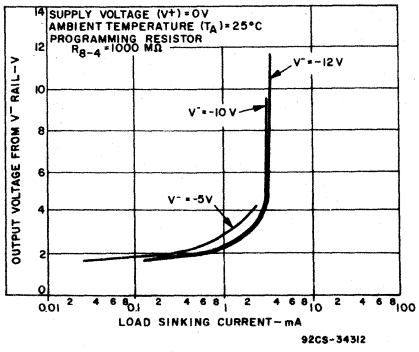


Fig. 5 - Output voltage versus sinking load current.

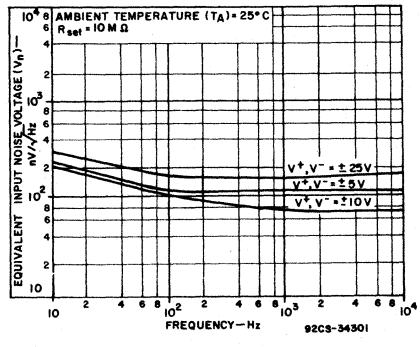


Fig. 6 - Input noise voltage versus frequency.

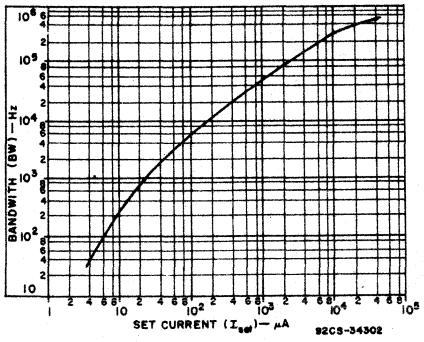


Fig. 7 - Bandwidth versus set current.

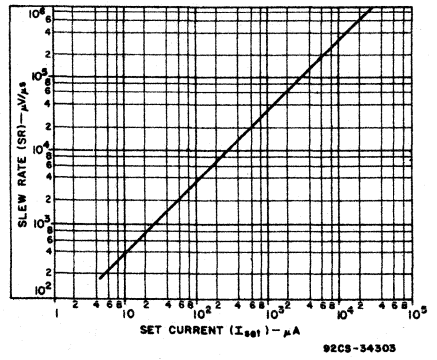


Fig. 8 - Slew rate versus set current.

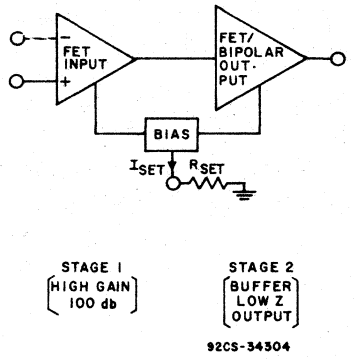


Fig. 9 - Nanopower op amp (supply current programmable using R_{SET}) 1-pA typical input bias current, 4.0 to 15-volt supply.

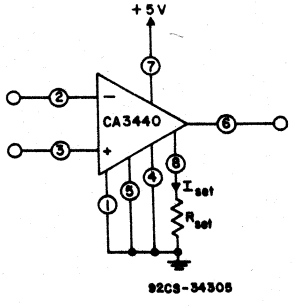


Fig. 10 - Nanopower op amp (usable standby power versus programming resistor R_{SET}).

As R_{SET} is increased, I_{SET} and the standby power decrease while the BW/SR also decreases.

Operating at a +5 V single supply, the CA3440 exhibits the following characteristics:

R_{SET}	Standby Power	BW	SR
1 MΩ	250 μW	164 kHz	0.17 V/μs
10 MΩ	25 μW	27 kHz	0.017 V/μs
100 MΩ	2.5 μW	2.6 kHz	.0017 V/μs
1000 MΩ	250 nW	78 Hz	0.00017 V/μs

The CA3440 is pin-compatible with the 741 except that pins 1 and 5 (typical negative nulling pins) must be connected either directly to pin 4 or to a negative nulling potentiometer. In addition, pin 8, the I_{SET} terminal, must be returned to either ground or −V via R_{SET}.

CA3440, CA3440A, CA3440B

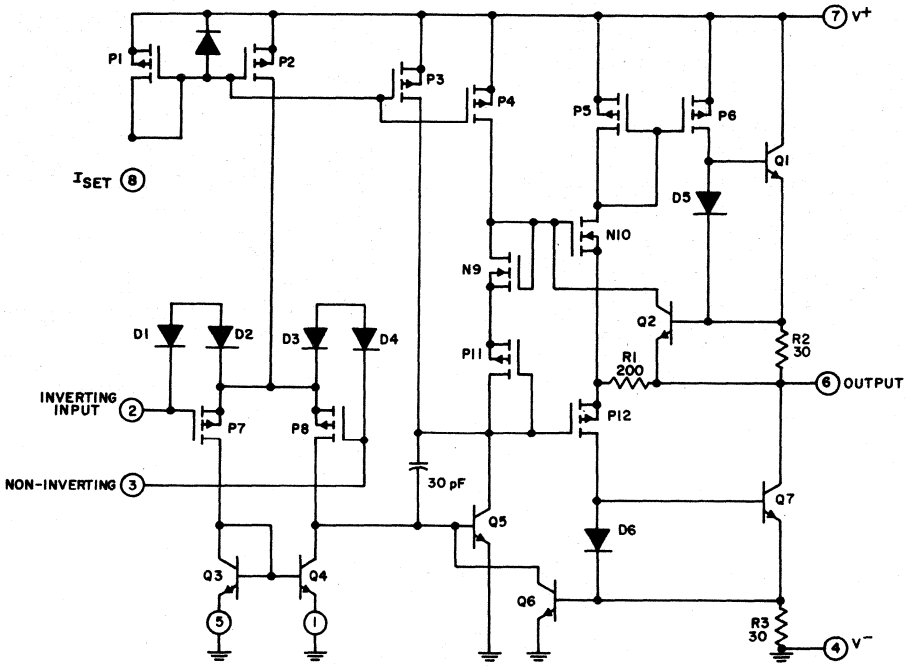


Fig. 11 - Schematic diagram for CA3440. 92CM-34308

APPLICATIONS CIRCUITS

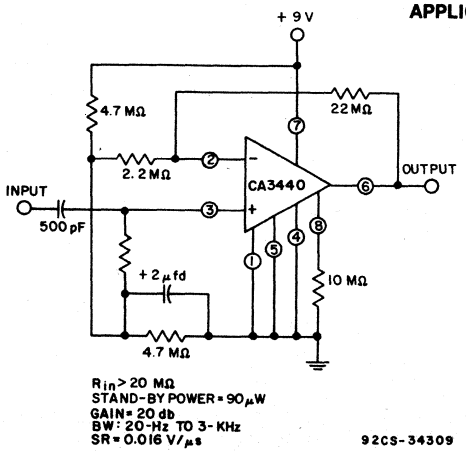


Fig. 12 - High-input impedance amplifier.

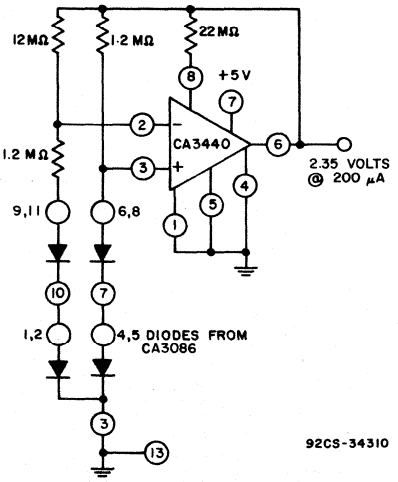
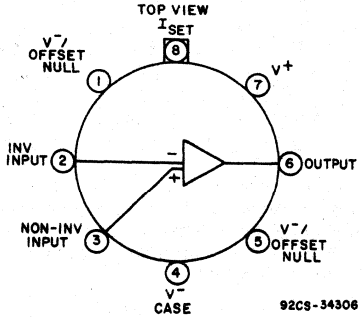
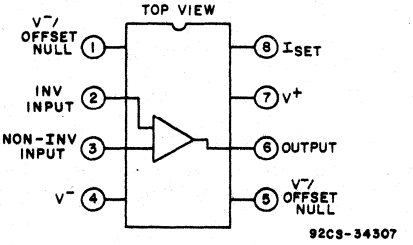


Fig. 13 - Micropower bandgap reference.

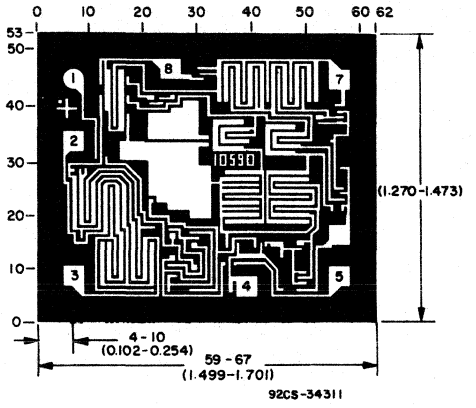


S and T Suffixes



E Suffix

Functional diagrams for CA3440 series.

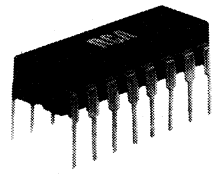


Dimensions and pad layout for CA3440H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3280, CA3280A



16-Lead Dual-In-Line Plastic Package

H-1622

Dual Variable Operational Amplifiers

Features:

- **Low initial input-offset voltage: 500 μV max. (CA3280A)**
- **Low offset-voltage change versus I_{ABC}: $<$ 500 μV typ. for all types**
- **Low offset-voltage drift: 5 μV/C max. (CA3280A)**
- **Excellent matching of the two amplifiers for all characteristics**
- **Internal current-driven linearizing diodes reduce the external input current to an offset component**
- **Differential amplifier emitters brought out for use in emitter-coupled dual-differential amplifier applications**
- **Low noise: 8 nV/$\sqrt{\text{Hz}}$ @ 1 kHz typ.**
- **Low distortion: 0.4% THD typ.**
- **Two modes of gain control**

The RCA-CA3280 and CA3280A types types consist of two variable operational amplifiers that are designed to substantially reduce the initial input offset voltage and the offset-voltage variation with respect to changes in programming current. This design results in reduced "AGC thump," an objectionable characteristic of many AGC systems. Interdigitation, or crosscoupling, of critical portions of the circuit reduces the amplifier dependence upon thermal and processing variables.

The CA3280 has all the generic characteristics of an operational voltage amplifier

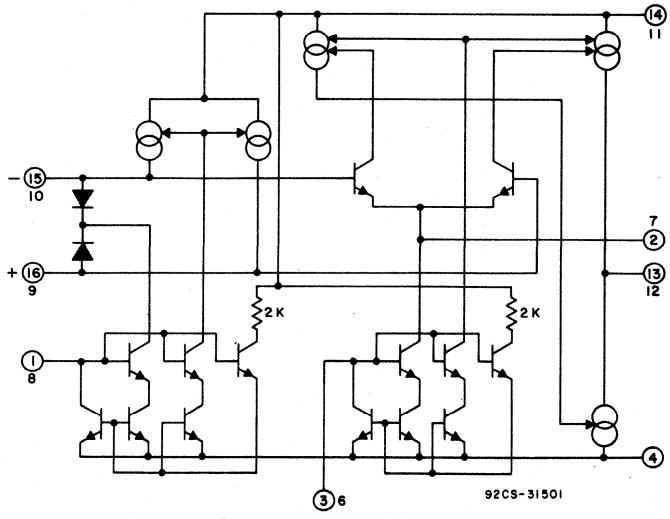


Fig. 1 — Functional diagram of 1/2 CA3280.

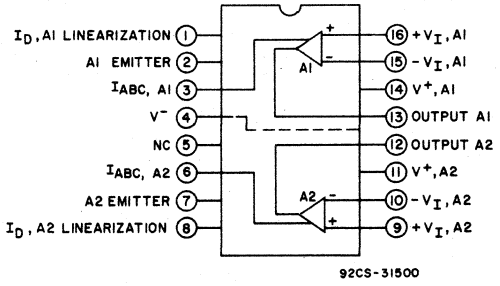
except that the forward transfer characteristic is best described by transconductance rather than voltage gain, and the output is current, not voltage. The magnitude of the output current is equal to the product of transconductance and the input voltage. This type of operational transconductance amplifier was first introduced by RCA in 1969*, and it has since gained wide acceptance as a gateable, gain-controlled building block for instrumentation and audio applications, such as linearization of transducer outputs, standardization of widely changing signals for data processing, multiplexing, instrumentation amplifiers operating from the nanopower range to high current and high-speed comparators.

* "OTA Obsoletes Op Amp," by C.F. Wheatley and H.A. Wittlinger, NEC Proceedings, December, 1969.

The CA3280 and CA3280A are supplied in the 16-lead dual-in-line plastic package (E suffix). The operating-temperature ranges are -55 to +125° C for the CA3280A and 0 to +70° C for the CA3280. The CA3280 is also supplied as a hermetic (H suffix).

Applications:

- **Voltage-controlled amplifiers**
- **Voltage-controlled filters**
- **Voltage-controlled oscillators**
- **Multipliers**
- **Demodulators**
- **Sample and hold**
- **Instrumentation amplifiers**
- **Function generators**
- **Triangle wave-to-sine wave converters**
- **Comparators**
- **Audio preamplifiers**



Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE RANGE	V^+ to V^-
INPUT SIGNAL CURRENT AT $I_D = 0$	100 μA
AMPLIFIER BIAS CURRENT	10 mA
OUTPUT SHORT CIRCUIT DURATION*	Indefinite
LINEARIZING DIODE BIAS CURRENT, I_D	5 mA
PEAK INPUT CURRENT WITH LINEARIZING DIODE	$\pm I_D$
POWER DISSIPATION, P_D:	
Either Amplifier	600 mW
Total Package	750 mW
Above 55°C	Derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE, T_A:	
Operating:	
CA3280	0 to +70°C
CA3280A	−55 to +125°C
Storage, All Types	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10 sec. max.	+265°C

* Short circuit may be applied to ground or to either supply.

CA3280, CA3280A

ELECTRICAL CHARACTERISTICS at T_A = 25°C, $V^{\pm}$ = 15 V (Unless Otherwise Stated) For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA3280			CA3280A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}	I_{ABC}=1 mA	–	–	3	–	–	0.5	mV
	I_{ABC}=100μA	–	0.7	3	–	0.25	0.5	
	I_{ABC}=10μA	–	–	3	–	–	0.5	
	I_{ABC}=1mA to 10μA T_A=full temp. range	–	0.8	4	–	0.8	1.5	
Input Offset Voltage Change, $\lvert\Delta V_{IO}\rvert$	I_{ABC}=1μA to 1mA	–	0.5	1	–	0.5	1	mV
	I_{ABC}=100μA T_A=full temp. range	–	5	–	–	3	5	μV/°C
Amplifier Bias Voltage, V_{ABC}	I_{ABC}=100μA	–	1.2	–	–	1.2	–	V
Peak Output Voltage: Positive VOM^+	I_{ABC}=500μA	12	13.7	–	12.5	13.7	–	V
Negative VOM^-		12	−14.3	–	−13.3	−14.3	–	
Positive VOM^+	I_{ABC}=5μA	12	13.9	–	12.5	13.9	–	
Negative VOM^-		12	−14.5	–	−13.5	−14.5	–	
Common-Mode Input Voltage Range, V_{ICR}	I_{ABC}=100μA	−13	–	13	−13	–	13	V
Noise Voltage, e_N: 10 Hz	I_{ABC}=500μA	–	20	–	–	20	–	$nV/\sqrt{Hz}$
1 kHz		–	8	–	–	8	–	$\mu V/\sqrt{Hz}$
10 kHz		–	7	–	–	7	–	$nV/\sqrt{Hz}$
Input Offset Current, I_{IO}	I_{ABC}=500μA	–	0.3	0.7	–	0.3	0.7	μA
Input Bias Current, I_{IB}	I_{ABC}=500μA	–	1.8	5	–	1.8	5	μA
	I_{ABC}=500μA T_A=full temp. range	–	3	8	–	3	8	
Peak Output Current: Source IOM^+	I_{ABC}=500μA	350	410	650	350	410	650	μA
Sink IOM^-		−350	−410	−650	−350	−410	−650	
Source IOM^+	I_{ABC}=5μA	3	4.1	7	3	4.1	7	
Sink IOM^-		−3	−4.1	−7	−3	−4.1	−7	
Sink and Source, IOM^-, IOM^+	I_{ABC}=500μA T_A=full temp. range	350	450	550	350	450	550	
Linearization Diodes: Dynamic Impedance	I_D = 100μA	–	700	–	–	700	–	Ω
Offset Current	I_D =100μA	–	10	–	–	10	–	μA
	I_D=10μA	–	0.5	1	–	0.5	1	

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA3280			CA3280A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Diode Network Supply Current	I_{ABC}=100μA	250	400	800	250	400	800	μA
Amplifier Supply Current (Per amplifier)	I_{ABC}=500μA	–	2	2.4	–	2	2.4	mA
Amplifier Output Leakage Current, I_{OL}	I_{ABC}=0, V_O=0V	–	0.015	0.1	–	0.015	0.1	nA
	I_{ABC}=0, V_O=30V	–	0.15	1	–	0.15	1	
Common-Mode Rejection Ratio, CMRR	I_{ABC}=100μA	80	100	–	94	100	–	dB
Power-Supply Rejection Ratio, PSRR	I_{ABC}=100μA	86	105	–	94	105	–	dB
Open-Loop Voltage Gain, A_{OL}	I_{ABC}=100μA, R_L=∞,	94	100	–	94	100	–	dB
	V_O=20 Vp-p	50K	100K	–	50K	100K	–	V/V
Forward Transconductance: Large Signal, Gm	I_{ABC}=50μA	–	0.8	1.2	–	0.8	1.2	mmho
Small Signal, gm	I_{ABC}=1mA	–	16	22	–	16	22	
Input Resistance, R_I	I_{ABC}=10μA	0.5	–	–	0.5	–	–	MΩ
Channel Separation	f=1 kHz	–	94	–	–	94	–	dB
Open-Loop Total Harmonic Distortion	f=1 kHz, I_{ABC}= 1.5 mA, R_L=15kΩ, V_O= 20 Vp-p	–	0.4	–	–	0.4	–	%
Bandwidth	I_{ABC}=1mA, R_L=100Ω	–	9	–	–	9	–	MHz
Slew Rate, SR: Open Loop	I_{ABC}=1mA	–	125	–	–	125	–	V/μs
Capacitance: Input, C_I	I_{ABC}=100μA	–	4.5	–	–	4.5	–	pF
Output, C_O		–	7.5	–	–	7.5	–	
Output Resistance, R_O	I_{ABC}=100μA	–	63	–	–	63	–	MΩ

Figs. 2 and 3 show the equivalent circuits for the current source and linearization diodes in the CA3280. The current through the linearization network is approximately equal to the programming current. There are several advantages to driving these diodes with a current source. First, only the offset current from the biasing network flows through the input resistor. Second, another input is provided to extend the gain control dynamic range. And third, the input is truly differential and can accept signals within the common-mode range of the CA3280.

The structure of the variable operational amplifier eliminates the need for matched resistor networks in differential to single-ended converters, as shown in Fig. 4. A matched resistor network requires ratio matching of 0.01% or trimming for 80 dB of common-mode rejection. The CA3280, with its excellent common-mode rejection ratio, is capable of converting a small (±25 mV) differential input signal to a single-ended output without the need for a matched resistor network.

Fig. 5 shows the CA3280 in a typical gain-control application. The input-signal range as a function of distortion at various levels of linearization diode current is shown in Fig. 6. This curve shows only the AGC capability of the diode network, but gain control can also be performed with the amplifier bias current (I_{ABC}). With no diode bias current, the gain is merely gmR_L. For example, with an I_{ABC} of 1 mA, the gm is approximately 16 mmhos. With the CA3280 operating into a 5 kΩ resistor, the gain is 80.

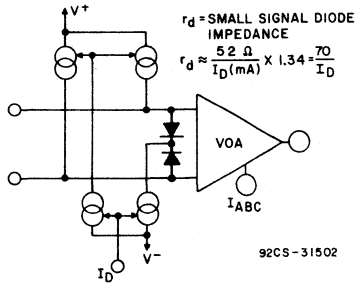


Fig. 2 – VOA showing linearization diodes and current drive.

The need for external buffers can be eliminated by the use of low-value load resistors, but the resulting increase in the required amplifier bias current reduces the input impedance of the CA3280. The linearization diode impedance also decreases as the diode bias current increases, which further loads the input. The diodes, in addition to acting as a linearization network, also operate as an additional attenuation system to accommodate input signals in the volt range when they are applied through appropriate input resistors.

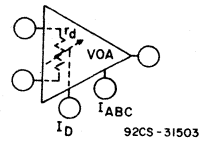


Fig. 3 – Block diagram of linearized VOA.

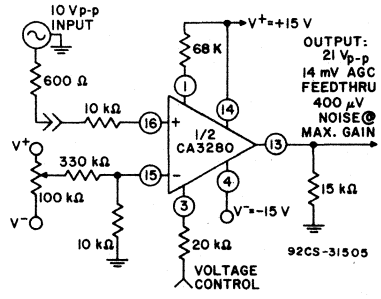


Fig. 5 – Typical gain control circuit.

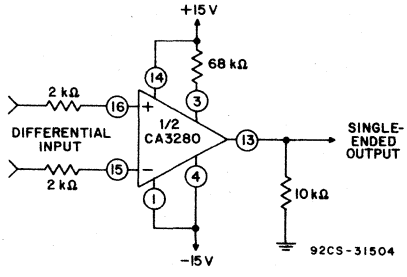


Fig. 4 – Differential to single-ended converter.

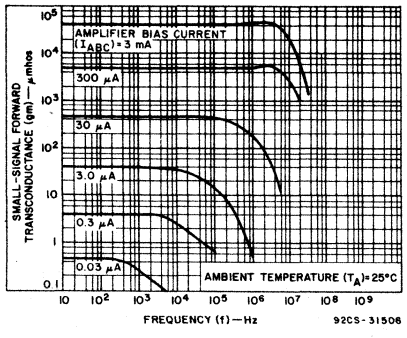


Fig. 6 – Amplifier gain as a function of frequency.

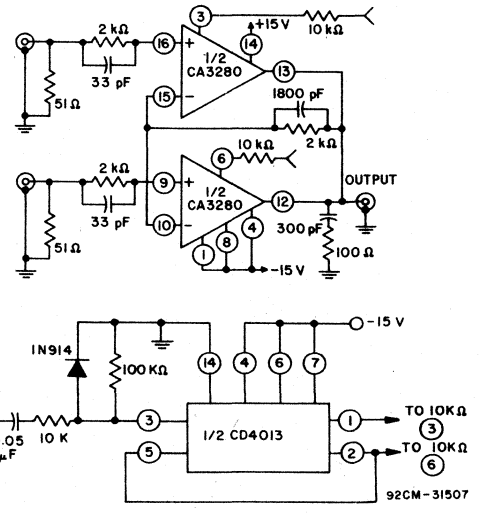


Fig. 7 – Two-channel linear multiplexer.

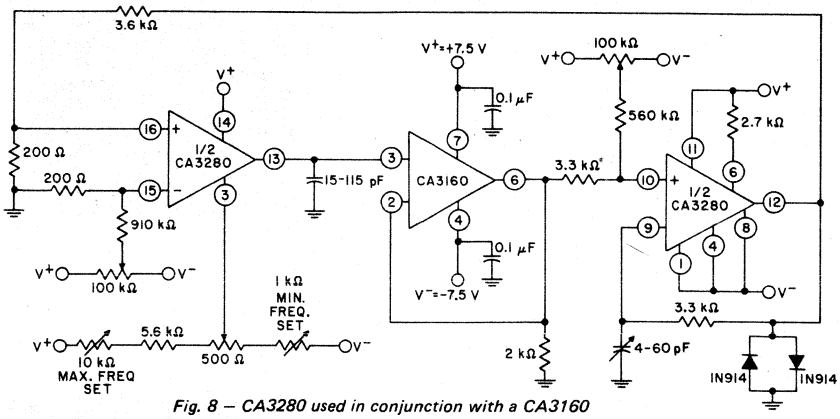


Fig. 8 – CA3280 used in conjunction with a CA3160 to provide a function generator with a tunable range of from 2 Hz to 1 MHz.

Fig. 9 shows a triangle wave-to-sine wave converter using the CA3280. Two 100KΩ resistors are connected between the differential amplifier emitters and V^+ to reduce the current flow through the differential amplifier. This allows the amplifier to fully cut off during peak input signal excursions. THD is approximately 0.37% for this circuit.

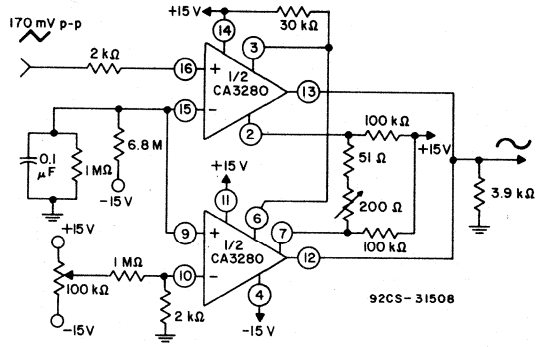


Fig. 9 – Triangle wave-to-sine wave converter.

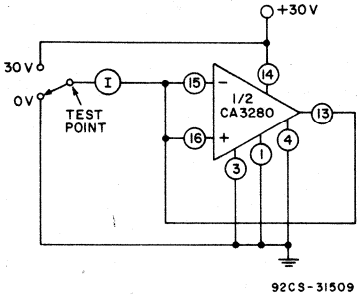


Fig. 10 – Leakage current test circuit.

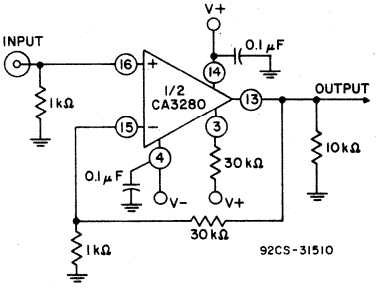
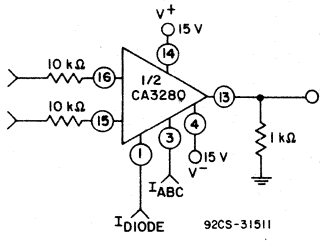
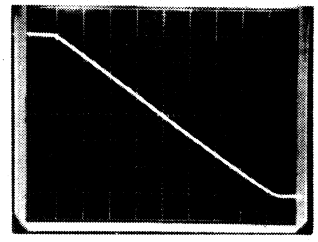
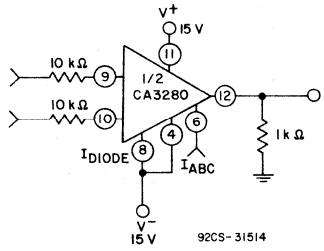


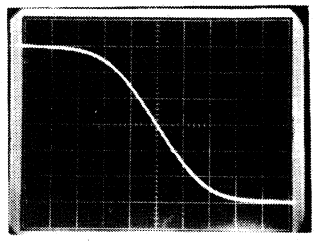
Fig. 11 – Channel separation test circuit.





a) With diode programming terminal active





b) With diode programming terminal cut-off

Fig. 12 – CA3280 transfer characteristics.

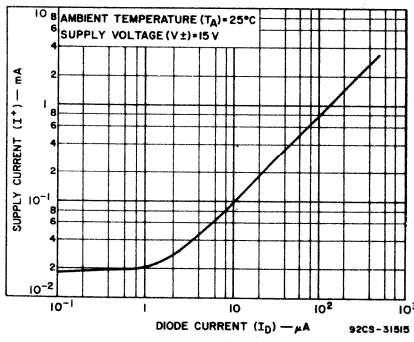


Fig. 13 – Supply current as a function of diode current.

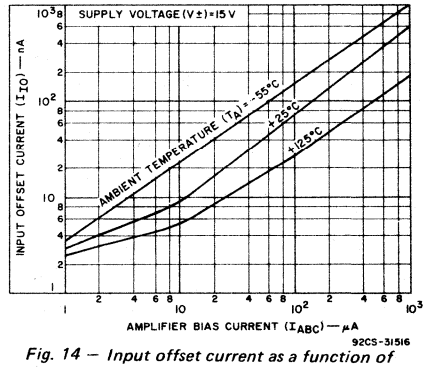


Fig. 14 – Input offset current as a function of amplifier bias current.

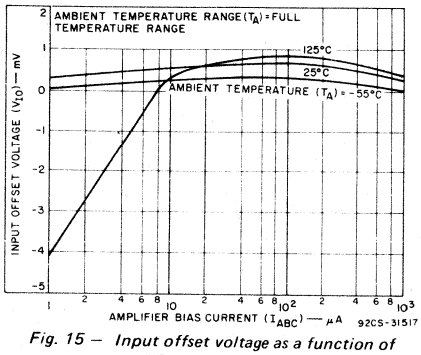


Fig. 15 – Input offset voltage as a function of amplifier bias current.

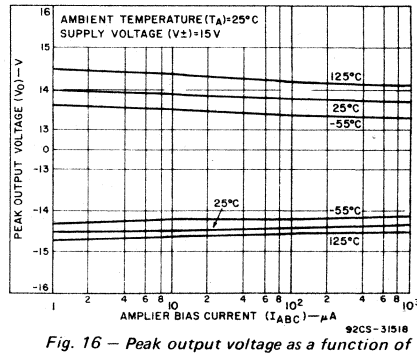


Fig. 16 – Peak output voltage as a function of amplifier bias current.

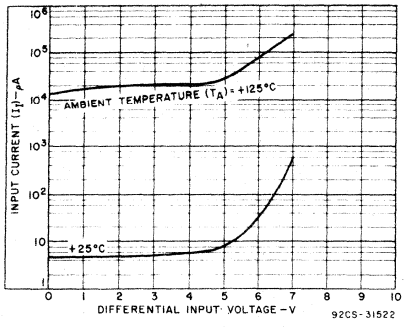


Fig. 17 – Input current as a function of input differential voltage.

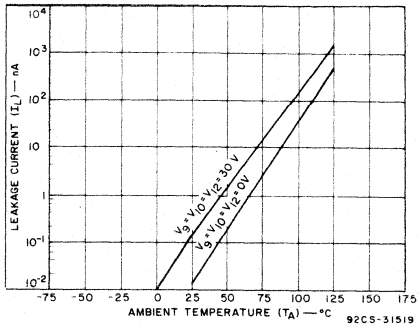


Fig. 18 – Leakage current as a function of temperature.

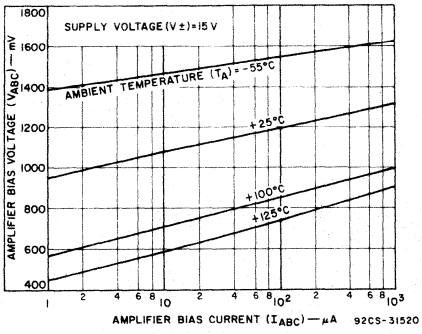


Fig. 19 – Amplifier bias voltage as a function of amplifier bias current.

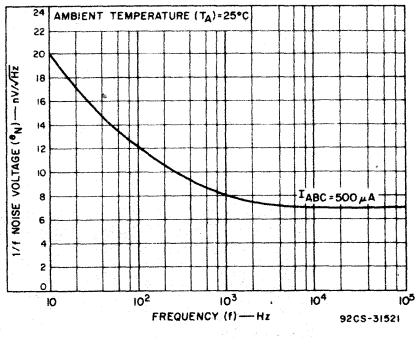


Fig. 20 – I/F noise as a function of frequency.

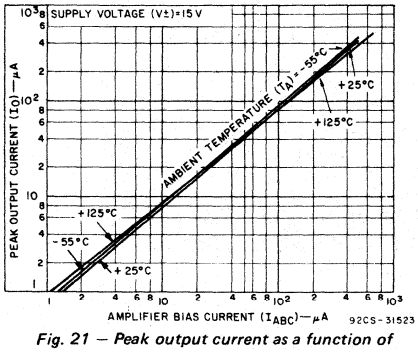


Fig. 21 – Peak output current as a function of amplifier bias current.

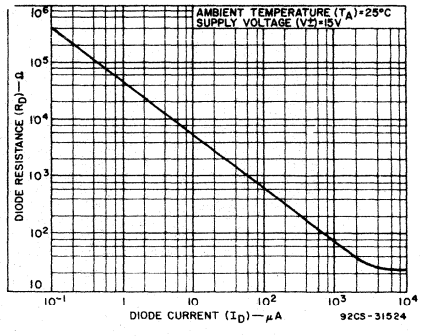


Fig. 22 – Diode resistance as a function of diode current.

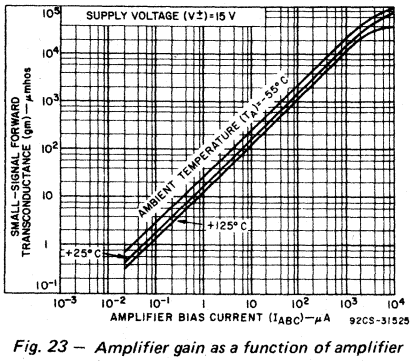


Fig. 23 – Amplifier gain as a function of amplifier bias current.

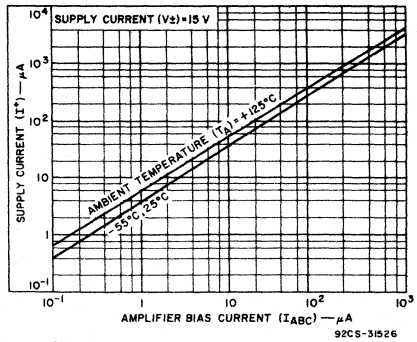


Fig. 24 – Supply current as a function of amplifier bias current.

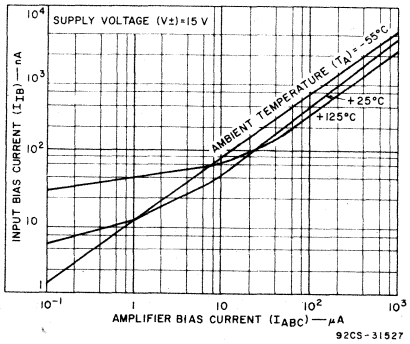
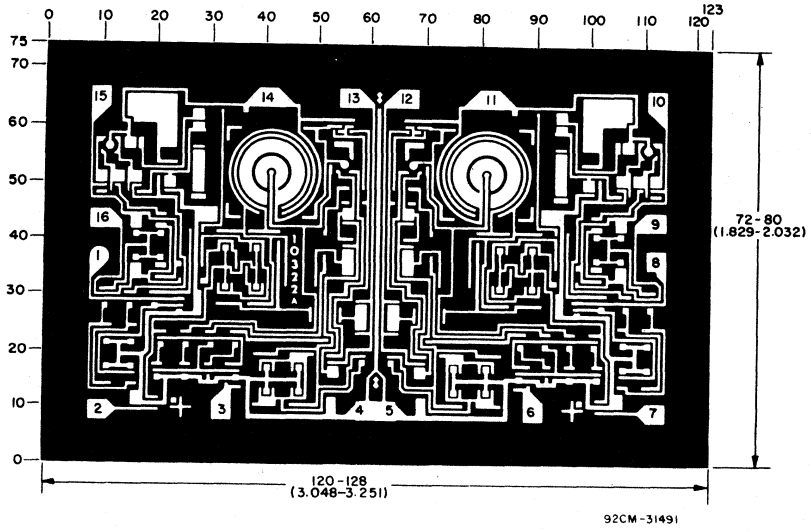


Fig. 25 – Input bias current as a function of amplifier bias current.



Dimensions and pad layout for CA3280H.

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Voltage Comparators
Technical Data

+Programmable
*BIMOS types

CA311

S-Suffix Types
(DIL-CAN)

H-1787

T-Suffix Types
(TO-5 Style)

H-1528

E-Suffix Types
(Mini-DIP)

H-1817

Voltage Comparator

For Commercial and Industrial Applications

Features:

- *Single- or dual-supply operation*
- *Power consumption - 135 mW at ±15 V*
- *Strobe capability*
- *Low input-offset current - 6 nA(typ.)*
- *Differential input-voltage range - ±30 V*
- *Directly interchangeable with National Semiconductor LM311 Series*

Applications:

- *Multivibrators*
- *Positive and negative peak detectors*
- *Crystal oscillators*
- *Zero-crossing detectors*
- *Solenoid, relay, and lamp drivers*

The RCA CA311 is a monolithic voltage comparator that operates from dual supplies up to ±15 V, or from single supplies down to 5 V. This single supply capability makes the outputs of these devices compatible with RTL, DTL, TTL, and MOS circuits. In addition they can drive lamps or relays, and switch voltages up to 40 V at currents as high as 50 mA.

The inputs and outputs of the CA311 can be isolated from system ground, allowing the output to drive loads referred to ground V^+, or V^-.

The CA311 is available in 8-lead TO-5 style packages with standard leads (T suffix), dual-in-line formed leads ("DIL-CAN", S suffix), 8-lead dual-in-line plastic package ("MINI-DIP", E suffix), and in chip form (H suffix).

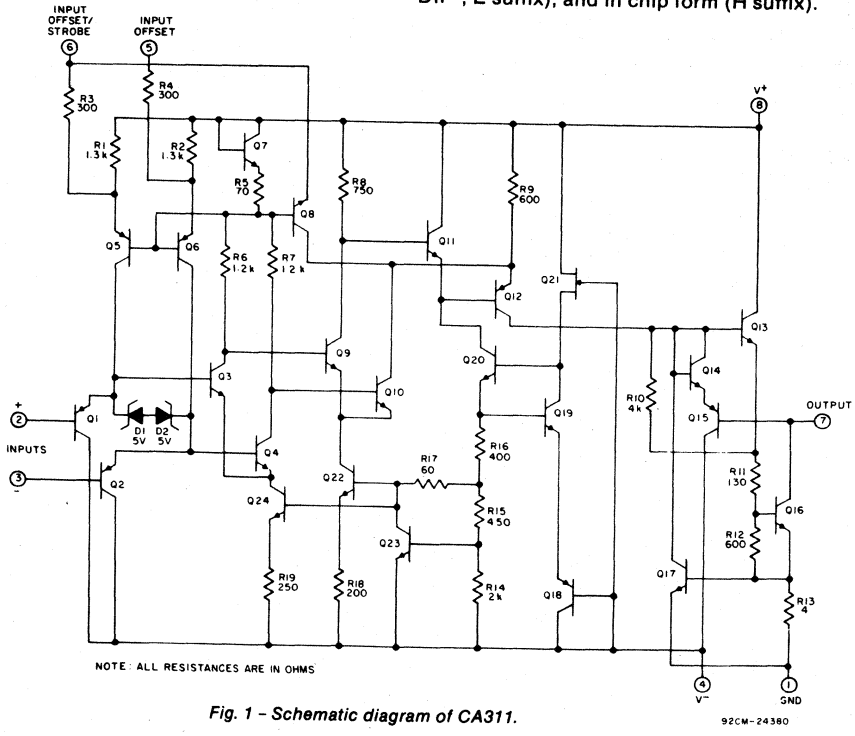


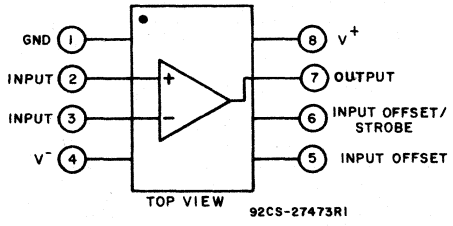
Fig. 1 - Schematic diagram of CA311.

Maximum Ratings, *Absolute Maximum Values at T_A = 25°C:*

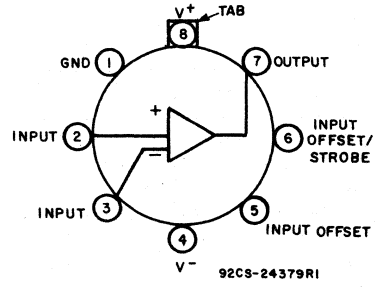
DC SUPPLY VOLTAGE (between V+ and V⁻ terminals) ..... 36 V
DC INPUT VOLTAGE* ..... ±15 V
DIFFERENTIAL INPUT VOLTAGE ..... ±30 V
OUTPUT TO NEGATIVE SUPPLY VOLTAGE (V_{7-4}) ..... 40 V
GROUND TO NEGATIVE SUPPLY VOLTAGE (V_{1-4}) ..... 30 V
OUTPUT SHORT-CIRCUIT DURATION ..... 10 s
DEVICE DISSIPATION:
  UP TO T_A = 25°C ..... 500 mW
  Above T_A = 25°C ..... derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:
  Operating ..... 0 to +70°C†
  Storage ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

*This rating applies for ±15 V supplies. The positive input-voltage limit is 30 V above the negative supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.

†Types CA311 E, S, and T can be operated over the temperature range of -55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70°C.



FUNCTIONAL DIAGRAM FOR PLASTIC PACKAGE.



FUNCTIONAL DIAGRAM FOR TO-5 STYLE PACKAGE.

TYPICAL CHARACTERISTICS

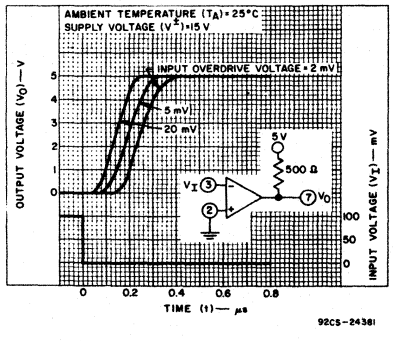


Fig. 2 - Response time for various input overdrive voltages - positive input.

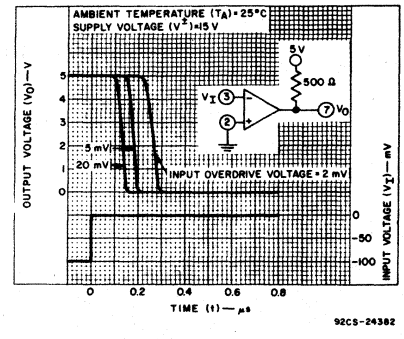


Fig. 3 - Response time for various input overdrive voltages - negative input.

CA311

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS		LIMITS			UNITS
		SUPPLY VOLTAGE (V±) = 15V UNLESS OTHERWISE SPECIFIED		CA311			
				MIN.	TYP.	MAX.	
Input Offset Voltage	V_{IO}	$R_S \leq 5$ kΩ, Note 2	T_A = 25°C	—	2	7.5	mV
			Note 1	—	—	10	
Saturation Voltage		$V_I \leq$ -10 mV, I_O = 50 mA	T_A = 25°C	—	0.75	1.5	V
		$V^+ \geq 4.5$ V, V^- -0, $V_I \leq$ -10 mV, $I_{SINK} \leq 8$ mA	Note 1	—	0.23	0.4	
Input Voltage Range	V_{IPP}		Note 1	—	±14	—	V
Input Offset Current	I_{IO}	Note 2	T_A = 25°C	—	6	50	nA
			Note 1	—	—	70	
Input Bias Current	I_{IB}	Note 2	T_A = 25°C	—	100	250	nA
			Note 1	—	—	300	
Postive Supply Current	I^+		T_A = 25°C	—	5.1	7.5	mA
Negative Supply Current	I^-		T_A = 25°C	—	4.1	5	mA
Output Leakage Current		$V_I \geq$ 10 mV, V_O = 35 V	T_A = 25°C	—	—	50	nA
Strobe on Current			T_A = 25°C	—	3	—	mA
Voltage Gain, A			T_A = 25°C	40	200	—	V/mV
Response Time		100 mV Input Step with 5 mV Overdrive Voltage	T_A = 25°C	—	200	—	ns
Input Voltage Range			T_A = 25°C	-14.5	13.8- -14.7	13	V

Note 1: Ambient temperature (T_A) over applicable operating temperature of 0 to + 70° C.

Note 2: The input offset characteristics given are the values required to drive the output to within 1 V of either supply with a 1 mA load. These characteristics define an error band which takes into account the worst-case effects of voltage gain and input impedance. The input offset voltage, input offset current, and input bias current specifications apply for any supply voltage from a 5 V single supply up to a ± 15 V dual supply.

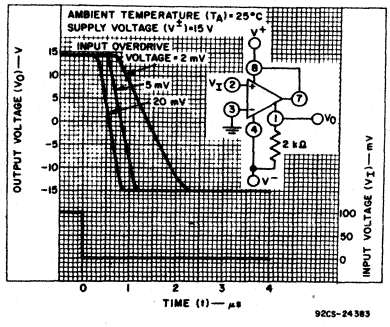


Fig. 4 - Response time for various input overdrive voltages - positive input.

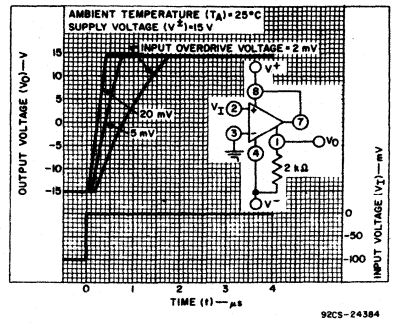


Fig. 5 - Response time for various input overdrive voltages - negative input.

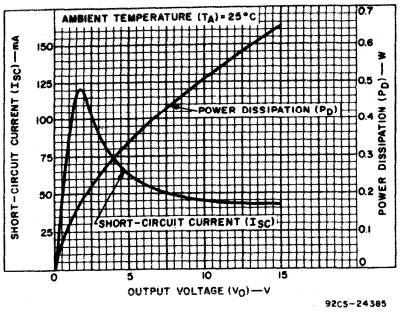


Fig. 6 - Output limiting characteristics.

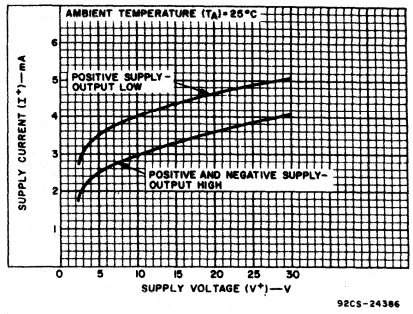


Fig. 7 - Supply current vs. supply voltage.

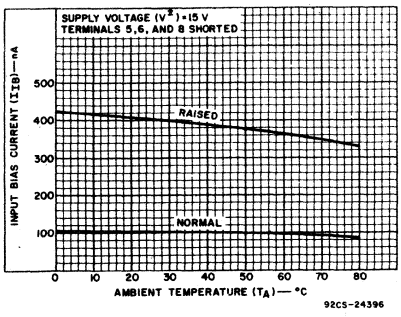


Fig. 8 - Input bias current vs. ambient temperature.

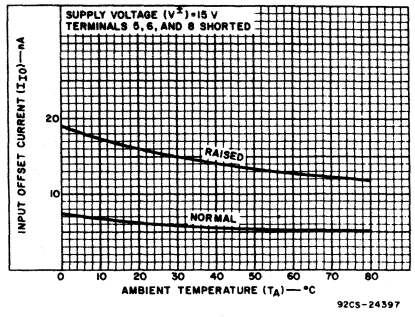


Fig. 9 - Input offset current vs. ambient temperature.

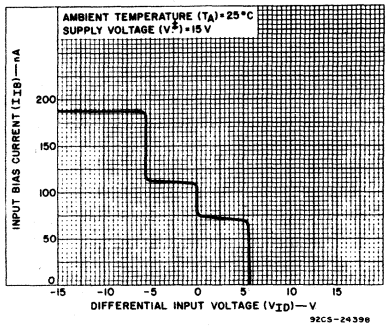


Fig. 10 - Input characteristics.

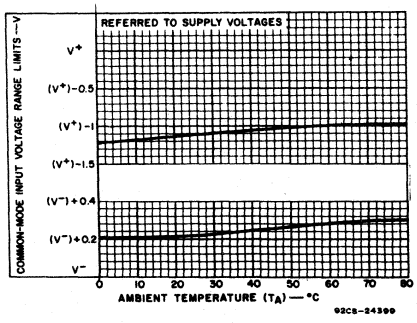


Fig. 11 - Common-mode voltage range limits vs. ambient temperature.

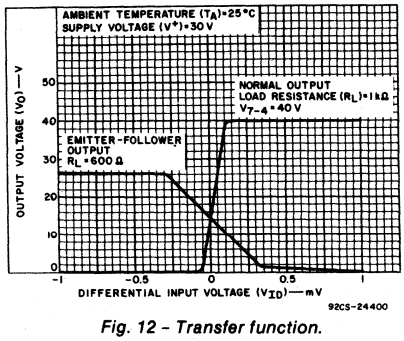


Fig. 12 - Transfer function.

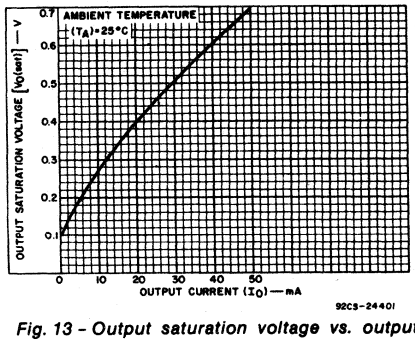


Fig. 13 - Output saturation voltage vs. output current.

CA311

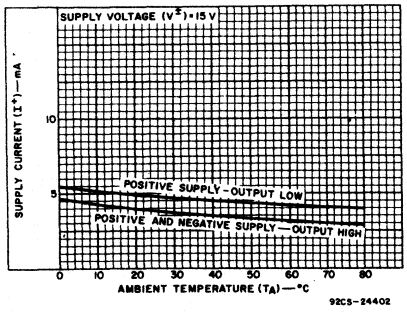


Fig. 14 - Supply current vs. ambient temperature.

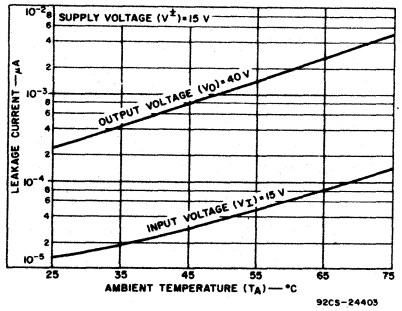


Fig. 15 - Input and output leakage current vs. ambient temperature.

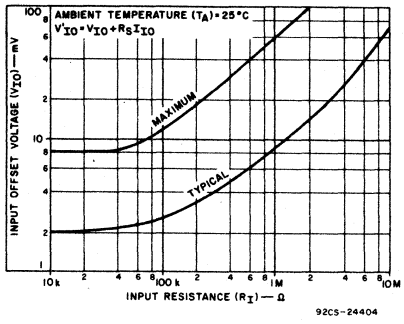


Fig. 16 - Offset error.

TYPICAL APPLICATIONS

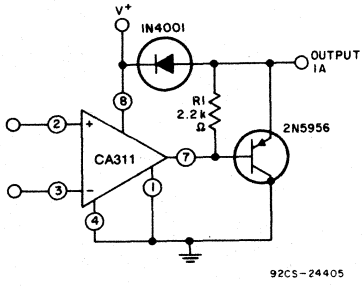


Fig. 17 - Comparator and solenoid driver.

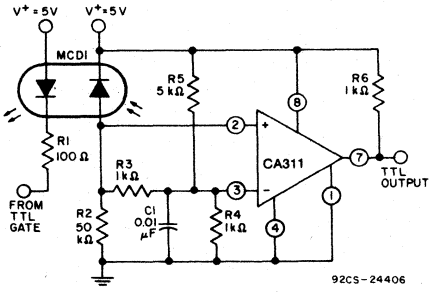


Fig. 18 - Digital transmission isolator.

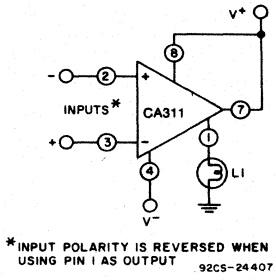


Fig. 19 - Driving a ground-referred load.

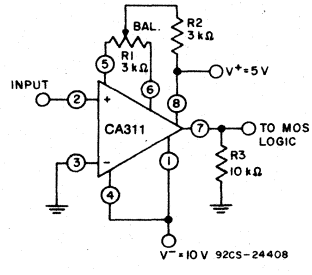


Fig. 20 - Zero-crossing detector driving MOS logic.

TYPICAL APPLICATIONS (cont'd)

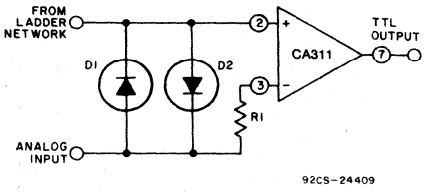


Fig. 21 - Using clamp diodes to improve response.

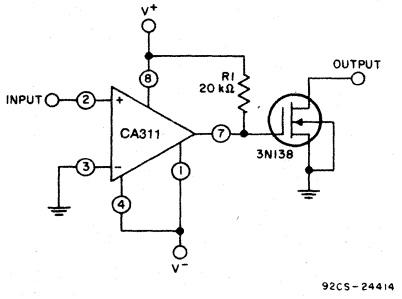


Fig. 23 - Zero-crossing detector driving and MOS switch.

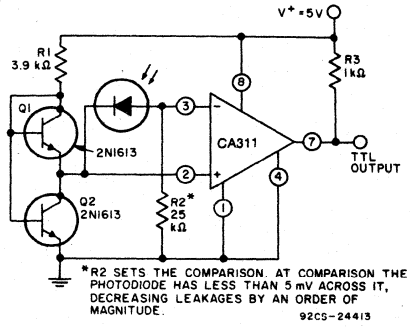


Fig. 25 - Precision photodiode comparator.

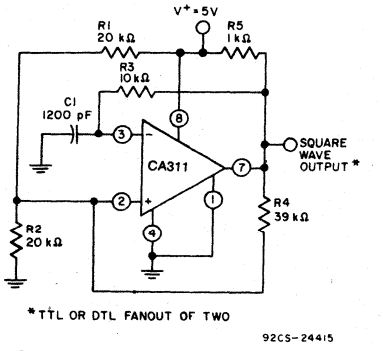


Fig. 26 - 100-kHz free-running multivibrator.

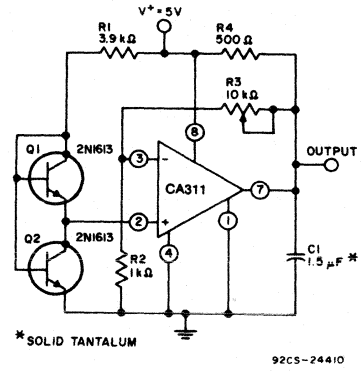


Fig. 22 - Low-voltage adjustable-reference supply.

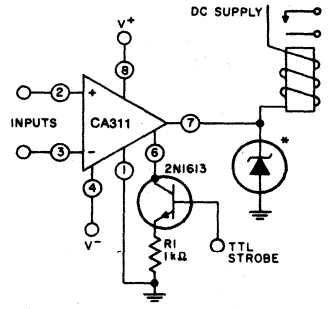


Fig. 24 - Relay driver with strobe.

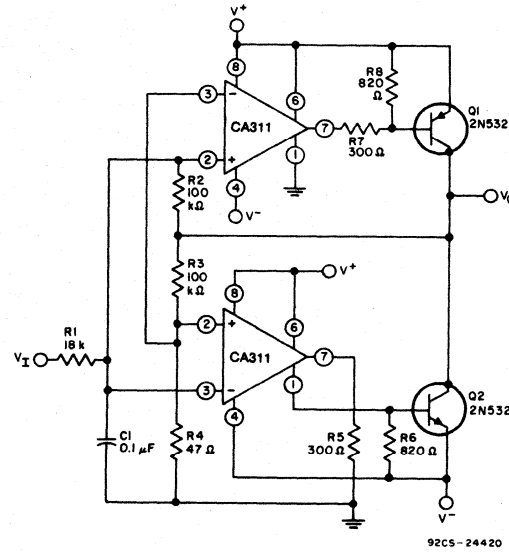


Fig. 27 - Switching power amplifier.

TYPICAL APPLICATIONS (cont'd)

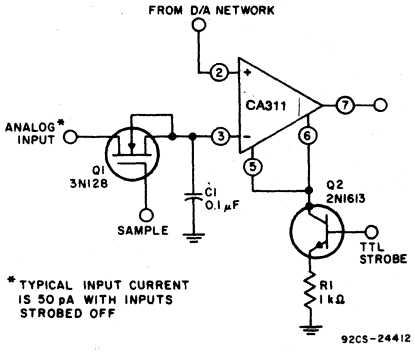


Fig. 28 - Strobing off both input and output stages.

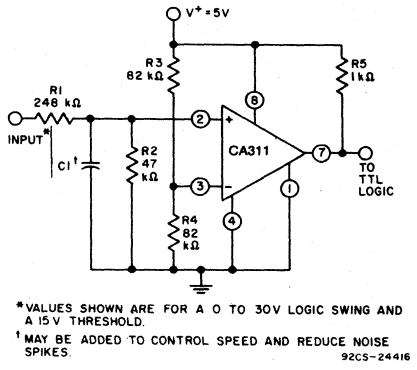


Fig. 29 - TTL interface with high-level logic.

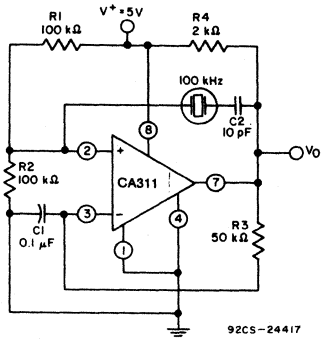


Fig. 30 - Crystal oscillator.

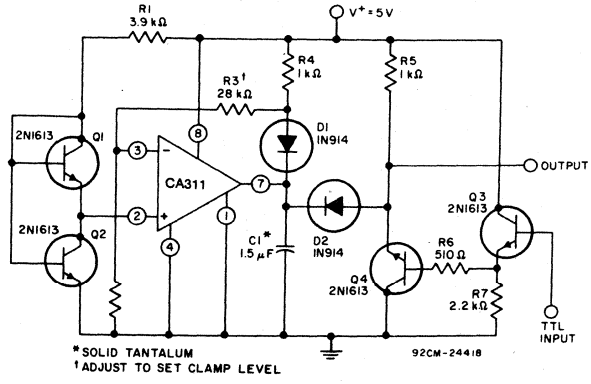


Fig. 31 - Precision squarer.

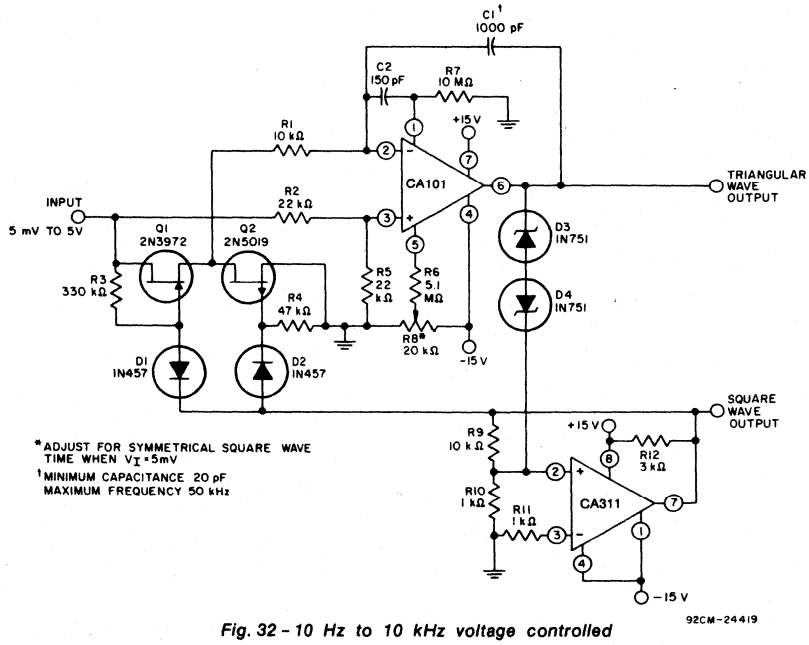


Fig. 32 - 10 Hz to 10 kHz voltage controlled oscillator.

TYPICAL APPLICATIONS (cont'd)

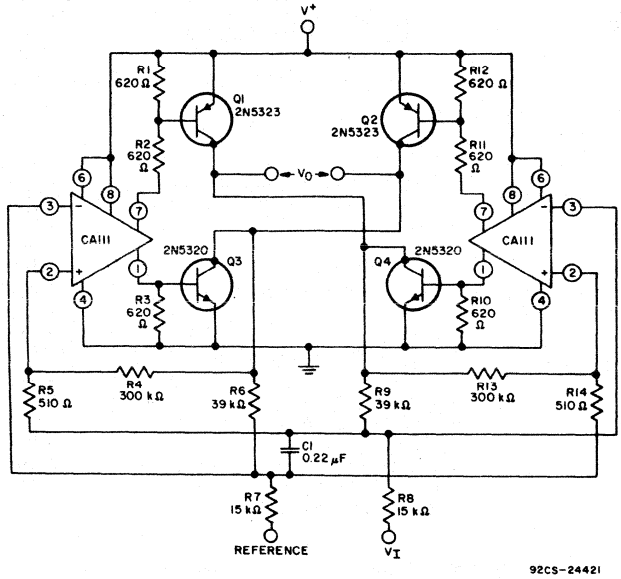
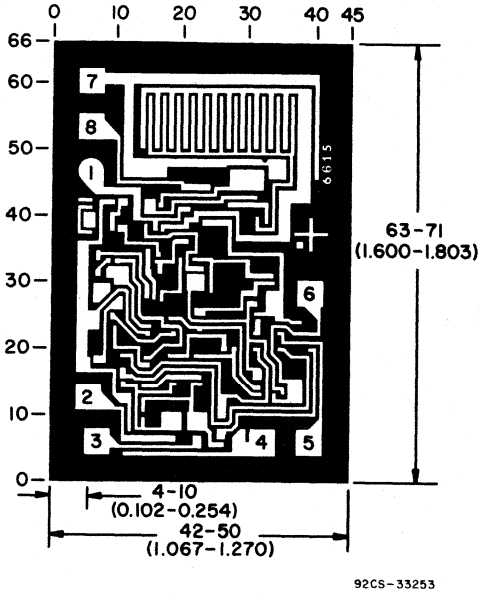


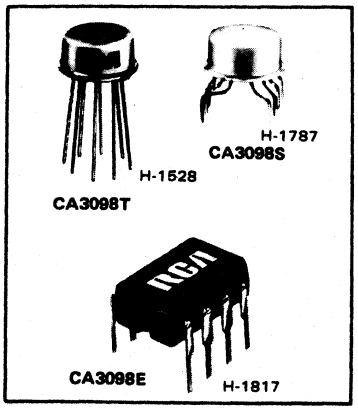
Fig. 33 - Switching power amplifier.



Dimensions and pad layout for CA311H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3098



Programmable Schmitt Trigger — With Memory

— Dual-Input Precision Level Detectors

Features:

- *Programmable operating current*
- *Micropower standby dissipation*
- *Direct control of currents up to 150 mA*
- *Low input on/off current of less than 1 nA for programmable bias current of 1 μA*
- *Built-in hysteresis: 20 mV max.*
- *Programmable hysteresis: 20 mV to V+*
- *Dual reference input*
- *High sensor range: 100 Ω to 100 MΩ*
- *Stable predictable switching levels*
- *Temperature-compensated reference voltage*
- *Power can be strobed off via term. 2*

Applications:

- *Control of relays, heaters, LED's lamps, photo-sensitive devices, thyristors, solenoids, etc.*
- *Signal reconditioning*
- *Phase and frequency modulators*
- *On/off motor switching*
- *Schmitt triggers, level detectors*
- *Time delays*
- *Overvoltage, overcurrent, over-temperature protection*
- *Battery-operated equipment*
- *Square and triangular-wave generators*

The RCA-CA3098 Programmable Schmitt Trigger is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3098 can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with maximum operating voltage of ±8 volts. It can directly control currents up to 150 mA and operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3098 contains the following major circuit-function features (see Fig. 1):

1. Differential amplifiers and summer: the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.

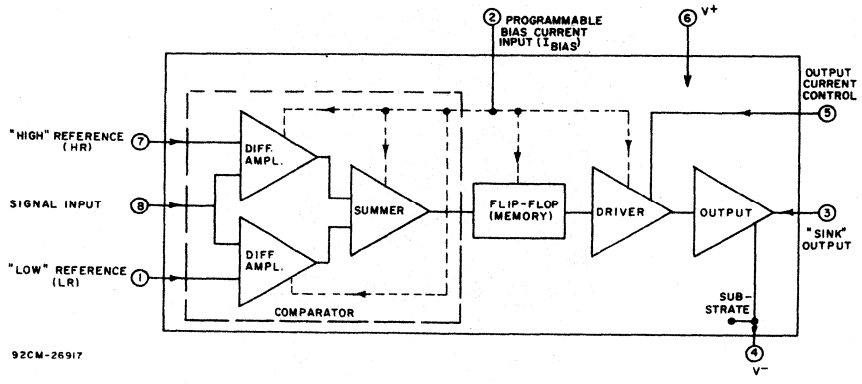


Fig. 1 — Block diagram of CA3098 programmable Schmitt trigger.

2. Flip-flop: the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. Driver and otuput stages: these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. Programmable operating current: the circuit incorporates access at terminal 2 to permit programming the desired quiescent operating current and performance parameters.

The CA3098 is supplied in the 8-lead dual-in-line plastic package ("Mini-Dip", E suffix), 8-lead TO-5 style package (T suffix), 8-lead TO-5-style package with formed leads "DIL-CAN" (S suffix), and in chip form (H suffix).

For information on another RCA Dual-Input Precision Level Detector, see the data bulletin for the RCA-CA3099E, File No. 620.

ELECTRICAL CHARACTERISTICS at T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	Fig. No.	LIMITS			UNITS
			Min.	Typ.	Max.	
Input Offset Voltage: "Low" Ref., $V_{IO(LR)}$	V_{LR} = Gnd, V_{HR} = 3 V, I_{BIAS} = 100 μA	5	−15	−3	6	mV
"High" Ref., $V_{IO(HR)}$	V_{HR} = Gnd, V_{LR} = −3 V, I_{BIAS} = 100 μA	6	−10	±10	10	
Temp. Coeff: "Low" Ref.	−55 °C to + 125 °C	7	–	4.5	–	μV/°C
"High" Ref.	−55 °C to + 125 °C	8	–	±8.2	–	
Min. Hysteresis Voltage $V_{IO(HR-LR)}$:	V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	9	–	3	20	mV
Temp. Coeff.	−55°C to + 125 °C	10	–	6.7	–	μV/°C
Output Saturation Voltage, $V_{CE(SAT)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	11,12	–	0.72	1.2	V
Total Supply Current, I_{TOTAL}: "ON"	V_I = 4 V, V_{REG} = 6 V; V^+ = 12 V, I_{BIAS} = 100 μA	13,14	500	710	800	μA
"OFF"	V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA		400	560	750	μA
Input Bias Current, I_{IB}: $I_{B(p-n-p)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	15	–	42	100	nA
$I_{B(n-p-n)}$	V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA		–	28	100	nA
Output Leakage Current, $I_{CE(OFF)}$	Current from Term. 3 when Q46 is "OFF"	–	–	–	10	μA
Switching Times: Delay, t_d	I_C = 100 μA, I_{BIAS} = 100 μA, V^+ = 5 V, V_{REG} = 2.5 V	18	–	600	–	ns
Fall, t_f			–	50	–	ns
Rise, t_r			–	500	–	ns
Storage, t_s			–	4.5	–	μs
Output Current, I_O	V^+ = 12 V, I_{BIAS} = 50 μA	–	100	–	–	mA

Maximum Ratings, *Absolute-Maximum Values at* $T_A = 25°C$*:*

Supply Voltage Between Terminals 6 and 4,	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4	16	V
Differential Input Voltage Between Terminals 8 and 1, and Terminals 7 and 8	10	V
Operating Voltage Range:		
Term. 8	V^- to V^+	
Term. 7	(V^- plus 2.0 V) to V^+	
Term. 1	(V^-) to (V^+ minus 2.0 V)	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programmable Bias Current (Term. 2)	1	mA
Output Current Control (Term. 5)	15	mA
Power Dissipation:		
Without Heat Sink:		
Up to $T_A = 55°C$		
CA3098S, CA3098T	630	mW
CA3098E	630	mW
Above $T_A = 55°C$ Derate linearly at	6.67	mW/°C
With Heat Sink:		
Up to $T_A = 55°C$		
CA3098S, CA3098T	1.6	W
Above $T_A = 55°C$		
CA3098S, CA3098T Derate linearly at	16.67	mW/°C
Ambient Temperature Range (All Packages):		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

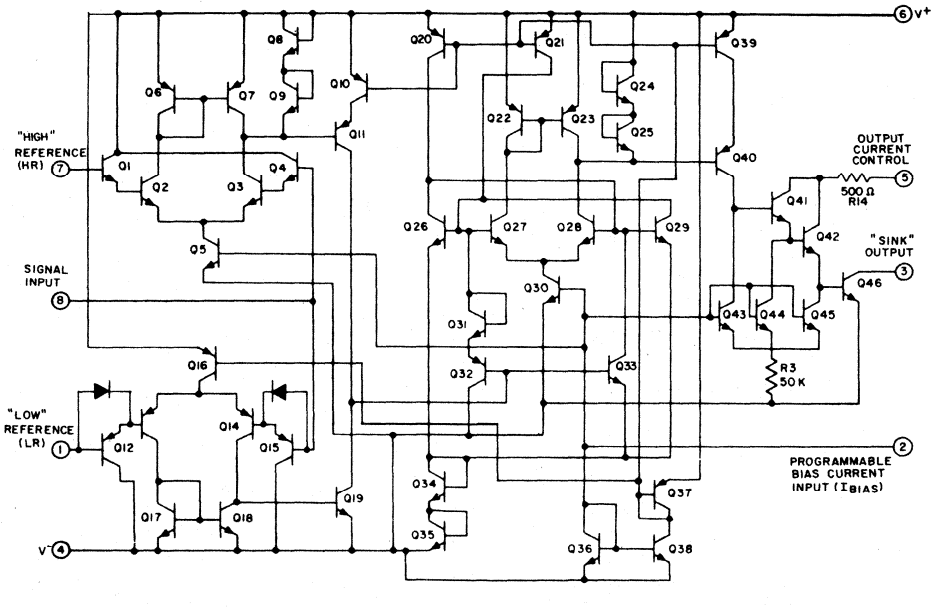


Fig. 2 – Schematic Diagram of CA3098.

General Description of Circuit Operation (Refer to Figs. 2, 3, 4)

When the signal-input voltage of the CA3098 is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

The CA3098 comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{bias}) supplied to terminal 2.

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 5. Figs. 3 and 4 highlight the operation of the CA3098 when connected as a simple hysteresis switch (Schmitt trigger).

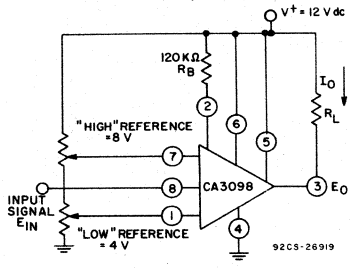


Fig. 3 – Basic hysteresis switch (Schmitt trigger).

Sequence	Input Signal Level	Output Voltage (V) (Term. 3)
1	$4 \geqslant E_{IN} > 0$	0
2	$8 \geqslant E_{IN} > 4$	0
3	$E_{IN} > 8$	12
2	$8 \geqslant E_{IN} > 4$	12
1	$4 \geqslant E_{IN} > 0$	0

Fig. 4 – Resultant output states of the CA3098, shown in Fig. 3 as a function of various input signal levels.

TYPICAL CHARACTERISTIC CURVES

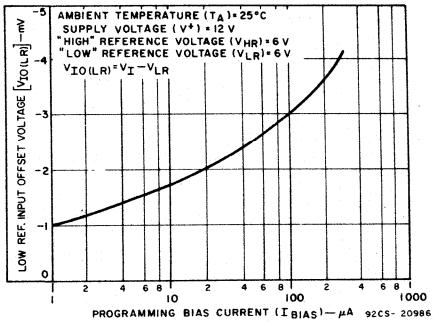


Fig. 5 – Input-offset voltage ("low" reference) vs. programming bias current.

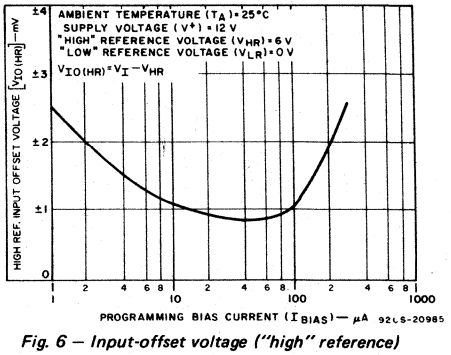


Fig. 6 – Input-offset voltage ("high" reference) vs. programming bias current.

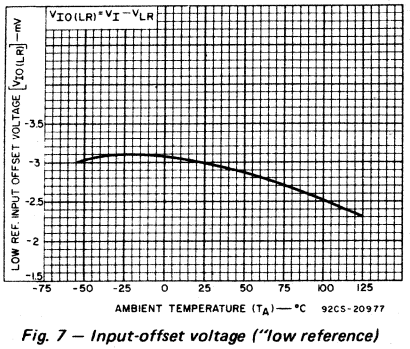


Fig. 7 – Input-offset voltage ("low reference) vs. ambient temperature.

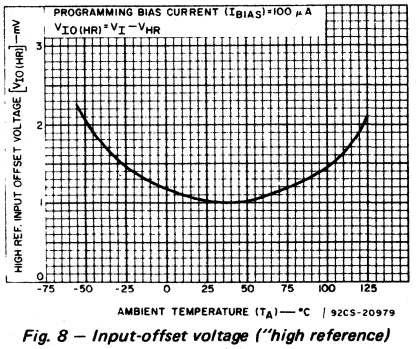


Fig. 8 – Input-offset voltage ("high reference) vs. ambient temperature.

TYPICAL CHARACTERISTIC CURVES (Cont'd)

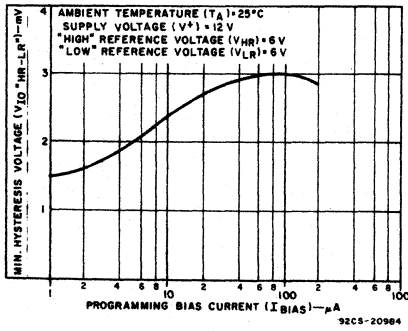


Fig. 9 – Min. hysteresis voltage vs. programming bias current.

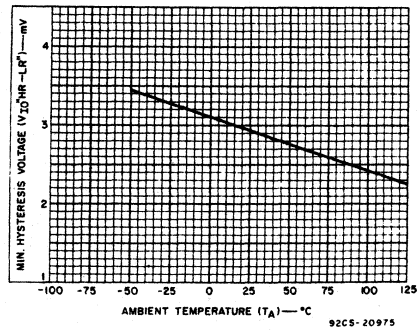


Fig. 10 – Min. hysteresis voltage vs. ambient temperature.

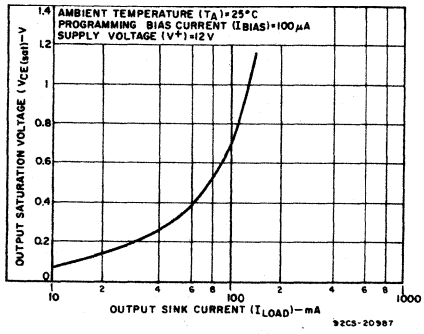


Fig. 11 – Output saturation voltage vs. output sink current.

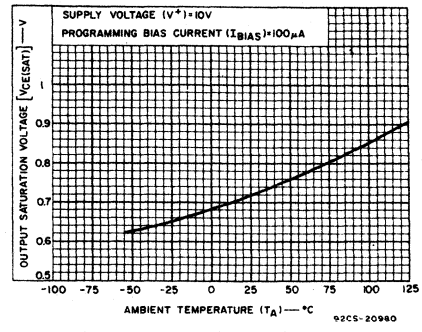


Fig. 12 – Output saturation voltage vs. ambient temperature.

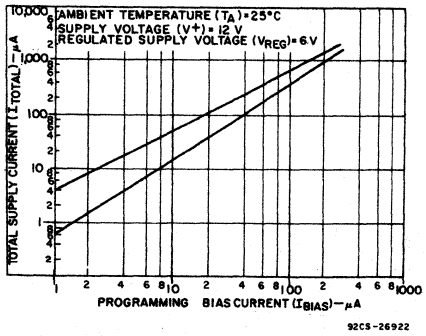


Fig. 13 – Total supply current vs. programming bias current.

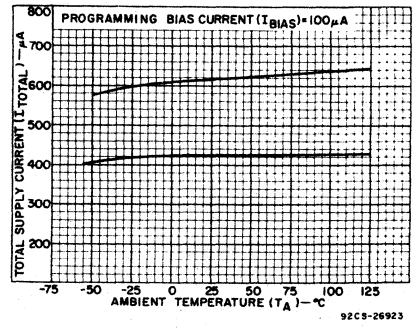


Fig. 14 – Total supply current vs. ambient temperature.

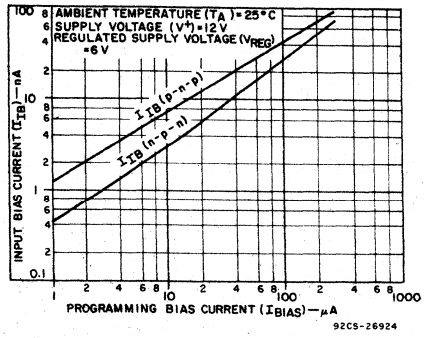


Fig. 15 – Input bias current vs. programming bias current.

TEST CIRCUIT

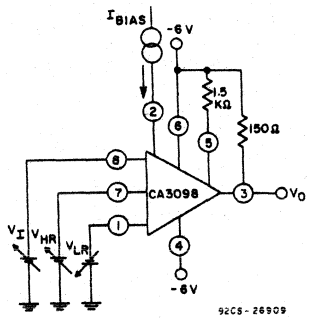


Fig. 16 – Input-offset voltage test circuit.

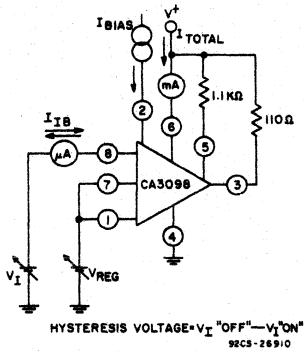


Fig. 17 – Min. hysteresis voltage, total supply current, and input-bias-current test circuit.

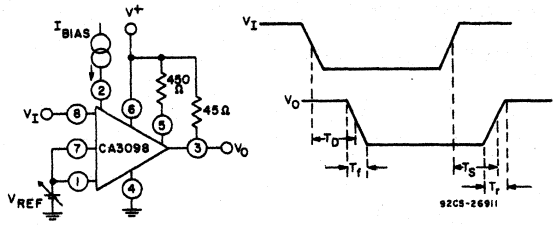


Fig. 18 – Switching time test circuit.

TYPICAL APPLICATIONS

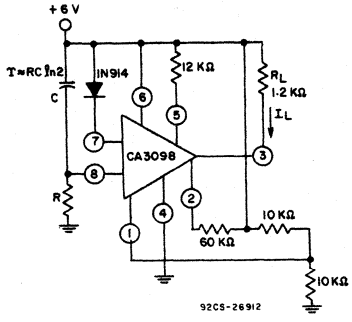


Fig. 19 – Time delay circuit: Terminal 3 "sinks" after τ seconds.

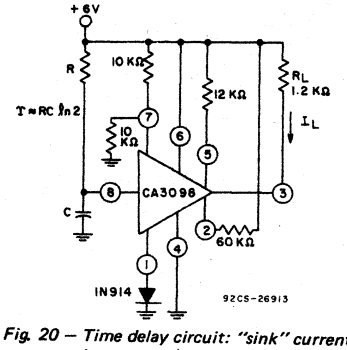


Fig. 20 – Time delay circuit: "sink" current interrupted after τ seconds.

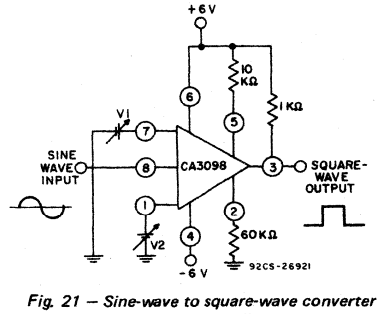
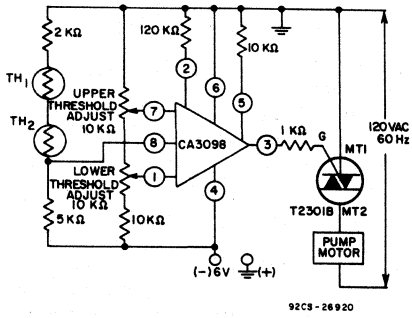


Fig. 21 – Sine-wave to square-wave converter with duty-cycle adjustment (V_1 and V_2).

TYPICAL APPLICATIONS (Cont'd)



Notes (a) Motor pump is "ON" when water level rises above thermistor TH_2.
(b) Motor pump remains "ON" until water level falls below thermistor TH_1.
(c) Thermistors, operate in self-heating mode.

Fig. 22(a) – Water-level control.

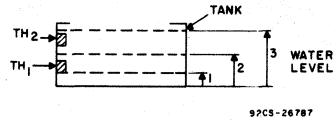


Fig. 22(b) – Water level diagram for circuit of Fig. 22(a).

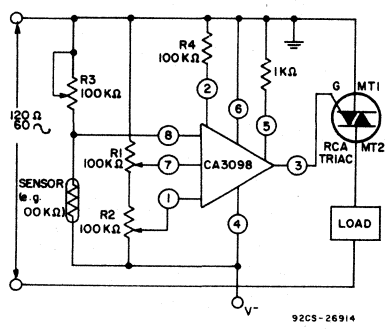


Fig. 23 – OFF/ON control of triac with programmable hysteresis.

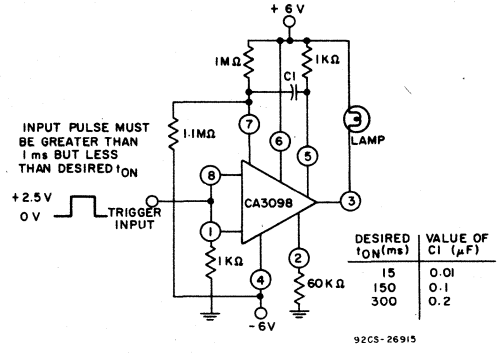
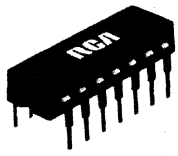


Fig. 24 – One-shot multivibrator.

CA3099E

Programmable Comparator - - With Memory



14-Lead Dual-in-Line Plastic Package H-1517

Features:

- Programmable operating current
- Micro-power standby dissipation
- Directly controls current up to 150 mA
- Low input on/off current of less than 1 nA for programmable bias current of 1 μA
- Built-in hysteresis: 10 mV max.
- Programmable hysteresis: 10 mV to V^+
- Dual reference input
- High sensor range: 100 Ω to 100 MΩ
- Stable predictable switching levels
- Temperature-compensated reference voltage

Applications:

- Control of relays, heaters, LED's, lamps, photo-sensitive devices, thyristors, solenoids, etc.
- Signal reconditioning
- Phase and frequency modulators
- On/off motor switching
- Schmitt triggers, level detectors
- Time delays
- Overvoltage, overcurrent, overtemperature protection
- Battery-operated equipment
- Square and triangular-wave generators

RCA-CA3099E* Programmable Comparator is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3099E can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with a maximum operating voltage of ± 8 volts. It can directly control currents up to 150 mA. It operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3099E contains the following six (6) major circuit-function features (Figure 1):

1. **Differential amplifiers and summer;** the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.

* Formerly Developmental No. TA6189.

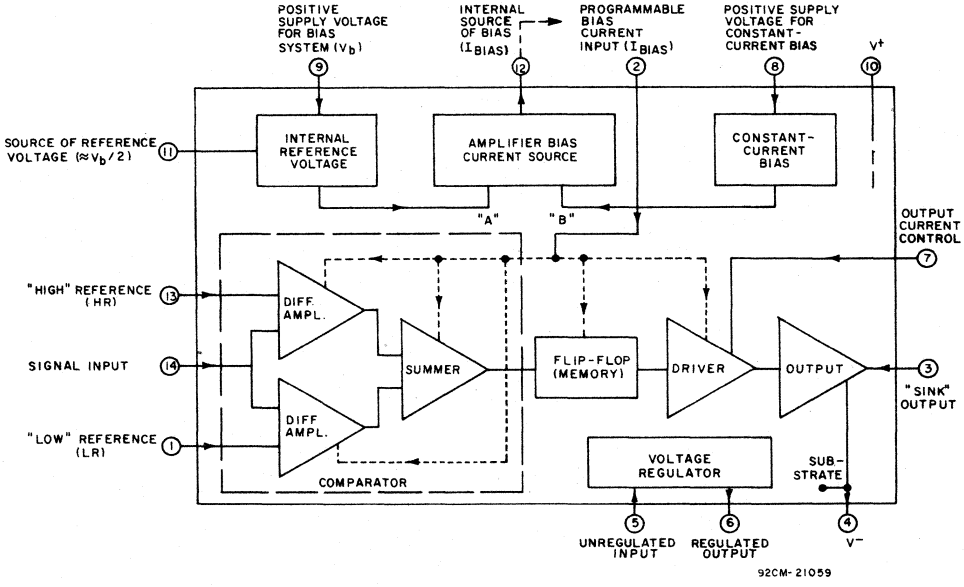


Fig. 1—Block diagram of CA3099E programmable comparator.
(See page 3 for general description of circuit operation.)

CA3099E

Major Circuit-Function Features (Cont'd)

2. **Flip-flop;** the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. **Driver and output stages;** these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. **Programmable operating current;** the circuit incorporates a separate terminal to permit programming the desired quiescent operating current and performance parameters.
5. **Internal sources of reference voltage and programmable bias current;** an integral circuit supplies a temperature-compensated reference voltage ($V_b/2$) which is about 1/2 of the externally applied bias voltage (V_b). Additionally, integral circuitry can optionally be used to supply an uncompensated constant-current source of bias (I_{bias}).
6. **Voltage regulator;** provides optional on-chip voltage regulation when power for the CA3099E is provided by an unregulated supply.

Maximum Ratings, *Absolute-Maximum Values at $T_A = 25^oC$:*

Supply Voltage Between Terminals 10 and 4, 9 and 4, 8 and 4	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4.	16	V
Differential Input Voltage Between Terminals 14 and 1, and Terminals 13 and 14	10	V
Operating Voltage Range:		
Term. 14	0 V to V^+	
Term. 13	2.0 V to V^+	
Term. 1	0 V to V^+ minus 2.0 V	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programming Bias Current (Term. 2)	1	mA
Output Current Control (Term. 7)	15	mA
Power Dissipation:		
Up to $T_A = 55^oC$	750	mW
Above $T_A = 55^oC$. Derate Linearly at	6.67	mW/^oC
Ambient Temperature Range:		
Operating	−55 to +125	^oC
Storage	−65 to +150	^oC
Lead Termperature (During Soldering): At distance not less than 1/32 inch (3.17 mm) from seating plane for 10 s maximum	+265	^oC

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$ *(Unless otherwise indicated)*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS $T_A = 25^oC$ Unless Otherwise Indicated	FIG. No.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Reference Voltage	V_{REF}	Term. 9 = 12 V, Term.4 = Grd, Term.11 = Test	–	5.7	6	6.3	V
Reference Voltage Temperature Coefficient			–	–	100	–	μV/^oC
Regulated Supply Voltage	V_{REG}	Term.5 1K to 12V, Term.4 = Grd, Term.6 10K to Grd	5	6	7.2	8	V
Regulated Supply Voltage Temperature Coefficient			5	–	2.9	–	mV/^oC
Input Offset Voltage: "Low" Reference	V_{IO} (LR)	V_{LR} = Grd, V_{HR} = 3 V, I_{BIAS} = 100 μA	20, 6	−8	−3	2	mV
"High" Reference	V_{IO} (HR)	V_{HR} = Grd, V_{LR} = −3 V, I_{BIAS} = 100 μA	20, 7	−5	±1	5	mV
"Low" Reference Temp. Coefficient		−55°C to +125°C	20, 8	–	4.5	20	μV/^oC
"High" Reference Temp. Coefficient		−55°C to +125°C	20, 9	–	±8.2	±20	μV/^oC
Min. Hysteresis Voltage	$V_{IO(HR-LR)}$	V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21, 10	–	3	10	mV
Min. Hysteresis Voltage Temperature Coefficient		−55°C to +125°C	11	–	6.7	20	μV/^oC
Output Saturation Voltage	$V_{CE(SAT)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,12,13	–	0.72	1.2	V
Total Supply Current: I_{TOTAL} "ON"	I_{TOTAL}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,14,15	600	710	800	μA
I_{TOTAL} "OFF"		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,14,15	420	560	750	μA
Input Bias Current: $I_{B(p-n-p)}$	I_{IB}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,16,17	–	33	200	nA
$I_{B(n-p-n)}$		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,16,17	–	20	60	nA
Output Leakage Current	$I_{CE(OFF)}$	Current from Term.3 when Q46 is "OFF"	–	–	–	10	μA
Internal Bias Current	I_{IBC}		18,19	120	200	280	μA
Switching Times:		I_C = 100 μA, I_{BIAS} = 100 μA, V^+ = 5 V, V_{REG} = 2.5 V					
Delay	t_d		22	–	600	–	ns
Fall	t_f		22	–	50	–	ns
Rise	t_r		22	–	500	–	ns
Storage	t_s		22	–	4.5	–	ns

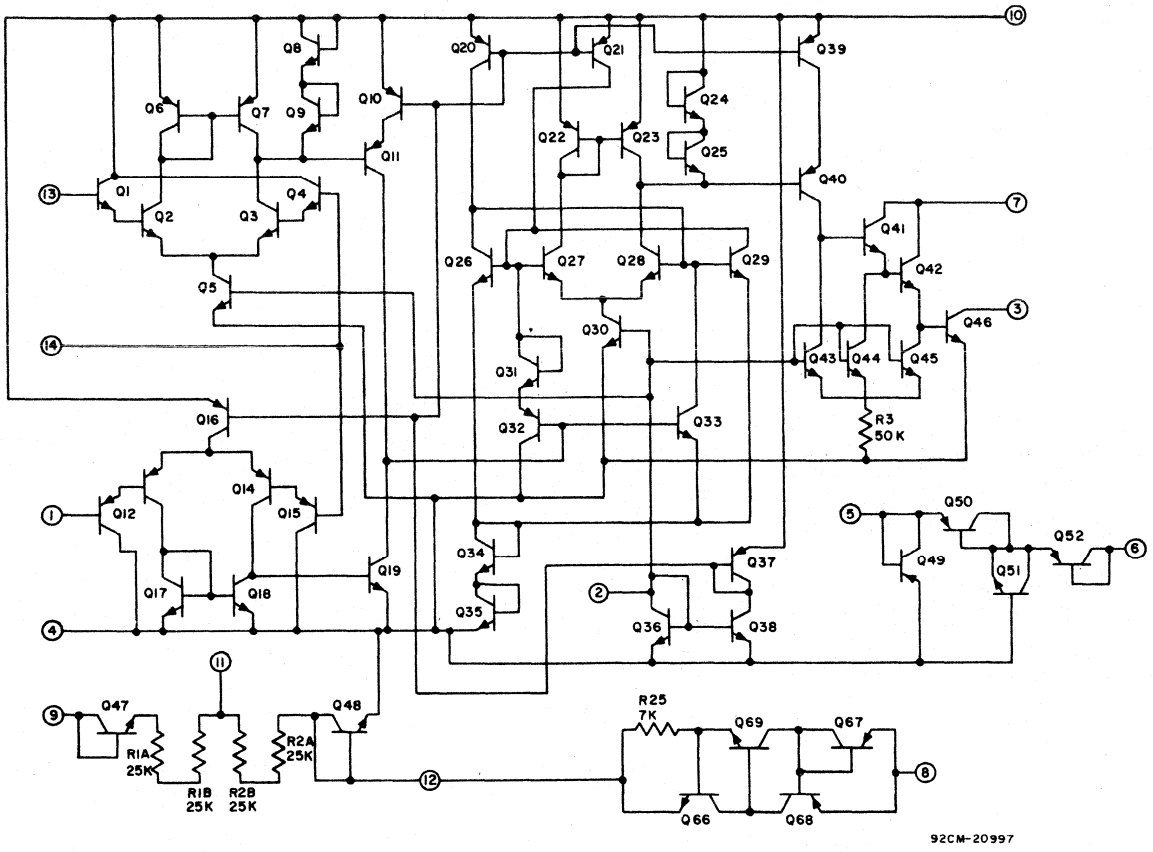


Fig.2–Schematic diagram of CA3099E.

General Description of Circuit Operation (Refer to Fig.1)

When the signal-input voltage of the CA3099E is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

The CA3099E comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{bias}) supplied to terminal 2. As an alternative to externally supplied bias current, the CA3099E contains an internal source of regulated bias current accessible at terminal 12. This internal source of bias current is developed by two alternative methods; in the first method, bias voltage (V_b) applied at terminal 9 develops a source of temperature-compensated reference voltage ($\approx V_b/2$) at terminal 11 and additionally supplies a source of bias current at terminal 12 via line "A". Alternately, when a positive supply voltage is applied at terminal 8, a source of constant-current biasing is provided at terminal 12 via line "B".

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 7. The CA3099E contains an on-chip voltage regulator which may optionally be used to regulate the voltages and bias currents (exclusive of the load current at terminal 3) needed for the operation of the IC.

Fig. 2 is the schematic diagram of the CA3099E. Figs. 3 and 4 are, respectively, functional and logic diagrams of CA3099E operation.

CA3099E

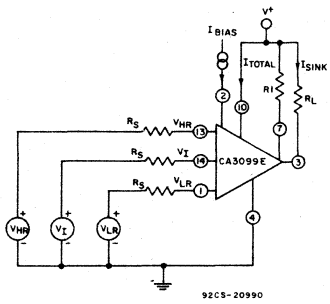


Fig.3—Functional diagram.

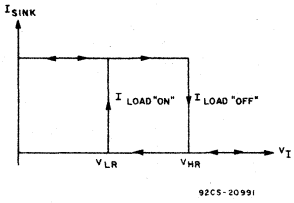


Fig.4—Logic diagram.

TYPICAL CHARACTERISTIC CURVES

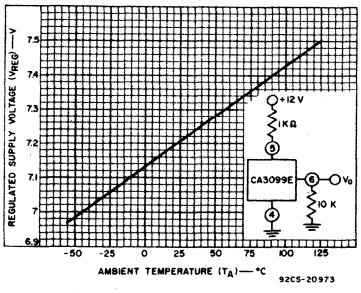


Fig.5—Regulated supply voltage vs. ambient temperature.

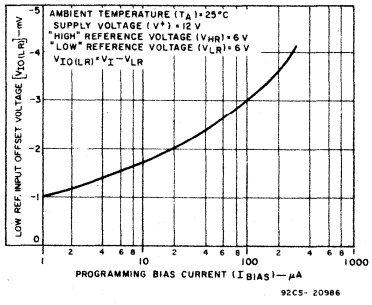


Fig.6—Input-offset voltage ("low" reference) vs. programming bias current.

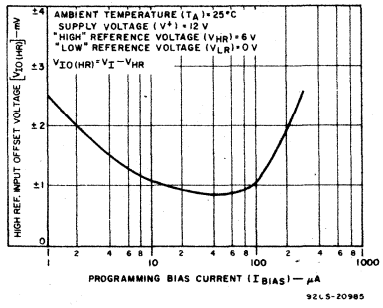


Fig.7—Input-offset voltage ("high" reference) vs. programming bias current.

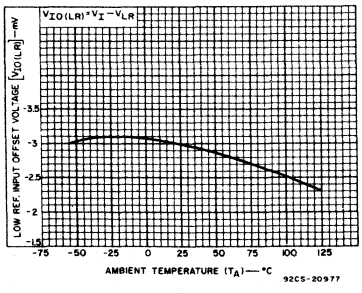


Fig.8—Input-offset voltage ("low" reference) vs. ambient temperature.

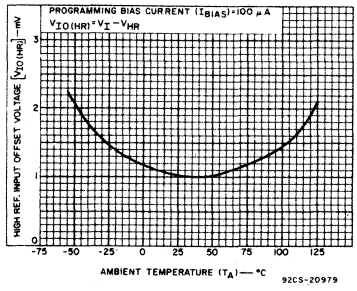


Fig.9—Input-offset voltage ("high" reference) vs. ambient temperature.

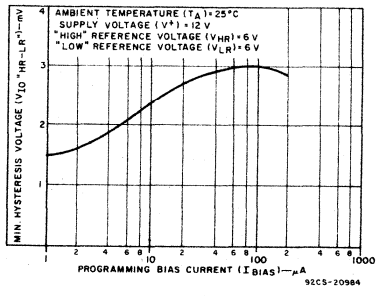


Fig.10—Min. hysteresis voltage vs. programming bias current.

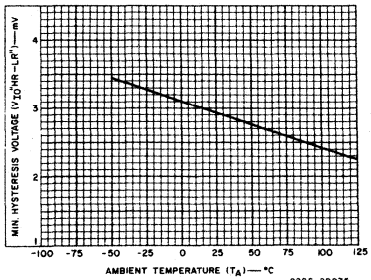


Fig.11—Min. hysteresis voltage vs. ambient temperature.

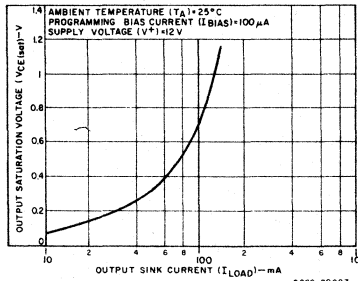


Fig.12—Output saturation voltage vs. output sink current.

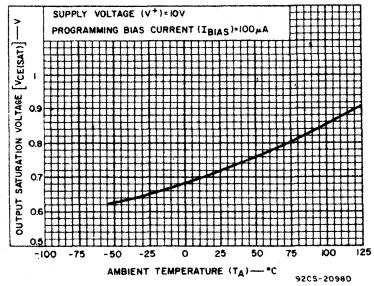


Fig.13—Output saturation voltage vs. ambient temperature.

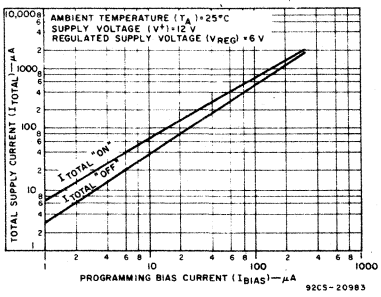


Fig.14—Total supply current vs. programming bias current.

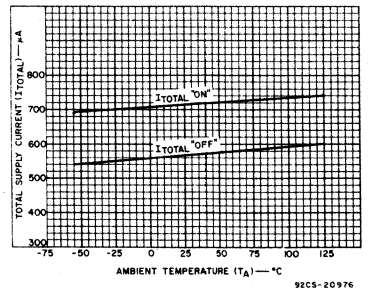


Fig.15—Total supply current vs. ambient temperature.

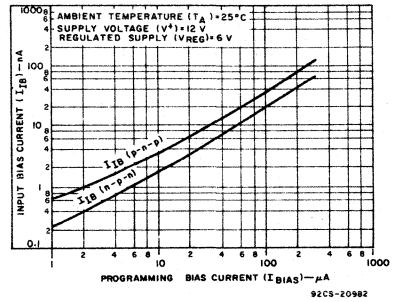


Fig.16—Input bias current vs. programming bias current.

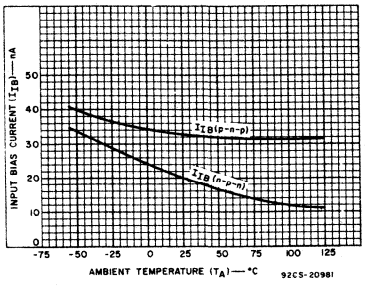


Fig.17—Input bias current vs. ambient temperature.

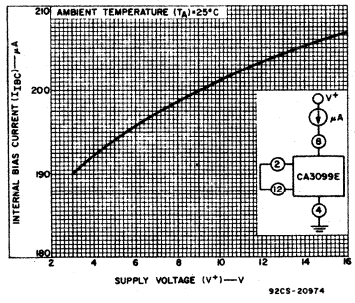


Fig.18—Internal bias current vs. supply voltage.

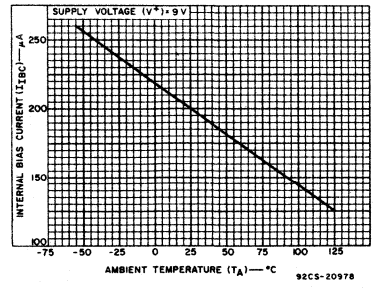


Fig.19—Internal bias current vs. ambient temperature.

TEST CIRCUITS

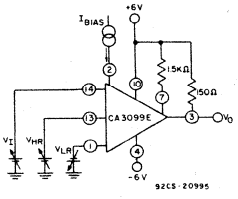


Fig.20—Input-offset voltage test circuit.

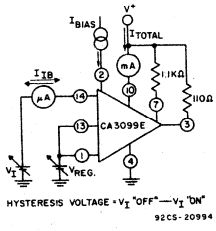


Fig.21—Min. hysteresis voltage, total supply current, and input-bias-current test circuit.

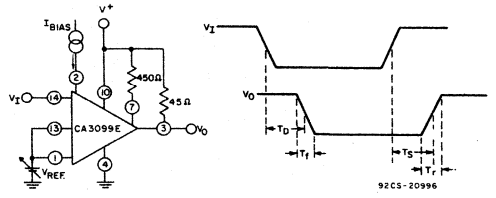


Fig.22—Switching time test circuit.

TYPICAL APPLICATIONS

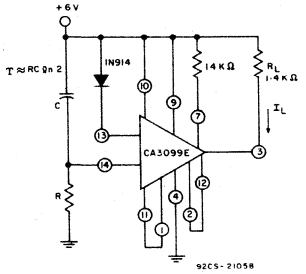


Fig.23(a)—Time delay circuit: Terminal 3 "sinks" after T seconds.

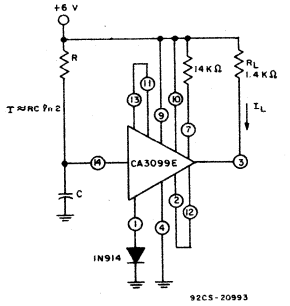


Fig.23(b)—Time delay circuit: "sink" current interrupted after T seconds.

CA3099E

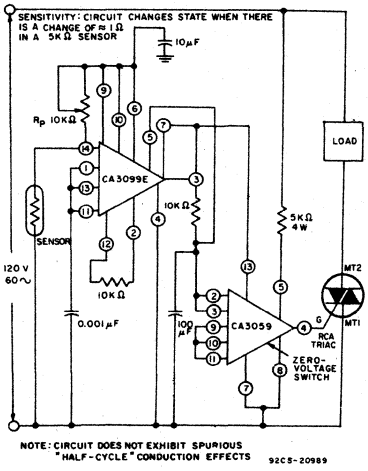


Fig.24—Sensitive temperature control.

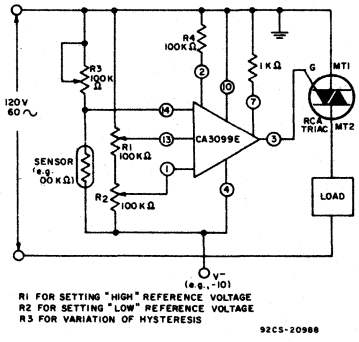


Fig.25—OFF/ON control of triac with programmable hysteresis.

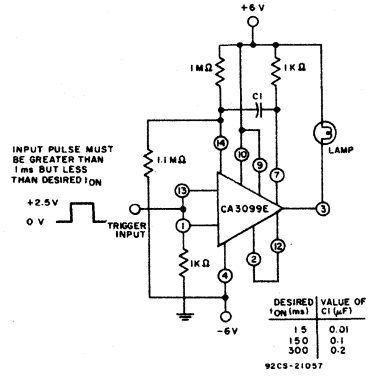


Fig.26—One-shot multivibrator.

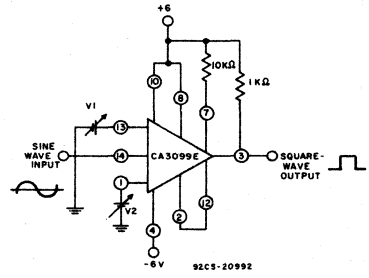
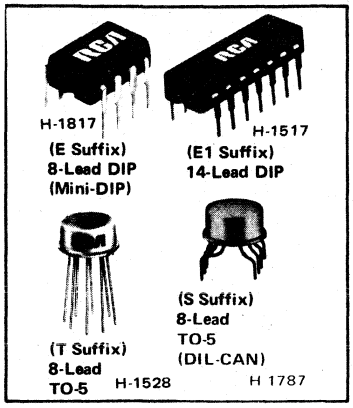


Fig.27—Sine-wave to square-wave converter with duty-cycle adjustment (V_1 and V_2).



BiMOS Dual Voltage Comparators

With MOS/FET Input, Bipolar Output

Features:

- *MOS/FET input stage:*
  - (a) *Very high input impedance (Z_{IN}) - 1.7 TΩ typ.*
  - (b) *Very low input current - 3.5 pA typ. at +5 V supply voltage*
  - (c) *Low input-offset voltage (V_{IO}) - to 6 mV max. (CA3290B)*
  - (d) *Wide common-mode input-voltage range (V_{ICR}) - can be swung 1.5 V (typ.) below negative supply-voltage rail*
  - (e) No phase reversal of output signal for input signals down to 5 V below negative supply-voltage rail
  - (f) *MOS/FET input stage - zener diode protected*
  - (g) *Virtually eliminates errors due to flow of input currents*
- *Wide supply-voltage range:*
  Single supply - 4 to 36 V dc
  Dual supply - $^{+3.5}_{-0.5}$ to ±18 V dc
  (B-types up to 44 or ±22 V dc)
- *Very low supply-current drain - 0.8 mA at +5 V*
- *Differential input-voltage range - up to ±36 V*
- *Low output saturation voltage - 120 mV at 4 mA*
- *Output voltage compatible with TTL, DTL, ECL, MOS, and CMOS logic systems*
- *All types are rated for operation over the range of −55 to +125° C*
- *Stable V_{IO} vs. time due to source-follower inputs*

Applications:

- *High-source-impedance voltage comparators*
- *Long time delay circuits*
- *Square-wave generators*
- *A/D converters*
- *Window comparators*

SELECTION CHART

Selection	Characteristic				Package & Suffix			
					TO-5		Plastic	
	Max. V_{IO} (mV)	Max. I_I (pA)	Min. A_{OL}	V^+ (V)	Std.	DIL-CAN	8-Ld.	14-Ld.
CA3290B	6	30	50K	44	T	S	—	—
CA3290A	10	40	25K	36	T	S	E	E1
CA3290	20	50	25K	36	T	S	E	E1

The CA3290 is also available in chip form (H suffix)

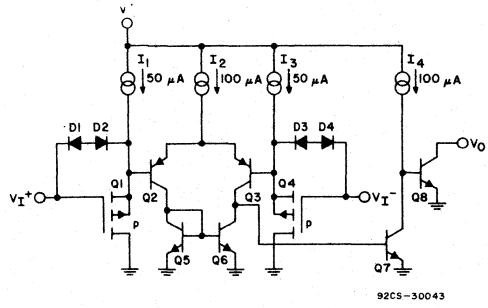


Fig. 1 – Basic CA3290 comparator.

CA3290, CA3290A, CA3290B

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
- Single Supply:
  - CA3290B . . . . . +44 V
  - CA3290A, CA3290 . . . . . +36 V
- Dual Supply:
  - CA3290B . . . . . ±22 V
  - CA3290A, CA3290 . . . . . ±18 V

DIFFERENTIAL INPUT VOLTAGE . . . . . ±36 V or ± [(V^+–V^-)+5 V] (whichever is less)

COMMON-MODE INPUT VOLTAGE . . . . . V^++5 V to V^-–5 V

DEVICE DISSIPATION:
- Up to 55°C . . . . . 630 mW
- Above 55°C . . . . . Derate linearly at 6.67 mW/°C

OUTPUT-TO-V^- SHORT CIRCUIT DURATION* . . . . . CONTINUOUS

TEMPERATURE RANGE, ALL TYPES:
- Operating . . . . . –55 to +125°C
- Storage . . . . . –65 to +150°C

INPUT TERMINAL CURRENT . . . . . 1 mA

LEAD TEMPERATURE (DURING SOLDERING):
- AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX. . . . . 265°C

*Short circuits from the output to V^+ can cause excessive heating and eventual destruction of the device.

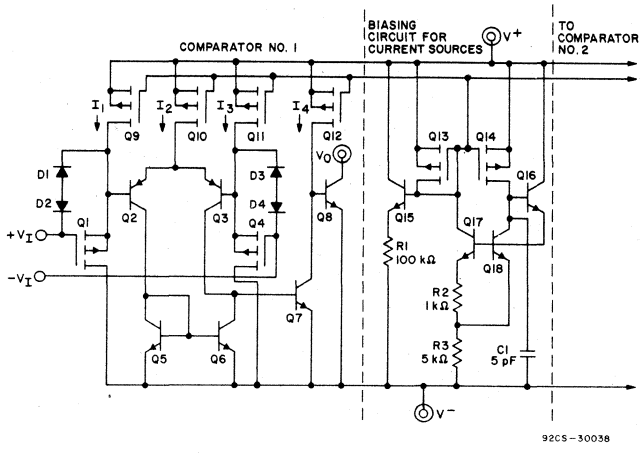


Fig. 2 – Schematic diagram of CA3290 (only one is shown).

CIRCUIT DESCRIPTION

The Basic Comparator

Fig. 1 shows the basic circuit diagram for one of the two comparators in the CA3290. It is generically similar to the industry-type "139" comparators, with PMOS transistors replacing p-n-p transistors as input stage elements. Transistors Q1 through Q4 comprise the differential input stage, with Q5 and Q6 serving as a mirror-connected active load and differential-to-single-ended converter. The differential input at Q1 and Q4 is amplified so as to toggle Q6 in accordance with the input-signal polarity. For example, if $+V_{IN}$ is greater than $-V_{IN}$, Q1, Q2, and current mirror transistors Q5 and Q6 will be turned off; transistors Q3, Q4, and Q7 will be turned on, causing Q8 to be turned off. The output is pulled positive when a load resistor is connected between the output and V^+.

In essence, Q1 and Q4 function as source-followers to drive Q2 and Q3, respectively, with zener diodes D1 through D4 providing gate-oxide protection against input voltage transients (e.g., static electricity). The current flow in Q1 and Q2 is established at approximately 50 microamperes by constant-current sources I_1 and I_3, respectively. Since Q1 and Q4 are operated with a constant current load, their gate-to-source voltage drops will be effectively constant as long as the input voltages are within the common-mode

range. As a result, the input offset voltage ($V_{GS(Q1)} + V_{BE(Q2)} - V_{BE(Q3)} - V_{GS(Q4)}$) will not be degraded when a large differential dc voltage is applied to the device for extended periods of time at high temperatures.

Additional voltage gain following the first stage is provided by transistors Q7 and Q8. The collector of Q8 is open, offering the user a wide variety of options in applications. An additional discrete transistor can be added if it becomes necessary to boost the output sink-current capability.

The detailed schematic diagram for one comparator and the common current-source biasing is shown in Fig. 2. PMOS transistors Q9 through Q12 are the current-source elements identified in Fig. 1 as I_1 through I_4, respectively. Their gate-source potentials (V_{GS}) are supplied by a common bus from the biasing circuit shown in the right-hand portion of the Fig. 2. The currents supplied by Q10 and Q12 are twice those supplied by Q9 and Q11. The transistor geometries are appropriately scaled to provide the requisite currents with common V_{GS} applied to Q9 through Q12.

ELECTRICAL CHARACTERISTICS at T_A = –55 to +125°C

CHARACTERISTIC	TEST CONDITIONS		VALUES						UNITS
			CA3290B		CA3290A		CA3290		
		V^+	Typ.	Max.	Typ.	Max.	Typ.	Max.	
Input Offset Voltage, V_{IO}	V_{CM}=1.4 V, V_O=1.4 V	5 V	3.5	–	4.5	–	8.5	–	mV
	V_{CM}=0 V, V_O=0 V	±15 V	3.5	–	8.5	–	8.5		
Temp. Coefficient of Input Offset Voltage, $\Delta V_{IO}/\Delta T$			8	–	8	–	8	–	µV/°C
Input Offset Current, I_{IO}	V_{CM}=1.4 V	5 V	2	22	2	28	2	32	nA
	V_{CM}=0 V	±15 V	7	22	7	28	7	32	
Input Current, I_I▲	V_{CM}=1.4 V	5 V	2.8	32	2.8	45	2.8	55	nA
	V_{CM}=0 V	±15 V	13	32	13	45	13	55	
Supply Current, I^+*	$R_L = \infty$	5 V	0.85	1.6	0.85	1	0.85	1.6	mA
		30 V	1.62	3.5	1.62	3	1.62	3.5	
Voltage Gain, A_{OL}	R_L=15 kΩ	±15 V	150	–	150	–	150	–	V/mV
			103	–	103	–	103	–	dB
Saturation Voltage I_{SINK} = 4 mA	V^+=5 V, $+V_I$=0 V, $-V_I$=1 V	+125°C	0.22	0.7	0.22	0.7	0.22	0.7	V
		–55°C	0.1	–	0.1	–	0.1	–	
Output Leakage Current, I_{OL}		15 V	65	–	65	–	65	–	nA
		36 V	130	1k	130	1k	130	1k	

▲At T_A = +125°C
*At T_A = –55°C

CA3290, CA3290A, CA3290B

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

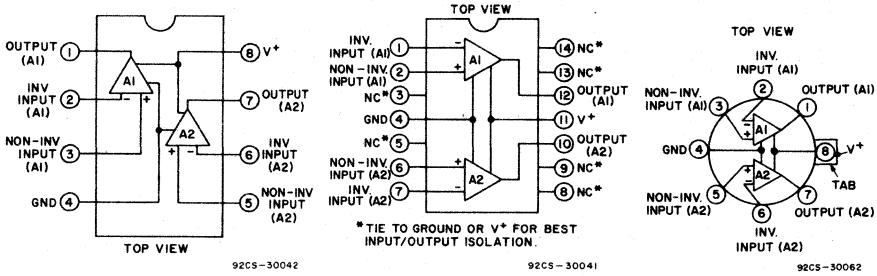
CHARACTERISTIC	TEST COND. V^+	LIMITS						UNITS
		CA3290B			CA3290A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, V_{IO} V_{CM}=1.4 V, V_O=1.4 V	5 V	–	3	6	–	4	10	mV
V_{CM}=0 V, V_O=0 V	±15 V	–	3	6	–	4	10	mV
Input Current, I_I V_{CM}=1.4 V	5 V	–	3.5	30	–	3.5	40	pA
V_{CM}=0 V	±15 V	–	12	30	–	12	40	pA
Input Offset Current, I_{IO} V_{CM}=1.4 V	5 V	–	2	20	–	2	25	pA
V_{CM}=0 V	±15 V	–	7	20	–	7	25	pA
Common-Mode Input-Voltage Range, V_{ICR} V_O=1.4 V	5 V	V^+–3.5 to V^-	V^+–3.1 to V^-–1.5	–	V^+–3.5 to V^-	V^+–3.1 to V^-–1.5	–	V
V_O=0 V	±15 V	V^+–3.8 to V^-	V^+–3.4 to V^-–1.6	–	V^+–3.8 to V^-	V^+–3.4 to V^-–1.6	–	V
Supply Current, I^+ R_L = ∞	30 V	–	1.35	3	–	1.35	3	mA
	5 V	–	0.8	1.4	–	0.8	1.4	mA
Voltage Gain, A_{OL} R_L=15 kΩ	±15 V	50	800	–	25	800	–	V/mV
		94	118	–	88	118	–	dB
Output Sink Current V_O=1.4 V	5 V	6	30	–	6	30	–	mA
Saturation Voltage $+V_I$=0 V, $-V_I$=1 V, I_{SINK} = 4 mA	5 V	–	0.12	0.4	–	0.12	0.4	V
Output Leakage Current, I_{OL}	15 V	–	100	–	–	100	–	pA
	36 V	–	500	–	–	500	–	pA
Response Time R_L=5.1 kΩ Rising Edge	15 V	–	1.2	–	–	1.2	–	μs
Falling Edge		–	200	–	–	200	–	ns
Common-Mode Rejection Ratio, CMRR	±15 V	–	44	316	–	44	562	μV/V
	5 V	–	100	316	–	100	562	μV/V
Power-Supply Rejection Ratio, PSRR	±15 V	–	15	316	–	15	316	μV/V
Large-Signal Response Time R_L=5.1 kΩ	15 V	–	500	–	–	500	–	ns
	5 V	–	400	–	–	400	–	ns

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$

CHARACTERISTIC	TEST COND. V^+	LIMITS CA3290 Min.	LIMITS CA3290 Typ.	LIMITS CA3290 Max.	UNITS
Input Offset Voltage, V_{IO} V_{CM}=1.4 V, V_O=1.4 V	5 V	–	7.5	20	mV
V_{CM}=0 V, V_O=0 V	±15 V	–	7.5	20	mV
Input Current, I_I V_{CM}=1.4 V	5 V	–	3.5	50	pA
V_{CM}=0 V	±15 V	–	12	50	pA
Input Offset Current, I_{IO} V_{CM}=1.4 V	5 V	–	2	30	pA
V_{CM}=0 V	±15 V	–	7	30	pA
Common-Mode Input-Voltage Range, V_{ICR} V_O=1.4 V	5 V	V^+–3.5 V^-	V^+–3.1 V^-–1.5	–	V
V_O=0 V	±15 V	V^+–3.8 V^-	V^+–3.4 V^-–1.6	–	V
Supply Current, I^+ $R_L = \infty$	30 V	–	1.35	3	mA
	5 V	–	0.8	1.4	mA
Voltage Gain, A_{OL} R_L = 15 kΩ	±15 V	25	800	–	V/mV
		88	118	–	dB
Output Sink Current V_O=1.4 V	5 V	6	30	–	mA
Saturation Voltage $+V_I$=0 V, $-V_I$=1 V, I_{SINK} = 4 mA	5 V	–	0.12	0.4	V
Output Leakage Current, I_{OL}	15 V	–	100	–	pA
	36 V	–	500	–	pA
Response Time R_L=5.1 kΩ Rising Edge	15 V	–	1.2	–	μs
Falling Edge		–	200	–	ns
Common-Mode Rejection Ratio, CMRR	±15 V	–	44	562	μV/V
	5 V	–	100	562	μV/V
Power-Supply Rejection Ratio, PSRR	±15 V	–	15	316	μV/V
Large-Signal Response Time R_L=5.1 kΩ	15 V	–	500	–	ns
	5 V	–	400	–	ns

CA3290, CA3290A, CA3290B

TERMINAL ASSIGNMENTS



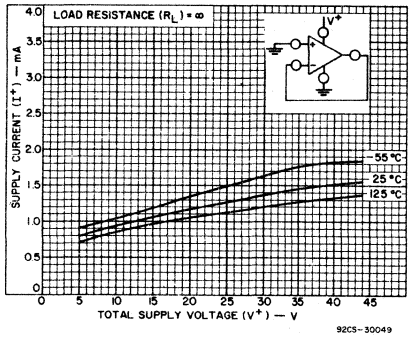


Fig. 3 — Supply current as a function of supply voltage (both amplifiers).

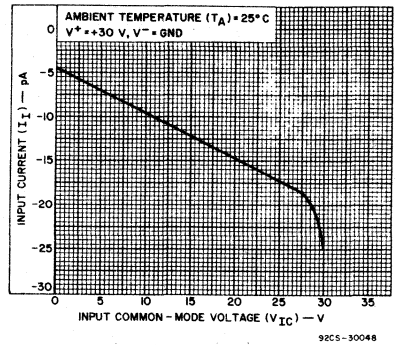


Fig. 4 — Input current as a function of input common-mode voltage.

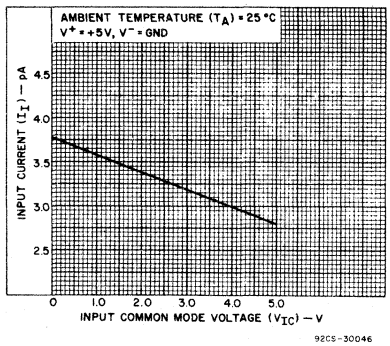


Fig. 5 — Input current as a function of input common-mode voltage.

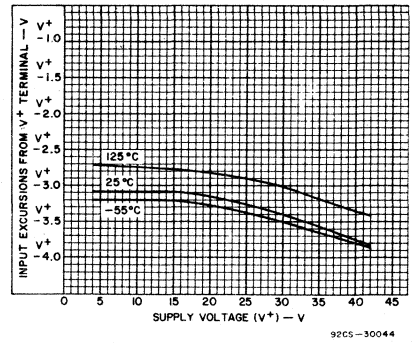


Fig. 6 — Positive common-mode input voltage range as a function of supply voltage.

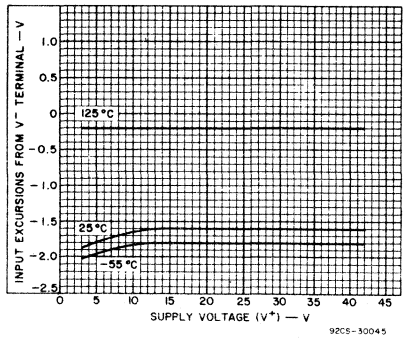


Fig. 7 — Negative common-mode input voltage range as a function of supply voltage.

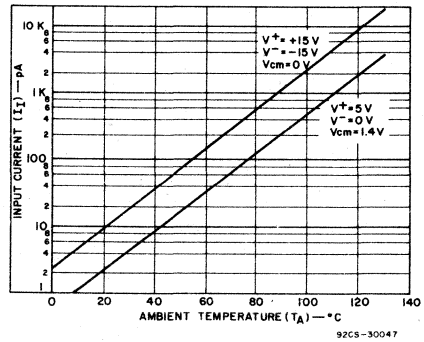


Fig. 8 — Input current as a function of ambient temperature.

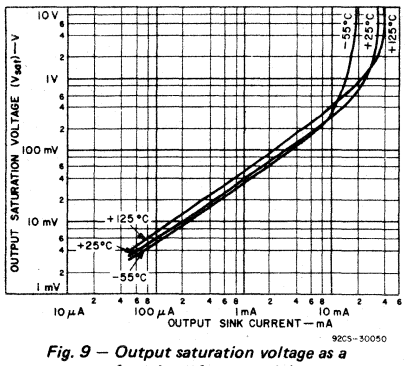


Fig. 9 – Output saturation voltage as a function of output sink current.

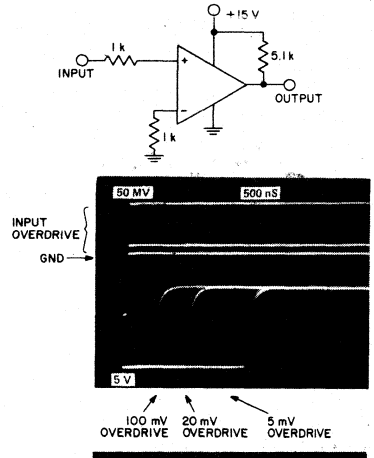
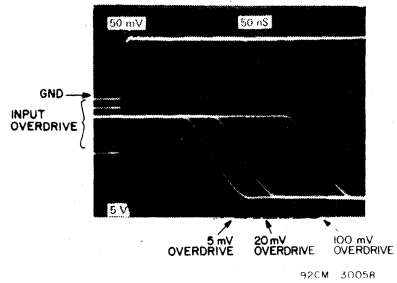
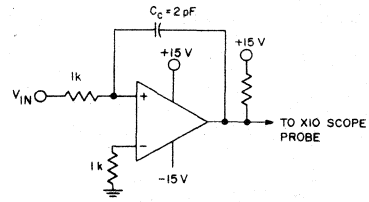
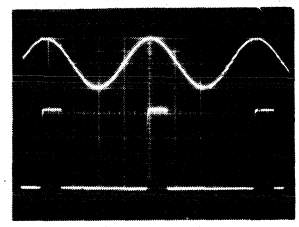


Fig. 11 – Non-inverting comparator response-time test circuit and waveforms.

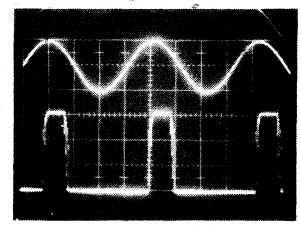






WITH C_C

TOP TRACE ≈ 4.5 mV/DIV = V_{IN}
BOTTOM TRACE = 10 V/DIV = V_{OUT}
H = 5 μs/DIV

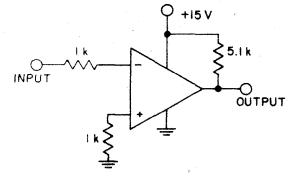


WITHOUT C_C

TOP TRACE ≈ 4.5 mV/DIV
BOTTOM TRACE = 10 V/DIV
H = 5 μs/DIV

92CM-30059R1

Fig. 10 – Parasitic-oscillations test circuit and associated waveforms.



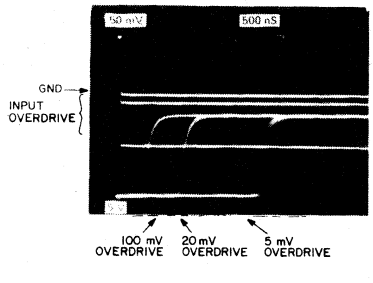


Fig. 12 – Inverting comparator response-time test circuit and waveforms.

OPERATING CONSIDERATIONS

Input Circuit

The use of MOS transistors in the input stage of the CA3290 series circuits provides the user with the following features for comparator applications:

1. Ultra-high input impedance ($\cong 1.7\ T\Omega$);
2. The availability of common-mode rejection for input signals at potentials below that of the negative power-supply rail;
3. Retention of the in-phase relationship of the input and output signals for input signals below the negative rail.

Although the CA3290 employs rugged bipolar (zener) diodes for protection of the input circuit, the input-terminal currents should not exceed 1 mA. Appropriate series-connected limiting resistors should be used in circuits where greater current flows might exist, allowing the signal input voltage to be greater than the supply voltage without damaging the circuit.

Output Circuit

The output of the CA3290 is the open collector of an n-p-n transistor, a feature providing flexibility in a broad range of comparator applications. An output ORing function can be implemented by parallel-connection of the open collectors. An output pull-up resistor can be connected to a power supply having a voltage range within the rating of the particular CA3290 in use; the magnitude of this voltage may be set at a value which is independent of that applied to the V^+ terminal of the CA3290.

Parasitic Oscillations

The ideal comparator has, among other features, ultra-high input impedance, high gain, and wide bandwidth. These desirable characteristics may, however, produce parasitic oscillations unless certain precautions are observed to minimize the stray capacitive coupling between the input and output terminals. Parasitic oscillations manifest themselves during the output voltage transition intervals as the comparator switches states. For high source impedances, stray capacitance can induce parasitic oscillations. The addition of a small amount (1 to 10 mV) of positive feedback (hysteresis) produces a faster transition, thereby reducing the likelihood of parasitic oscillations. Furthermore, if the input signal is a pulse waveform, with relatively rapid rise and fall times, parasitic tendencies are reduced.

When dual comparators, like the CA3290, are packaged in an 8-lead configuration, the output terminal of each comparator is adjacent to an input terminal. The lead-to-lead capacitance is approximately 1 pF, which may be sufficient to cause undesirable feedback effects in certain applications. Circuit factors such as impedance levels, supply voltage, toggling rate, etc., may increase the possibility of parasitic oscillations. To minimize this potential oscillatory condition, it is recommended that for source impedances greater than 1 $k\Omega$ a capacitor ($\geqslant$ 1-2 pF) be connected between the appropriate input terminal and the output terminal. (See Fig. 10.)

The CA3290A and CA3290 are also supplied in a 14-lead dual-in-line plastic package. To minimize the possibility of parasitic oscillations the input and output terminals are positioned on opposite sides of the package. In addition, there are two leads between the output terminal of each comparator and its corresponding inverting input terminal, reducing the input/output coupling significantly. These leads (8, 9, 13, 14) should be tied to either the V^+ or V^- supply rail. If either comparator is unused, its input terminals should also be tied to either the V^+ or V^- supply rail.

TYPICAL APPLICATIONS

Light-Controlled One-Shot Timer

In Fig. 13 one comparator (A1) of the CA3290 is used to sense a change in photo diode current. The other comparator (A2) is configured as a one-shot timer and is triggered by the output of A1. The output of the circuit will switch to a low state for approximately 60 seconds after the light source to the photo diode has been interrupted. The circuit operates at normal room lighting levels. The sensitivity of the circuit may be adjusted by changing the values of R1 and R2. The ratio of R1 to R2 should be constant to insure constant reverse voltage bias on the photo diode.

Low-Frequency Multivibrator

In this application, one-half of the CA3290 is used as a conventional multivibrator circuit. Because of the extremely high input impedance of this device, large values of timing resistor (R1) may be used for long time delays with relatively small leakage timing capacitors. The second half of the CA3290 is used as an output buffer to insure that the multivibrator frequency will not be affected by output loading.

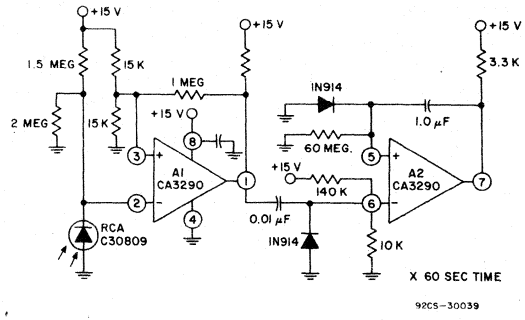


Fig. 13 – Light-controlled one-shot timer.

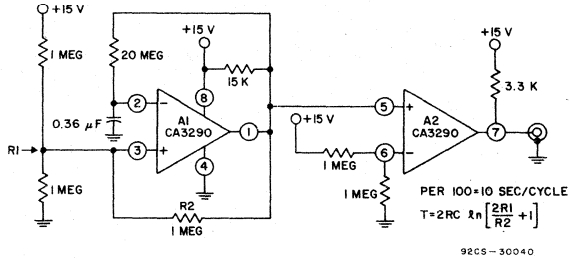


Fig. 14 – Low-frequency multivibrator.

Window Comparator

Both halves of the CA3290 can be used in a high input-impedance window comparator as shown in Fig. 15. The LED will be turned "on" whenever the input signal is above the lower limit (V_L) but below the upper limit (V_U), as determined by the R1/R2/R3 resistor divider.

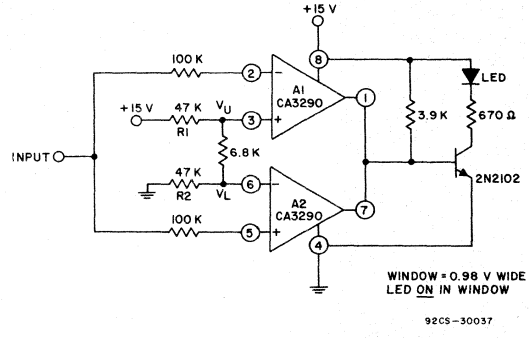


Fig. 15 – Window comparator.

CA3290, CA3290A, CA3290B

LED Bar Graph Driver

The circuit in Fig. 16 demonstrates the use of the CA3290 in a bar graph display. The non-inverting inputs of both comparators are tied to the voltage divider reference and the input signal is applied to both of the inverting inputs. The LED for a particular comparator will be turned "on" when the input voltage reaches the voltage on the resistor divider reference. The CA3290 is ideal for this application where input-signal loading is critical even though many comparator inputs are driven in parallel.

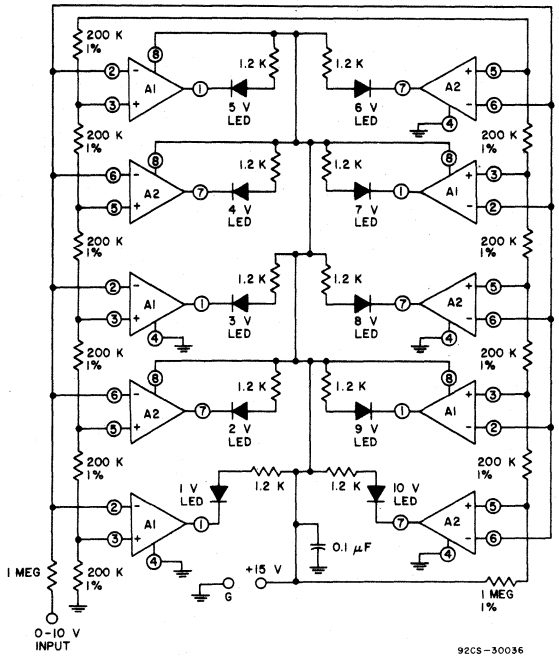
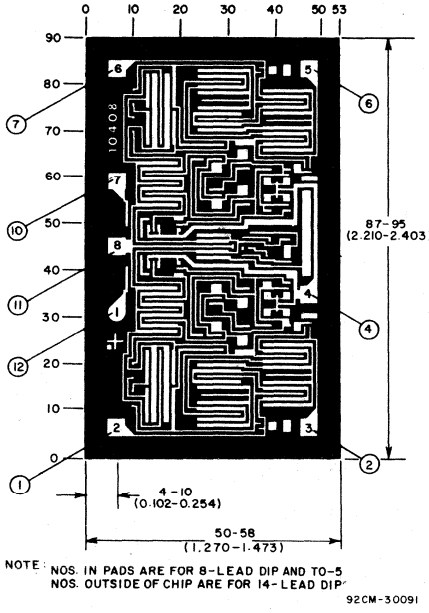


Fig. 16 – LED bar-graph driver.

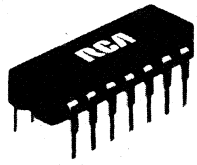


Dimensions and pad layout for the CA3290H.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA139, CA239, CA339 Types



14-Lead Dual-In-Line
"E" Suffix — Standard
Plastic Package

H-1517

Quad Voltage Comparators

For Industrial, Commerical, and Military Applications

"E" Suffix Types — Standard Dual-In-Line Plastic Package

Features:

- *Operation from single or dual supplies*
- *Common-mode input-voltage range to ground*
- *Output voltage compatible with TTL, DTL, ECL, MOS and CMOS*
- *Differential input-voltage range equal to the supply voltage*
- *Maximum input-offset voltage (V_{IO}):*
  CA139A, CA239A, CA339A - 2 mV
  CA139, CA239, CA339 - 5 mV
- *Replacement for industry types 139, 239, 339, 139A, 239A, and 339A*

The RCA-CA139, CA239, CA339, CA139A, CA239A, and CA339A types consist of four independent single- or dual-supply voltage comparators on a single monolithic substrate. The common-mode input voltage range includes ground even when operated from a single supply, and the low power supply current drain makes these comparators suitable for battery operation. These types were designed to directly interface with TTL and CMOS.

Types CA139A, CA239A, and CA339A have all the features and characteristics of their prototype counter parts CA139, CA239, and CA339 plus an even lower input-offset-voltage characteristic. These devices are supplied in a 14-lead dual-in-line plastic package (E suffix). The CA339 is also available in chip form (H suffix).

Applications:

- *Square-wave generators*
- *Time-delay generators*
- *Pulse generators*
- *Multivibrators*
- *High-voltage digital logic gates*
- *A/D converters*
- *MOS clock timers*

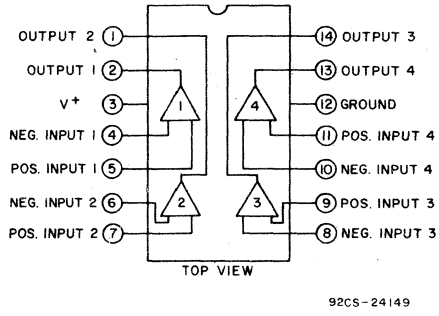


Fig. 1 - Functional diagram.

CA139, CA239, CA339 Types

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^oC$*:*

DC SUPPLY VOLTAGE	36 V or ±18 V
DC DIFFERENTIAL INPUT VOLTAGE	±36 V
INPUT VOLTAGE	−0.3 V to +36 V
INPUT CURRENT ($V_I < -0.3$ V)*	50 mA
OUTPUT SHORT CIRCUIT TO GROUND▲	
(Single Supply)	Continuous
DEVICE DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

* Inputs must not go more negative than −0.3 V.

▲Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current independent of V^+ is approximately 20 mA.

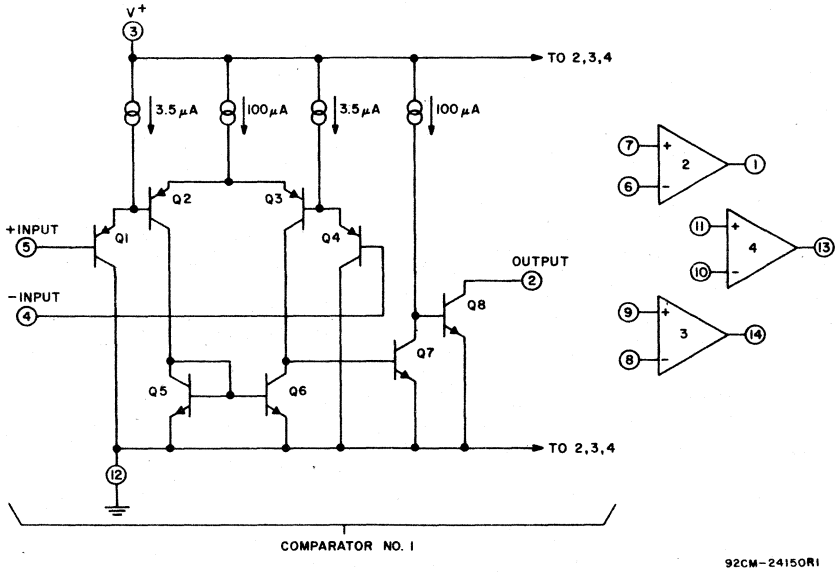


Fig. 2—Schematic diagram.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS ($V^+ = 5$ V Unless otherwise indicated)		LIMITS						UNITS
			CA139			CA139A			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage (V_{IO}) At Output Switch Point $V \cong 1.4$ V	V_{REF} = 1.4 V, $R_S = 0$	25°C	–	2	5	–	1	2	mV
		Note 1	–	–	9	–	–	4	
Differential Input Voltage (V_{ID})	Keep all inputs ≥0 V for V^- (If used), Notes 1, 2		–	–	36	–	–	36	V
Saturation Voltage (V_{sat})	$V_I^- = 1$ V, $V_I^+ = 0$ V, $I_{SINK} \leq$ 4 mA	25°C	–	250	400	–	250	400	mV
		Note 1	–	–	700	–	–	700	
Common-Mode Input Voltage Range (V_{ICR})	Note 3	25°C	0	–	$V^+-1.5$	0	–	$V^+-1.5$	V
		Note 1	0	–	V^+-2	0	–	V^+-2	
Input Offset Current (I_{IO})	$I_I^+ - I_I^-$	25°C	–	3	25	–	3	25	nA
		Note 1	–	–	100	–	–	100	
Input Bias Current (I_{IB})	I_I^+ or I_I^- with Output in Linear Range	25°C	–	25	100	–	25	100	nA
		Note 1	–	–	300	–	–	300	
Supply Current (I^+)	$R_L = \infty$ on all comparators, T_A = 25°C		–	0.8	2	–	0.8	2	mA
Output Leakage Current	$V_I^+ \geq 1$ V, $V_I^- = 0$, $V_O = 5$ V	25°C	–	0.1	–	–	0.1	–	nA
	$V_I^+ \geq 1$ V, $V_I^- = 0$, $V_O = 30$ V	Note 1	–	–	1	–	–	1	μA
Output Sink Current	$V_I^- \geq 1$ V, $V_I^+ = 0$, $V_O \leq +1.5$ V, T_A = 25°C		6	16	–	6	16	–	mA
Voltage Gain (A_{OL})	$R_L \geq 15$ kΩ, $V^+ = 15$ V, T_A = 25°C		–	200	–	50	200	–	V/mV
Large Signal Response Time	V_I = TTL Logic Swing, V_{REF} = +1.4 V, $V_{RL} = 50$ V, $R_L = 5.1$ kΩ, T_A = 25°C		–	300	–	–	300	–	ns
Response Time See Figs. 5 & 6	$V_{RL} = 5$ V, $R_L = 5.1$ kΩ, T_A = 25°C		–	1.3	–	–	1.3	–	μs

Note 1: Ambient Temperature (T_A) applicable over operating temperature range as shown below.

CA139 / CA139A (–55 to +125°C) | CA239 / CA239A (–25 to +85°C) | CA339 / CA339A (0 to +70°C)

Note 2: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than –0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

Note 3: The upper end of the common-mode voltage range is (V^+) – 1.5 V, but either or both inputs can go to +30 V without damage.

CA139, CA239, CA339 Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS (V^+ = 5 V, Unless otherwise indicated)		CA239, CA339 Min.	CA239, CA339 Typ.	CA239, CA339 Max.	CA239A, CA339A Min.	CA239A, CA339A Typ.	CA239A, CA339A Max.	UNITS
Input Offset Voltage (V_{IO}) At Output Switch Point V ≅ 1.4 V	V_{REF} = 1.4 V, R_S = 0	25°C	–	2	5	–	1	2	mV
		Note 1	–	–	9	–	–	4	
Differential Input Voltage (V_{ID})	Keep all inputs ≥0 V for V^- (If used), Notes 1, 2		–	–	36	–	–	36	V
Saturation Voltage (V_{sat})	V_I^- = 1 V, V_I^+ = 0 V, I_{SINK} ≤ 4 mA	25°C	–	250	400	–	250	400	mV
		Note 1	–	–	700	–	–	700	
Common-Mode Input Voltage Range (V_{ICR})	Note 3	25°C	0	–	V^+–1.5	0	–	V^+–1.5	V
		Note 1	0	–	V^+–2	0	–	V^+–2	
Input Offset Current (I_{IO})	$I_I^+ - I_I^-$	25°C	–	5	50	–	5	50	nA
		Note 1	–	–	150	–	–	150	
Input Bias Current (I_{IB})	I_I^+ or I_I^- with Output in Linear Range	25°C	–	25	250	–	25	250	nA
		Note 1	–	–	400	–	–	400	
Supply Current (I^+)	R_L = ∞ on all comparators, T_A = 25°C		–	0.8	2	–	0.8	2	mA
Output Leakage Current	V_I^+ ≥1 V, V_I^- = 0, V_O = 5 V	25°C	–	0.1	–	–	0.1	–	nA
	V_I^+ ≥1 V, V_I^- = 0, V_O = 30 V	Note 1	–	–	1	–	–	1	μA
Output Sink Current	V_I^- ≥1 V, V_I^+ = 0, V_O ≤+1.5 V, T_A = 25°C		6	16	–	6	16	–	mA
Voltage Gain (A_{OL})	R_L ≥15 kΩ, V^+=15 V, T_A = 25°C		–	200	–	50	200	–	V/mV
Large Signal Response Time	V_I = TTL Logic Swing, V_{REF} = +1.4 V, V_{RL} = 50 V, R_L = 5.1 kΩ, T_A = 25°C		–	300	–	–	300	–	ns
Response Time See Figs. 5 & 6	V_{RL} = 5 V, R_L = 5.1 kΩ, T_A = 25°C		–	1.3	–	–	1.3	–	μs

Note 1: Ambient Temperature (T_A) applicable over operating temperature range as shown below.
CA139, CA139A (–55 to +125°C) CA239, CA239A (–25 to +85°C) CA339, CA339A (0 to +70°C)

Note 2: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than –0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

Note 3: The upper end of the common-mode voltage range is (V^+) – 1.5 V, but either or both inputs can go to +30 V without damage.

TYPICAL CHARACTERISTICS

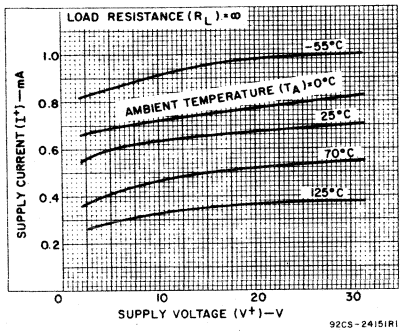


Fig. 3—Supply current vs. supply voltage.

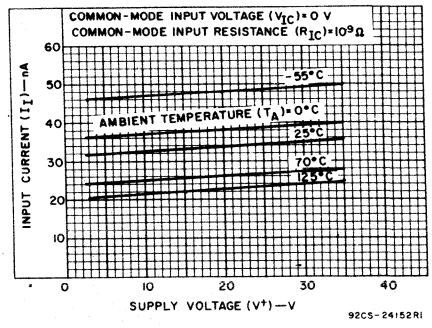


Fig. 4—Input current vs. supply voltage.

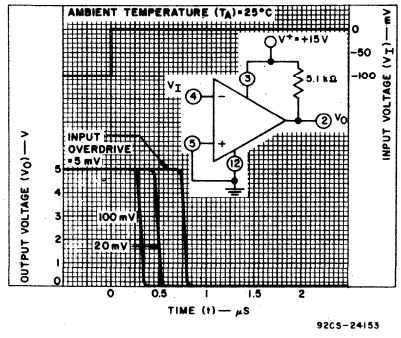


Fig. 5—Response time for various input overdrives—negative transition.

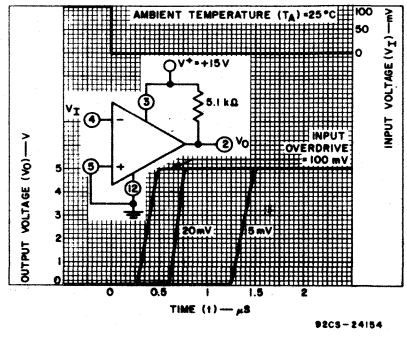


Fig. 6—Response time for various input overdrives—positive transition.

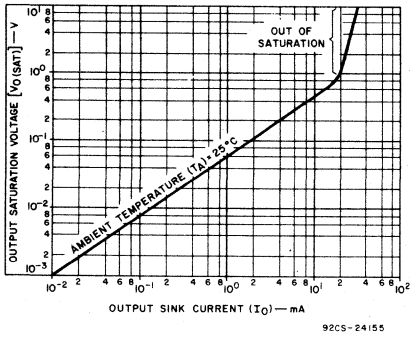
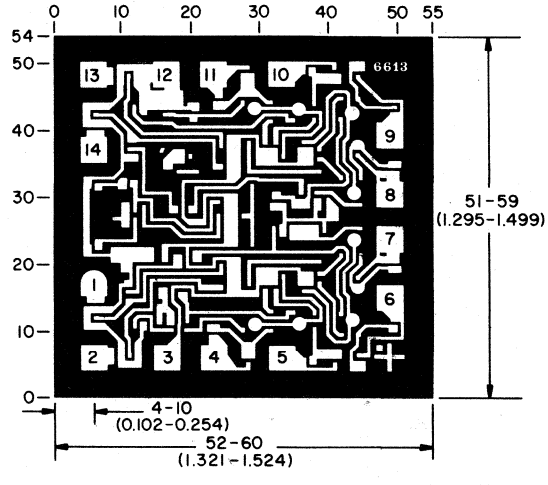


Fig. 7—Output saturation voltage vs. output sink current.

Chip Version (CA339H)



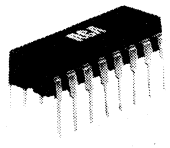
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Data Conversion Circuits
Technical Data

4

*BiMOS types

CA3162E



16-Lead Dual-In-Line Plastic Package

H-1622

A/D Converter for 3-Digit Display

Features:

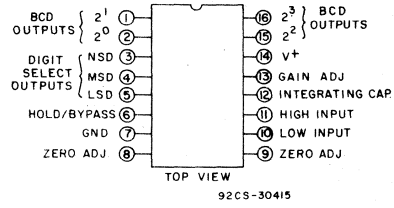
- *Dual-slope A/D conversion*
- *Multiplexed BCD display*
- *Ultra-stable internal band-gap voltage reference*
- *Capable of reading 99 mV below ground with single supply*
- *Differential input*
- *Internal timing - no external clock required*
- *Choice of low-speed [4-Hz] or high-speed [96-Hz] conversion rate*
- *"Hold" inhibits conversion but maintains delay*
- *Overrange indication - "EEE" for reading greater than + 999 mV, "-" for reading more negative than -99 mV when used with CA3161E BCD-to-Seven Segment Decoder/Driver*

The CA3162E is an I^2L monolithic A/D converter that provides a 3-digit multiplexed BCD output. It is used with the CA3161E BCD-to-Seven-Segment Decoder/Driver* and a minimum of external parts to implement a complete 3-digit display.

The CA3162 is supplied in 16-lead dual-in-line plastic package (E suffix). The CA3162 is also available in chip form (H suffix).

*The CA3161E is described in RCA data bulletin File No. 1079.

TERMINAL ASSIGNMENT
CA3162E



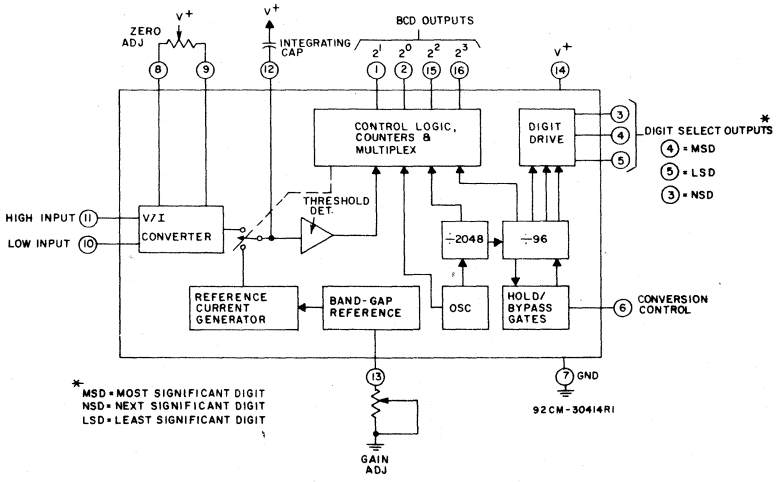


Fig. 1 — Functional block diagram of the CA3162E.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (between terminals 7 and 14) ..... +7 V
INPUT VOLTAGE (terminal 10 or 11 to ground) ..... ±15 V
DEVICE DISSIPATION:
Up to T_A = +55°C ..... 750 mW
Above T_A = +55°C ..... derate linearly at 7.9 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating ..... 0 to +75°C
Storage ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 5 V, Zero pot centered, gain pot = 2.4 kΩ unless otherwise stated

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Operating Supply Voltage Range, V^+		4.5	5	5.5	V
Supply Current, I^+	100 kΩ to V^+ on terms. 3,4,5	—	—	17	mA
Input Impedance, Z_I		—	100	—	MΩ
Input Bias Current, I_{IB}	Terms. 10 and 11	—	−80	—	nA
Unadjusted Zero Offset	$V_{11} - V_{10}$ = 0 V, read decoded output	−12	—	+12	mV
Unadjusted Gain	$V_{11} - V_{10}$ = 900 mV, read decoded output	846	—	954	mV
Linearity	See Notes 1 and 2	−1	—	+1	Count
Conversion Rate: Slow Mode	Term. 6 = open or gnd	—	4	—	Hz
Fast Mode	Term. 6 = 5 V	—	96	—	Hz
Conversion Control Voltage (Hold Mode) at Terminal 6		0.8	1.2	1.6	V
Common-Mode Input Voltage Range, V_{ICR}	See Note 3, 4	−0.2	—	+0.2	V
BCD Sink Current at terms. 1,2,15,16	$V_{BCD} \geq$ 0.5 V, at logic zero state	0.4	1.6	—	mA
Digit Select Sink Current at terms. 3,4,5	$V_{Digit\ Select}$ = 4 V at logic zero state	1.6	2.5	—	mA
Zero Temperature Coefficient	V_I = 0 V, zero pot centered	—	10	—	μV/°V
Gain Temperature Coefficient	V_I = 900 mV, gain pot = 2.4 kΩ	—	0.005	—	%/°C

Notes:

1. Apply zero volts across V_{11} to V_{10}. Adjust zero potentiometer to give 000 mV reading. Apply 900 mV to input and adjust gain potentiometer to give 900 mV reading.
2. Linearity is measured as a difference from a straight line drawn through zero and positive full scale. Limits do not include ±0.5 count bit digitizing error.
3. For applications where negative terminal 10 is not operated at terminal 7 potential, a return path of not more than 100 kΩ resistance must be provided for input bias currents.
4. The common-mode input voltage above ground cannot exceed +0.2 V if the full input signal range of 999 mV is required at terminal 11. That is, terminal 11 may not operate higher than 1.2 V positive with respect to ground or 0.2 V negative with respect to ground. If the maximum input signal is less than 999 mV, the common-mode input voltage may be raised accordingly.

CA3162E

Circuit Description

The functional block diagram of the CA3162E is shown in Fig. 1. The heart of the system is the V/I converter and reference-current generator. The V/I converter converts the input voltage applied between terminals 10 and 11 to a current that charges the integrating capacitor on terminal 12 for a predetermined time interval. At the end of the charging interval, the V/I converter is disconnected from the integrating capacitor, and a band-gap reference constant-current source of opposite polarity is connected. The number of clock counts that elapse before the charge is restored to its original value is a direct measure of the signal induced current. The restoration is sensed by the comparator, which in turn latches the counter. The count is then multiplexed to the BCD outputs.

The timing for the CA3162E is supplied by a 786-Hz ring oscillator, and the input at terminal 6 determines the sampling rate. A 5-V input provides a high-speed sampling rate (96 Hz), and grounding or floating terminal 6 provides a low-speed (4 Hz) sampling rate. When terminal 6 is fixed at +1.2 V (by placing a 12 K resistor between terminal 6 and the +5-V supply) a "hold" feature is available. While the CA3162E is in the hold mode, sampling continues at 4 Hz but the display data are latched to the last reading prior to the application of the 1.2 V. Removal of the 1.2 V restores continuous display changes. Note, however, that the sampling rate remains at 4 Hz.

Fig. 3 shows the timing of sampling and digit select pulses for the high-speed mode. Note that the basic A/D conversion process requires approximately 5 ms in both modes.

The "EEE" or "---" displays indicate that the range of the system has been exceeded in the positive or negative direction, respectively. Negative voltages to −99 mV are displayed with the minus sign in the MSD. The BCD code is 1010 for a negative overrange (---) and 1011 for a positive overrange (EEE).

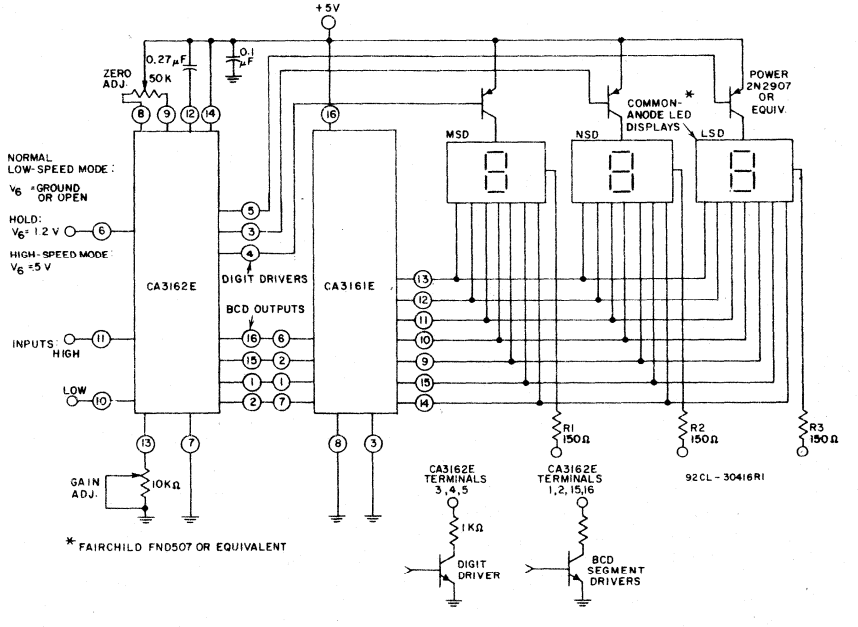


Fig. 2—Basic digital readout system using the CA3162E and the CA3161E.

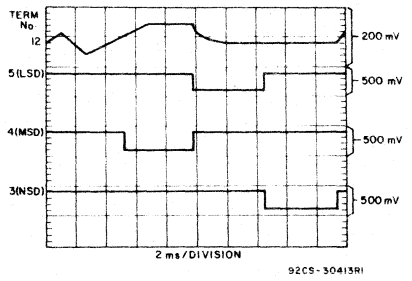


Fig. 3—High speed mode timing diagram.

CA3162E Liquid Crystal Display (LCD) Application

Fig. 4 shows the CA3162E in a typical LCD application. LCD's may be used in favor of LED displays in applications requiring lower power dissipation, such as battery-operated equipment, or when visibility in high-ambient-light conditions is desired.

Multiplexing of LCD digits is not practical, since LCD's must be driven by an ac signal and the average voltage across each segment is zero. Three CD4056B liquid-crystal decoder/drivers are therefore used. Each CD4056B contains an input latch so that the BCD data for each digit may be latched into the decoder. using the inverted digit-select outputs of the CA3162E as strobes.

Inverters G1 and G2 are used as an astable multivibrator to provide the ac drive to the LCD backplane. Inverters G3, G4, and G5 are the digit-select inverters

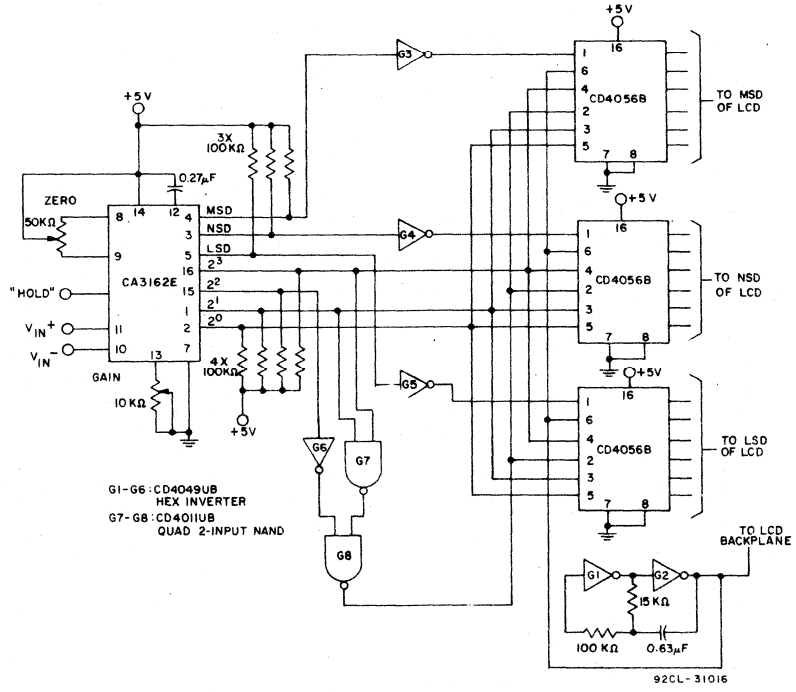


Fig. 4—Typical LCD application.

and require pull-up resistors to interface the open-collector outputs of the CA3162E to COS/MOS logic. The BCD outputs of the CA3162E may be connected directly to the corresponding CD4056B inputs (using pull-up resistors). In this arrangement, the CD4056B decodes the negative sign (—) as an "L" and the positive overlaod indicator (E) as an "H".

CA3162E Common-Cathode, LED Display Application

Fig. 5 shows the CA3162E connected to a CD4511B decode/driver to operate a common-cathode LED display. Unlike the CA3161E, the CD4511B remains blank for all BCD codes greater than nine. After 999 mV the display blanks rather than displaying EEE, as with the CA3161E. When displaying negative voltage, the first digit remains blank instead of (—), and during a negative or positive overrange the display blanks.

The additional logic shown within the dotted area of Fig. 5 restores the negative sign (—), allowing the display of negative numbers as low as —99 mV. Negative overrange is indicated by a negative sign (—) in the MSD position. The rest of the display is blanked. During a positive overrange, only segment b of the MSD is displayed. One inverter from the CD4049B is used to operate the decimal points. By connecting the inverter input to either the MSD or NSD line either DP1 or DP2 will be displayed. Fig. 7 shows the P.C. board and component placement.

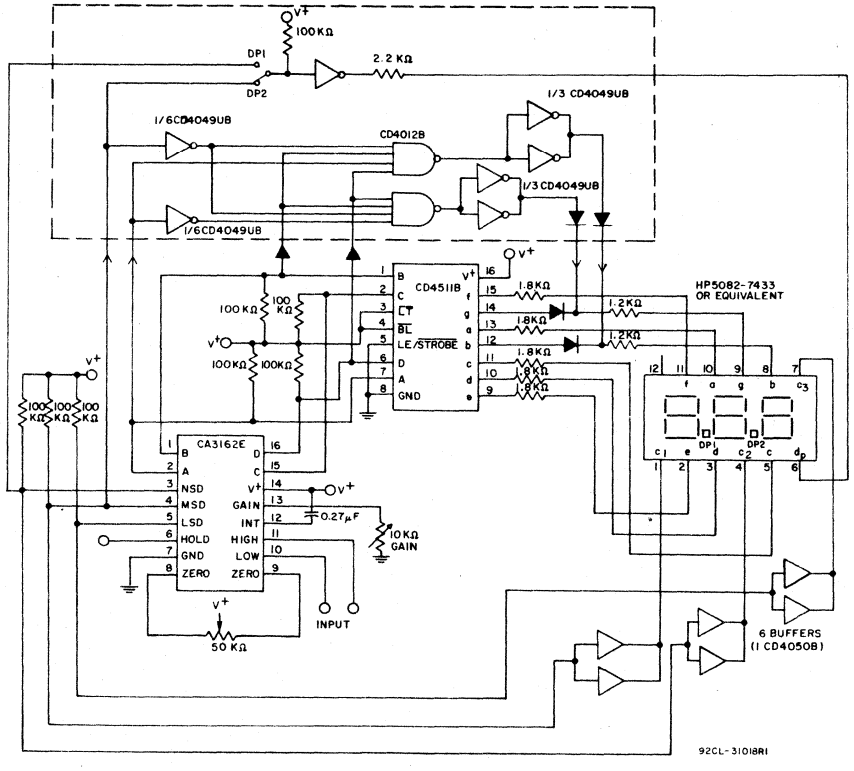
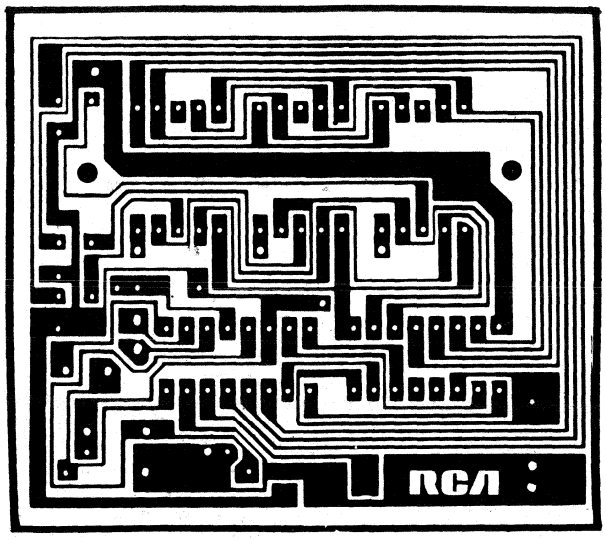


Fig. 5—Typical common-cathode LED application.



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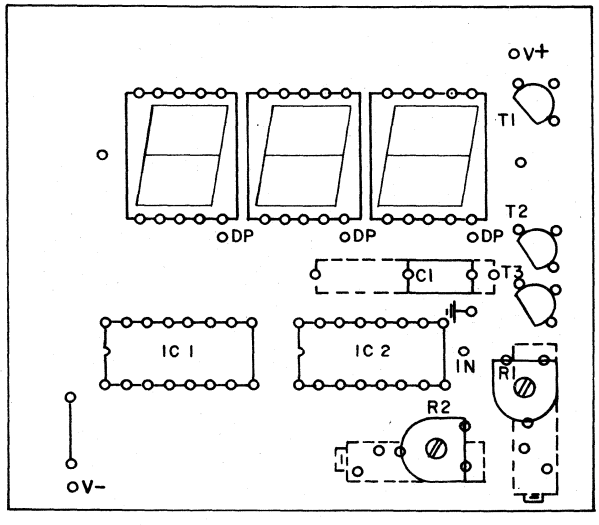
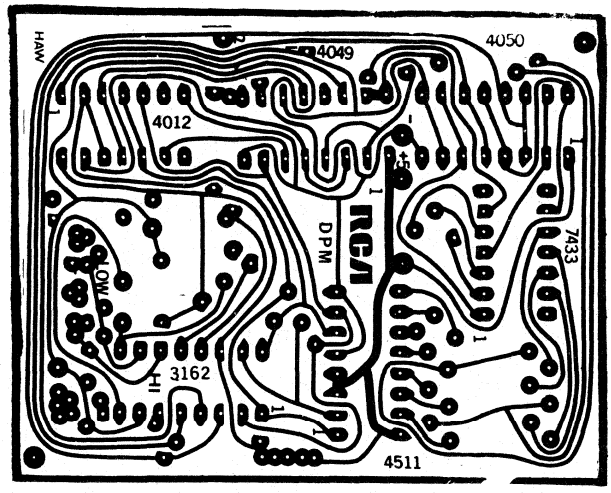


92CS-32693

Fig. 6—P.C. board template (actual size ±3%) and component layout guide for circuit shown in Fig. 2.*

**P.C. board courtesy ETS. Velleman P.V.B.A., St. Amandsberg, Belgium*

CA3162E



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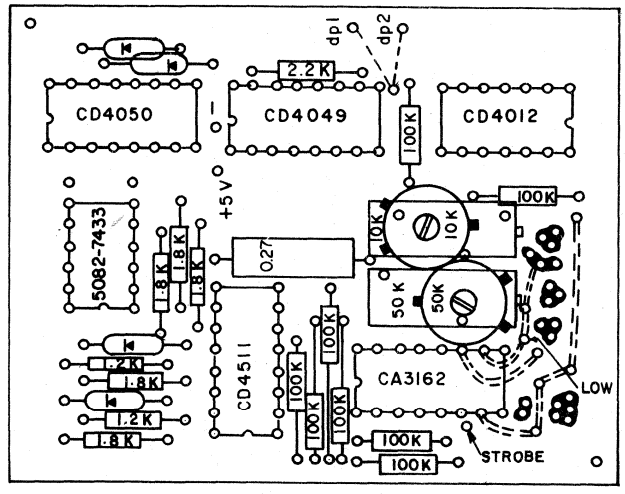
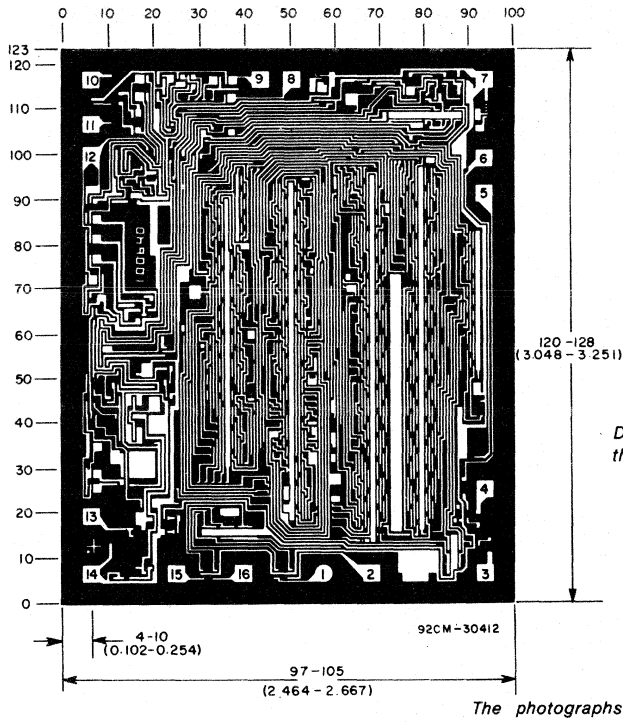


92CS-32694

Fig. 7—P.C. board template (actual size ±3%) and component layout guide for circuit shown in Fig. 5.

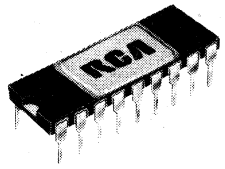


Dimensions and pad layout for the CA3162H Chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each Linear chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3300



18-LEAD DUAL-IN-LINE
SIDE-BRAZED
CERAMIC PACKAGE H-1910

CMOS Video Speed 6-Bit Flash Analog-to-Digital Converter

For Use in Low-Power Consumption, High-Speed Digitization Applications

FEATURES:

- *CMOS low power with speed*
- *Parallel conversion technique*
- *15-MHz sampling rate (66-ns conversion time)*
- *6-bit latched 3-state output with overflow bit*
- *±½ LSB accuracy*
- *Single supply voltage (3 to 10 V)*
- *2 units in series allow 7-bit output*
- *2 units in parallel allow 30-MHz sampling rate*
- *Internal VREF with ext VREF option*

The RCA-CA3300 is a CMOS 50-mW parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high-speed digitization.

The CA3300 operates over a wide full-scale input-voltage range of 2.4 volts up to the dc supply voltage with maximum power consumptions as low as 50 to 200 mW, depending upon the clock frequency selected. When operated from a 5-volt supply at a clock frequency of 11 MHz, the power consumption of the CA3300 is less than 50 mW. When operated from an 8-volt supply at a frequency of 15 MHz, the power consumption is less than 150 mW.

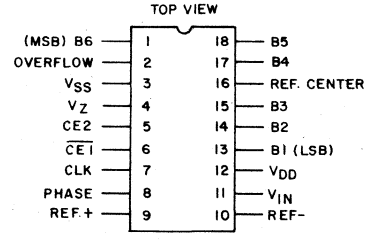
The intrinsic high conversion rate makes the CA3300 ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3300s in series to increase the resolution of the conversion system. A series connection of two CA3300s may be used to produce a 7-bit high-speed converter. Operation of two CA3300s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz). CA3300s in parallel may be combined with a high-speed 6-bit D/A converter, a binary adder, control logic, and an op amp to form a very high-speed A/D converter.

Sixty-four paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3300. Sixty-three comparators are required to quantize all input voltage levels in this 6-bit converter, and the additional comparator is required for the overflow bit.

The CA3300 type is available in an 18-lead dual-in-line ceramic package (D suffix) or in chip form (H suffix).

APPLICATIONS

- *The CA3300 is especially suited for high-speed conversion applications where low power is also important*
- *TV video digitizing (industrial/security)*
- *High-speed A/D conversion*
- *Ultrasound signature analysis*
- *Transient signal analysis*
- *High-energy physics research*
- *High-speed oscilloscope storage/display*
- *General-purpose hybrid ADCs*
- *Optical character recognition*
- *Radar pulse analysis*
- *Motion signature analysis*



92CS-32263RI

TERMINAL ASSIGNMENT

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	6	Bits
Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=15 MHz, gain adjusted	—	±0.5	±0.8	LSB
Differential Linearity Error	V_{DD}=8, V_{REF}=7.68 V CLK=15 MHz	—	±0.5	±0.8	
Quantizing Error		-1/2	—	1/2	
Analog Input: Full Scale Range	V_{DD}=8 V CLK=15 MHz	2.4	—	V_{DD} +0.5	V
Input Capacitance		—	50	—	pF
Input Current		—	600	1000	μA
Gain Temperature Coefficient	V_{DD}=8 V, CLK=15 MHz	—	0.016	—	LSB/°C
Maximum Conversion Speed	V_{DD}=5 V	—	12M	—	SPS
	V_{DD}=8 V	15M	19M	—	
Device Current (Excludes I_{REF}, I_Z)	V_{DD}=5 V (CLK=11 MHz)	—	7	—	mA
	V_{DD}=8 V (CLK=15 MHz)	—	22	—	
	V_{DD}=5 V (Auto Balance State)	—	6.4	16	
	V_{DD}=8 V (Auto Balance State)	—	24	40	
Ladder Impedance		1000	1400	1800	Ω
Digital Inputs: Low Voltage	V_{DD}=5 V	—	—	1.5	V
	V_{DD}=8 V	—	—	2.5	V
High Voltage	V_{DD}=5 V	3.5	—	—	V
	V_{DD}=8 V	5.5	—	—	V
Input Current	V_{DD}=8 V	—	±1	—	μA
Digital Outputs: Output Low (Sink) Current	V_{DD}=5 V, V_O=0.4 V	1.6	10	—	mA
	V_{DD}=8 V, V_O=0.5	3.2	15	—	
Output High (Source) Current	V_{DD}=5 V, V_O=4.6 V	-0.8	6	—	
	V_{DD}=8 V, V_O=7.5 V	-1.6	9	—	
Zener Voltage	I_Z=10 mA	6.2	6.8	7.4	V
Zener Dynamic Impedance	I_Z=10 mA	—	10	30	Ω
Zener Temperature Coefficient		—	0.5	—	mV/°C
Digital Output Delay, t_d	V_{DD}=8 V	—	20	—	ns
Aperture Time	V_{DD}=8 V	—	25	—	

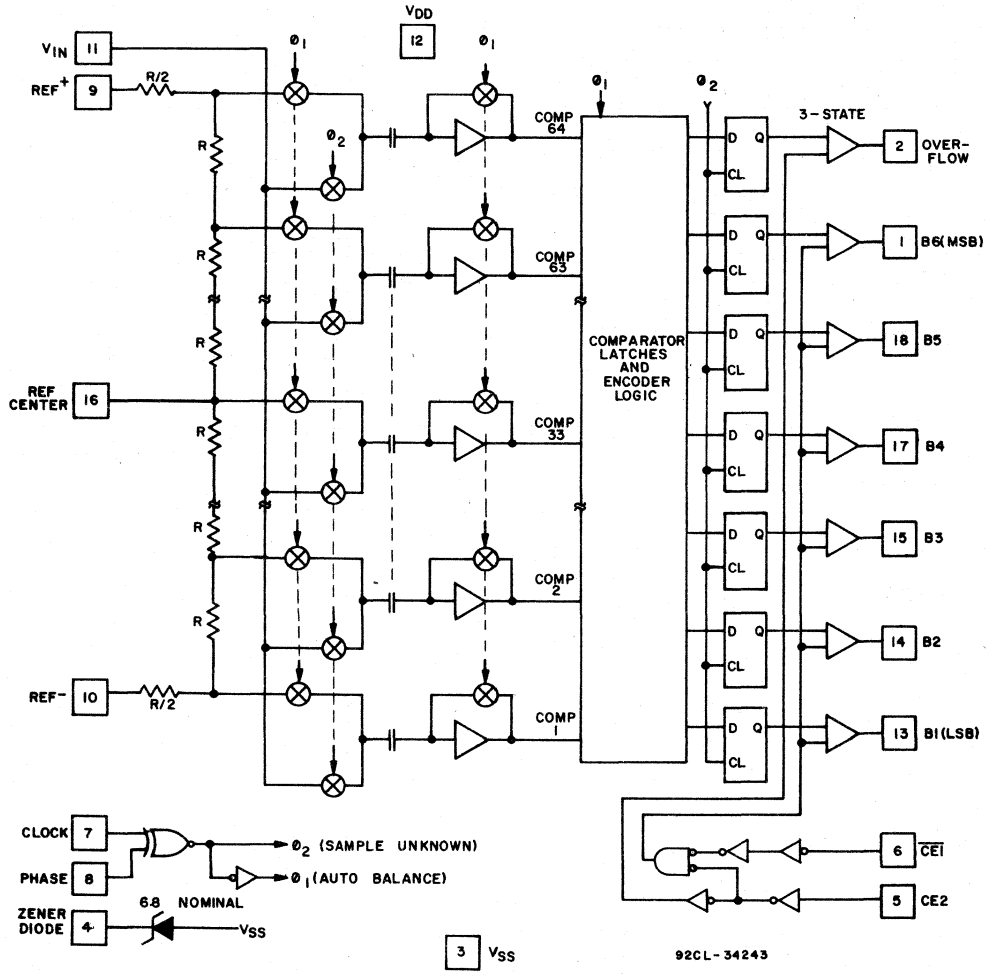
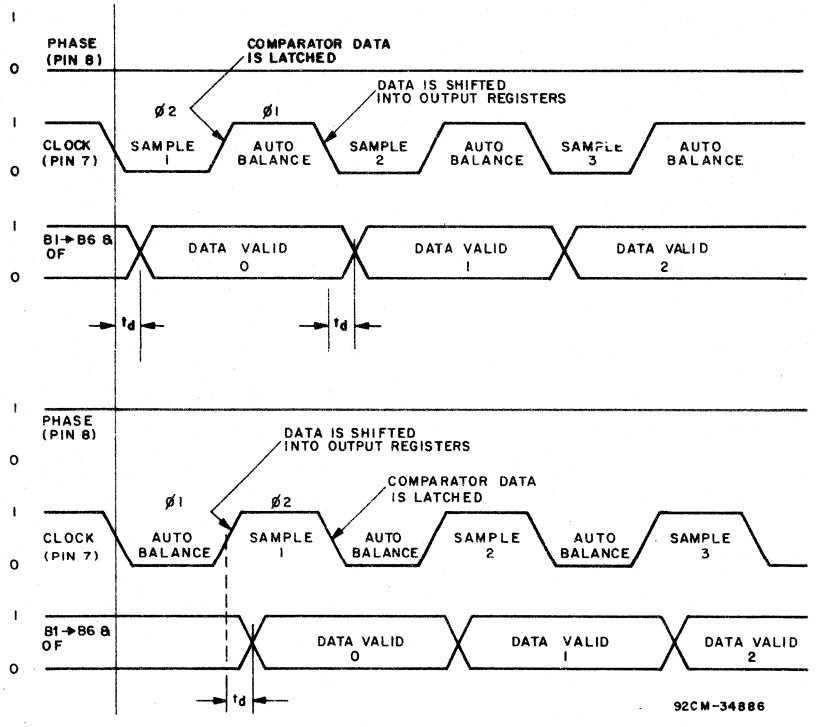


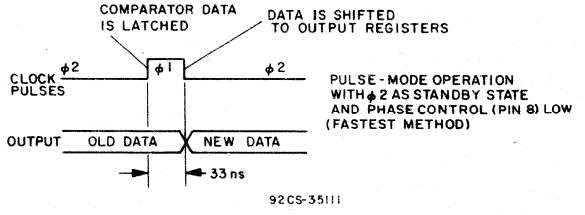
Fig. 1 - Block diagram for the CA3300.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

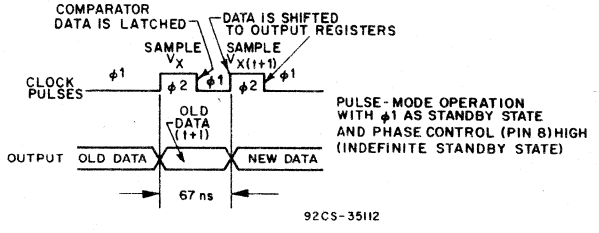
DC SUPPLY VOLTAGE RANGE (V_{DD})
(VOLTAGE REFERENCED TO V_{SS} TERMINAL) ..... -0.5 to 10 V
INPUT VOLTAGE RANGE
ALL INPUTS EXCEPT ZENER (PIN 4) ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT
CLK, PH, $\overline{CE1}$, CE2, V_{IN} ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = -40 to 55°C ..... 315 mW
FOR T_A = 55°C to 85°C ..... Derate linearly at 3.3 mW/°C
TEMPERATURE RANGE
OPERATING ..... -40 to +85°C
STORAGE ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
AT DISTANCE 1/16 ± 1/32 in. (1.59 ± 0.79 mm) FROM CASE FOR 10 s MAX. ..... +265°C



(a)



(b)



(c)

Fig. 2 - Timing diagrams for the CA3300.

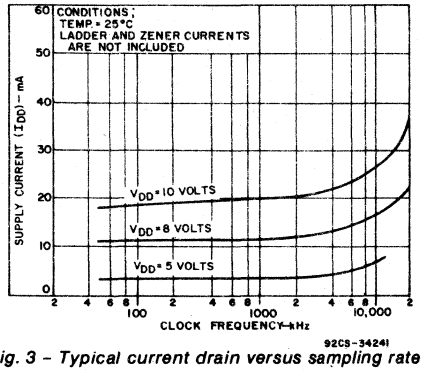


Fig. 3 - Typical current drain versus sampling rate as a function of supply voltage.

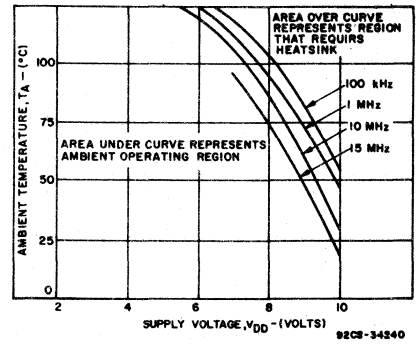


Fig. 4 - Maximum ambient temperature versus supply voltage. (Above curve includes ladder dissipation but not the zener dissipation.)

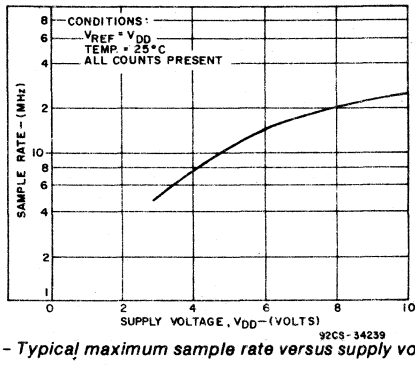


Fig. 5 - Typical maximum sample rate versus supply voltage.

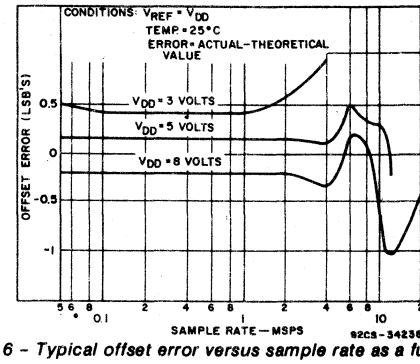


Fig. 6 - Typical offset error versus sample rate as a function of supply voltage. (See literature for offset trim.)

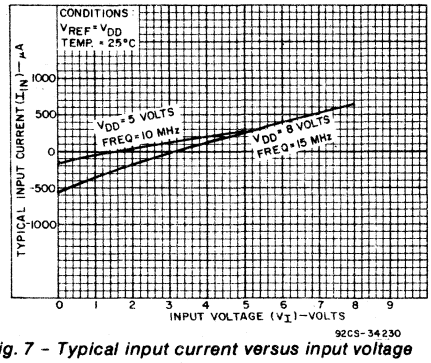


Fig. 7 - Typical input current versus input voltage as a function of supply voltage.

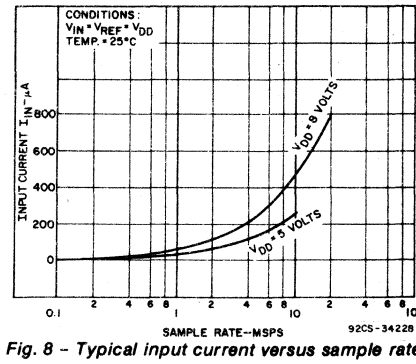


Fig. 8 - Typical input current versus sample rate as a function of supply voltage.

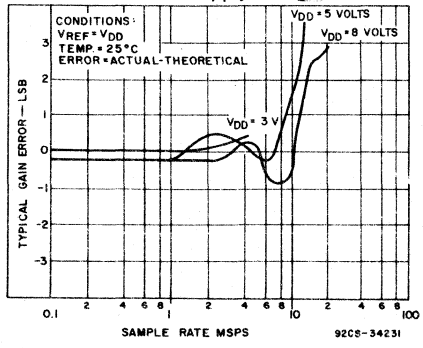


Fig. 9 - Typical gain error versus sample rate as a function of supply voltage. (See literature for gain trim.)

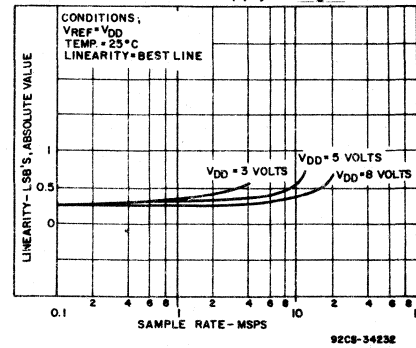


Fig. 10 - Typical linearity versus sample rate as a function of supply voltage.

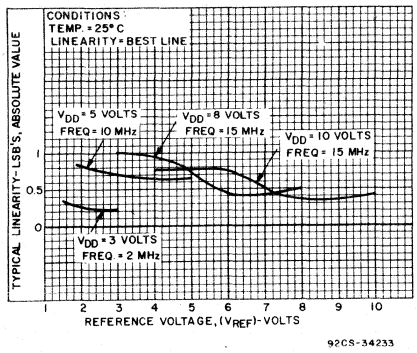


Fig. 11 - Typical linearity versus reference voltage as a function of supply voltage.

Device Operation

A sequential parallel technique is used by the CA3300 converter to obtain its high-speed operation. The sequence consists of the "Auto Balance" phase, Ø1, and the "Sample Unknown" phase Ø2. (Refer to the circuit diagram.) Each conversion takes one clock cycle.* With the phase control (pin 8) low, the "Auto Balance" (Ø1) occurs during the High period of the clock cycle, and the "Sample Unknown" (Ø2) occurs during the low period of the clock cycle.

During the "Auto Balance" phase, a transmission switch is used to connect each of 64 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{tap}(N) = [(V_{REF}/64) \times N] - [V_{REF}/(2 \times 64)]$$
$$= V_{REF}[(2N - 1)/128]$$

Where: $V_{tap}(n)$=reference ladder tap voltage at point n.
V_{REF}=voltage across R^- to R^+
N=tap number (1 through 64)

The other side of the capacitor is connected to a single stage amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately, $(V_{DD}-V_{SS})/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Sample Unknown" phase, all ladder tap switches are opened, the comparator amplifiers are no longer shorted, and V_{IN} is switch to all 64 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators with tap voltages greater than V_{IN} will drive the comparator outputs to a "low" state, all comparators with tap voltage lower than V_{IN} will drive the comparator outputs to a "high" state.

*This device requires only a single phase clock. The terminology of $\phi 1$ and $\phi 2$ refers to the High and Low periods of the same clock.

The status of all these comparator amplifiers are stored at the end of this phase (Ø2), by a secondary latching amplifier stage. Once latched, the status of the 64 comparators is decoded by a 64 to 7 bit decode array and the results are clocked into a storage register at the rising edge of the next Ø2.

A 3-state buffer is used at the output of the 7 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B6 when it is in a high state. CE2 will independently disable B1 through B6 and the OF buffers when it is in the low state.

To facilitate usage of this device a phase control input is provided which can effectively complement the clock as it enters the chip. Also, an onboard zener is provided for use as a reference voltage.

Continuous Clock Operation

One complete conversion cycle can be traced through the CA3300 via the following steps. (Refer to timing diagram Fig. 2a.) With the phase control in a 'High' state, the rising edge of the clock input will start a "sample" phase. During this entire 'High' state of the clock, the 64 comparators will track the input voltage and the 64 latches will track the comparator outputs. At the falling edge of the clock, all 64 comparator outputs are captured by the 64 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this 'Low' state of the clock the output of the latches propagates through the decode array and a 7-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 7-bit code is shifted into the output registers and appears with time delay t_d as valid data at the output of the 3-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse Mode Operation

For sampling high-speed nonrecurrent or transient data, the converter may be operated in a pulse mode in one of two ways. The fastest method is to keep the converter in the Sample Unknown phase, Ø2, during the standby state. The device can now be pulsed through the Auto Balance phase with as little as 33 ns. The analog value is captured on the leading edge of Ø1 and is transferred into the output registers on the trailing edge of Ø1. We are now back in the standby state, Ø2, and another conversion can be started within 33 ns, but not later than 10 μs due to the eventual droop of the commutating capacitors. Another advantage of this method is that it has the potential of having the lowest power drain. The larger the time ratio between Ø2 and Ø1, the lower the power consumption. (See timing diagram Fig. 2b.)

The second method uses the Auto Balance phase, Ø1, as the standby state. In this state the converter can stay indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two Ø2 pulses. The first pulse starts a Sample Unknown phase and captures the analog value in the comparator latches on the trailing edge. A second Ø2 pulse is needed to transfer the data into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes place in 67 ns, but the repetition rate may be as slow as desired. The disadvantage to this method is the higher device dissipation due to the low ratio of Ø2 to Ø1. (See timing diagram Fig. 2c.)

Increased Accuracy

In most cases the accuracy of the CA3300 should be

sufficient without any adjustments. In applications where accuracy is of utmost importance, three adjustments can be made to obtain better accuracy; i.e., offset trim, gain trim, and midpoint trim.

Offset Trim

In general offset correction can be done in the preamp circuitry by introducing a DC shift to V_{IN} or by the offset trim of the op-amp. When this is not possible the R^- (pin 10) input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is ½ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = \tfrac{1}{2} \text{ LSB} = \tfrac{1}{2}(V_{REF}/64)$$
$$= V_{REF}/128$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50-ohm pot connected between R^- and ground will accomplish the adjustment. Set V_{IN} to ½ LSB and trim the pot until the 0 to 1 transition occurs.

If V_{IN} for the first transition is greater than the theoretical, then the 50-ohm pot should be connected between R^- and a negative voltage of about 2 LSB's. The trim procedure is as stated previously.

Gain Trim

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op-amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 63 to overflow transition. That voltage is ½ LSB less than V_{REF} and is calculated as follows:

$$V_{IN} \text{ (63 to 64 transition)} = V_{REF} - V_{REF}/128$$
$$= V_{REF}\,(127/128)$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 63 to overflow transition. Now adjust V_{REF} until that transition occurs on the outputs.

Midpoint Trim

The reference center (RC), pin 16, is available to the user as the approximate midpoint of the resistor ladder. The actual count that is brought out is count 33. To trim the midpoint the offset and gain trims should be done first. The theoretical transition from count 32 to 33 occurs at 32½ LSB's. That voltage is as follows:

$$V_{IN} \text{ (32 to 33 transition)} = 32.5\,(V_{REF}/64)$$

An adjustable voltage follower can be connected to the RC pin or a 2K pot can be connected between R^+ and R^- with the wiper connected to RC. Set V_{IN} to the 32 to 33 transition voltage, then adjust the voltage follower or the pot until the transition occurs on the output bits.

The Reference Center point can also be used to create some unique transfer functions. For example, if R^- is grounded, RC is connected to 3.25 volts, and R^+ is connected to 4.8 volts then the lower order counts, 1 through 33, will have an LSB value of 100 mV while the upper order counts, 34 through Overflow, will have an LSB value of 50 mV. This effectively provides twice the sensitivity in the upper counts as compared to the lower counts.

7-Bit Resolution

To obtain 7-bit resolution, two CA3300s can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enabler controls—all of which are available on the CA3300.

The first step for connecting a 7-bit circuit is to totem-pole the ladder networks, as illustrated in Fig. 13. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the seventh bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower a-d converter and the CE2 control of the upper a-d converter. The three-state outputs of the two devices (bits 1 through 6) are now connected in parallel to complete the circuitry. The complete circuit for a 7-bit a-d converter is shown in Fig. 14.

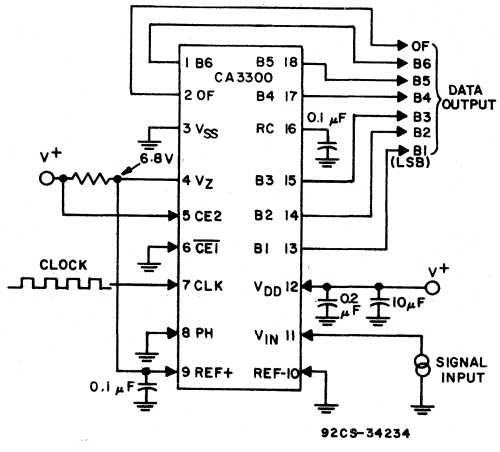


Fig. 12 - Typical CA3300 6-bit configuration 15-MHz sampling rate.

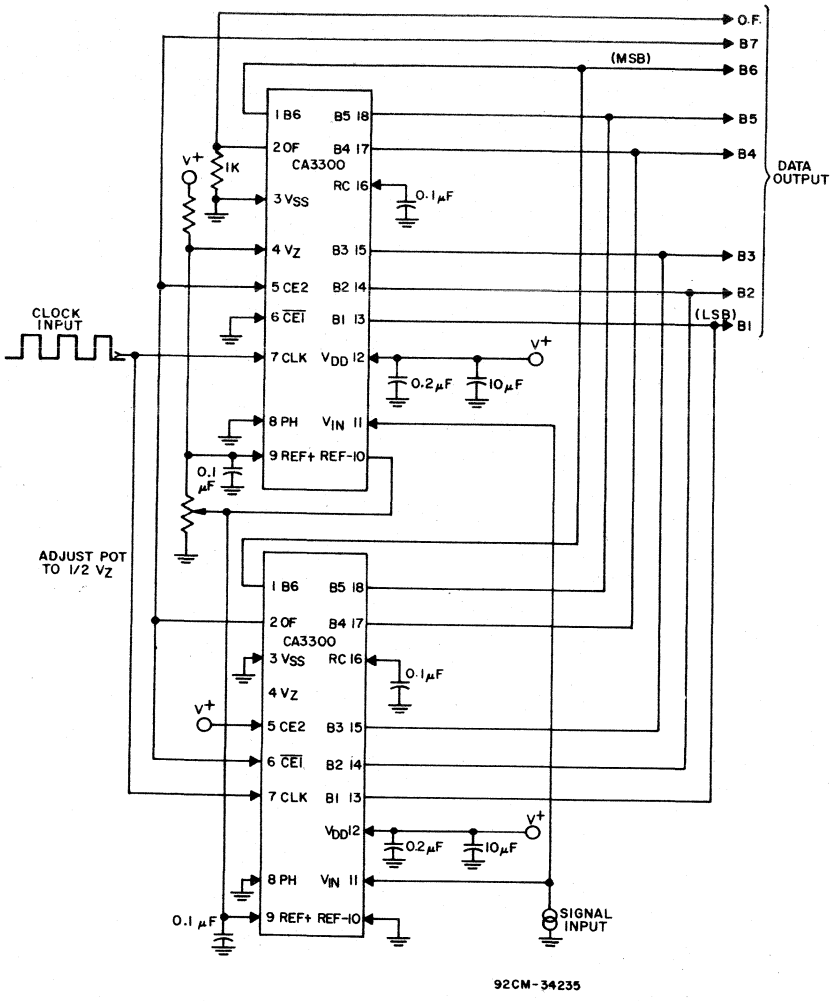


Fig. 13 - Typical CA3300 7-bit resolution configuration 15-MHz sampling rate.

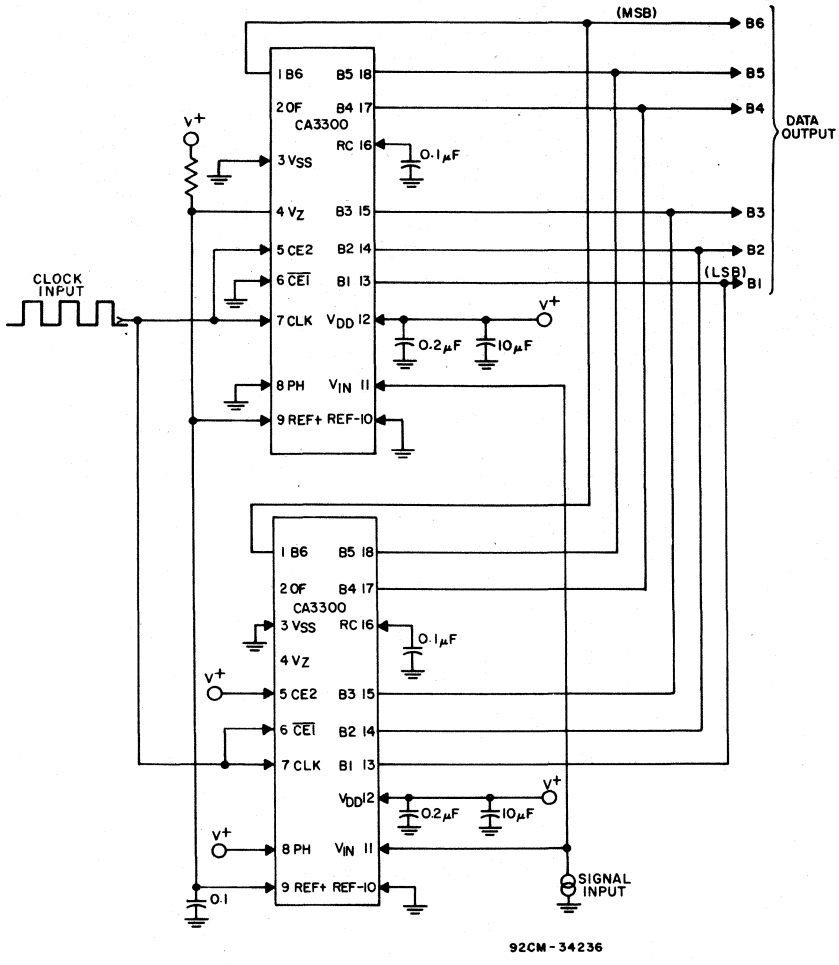


Fig. 14 - Typical CA3300 6-bit resolution configuration 30-MHz sampling rate.

8-Bit to 12-Bit Conversion Techniques

To obtain 8 to 12-bit resolution and accuracy, use a feed-forward conversion technique. Two a-d converters will be needed to convert up to 11 bits; three a-d converters to convert 12 bits. The high speed of the CA3300 allows 12-bit conversions in the 500 to 900-ns range.

The circuit diagram of a high-speed 12-bit a-d converter is shown in Fig. 15. In the feed-forward conversion method two sequential conversions are made. Converter A first does a coarse conversion to 6 bits. The output is applied to a 6-bit d-a converter whose accuracy level is good to 12 bits. The d-a converter output is then subtracted from the input voltage, multiplied by 32, and then converted by a second flash a-d converter, which is connected in a 7-bit configuration. The answers from the first and second conversions are added together with bit 1 of the first conversion overlapping bit 7 of the second conversion.

When using this method, take care that:

- The linearity of the first converter is better than ½ LSB.
- An offset bias of 1 LSB (1/64) is subtracted from the first conversion since the second converter is unipolar.
- The d-a converter and its reference are accurate to the total number of bits desired for the final conversion (the a-d converter need only be accurate to 6 bits).

  The first converter can be offset-biased by adding a 20-Ω resistor at the bottom of the ladder and increasing the reference voltage by 1 LSB. If a 6.40-voltage reference is used in the system, for example, then the first CA3300 will require a 6.5-V reference.

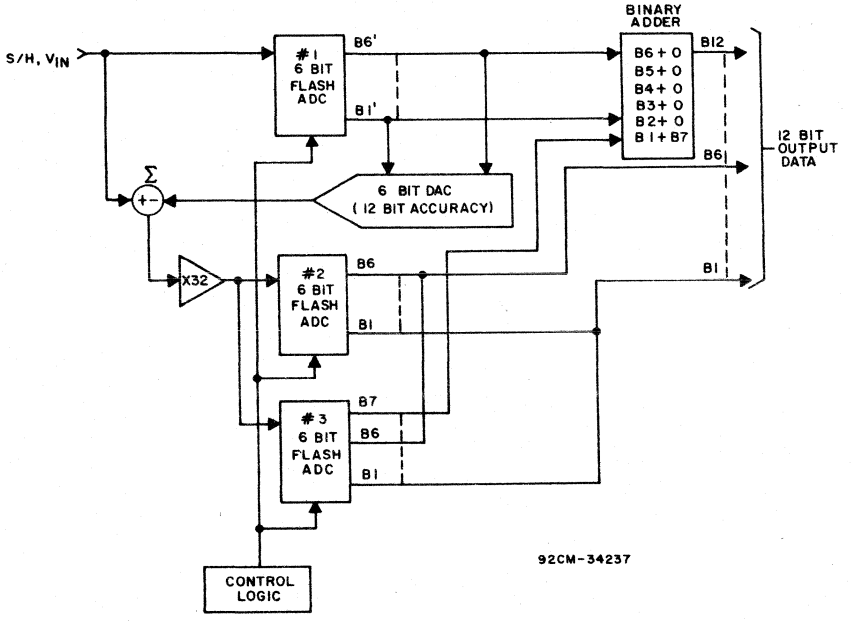


Fig. 15 - Typical CA3300 800-nanosecond 12-bit ADC system.

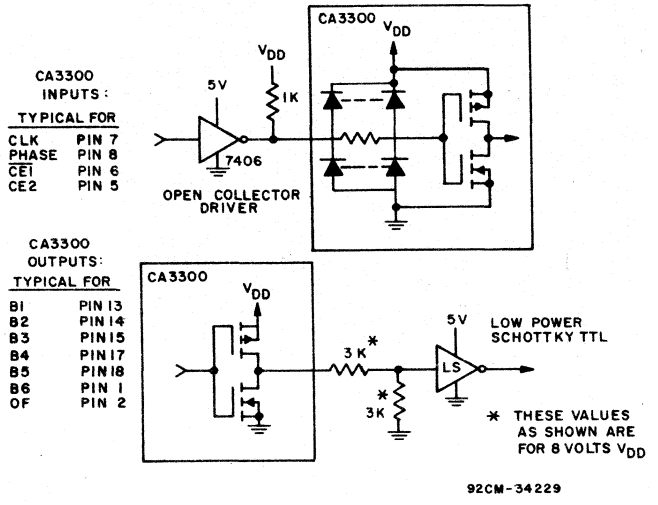
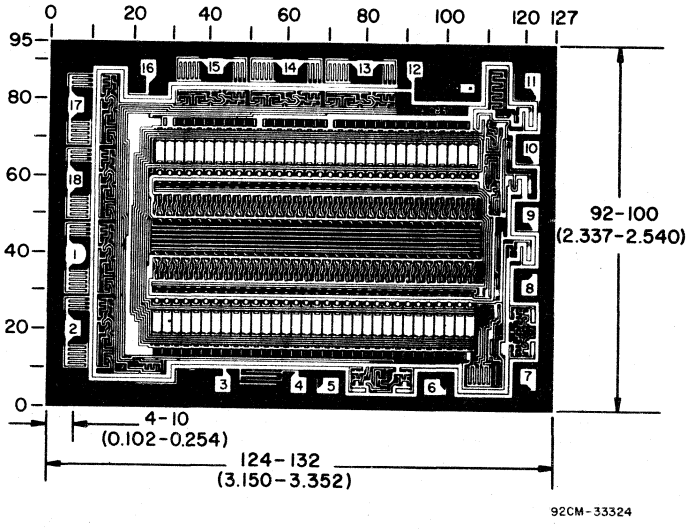


Fig. 16 - TTL interface circuit for V_{DD} >5.5 volts.

OUTPUT CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE* VREF 7.68 (VOLTS)	VREF 6.40 (VOLTS)	VREF 5.12 (VOLTS)	VREF 3.20 (VOLTS	BINARY OUTPUT CODE 0.F	B6	B5	B4	B3	B2	(LSB) B1	DECIMAL COUNT
ZERO	0.00	0.00	0.00	0.00	0	0	0	0	0	0	0	0
1 LSB	0.12	0.10	0.08	0.05	0	0	0	0	0	0	1	1
2 LSB	0.24	0.20	0.16	0.10	0	0	0	0	0	1	0	2
'	'	'	'	'	'	'	'	'	'	'	'	'
'	'	'	'	'	'	'	'	'	'	'	'	'
'	'	'	'	'	'	'	'	'	'	'	'	'
'	'	'	'	'	'	'	'	'	'	'	'	'
½ Full Scale — 1 LSB	3.72	3.10	2.48	1.55	0	0	1	1	1	1	1	31
½ Full Scale	3.84	3.20	2.56	1.60	0	1	0	0	0	0	0	32
½ Full Scale +1 LSB	3.96	3.30	2.64	1.65	0	1	0	0	0	0	1	33
'	'	'	'	'	'	'	'	'	'	'	'	'
'	'	'	'	'	'	'	'	'	'	'	'	'
'	'	'	'	'	'	'	'	'	'	'	'	'
'	'	'	'	'	'	'	'	'	'	'	'	'
Full Scale — 1 LSB	7.44	6.20	4.96	3.10	0	1	1	1	1	1	0	62
Full Scale	7.56	6.30	5.04	3.15	0	1	1	1	1	1	1	63
Overflow	7.68	6.40	5.12	3.20	1	1	1	1	1	1	1	127

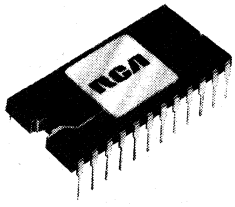
*THE VOLTAGES LISTED BELOW ARE THE IDEAL CENTERS OF EACH OUTPUT CODE SHOWN AS A FUNCTION OF ITS ASSOCIATED REFERENCE VOLTAGE.



Dimensions and pad layout for CA3300H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



(D) SUFFIX
24-Lead Dual-In-Line
Side-Brazed Ceramic Package

CMOS Video Speed 8-Bit Flash Analog-to-Digital Converter

For Use in Low-Power Consumption, High-Speed Digitization Applications

Features:
- *CMOS low power with SOS speed*
- *Parallel conversion technique*
- *15-MHz sampling rate (66-ns conversion time)*
- *8-bit latched 3-state output with overflow bit*
- *± ½ LSB accuracy (typ.)*
- *Single supply voltage (4 to 8 V)*
- *2 units in series allow 9-bit output*
- *2 units in parallel allow 30-MHz sampling rate*

The RCA CA3308* is a CMOS 240-mW parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high-speed digitization.

The CA3308 operates over a wide full-scale input-voltage range of 4 volts up to 8 volts with maximum power consumptions as low as 240 mW, depending upon the clock frequency selected. When operated from a 5-volt supply at a clock frequency of 15 MHz, the power consumption of the CA3308 is typically 240 mW.

The intrinsic high conversion rate makes the CA3308 ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3308s in series to increase the resolution of the conversion system. A series connection of two CA3308s may be used to produce a 9-bit high-speed converter. Operation of two CA3308s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz). CA3308s may be combined with a high-speed 8-bit D/A converter, a binary adder, control logic, and an op amp to form a very high-speed 15-bit A/D converter.

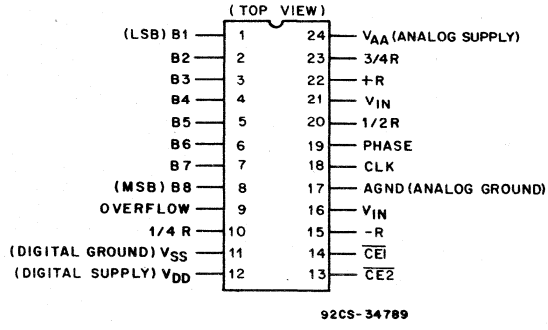
256 paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3308.

255 comparators are required to quantize all input voltage levels in this 8-bit converter, and the additional comparator is required for the overflow bit.

The voltage supply for analog circuitry is termed V_{AA} and AGND. The voltage supply for digital circuitry is termed V_{DD} and V_{SS}.

The CA3308 type is available in a 24-lead dual-in-line ceramic package (D suffix).

Applications:
- *The CA3308 is especially suited for high-speed conversion applications where low power is also important*
- *TV video digitizing (industrial/security/broadcast)*
- *High-speed A/D conversion*
- *Ultrasound signature analysis*
- *Transient signal analysis*
- *High-energy physics research*
- *High-speed oscilloscope storage/display*
- *General-purpose hybrid ADCs*
- *Optical character recognition*
- *Radar pulse analysis*
- *Motion signature analysis*
- *µP data acquisition systems*



TERMINAL ASSIGNMENT

* Formerly Developmental Type No. TA11279.

CA3308

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE (V_{DD} AND V_{AA})
(VOLTAGE REFERENCED TO V_{SS} TERMINAL) ..... −0.5 to +8 V

INPUT VOLTAGE RANGE
ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

DC INPUT CURRENT
CLK, PH, CE1, CE2, V_{IN} ..... ±10 mA

POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A=−40 to 55°C ..... 315 mW
FOR T_A=55°C to 85°C ..... Derate linearly at 3.3 mW/°C

TEMPERATURE RANGE
OPERATING ..... −40 to +85°C
STORAGE ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING)
AT DISTANCE 1/16 ± 1/32 in. (1.59 ± 0.79 mm) FROM CASE FOR 10 s MAX. ..... +265°C

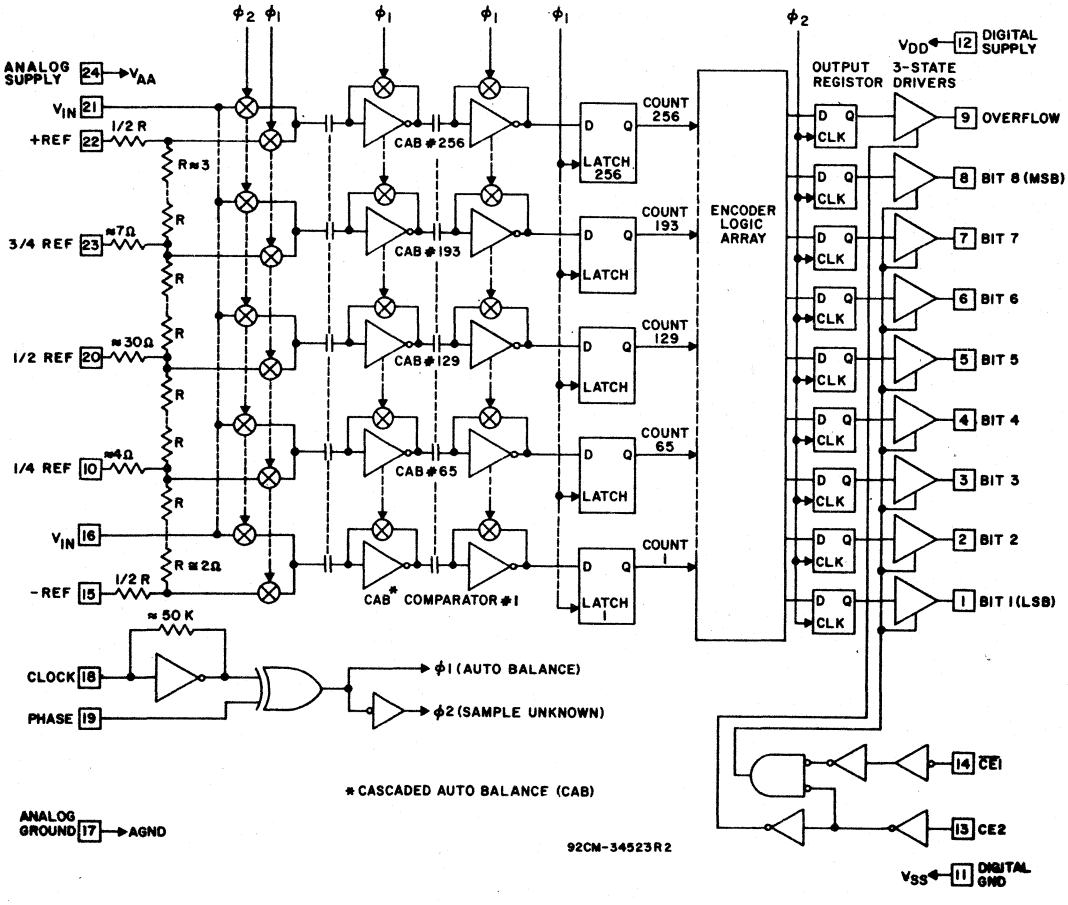


Fig. 1-Block diagram for the CA3308.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS $V_{AA} = V_{DD}$	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	8	Bits
Linearity Error	V_{DD}=5 V, V_{REF}=6.4 V CLK=15 MHz, gain adjusted	—	—	±1	(CA3308D)
Differential Linearity Error	V_{DD}=5 V_{REF}=6.4 V CLK=15 MHz	—	—	±1	(CA3308D)
Quantizing Error		−½	—	½	LSB
Analog Input:	V_{DD}=5 V				
Full Scale Range	CLK=15 MHz	4	—	8	V
Input Capacitance		—	50	—	pF
Input Current	V_{IN}= 6.4 V	—	1000	2000	μA
Maximum Conversion Speed	V_{DD}=5 V	15 M	17 M	—	SPS
Device Current (Excludes I_{REF})	V_{DD}=5 V (CLK=15 MHz)	—	30	—	mA
Ladder Impedance		300	600	900	Ω
Digital Inputs:					
Low Voltage		—	—	1.5	V
High Voltage	V_{DD}=5 V	3.5	—	—	V
Input Current (Except Pin 18)		—	±1	—	μA
Digital Outputs:					
Output Low (Sink) Current	V_{DD}=5 V, V_O=0.4 V	3.2	10	—	mA
Output High (Source) Current	V_{DD}=5 V, V_O=4.6 V	1.6	−6	—	
Digital Output Delay, t_d	V_{DD}=5 V	—	25	—	ns

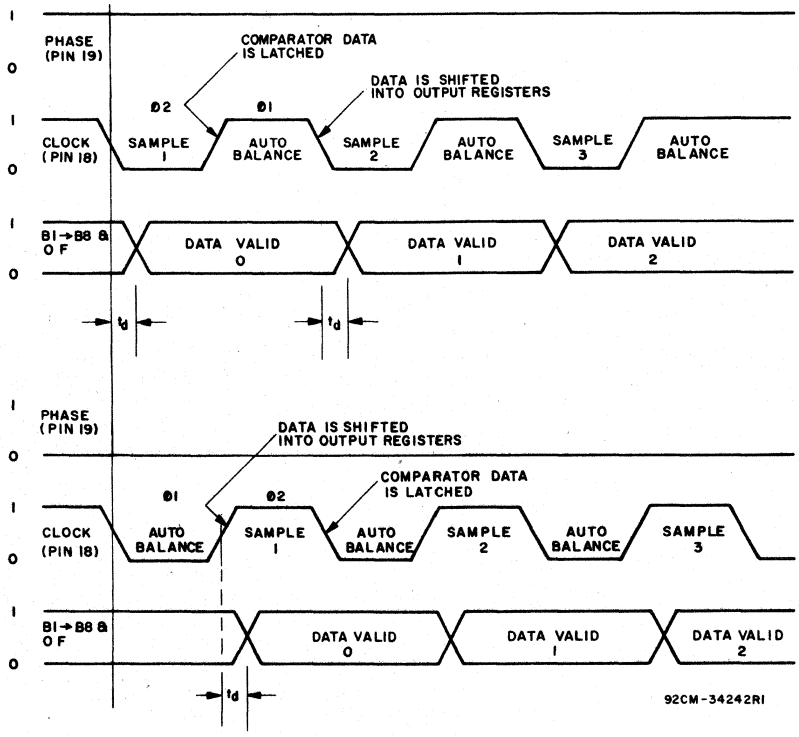


Fig. 2-Timing diagram for the CA3308.

CA3308

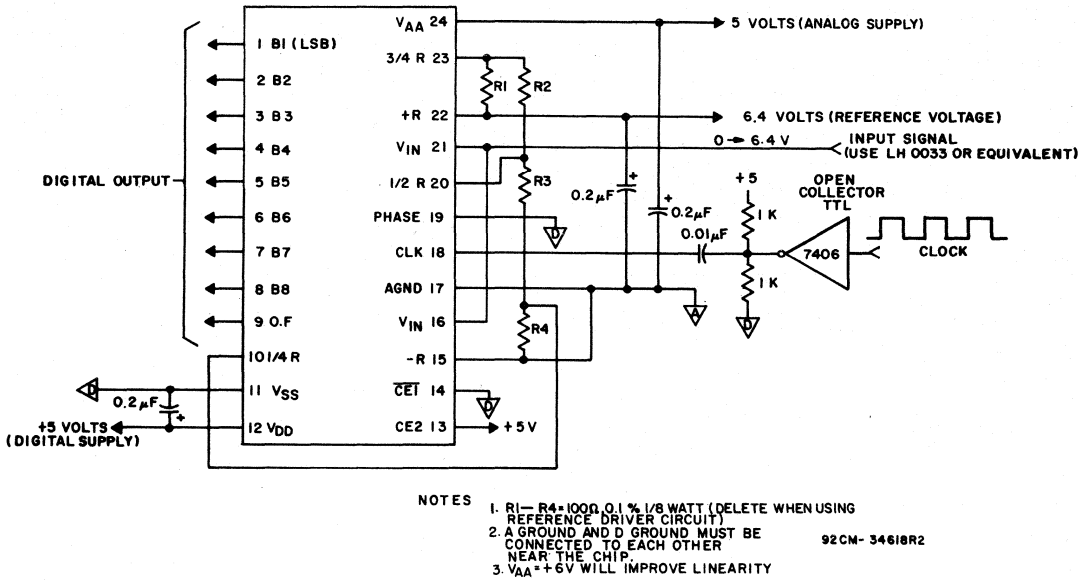


Fig. 3-Typical circuit configuration for the CA3308.
(15-MHz sampling rate)

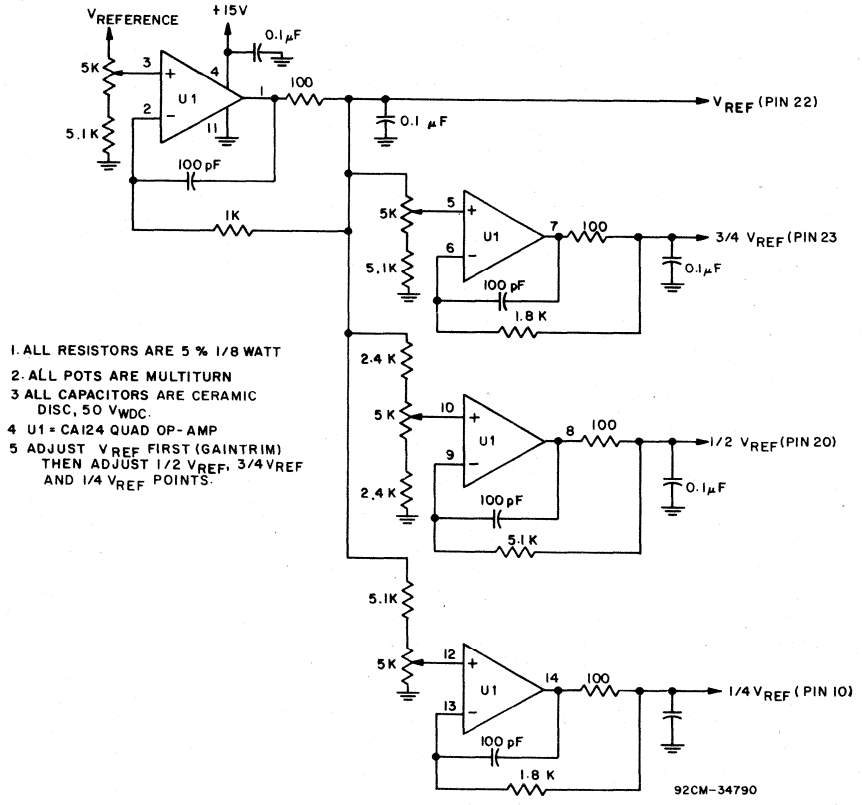


Fig. 4-Reference driver circuit.
(Use for maximum linearity)

Device Operation

A sequential parallel technique is used by the CA3308 converter to obtain its high-speed operation. The sequence consists of the "Auto Balance" phase, Ø1, and the "Sample Unknown" phase Ø2. (Refer to the circuit diagram.) Each conversion takes one clock cycle.* With the phase control (pin 8) high, the "Auto Balance" (Ø1) occurs during the High period of the clock cycle, and the "Sample Unknown" (Ø2) occurs during the low period of the clock cycle.

During the "Auto Balance" phase, a transmission switch is used to connect each of the first set of 256 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{tap}(N)=[(N/256)\,V_{REF}]-[(1/512)\,V_{REF}]$$
$$=[(2N-1/512]V_{REF}$$

Where:

$V_{tap}(n)$=reference ladder tap voltage at point n.

V_{REF}=voltage across −REF to +REF

N=tap number (1 through 256)

The other side of these capacitors are connected to single stage amplifiers whose outputs are shorted to their inputs by switches. This balances the amplifiers at their intrinsic trip points, which is approximately, $V_{DD}-V_{SS}/2$. The first set of capacitors now charge to their associated tap voltages.

At the same time a second set of commutating capacitors and amplifiers are also auto-balanced. The balancing of the second stage amplifier at its intrinsic trip point removes any tracking differences between the first and second amplifier stages. The cascaded auto-balance (CAB) technique, used here, increases comparator sensitivity and temperature tracking.

In the "Sample Unknown" phase, all ladder tap switches and comparator shorting switches are opened. At the same time V_{in} is switched to the first set of commutating capacitors. Since the other end of the capacitors are now looking into an effectively open circuit, any input voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators that had tap voltages greater than V_{in} will go to a "low" state at their outputs. All comparators that had tap voltages lower than V_{in} will go to a "high" state.

The status of all these comparator amplifiers are ac coupled through the second stage comparator and stored at the end of this phase (Ø2), by a latching amplifier stage. Once latched, the status of the comparators are decoded by a 256 to 9-bit decode array and the results are clocked into a storage register at the rising edge of the next Ø2.

A 3-state buffer is used at the output of the 9 storage registers which are controlled by two chip-enable signals. CE1 will independently disable B1 through B8 when it is in a high state. CE2 will independently disable B1 through B8 and the OF buffers when it is in the low state.

To facilitate usage of this device a phase control input is provided which can effectively complement the clock as it enters the chip.

Continuous Clock Operation

One complete conversion cycle can be traced through the CA3308 via the following steps. (Refer to timing diagram No. 1.) With the phase control in a "low" state, the rising edge of the clock input will start a "sample" phase. During this entire "high" state of the clock, the comparators will track the input voltage and the latches will track the comparator outputs. At the falling edge of the clock, all 256 comparator outputs are captured by the 256 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this "low" state of the clock the output of the latches propagates through the decode array and a 9-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 9-bit code is shifted into the output registers and appears with time delay t_d as valid data at the output of the 3-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

*This device requires only a single phase clock. The terminology of 01 and 02 refers to the High and Low periods of the same clock.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD}—V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

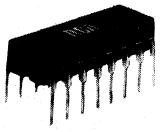
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

CA3081, CA3082 Types

16-Lead Dual-In-Line
Frit-Seal (Hermetic)
Package H-1807



16-Lead Dual-In-Line
Plastic Package H-1622

General-Purpose High-Current N-P-N Transistor Arrays

CA3081 — Common-Emitter Array
CA3082 — Common-Collector Array

Directly Drive 7-Segment Incandescent Displays and Light-Emitting-Diode (LED) Displays

Features:

- *7 transistors permit a wide range of applications in either a common-emitter [CA3081] or common-collector [CA3082] configuration*
- *High I_C: 100 mA max.*
- *Low V_{CE} sat (at 50 mA): 0.4 V typ.*

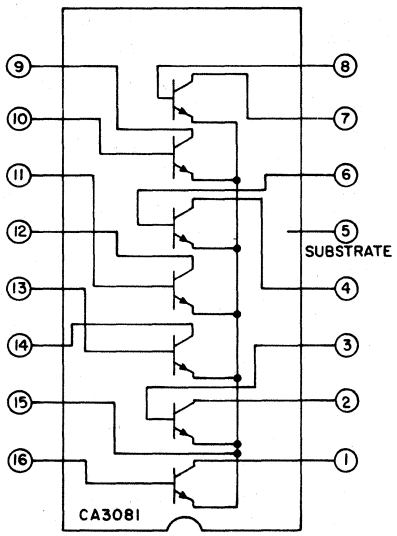
Applications:

- *Drivers for:*
  - *Incandescent display devices [e.g. RCA NUMITRON DR2000 Series and lamps]*
  - *LED [e.g. RCA-40736R GaAs High-Efficiency Emitting Diode]*
  - *Relay control*
  - *Thyristor firing*

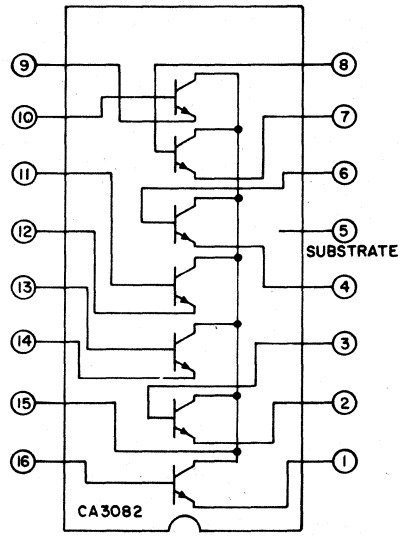
RCA-CA3081 and CA3082 consist of seven high-current (to 100 mA) silicon n-p-n transistors on a common monolithic substrate. The CA3081 is connected in a common-emitter configuration and the CA3082 is connected in a common-collector configuration.

The CA3081 and CA3082 are capable of directly driving seven-segment displays, such as the RCA NUMITRON devices (DR2000 and DR2010), and light-emitting diode (LED) displays. These types are also well-suited for a variety of other drive applications, including relay control and thyristor firing.

The CA3081 and CA3082 are supplied in a 16-lead dual-in-line plastic package, and the CA3081F and CA3082F in a 16-lead dual-in-line frit-seal ceramic package, which includes a separate substrate connection for maximum flexibility in circuit design. Both types are also available in chip form.



(a)
COMMON-EMITTER CONFIGURATION
92CS-17958



(b)
COMMON-COLLECTOR CONFIGURATION
92CS-17957

Fig. 1 — Functional diagrams of types CA3081 and CA3082.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:		
Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to + 150	°C
Lead Temperature (During Soldering):		
At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 seconds max.	265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO})	16	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})*	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

* The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CES}$	I_C = 500 μA, I_E = 0	–	20	60	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 500 μA, I_E = 0, I_B = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	16	24	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_C = 500 μA	–	5	6.9	–	V
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 0.5 V, I_C = 30 mA	–	30	68	–	
		V_{CE} = 0.8 V, I_C = 50 mA	–	40	70	–	
Base-to-Emitter Saturation Voltage	$V_{BE\ sat}$	I_C = 30 mA, I_B = 1 mA	3	–	0.87	1.0	V
Collector-to-Emitter Saturation Voltage: CA3081, CA3082	$V_{CE\ sat}$	I_C = 30 mA, I_B = 1 mA	–	–	0.27	0.5	V
CA3081		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.7	
CA3082		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.8	
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	–	–	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	–	1	μA

CA3081, CA3082 Types

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR OF TYPES CA3081 AND CA3082

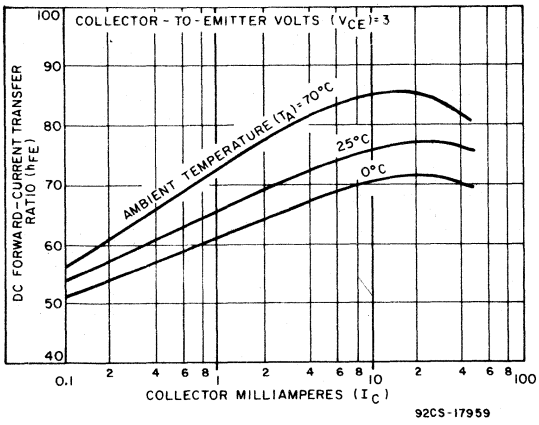


Fig.2—h_{FE} vs. I_C

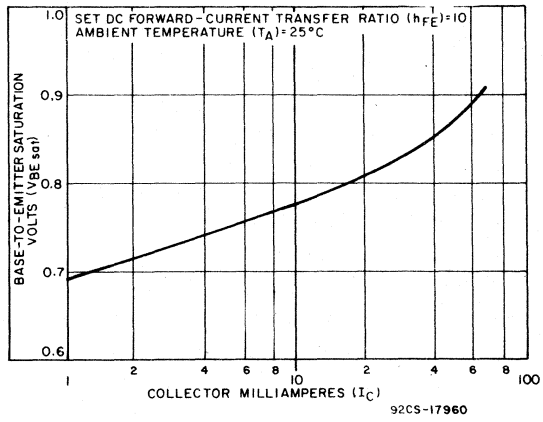


Fig.3—V_{BEsat} vs. I_C

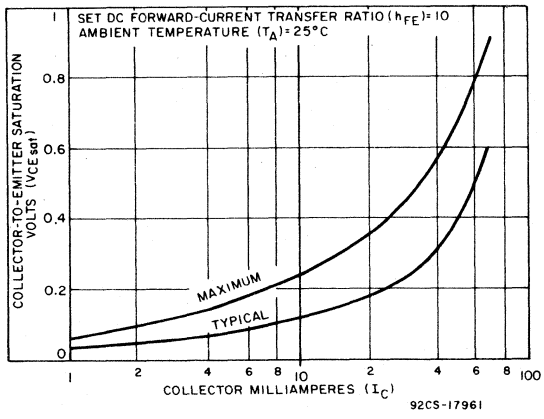


Fig.4—V_{CEsat} vs. I_C at T_A = 25°C.

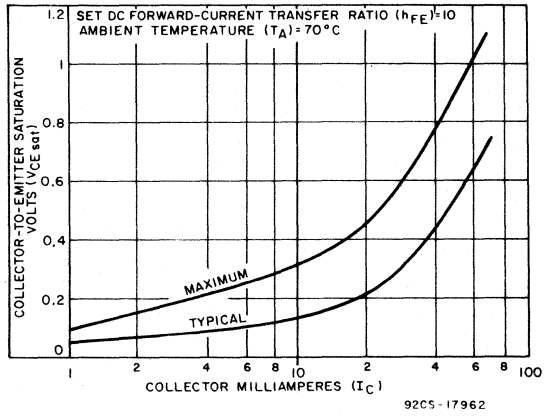


Fig.5—V_{CEsat} vs. I_C at T_A = 70°C.

TYPICAL READ-OUT DRIVER APPLICATIONS

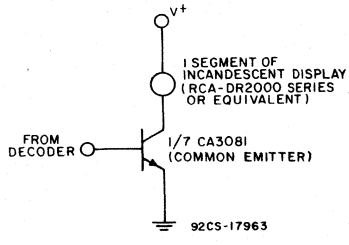
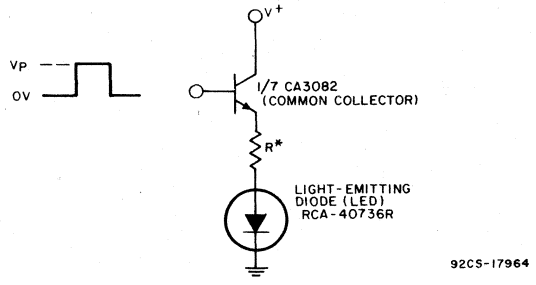


Fig.6—Schematic diagram showing one transistor of the CA3081 driving one segment of an incandescent display.



*THE RESISTANCE FOR R IS DETERMINED BY THE RELATIONSHIP

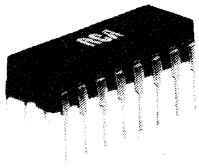
$$R = \frac{V_P - V_{BE} - V_F(LED)}{I\,(LED)}$$

WHERE: V_P = INPUT PULSE VOLTAGE

V_F = FORWARD VOLTAGE DROP ACROSS THE DIODE

$R = 0$ FOR $V_P = V_{BE} + V_F(LED)$

Fig.7—Schematic diagram showing one transistor of the CA3082 driving a light-emitting diode (LED).



16-Lead Dual-In-Line Plastic Package H-1622

BCD-to-Seven-Segment Decoder/Driver

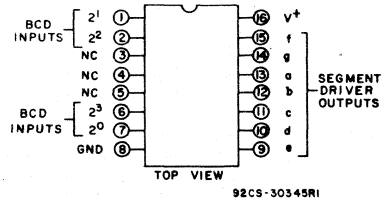
Features:

- *TTL-compatible input logic levels*
- *25-mA [typ.] constant-current segment outputs*
- *Eliminates need for output current-limiting resistors*
- *Pin compatible with other industry standard decoders*
- *Low standby power dissipation – 18 mW (typ.)*

The RCA-CA3161E is a monolithic intergrated circuit that performs the BCD-to-seven-segment decoding function and features constant-current segment drivers. When used with the CA3162E A/D Converter* the CA3161E provides a complete digital readout system with a minimum number of external parts.

The CA3161 is supplied in the 16-lead dual-in-line plastic package (E suffix). The CA3161 is also available in chip form (H suffix).

*The CA3162E is described in RCA data bulletin File No. 1080.



TERMINAL ASSIGNMENT
CA3161E

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (between terminals 1 and 10) ..... +7 V

INPUT VOLTAGE (terminals 1, 2, 6, 7) ..... +5.5 V

OUTPUT VOLTAGE:

Output "Off" ..... +7 V

Output "On" (See note 1) ..... +10 V

DEVICE DISSIPATION:

Up to T_A = +55°C ..... 1 W

Above T_A = +55°C ..... derate linearly at 10.5 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... 0 to +75°C

Storage ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

NOTE 1: This is the maximum output voltage for any single output. The output voltage must be consistent with the maximum dissipation and derating curve for worst-case conditions. Example: All segments "on", 100% duty cycle.

CA3161E

TRUTH TABLE

BINARY STATE	INPUTS				OUTPUTS							DISPLAY
	2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	
0	L	L	L	L	L	L	L	L	L	L	H	0
1	L	L	L	H	H	L	L	H	H	H	H	1
2	L	L	H	L	L	L	H	L	L	H	L	2
3	L	L	H	H	L	L	L	L	H	H	L	3
4	L	H	L	L	H	L	L	H	H	L	L	4
5	L	H	L	H	L	H	L	L	H	L	L	5
6	L	H	H	L	L	H	L	L	L	L	L	6
7	L	H	H	H	L	L	L	H	H	H	H	7
8	H	L	L	L	L	L	L	L	L	L	L	8
9	H	L	L	H	L	L	L	L	H	L	L	9
10	H	L	H	L	H	H	H	H	H	H	L	—
11	H	L	H	H	L	H	H	L	L	L	L	E
12	H	H	L	L	H	L	L	H	L	L	L	H
13	H	H	L	H	H	H	H	L	L	L	H	L
14	H	H	H	L	L	L	H	H	L	L	L	P
15	H	H	H	H	H	H	H	H	H	H	H	BLANK

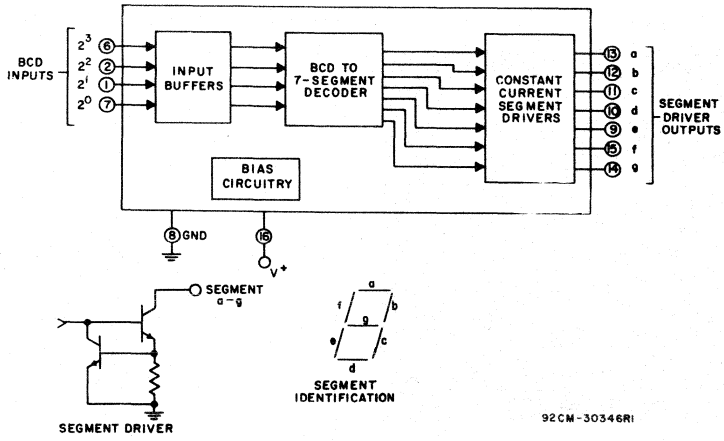
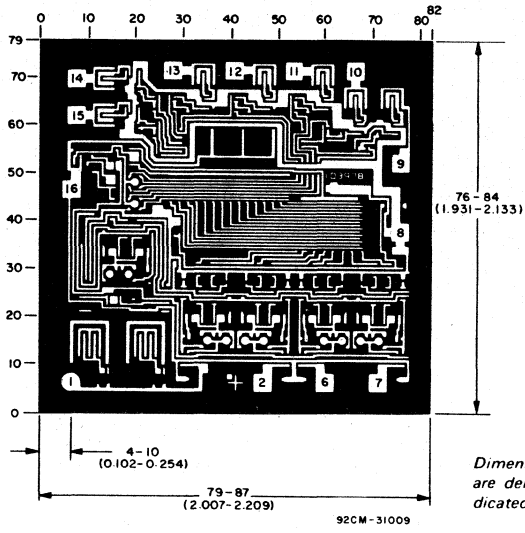


Fig. 1-Functional block diagram of the CA3161E.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTIC		LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Voltage Operating Range, V^+		4.5	5	5.5	V
Supply Current, I^+ (all inputs high)		–	3.5	8	mA
Output Current Low (V_O = 2 V)		18	25	32	mA
Output Current High (V_O = 5.5 V)		–	–	250	μA
Input Voltage High (logic "1" level)		2	–	–	V
Input Voltage Low (logic "0" level)		–	–	0.8	V
Input Current High (logic "1")	2 V	–30	–	–	μA
Input Current Low (logic "0")	0 V	–40	–	–	μA
Propagation Delay Time	t_{PHL}	–	2.6	–	μs
	t_{PLH}	–	1.4	–	

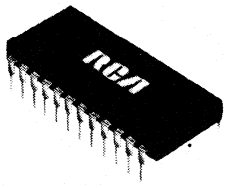
CA3161E



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for the CA3161H.



24-Lead Dual-In-Line Plastic Package

H-1855

2-Digit BCD-to-7-Segment Decoder/Driver

For Common-Anode LED Displays

Features

- *Separate BCD inputs and segment outputs for each digit*
- *Input loading less than 15 μA*
- *I^2L logic with buffered inputs and outputs*
- *Internal input overrange protection circuit*
- *5-V supply operation*
- *Internal biasing circuits*
- *Output drive capability of 25 mA per segment*
- *Open collector outputs drive indicators directly*

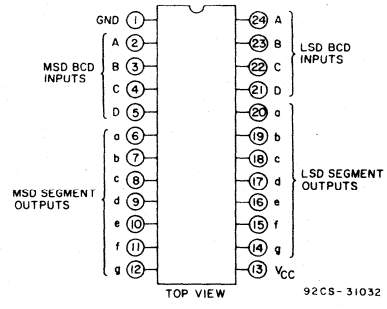
The RCA-CA3168E• is a monolithic integrated circuit intended for 2-digit display such as "numbers" for TV and "CB" channel selection, and other 0-99 numerical or counting for consumer or industrial indicator applications. It consists of two independent BCD-to-7-segment decoder/drivers. Two sets of BCD inputs are buffered with p-n-p differential amplifier stages internally referenced to 1.7 V. Each of the eight input terminals draws less than 15 μA and is provided with an internal protection circuit.

Decoding is accomplished with I^2L ROM's. The fourteen output terminals are buffered with Darlington pairs driving common-emitter output transistors. Each output is capable of sinking 25 mA for an LED common-anode display device. The supply-voltage range (V_{CC}) is intended to be 4.5 V to 6 V. The output voltage (V_O) must not exceed 12 V, which provides for a wide range of common-anode voltage sources.

The CA3168E is supplied in the 24-lead dual-in-line plastic package.

•Formerly RCA Dev. Type No. TA10337

CA3168E
TERMINAL ASSIGNMENT



MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY-VOLTAGE, V_{CC} ..... 6 V
INPUT-VOLTAGE (MIN./MAX.) ..... $-0.3/V_{CC}$ V
INPUT CURRENT (PROTECTION CIRCUIT) ..... ±10 mA
OUTPUT VOLTAGE, V_O ..... 12 V
OUTPUT SEGMENT CURRENT, $I_{DISPLAY}$ ..... 25 mA
AMBIENT TEMPERATURE RANGE:
  Operating ..... 0 to +70°C
  Storage ..... -55 to +150°C
POWER DISSIPATION:
  Up to +70°C ..... 400 mW
  Above +70°C ..... derate linearly at 8.7 mW/°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for
  10 seconds max. ..... +265°C

CA3168E

TYPICAL ELECTRICAL CHARACTERISTICS at V_{CC} = 5 V, V_1 = GND, $V_{DISP.}$ = 12 V, and T_A = 25°C, See Fig. 2
Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Input Voltage High, V_{IH}		2.4	5	V_{CC}	V
Input Voltage Low, V_{IL}		0	–	0.6	V
Input Current High, I_{IH}	All BCD Inputs = 5 V	–	–	15	μA
Input Current Low, I_{IL}	All BCD inputs = 0 V	−10	–	–	μA
On-State Output Voltage, V_{OL}	$I_{O(Sink)}$ = 25 mA	–	–	1	V
Off-State Output Current, I_{OH}		–	5	50	μA
Power Supply Drain Current, I_{CC}	V_{CC} = 6 V	–	17	25	mA
Input Capacitance, C_I		–	5	–	pF

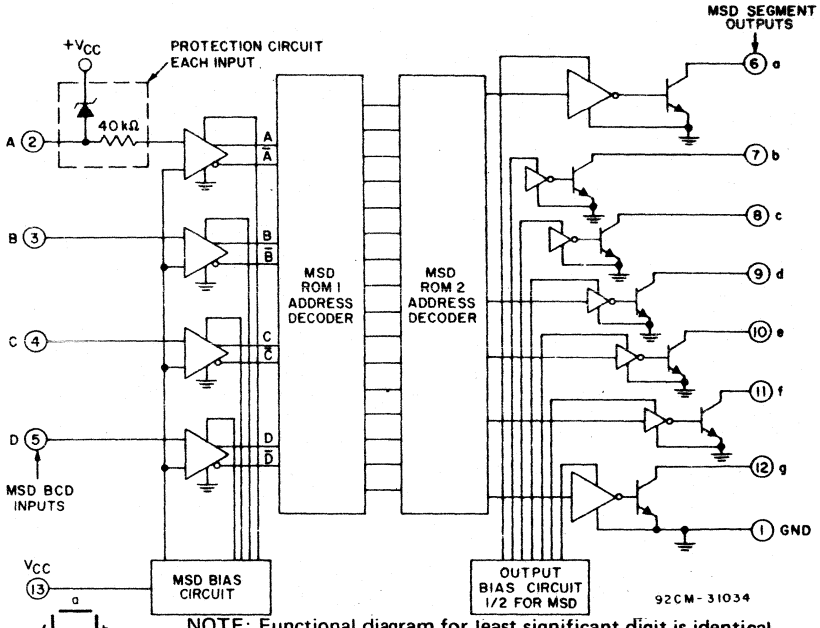
TRUTH TABLES

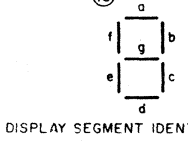
Most Significant Digit (MSD)

INPUTS	OUTPUTS							DISPLAY
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	0	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	0	1	0	0	9
1	0	1	0	0	1	1	0	0	0	1	C
1	0	1	1	0	0	0	1	0	0	0	A
1	1	0	0	0	0	1	1	0	0	0	P
1	1	0	1	0	1	1	0	0	0	0	E
1	1	1	0	1	1	1	1	1	1	0	–
1	1	1	1	1	1	1	1	1	1	1	BLANK

Least Significant Digit (LSD)

INPUTS	OUTPUTS							DISPLAY
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	0	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	0	1	0	0	9
1	0	1	0	1	0	0	1	0	0	0	H
1	0	1	1	1	0	0	0	0	1	1	J
1	1	0	0	1	1	1	0	0	0	1	L
1	1	0	1	0	1	1	1	0	0	0	F
1	1	1	0	1	1	1	1	1	1	0	–
1	1	1	1	1	1	1	1	1	1	1	BLANK

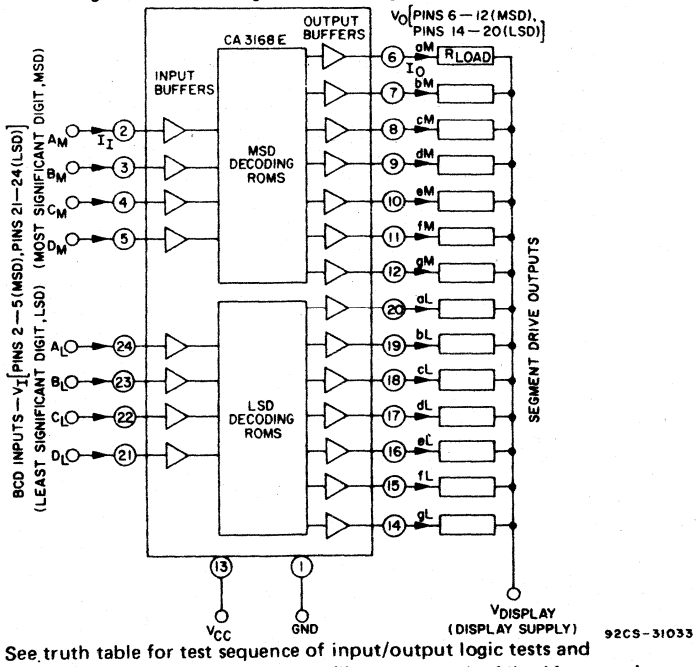




DISPLAY SEGMENT IDENTIFICATION

NOTE: Functional diagram for least significant digit is identical to functional diagram used for MSD with the exception of Terminal Assignments (see Terminal Assignment diagram). A separate LSD Bias circuit, and ½ of the Output Bias Circuit is used for LSD.

Fig. 1 - Functional diagram for Most Significant Digit (MSD).



NOTE: See truth table for test sequence of input/output logic tests and

Minimum $R_{LOAD} = \frac{V_{DISPLAY} - V_{OL}}{\text{Max. } I_{DISPLAY}}$ **for each of the 14 segment**

drive output terminals. (LED is not used in test circuit)

Fig. 2 - Test circuit.

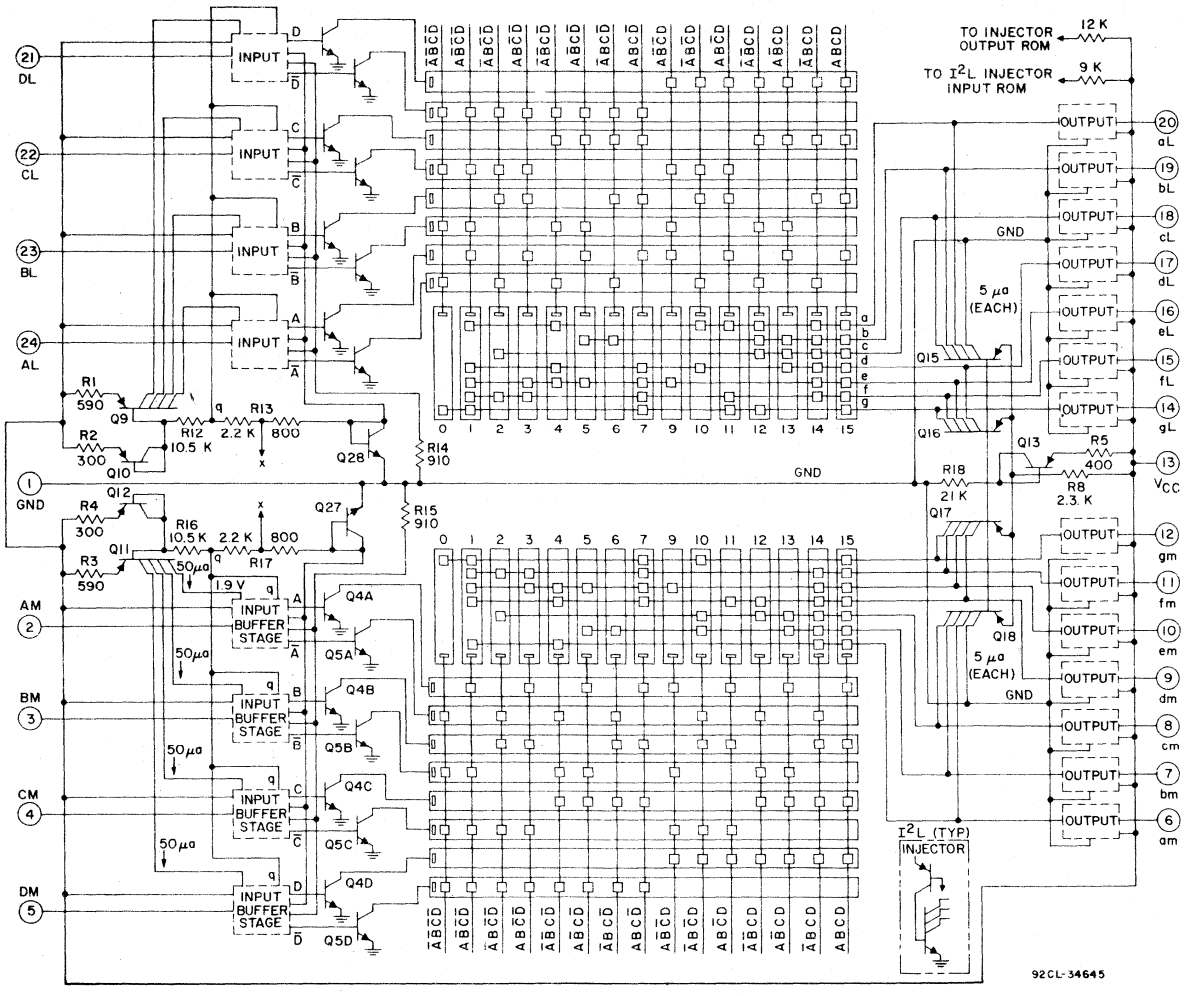


Fig. 3 - Schematic diagram of CA3168E.

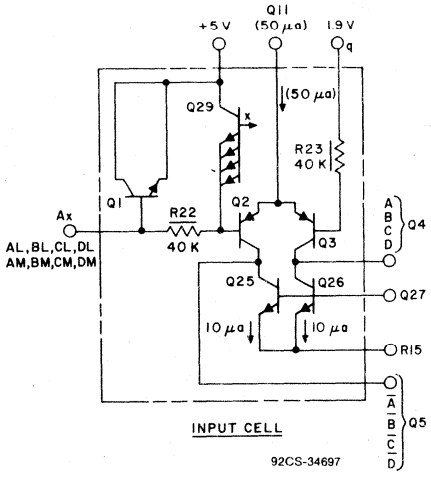


Fig. 4 - Schematic diagram of CA3168E input cell.

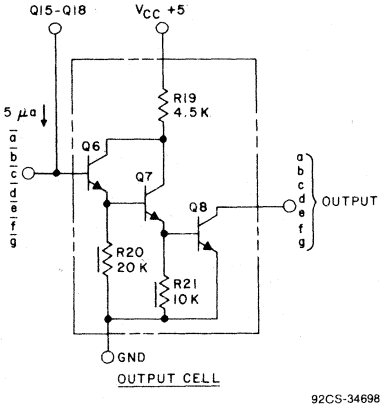


Fig. 5 - Schematic diagram of CA3168E output cell.

CA3207E, CA3208E

H-1917

22-Lead Dual-In-Line Plastic Package (E)

BiMOS Sequencer Driver and Segment Latch-Driver for Vacuum Fluorescent Displays

Features:
- *Serial input, parallel output*
- *Total of 14 outputs*
- *CMOS and T^2L compatible inputs*
- *Low-power CMOS Logic–Bipolar high-voltage output BiMOS process*
- *Use with vacuum fluorescent display*
- *Will operate in an output voltage range of 35 V to 55 V*

Sequencer Driver (CA3207E)
- *Sequentially turns on 1 of 14 characters (or 2 of 28 when used with 2 CA3208E's)*
- *Signal dimming through Gates 1 or 2*

Latch Driver (CA3208E)
- *Drives any combination of 14 outputs selected by DATA input*
- *Two or more devices may be interconnected by means of the CE and $\overline{CE}$ inputs to drive more than 14 characters*

The RCA-CA3207E and CA3208E★, sequence-driver and segment latch-driver, respectively, are used in combination to drive vacuum fluorescent display devices of up to 14 segments with up to 14 characters of display. The CA3207E selects the digit or character to be displayed in sequence and the CA3208E turns on the required number of segments of the character selected.

Each sequencer-driver will sequentially activate 14 characters. The sequencer-driver clock line may be used to drive the cross-coupled $\overline{CE}$ and CE inputs of 2 segment-latch drivers to provide for the display of up to 28 characters (see Fig. 12). The logic portion of both circuits use CMOS technology operating at 5 volts. The output drivers use bipolar technology and operate at supply voltages up to 55 volts. The CA3207E will source 40-mA per character and the CA3208E will source 7.5-mA per segment.

Both types are supplied in the 22-lead dual-in-line plastic package (E suffix), and they are also available in chip form (H suffix).

★Formerly Dev. Type No. TA10563 and TA10564, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:

V_{CC}, Pin 3 to GND, Pin 10	55 V
V_{DD}, Pin 4 to GND, Pin 10	6 V

DEVICE DISSIPATION:

Up to T_A=+85°C	750 mW
Above T_A=+85°C	13 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating	-40 to +85°C
Storage	-55 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	265°C

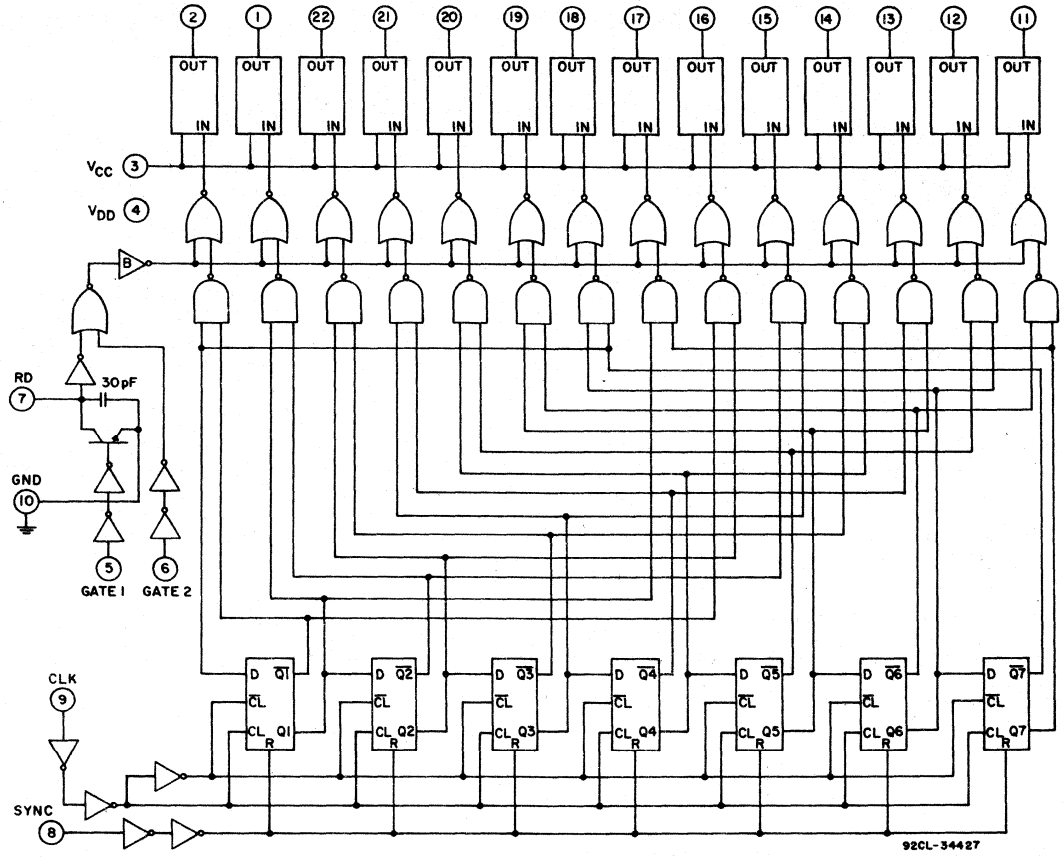
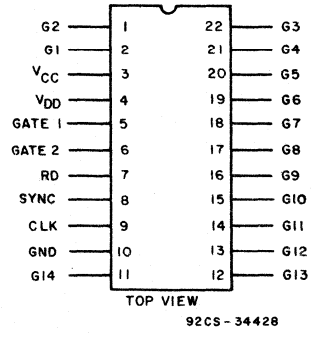


Fig. 1 - Sequencer-driver (CA3207E) logic diagram.



TERMINAL ASSIGNMENT
CA3207E

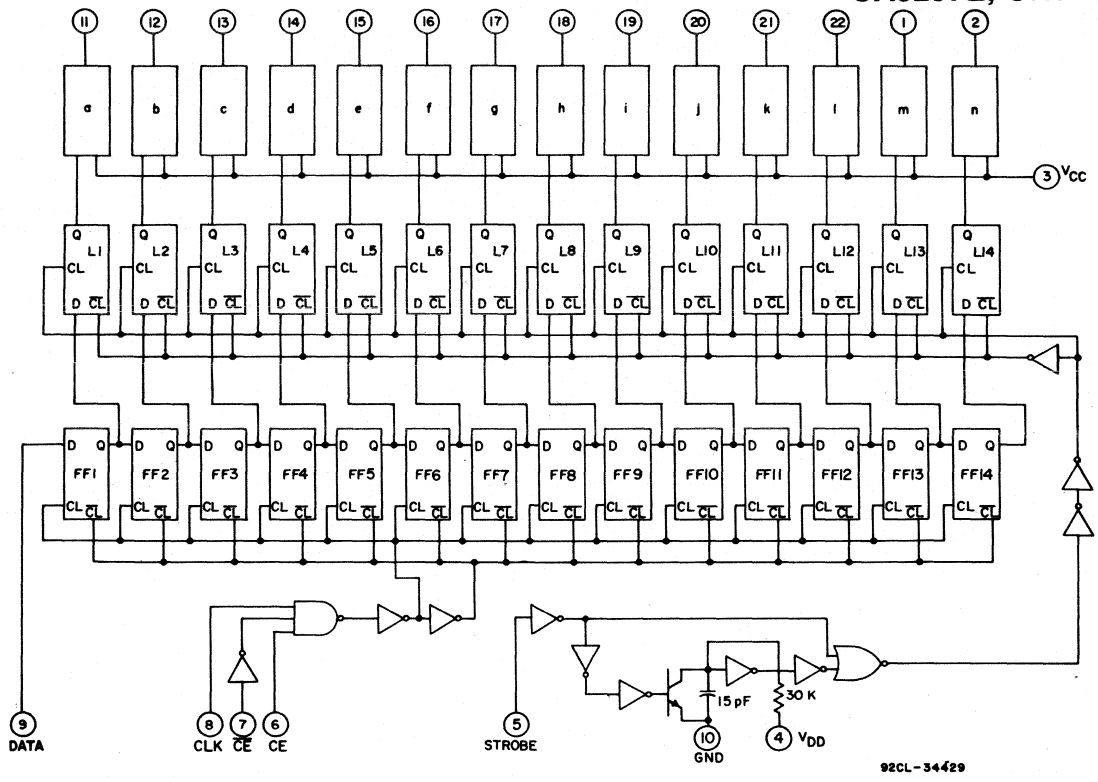
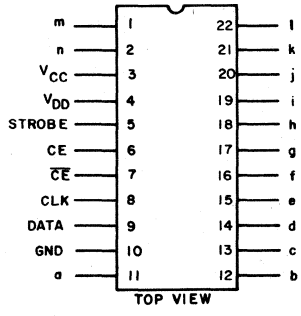


Fig. 2 - Segment-latch driver (CA3208E) logic diagram.

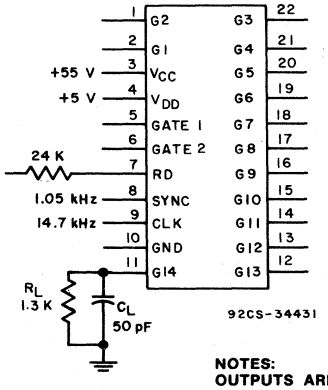


TERMINAL ASSIGNMENT
CA3208E

CA3207E, CA3208E

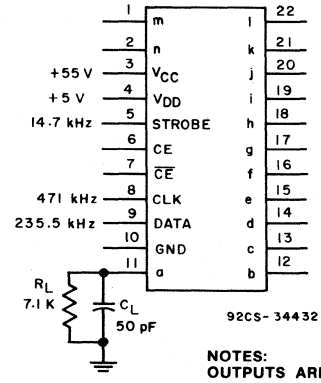
STATIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=+55 V, V_{DD}=+5 V, C_L=50 pF, See Fig. 3 and Fig. 4.

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			CA3207E		CA3208E		
			Min.	Max.	Min.	Max.	
V_{CC} Supply Current	I_{CC}	No outputs "ON"	—	10	—	—	mA
		Half outputs HIGH "ON"	—	—	—	65	
V_{DD} Supply Current	I_{DD}	All inputs HIGH	—	1	—	—	mA
		All inputs LOW	—	—	—	800	μA
		All inputs HIGH	—	—	—	1	
Input Current, Low-Level	I_{IL}	V_{IN}=0 V	—	1	—	1	μA
Input Current, High-Level	I_{IH}	V_{IN}=5 V	—	1	—	1	
Output Voltage, Low-Level	V_{OL}	R_L=1.3K	—	1	—	—	V
		R_L=7.1K	—	—	—	1	
Output Voltage, High-Level	V_{OH}	I_{OH}=40 mA	53	—	—	—	
		I_{OH}=7.5 mA	—	—	53	—	
Input Low Voltage	V_{IL}		—	1.5	—	1.5	V
Input High Voltage	V_{IH}		3.5	—	3.5	—	



NOTES:
OUTPUTS ARE PINS 1, 2 AND 11 THROUGH 22.
OUTPUT LOADS ARE R_L (1.3 K) AND C_L (50 pF) WHICH RESULTS IN A 40-mA LOAD CURRENT.
INPUT VOLTAGE LEVELS ARE 0 V and 5 V.

Fig. 3 - Sequencer-driver (CA3207E) test circuit.



NOTES:
OUTPUTS ARE PINS 1, 2 AND 11 THROUGH 22.
OUTPUT LOADS ARE R_L (7.1 K) AND C_L (50 pF) WHICH RESULTS IN A 7.5-mA LOAD CURRENT.
INPUT VOLTAGE LEVELS ARE 0 V AND 5 V.

Fig. 4 - Segment-latch driver (CA3208E) test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=+55 V, V_{DD}=+5 V, C_L=50 pF, R_L=1.3K

CHARACTERISTIC		LIMITS CA3207E Min.	LIMITS CA3207E Max.	UNITS
Sequencer-Driver, See Fig. 5				
Sync Pulse Width	t_{SW}	2	—	μs
Time Delay Gate 1:				
Input-to-Output Inhibit	t_{GI}	—	1.5	μs
Input-to-Output Enable	t_{GE}	—	2.3	μs
Lead Time Sync to Gate	t_{SG}	0.5	—	μs
Lead Time Clock to Gate	t_{CG}	0.5	—	μs
Clock Frequency	f_{CL}	—	14	kHz

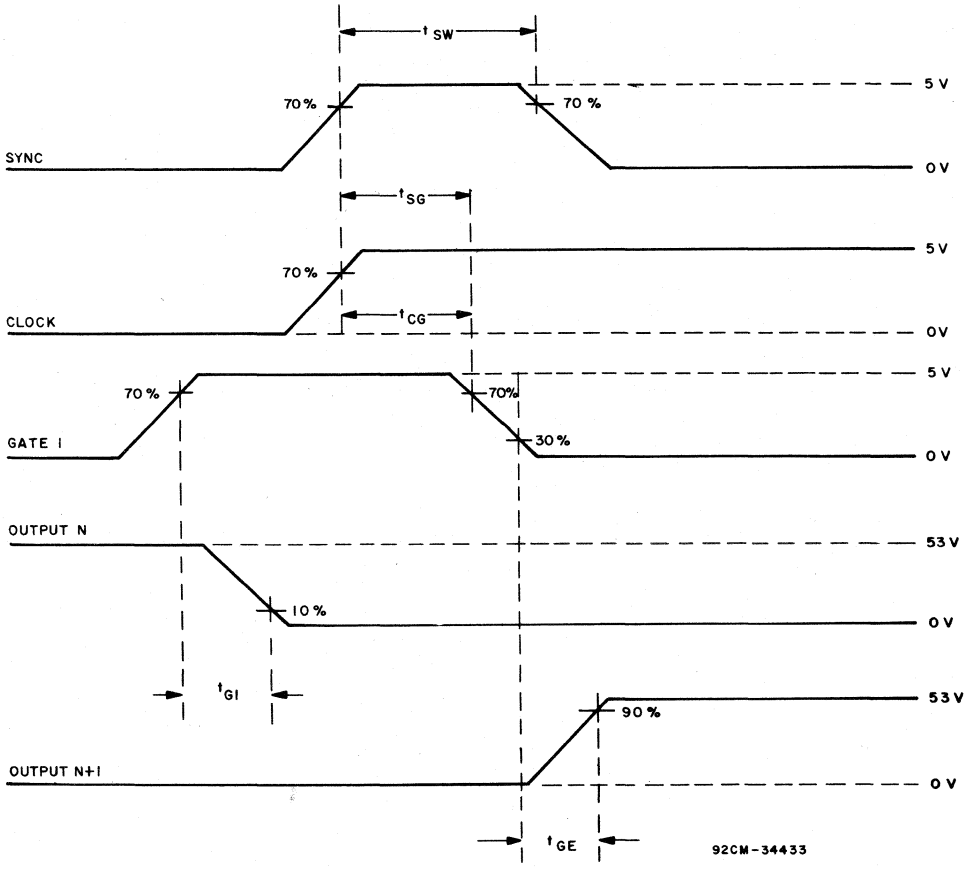


Fig. 5 - Sequencer-driver (CA3207E) timing waveforms.

CA3207E, CA3208E

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=+55 V, V_{DD}=+5 V, C_L= 50 pF, R_L=7.1 K

CHARACTERISTIC		LIMITS CA3208E Min.	LIMITS CA3208E Max.	UNITS
Segment-Latch Driver, See Fig. 6				
Time Delay:				
Strobe to Output	t_{PLH}	0.4	1.8	
Strobe to Output	t_{PHL}	—	2.6	μs
CE or $\overline{CE}$ to Clock	t_{CE}	0.8	—	
Input Data Set-Up Time	t_{SU}	0.5	—	μs
Input Data Hold Time	t_H	0.5	—	
Clock Frequency	f_{CL}	—	448	kHz
Data Frequency	f_D	—	224	

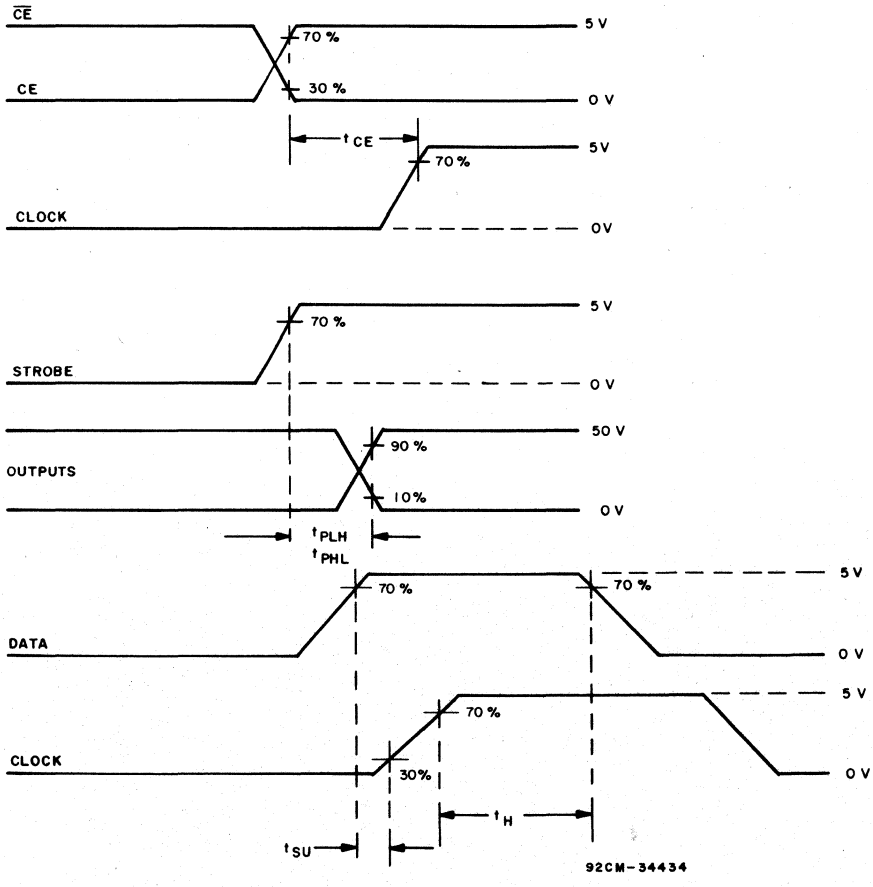


Fig. 6 - Segment-latch driver (CA3208E) timing waveforms.

Circuit Descriptions

Sequencer-Driver (CA3207E)

The CA3207E circuit consists of a 7-stage Johnson counter, which is reset by the positive transition of the sync pulse and which is clocked on the positive transitions of the clock pulse. The outputs of the counter are decoded to turn on one output driver at a time in sequence, for the period of one clock pulse (normally 70 μs). The 14 output drivers are each capable of sourcing 40 mA of current and in a typical application will be connected to the grids of a vacuum fluorescent display, thereby performing a digit select function on a display of up to 14 characters. All outputs are set to zero by the application of a positive "1" level to either of the gate terminals, 5 and 6. The action of the 7-stage counter is unaffected by the presence of inhibit levels on the gate terminals. The gate terminals can be used for a controlled power down or for chopping where display dimmer is desired. The only difference between the two terminals is that gate 1, pin 5, has a delayed falling edge, which delays the release of the output drivers for a time determined by the value of the resistor connected between pin 7 and V_{DD}.

Segment-Latch Driver (CA3208E)

This circuit consists of a 14-bit shift register accepting serial data at pin 9 at a typical rate of 224 kHz and being clocked on the rising edge of the 448-kHz clock signal.

The leading edge of a 14-kHz strobe signal generates an internal strobe pulse through the one shot, which shifts the data, in parallel, from the shift register to the output latches, which in turn set the output drivers to the corresponding state. There are 14 output drivers, each capable of driving 7.5-mA at 55 volts, simultaneously. The drivers are normally connected to the anodes or segments of the vacuum fluorescent display. In a multi-character display, all corresponding segments in each character would be linked together. Activation of a particular character is made by the CA3207E Sequencer-Driver turning on the appropriate output and raising the grid of the display to a positive value.

Clock Enable (CE) and Clock Enable Not ($\overline{CE}$) pins are available for use in system applications. The first enables the chip with a logic level "1" and the second with a logic level"0".

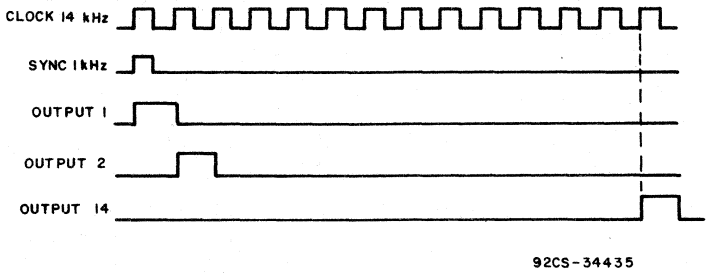


Fig. 7 - Sequencer driver (CA3207E) timing waveforms.

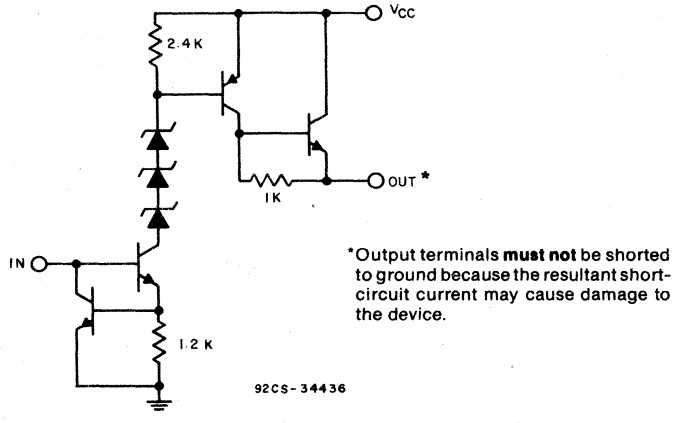


Fig. 8 - Sequencer driver (CA3207E) output circuit.

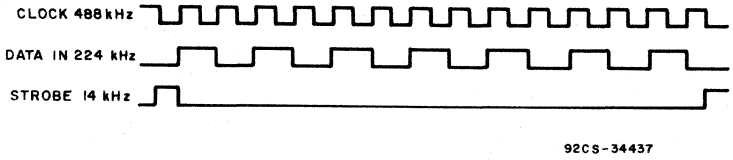
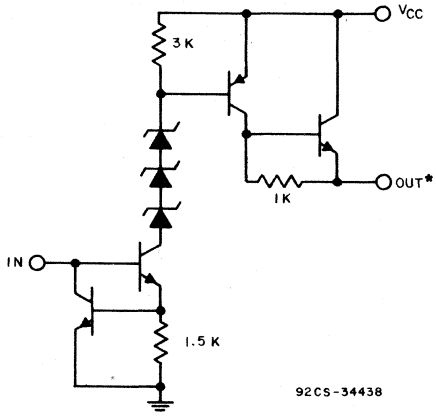


Fig. 9 - Segment-latch driver (CA3208E) timing waveforms.



*Output terminals **must not** be shorted to ground because the resultant short-circuit current may cause damage to the device.

Fig. 10 - Segment latch-driver (CA3208E) output circuit.

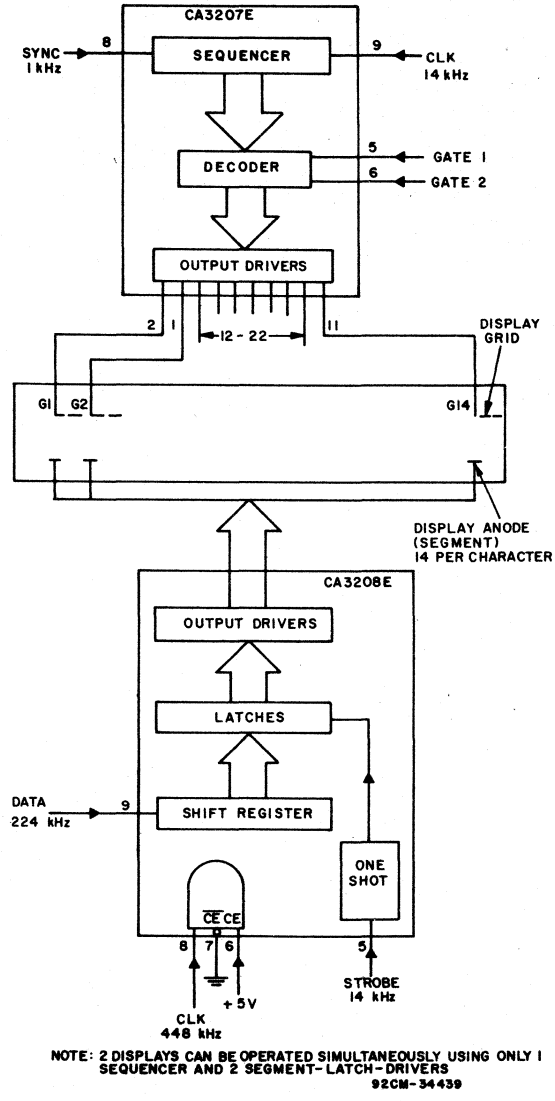


Fig. 11 - Typical systems application of the CA3207E and CA3208E display circuits.

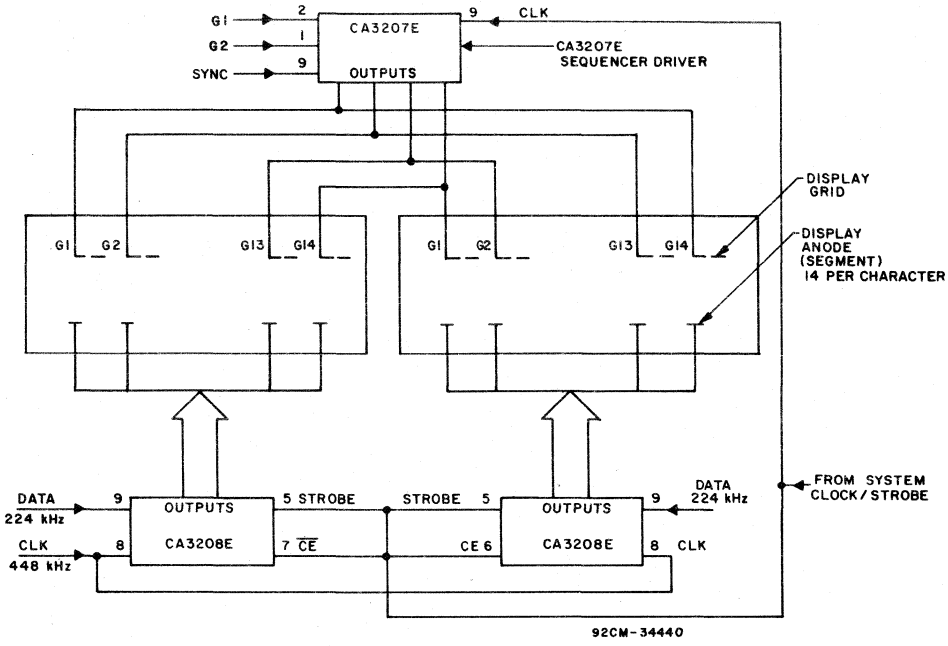
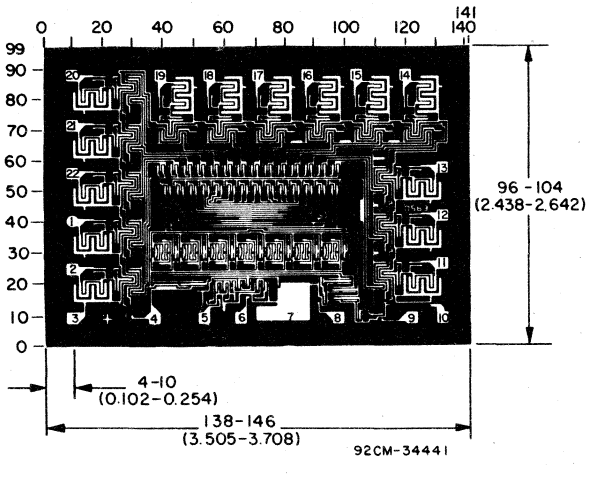
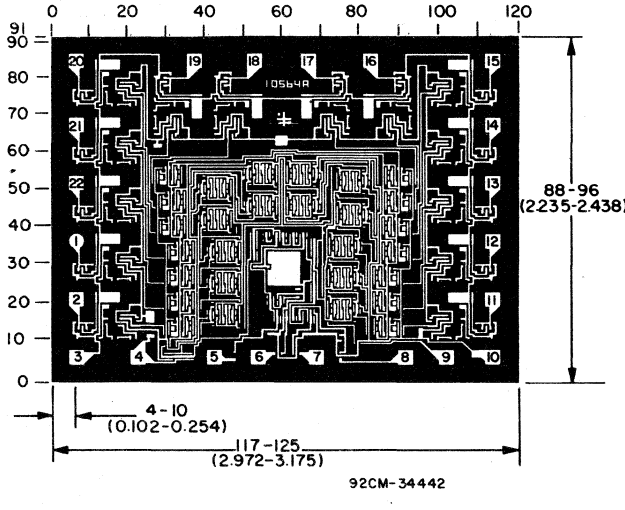


Fig. 12 - Typical systems application of the CA3207E and 2 CA3208E circuits for a total 28-character display.



Dimensions and pad layout for the CA3207H.



Dimensions and pad layout for the CA3208H.

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Arrays
Technical Data

Amplifier/ Diode

Transistor

5

ΔCMOS types

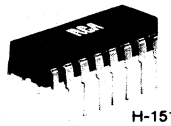
CA3026, CA3054

CA3026

H-1463

12-Lead TO-5

CA3054



H-1517

14-Lead Dual-In-Line Plastic Package

Transistor Array - Dual Independent Differential Amplifiers

For Low Power Applications at Frequencies from DC to 120 MHz

Features

- *Two differential amplifiers on a common substrate*
- *Independently accessible inputs and outputs*
- *Maximum input offset voltage - ± 5 mV*
- *Full military temperature-range capability - −55°C to +125°C*
- *Limited temperature range - 0°C to 85°C for CA3054*

The CA3026 and CA3054 each consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six n-p-n transistors which comprise the amplifiers are general-purpose devices which exhibit low 1/f noise and a value of f_T in excess of 300 MHz. These features make the CA3026 and CA3054 useful from dc to 120 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3026 and CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3026 is supplied in a hermetic 12-lead TO-5-style package and is rated for full military operating-temperature range of −55°C to +125°C.

The CA3054 is supplied in a 14-lead plastic dual-in-line package with a limited temperature range. The availability of extra terminals allows the introduction of an independent substrate connection for maximum flexibility.

Applications

- *Dual sense amplifiers*
- *Dual Schmitt triggers*
- *Multifunction combinations - RF/Mixer/Oscillator; Converter/IF*
- *IF amplifiers (differential and/or cascode)*
- *Product detectors*
- *Doubly balanced modulators and demodulators*
- *Balanced quadrature detectors*
- *Cascade limiters*
- *Synchronous detectors*
- *Pairs of balanced mixers*
- *Synthesizer mixers*
- *Balanced (push-pull) cascode amplifiers*

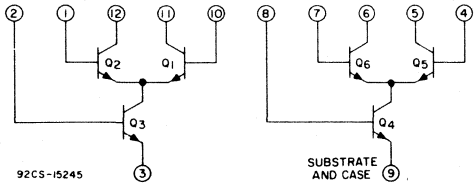


Fig.1a - Schematic Diagram for CA3026.

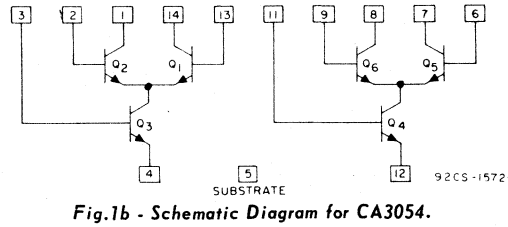


Fig.1b - Schematic Diagram for CA3054.

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device. See Maximum Voltage Ratings chart.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C

Power Dissipation, P:	CA3026	CA3054	
Any one transistor	300	300	mW
Total package	600	750	mW
For T_A > 55°C	Derate at 5	6.67	mW/°C
Temperature Range:			
Operating	-55 to + 125	-40 to +85	°C
Storage	-65 to + 150	-65 to +150	°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3026 and CA3054 is isolated from the substrate by an integral diode. *The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.*

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 1† and horizontal terminal 3† is +15 to -5 volts.

† For CA3026; corresponding terminals for CA3054 are vertical terminal 2 and horizontal terminal 4.

CA3054 TERMINAL No. →		13	14	1	2	3	4	6	7	8	9	11	12	5
↓	CA3026 → TERMINAL No. ↓	10	11	12	1	2	3	4	5	6	7	8	Note 1 9	Note 1 9
13	10		0 -20	*	+5 -5	*	+15 -5	*	*	*	*	*	*	*
14	11			*	*	*	+20 0	*	*	*	*	*	*	+20 0
1	12				+20 0	*	+20 0	*	*	*	*	*	*	+20 0
2	1					*	+15 -5	*	*	*	*	*	*	*
3	2						+1 -5	*	*	*	*	*	*	*
4	3							*	*	*	*	*	*	*
6	4								0 -20	*	+5 -5	*	+15 -5	*
7	5									*	*	*	*	+20 0
8	6										+20 0	*	*	+20 0
9	7											*	+15 -5	*
11	8												+1 -5	*
12	9													*
5	9													Ref Sub-strate

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Note 1: In the CA3026 terminal No.9 is connected to the emitter of Q_4, the reference substrate, and the case; therefore, the case should not be grounded. Two terminal 9 columns (CA3026) appear in the voltage rating chart because it is a composite chart for both the CA3026 and the CA3054. Wherever an asterisk is shown in one column 9 and a rating is shown in the other column 9, the asterisk should be ignored.

Maximum Current Ratings

CA3054 TERMINAL No.●	CA3026 TERMINAL No.	I_{IN} mA	I_{OUT} mA
13	10	5	0.1
14	11	50	0.1
1	12	50	0.1
2	1	5	0.1
3	2	5	0.1
4	3	0.1	-50
6	4	5	0.1
7	5	50	0.1
8	6	50	0.1
9	7	5	0.1
11	8	5	0.1
12	9	0.1	50

● Terminal No.10 of CA3054 is not used

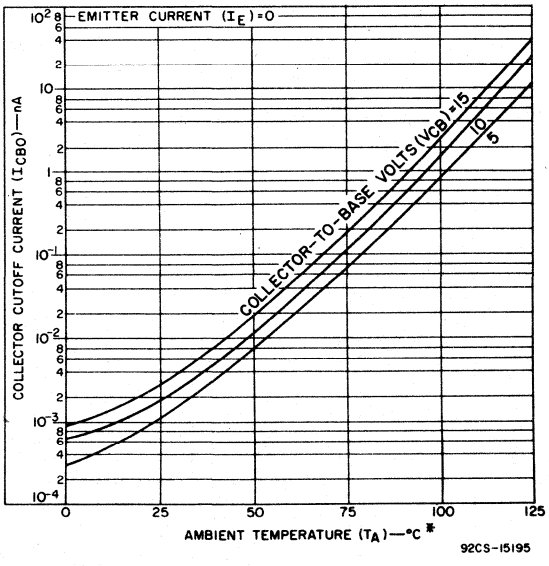
CA3026, CA3054

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	CA3026 CA3054 LIMITS			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC CHARACTERISTICS								
For Each Differential Amplifier								
Input Offset Voltage	V_{IO}	V_{CB} = 3 V $I_{E(Q3)} = I_{E(Q4)}$ = 2 mA	-	-	0.45	5	mV	6
Input Offset Current	I_{IO}		-	-	0.3	2	μA	7
Input Bias Current	I_I		-	-	10	24	μA	3
Quiescent Operating Current Ratio	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$ or $\frac{I_{C(Q5)}}{I_{C(Q6)}}$		-	-	0.98 to 1.02	-	-	3
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		-	-	1.1	-	μV/°C	5
For Each Transistor								
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CB} = 3 V, I_C = 50 μA	-	-	0.630	0.700	V	6
		I_C = 1 mA	-	-	0.715	0.800		
		I_C = 3 mA	-	-	0.750	0.850		
		I_C = 10 mA	-	-	0.800	0.900		
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3 V, I_C = 1 mA	-	-	-1.9	-	μV/°C	4
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	-	0.002	100	nA	2
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	-	15	24	-	V	-
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	-	20	60	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	-	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	-	5	7	-	V	-
DYNAMIC CHARACTERISTICS								
Common-Mode Rejection Ratio For Each Amplifier	CMR	V_{CC} = 12 V V_{EE} = -6 V V_X = -3.3 V f = 1 kHz	8a	-	100	-	dB	8b
AGC Range, One Stage	AGC		9a	-	75	-	dB	9b
Voltage Gain, Single Stage Double-Ended Output	A		9a	-	32	-	dB	9b
AGC Range, Two Stage	AGC		10a	-	105	-	dB	10b
Voltage Gain, Two Stage Double-Ended Output	A		10a	-	60	-	dB	10b
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (For Single Transistor)								
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	-	110	-	-	11
Short-Circuit Input Impedance	h_{ie}		-	-	3.5	-	kΩ	11
Open-Circuit Output Impedance	h_{oe}		-	-	15.6	-	μmho	11
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	-	1.8×10^{-4}	-	-	11

DYNAMIC CHARACTERISTICS CONT'D.								
1/f Noise Figure (For Single Transistor)	NF	f = 1 kHz, V_{CE} = 3 V	-	-	3.25	-	dB	-
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 3 V, I_C = 3 mA	-	-	550	-	MHz	12
Admittance Characteristics; Differential Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Each Collector $I_C \approx$ 1.25 mA f = 1 MHz	-	-	-20+j0	-	mmho	13a
Input Admittance	y_{11}		-	-	0.22+j0.1	-	mmho	13b
Output Admittance	y_{22}		-	-	0.01+j0	-	mmho	13c
Reverse Transfer Admittance	y_{12}		-	-	-0.003 +j0	-	mmho	13d
Admittance Characteristics; Cascode Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Total Stage $I_C \approx$ 2.5 mA f = 1 MHz	-	-	68-j0	-	mmho	14a
Input Admittance	y_{11}		-	-	0.55+j0	-	mmho	14b
Output Admittance	y_{22}		-	-	0+j0.02	-	mmho	14c
Reverse Transfer Admittance	y_{12}		-	-	0.004-j0.005	-	μmho	14d
Noise Figure	NF	f = 100 MHz	-	-	8	-	dB	-

TYPICAL STATIC CHARACTERISTICS



* For CA3054: use data from 0°C to 85°C only

Fig.2 - Collector-to-base cutoff current vs ambient temperature for each transistor.

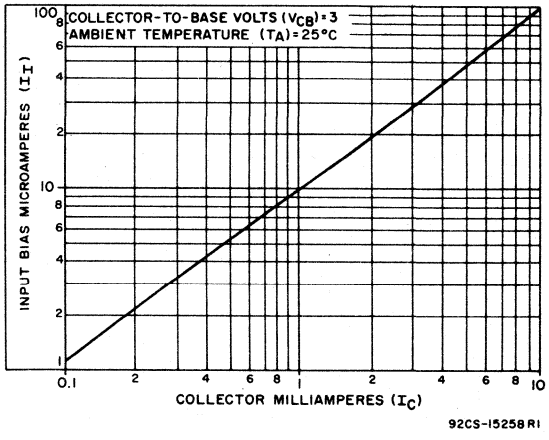


Fig.3 - Input bias current characteristic vs collector current for each transistor.

TYPICAL STATIC CHARACTERISTICS

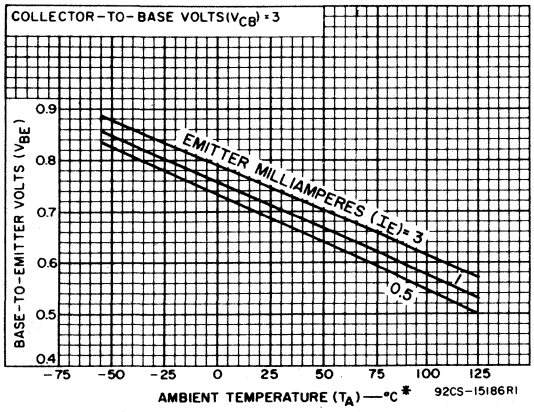


Fig.4 - Base-to-emitter voltage characteristic for each transistor vs ambient temperature.

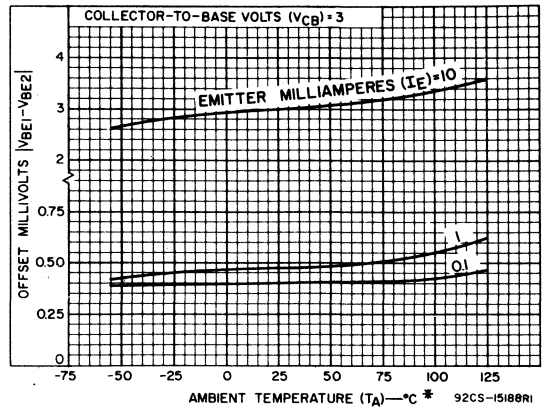


Fig.5 - Offset voltage characteristic vs ambient temperature for differential pairs.

* For CA3054: use data from 0°C to 85°C only

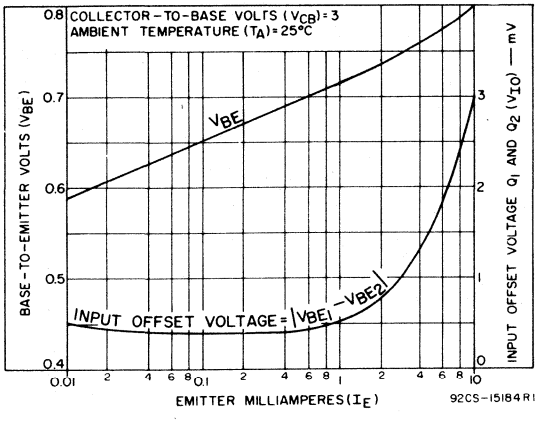


Fig.6 - Static base-to-emitter voltage characteristic and input offset voltage for differential pairs vs emitter current.

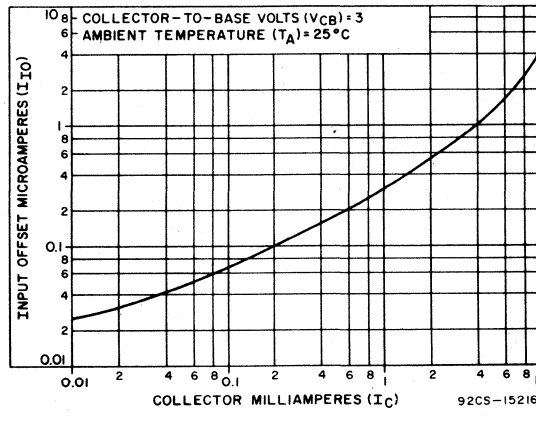
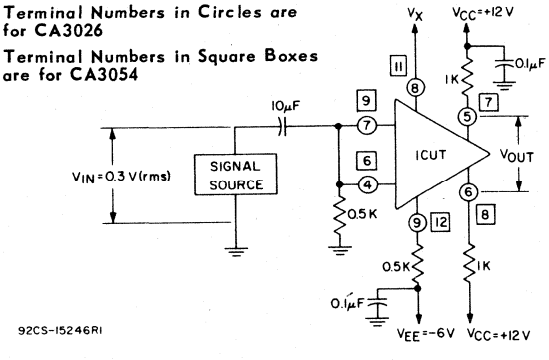


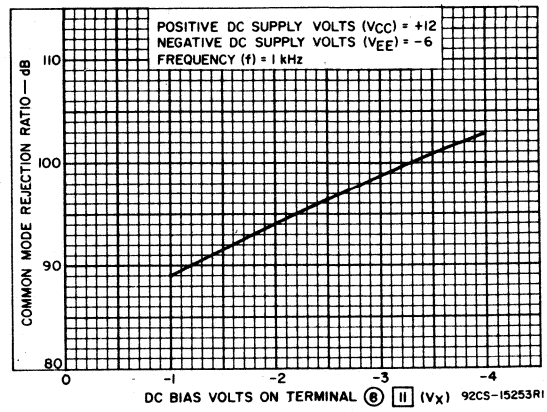
Fig.7 - Input offset current for matched differential pairs vs collector current.

TYPICAL DYNAMIC CHARACTERISTICS

COMMON MODE REJECTION RATIO



(a) Test setup

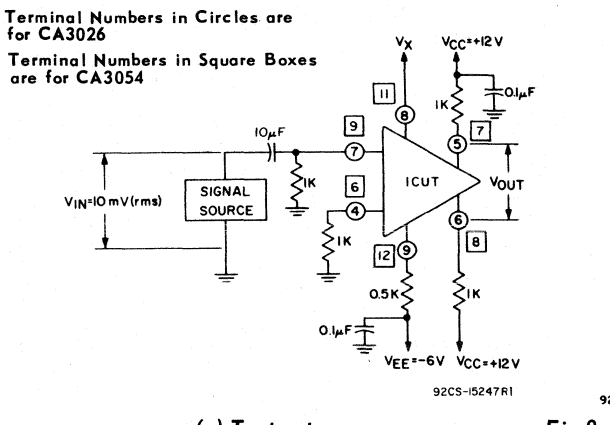


(b) Characteristic

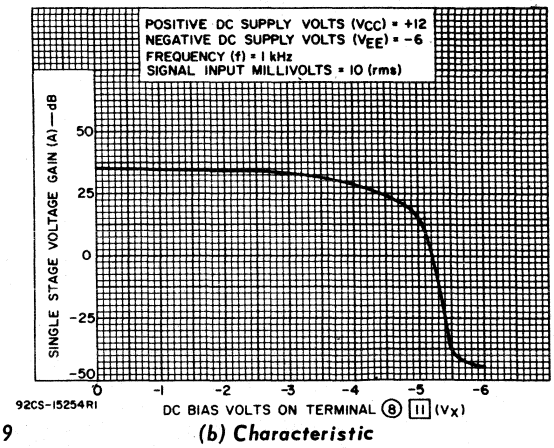
Fig.8

TYPICAL DYNAMIC CHARACTERISTICS (cont'd)

SINGLE-STAGE VOLTAGE GAIN



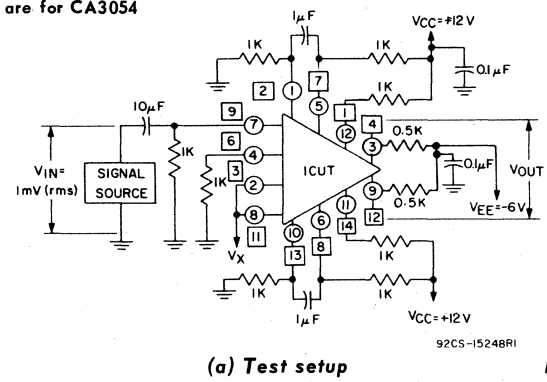
(a) Test setup



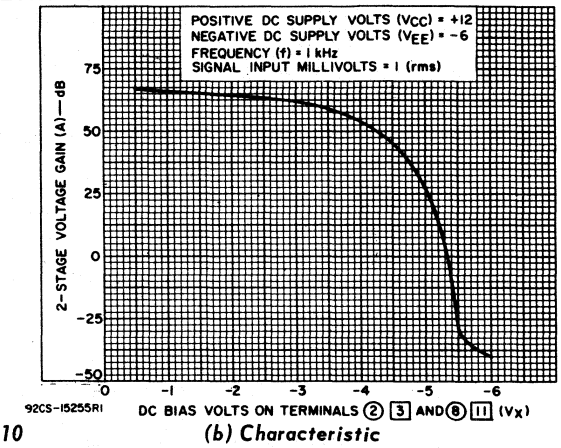
(b) Characteristic

Fig.9

TWO-STAGE VOLTAGE GAIN



(a) Test setup



(b) Characteristic

Fig.10

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

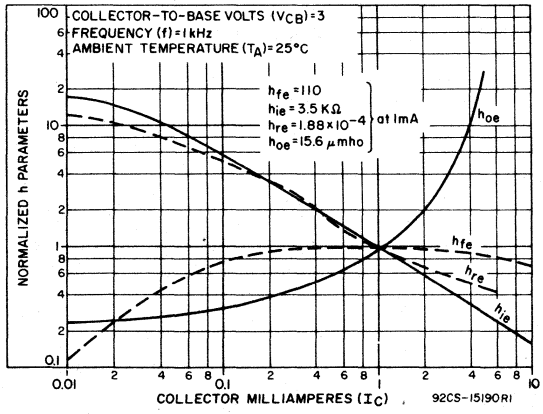


Fig.11 - Forward current-transfer ratio (h_{fe}), short-circuit input impedance (h_{ie}), open-circuit output impedance (h_{oe}), and open-circuit reverse voltage-transfer ratio (h_{re}) vs collector current for each transistor.

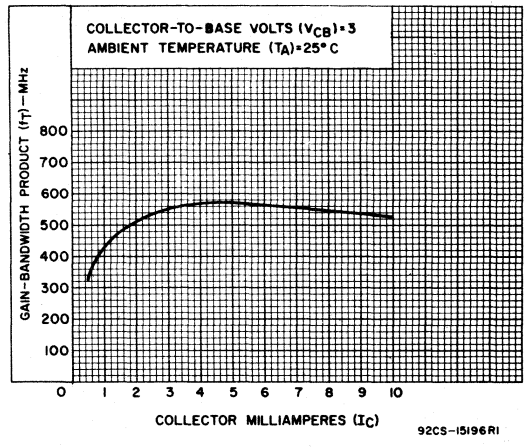


Fig.12 - Gain-bandwidth product (f_T) vs collector current.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER

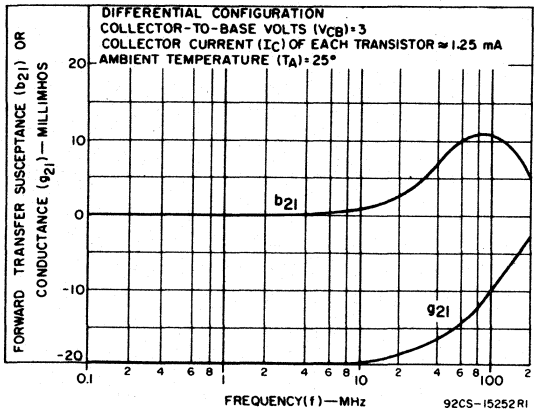


Fig.13(a) - Forward transfer admittance (Y_{21}) vs frequency.

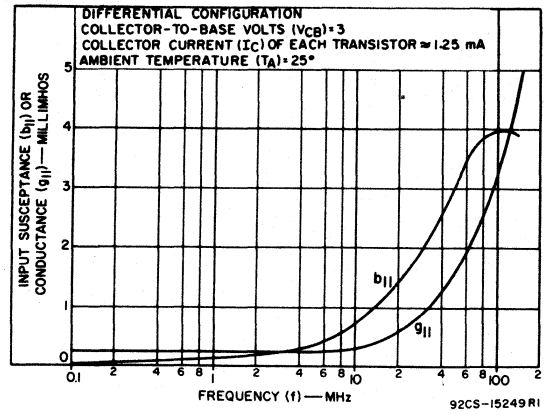


Fig.13(b) - Input admittance (Y_{11}).

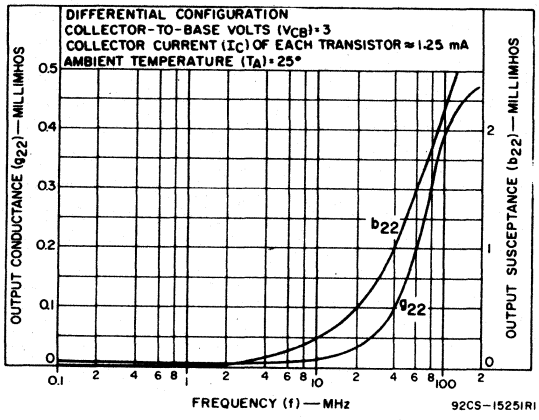


Fig.13(c) - Output admittance (Y_{22}) vs frequency.

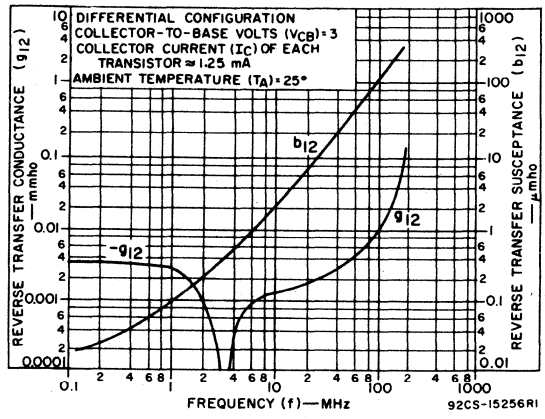


Fig.13(d) - Reverse transfer admittance (Y_{12}) vs frequency.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH CASCODE AMPLIFIER

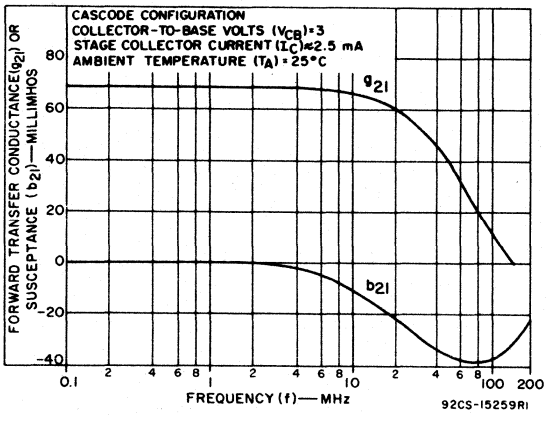


Fig.14(a) - Forward transfer admittance (Y_{21}) vs frequency.

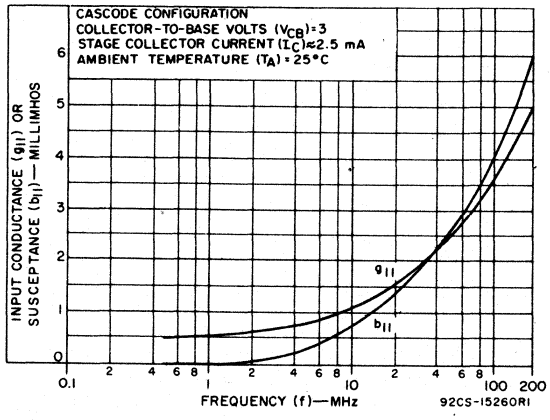


Fig.14(b) - Input admittance (Y_{11}) vs frequency.

TYPICAL CHARACTERISTICS FOR EACH CASCODE AMPLIFIER (cont'd)

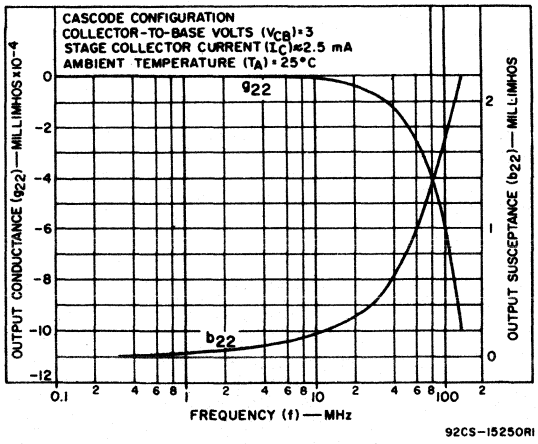


Fig.14(c) - Output admittance (Y_{22}) vs frequency.

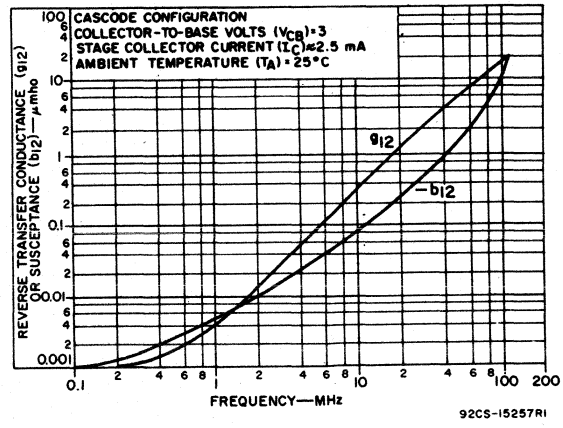


Fig.14(d) - Reverse transfer admittance (Y_{12}) vs frequency.

CA3035, CA3035V1

10-Lead TO-5

H-1384

Ultra-High-Gain Wide-Band Amplifier Array

Features:

- *Three separate amplifiers - gain and bandwidth for each amplifier can be adjusted with suitable external circuitry*
- *Amplifiers operable independently or in cascade*
- *Exceptionally high cascade voltage gain - 129 dB typ. at 40 kHz*
- *Low noise performance*
- *Wide-band response*
- *All amplifiers single-ended - only one power supply required*
- *Wide operating temperature range - -55° C to +125° C*
- *Built-in temperature compensation*
- *Hermetically sealed, all-welded 10-lead TO-5 style metal package with straight or formed leads*

Applications:

- *Three individual general-purpose amplifiers*
- *Ideal for service in remote-control amplifiers - e.g., TV receivers*
- *Available in two electrically identical versions: CA3035 with straight leads; CA3035V1 with formed leads*

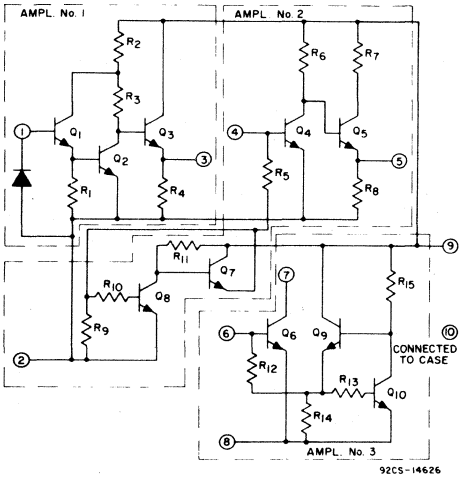


Fig. 1 — Schematic Diagram for CA3035 and CA3035V1

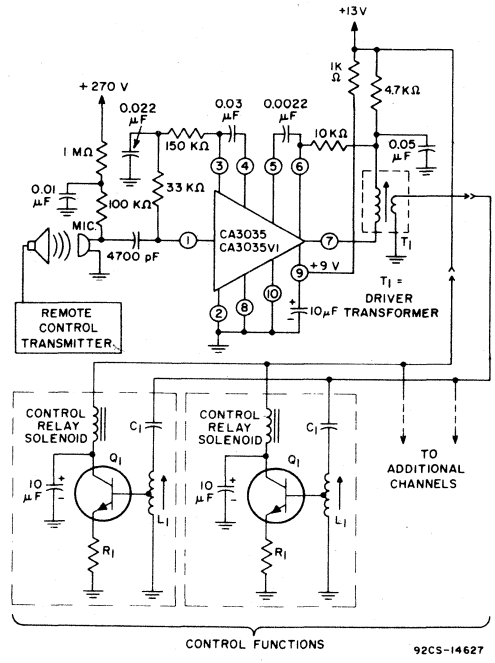


Fig. 2 — Typical Remote Control System

ABSOLUTE-MAXIMUM RATINGS:

Operating Temperature Range . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +200°C
Device Dissipation . . . . . 300 mW
Input Voltage . . . . . 1 V p-p
Supply Voltage . . . . . +15 V

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	TEST CIRCUITS AND CHARAC-TERISTICS CURVES	LIMITS CA3035, CA3035V1 Min.	Typ.	Max.	UNITS
STATIC CHARACTERISTICS							
Quiescent Operating Voltage	V3 V5 V7	V_{CC} = +9V	Fig.3	– – –	2 1.9 4.9	– – –	V V V
Total Current Drain	I_d	V_{CC} = +9V, R_{L3} = 5KΩ	Fig.3	3.5	5	7.5	mA
DYNAMIC CHARACTERISTICS							
Voltage Gain: Amplifier No.1 Amplifier No.2 Amplifier No.3	 A_1 A_2 A_3	 f = 40 kHz, V_{CC} = +9V		 40 40 38	 44 46 42	 – – –	 dB dB dB
Output Voltage Swing	V_{out} V_{1out} V_{2out} V_{3out}	 R_{L1} = 10KΩ R_{L2} = 10KΩ R_{L3} = 5KΩ Sinusoidal Output, V_{CC} = +9V		 – – –	 2 2.6 8	 – – –	 Vp-p Vp-p Vp-p
Input Resistance: Amplifier No.1 Amplifier No.2 Amplifier No.3	 R_1in R_2in R_3in	 f = 40 kHz		 – – –	 50K 2K 670	 – – –	 Ω Ω Ω
Output Resistance	R_1out R_2out R_3out	 f = 40 kHz		 – – –	 270 170 100K	 – – –	 Ω Ω Ω
Bandwidth at -3dB point: Amplifier No.1 Amplifier No.2 Amplifier No.3	 BW_1 BW_2 BW_3	 V_{CC} = +9V	 Fig.5 Fig.6 Fig.7	 – – –	 500 2.5 2.5	 – – –	 kHz MHz MHz
Noise Figure Amplifier No.1	 NF_1	 f = 1 kHz, R_S = 1 KΩ	 Fig.4	 –	 6	 7	 dB
Sensitivity		V_{CC} = +13 V Relay (K_1) Current = 7.5 mA	Fig.2	–	100	150	μV

STATIC CHARACTERISTICS

TEST CIRCUIT

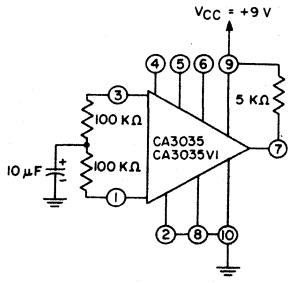
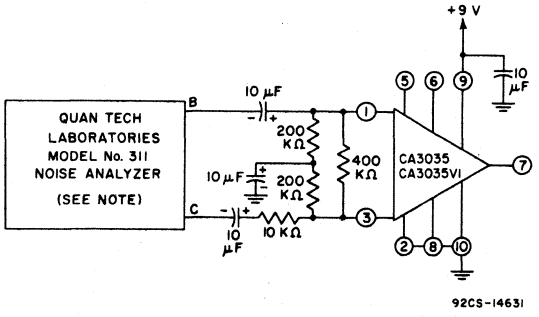


Fig.3

NOISE FIGURE TEST CIRCUIT



NOTE: SET ALL INTERNAL POWER SUPPLIES ON QUAN TECH NOISE ANALYZER TO ZERO VOLTS.

Fig.4

TYPICAL 1st-AMPLIFIER RESPONSE

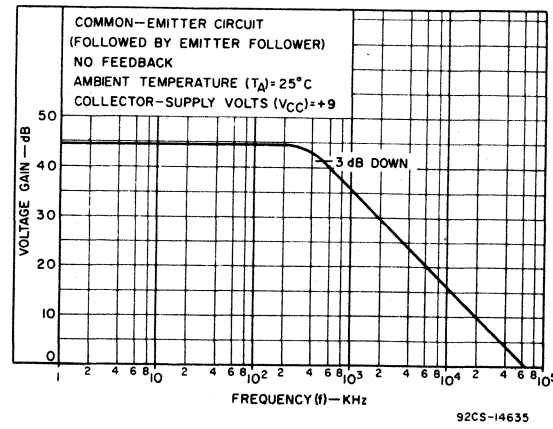


Fig.5

TYPICAL 2nd-AMPLIFIER RESPONSE

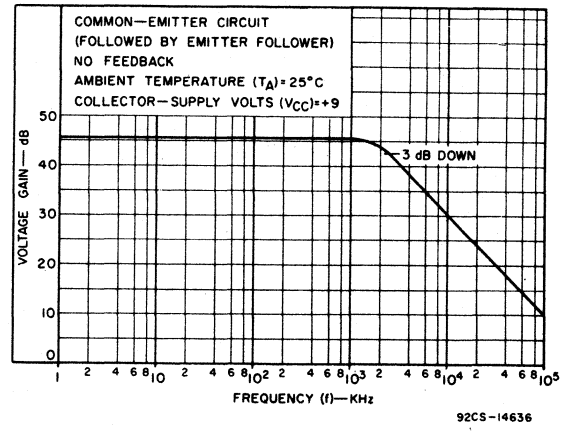


Fig.6

TYPICAL 3rd-AMPLIFIER RESPONSE

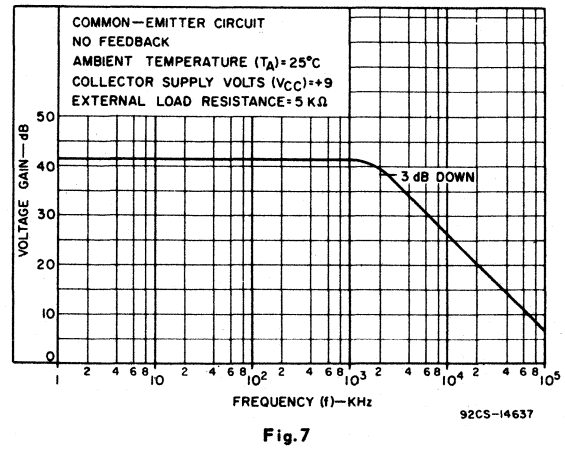
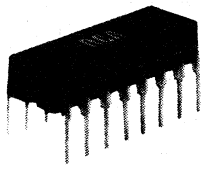


Fig.7



16-Lead Dual-in-Line Plastic Package

CA3048 H-1622

Four Independent AC Amplifiers

For Low-Noise and General AC Applications In Industrial Service

FEATURES

- Four AC amplifiers on a common substrate
- Independently accessible inputs and outputs
- Operates from single-ended supply

EACH AMPLIFIER

- Noise figure at 1 kHz ..... 2 dB typ.
- High voltage gain ..... 53 dB min.
- High input resistance ..... 90 kΩ typ.
- Undistorted output voltage 2 V rms min.
- Output Impedance ..... 1 kΩ typ.
- Open-loop bandwidth ..... 300 kHz typ.

The RCA CA3048 is a silicon monolithic integrated circuit consisting of four independent identical AC amplifiers which can operate from a single-ended power supply..

The amplifiers include internal DC bias and feedback to provide temperature-stabilized operation. They may be used in a wide variety of AC applications in which operational amplifiers have previously been used.

Each high gain amplifier has a high impedance non-inverting input, and a lower impedance inverting input for the application of feedback. Two power-supply terminals and two ground terminals are provided to reduce internal and external coupling between amplifiers.

The CA3048 is supplied in a 16-lead dual-in-line plastic package.

APPLICATIONS

- Multi-channel or cascade operation
- Low-level preamplifiers
- Equalizers
- Linear signal mixers
- Tone generators
- Multivibrators
- AC integrators

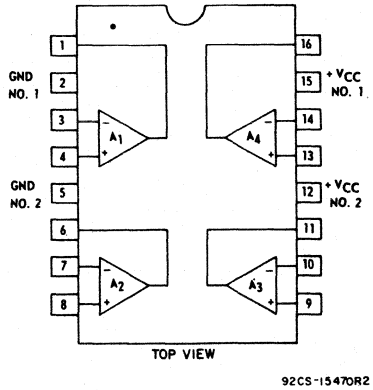


Fig. 1 - Block diagram for CA3048.

CA3048

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C:

DISSIPATION:

At T_A = 55°C . . . . . 750 mW

Above T_A = 55°C. . . . . Derate linearly at 7.7 mW/°C

TEMPERATURE RANGE:

Operating . . . . . -40°C to +85°C

Storage . . . . . -65°C to +150°C

POWER SUPPLY VOLTAGE . . . . . +16 V

AC INPUT VOLTAGE . . . . . 0.5 V rms

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 -16	*
2			*	+2 -3.6	0	*	*	+2 -3.6	-3.6	*	*	+16 0	+2 -3.6	*	+16 0	0 -16
3				+5 -5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 -2	*	*	*	*	*	*	*	*	*	*	*
5						0 -16	*	+2 -3.6	+2 -3.6	*	0 -16	+16 0	+2 -3.6	*	+16 0	*
6							*	*	*	*	*	*	0 -16	*	*	*
7								+5 -5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 -5	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 -16	*	*	*
13														+5 -5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	LIMITS CA3048			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC								
Current drain per amplifier pair	I_{12} or I_{15}	V_{CC} = +12V	3	9.5	13.5	17.5	mA	4,5
DC Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	V_{CC} = +12V	3	6.1	6.9	8.1	V	-
DC Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	V_{CC} = +12V	3	1.7	2.0	2.3	V	-
DC Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	V_{CC} = +12V	3	2.2	2.5	2.8	V	-
DYNAMIC (Characteristics given are for each amplifier with no AC feedback)								
Open-Loop Gain	A_{OL}	V_{CC} = +12V, E_{IN} = 2mV, f = 10kHz	6	53	58	-	dB	7,8
Output Voltage Swing	V_O(rms)	V_{CC} = +12V, f = 1kHz, THD = 5%	6	2.0	2.4	-	V	-
Open-Loop -3dB Bandwidth	BW	V_{CC} = +12V, E_{IN} = 2mV	6	250	300	-	kHz	9
Total Harmonic Distortion	THD	V_{CC} = +12V, f = 1kHz, E_{OUT} = 2V rms	6	-	0.65	-	%	10
Input Resistance	R_{IN}	OPEN LOOP Terminals 3, 7, 10, and 14 are by-passed to ground, f = 1kHz	-	-	90	-	kΩ	-
Input Capacitance	C_{IN}	f = 1MHz	-	-	9	-	pF	-
Output Resistance	R_{OUT}	Terminals 3, 7, 10 and 14 are by-passed to ground	-	-	1	-	kΩ	-
Output Capacitance	C_{OUT}	f = 1MHz	-	-	18	-	pF	-
Feedback Capacitance (Output to non-inverting Input)	C_{FB}	V_{CC} = +12V, f = 1MHz	-	-	<0.1	-	pF	-
Broad-Band Output Noise Voltage	E_N	V_{CC} = +12V, R_S = 10kΩ, A = 40dB, Equivalent Noise BW = 50kHz	11	-	0.3	1	mV	-
Output Noise Voltage "Weighted"	$E_{N(WT)}$		12	-	0.5	2.2	mV	-
Noise Figure	NF (R_S = 5kΩ)	f = 10Hz	-	-	10	-	dB	-
		f = 100Hz	-	-	5.8	-	dB	
		f = 1kHz	-	-	2	-	dB	
		f = 10kHz	-	-	1.1	-	dB	
		f = 100kHz	-	-	0.6	-	dB	
Inter-Amplifier Audio Separation "Cross Talk"		V_{CC} = +12V, f = 1kHz, 0dB = 0.78V	13	-	<-45	-	dB	-
Inter-Amplifier Capacitance (Any amplifier output to any *other* amplifier input)	C	V_{CC} = +12V, f = 1MHz	-	-	<0.02	-	pF	-

CA3048

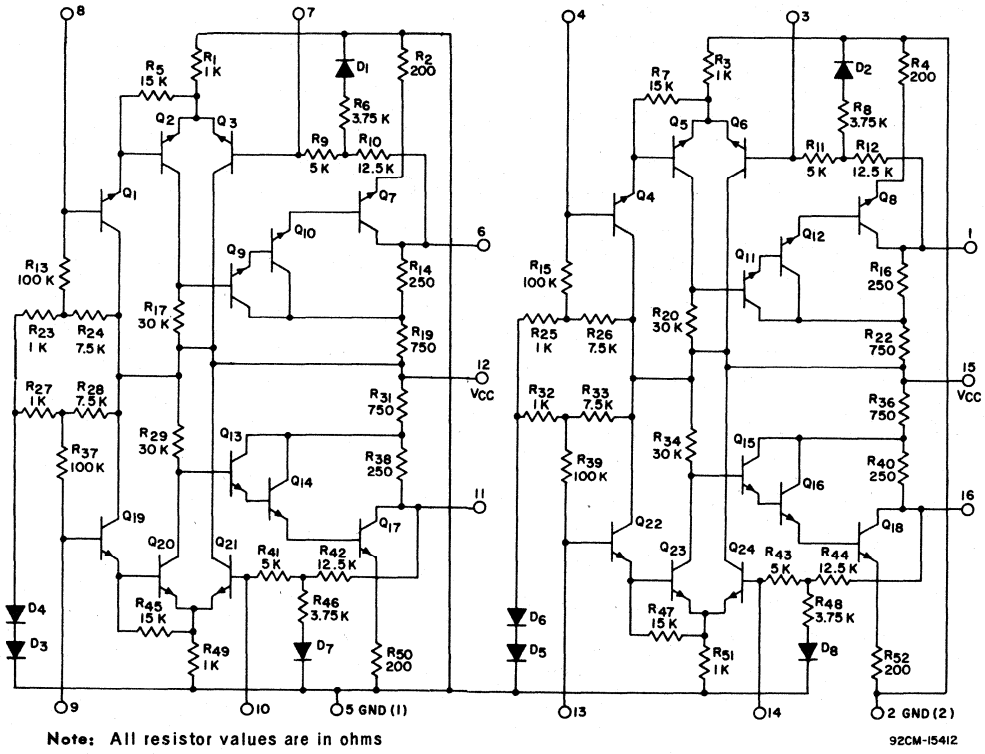


Fig.2 - Schematic diagram for CA3048.

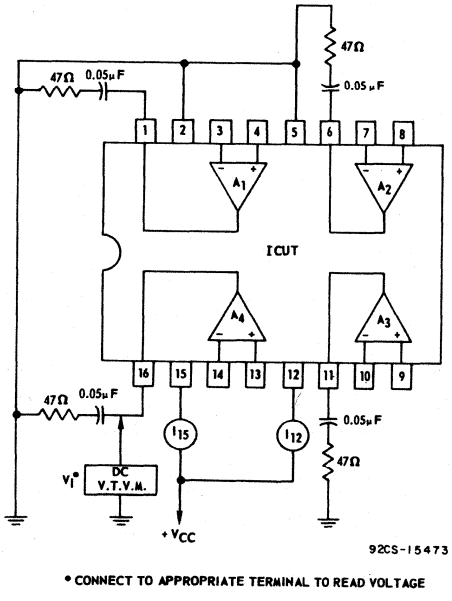


Fig.3 - Test circuit for measurement of collector supply voltage and currents.

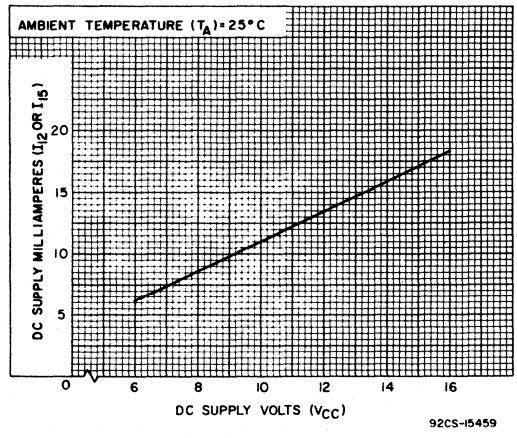


Fig.4 - Typical DC supply current vs supply voltage.

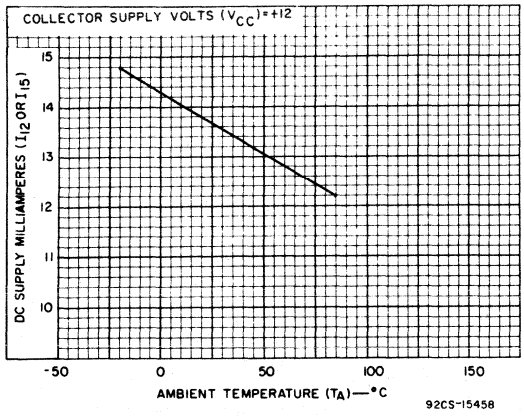


Fig.5 - Typical DC supply current vs ambient temperature.

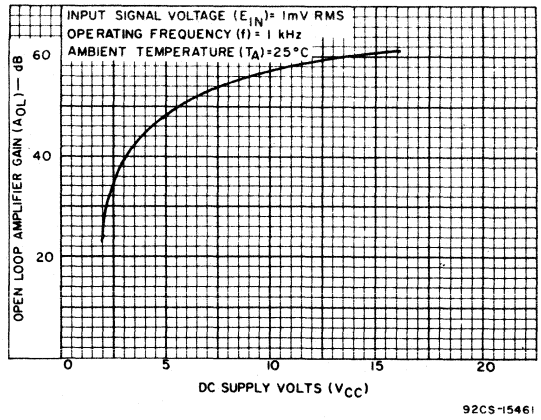
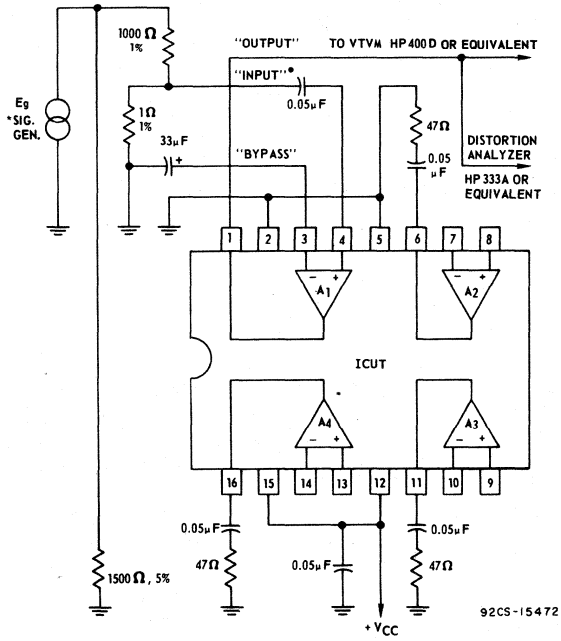


Fig.7 - Typical amplifier gain vs DC supply voltage.



* Sig Gen should be a low distortion type (0.2% THD or less) HP206A or equivalent.

● Adjustment of E_g to 2 volts will make E_S = 2mV.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.6 - Test circuit for measurement of distortion, open-loop gain and bandwidth characteristics.

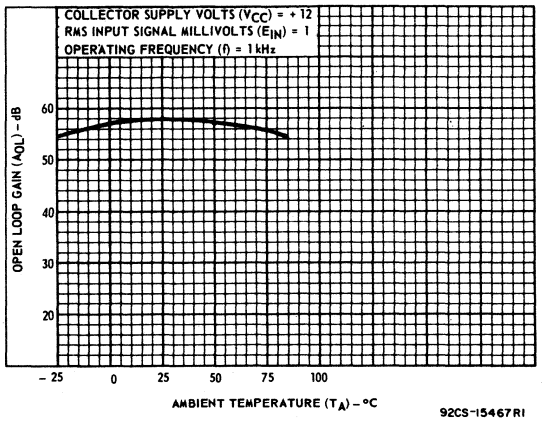


Fig.8 - Typical open-loop gain vs ambient temperature.

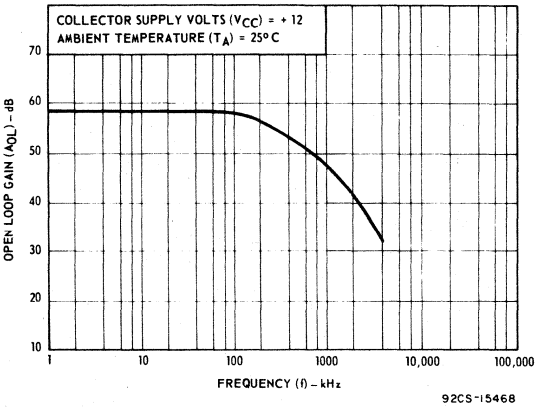


Fig.9 - Typical open-loop gain vs frequency.

CA3048

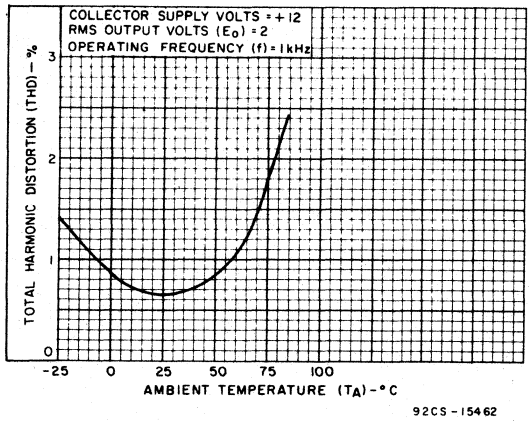
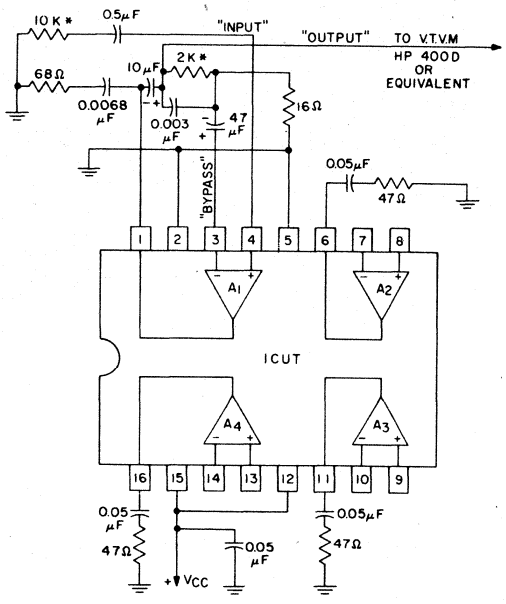


Fig.10 - Typical total harmonic distortion vs ambient temperature.



* RESISTORS ARE METALFILM TYPE, 1%

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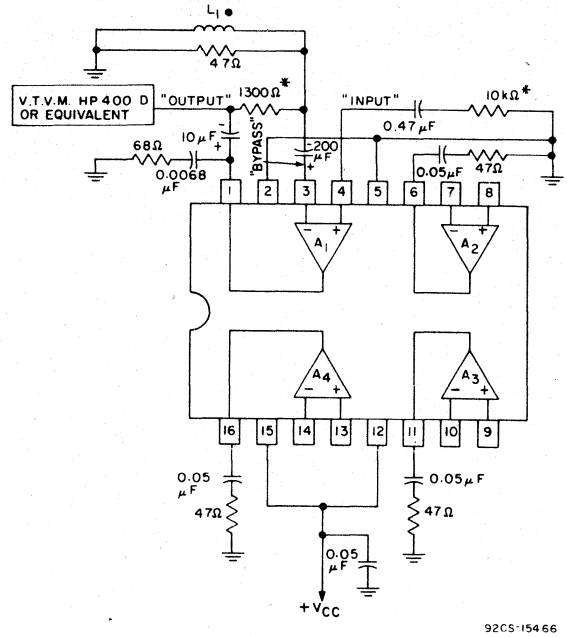
To test Amplifiers 1, 2, 3, or 4, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.11 - Test circuit for measurement of broadband noise characteristic.

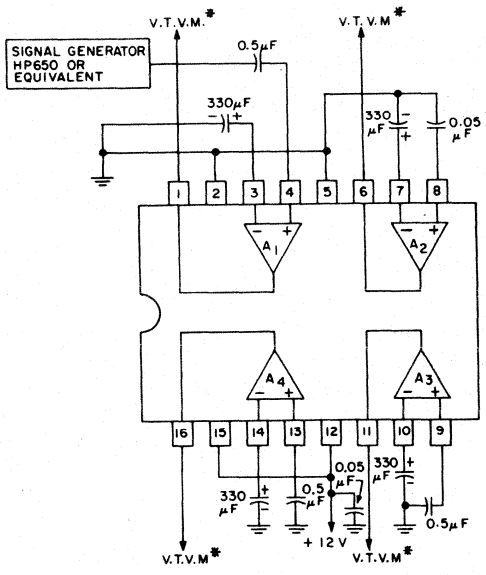


● L_1 - 2.5 millihenry inductor, dc resistance 0.3 ohms or less.

* Resistors metal film type, 1%. To test amplifiers, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.12 - Test circuit for measurement of "weighted" output noise voltage characteristic.



* V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig.13 - Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.

OPERATING CONSIDERATIONS

Economical Gain Control

The CA3048 is designed to permit flexibility in the methods by which amplifier gain can be controlled. Fig.14 shows a curve of the gain of an amplifier when the internal resistive feedback of the device is used in conjunction with an external resistor. Although measured gain of various amplifiers will not be uniform, because of tolerances of internal resistances, this method is very economical and easy to apply.

Stability

The CA3048, as in other devices having high gain-bandwidth product, requires some attention to circuit layout, design, and construction to achieve stability.

Should the CA3048 be left unterminated, socket capacitance alone will provide sufficient feedback to cause high frequency oscillations; therefore, all test circuits in this data bulletin include loading networks that provide stability under all conditions.

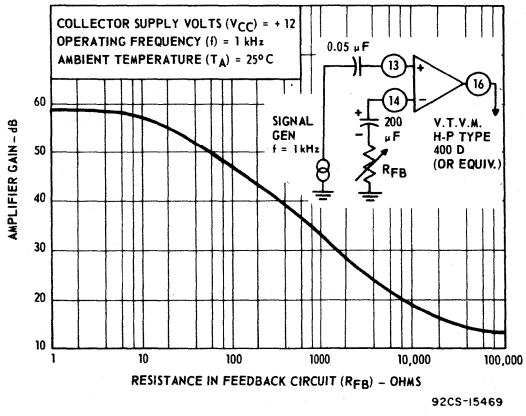
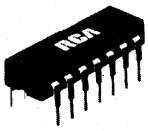


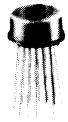
Fig.14 - Typical amplifier gain vs feedback resistance.

CA3049T, CA3102E

14-Lead DIP
CA3102E



12-Lead TO-5



CA3049T

DUAL HIGH-FREQUENCY DIFFERENTIAL AMPLIFIERS

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- **Power Gain 23 dB (typ.) at 200 MHz**
- **Noise Figure 4.6 dB (typ.) at 200 MHz**
- **Two differential amplifiers on a common substrate**
- **Independently accessible inputs and outputs**
- **Full military-temperature-range capability- (−55°C to + 125°C) for the CA3102E and for the CA3049T**

RCA-CA3049T and CA3102E* consist of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general-purpose devices which exhibit low I/f noise and a value of f_T in excess of 1 GHz. These features make the CA3049T and CA3102E useful from dc to 500 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

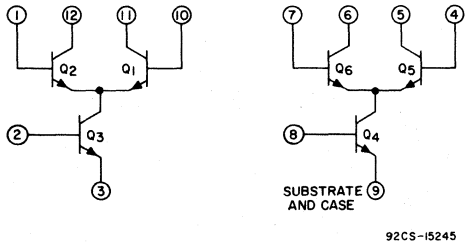
The monolithic construction of the CA3049T and CA3102E provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3102E is like the CA3049T except that it has a separate substrate connection for greater design flexibility. The CA3049T is supplied in the 12-lead TO-5 package; the CA3102E, in the 14-lead plastic dual-in-line package.

Applications

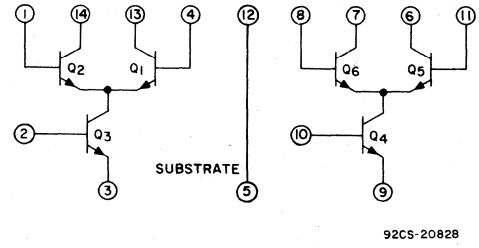
- **VHF amplifiers**
- **VHF mixers**
- **Multifunction combinations – RF/Mixer/Oscillator; Converter/IF**
- **IF amplifiers (differential and/or cascode)**
- **Product detectors**
- **Doubly balanced modulators and demodulators**
- **Balanced quadrature detectors**
- **Cascade limiters**
- **Synchronous detectors**
- **Balanced mixers**
- **Synthesizers**
- **Balanced (push-pull) cascode amplifiers**
- **Sense amplifiers**

*Formerly Developmental No. TA6228.



92CS-15245

Schematic Diagram for CA3049T



92CS-20828

Schematic Diagram for CA3102E

MAXIMUM RATINGS, *ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C*

Power Dissipation, P:	CA3049T	CA3102E	
Any one transistor	300	300	mW
Total package	600	750	mW
For $T_A > 55°C$ Derate at:	5	6.67	mW/°C
Temperature Range:			
Operating	−55 to + 125	−55 to + 125	°C
Storage	−65 to + 150	−65 to + 150	°C

The following ratings apply for each transistor in the devices

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor of the CA3049T and CA3102E is isolated from the substrate by an integral diode. The substrate (terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIR-CUIT	CA3102E LIMITS			CA3049T LIMITS				TYPICAL CHARAC-TERISTICS CURVES
				FIG.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	FIG.
STATIC CHARACTERISTICS												
For Each Differential Amplifier												
Input Offset Voltage	V_{IO}			1	---	0.25	5	---	0.25	---	mV	-4
Input Offset Current	I_{IO}	$I_3 = I_9$ = 2 mA		1	---	0.3	3	---	0.3	---	μA	---
Input Bias Current	I_{IB}			1	---	13.5	33		13.5	33	μA	5
Temperature Coefficient Magnitude of Input-Offset Voltage	$\left\|\frac{\Delta V_{IO}}{\Delta T}\right\|$			1	---	1.1	---	---	1.1	---	μV/°C	4
For Each Transistor												
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 6 V, I_C = 1 mA		---	674	774	874	---	774	---	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 6 V, I_C = 1 mA		---	---	-0.9	---	---	-0.9	---	mV/°C	6
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		---	---	0.0013	100	---	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0		---	15	24	---	15	24	---	V	---
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		---	20	60	---	20	60	---	V	---
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_B = 0, I_E = 0		---	20	60	---	20	60	---	V	---
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0		---	5	7	---	5	7	---	V	---
DYNAMIC CHARACTERISTICS												
1/f Noise Figure (For Single Transistor)	NF	f = 100 KHz, R_S = 500 Ω, I_C = 1 mA		---	---	1.5	---	---	1.5	---	dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 6 V, I_C = 5 mA		---	---	1.35	---	---	1.35	---	GH_z	11
Collector-Base Capacitance	C_{CB}	I_C = 0	V_{CB} = 5V	*	---	0.28	---	---	0.28	---	pF	8
				**	---	0.15	---	---	0.28	---	pF	
Collector-Substrate Capacitance	C_{CI}	I_C = 0	V_{CI} = 5V		---	1.65	---	---	1.65	---	pF	8
For Each Differential Amplifier												
Common-Mode Rejection Ratio	CMR	$I_3 = I_9$ = 2 mA		---	---	100	---	---	100	---	dB	---
AGC Range, One Stage	AGC	Bias Voltage = -6V		2	---	75	---	---	75	---	dB	---
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V, f = 10 MHz		2	18	22	---	---	22	---	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz	Cascode	3	---	23	---	---	23	---	dB	---
Noise Figure	NF	V_{CC} = 12V	Cascode	3	---	4.6	---	---	4.6	---	dB	---
Input Admittance	Y_{11}	For Cascode Configuration, $I_3 = I_9$ = 2 mA	Cascode	---	---	1.5 + j 2.45	---	---	1.5 + j 2.45	---	mmho	14, 16, 18
			Diff.Amp.	---	---	0.878 + j 1.3	---	---	0.878 + j 1.3	---		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff. Amplifier Configuration, $I_3 = I_9$ = 4mA (each collector $I_C \simeq$ 2mA)	Cascode	---	---	0 - j 0.008	---	---	0 - j 0.008	---	mmho	---
			Diff.Amp.	---	---	0 - j 0.013	---	---	0 - j 0.013	---		---
Forward Transfer Admittance	Y_{21}		Cascode	---	---	17.9 - j 30.7	---	---	17.9 - j 30.7	---	mmho	26, 28, 30
			Diff. Amp.	---	---	- 10.5 + j 13	---	---	- 10.5 + j 13	---		27, 29, 31
Output Admittance	Y_{22}		Cascode	---	---	- 0.503 - j 15	---	---	- 0.603 - j 15	---	mmho	20, 22, 24
			Diff.Amp.	---	---	0.071 + j 0.62	---	---	0.071 + j 0.62	---		21, 23, 25

*Terminals 1 & 14, or 7 & 8. (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11. (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

CA3049T, CA3102E

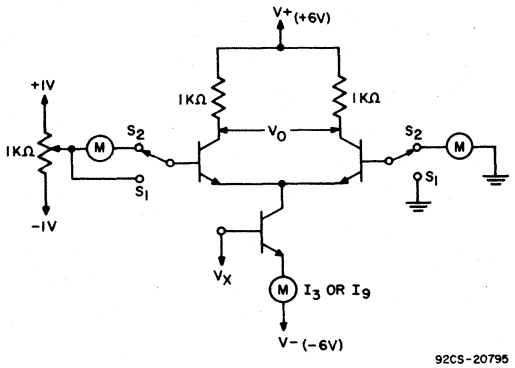


Fig.1—Static characteristics test circuit for CA3102E.

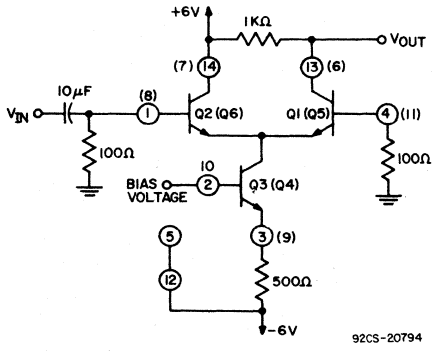
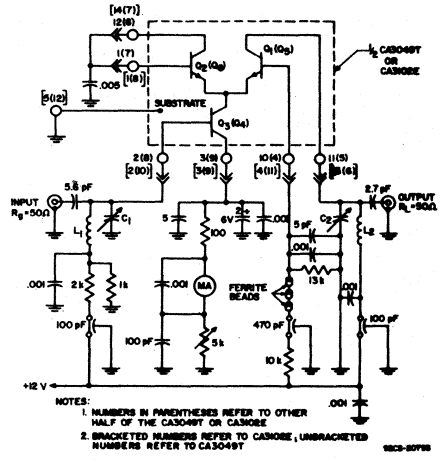


Fig.2—AGC range and voltage gain test circuit for CA3102E.



L_1, L_2 – Approx. 1/2 Turn #18 Tinned Copper Wire, 5/8" Dia.

C_1, C_2 – 15 pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent)

All Capacitors in μF Unless Otherwise Indicated

All Resistors in Ohms Unless Otherwise Indicated

Fig.3—200 MHz cascode power gain and noise figure test circuit.

Typical Characteristics for CA3049T and CA3102E

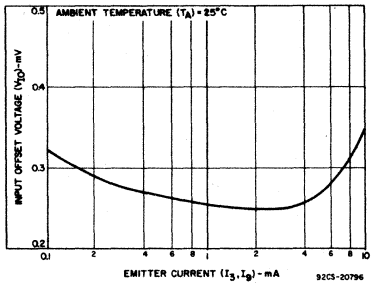


Fig. 4—Input offset voltage vs. emitter current.

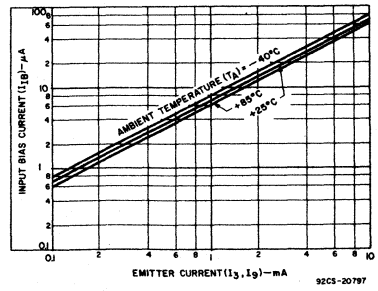


Fig. 5—Input bias current vs. emitter current.

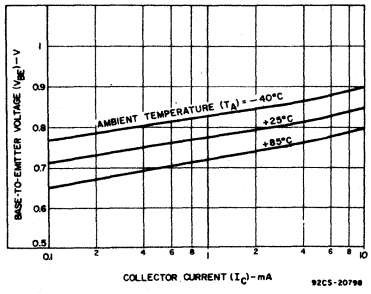


Fig. 6—Base-to-emitter voltage vs. collector current.

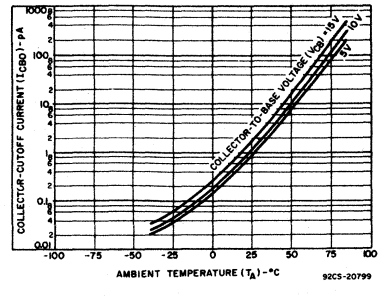


Fig. 7—Collector-cutoff current vs. temperature.

Typical Characteristics for CA3049T and CA3102E (cont'd)

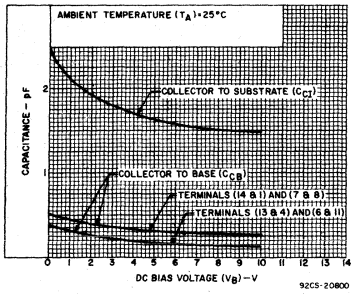


Fig. 8—Capacitance vs. dc bias voltage.

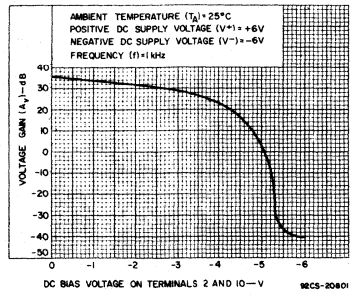


Fig. 9—Voltage gain vs. dc bias voltage.

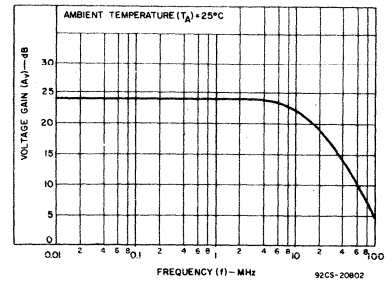


Fig. 10—Voltage gain vs. frequency.

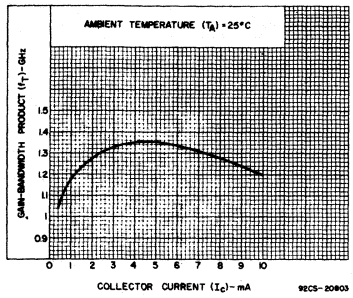


Fig. 11—Gain-bandwidth product vs. collector current.

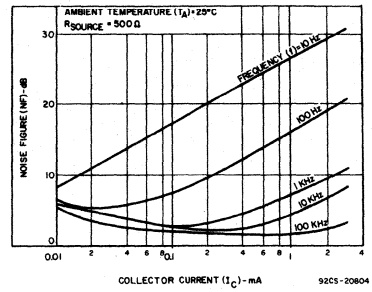


Fig. 12—1/f noise figure vs. collector current.

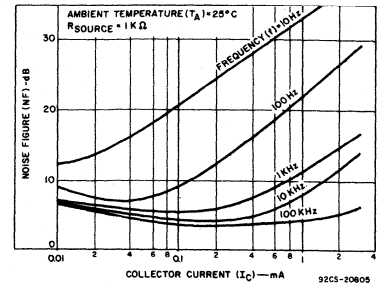


Fig. 13—1/f noise figure vs. collector current.

Typical Input Admittance Characteristics for CA3049T and CA3102

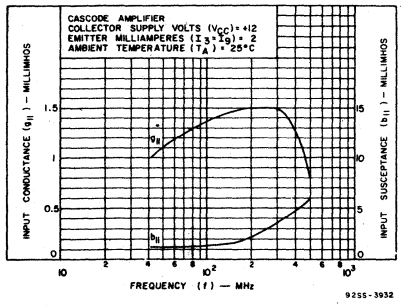


Fig. 14—Input admittance (Y_{11}) vs. frequency.

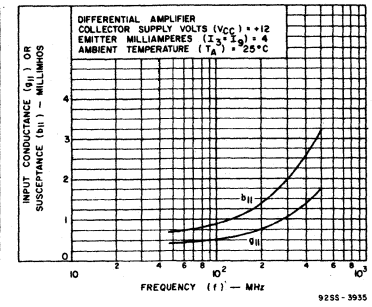


Fig. 15—Input admittance (Y_{11}) vs. frequency.

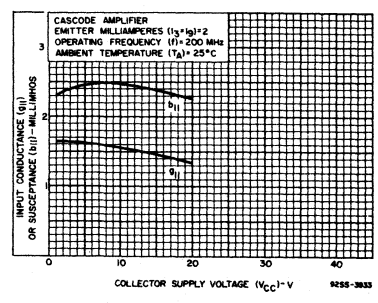


Fig. 16—Input admittance (Y_{11}) vs. collector supply voltage.

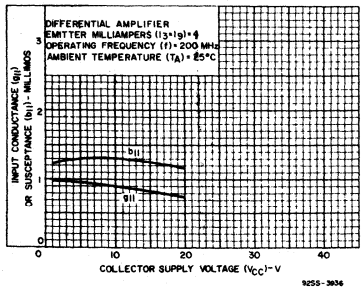


Fig. 17—Input admittance (Y_{11}) vs. collector supply voltage.

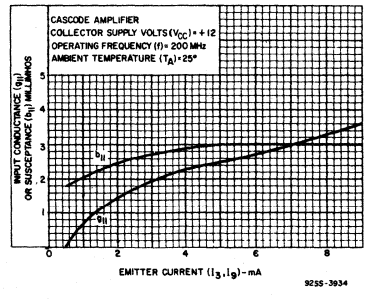


Fig. 18—Input admittance (Y_{11}) vs. emitter current.

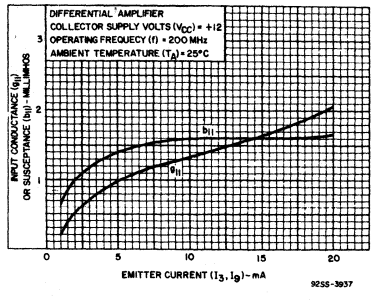


Fig. 19—Input admittance (Y_{11}) vs. emitter current.

Typical Output Admittance Characteristics for CA3049T and CA3102E

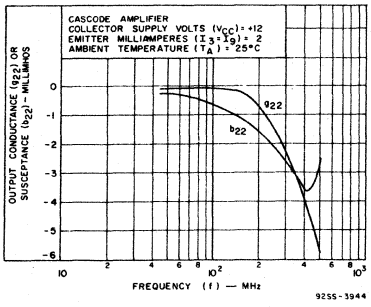


Fig. 20—Output admittance (Y_{22}) vs. frequency.

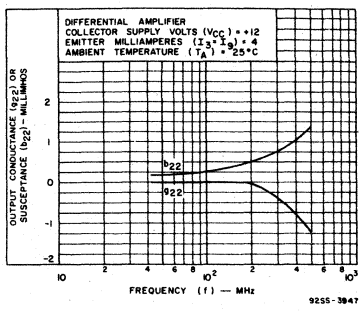


Fig. 21—Output admittance (Y_{22}) vs. frequency.

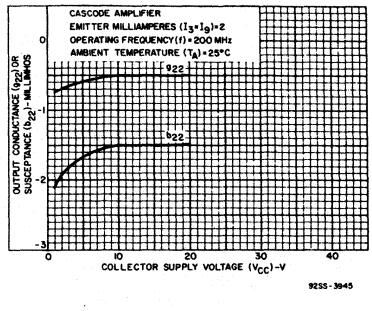


Fig. 22—Output admittance (Y_{22}) vs. collector supply voltage.

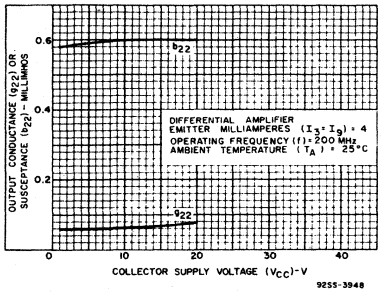


Fig. 23—Output admittance (Y_{22}) vs. collector supply voltage.

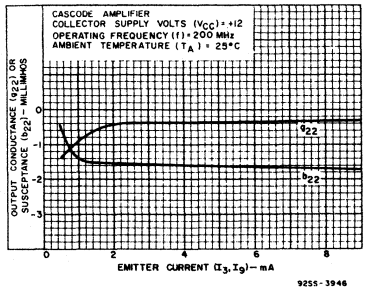


Fig. 24—Output admittance (Y_{22}) vs. emitter current.

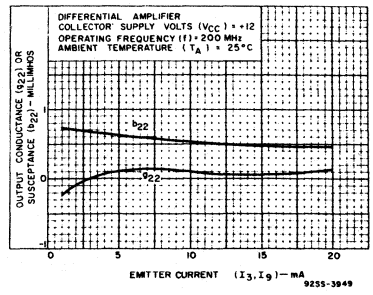


Fig. 25—Output admittance (Y_{22}) vs. emitter current.

Typical Forward Transfer Characteristics for CA3049T and CA3102E

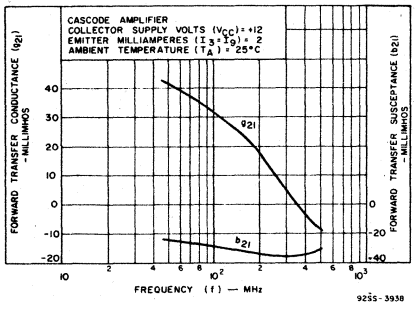


Fig. 26—Forward transfer admittance (Y_{21}) vs. frequency.

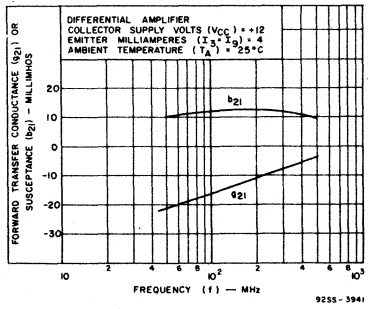


Fig. 27—Forward transfer admittance (Y_{21}) vs. frequency.

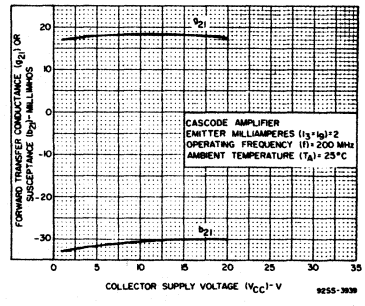


Fig. 28—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

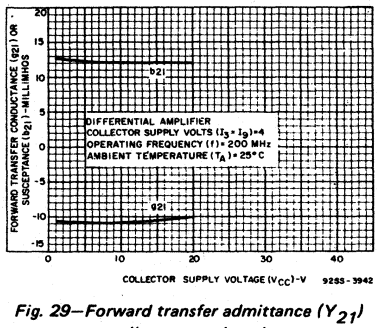


Fig. 29—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

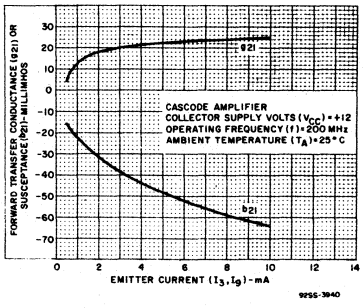


Fig. 30—Forward transfer admittance (Y_{21}) vs. emitter current.

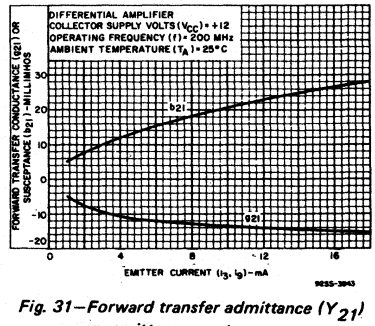
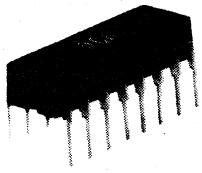


Fig. 31—Forward transfer admittance (Y_{21}) vs. emitter current.



H-1622

16-Lead Dual-In-Line Plastic Package

Four Independent AC Amplifiers

Special-Function Sub-System for Stereo Preamplifiers, Magnetic Pickups, Tape Heads, etc.

Features:

- *Four AC amplifiers on a common substrate*
- *Independently accessible inputs and outputs*
- *Operates from single-ended supply*

EACH AMPLIFIER

- *High voltage gain - 53 dB min.*
- *High input resistance - 90 kΩ typ.*
- *Undistorted output voltage - 2 V rms min.*
- *Output impedance - 1 kΩ typ.*
- *Open-loop bandwidth - 300 kHz typ.*

Applications:

- *Full-function stereo preamplifiers*
- *Tape recorder and playback preamplifiers*
- *Tone generators*

The RCA-CA3052 is a silicon monolithic integrated circuit designed specifically for stereo preamplifier service. The circuit consists of four independent ac amplifiers which can operate from a single-ended supply.

The CA3052 can operate as an equalizer amplifier in tape recorders, magnetic cartridge phonograph applications, and tone control amplifiers. It can provide all of the amplification necessary for a full-function stereo preamplifier.

The CA3052 is supplied in a 16-lead dual-in-line plastic package.

RCA-CA3052 is schematically identical with the CA3048 Amplifier Array (File No. 377). Each amplifier of the CA3048 is tightly specified for equivalent output noise under a variety of test methods. The CA3052 is specified using RIAA test methods for equivalent input noise using one test method for amplifiers 1 and 4, and an appropriately different method for amplifiers 2 and 3.

ABSOLUTE-MAXIMUM RATING *at* $T_A = 25°C$:

DISSIPATION:

Up to $T_A = 55°C$ ..... 750 mW

Above $T_A = 55°C$ ..... Derate linearly at 7.7 mW/°C

TEMPERATURE RANGE:

Operating ..... −40°C to +85°C

Storage ..... −65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)

from case for 10 seconds max. ..... +265°C

POWER SUPPLY VOLTAGE ..... +16 V

AC INPUT VOLTAGE ..... 0.5 V rms

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 -16	*
2			*	+2 -3.6	0	*	*	+2 -3.6	+2 -3.6	*	*	+16 0	+2 -3.6	*	+16 0	0 -16
3				+5 -5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 -2	*	*	*	*	*	*	*	*	*	*	*
5						0 -16	*	+2 -3.6	+2 -3.6	*	0 -16	+16 0	+2 -3.6	*	+16 0	*
6							*	*	*	*	*	*	0 -16	*	*	*
7								+5 -5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 -5	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 -16	*	*	*
13														+5 -5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

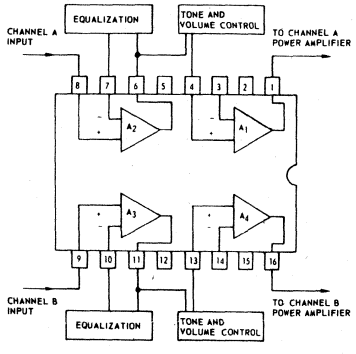


Fig. 1 – Block diagram of stereo preamplifier using CA3052.

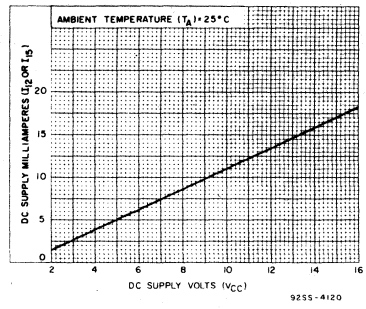


Fig. 2 – Typical DC supply current vs supply voltage.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS CA3052			UNITS
			MIN.	TYP.	MAX.	
STATIC						
Current drain per amplifier pair	I_{12} or I_{15}	V_{CC} = +12 V	9.5	13.5	17.5	mA
DC Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	V_{CC} = +12 V	6.1	6.9	8.1	V
DC Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	V_{CC} = +12 V	1.7	2.0	2.3	V
DC Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	V_{CC} = +12 V	2.2	2.5	2.8	V
DYNAMIC each amplifier with no AC feedback unless otherwise noted--terminals 3, 7, 10, & 14 bypassed to ground						
Open-Loop Gain	A_{OL}	V_{CC} = +12 V E_{IN} = 2 mV f = 10 kHz	53	58	–	dB
Open-Loop Output Voltage Swing	V_O(rms)	V_{CC} = +12 V f = 1 kHz THD = 5%	2.0	2.4	–	V
Open-Loop -3 dB Bandwidth	BW	V_{CC} = +12 V E_{IN} = 2 mV	–	300	–	kHz
Open-Loop Total Harmonic Distortion	THD	V_{CC} = +12 V, f = 1 kHz E_{OUT} = 2 V rms	–	0.65	–	%
Input Resistance	R_I	V_{CC} = +12 V, f = 1 kHz	–	90	–	kΩ
Input Capacitance	C_I	V_{CC} = +12 V, f = 1 MHz	–	9	–	pF
Output Resistance	R_O	V_{CC} = +12 V, f = 1 kHz	–	1	–	kΩ
Feedback Capacitance (Output to non-inverting Input)	C_{FB}	V_{CC} = +12 V f = 1 MHz	–	<0.1	–	pF
Equivalent Input Noise Voltage (Amplifiers 1 & 4), "C" Filter at Output*	E_{N1}‡	V_{CC} = +10 V R_S = 5 kΩ A = 45 dB	–	1.7	6.4	μV
Equivalent Input Noise Voltage (Amplifiers 2 & 3) RIAA Compensated*	E_{N2}‡	V_{CC} = +10 V R_S = 5 kΩ A = 64 dB (1 kHz)	–	4	15.0	μV
Inter-Amplifier Audio Separation "Cross Talk"[11]		V_{CC} = +12 V f = 1 kHz 0 dB = 0.78 V	–	<-45	–	dB
Inter-Amplifier Capacitance (Any amplifier output to any *other* amplifier input)	C	V_{CC} = +12 V f = 1 MHz	–	< 0.02	–	pF

*Per IHF Standard Methods of Measurement for Audio Amplifiers IHF–A–201, 1966

‡ ac feedback included in test circuit

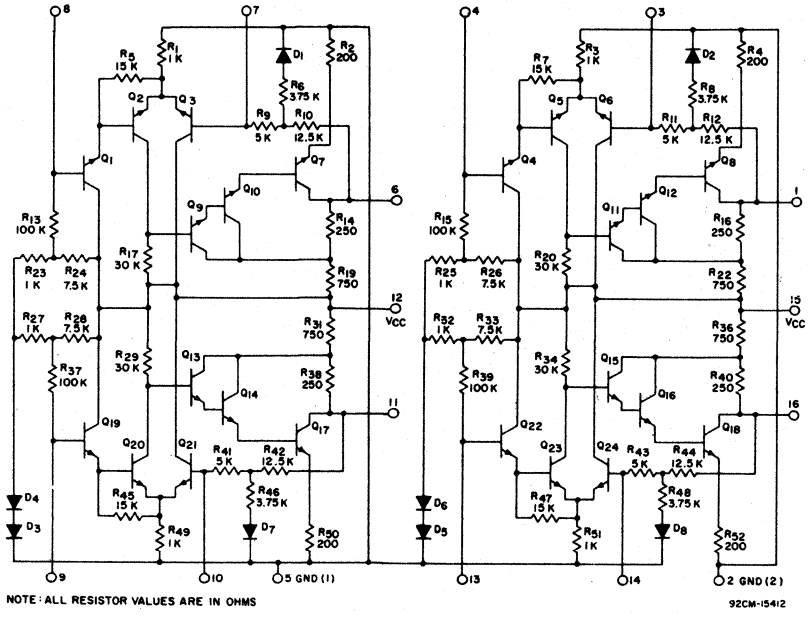


Fig. 3 – Schematic diagram for CA3052.

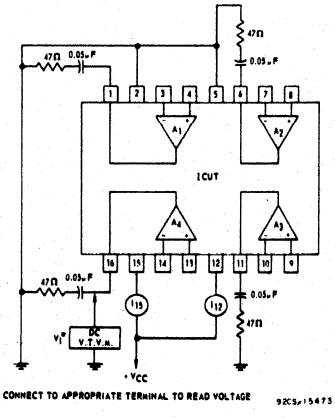


Fig. 4 – Test circuit for measurement of collector supply voltage and currents.

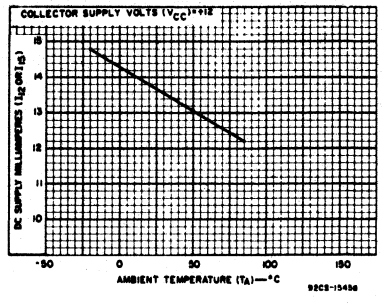
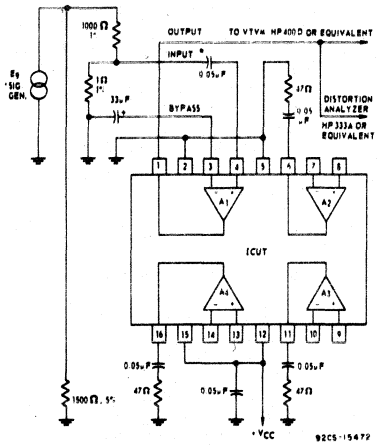


Fig. 5 – Typical DC supply current vs ambient temperature.



* Sig Gen should be a low distortion type (0.2% THD or less) HP206A or equivalent.

● Adjustment of E_g to 2 volts will make E_s = 2mV.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig. 6 – Test circuit for measurement of distortion, open-loop gain, and bandwidth characteristics.

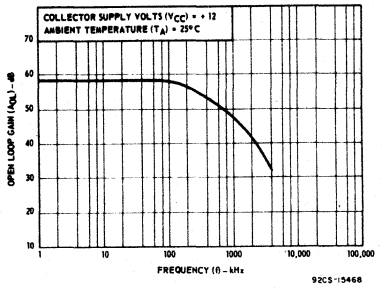


Fig. 9 – Typical open-loop gain vs frequency.

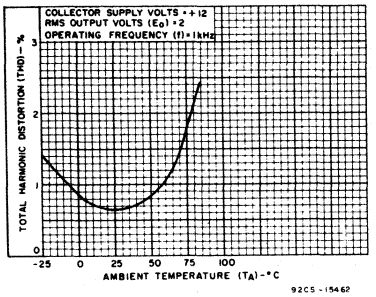


Fig. 10 – Typical total harmonic distortion vs ambient temperature.

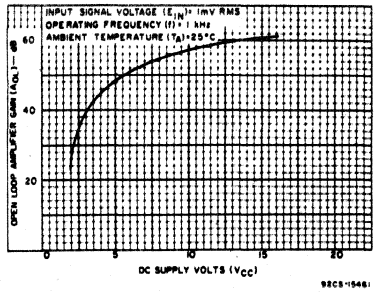


Fig. 7 – Typical amplifier gain vs DC supply voltage.

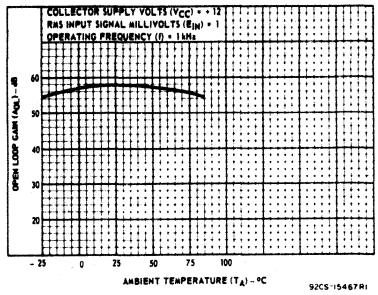
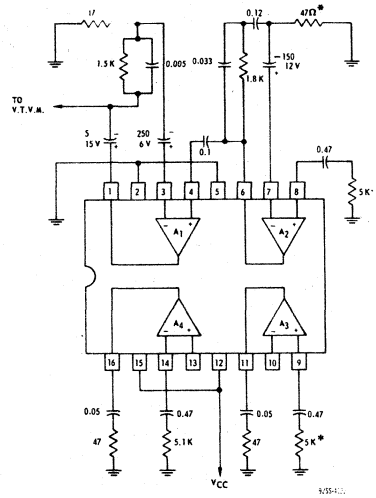
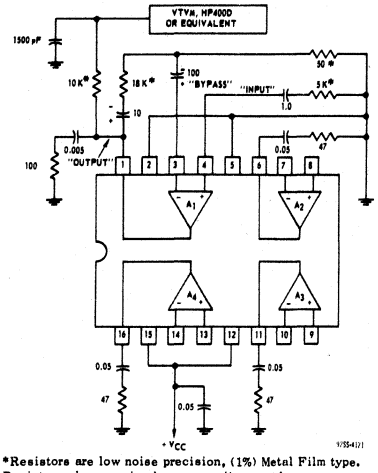


Fig. 8 – Typical open-loop gain vs ambient temperature.



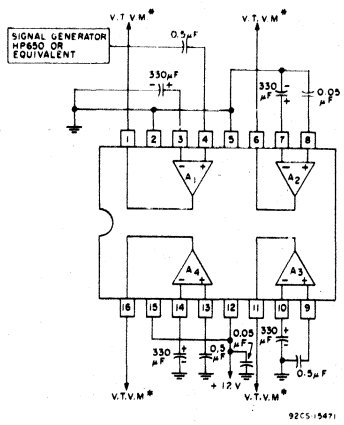
*Resistors are low noise precision (1%) Metal Film type.

Fig. 11 – Test circuit for equivalent input noise voltage measurement, RIAA compensated.



*Resistors are low noise precision, (1%) Metal Film type. Resistor values are in ohms; capacitance values are in microfarads, unless otherwise specified.

Fig. 12— Test circuit for measurement of equivalent input noise voltage of amplifiers 1 and 4.

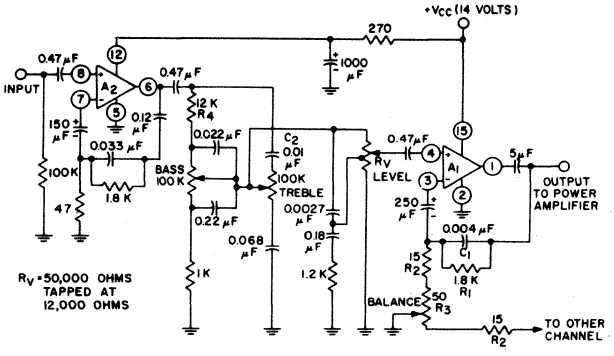


*V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig. 13 — Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.



Performance Data

Gain at 1-kHz reference	47 dB
Boost at 100 Hz	11.5 dB
Boost at 10 kHz	11.5 dB
Cut at 100 Hz	10 dB
Cut at 10 kHz	9 dB
Noise:	
At maximum volume (input shorted)	> 70 dB below 1 volt
At minimum volume	> 80 dB below 1 volt
Total harmonic distortion (at 1-kHz reference and an output of 1 volt)	< 0.3 per cent

92CM-29305

Fig. 14 — Schematic of one channel of a complete stereo preamplifier.

OPERATING CONSIDERATIONS

Economical Gain Control

The CA3052 is designed to permit flexibility in the methods by which amplifier gain can be controlled. Fig. 15 shows a curve of the gain of an amplifier when the internal resistive feedback of the device is used in conjunction with an external resistor. Although measured gain of various amplifiers will not be uniform, because of tolerances of internal resistances, this method is very economical and easy to apply.

Stability

The CA3052, as in other devices having high gain-band-width product, requires some attention to circuit layout, design, and construction to achieve stability.

Should the CA3052 be left unterminated, socket capacitance alone will provide sufficient feedback to cause high frequency oscillations; therefore, all test circuits in this data bulletin include loading networks that provide stability under all conditions.

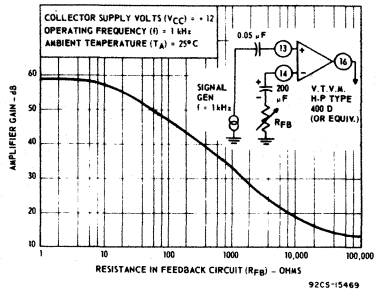
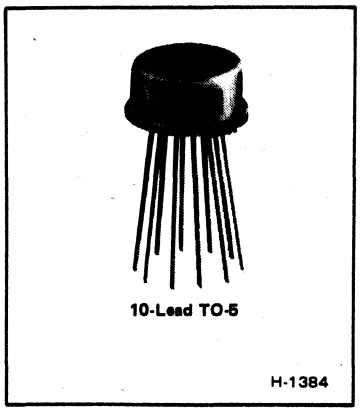


Fig. 15 — Typical amplifier gain vs feedback resistance.

CA3019



Ultra-Fast Low-Capacitance Matched Diodes

For Applications in Communications and Switching Systems

Features:

- *Excellent diode match*
- *Low leakage current*
- *Low pedestal voltage when gating*
- *Companion Application Note, ICAN-5299: "Application of the RCA-CA3019 Integrated-Circuit Diode Array"*

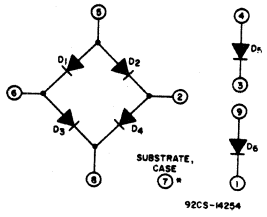
Applications:

- *Modulator*
- *Mixer*
- *Balanced modulator*
- *Analog switch*
- *Diode gate for chopper-modulator applications*

The RCA-CA3019 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Four of the diodes are internally connected as a "quad" and two are independently accessible. The substrate is internally connected to the 10-lead TO-5-style case.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.



*Connect to most negative circuit potential.

Fig. 1 — Schematic Diagram.

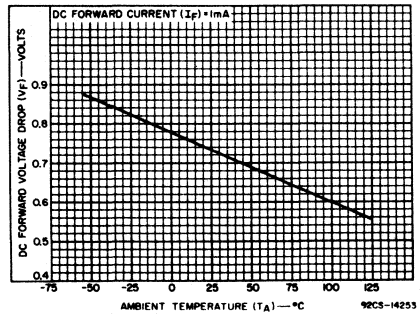


Fig. 2 – DC forward voltage drop (any diode) as a function of temperature.

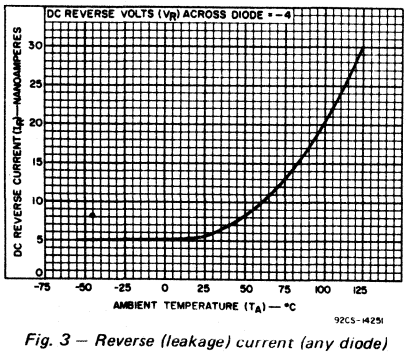


Fig. 3 – Reverse (leakage) current (any diode) as a function of temperature.

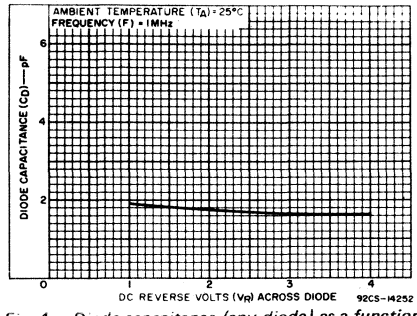


Fig. 4 – Diode capacitance (any diode) as a function of reverse voltage.

Absolute-Maximum Ratings:

DISSIPATION:
- Any one diode unit . . . 20 max. mW
- Total for device . . . . 120 max. mW

TEMPERATURE RANGE:
- Storage . . . . . −65 to +200 °C
- Operating . . . . . −55 to +125 °C

DC Forward Current, I_F . . 25 mA

Peak Recurrent Forward Current, I_f . . . . . 100 mA

Peak Forward Surge Current, I_f (surge) . . . 100 mA

VOLTAGE: See Table

Absolute-Maximum Voltage Limits:

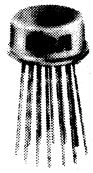
TERM.	VOLTAGE LIMITS		CONDITIONS	
	NEG.	POS.	TERM.	VOLT.
1	−3	+12	7	−6
2	−3	+12	7	−6
3	−3	+12	7	−6
4	−3	+12	7	−6
5	−3	+12	7	−6
6	−3	+12	7	−6
7	−18	0	1,2, 3,6, 8	0
8	−3	+12	7	−6
9	−3	+12	7	−6
10	NO CONNECTION			
CASE	INTERNALLY CONNECTED TO TERMINAL 7 **DO NOT GROUND**			

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$

Characteristics Apply for Each Diode Unit, Unless Otherwise Specified

CHARACTERISTICS	SPECIAL TEST CONDITIONS	LIMITS TYPE CA3019			Units
		Min.	Typ.	Max.	
DC Forward Voltage Drop	DC Forward Current (I_F) = 1 mA	–	0.73	0.78	V
DC Reverse Breakdown Voltage	DC Reverse Current (I_R) = −10 μA	4	6	–	V
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	DC Reverse Current (I_R) = −10 μA	25	80	–	V
DC Reverse (Leakage) Current	DC Reverse Voltage (V_R) = −4 V	–	0.0055	10	μA
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	DC Reverse Voltage (V_R) = −4 V	–	0.010	10	μA
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	DC Forward Current (I_F) = 1 mA	–	1	5	mV
Single Diode Capacitance	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) = −2V	–	1.8	–	pF
Diode Quad-to-Substrate Capacitance	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) between Terminal 2,5,6, or 8 of Diode Quad and Terminal 7 (Substrate) = −2 V				
	Terminal 2 or 6 to Terminal 7	–	4.4	–	pF
	Terminal 5 or 8 to Terminal 7	–	2.7	–	pF
Series Gate Switching Pedestal Voltage		–	10	–	mV

CA3039



12-Lead TO-5

H-1463

Diode Array

Six Matched Diodes on a Common Substrate

Ultra-Fast Low-Capacitance Matched Diodes For Applications in Communications and Switching Systems

Features:

- *Excellent reverse recovery time - 1 ns typ.*
- *Matched monolithic construction - V_F matched within 5 mV*
- *Low diode capacitance - C_D = 0.65 pF typical at V_R = −2 V*

The RCA-CA3039 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

Applications

- *Balanced modulators or demodulators*
- *Ring modulators*
- *High speed diode gates*
- *Analog switches*

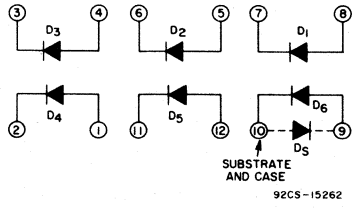


Fig. 1 — Schematic Diagram for CA3039.

ABSOLUTE MAXIMUM RATINGS at T_A = 25 °C

Dissipation:
- Any one diode unit . . . . . 100 mW
- Total for device . . . . . 600 mW
- For T_A > 55 °C . . . . . derate linearly 5.7 mW/°C

Temperature Range:
- Operating . . . . . -55 to +125 °C
- Storage . . . . . -65 to +150°C

Peak Inverse Voltage, PIV for: D_1-D_5 . . . 5 V
D_6 . . . . . 0.5 V

Peak Diode-to-Substrate Voltage, V_{DI}
for D_1-D_5 (term. 1,4,5,8 or 12 to term. 10) +20, -1 V

DC Forward Current, I_F . . . . . 25 mA

Peak Recurrent Forward Current, I_f . . . . . 100 mA

Peak Forward Surge Current, I_f (surge) . . . 100 mA

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . + 265 °C

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

Characteristics apply for each diode unit, unless otherwise specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS			UNITS	CHARACTERISTIC CURVES
			MIN.	TYP.	MAX.		FIG.
DC Forward Voltage Drop	V_F	I_F = 50 μA	–	0.65	0.69	V	2
		1 mA	–	0.73	0.78	V	
		3 mA	–	0.76	0.80	V	
		10 mA	–	0.81	0.90	V	
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = -10 μA	5	7	–	V	–
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	I_R = -10 μA	20	–	–	V	–
DC Reverse (Leakage) Current	I_R	V_R = -4 V	–	0.016	100	nA	3
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	V_R = -10 V	–	0.022	100	nA	4
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F_1} - V_{F_2} \rvert$	I_F = 1 mA	–	0.5	5	mV	2
Temperature Coefficient of $\lvert V_{F_1} - V_{F_2} \rvert$	$\frac{\Delta \lvert V_{F_1} - V_{F_2} \rvert}{\Delta T}$	I_F = 1 mA	–	1	–	μV/°C	5
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	I_F = 1 mA	–	-1.9	–	mV/°C	6
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1 mA	–	0.65	–	V	–
Reverse Recovery Time	t_{rr}	I_F = 10 mA, I_R = 10 mA	–	1	–	ns	–
Diode Resistance	R_D	f = 1 kHz, I_F = 1 mA	25	30	45	Ω	7
Diode Capacitance	C_D	V_R = -2 V, I_F = 0	–	0.65	–	pF	8
Diode-to-Substrate Capacitance	C_{DI}	V_{DI} = +4 V, I_F = 0	–	3.2	–	pF	9

TYPICAL CHARACTERISTICS

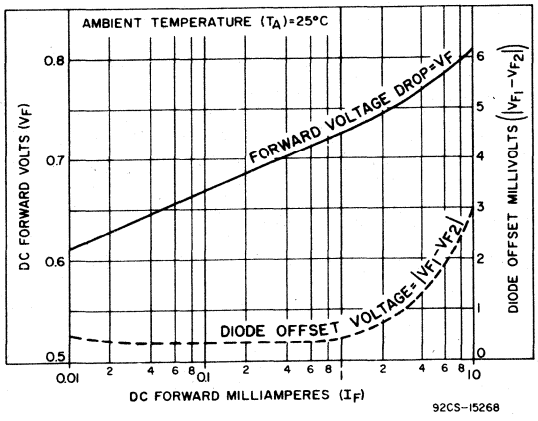


Fig. 2 - DC forward voltage drop (any diode) and diode offset voltage vs DC forward current

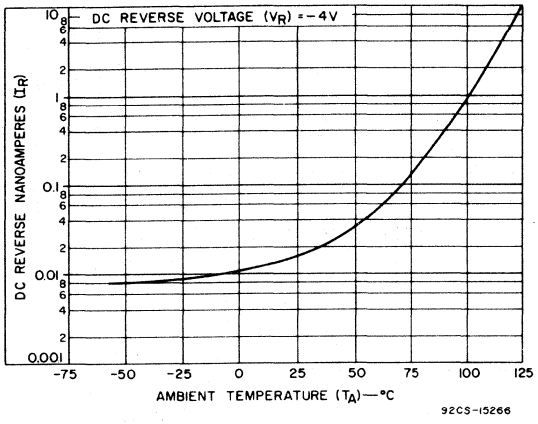


Fig. 3 - DC reverse (leakage) current (diodes 1,2,3,4,5) vs temperature

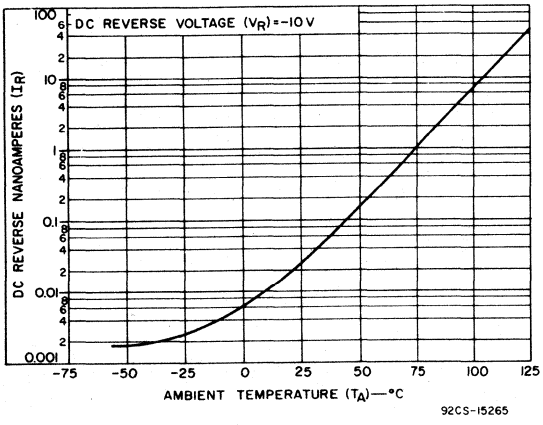


Fig. 4 - DC reverse (leakage) current between diodes (1,2,3,4,5) and substrate vs temperature

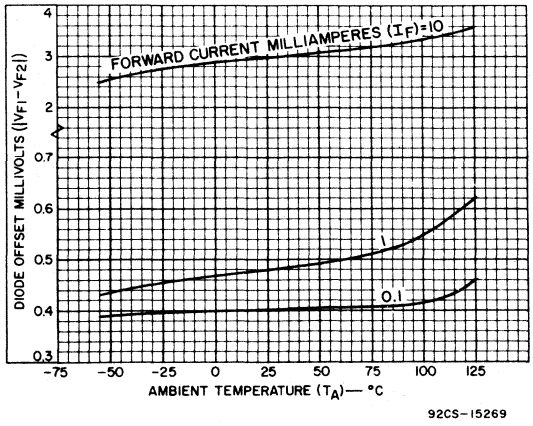


Fig. 5 - Diode offset voltage (any diode) vs temperature

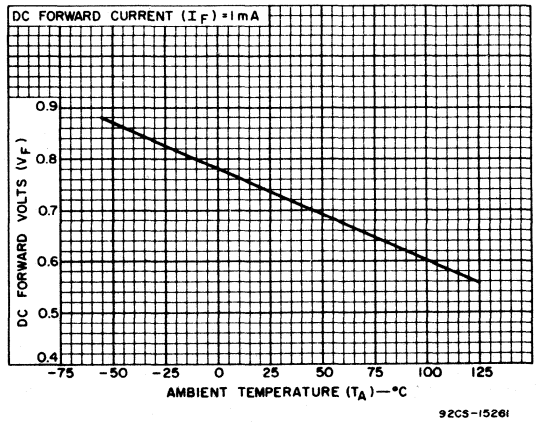


Fig. 6 - DC forward voltage drop (any diode) vs temperature

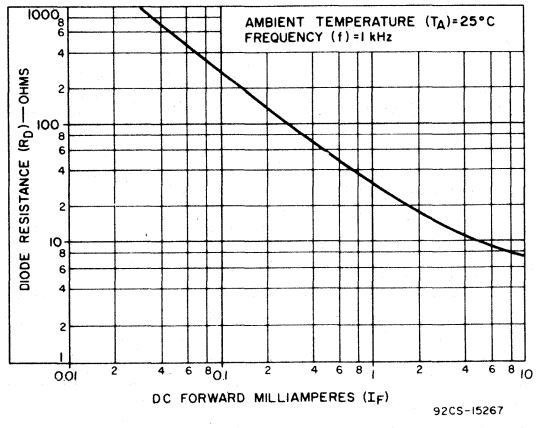


Fig. 7 - Diode resistance (any diode) vs DC forward current

TYPICAL CHARACTERISTICS

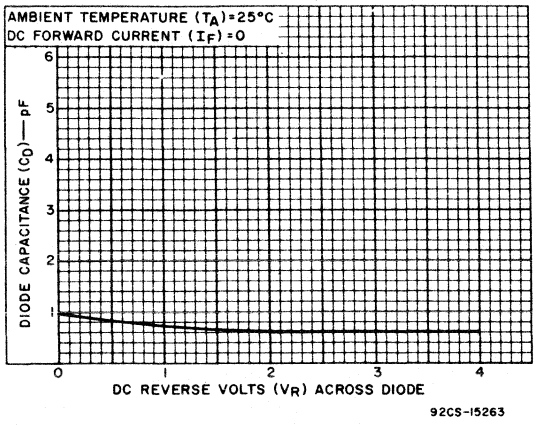


Fig. 8 - Diode capacitance (diodes 1,2,3,4,5) vs reverse voltage

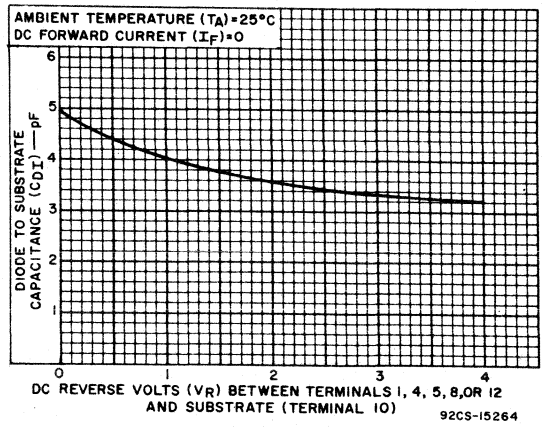
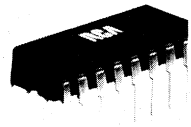


Fig. 9 - Diode-to-substrate capacitance vs reverse voltage

CA3141E



16-Lead Dual-in-Line
Plastic Package
(E suffix)

H-1622

High-Voltage Diode Array

For Commercial, Industrial, and Military Applications

Features:

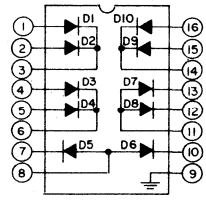
- *Matched monolithic construction - V_F for each diode pair matched to within 0.55 mV (typ.) at I_F = 1 mA*
- *Low diode capacitance - 0.3 pF (typ.) at V_R = 2 V*
- *High diode-to-substrate breakdown voltage - 30 V (min.)*
- *Low reverse (leakage) current - 100 nA (max.)*

Applications:

- *Balanced modulators or demodulators*
- *Analog switches*
- *High-voltage diode gates*
- *Current ratio detectors*

The RCA-CA3141E High-Voltage Diode Array consists of ten general-purpose high-reverse-breakdown diodes. Six diodes are internally connected to form three common-cathode diode pairs, and the remaining four diodes are internally connected to form two common-anode diode pairs. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the CA3141E extremely useful for a wide variety of applications in communications and switching systems.

The CA3141 is supplied in the 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).



92CS-27173

Fig. 1 — Terminal assignment.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

PEAK INVERSE VOLTAGE (PIV) ..... 30 V

PEAK DIODE-TO-SUBSTRATE VOLTAGE ..... 30 V

PEAK FORWARD SURGE CURRENT [I_F (SURGE)] ..... 100 mA

DC FORWARD CURRENT (I_F) ..... 25 mA

DISSIPATION:

Any one diode unit ..... 50 mW

Total Package:

Up to 55° C ..... 650 mW

For $T_A > 55°$ C ..... Derate linearly at 6.67 mW/° C

AMBIENT TEMPERATURE RANGE:

Operating ..... −55 to +125° C

Storage ..... −65 to +150° C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max. ..... +265° C

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTIC	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNIT
DC Forward Voltage Drop, V_F	I_F (Anode)	100 μA	–	0.7	0.9	V
		1 mA	–	0.78	1	
		10 mA	–	0.93	1.2	
DC Reverse Breakdown Voltage, $V_{(BR)R}$	$I_F = -10$ μA		30	50	–	V
DC Breakdown Voltage Between Any Diode and Substrate, $V_{(BR)DI}$	$I_{DI} = 10$ μA		30	50	–	V
DC Reverse (Leakage) Current, I_R	$V_F = -20$ V		–	–	100	nA
DC Reverse (Leakage) Current Between Any Diode and Substrate, I_{DI}	$V_{DI} = 20$ V		–	–	100	nA
Magnitude of Diode Offset Voltage Between Diode Pairs	$V_{DI} = 20$ V, $I_{FA} = 1$ mA		–	0.55	–	mV
Temperature Coefficient of Forward Voltage Drop, $\Delta V_F/\Delta T$	$I_F = 1$ mA		–	−1.5	–	mV/°C
Reverse Recovery Time, t_{rr}	$I_F = 2$ mA, $I_R = 2$ mA		–	50	–	ns
Diode Capacitance, C_D			See Fig. 5			pF
Diode Anode-to-Substrate Capacitance, C_{DAI}			See Fig. 6			pF
Diode Cathode-to-Substrate Capacitance, C_{DCI}			See Fig. 7			pF
Magnitude of Cathode-to-Anode Current Ratio, $\lvert I_{FC}/I_{FA} \rvert$	$I_{FA} = 1$ mA, $V_{DS} = 10$ V		0.9	0.96	–	

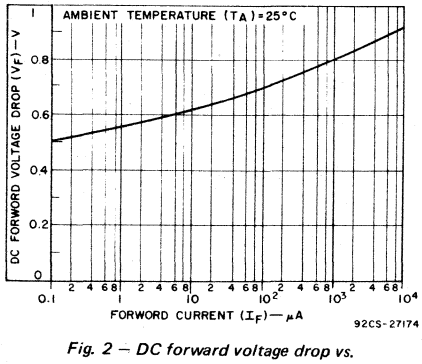


Fig. 2 – DC forward voltage drop vs. forward current.

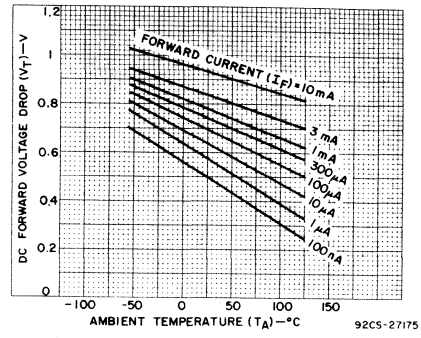


Fig. 3 – DC forward voltage drop vs. ambient temperature.

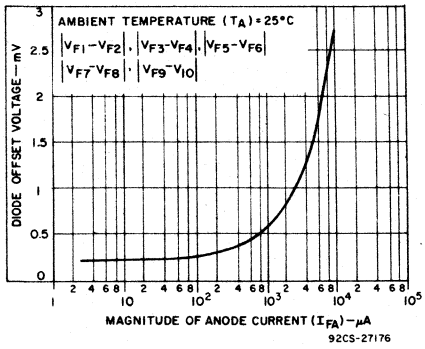


Fig. 4 — Diode offset voltage vs. magnitude of anode current.

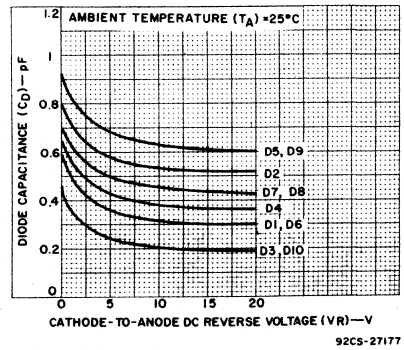


Fig. 5 — Diode capacitance vs. cathode-to-anode reverse voltage.

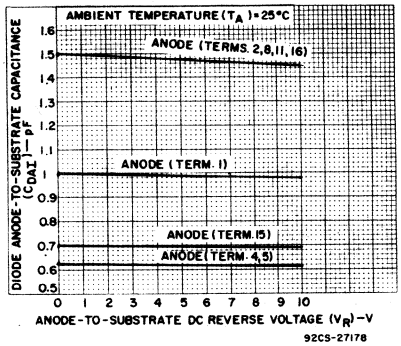


Fig. 6 — Diode anode-to-substrate capacitance vs. reverse voltage.

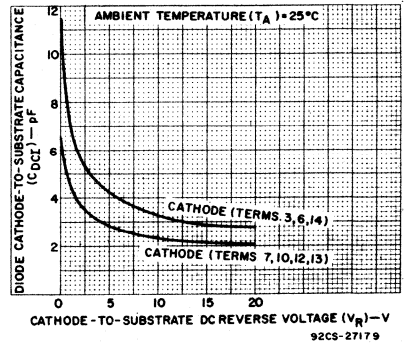


Fig. 7 — Diode cathode-to-substrate capacitance vs. cathode-to-substrate DC reverse voltage.

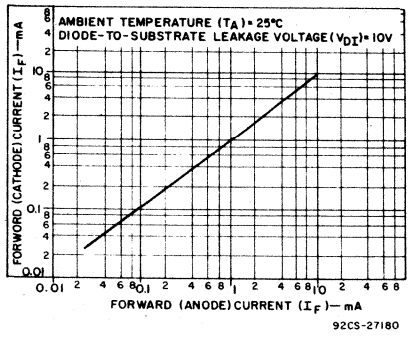


Fig. 8 — Forward (cathode) current vs. forward (anode) current.

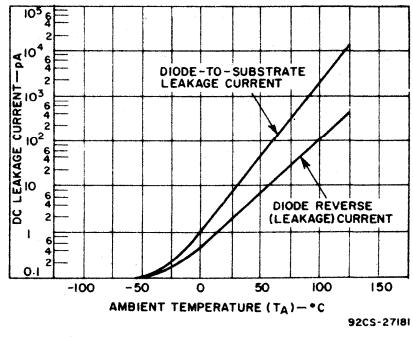
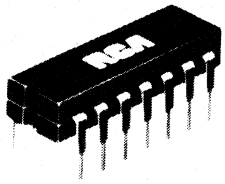


Fig. 9 — DC leakage current vs. ambient temperature.



14-Lead Dual-In-Line
Plastic Package
(E Suffix)
H-1517

High-Current N-P-N Transistor Arrays

Four Individual Sealed-Junction
High-Current N-P-N Transistors

Features:

- **High Current — 1 A**
- **High Breakdown Voltage:**
  CA1725 = 80 V dc min. $V_{(BR)CES}$ @ I_C = 10 μA
  CA1724 = 70 V dc min. $V_{(VR)CES}$ @ I_C = 10 μA

The RCA-CA1724 and -CA1725 are high-current n-p-n transistor arrays each containing 4 individual sealed-junction high-current n-p-n transistors. They are intended for high-current driver applications.

These devices are alike except for breakdown voltage ratings.

The CA1724 and CA1725 are supplied in a 14-lead dual-in-line plastic package and operate over the full military temperature range of −55°C to +125°C.

- **Silicon Nitride Passivated**
- **Platinum Silicide Ohmic Contacts**
- **Electrically similar and pin compatible with industry types MPQ3724, MPQ3725; FPQ3724, FPQ3725; DH3724, DH3725; SP3724, SP3725 in similar packages**

Applications

- **High-Current LED Driver**
- **High-Voltage Switching**
- **Relay and Solenoid Driver**
- **Lamp Driver**

Comparison of High Current N-P-N Arrays

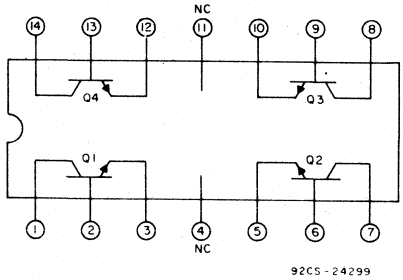
CHARACTERISTIC	CA1725			CA3725			CA3138A		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
V_{CEO}(sus)	50	58	—	50	—	—	15	20	—
$V_{(BR)CBO}$	80	94	—	80	—	—	25	60	—
$V_{(BR)EBO}$	6	6.9	—	6	—	—	5	7.2	—
h_{FE} @ 1A	20	25	—	20	—	—	40	170	—
h_{FE} @ 500 mA	30	35	—	30	—	—	95	170	—
h_{FE} @ 100 mA	35	40	—	35	—	—	80	160	450
V_{CE}(SAT) @ 500 mA	—	0.38	0.5	—	—	0.5	—	0.26	0.4
t_{ON} @ 500 mA	—	38	—	—	—	40	—	31	—
t_{OFF} @ 500 mA	—	185	—	—	—	60	—	105	—
C_{EB}	—	100	—	—	95	—	—	77	—
C_{CB}	—	12.5	—	—	12	—	—	18	—

CA1724, CA1725 Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristic	Test Conditions	LIMITS						Units
		CA1724			CA1725			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector-to-Emitter Sustaining Voltage, $V_{CEO(sus)}$*	I_C = 10 mA, I_B = 0	40	45	—	50	58	—	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$	I_C = 10 μA, I_B = 0	70	75	—	80	94	—	V
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	70	75	—	80	94	—	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	6	6.9	—	6	6.9	—	V
Base-to-Emitter Saturation Voltage, $V_{BE(sat)}$*	I_C = 500 mA, I_B = 50 mA	0.75	0.89	1.0	0.75	0.9	1.0	V
Collector-to-Emitter Saturation Voltage $V_{CE(sat)}$	I_C = 500 mA, I_B = 50 mA	—	0.36	0.5	—	0.38	0.5	V
Collector-Cutoff Current, I_{CBO}	V_{CB} = 40 V, I_E = 0	—	0.3	1.7	—	0.3	1.7	μA
Static Forward-Current Transfer Ratio (Beta), h_{FE}	I_C = 100 mA V_{CE} = 1.0 V I_C = 500 mA, V_{CE} = 1.0 V I_C = A, V_{CE} = 1.0 V	35 30 20	40 35 25	— — —	35 30 20	40 35 25	— — —	
Turn-On Time (See (Test Ckt.Fig.6), t_{on}	I_C = 500 mA, I_{B_1} = 50 mA	—	38	—	—	38	—	ns
Turn-Off Time (See Test Ckt.Fig.6), t_{off}	I_C = 500mA, I_{B_1} = I_{B_2} = 50 mA	—	185	—	—	185	—	ns
Emitter-to-Base Capacitance, C_{eb}	I_C = 0 V_{EB} = 0.5 V	—	102	—	—	100	—	pF
Collector-to-Base Capacitance, C_{cb}	I_E = 0, V_{CB} = 10 V	—	14	—	—	12.5	—	pF

* Pulse Conditions: width = 300 μs; duty cycle = 1%.



92CS-24299

Fig. 1—Terminal diagram (top view).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		CA1724	CA1725	
COLLECTOR-TO-EMITTER VOLTAGE With Base Open	V_{CEO}	40	50	V
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	70	80	V
EMITTER-TO-BASE VOLTAGE With Collector Open	V_{EBO}	6		V
COLLECTOR CURRENT	I_C	1.0		A
POWER DISSIPATION:	P_D			
For Each Transistor		1.0		W
Total Package		2.0		W
At T_A above 25°C derate linearly (Total Package)		20		mw/°C
AMBIENT TEMPERATURE RANGE:				
Operating		−55 to +125		°C
Storage		−65 to +150		°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/32" (3.17 mm) from seating plane for 10 s max.		300		°C

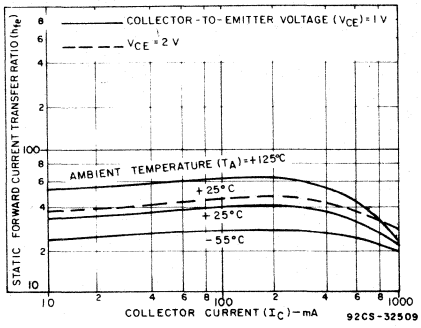


Fig. 2—Static forward current transfer ratio as a function of collector current.

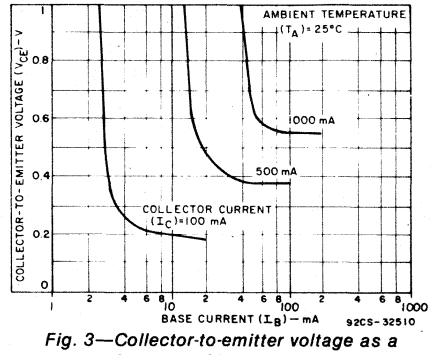


Fig. 3—Collector-to-emitter voltage as a function of base current.

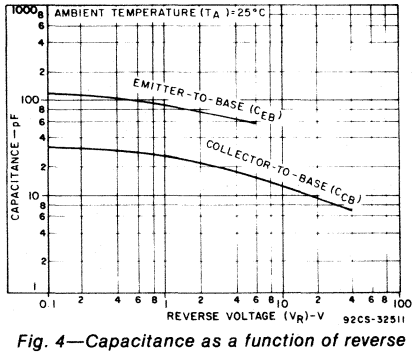


Fig. 4—Capacitance as a function of reverse voltage.

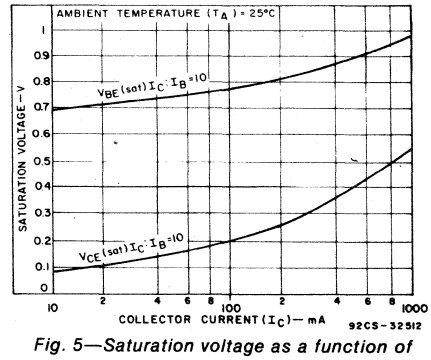


Fig. 5—Saturation voltage as a function of collector current.

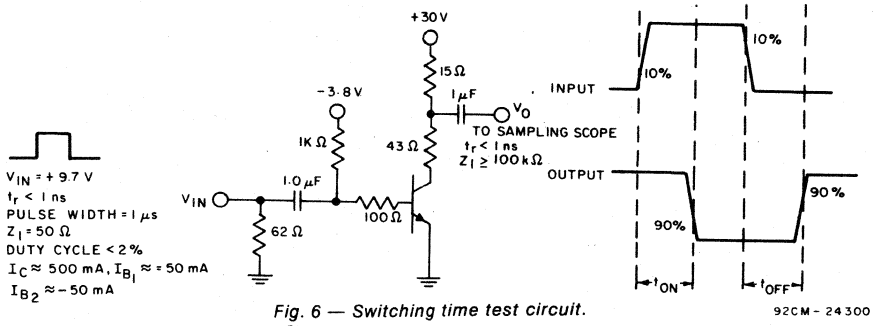


Fig. 6 — Switching time test circuit.

CA3018, CA3018A

12-Lead TO-5

H-1463

General-Purpose Transistor Arrays

Two Isolated Transistors and
a Darlington-Connected Transistor Pair

For Low-Power Applications at Frequencies
from DC Through the VHF Range

Features:

- *Matched monolithic general purpose transistors*
- *H_{FE} matched ± 10%*
- *V_{BE} matched ± 2 mV CA3018A (± 5m V CA3018)*
- *Operation from DC to 120 MHz*
- *Wide operating current range*
- *CA3018A performance characteristics controlled from 10 μA to 10 mA*
- *Low noise figure - 3.2 dB typical at 1KHz*
- *Full military temperature range capability (−55 to +125° C)*

Applications

- *General use in signal processing systems in DC through VHF range*
- *Custom designed differential amplifiers*
- *Temperature compensated amplifiers*
- *See RCA Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated-Circuit Transistor Array" for suggested applications.*

The CA3018 and CA3018A consist of four general purpose silicon n-p-n transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low-power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

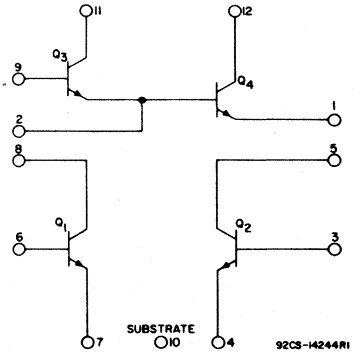


Fig. 1 — Schematic Diagram for CA3018 and CA3018A

CA3018, CA3018A

Maximum Ratings, Absolute-Maximum Values, at TA=25°C

	CA3018	CA3018A	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	450	450	mW
Derate at 5 mW/°C for $T_A > 85°C$			
Temperature Range:			
Operating	-55 to + 125	-55 to + 125	°C
Storage	-65 to + 150	-65 to + 150	°C

The following ratings apply for each transistor in the device:

	CA3018	CA3018A	
Collector-to-Emitter Voltage, V_{CEO}	15	15	V
Collector-to-Base Voltage, V_{CBO}	20	30	V
Collector-to-Substrate Voltage, V_{CIO}*	20	40	V
Emitter-to-Base Voltage, V_{EBO}	5	5	V
Collector Current, I_C	50	50	mA

*The collector of each transistor of the CA3018 and CA3018A is isolated from the substrate by an integral diode. *The substrate (terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

Characteristics apply for each transistor in the CA3018 and CA3018A as specified.

ELECTRICAL CHARACTERISTICS at T_A = 25°C	SYMBOLS	SPECIAL TEST CONDITIONS	CA3018 LIMITS			CA3018A LIMITS			Units	CHARACTERISTICS CURVES
			Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS										
Collector-Cutoff Current	I_{CBO}	V_{CB}=10V, I_E=0	–	0.002	100	–	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE}=10V, I_B=0	–	See Curve	5	–	See Curve	0.5	μA	3
Collector-Cutoff Current Darlington Pair	I_{CEOD}	V_{CE}=10V, I_B=0	–	–	–	–	–	5	μA	–
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	15	24	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10μA, I_E=0	20	60	–	30	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=10μA, I_C=0	5	7	–	5	7	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C=10μA, I_{CI}=0	20	60	–	40	60	–	V	–
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B=1mA, I_C=10mA	–	0.23	–	–	0.23	0.5	V	–
Static Forward Current Transfer Ratio	h_{FE}	V_{CE}=3V, I_C=10mA V_{CE}=3V, I_C=1mA V_{CE}=3V, I_C=10μA	– 30 –	100 100 54	– 200 –	50 60 30	100 100 54	– 200 –	– – –	4
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)		V_{CE}=3V, I_{C1}=I_{C2}=1mA	0.9	0.97	–	0.9	0.97	–	–	4
Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	h_{FED}	V_{CE}=3V I_C=1mA V_{CE}=3V I_C=100μA	1500 –	5400 –	– –	2000 1000	5400 2800	– –	–	5
Base-to-Emitter Voltage	V_{BE}	V_{CE}=3V I_E=1mA V_{CE}=3V I_E=10mA	– –	0.715 0.800	– –	0.600 –	0.715 0.800	0.800 0.900	V	6
Input Offset Voltage	$\lvert V_{BE_1} - V_{BE_2} \rvert$	V_{CE}=3V, I_E=1mA	–	0.48	5	–	0.48	2	mV	6,8
Temperature Coefficient: Base-to-Emitter Voltage Q_1,Q_2	$\frac{\lvert \Delta V_{BE} \rvert}{\Delta T}$	V_{CE}=3V, I_E=1mA	–	-1.9	–	–	-1.9	–	mV/°C	7
Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	V_{BED} (V_{9-1})	V_{CE}=3V I_E=10mA V_{CE}=3V I_E=1mA	– –	1.46 1.32	– –	– 1.10	1.46 1.32	1.60 1.50	V	9
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3,Q_4	$\frac{\lvert \Delta V_{BED} \rvert}{\Delta T}$	V_{CE}=3V, I_E=1mA	–	4.4	–	–	4.4	–	mV/°C	10
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert V_{BE_1} - V_{BE_2} \rvert}{\Delta T}$	V_{CC}=+6V, V_{EE}=-6V, I_{C1}=I_{C2}=1mA	–	10	–	–	10	–	μV/°C	–

CA3018, CA3018A

ELECTRICAL CHARACTERISTICS, (CONT'D)

DYNAMIC CHARACTERISTICS										
Low Frequency Noise Figure	NF	f=1 KHz, V_{CE}=3V, I_C=100μA Source resistance=1 KΩ	–	3.25	–	–	3.25	–	dB	11(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Forward Current-Transfer Ratio	h_{fe}	f=1kHz, V_{CE}=3V, I_C=1mA	–	110	–	–	110	–	–	12
Short-Circuit Input Impedance	h_{ie}		–	3.5	–	–	3.5	–	KΩ	12
Open-Circuit Output Impedance	h_{oe}		–	15.6	–	–	15.6	–	μmho	12
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		–	$1.8x10^{-4}$	–	–	$1.8x10^{-4}$	–	–	12
Admittance Characteristics:										
Forward Transfer Admittance	Y_{fe}	f=1MHz, V_{CE}=3V, I_C=1mA	–	31-j1.5	–	–	31-j1.5	–	mmho	13
Input Admittance	Y_{ie}		–	0.3+j0.04	–	–	0.3+j0.04	–	mmho	14
Output Admittance	Y_{oe}		–	0.001+j0.03	–	–	0.001+j0.03	–	mmho	15
Reverse Transfer Admittance	Y_{re}		See Curve			See Curve			mmho	16
Gain-Bandwidth Product	f_T	V_{CE}=3V, I_C=3mA	300	500	–	300	500	–	MHz	17
Emitter-to-Base Capacitance	C_{EB}	V_{EB}=3V, I_E=0	–	0.6	–	–	0.6	–	pF	–
Collector-to-Base Capacitance	C_{CB}	V_{CB}=3V, I_C=0	–	0.58	–	–	0.58	–	pF	–
Collector-to-Substrate Capacitance	C_{CI}	V_{CI}=3V, I_C=0	–	2.8	–	–	2.8	–	pF	–

STATIC CHARACTERISTICS

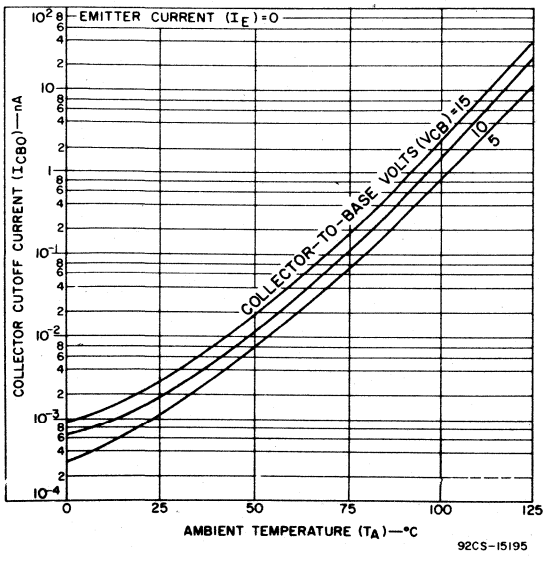


Fig.2 - Typical Collector-To-Base Cutoff Current vs Ambient Temperature for Each Transistor.

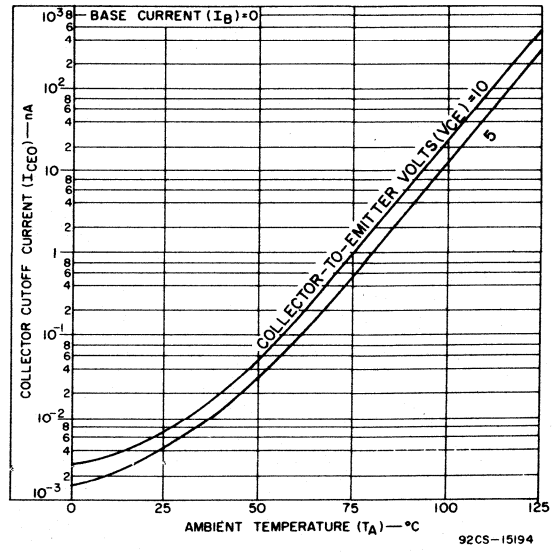


Fig.3 - Typical Collector-To-Emmiter Cutoff Current vs Ambient Temperature for Each Transistor.

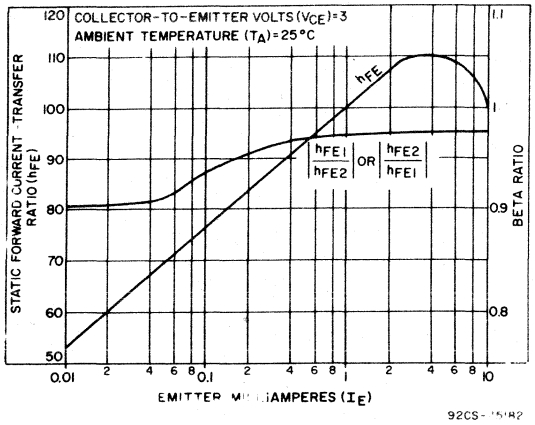


Fig.4 - Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q, and Q_2 vs Emitter Current.

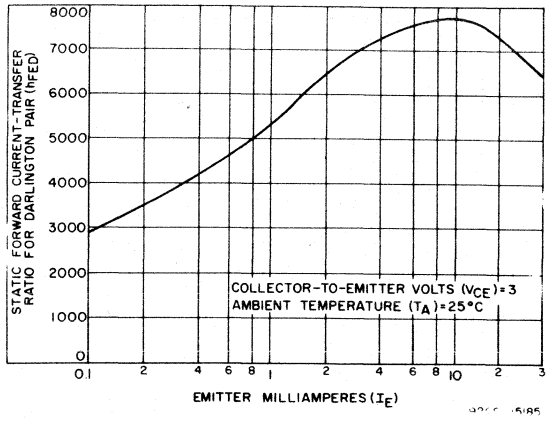


Fig.5 - Typical Static Forward Current - Transfer Ratio for Darlington-connected Transisters Q_3 and Q_4 vs Emitter Current.

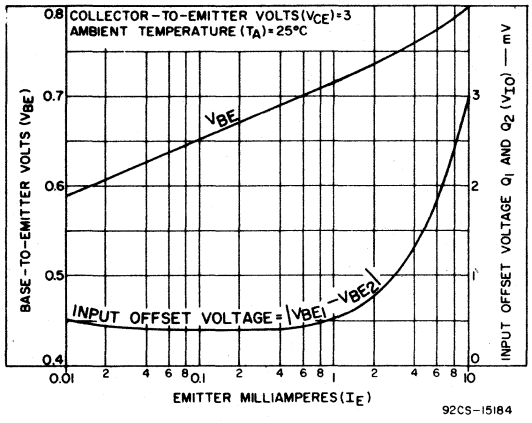


Fig.6 - Typical Static Base-to-Emitter Voltage Characteristic and Input Offset Voltage for Q_1 and Q_2 vs Emitter Current.

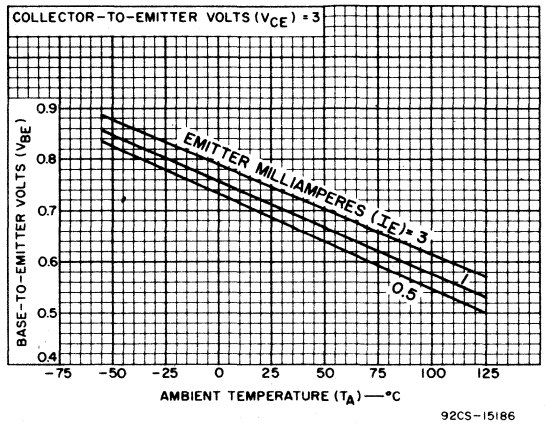


Fig.7 - Typical Base-To-Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature

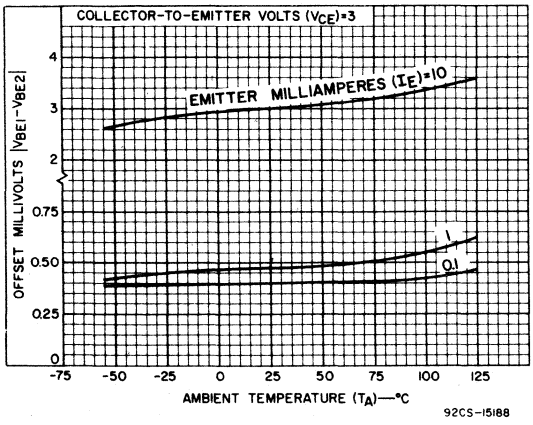


Fig.8 - Typical Offset Voltage Characteristic vs Ambient Temperature

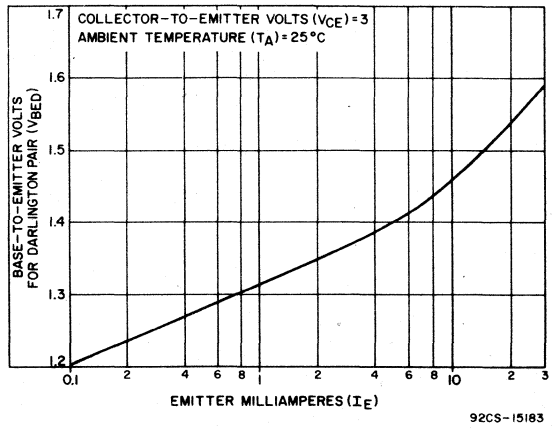


Fig.9 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Emitter Current

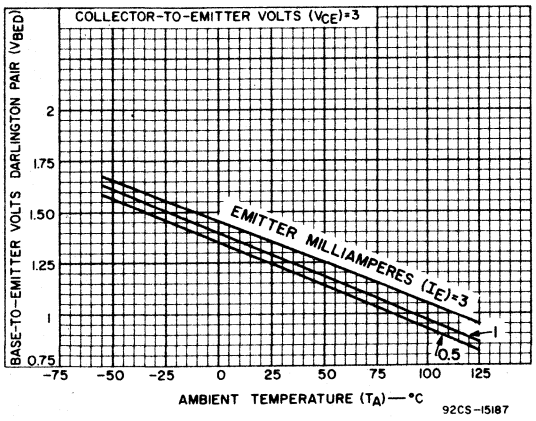


Fig.10 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Ambient Temperature.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

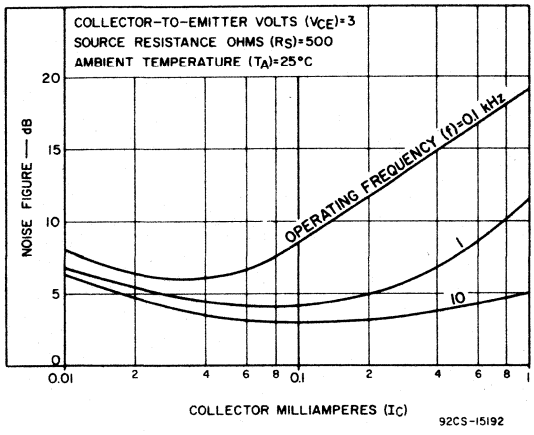


Fig.11(a) - Noise Figure vs Collector Current, R_S = 500 Ω.

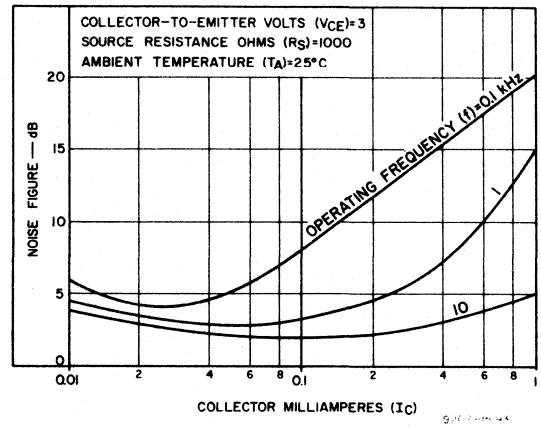


Fig.11(b) - Noise Figure vs Collector Current, R_S = 1 KΩ.

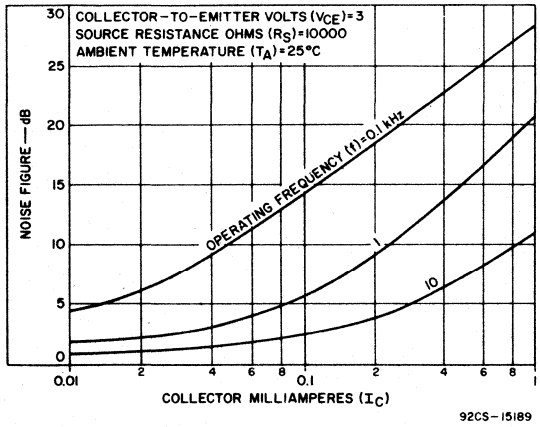


Fig.11(c) - Noise Figure vs Collector Current, R_S = 10 KΩ.

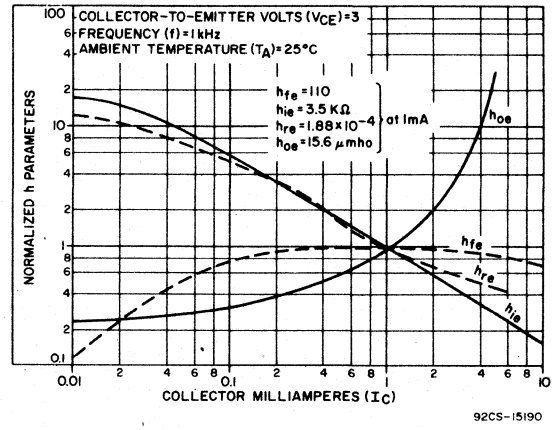


Fig.12 - Forward Current-Transfer Ratio (h_{fe}), Short-Circuit Input Impedance (h_{ie}), Open-Circuit Output Impedance (h_{oe}), and Open-Circuit Reverse Voltage-Transfer Ratio (h_{re}) vs Collector Current

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

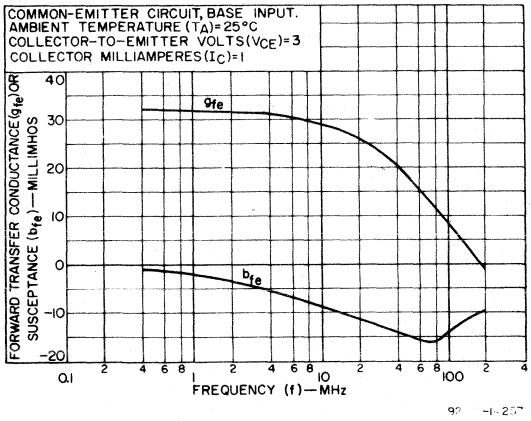


Fig. 13 - Forward Transfer Admittance (Y_{fe})

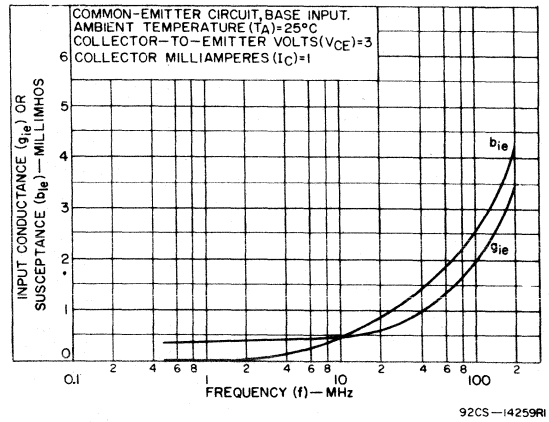


Fig. 14 - Input Admittance (Y_{ie})

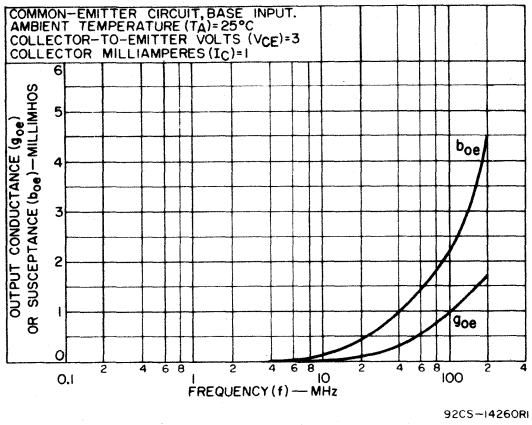


Fig. 15 - Output Admittance (Y_{oe})

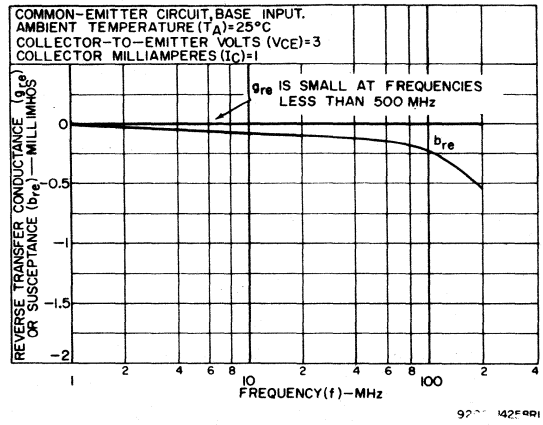


Fig. 16 - Reverse Transfer Admittance (Y_{re})

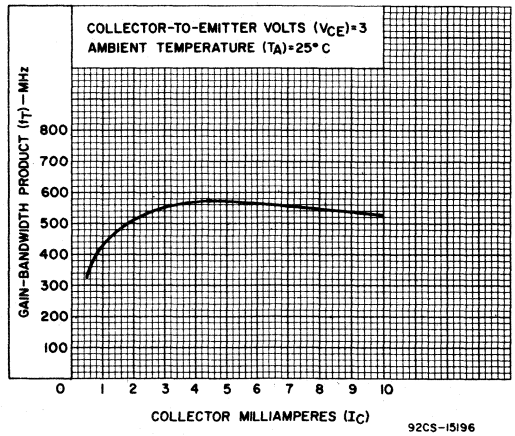
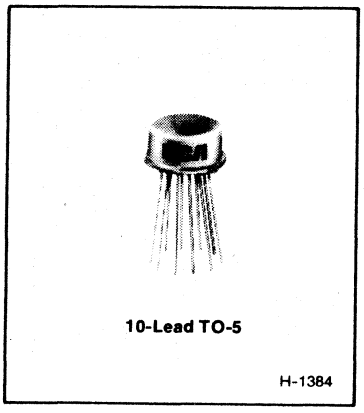


Fig. 17 - Typical Gain-Bandwidth Product (f_T) vs Collector Current

CA3036



10-Lead TO-5

H-1384

Dual Darlington Array

Features

- *Two independent low-noise wide-band amplifier channels*
- *Particularly useful for preamplifier and low-level amplifier applications in single-channel and stereo systems*
- *Wide application in low-noise industrial instrumentation amplifiers*

Applications

- *Stero phonograph preamplifiers*
- *Low-level stereo and single-channel amplifier stages*
- *Low-noise, emitter-follower differential amplifiers*
- *Operational amplifier drivers*

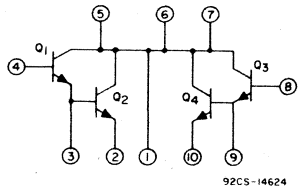


Fig. 1 - Schematic diagram for CA3036.

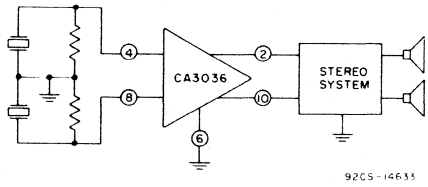


Fig. 2 - Block diagram of stereo system using CA3036 as phono preamplifier.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

POWER DISSIPATION, P:
- ANY ONE TRANSISTOR ..... 300 max. mW
- TOTAL FOR ARRAY ..... 300 max. mW

TEMPERATURE RANGE:
- OPERATING ..... −55 to +125°C
- STORAGE ..... − 65 to +200°C

THE FOLLOWING RATINGS APPLY FOR EACH TRANSISTOR IN THE ARRAY:
- COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO} ..... 15 max. V
- COLLECTOR-TO-BASE VOLTAGE, V_{CBO} ..... 30 max. V
- EMITTER-TO-BASE VOLTAGE, V_{EBO} ..... 5 max. V
- COLLECTOR CURRENT, I_C ..... 50 max. mA

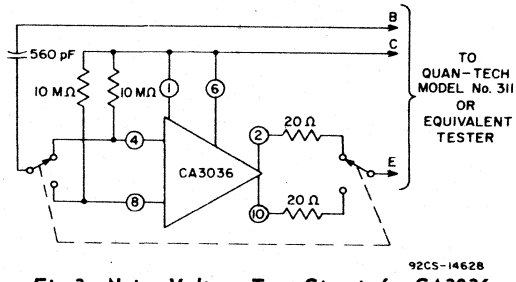


Fig.3 - Noise Voltage Test Circuit for CA3036.

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$

CHARACTERISTICS		SYMBOLS	TEST CONDITIONS	LIMITS TYPE CA3036			UNITS
				Min.	Typ.	Max.	
For Each Transistor (Q_1, Q_2, Q_3, Q_4)	Collector-Cutoff Current	I_{CBO}	$V_{CB} = 5V$, $I_E = 0$	--	--	0.5	μA
	Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	--	--	5	μA
	Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	15	20	--	V
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\ \mu A$, $I_E = 0$	30	44	--	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\ \mu A$, $I_C = 0$	5	6	--	V
For Either Input Transistor (Q_1 or Q_3)	Static Forward Current-Transfer Ratio	h_{FE}	I_{C1} or $I_{C3} = 1$ mA	30	82	--	--
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO(D)}$	I_{E2} or $I_{E4} = 10\ \mu A$	10	12.6	--	V
	Static Forward Current-Transfer Ratio	$h_{FE(D)}$	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ $= 1$ mA	1000	4540	--	--
For Each Input Transistor (Q_1 or Q_3)	Short-Circuit Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, I_{C1} or $I_{C3} = 1$ mA	--	82	--	--
	Short-Circuit Input Impedance	h_{ie}		--	2.6K	--	Ω
	Open-Circuit Output Admittance	h_{oe}		--	7	--	μmho
	Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		--	9.8×10^{-5}	--	--
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Short-Circuit Forward Current-Transfer Ratio	$h_{fe(D)}$	f = 1 kHz, $I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ $= 1$ mA	--	1300	--	--
	Short-Circuit Input Impedance	$h_{ie(D)}$		--	82K	--	Ω
	Open-Circuit Output Admittance	$h_{oe(D)}$		--	108	--	μmho
	Open-Circuit Reverse Voltage-Transfer Ratio	$h_{re(D)}$		--	2.7×10^{-3}	--	--
	Voltage Gain	$A_{(D)}$		--	26	--	dB
	Power Gain	$G_{p(D)}$		--	47	--	dB
	Noise Voltage See Fig.3 for Test Circuit	E_N	f = 100 Hz	--	0.2	3	$\frac{\mu V(rms)}{\sqrt{f(Hz)}}$
			f = 1 kHz	--	0.05	0.3	
			f = 10 kHz	--	0.012	0.1	
For Either Input Transistor (Q_1 or Q_3)	Forward Transfer Admittance	y_{fe}	f = 50 MHz, I_{C1} or $I_{C3} = 2$ mA	--	0.68 + j 7.9	--	mmho
	Input Admittance (Output Short-Circuited)	y_{ie}		--	4.14 + j 5.95	--	mmho
	Output Admittance (Input Short-Circuited)	y_{oe}		--	1.94 + j 2.64	--	mmho
	Reverse Transfer Admittance (Input Short-Circuited)	y_{re}		--	Negligible	--	mmho
For either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Input Admittance (Output Short-Circuited)	$y_{ie(D)}$	f = 50 MHz, $I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ $= 2$ mA	--	1.71 + j 2.8	--	mmho
	Output Admittance (Input Short-Circuited)	$y_{oe(D)}$		--	3.96 + j 2.6	--	mmho
	Gain-Bandwidth Product	$f_{T(D)}$		150	200	--	MHz

CA3045, CA3046 Types

14-Lead Dual-In-Line Ceramic

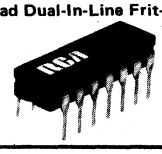
H-1553

14-Lead Dual-In-Line Plastic

H-1517

14-Lead Dual-In-Line Frit-Seal

Hermetic Package



H-1806

General-Purpose Transistor Arrays

THREE ISOLATED TRANSISTORS AND ONE DIFFERENTIALLY-CONNECTED TRANSISTOR PAIR

For Low-Power Applications at Frequencies from DC through the VHF Range

Features

- Two matched pairs of transistors
  V_{BE} matched ± 5 mV
  Input offset current 2 μA max. at I_C = 1 mA
- 5 general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure - - 3.2 dB typ. at 1 kHz
- Full military temperature range for CA3045
  -55 to +125°C

The CA3045 and CA3046 each consist of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

The CA3045 is supplied in a 14-lead dual-in-line hermetic (welded-seal) ceramic package and the CA3045F in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

The CA3046 is electrically identical to the CA3045 but is supplied in a dual-in-line plastic package for applications requiring only a limited temperature range.

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.

The CA3045 and CA3046 are available in the packages shown below

Package	Suffix Letter	CA3045	CA3046
14-Lead Dual-In-Line Plastic	E		√
14-Lead Dual-In-Line Ceramic	D	√	
14-Line Dual-In-Line Frit-Seal Ceramic	F	√	
Beam Lead	L	√	
Chip	H	√	

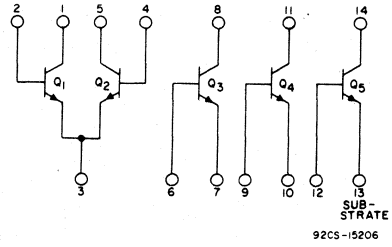


Fig.1 - Schematic diagram.

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C	CA3045		CA3046, CA3045F		
	Each Transistor	Total Package	Each Transistor	Total Package	
Power Dissipation:					
T_A up to 55°C	–	–	300	750	mW
T_A > 55°C	–	–	Derate at 6.67		mW/°C
T_A up to 75°C	300	750	–	–	mW
T_A > 75°C	Derate at 8		–	–	mW/°C
Collector-to-Emitter Voltage, V_{CEO}	15	–	15	–	V
Collector-to-Base Voltage, V_{CBO}	20	–	20	–	V
Collector-to-Substrate Voltage, V_{CIO}*	20	–	20	–	V
Emitter-to-Base Voltage, V_{EBO}	5	–	5	–	V
Collector Current	50	–	50	–	mA
Temperature Range:					
Operating	–55 to +125		–55 to +125		°C
Storage	–65 to +150		–65 to +150		°C
Lead Temperature (During Soldering): At distance 1/16 ±1/32" (1.59 ±0.79 mm) from case for 10 seconds max.	+265		+265		°C

* The collector of each transistor of the CA3045 and CA3046 is isolated from the substrate by an integral diode. *The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046 MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES FIG.
STATIC CHARACTERISTICS							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60	-	V	-
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7	-	V	-
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	-	See curve	0.5	μA	3
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE}	V_{CE} = 3 V, I_C = 10 mA	-	100	-	-	4
		V_{CE} = 3 V, I_C = 1 mA	40	100	-	-	
		V_{CE} = 3 V, I_C = 10 μA	-	54	-	-	
Input Offset Current for Matched Pair Q_1 and Q_2. $\lvert I_{IO_1} - I_{IO_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.3	2	μA	5
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_E = 1 mA	-	0.715	-	V	6
		V_{CE} = 3 V, I_E = 10 mA	-	0.800	-		
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV	6,8
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV	6,8
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	-1.9	-	mV/°C	7
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1 mA, I_C = 10 mA	-	0.23	-	V	-
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	1.1	-	μV/°C	8

CA3045, CA3046 Types

ELECTRICAL CHARACTERISTICS (Cont'd.)

DYNAMIC CHARACTERISTICS							
Low-Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA Source Resistance = 1 kΩ	-	3.25	-	dB	9(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:							
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	110	-	-	10
Short-Circuit Input Impedance	h_{ie}		-	3.5	-	kΩ	
Open-Circuit Output Impedance	h_{oe}		-	15.6	-	μmho	
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	1.8×10^{-4}	-	-	
Admittance Characteristics:							
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	-	31-j1.5	-	-	11
Input Admittance	Y_{ie}		-	0.3+j0.04	-	-	12
Output Admittance	Y_{oe}		-	0.001+j0.03	-	-	13
Reverse Transfer Admittance	Y_{re}		-	See curve	-	-	14
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	550	-	-	15
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	-	0.6	-	pF	-
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	-	0.58	-	pF	-
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	-	2.8	-	pF	-

STATIC CHARACTERISTICS

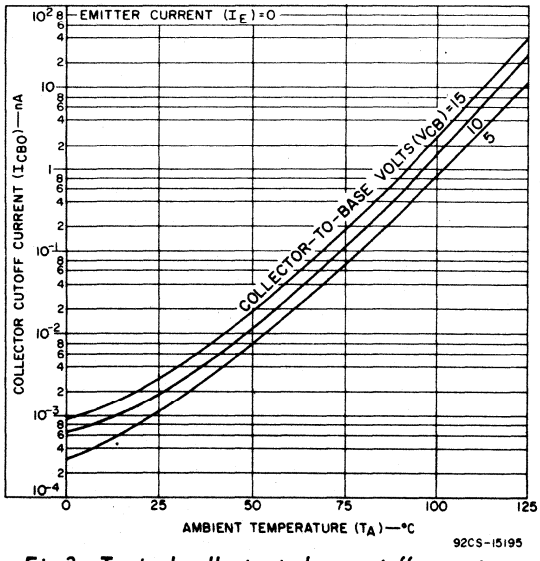


Fig.2 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

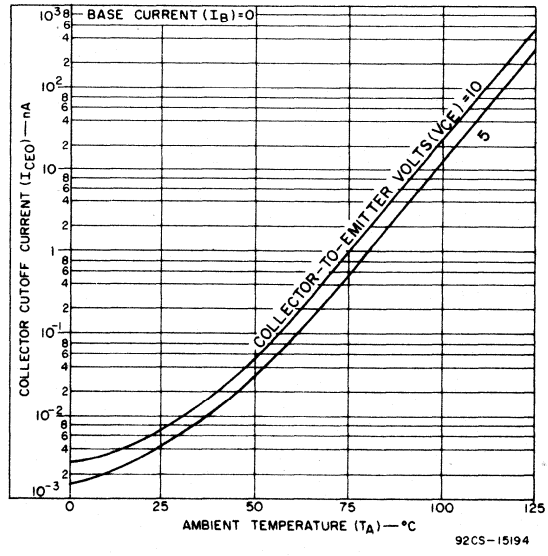


Fig.3 - Typical collector-to-emitter cutoff current vs ambient temperature for each transistor.

STATIC CHARACTERISTICS

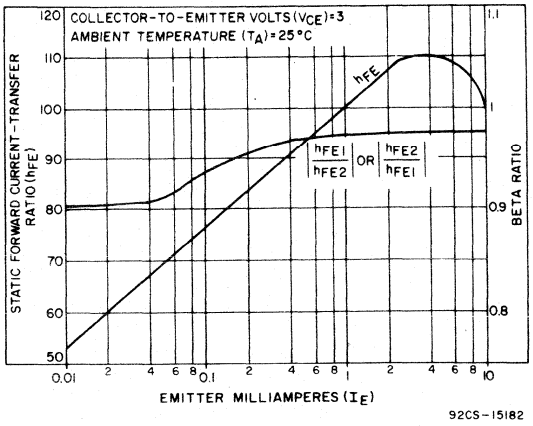


Fig.4 - Typical static forward current-transfer ratio and beta ratio for transistors Q_1 and Q_2 vs emitter current.

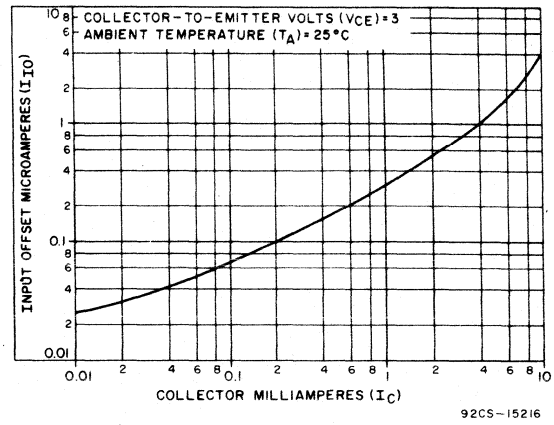


Fig.5 - Typical input offset current for matched transistor pair Q_1Q_2 vs collector current.

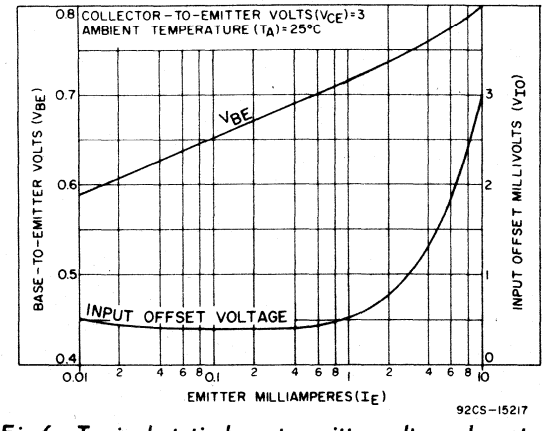


Fig.6 - Typical static base-to-emitter voltage characteristic and input offset voltage for differential pair and paired isolated transistors vs emitter current.

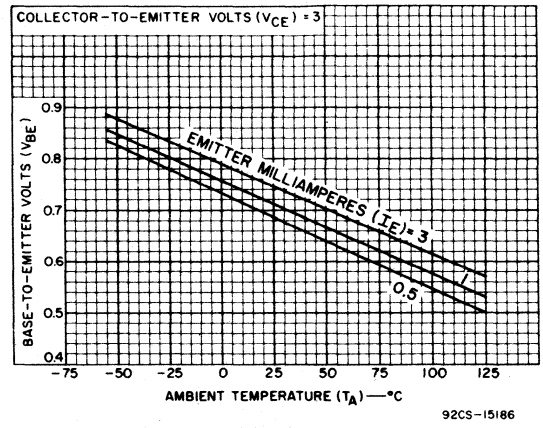


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

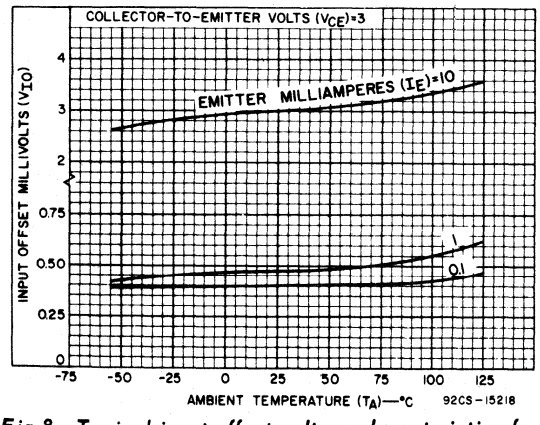


Fig.8 - Typical input offset voltage characteristics for differential pair and paired isolated transistors vs ambient temperature.

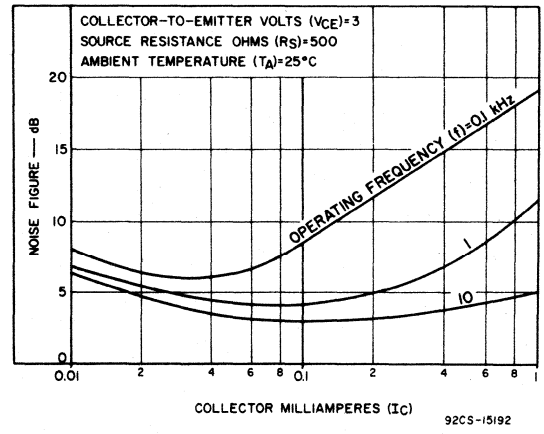


Fig.9(a) - Typical noise figure vs collector current.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

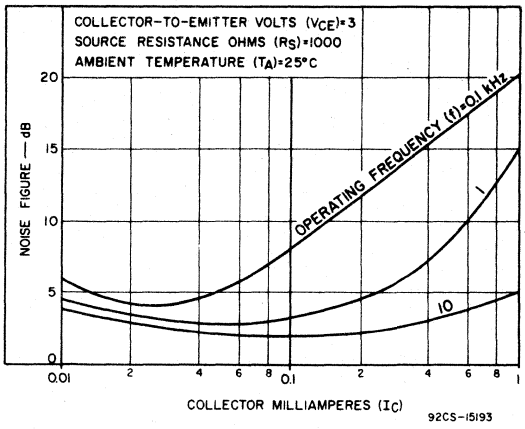


Fig.9(b) - Typical noise figure vs collector current.

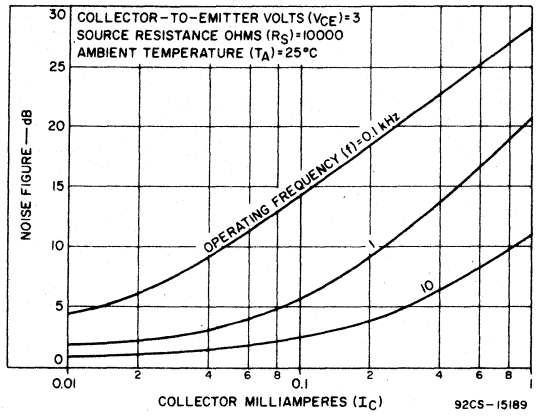


Fig.9(c) - Typical noise figure vs collector current.

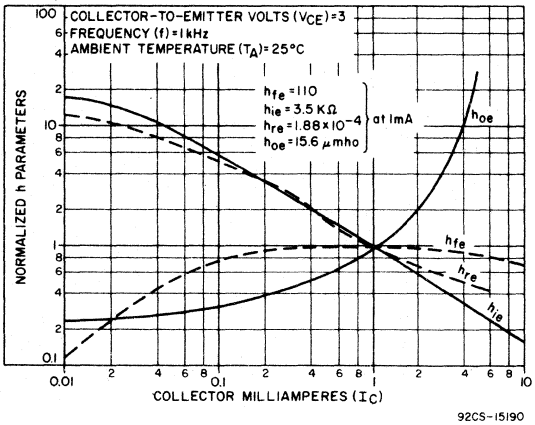


Fig.10 - Typical normalized forward current-transfer ratio, short-circuit input impedance, open-circuit output impedance, and open-circuit reverse voltage-transfer ratio vs collector current.

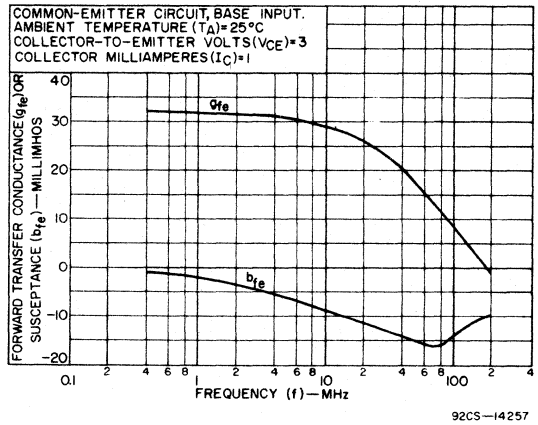


Fig.11 - Typical forward transfer admittance vs frequency.

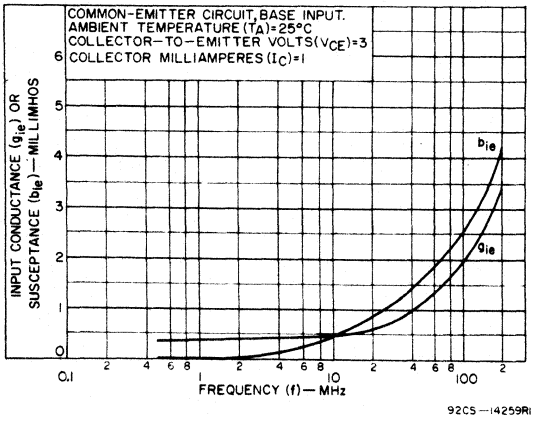


Fig.12 - Typical input admittance vs frequency.

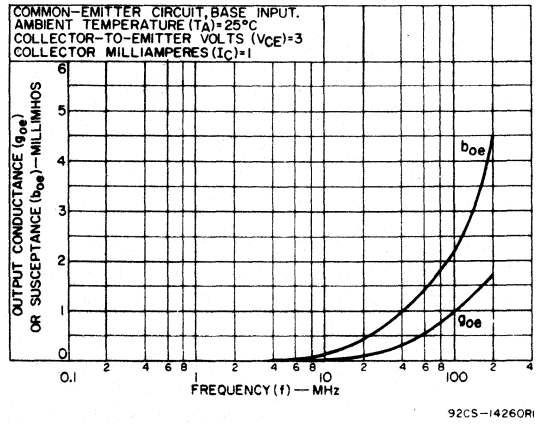


Fig.13 - Typical output admittance vs frequency.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

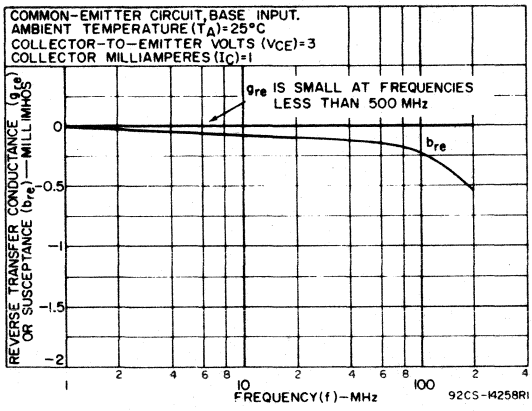


Fig.14 - Typical reverse transfer admittance vs frequency.

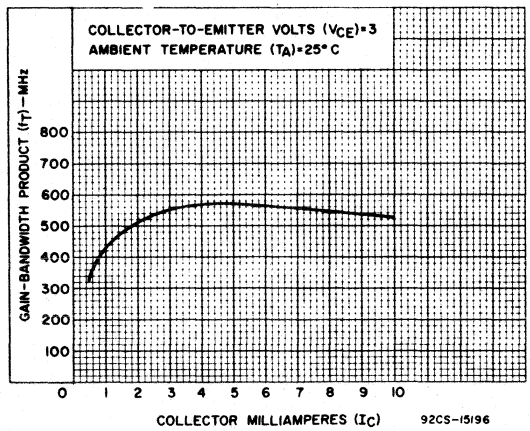
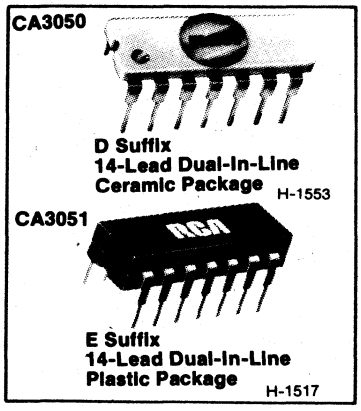


Fig.15 - Typical gain-bandwidth product vs collector current.

CA3050, CA3051



Dual Differential Amplifiers

Two Darlington-Connected Differential Amplifiers with Diode Bias String

For Low-Power Applications at Frequencies from DC to 20 MHz

Features:

- *Input offset current - 70 nA max.*
- *Input bias current - 500 nA max.*
- *Input offset voltage - 5 mV max.*
- *Input impedance - 460 kΩ typ.*
- *Independently accessible inputs and outputs*

Applications

- *Matched dual amplifiers*
- *Dual sense amplifiers*
- *Dual Schmitt triggers*
- *Dual multivibrators*
- *Doubly balanced detectors and modulators*
- *Balanced quadrature detectors*
- *Synthesizer mixers*
- *Product detectors*

The CA3050 and CA3051 each consists of two differential amplifiers with associated constant current transistors on a common substrate. Each amplifier is driven by Darlington-connected emitter follower inputs to provide high input impedance, low bias current, and low offset current. A string of diodes is included to provide temperature-compensated bias to the constant current transistors and a low impedance bias point for the inputs to the differential amplifiers when a single power supply is used.

The CA3050 is supplied in an hermetic 14-lead Dual-In-Line ceramic package rated for operation over the full military temperature range of −55°C to +125°C.

The CA3051 is supplied in a Dual-In-Line plastic package for applications requiring only a limited temperature range of −25°C to +85°C.

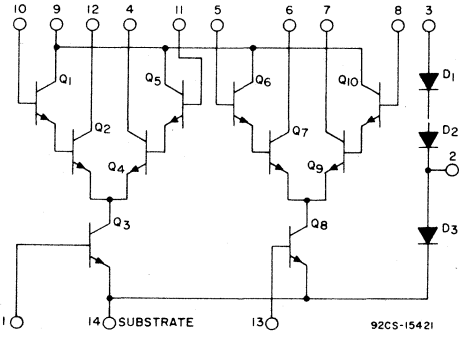


Fig. 1 — Schematic diagram.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C

	CA3050	CA3051	
Power Dissipation, P:			
Any one transistor	150	150	mW
Total package	900	750	mW
For T_A > 55°C, Derate at	8	6.67	mW/°C
Temperature Range:			
Operating	-55 to +125	-40 to +85	°C
Storage	-65 to +150	-65 to +150	°C
LEAD TEMPERATURE (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C		

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3050 and CA3051 is isolated from the substrate by an integral diode. *The substrate (terminal 14) must be more negative than all collectors to maintain isolation between transistors and to provide for normal transistor action.*

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 3 is +5 to -2 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	–	*	*	*	*	*	*	*	*	*	*	*	*	+1 -5
2			+5 -2	*	*	*	*	*	*	*	*	*	*	+1 -1
3				*	*	*	*	*	*	*	*	*	*	+3 -1
4					*	*	*	*	*	+14 -2.5 Note 3	+14 -2.5 Note 4	*	*	+20 -1
5						+2.5 -14 Note 1	+2.5 -14 Note 1	+10 -10	+1 -20	*	*	*	*	+16 -
6							*	+14 -2.5 Note 2	*	*	*	*	*	+20 -1
7								+14 -2.5 Note 2	*	*	*	*	*	+20 -1
8									+1 -20	*	*	*	*	+16 -
9										+20 -1	+20 -1	*	*	+20 -1
10											+10 -10	+2.5 -14 Note 3	*	+16 -
11												+2.5 -14 Note 4	*	+16 -
12														+20 -1
13														+1 -5
14														Ref. Substrate

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	0.1
2	50	50
3	50	1
4	50	1
5	5	0.1
6	50	1
7	50	1
8	5	0.1
9	50	1
10	5	0.1
11	5	0.1
12	50	1
13	5	0.1
14	100	5

Note 1: This rating is important only when terminal 5 is more positive than terminal 8.

Note 2: This rating is important only when terminal 8 is more positive than terminal 5.

Note 3: This rating is important only when terminal 10 is more positive than terminal 11.

Note 4: This rating is important only when terminal 11 is more positive than terminal 10.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

CA3050, CA3051

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	LIMITS CA3050/CA3051			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC								
Amplifier Characteristics								
Input Offset Voltage	V_{IO}		–	–	1.5	5	mV	2a,b
Input Offset Current	I_{IO}		–	–	7	70	nA	3a,b
Input Bias Current	I_I		–	–	200	500	nA	4a,b
Quiescent Operating Current Ratio	$\frac{(I_4+I_{12})}{I_3}$ or $\frac{(I_6+I_7)}{I_3}$	V_{CC} = + 6 V, I_3 = 2 mA	–	0.9	1.00	1.13	–	5a,b
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 50 μA	–	–	0.645	0.700	V	6
		V_{CE} = 3 V, I_C = 1 mA	–	–	0.725	0.800		
		V_{CE} = 3 V, I_C = 3 mA	–	–	0.760	0.850		
		V_{CE} = 3 V, I_C = 10 mA	–	–	0.805	0.900		
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	–	–	-1.9	–	mV/°C	7
Transistor Characteristics								
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	0.002	100	nA	8
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V	–
DYNAMIC								
Transistor Characteristics								
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	–	–	0.78	–	pF	9
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	–	–	0.47	–	pF	9
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	–	–	1.92	–	pF	9
Amplifier Characteristics								
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 5 V, I_C = 3 mA	–	–	600	–	MHz	10
Forward Transadmittance (With single-ended input and output)	$\lvert y_{21} \rvert$	V_{CC} = 10 V, I_3 = 2 mA, f = 1 MHz	11	7	9	11	mmho	11
Bandwidth at -3 dB Point	BW	V_{CC} = 10 V, I_3 = 2 mA	11	–	4.3	–	MHz	11
Input Impedance	Z_{IN}	V_{CC} = 10 V, I_3 = 2 mA, f = 1 KHz	12	–	460	–	kΩ	12
Output Impedance	Z_{OUT}	I_3 = 2 mA, f = 1 KHz	13	–	170	–	kΩ	13
Common-Mode Rejection Ratio	CMR	I_3 = 2 mA, f = 1 KHz	–	–	65	–	dB	–
AGC Range	AGC	I_3 = 2 mA, f = 1 KHz Terminal No.3 Grounded	11	–	60	–	dB	–

TYPICAL STATIC CHARACTERISTICS

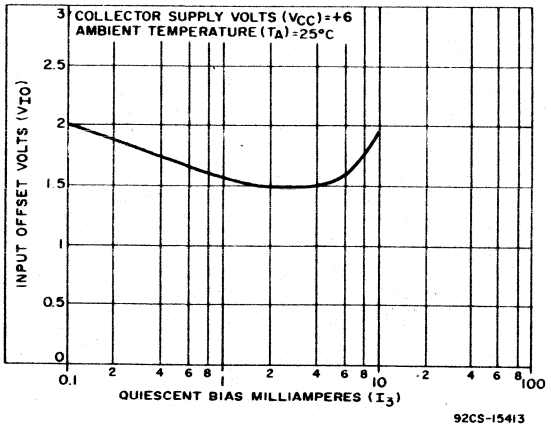


Fig.2(a) - Typical input offset voltage vs quiescent bias current.

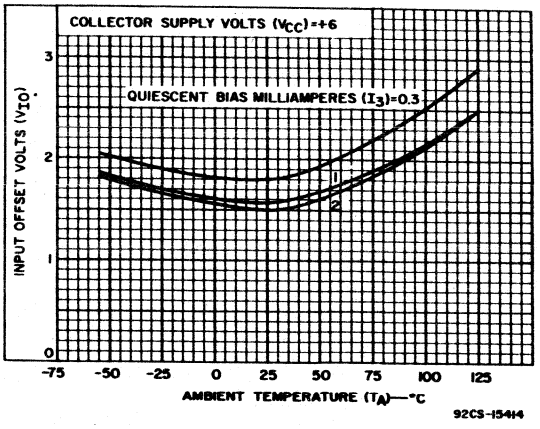


Fig.2(b) - Typical input offset voltage vs ambient temperature.

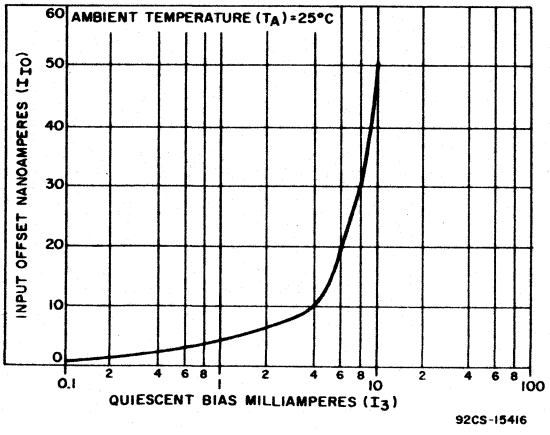


Fig.3(a) - Typical input offset current vs quiescent bias current.

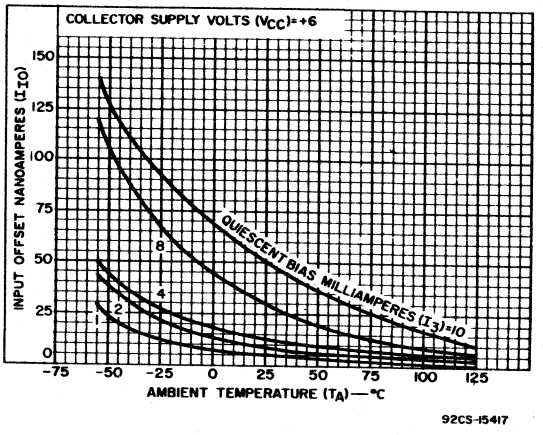


Fig.3(b) - Typical input offset current vs ambient temperature.

STATIC CHARACTERISTICS

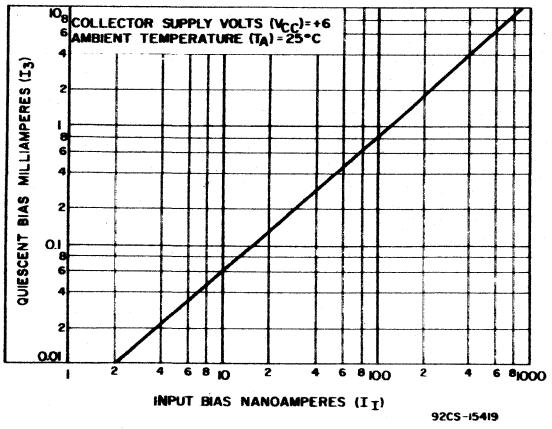


Fig.4(a) - Typical quiescent bias current vs input bias current.

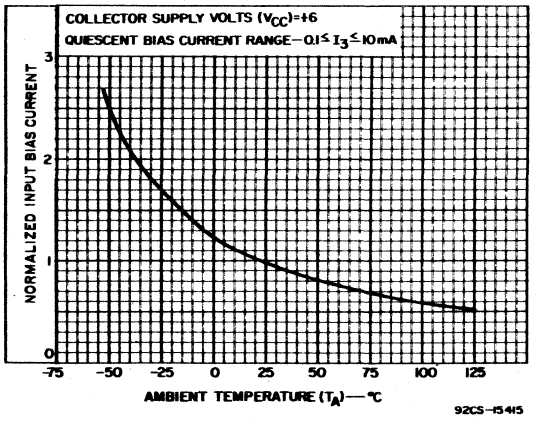


Fig.4(b) - Typical normalized input bias current vs ambient temperature.

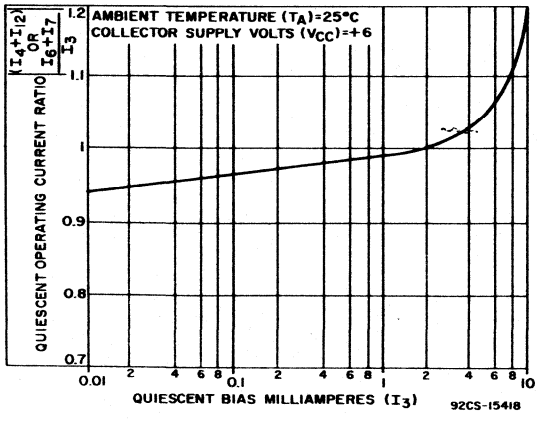


Fig.5(a) - Typical quiescent operating current ratio vs quiescent bias current.

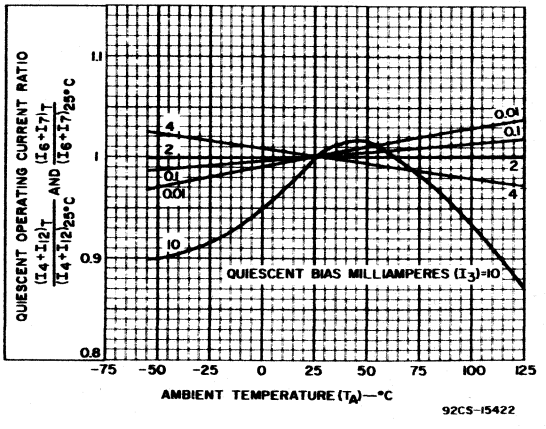


Fig.5(b) - Typical quiescent operating current ratio vs ambient temperature.

STATIC CHARACTERISTICS

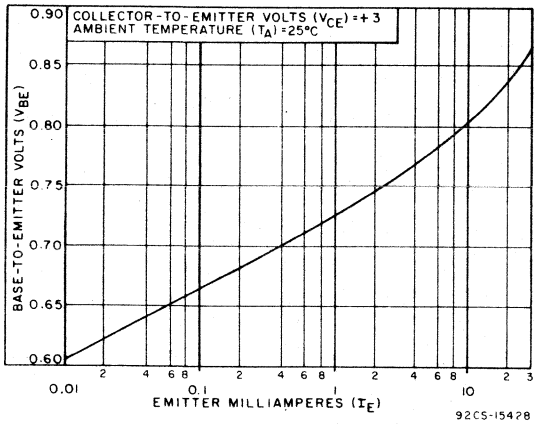


Fig.6 - Typical static base-to-emitter voltage characteristic vs emitter current for all transistors and forward diode voltage drops.

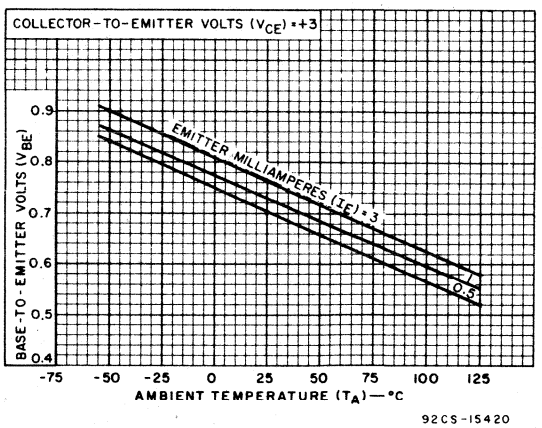


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

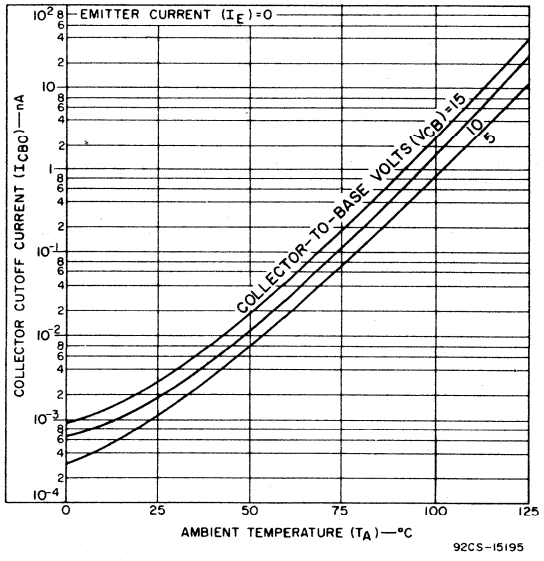


Fig.8 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

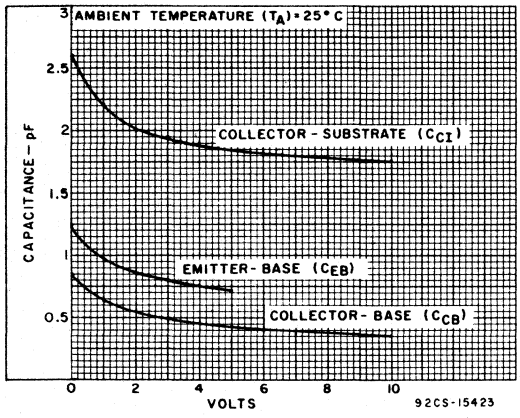


Fig.9 - Typical capacitance for each transistor.

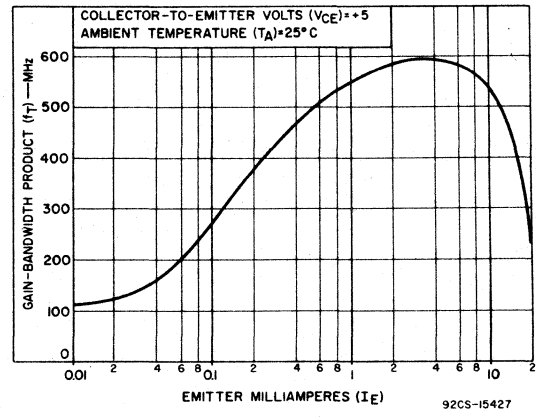
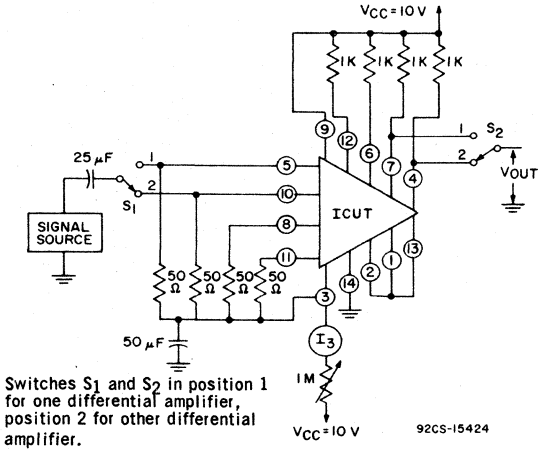


Fig.10 - Typical gain-bandwidth product (f_T) for each transistor vs emitter current.



Switches S_1 and S_2 in position 1 for one differential amplifier, position 2 for other differential amplifier.

Fig.11(a) - Test circuit for forward transadmittance, -3 dB bandwidth, and AGC range.

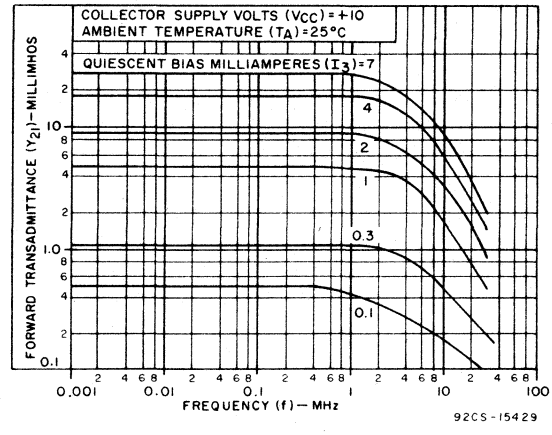


Fig.11(b) - Typical differential amplifier forward transadmittance with single-ended output vs frequency.

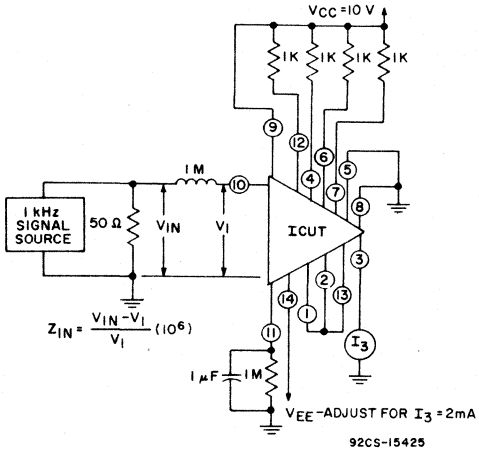


Fig.12(a) - Test circuit for input impedance.

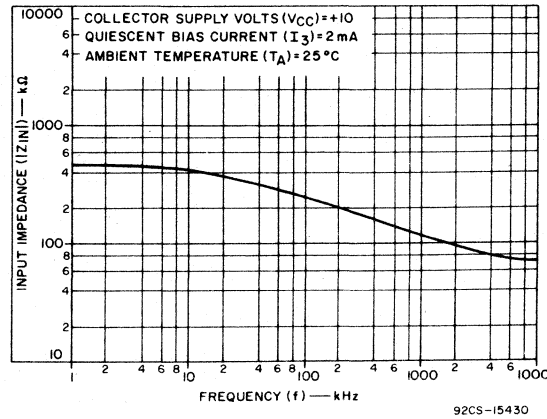
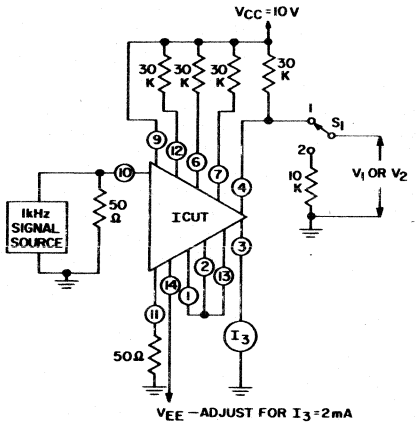


Fig.12(b) - Typical input impedance vs frequency with output short-circuited.

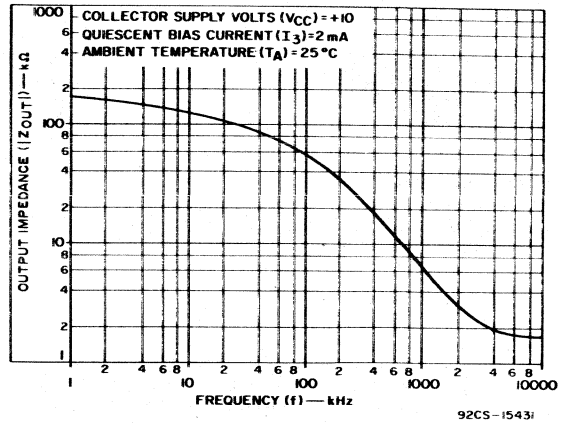
DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR



$$Z_{OUT} = \frac{(30K \times 10K)\frac{V_2}{V_1}}{\frac{V_2}{V_1}(30K+10K)-10K}$$

92CS-15426

Fig.13(a) - Test circuit for output impedance.

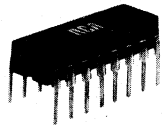


92CS-15431

Fig.13(b) - Typical output impedance vs frequency with input short-circuited.

CA3083

16-Lead Dual-In-Line Frit-Seal (Hermetic) Package H-1807



16-Lead Dual-In-Line Plastic Package H-1622

General-Purpose High-Current N-P-N Transistor Array

Features:

- *High I_C: 100 mA max.*
- *Low V_{CEsat} (at 50 mA): 0.7V max.*
- *Matched pair (Q1 and Q2) - V_{IO} (V_{BE} matched): ± 5 mV max. I_{IO} (at 1 mA): 2.5 μA max.*
- *5 independent transistors plus separate substrate connection*

Applications:

- *Signal processing and switching systems operating from DC to VHF*
- *Lamp and relay driver*
- *Differential amplifier*
- *Temperature-compensated amplifier*
- *Thyristor firing*
- *See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Circuit Transistor Array" for suggested applications*

RCA-CA3083 is a versatile array of five high-current (to 100mA) n-p-n transistors on a common monolithic substrate. In addition, two of these transistors (Q1 and Q2) are matched at low currents (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design. The CA3083 is supplied in a 16-lead dual-in-line frit-seal ceramic package. The CA3083 is also available in chip form.

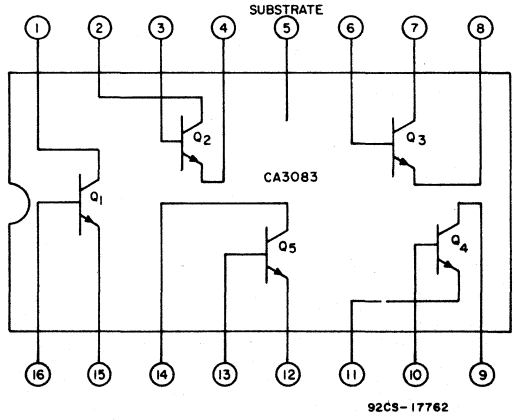


Fig. 1 — Functional diagram of the CA3083.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:

Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C

Ambient Temperature Range:

Operating	−55 to +125	°C
Storage	−65 to +150	°C

Lead Temperature (During Soldering):

At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 seconds max.	265	°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage (V_{CEO})	15	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})■	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

■ The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
For Each Transistor:							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	–	5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	–	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 10mA	2	40	76	–	
		V_{CE} = 3V, I_C = 50mA	2	40	75	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 50mA, I_B = 5mA	4	–	0.40	0.70	V
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 10 mA		–	450	–	MHz
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	7	–	1.2	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	8	–	0.7	2.5	μA

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

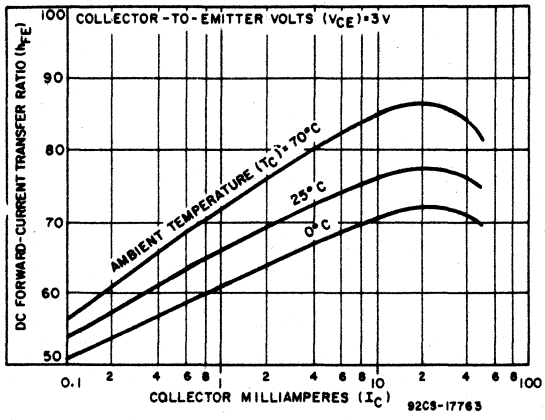


Fig.2 – h_{FE} vs I_C

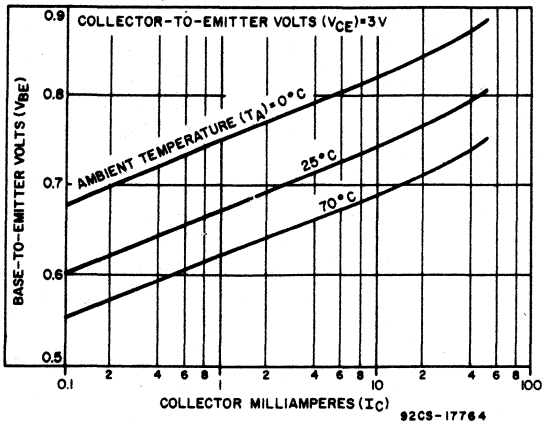


Fig.3 – V_{BE} vs I_C

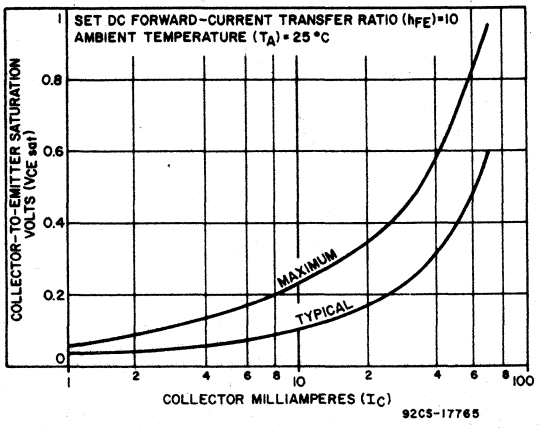


Fig.4 – V_{CEsat} vs I_C at 25°C

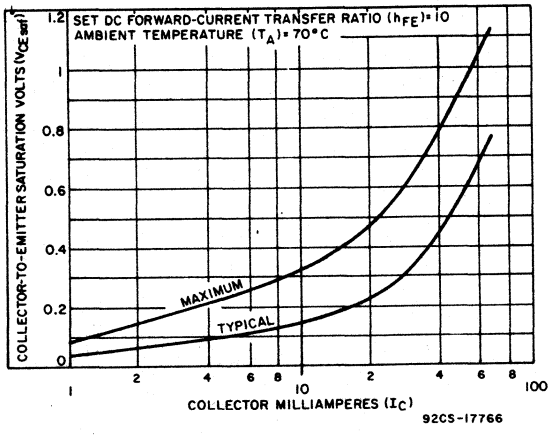


Fig.5 – V_{CEsat} vs I_C at 70°C

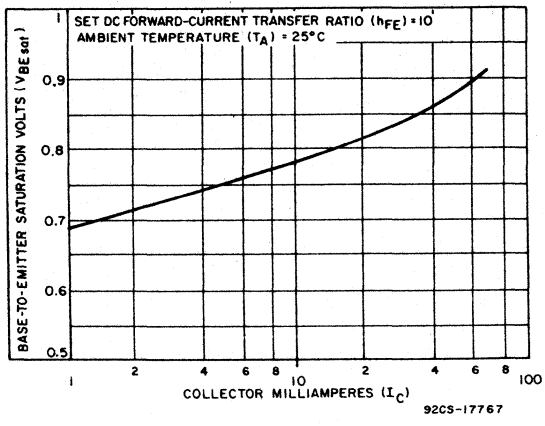


Fig.6 – V_{BEsat} vs I_C

TYPICAL STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

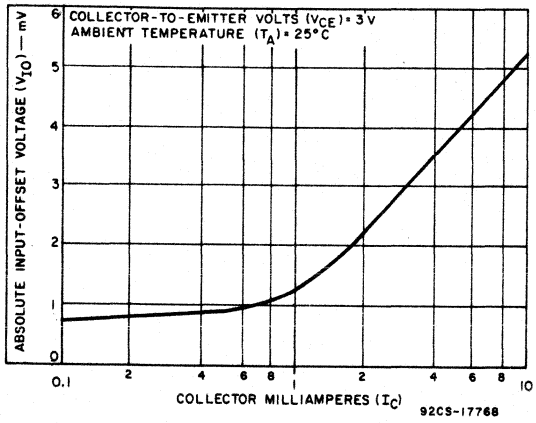


Fig.7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

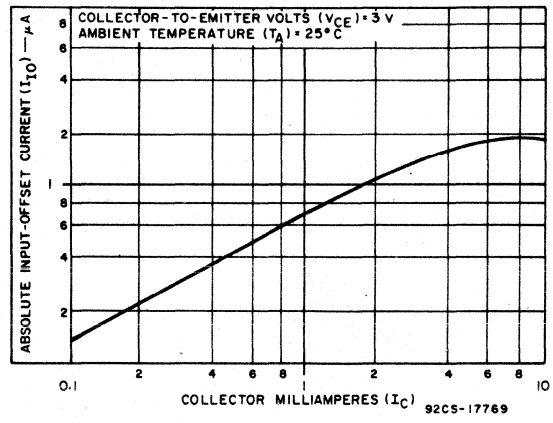
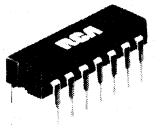


Fig.8 – I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).



H-1517

14-Lead Dual-In-Line
Plastic Package

General-Purpose P-N-P Transistor Array

FEATURES

- Matched transistor pair (Q1 and Q2)
  V_{IO} (V_{BE} matched): ± 6mV max.
  I_{IO} (at 100 μA): ± 0.6 μA
- Wide operating current range
- Low noise figure - - 3.2 dB typ. at 1 kHz

RCA-CA3084* is a general-purpose silicon p-n-p transistor array incorporating two independent transistors, a Darlington circuit, and a current-mirror pair with a shared diode.

The two independent transistors in the array may be used in a variety of circuit applications. The Darlington pair may be employed as the equivalent of a single high-beta transistor. The current-mirror pair is well suited for constant-current applications and can also be used as the active loads in a differential amplifier which uses n-p-n transistors.

The total array is especially useful for a wide range of applications in systems having low-power and low-frequency requirements. Although the transistors may be used as discrete units in conventional circuits, they offer the advantages inherent in integrated-circuit construction, that is, to provide close electrical and thermal matching.

The CA3084 utilizes the 14-lead dual-in-line plastic package.

*Formerly developmental type TA5799A.

APPLICATIONS

- General use in signal processing systems having low-power and low-frequency requirements
- Differential amplifiers
- Temperature compensated amplifiers
- Active loads for differential amplifiers using n-p-n transistors
- Complementary uses with RCA n-p-n transistor arrays

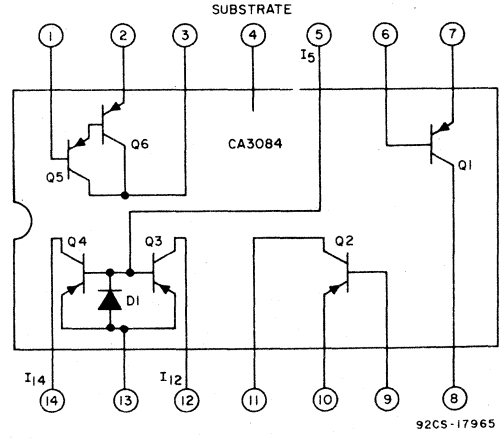


Fig. 1 -- Functional diagram of the CA3084.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Characteristics Curve Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Each Transistor:							
Collector-Cutoff Current	I_{CBO}	V_{CB} = −10V, I_E = 0	2	–	−0.055	−100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	3	–	−0.12	−100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_{CE} = −100μA, I_B = 0	–	−40	−70	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_{CB} = −100μA, I_E = 0	–	−40	−80	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_{EB} = −100μA, I_C = 0	–	−40	−100	–	V
Emitter-to-Substrate Breakdown Voltage	$V_{(BR)EIO}$	I_{EI} = 100μA	–	−40	−100	–	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_E = 1mA, I_B = 100μA	4	–	−0.125	−0.25	V
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = −10V	5	−0.50	−0.59	−0.68	V
DC Forward-Current Transfer Ratio	h_{FE}		7	15	40	–	
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Magnitude of Input Offset Voltage	$\lvert V_{IO} \rvert$	I_E = 100μA, V_{CE} = −10V	8	–	0.422	6	mV
Input Offset Current	I_{IO}		–	−0.6	0	0.6	μA
For Transistors Q3 and Q4 (Current-Mirror Configuration):							
Collector Current	I_C	V_{CE} = −10V, V_{CIO} = −10V,	10	0.85	1.00	1.15	μA
Magnitude of Collector Current Ratio	$\lvert I_C(Q3)/I_C(Q4) \rvert$	Term. 13 = Gnd. I_5 = −100μA,	11	0.90	1.00	1.10	
For Transistors Q5 and Q6 (Darlington Configuration):							
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	–	–	–	−1.0	μA
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = −10V	13	0.92	1.07	1.20	V
DC Forward-Current Transfer Ratio	h_{FE}		15	100	1230	–	

ELECTRICAL CHARACTERISTICS at T_A = 25°C
Typical Values Intended Only For Design Guidance

Magnitude of Temperature Coefficient:							
V_{BE} (for each transistor)	$\lvert \Delta V_{BE}/\Delta T \rvert$	I_E = 100μA,	6		−1.78		mV/°C
V_{IO} (as a differential amplifier)	$\lvert \Delta V_{IO}/\Delta T \rvert$	V_{CE} = −10V	9		0.54		μV/°C
V_{BE} (Darlington configuration)	$\lvert \Delta V_{BE}/\Delta T \rvert$		14		−3.7		mV/°C
For Each Transistor:							
Input Resistan e	R_I	f = 1kHz, V_{CE} = −10V,	19		9		kΩ
Output Resistance	R_O	I_C = −100μA	20	–	600	–	kΩ
Forward Transconductance	g_m		22	–	3	–	mmho
Collector-to-Base Capacitance	C_{CBO}	I_{CB} = 0	23	–	3.3	–	pF
Collector-to-Emitter Capacitance	C_{CEO}	I_{CE} = 0	23	–	2.5	–	pF
Base-to-Substrate Capacitance	C_{BIO}	I_{CIO} = 0	23	–	4.5	–	pF

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Dissipation:		
Any one transistor	200	mW
Total package	750	mW
Above T_A = 55°C	derate linearly6.67	mW/°C
Ambient Temperature Range:		
Operating	−40 to +85	°C
Storage	−55 to +150	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO})	−40	V
Collector-to-Base Voltage (V_{CBO})	−40	V
Base-to-Substrate Voltage (V_{BIO})*	−40	V
Emitter-to-Base Voltage (V_{EBO})	−40	V
Collector Current (I_C)	−10	mA

*The base of each transistor of the CA3084 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any base voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (4) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

STATIC CHARACTERISTICS FOR EACH TRANSISTOR

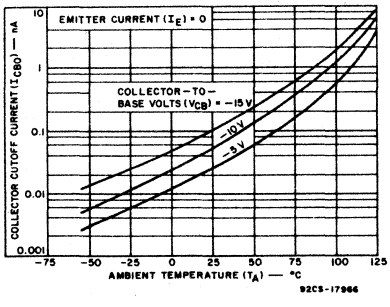


Fig.2 – I_{CBO} vs T_A.

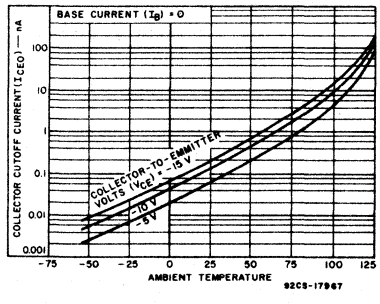


Fig.3 – I_{CEO} vs T_A.

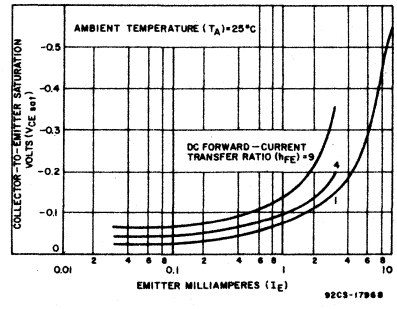


Fig.4 – V_{CEsat} vs I_E.

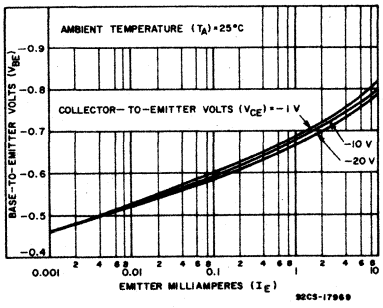


Fig.5 – V_{BE} vs I_E.

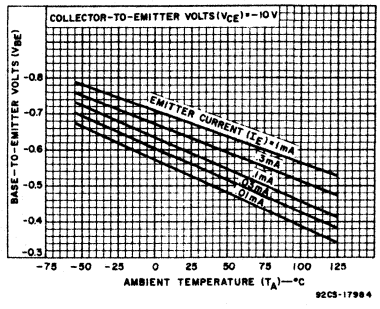


Fig.6 – V_{BE} vs T_A.

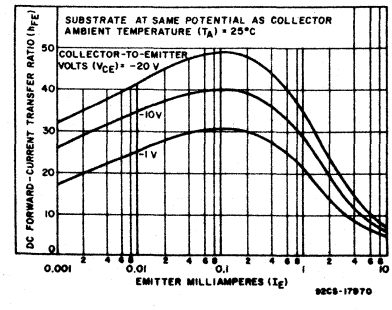


Fig.7 – h_{FE} vs I_E.

STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

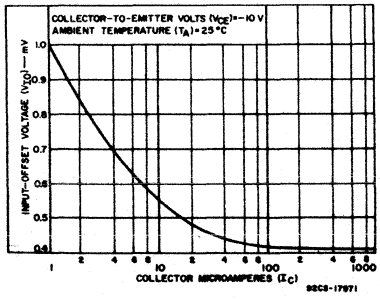


Fig.8–V_{IO} vs I_C, (transistors Q1 and Q2 as a differential amplifier).

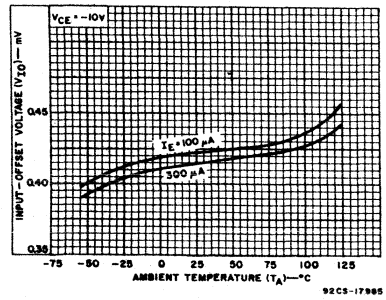


Fig.9–V_{IO} vs T_A (transistors Q1 and Q2 as a differential amplifier).

STATIC CHARACTERISTICS FOR CURRENT-MIRROR CONFIGURATION

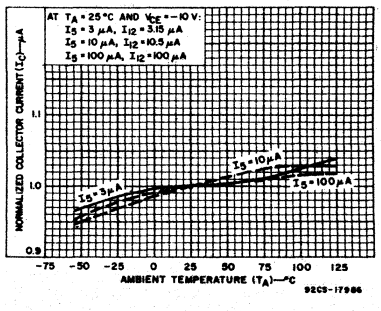


Fig.10–Normalized I_C vs T_A (transistors Q3 and Q4 in a current-mirror configuration.

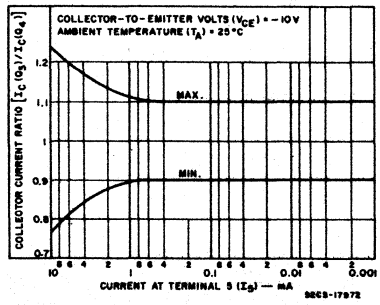


Fig.11–I_C ratio vs I_5 (transistors Q3 and Q4 in a current-mirror configuration.

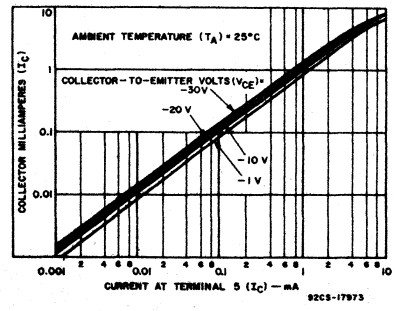


Fig.12–I_C vs I_5 (transistors Q3 and Q4 in a current-mirror configuration).

STATIC CHARACTERISTICS FOR DARLINGTON CONFIGURATION

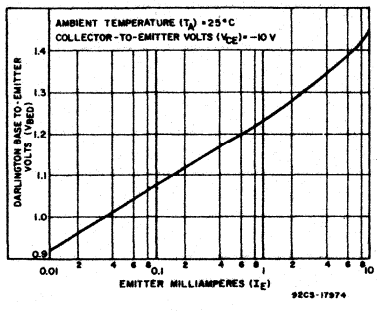


Fig.13–V_{BE} vs I_E (transistors Q5 and Q6 in a darlington configuration).

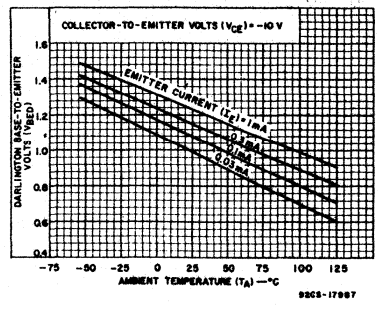


Fig.14–V_{BE} vs T_A (transistors Q5 and Q6 in a darlington configuration).

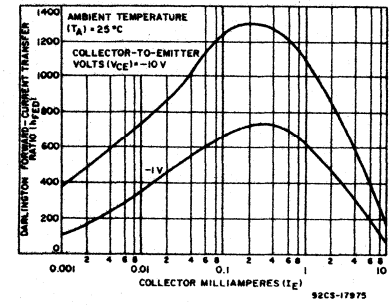


Fig.15–h_{FE} vs I_E (transistors Q5 and Q6 in a darlington configuration).

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

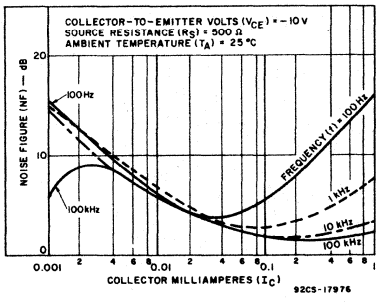


Fig.16 – NF vs I_C at R_S = 500Ω

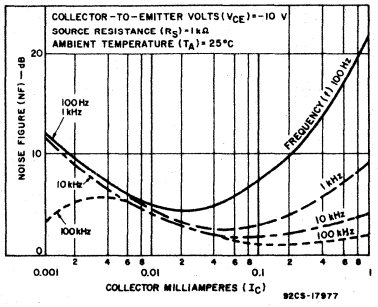


Fig.17 – NF vs I_C at R_S = 1kΩ

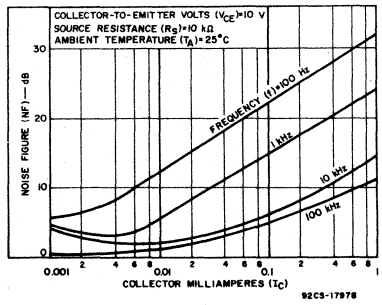


Fig.18 – NF vs I_C at R_S = 10kΩ

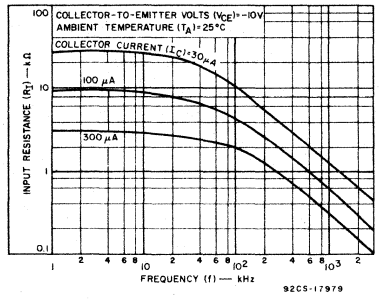


Fig.19 – R_I vs f

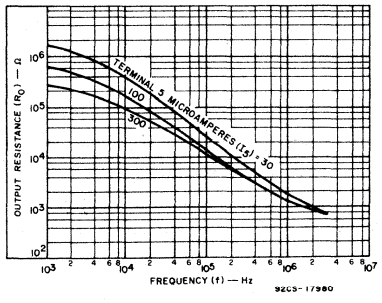


Fig.20 – R_O vs f

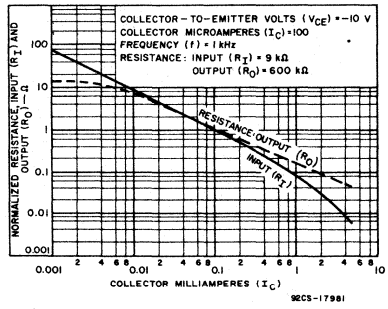


Fig.21 – Normalized R_I and R_O vs I_C

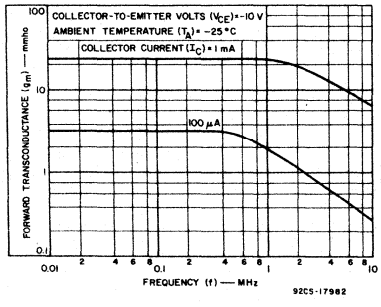


Fig.22 – g_m vs f

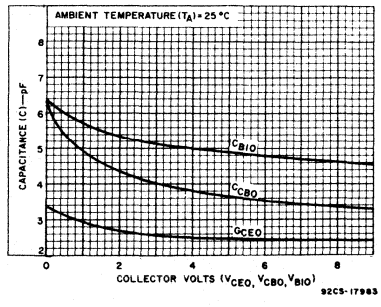
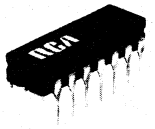


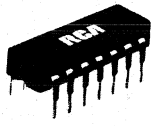
Fig.23 – Transistor capacitances vs collector voltages (V_{CEO}, V_{CBO}, V_{CIO})

14-Lead Dual-In-Line
Frit-Seal (Hermetic) Package



H-1806

14-Lead Dual-In-Line
Plastic Package



H-1517

General-Purpose N-P-N Transistor Array

Three Isolated Transistors and One Differentially–Connected Transistor Pair

For Low–Power Applications from DC to 120MHz

Applications

- **General-purpose use in signal processing systems operating in the DC to 120-MHz range**
- **Temperature compensated amplifiers**
- **See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.**

RCA-CA3086 consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120 MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching.

The CA3086 is supplied in a 14-lead dual-in line plastic package. The CA3086F is supplied in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

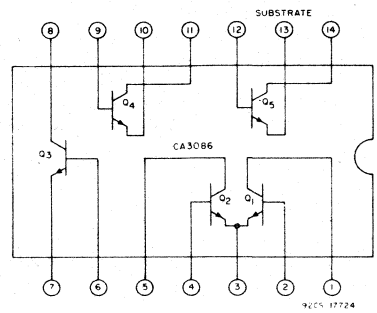


Fig. 1 – Functional diagram of the CA3086.

MAXIMUM RATINGS, Absolute–Maximum Values at T_A = 25°C

Dissipation:		
Any one transistor	300	mW
Total package up to T_A = 55°C	750	mW
Above T_A = 55°C	derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	–55 to + 125	°C
Storage	–65 to + 150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) From case for 10 seconds max.	+ 265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

CA3086

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	Typ. Characteristic Curves Fig. No.	LIMITS			UNITS
				Min.	Typ.	Max.	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	2	–	0.002	100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	3	—	See Curve	5	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 1mA	4	40	100	–	

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

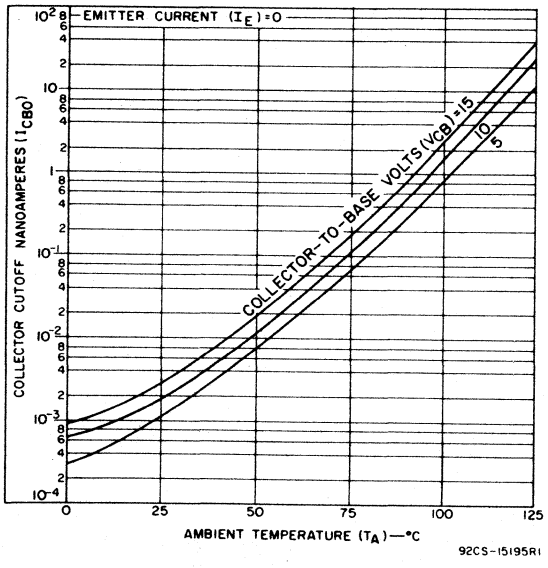


Fig.2– I_{CBO} vs T_A.

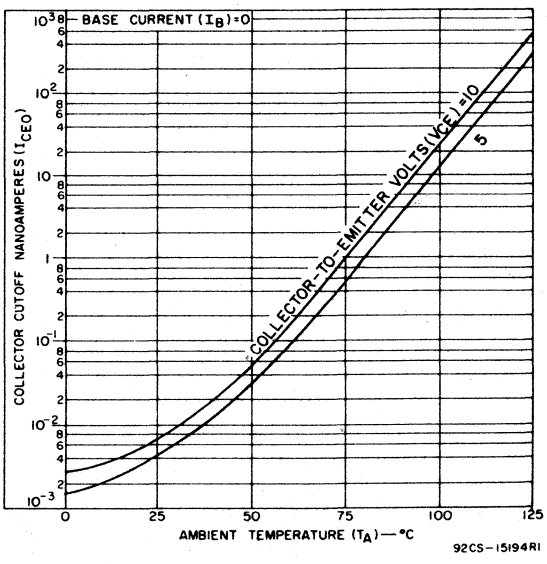


Fig.3– I_{CEO} vs T_A.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		Typ. Characteristics Curves Fig. No.	TYPICAL VALUES	UNITS
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3 V	I_C = 10 mA	4	100	
			I_C = 10 μA	4	54	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V	I_E = 1 mA	5	0.715	V
			I_E = 10 mA	5	0.800	V
V_{BE} Temperature Coefficient	$\Delta V_{BE}/\Delta T$	V_{CE} = 3V, I_C = 1mA		6	−1.9	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_B = 1mA, I_C = 10mA		—	0.23	V
Noise Figure (low frequency)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100μA, R_S = 1k Ω		—	3.25	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		7	100	—
Short-Circuit Input Impedance	h_{ie}			7	3.5	kΩ
Open-Circuit Output Impedance	h_{oe}			7	15.6	μmho
Open-Circuit Reverse-Voltage Transfer Ratio	h_{re}			7	1.8×10^{-4}	—
Admittance Characteristics:						
Forward Transfer Admittance	y_{fe}	f = 1MHz, V_{CE} = 3V, I_C = 1mA		8	31 − j1.5	mmho
Input Admittance	y_{ie}			9	0.3 + j0.04	mmho
Output Admittance	y_{oe}			10	0.001 + j0.03	mmho
Reverse Transfer Admittance	y_{re}			11	See Curve	—
Gain-Bandwidth Product	f_T	V_{CE} = 3V, I_C = 3mA		12	550	MHz
Emitter-to-Base Capacitance	C_{EBO}	V_{EB} = 3V, I_E = 0		—	0.6	pF
Collector-to-Base Capacitance	C_{CBO}	V_{CB} = 3V, I_C = 0		—	0.58	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 3V, I_C = 0		—	2.8	pF

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

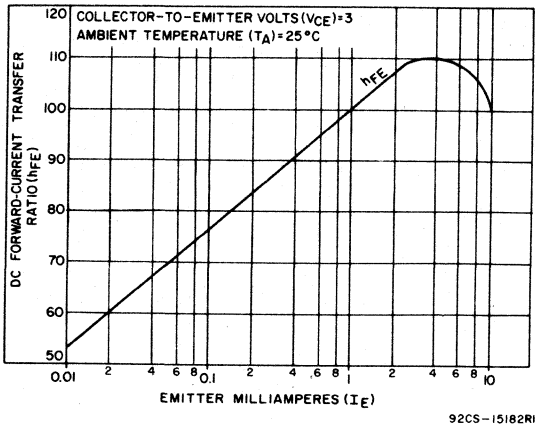


Fig.4 – h_{FE} vs I_E.

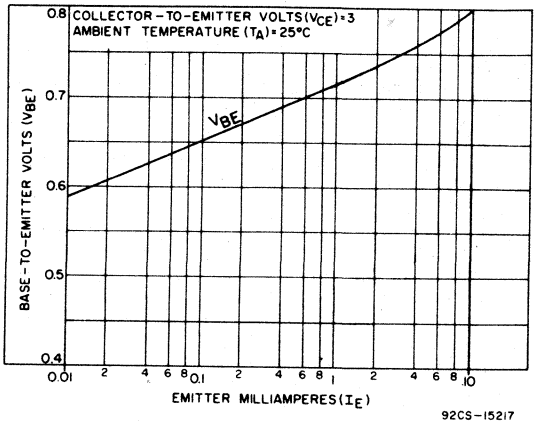


Fig.5 – V_{BE} vs I_E.

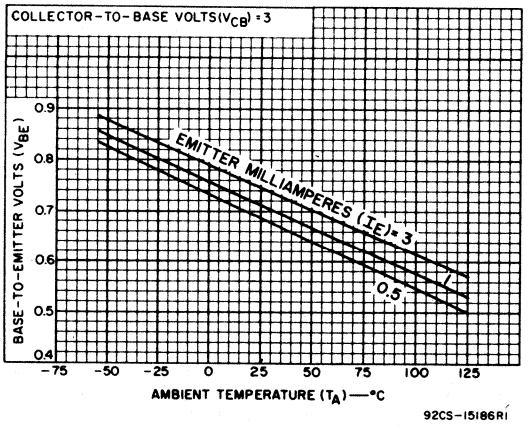


Fig.6 – V_{BE} vs T_A.

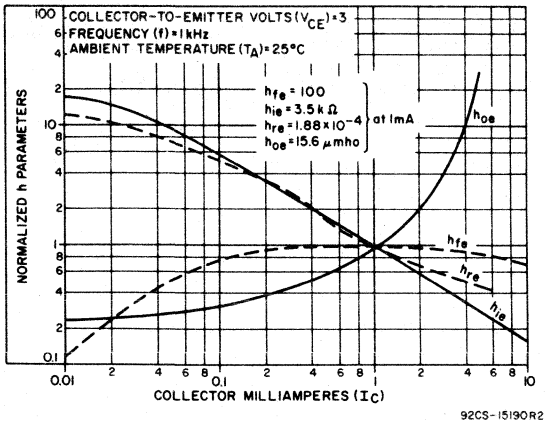


Fig.7 – Normalized h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C.

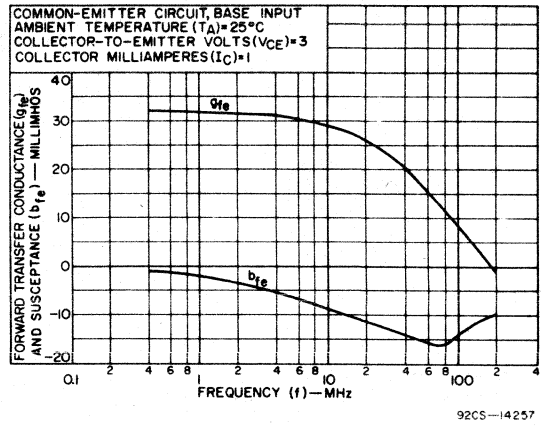


Fig.8 – y_{fe} vs f.

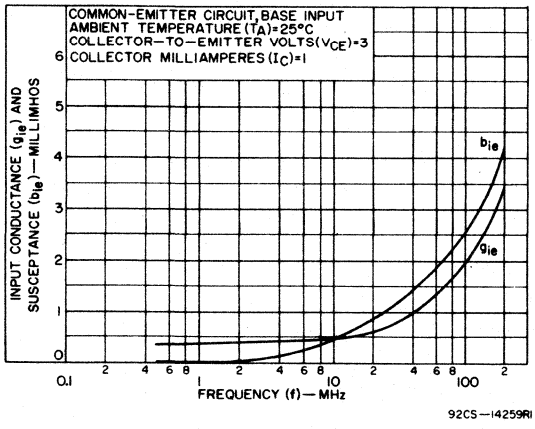


Fig.9 – y_{ie} vs f.

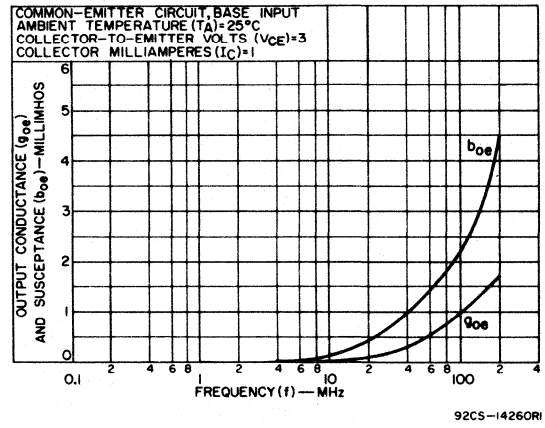


Fig.10 – y_{oe} vs f.

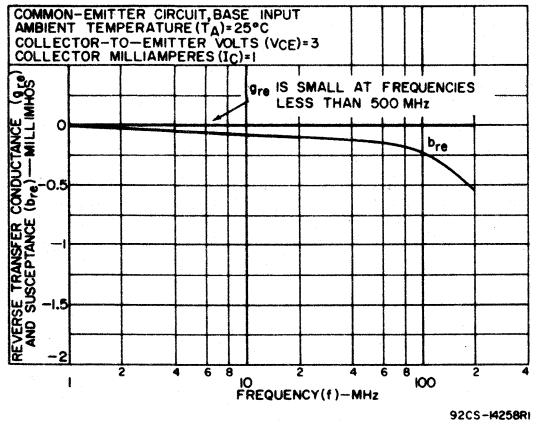


Fig.11 – y_{re} vs f.

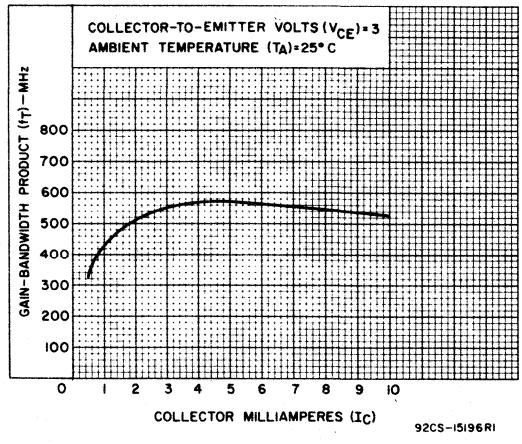
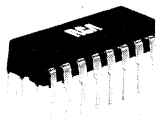


Fig.12 – f_T vs I_C.

CA3093E



16-Lead Dual-In-Line
Plastic Package H1622

General-Purpose High-Current N-P-N Transistor-Zener Diode-Diode Array

Applications

- Signal processing and switching systems operating from DC to VHF
- Lamp and relay driver
- Differential amplifier
- Temperature-compensated amplifier
- Thyristor firing
- Temperature-compensated shunt regulator
- Temperature-compensated series regulator
- Level shifting
- Voltage-level clamping

RCA CA3093E* is a versatile array of three high-current (to 100mA) NPN transistors, two 10%-tolerance Zener diodes and one conventional diode, all on a common monolithic substrate. Two of the transistors (Q_1 and Q_2) are matched at 1 mA for applications in which offset parameters are of special importance. The combination of positive Zener voltage temperature coefficients and negative forward base-emitter voltage temperature coefficients provides a unique temperature compensation capability.

Independent connections for each transistor and diode plus a separate terminal for the substrate permit maximum flexibility in circuit design.

*Formerly developmental type TA6119

#Z_1, Z_2 and D1 are transistors internally connected as shown below.

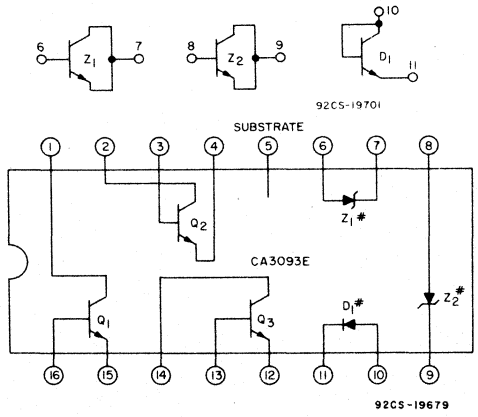


Fig. 1 — Functional diagram of the CA3093E (bottom view)

- Current regulator
- Voltage clamping
- Simple off-line regulated supply
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Circuit Transistor Array" for applications in addition to those given on pages 5 & 6 of this bulletin.

Features:

- **6 independent devices plus separate substrate connection**
- **Compensating temperature coefficients — V_{BE} and V_{D1} VS. V_Z**

Transistors

- **High I_C (100mA max)**
- **Matched pair (Q1 & Q_2)**
  V_{IO} = ± 5mV max, I_{IO} = 2.5 μA max } at I_C = 1mA
  $\Delta V_{IO}/\Delta T$ = 5 μV/°C typ
- **h_{FE} = 40 min @ I_C = 10mA or 50mA**
- **Low V_{CEsat} . . . 0.7V max @ 50mA**

Zener Diodes

- **Two 1/4W Zeners**
- **V_Z = 7V ± 10%**
- **z_Z = 15Ω typ**

Diode

- **Close forward voltage match to V_{BE}'s of Q_1 and Q_2**
- **V_{PIV} = 5.5V min.**

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

Power Dissipation:

Any one transistor	500	mW
Any one Zener Diode	250	mW
Total package	750	mW
Above 25°C ..... Derate linearly	6.67	mW/°C
Ambient Temperature Range:		
Operating	-40 to +85	°C
Storage	-55 to +150	°C

The following maximum ratings apply for each transistor

Collector-to-Emitter Voltage (V_{CEO})	15	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})*	20	V
Emitter-to-Base Voltage (V_{EBO})	5.5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	35	mA

The following maximum ratings apply for each Zener Diode or Diode

Zener Diode dc Current (I_Z)	35	mA
Zener Diode-to-Substrate Voltage (V_{ZIO})*	20	V
Diode (D1) Forward Current (I_{DF})	50	mA
Diode (D1) Reverse Voltage (V_{DR})	5.5	V
Diode (D1)-to-Substrate Voltage (V_{DIO})*	20	V

*The collector of each transistor, the cathode of each Zener diode, and the anode of the diode are isolated from the substrate by an internal diode. The substrate must be connected to a voltage which is more negative than any of these isolated terminals in order to maintain isolation between devices and provide normal transistor action. To avoid undesired coupling between devices, the substrate terminal (5) should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

CA3093E

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Each Transistor:							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	–	5.5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	–	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	–	1	μA
DC Forward Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 10mA	2	40	76	–	
		V_{CE} = 3V, I_C = 50mA	2	40	75	–	
Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 50mA, I_B = 5mA	4	–	0.40	0.70	V
Forward Base-to-Emitter Temp. Coefficient	$\Delta V_{BE}/\Delta T$	I_E = 10mA		–	-1.9	–	mV/°C
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	7	–	1.2	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	8	–	0.7	2.5	μA
Temp. Coefficient of Offset Voltage	$\lvert\Delta V_{IO}/\Delta T\rvert$	–	–	–	5	–	μV/°C
For Each Zener Diode							
Zener Voltage	V_Z	I_Z = 10mA	9	6.3	7	7.7	V
Zener Impedance	z_Z	I_Z = 10mA, f = 1 kHz	10	–	15	25	Ω
Zener Reverse Current	I_{ZR}	V_Z = +5V	–	–	–	1	μA
Zener Voltage Temp. Coefficient	$\Delta V_Z/\Delta T$	I_Z = 10mA	9	– i.e.	+3.6 +.05	–	mV/°C %/°C
Zener-to-Substrate Breakdown Voltage	$V_{(BR)ZIO}$	I_Z = 100μA (Terminals 7 & 9)	–	20	60	–	V
Dissipation		Refer to Example in Application "a"		–	–	250	mW
For Diode (D1)							
Diode Forward Voltage	V_{DF}	I_C = 10mA, V_{CE} = 3V	3	0.65	0.74	0.85	V
Diode Forward Current	I_{DF}		–	–	–	50	mA
Diode Reverse-Breakdown Voltage	$V_{(BR)DR}$	I_{DR} = 500μA	–	5.5	6.9	–	V
Diode-to-Substrate Breakdown Voltage	$V_{(BR)DIO}$	I_{Diode} = 100μA (Terminal 10)	–	20	60	–	V
Diode Forward-Voltage Temp. Coefficient	$\Delta V_{DF}/\Delta T$	I_{DF} = 5mA	3	–	-1.9	–	mV/°C

TYPICAL STATIC CHARACTERISTICS

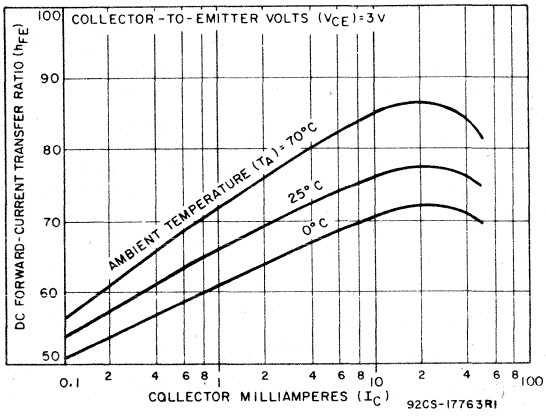


Fig. 2 – h_{FE} vs I_C

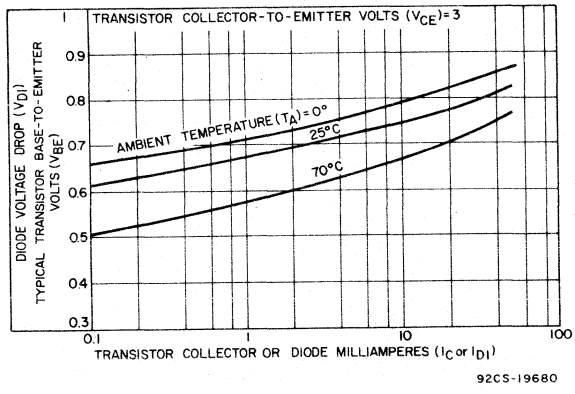


Fig. 3 – V_{BE} vs I_C and V_{D1} vs I_{D1}

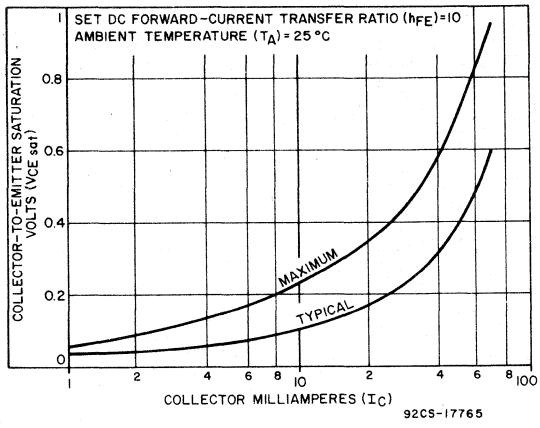


Fig. 4 – V_{CEsat} vs I_C at 25°C

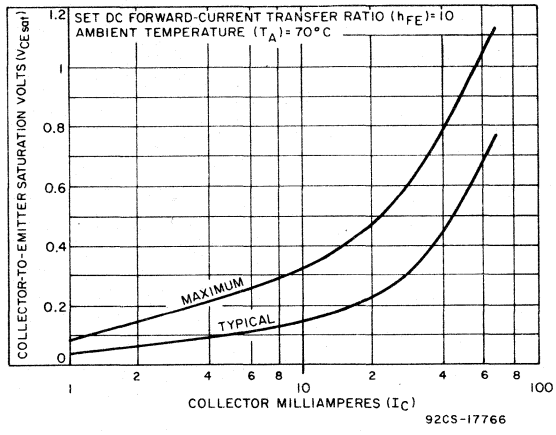


Fig. 5 – V_{CEsat} vs I_C at 70°C

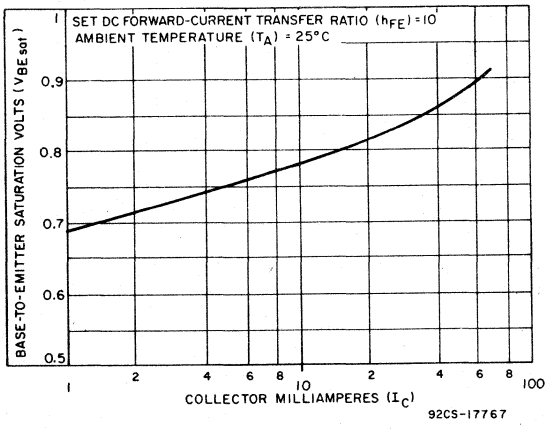


Fig. 6 – V_{BEsat} vs I_C

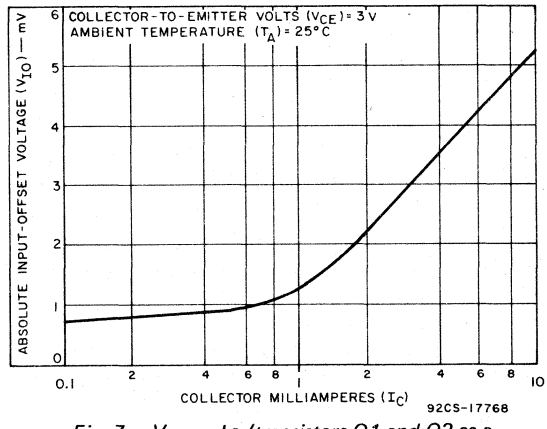


Fig. 7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier)

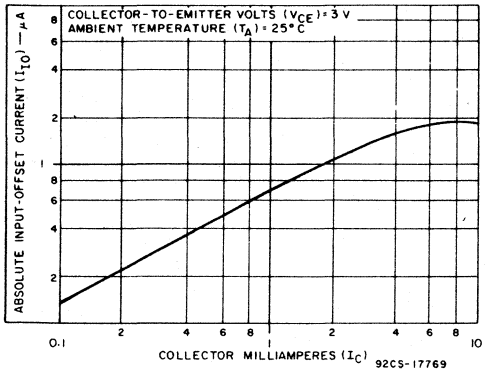


Fig. 8 – I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier)

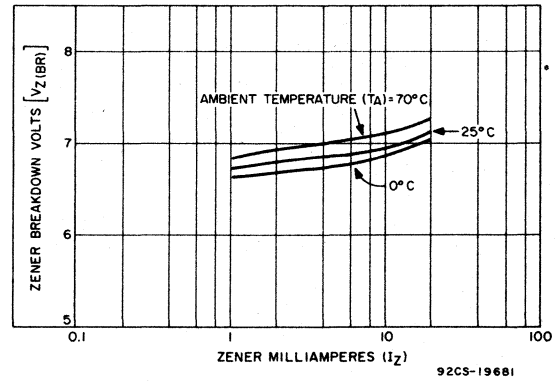


Fig. 9 – Typical Zener breakdown voltage vs current

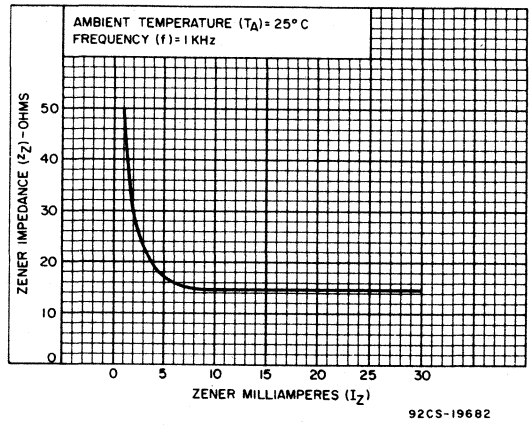
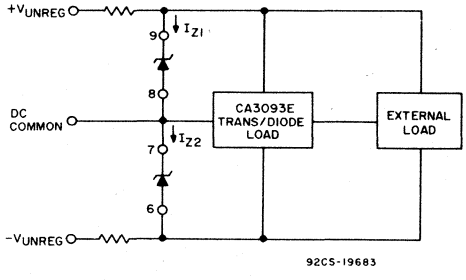


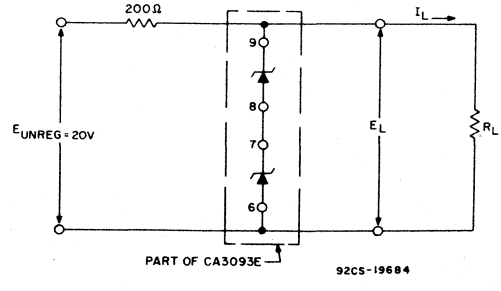
Fig. 10 – Typical Zener impedance vs current

TYPICAL APPLICATIONS

a) ±7V Regulator supplying CA3093E Transistors plus an external load.



b) 14V Regulator for Q1, Q2, Q3



Sample Computation for Determining Permissible Zener Dissipation at +25°C.

CA3093E Ratings at T_A = +25°C
Total Diss. Max = 750 mW (Derate @ 6.67 mW/°C above 25°C)
Each Zener Diss. Max = 250 mW
Max. Zener Current = 35 mA

Assume CA3093E Transistor/Diode Load Dissipation = 350 mW then max. total Zener Diss. ($P_{Z1} + P_{Z2}$) = 750 - 350 = 400 mW

$$(I_{Z1} + I_{Z2})\ max = \frac{400\ mW}{7V} = 57\ mA$$

(Note: Max. current rating on each Zener is 35 mA)

Typical Load Regulation for I_L = 0 to 25 mA

$\Delta E_L/E_L \times 100 \approx -6\%$
(no load to full load)

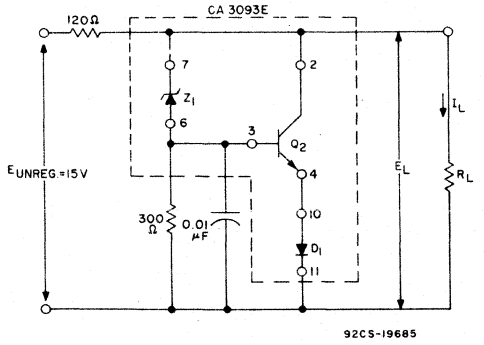
Typical Line Regulation

$$\frac{(\Delta E_L/E_L) \times 100}{\Delta E\ unreg.} \approx \pm 0.9\%/V$$

Typical Temperature Characteristic

$$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = +0.05\%/°C$$

c) 8.6V Temp.-Compensated Shunt Regulator



Typical Temperature Characteristic @ R_L = 330Ω

$$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = \pm\ 0.007\%/°C$$

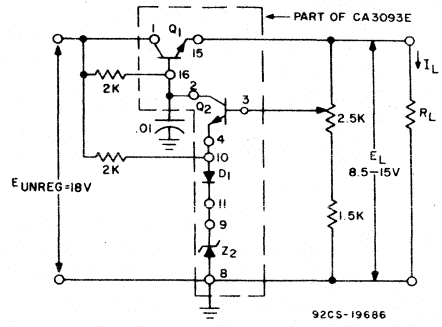
Typical Load Regulation I_L = 0 to 40 mA

$(\Delta E_L/E_L) \times 100 = -3\%$ (no load to full load)

Typical Line Regulation at R_L = 330Ω

$$\frac{\Delta E_L/E_L}{\Delta E \text{ unreg.}} \times 100 = \pm\ 0.55\%/V$$

d) Temp.-Compensated Series Voltage Regulator



Typical Temperature Characteristic @ E_L = 12V

$$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = \pm\ 0.009\%/°C$$

Typical Load Regulation @ E_L = 12V

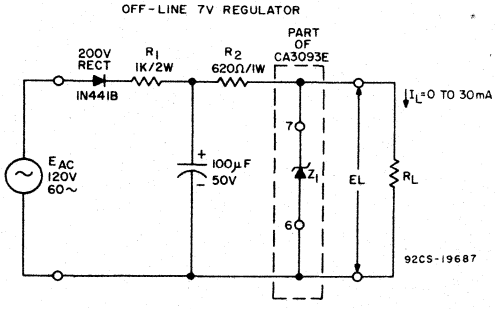
I_L = 0 to 40 mA

$$\frac{\Delta E_L}{E_L} \times 100 = \pm\ 0.4\% \text{ (no load to full load)}$$

Typical Line Regulation @ E_L = 12V

$$\frac{(\Delta E_L/E_L) \times 100}{\Delta E \text{ unreg.}} = \pm\ 0.45\%/V$$

e) Off-Line 7V Regulator



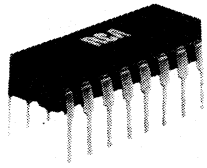
Typical E_L Ripple Voltage = 70 mV_{p-p}

Typical Load Regulation = $\frac{\Delta E_L}{E_L} \times 100 = -8.5\%$ (no load to full load)

I_L = 0 to 30 mA

Typical Line Regulation = $\frac{(\Delta E_L/E_L) \times 100}{\Delta E_{AC}} = \pm\ .075\%/V$

CA3096, CA3096A, CA3096C



(E SUFFIX)
16-Lead Dual-In-Line
Plastic Package

H-1622

N-P-N/P-N-P Transistor Array

Five-Independent Transistors: Three n-p-n and Two p-n-p

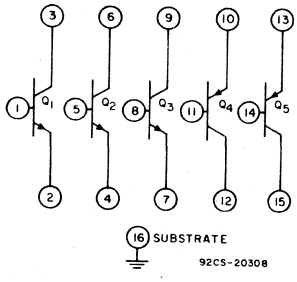
Applications:

- *Differential Amplifiers*
- *DC Amplifiers*
- *Sense Amplifiers*
- *Level Shifters*
- *Timers*
- *Lamp and Relay Drivers*
- *Thyristor Firing Circuits*
- *Temperature-Compensated Amplifiers*
- *Operational Amplifiers*

RCA-CA3096CE, CA3096E, and CA3096AE are general-purpose high-voltage silicon transistor arrays. Each array consists of five independent transistors (two p-n-p and three n-p-n types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096AE, CA3096E, and CA3096CE are identical, except that the CA3096AE specifications include parameter matching and greater stringency in I_{CBO}, I_{CEO}, and $V_{CE}(SAT)$. The CA3096CE is a relaxed version of the CA3096E.

The CA3096CE, CA3096E, and CA3096AE are supplied in 16-lead dual-in-line plastic packages. (E-suffix). The CA3096 is also available in chip form. (H suffix).



Schematic Diagram

CA3096AE, CA3096E, CA3096CE
ESSENTIAL DIFFERENCES

CHARACTERISTIC		CA3096AE	CA3096E	CA3096CE
$V_{(BR)CEO}$ (V) Min.	n-p-n	35	35	24
	p-n-p	−40	−40	−24
$V_{(BR)CBO}$ (V) Min.	n-p-n	45	45	30
	p-n-p	−40	−40	−24
h_{FE} @ 1 mA	n-p-n	150-500	150-500	100-670
	p-n-p	20-150	20-150	15-200
h_{FE} @ 100 μA	p-n-p	40-200	40-200	30-300
I_{CBO} (nA) Max.	n-p-n	40	100	100
	p-n-p	−40	−100	−100
I_{CEO} (nA) Max.	n-p-n	100	1000	1000
	p-n-p	−100	−1000	−1000
$V_{CE}(SAT)$ (V) Max.	p-n-p	0.5	0.7	0.7
$\lvert V_{IO}\rvert$ (mV) Max.	n-p-n	5	–	–
	p-n-p	5	–	–
$\lvert I_{IO}\rvert$ (μA) Max.	n-p-n	0.6	–	–
	p-n-p	0.25	–	–

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	EACH N-P-N	EACH P-N-P	
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}:			
CA3096AE, CA3096E	35	−40	V
CA3096CE	24	−24	V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}:			
CA3096AE, CA3096E	45	−40	V
CA3096CE	30	−24	V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}:			
CA3096AE, CA3096E	45	−	V
CA3096CE	30	−	V
EMITTER-TO-SUBSTRATE VOLTAGE, V_{EIO}:			
CA3096AE, CA3096E	−	−40	V
CA3096CE	−	−24	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}:			
CA3096E, CA3096E	6	−40	V
CA3096CE	6	−24	V
COLLECTOR CURRENT, I_C (All Types)	50	−10	mA
POWER DISSIPATION, P_D:			
Up to $T_A = 55°C$:			
Device (Total)	750		mW
Each Transistor	200		mW
Above $T_A = 55°C$ derate linearly at	6.67		mW/°C
AMBIENT-TEMPERATURE RANGE, T_A:			
Operating	−55 to +125°C		
Storage	−65 to +150°C		
LEAD TEMPERATURE (DURING SOLDERING):			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	265°C		

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096AE			CA3096E			CA3096CE			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each n-p-n Transistor											
I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	−	0.001	40	−	0.001	100	−	0.001	100	nA
I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	−	0.006	100	−	0.006	1000	−	0.006	1000	nA
$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	35	50	−	35	50	−	24	35	−	V
$V_{(BR)CBO}$	$I_C = 10\,\mu$A, $I_E = 0$	45	100	−	45	100	−	30	80	−	V
$V_{(BR)CIO}$	$I_{CI} = 10\,\mu$A, $I_B = I_E = 0$	45	100	−	45	100	−	30	80	−	V
$V_{(BR)EBO}$	$I_E = 10\,\mu$A, $I_C = 0$	6	8	−	6	8	−	6	8	−	V
V_Z	$I_Z = 10\,\mu$A	6	7.9	9.8	6	7.9	9.8	6	7.9	9.8	V
$V_{CE(SAT)}$	$I_C = 10$ mA, $I_B = 1$ mA	−	0.24	0.5	−	0.24	0.7	−	0.24	0.7	V
V_{BE}	$I_C = 1$ mA, $V_{CE} = 5$ V	0.6	0.69	0.78	0.6	0.69	0.78	0.6	0.69	0.78	V
h_{FE}		150	390	500	150	390	500	100	390	670	
$\lvert\Delta V_{BE}/\Delta T\rvert$	$I_C = 1$ mA, $V_{CE} = 5$ V	−	1.9	−	−	1.9	−	−	1.9	−	mV/°C

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ (Cont'd)
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096AE			CA3096E			CA3096CE			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each p-n-p Transistor											
I_{CBO}	$V_{CB} = -10$ V, $I_E = 0$	–	−0.006	−40	–	−0.06	−100	–	−0.06	−100	nA
I_{CEO}	$V_{CE} = -10$V, $I_B = 0$	–	−0.12	−100	–	−0.12	−1000	–	−0.12	−1000	nA
$V_{(BR)CEO}$	$I_C = -100\,\mu$A, $I_B = 0$	−40	−75	–	−40	−75	–	−24	−30	–	V
$V_{(BR)CBO}$	$I_C = -10\,\mu$A, $I_E = 0$	−40	−80	–	−40	−80	–	−24	−60	–	V
$V_{(BR)EBO}$	$I_E = -10\,\mu$A, $I_C = 0$	−40	−100	–	−40	−100	–	−24	−80	–	V
$V_{(BR)EIO}$	$I_{EI} = 10\,\mu$A, $I_B = I_C = 0$	−40	−100	–	−40	−100	–	−24	−80	–	V
$V_{CE(SAT)}$	$I_C = -1$ mA, $I_B = -100\,\mu$A	–	−0.16	−0.4	–	−0.16	−0.4	–	−0.16	−0.4	V
V_{BE}	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	−0.5	−0.6	−0.7	−0.5	−0.6	−0.7	−0.5	−0.6	−0.7	V
h_{FE}	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	40	85	250	40	85	250	30	85	300	
	$I_C = -1$ mA, $V_{CE} = -5$ V	20	47	200	20	47	200	15	47	200	
$\lvert\Delta V_{BE}/\Delta T\rvert$	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	–	2.2	–	–	2.2	–	–	2.2	–	mV/°C

I_{CBO} Collector-Cutoff Current

I_{CEO} Collector-Cutoff Current

$V_{(BR)CEO}$ Collector-to-Emitter Breakdown Voltage

$V_{(BR)CBO}$ Collector-to-Base Breakdown Voltage

$V_{(BR)CIO}$ Collector-to-Substrate Breakdown Voltage

$V_{(BR)EBO}$ Emitter-to-Base Breakdown Voltage

V_Z Emitter-to-Base Zener Voltage

$V_{CE(SAT)}$ Collector-to-Emitter Saturation Voltage

V_{BE} Base-to-Emitter Voltage

h_{FE} DC Forward-Current Transfer Ratio

$\lvert\Delta V_{BE}/\Delta T\rvert$ Magnitude of Temperature Coefficient: (for each transistor)

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ (CA3096AE Only)
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS	LIMITS CA3096AE			UNITS
			Min.	Typ.	Max.	
For Transistors Q1 and Q2 (as a Differential Amplifier)						
Absolute Input Offset Voltage,	$\lvert V_{IO}\rvert$	$V_{CE} = 5\,V$, $I_C = 1\,mA$	–	0.3	5	mV
Absolute Input Offset Current,	$\lvert I_{IO}\rvert$		–	0.07	0.6	μA
Absolute Input Offset Voltage Temperature Coefficient,	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		–	1.1	–	μV/°C
For Transistors Q4 and Q5 (As a Differential Amplifier)						
Absolute Input Offset Voltage,	$\lvert V_{IO}\rvert$	$V_{CE} = -5\,V$, $I_C = -100\,\mu A$, $R_S = 0$	–	0.15	5	mV
Absolute Input Offset Current,	$\lvert I_{IO}\rvert$		–	2	250	nA
Absolute Input Offset Voltage Temperature Coefficient,	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		–	0.54	–	μV/°C

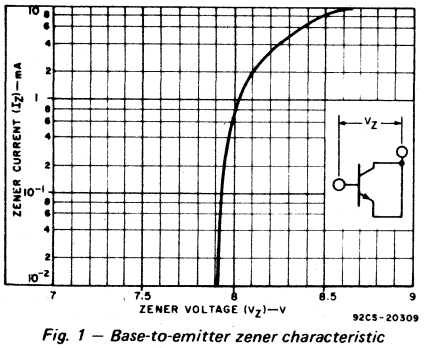


Fig. 1 – Base-to-emitter zener characteristic (n-p-n).

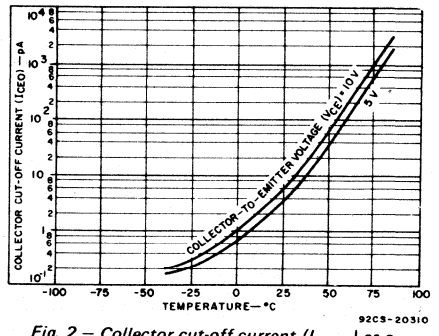


Fig. 2 – Collector cut-off current (I_{CEO}) as a function of temperature (n-p-n).

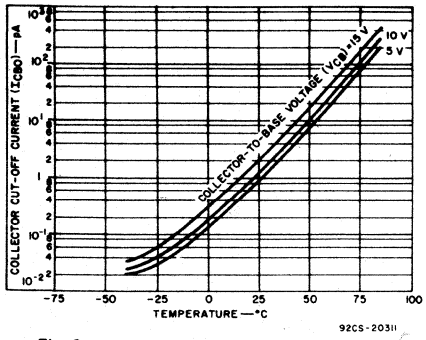


Fig. 3 – Collector cut-off current (I_{CBO}) as a function of temperature (n-p-n).

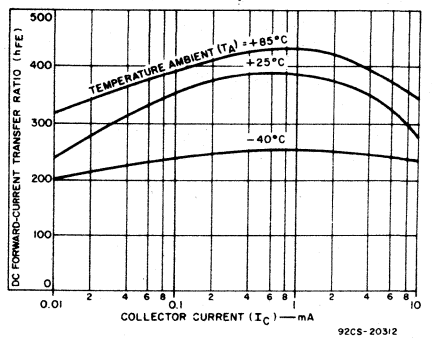


Fig. 4 – Transistor (n-p-n) h_{FE} as a function of collector current.

CA3096, CA3096A, CA3096C

DYNAMIC

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Typical Values Intended Only for Design Guidance

CHARACTERISTICS	TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each n-p-n Transistor			
Noise Figure (low frequency), NF	f = 1 kHz, V_{CE} = 5 V, I_C = 1 mA, R_S = 1 kΩ	2.2	dB
Low-Frequency, Input Resistance, R_i	f = 1.0 kHz, V_{CE} = 5 V, I_C = 1 mA	10	kΩ
Low-Frequency Output Resistance, R_o		80	kΩ
Admittance Characteristics:	f = 1 MHz, V_{CE} = 5 V, I_C = 1 mA		
Forward Transfer Admittance, $\frac{g_{fe}}{y_{fe}\ b_{fe}}$		7.5 −j13	mmho
Input Admittance, $\frac{g_{ie}}{y_{ie}\ b_{ie}}$		2.2 j3.1	mmho
Output Admittance, $\frac{g_{oe}}{y_{oe}\ b_{oe}}$		0.76 j2.4	mmho
Gain-Bandwidth Product, f_T	V_{CE} = 5 V, I_C = 1.0 mA	280	MHz
	V_{CE} = 5 V, I_C = 5 mA	335	
Emitter-to-Base Capacitance, C_{EB}	V_{EB} = 3 V	0.75	pF
Collector-to-Base Capacitance, C_{CB}	V_{CB} = 3 V	0.46	pF
Collector-to-Substrate Capacitance, C_{CI}	V_{CI} = 3 V	3.2	pF
For Each p-n-p Transistor			
Noise Figure (low frequency), NF	f = 1 kHz, I_C = 100 μA, R_S = 1 kΩ	3	dB
Low-Frequency Input Resistance, R_i	f = 1 kHz, V_{CE} = 5 V,	27	kΩ
Low-Frequency Output Resistance, R_o	I_C = 100 μA	680	kΩ
Gain-Bandwidth Product, f_T	V_{CE} = 5 V, I_C = 100 μA	6.8	MHz
Emitter-to-Base Capacitance, C_{EB}	V_{EB} = −3 V	0.85	pF
Collector-to-Base Capacitance, C_{CB}	V_{CB} = −3 V	2.25	pF
Base-to-Substrate Capacitance, C_{BI}	V_{BI} = 3 V	3.05	pF

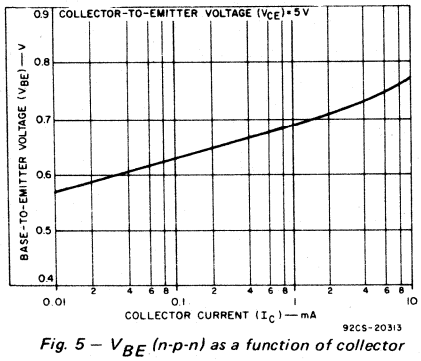


Fig. 5 – V_{BE} (n-p-n) as a function of collector current.

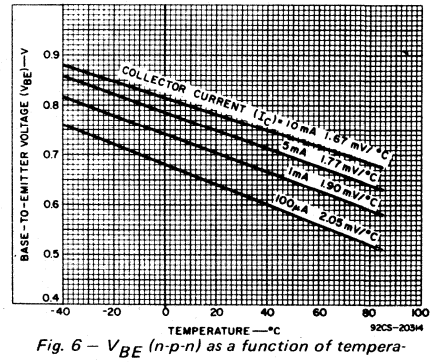


Fig. 6 – V_{BE} (n-p-n) as a function of temperature.

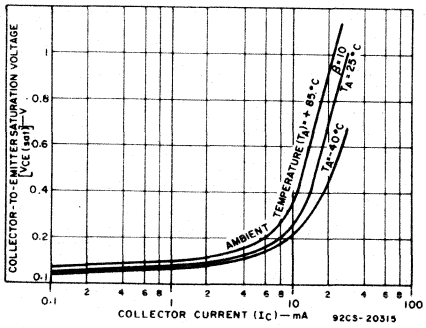


Fig. 7 – $V_{CE}(SAT)$ (n-p-n) as a function of collector current.

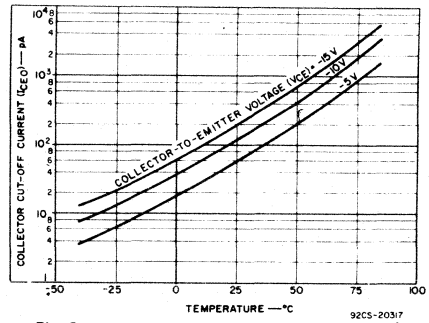


Fig. 8 – Collector cut-off current (I_{CEO}) as a function of temperature (p-n-p).

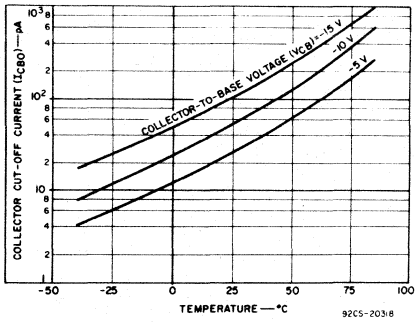


Fig. 9 – Collector cut-off current (I_{CBO}) as a function of temperature (p-n-p).

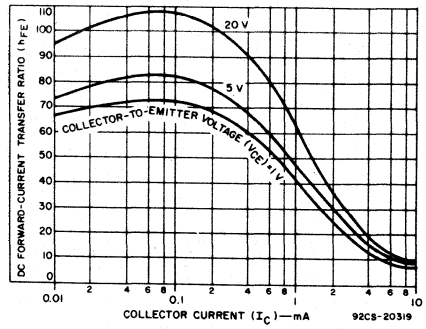


Fig. 10 – Transistor (p-n-p) h_{FE} as a function of collector current.

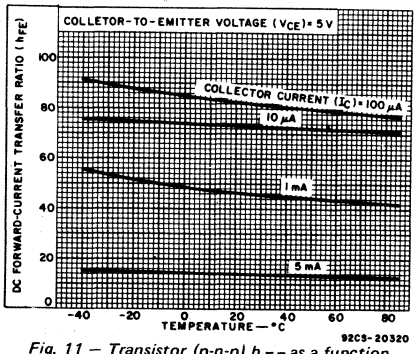


Fig. 11 – Transistor (p-n-p) h_{FE} as a function of temperature.

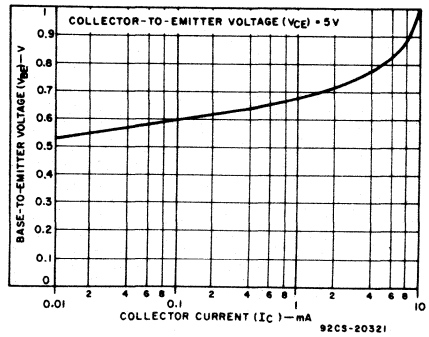


Fig. 12 – V_{BE} (p-n-p) as a function of collector current.

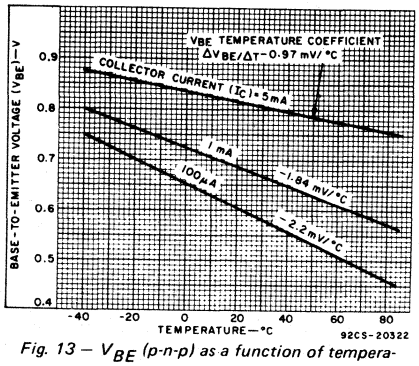


Fig. 13 – V_{BE} (p-n-p) as a function of temperature.

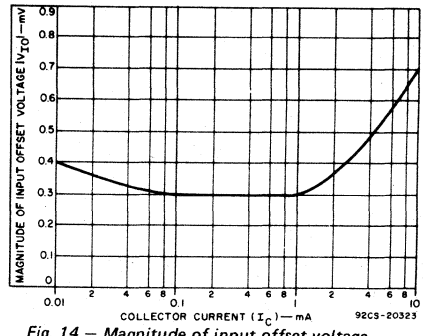


Fig. 14 – Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for n-p-n transistor Q_1–Q_2.

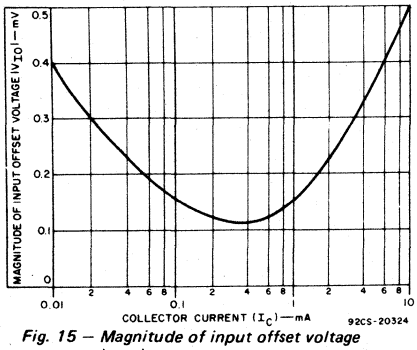


Fig. 15 – Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for p-n-p transistor Q_4–Q_5

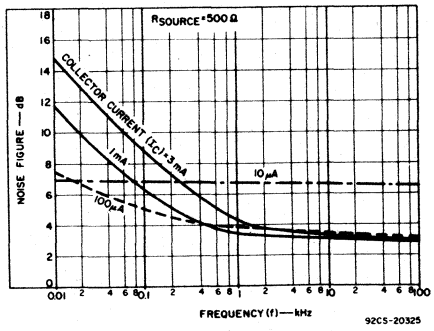


Fig. 16 – Noise figure as a function of frequency for n-p-n transistors.

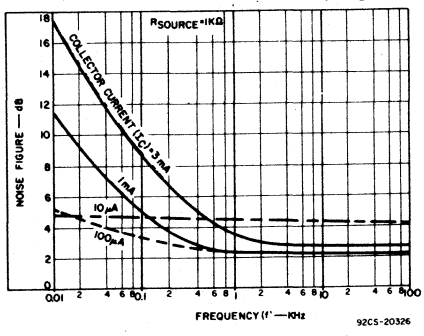


Fig. 17 – Noise figure as a function of frequency for n-p-n transistors.

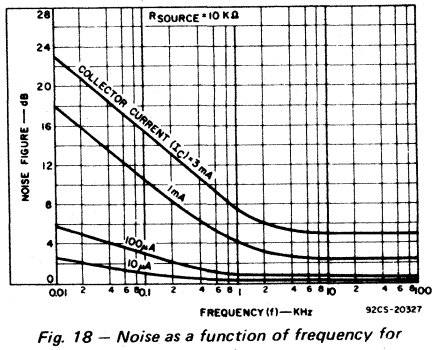


Fig. 18 – Noise as a function of frequency for n-p-n transistors.

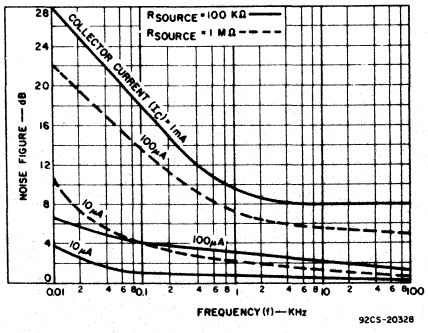


Fig. 19 – Noise figure as a function of frequency for n-p-n transistors.

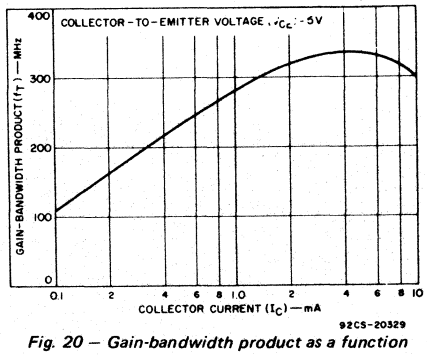


Fig. 20 – Gain-bandwidth product as a function of collector current (n-p-n).

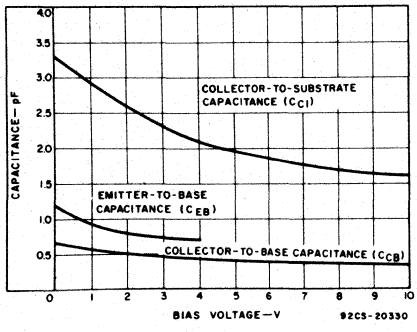


Fig. 21 – Capacitance as a function of bias voltage (n-p-n).

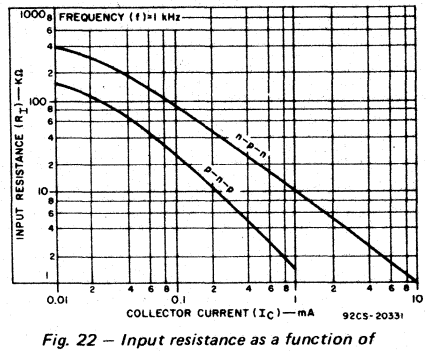


Fig. 22 – Input resistance as a function of collector current.

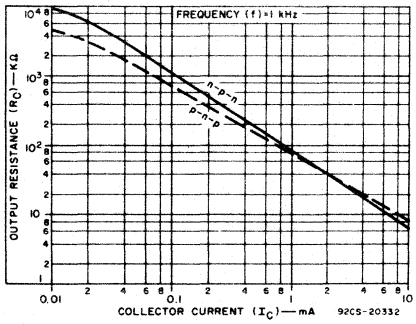


Fig. 23 – Output resistance as a function of collector current.

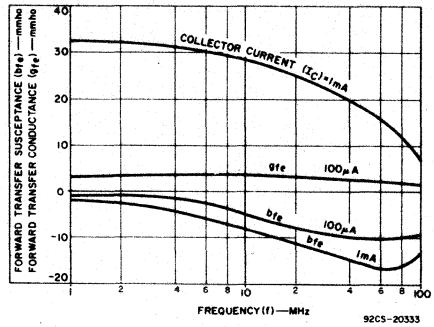


Fig. 24 – Forward transconductance as a function of frequency.

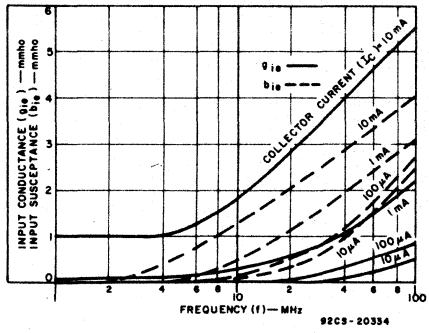


Fig. 25 – Input admittance as a function of frequency.

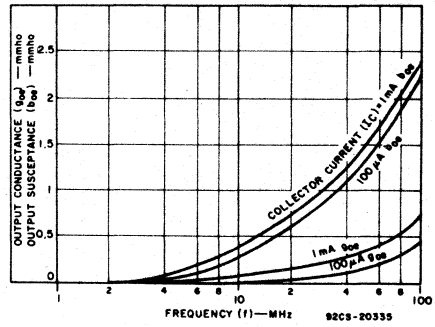


Fig. 26 – Output admittance as a function of frequency.

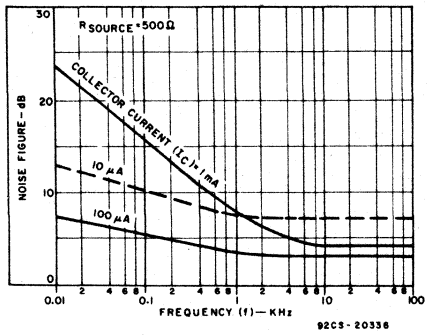


Fig. 27 – Noise figure as a function of frequency (p-n-p).

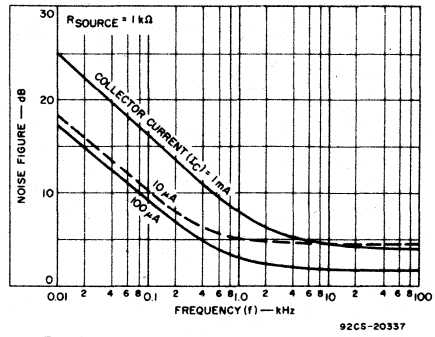


Fig. 28 – Noise figure as a function of frequency (p-n-p).

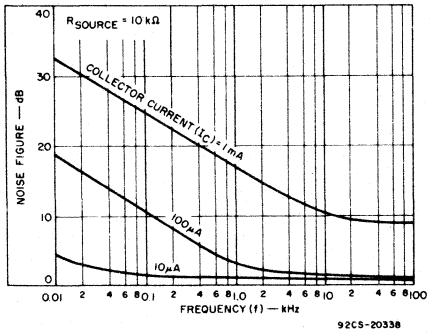


Fig. 29 – Noise figure as a function of frequency (p-n-p).

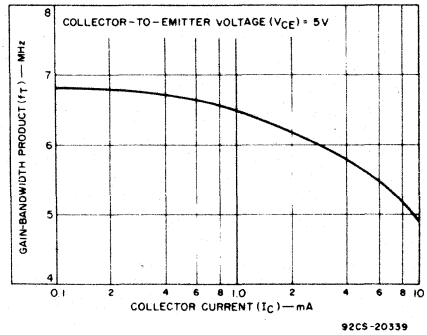


Fig. 30 – Gain-bandwidth product as a function of collector current (p-n-p).

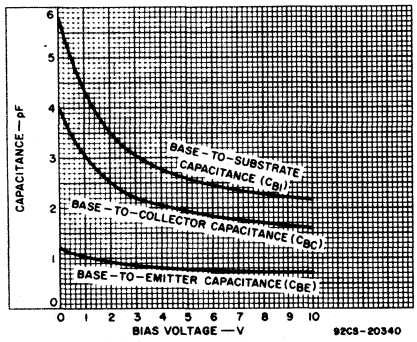


Fig. 31 – Capacitance as a function of bias voltage (p-n-p).

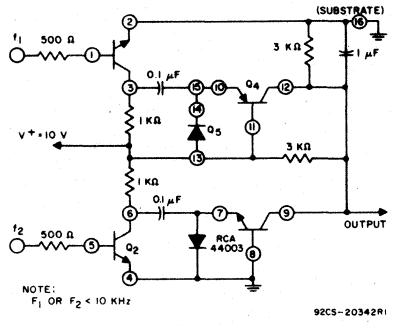


Fig. 32 – Frequency comparator using CA3096E.

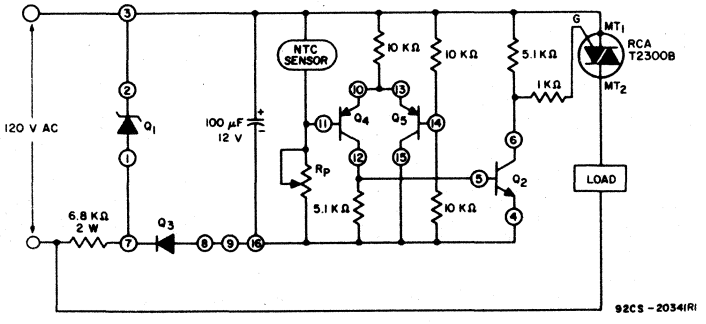


Fig. 33 – Line-operated level switch using CA3096AE or CA3096E.

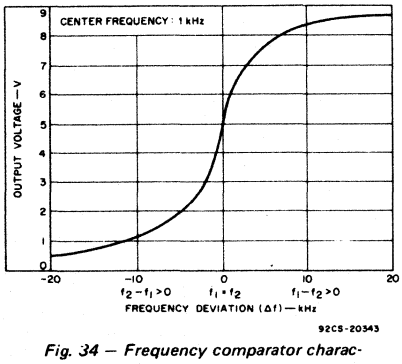


Fig. 34 – Frequency comparator characteristics.

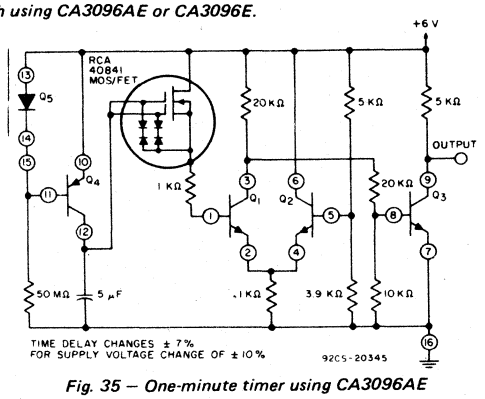


Fig. 35 – One-minute timer using CA3096AE and a MOS/FET.

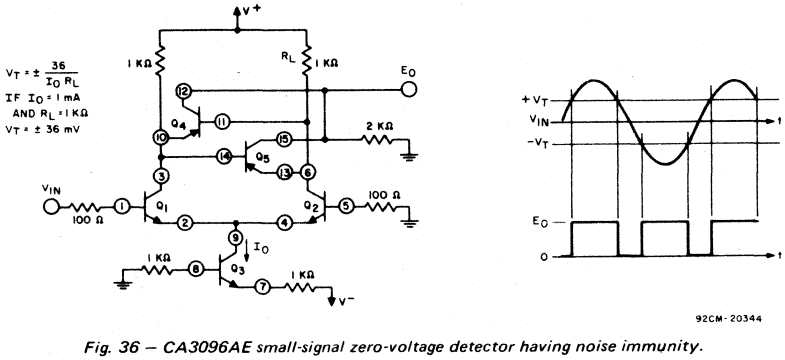


Fig. 36 – CA3096AE small-signal zero-voltage detector having noise immunity.

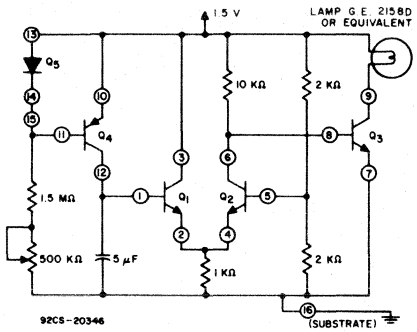


Fig. 37 – Ten-second timer operated form 1.5-volt supply using CA3096E.

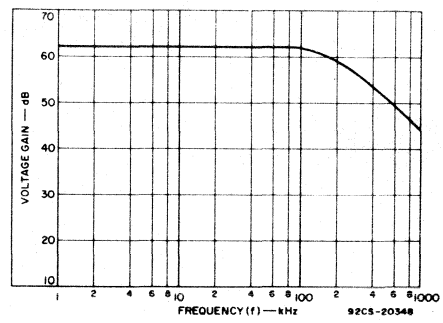


Fig. 38 – Gain-frequency characteristics.

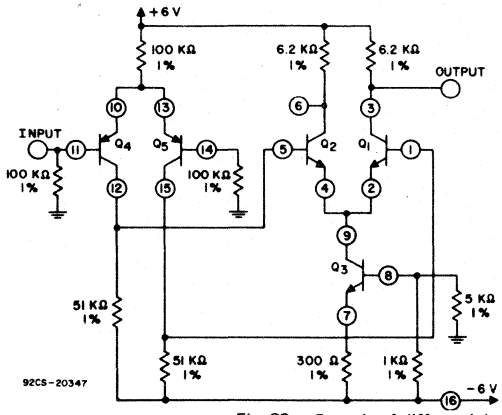
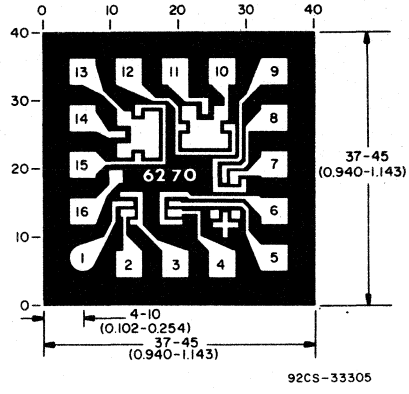


Fig. 39 – Cascade of differential amplifiers using CA3096AE.

Features:

1. Can be operated with either dual supply or single supply.
2. Wide-input common-mode range +5 V to −5 V.
3. Low bias current: $<1\ \mu A$.

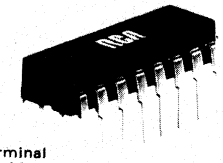


CA3096H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3097E



16-Lead Dual-In-Line Plastic Package

Thyristor/Transistor Array

For Military, Commercial, and Industrial Applications

Includes:

- *Uncommitted n-p-n transistor*
- *Sensitive-gate silicon controlled rectifier*
- *Programmable unijunction transistor (PUT)*
- *p-n-p/n-p-n transistor pair*
- *Zener diode*
- *Separate substrate connection*

Features:

- *Complete isolation between elements*
- *n-p-n transistor - V_{CEO} = 30 V (min.) I_C = 100 mA (max.)*
- *p-n-p/n-p-n transistor pair - beta ≥ 8000 (typ.) @ I_C = 10 mA, individual p-n-p, n-p-n, or transistor pair operation*
- *Programmable unijunction transistor [PUT] - peak-point current = 15 nA (typ.) at R_G = 1 MΩ; V_{AK} = ± 30 V*
- *(PUT) Extremely long RC time constants with low value of external capacitor*
- *Sensitive-gate silicon controlled rectifier (SCR) - 150 mA forward current (max.)*
- *Zener-diode impedance (Z_Z) = 15Ω (typ.) at 10 mA*

Applications:

- *Timers*
- *Light dimmers/motor controls*
- *Oscillators*
- *"One-shot" multivibrators*
- *Voltage regulators*
- *Comparators, Schmitt triggers*
- *Constant-current sources*
- *Amplifiers*
- *Logic circuits*
- *SCR triggering*
- *Pulse circuits*

RCA-CA3097E* Thyristor/Transistor Array is a monolithic integrated circuit that enables circuit designers to further integrate control systems. The CA3097E consists of five independent and completely isolated elements on one chip: an n-p-n transistor, a p-n-p/n-p-n transistor pair, a zener diode, a programmable unijunction transistor (PUT), and a sensitive-gate silicon controlled rectifier (SCR).

The CA3097 is supplied in either the 16-lead dual-in-line plastic package ("E" suffix) or the chip version ("H" suffix), and operates over the full military-temperature range of −55 to +125° C.

*Formerly Dev. No. TA6281.

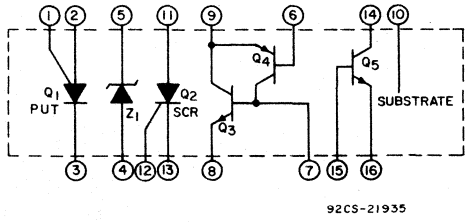


Fig. 1 — Schematic diagram of CA3097E.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

Isolation Voltage, any terminal to substrate*	+50 V
Dissipation, Total Package:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/°C
Ambient Temperature Range:	
Operating	−55 to +125°C
Storage	−65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265 °C
Each n-p-n Transistor (Q3,Q5)	
The following ratings apply with terminals 6 & 9 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	30 V
Collector-to-Base Voltage (V_{CBO})	50 V
Emitter-to-Base Voltage (V_{EBO})	5 V
Collector Current (I_C)	100 mA
Base Current (I_B)	20 mA
Dissipation (P_D)	500 mW
p-n-p Transistor (Q4)	
The following ratings apply with terminals 7 & 8 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	−40 V
Collector-to-Base Voltage (V_{CBO})	−50 V
Emitter-to-Base Voltage (V_{EBO})	−40 V
Collector Current (I_C)	−10 mA
Base Current (I_B)	−3 mA
Dissipation (P_D)	200 mW
p-n-p/n-p-n Transistor Pair (Q3,Q4)	
Dissipation (P_D)	500 mW
Programmable Unijunction Transistor, PUT (Q1)	
Gate-to-Cathode Positive Voltage (V_{GK})	30 V
Gate-to-Cathode Negative Voltage (V_{GKR})	5 V
Gate-to-Anode Negative Voltage (V_{GA})	30 V
Anode-to-Cathode Voltage (V_{AK})	±30 V
DC Anode Current	150 mA
Peak Anode Non-Recurrent Forward (On-State) Current (10 μs pulse)	2 A
Total Average Dissipation	300 mW
Silicon Controlled Rectifier, SCR (Q2)	
Repetitive Peak Reverse Voltage (V_{RRXM}), R_{GK} = 1 KΩ	30 V
Repetitive Peak Off-State Voltage (V_{DRXM}), R_{GK} = 1 kΩ	30 V
DC On-State Current (I_{TDC})	150 mA
Peak Surge (Non-Repetitive) On-State Current (10 μs pulse)	2 A
Forward Peak Gate Current (I_{GFM})	20 mA
Peak Gate-to-Cathode Reverse Voltage (V_{GRM})	5 V
Total Average Dissipation	300 mW
Zener Diode, (Z1)	
DC Current (I_Z)	25 mA
Dissipation (P_D)	250 mW

* One or more of the terminals of each element of the CA3097E is isolated from the substrate by a junction diode. In order to maintain electrical isolation between elements, the substrate terminal must be connected to a voltage which is no more positive than that of any other terminal. To avoid undesirable coupling between elements, the substrate terminal (terminal 10) should be maintained at either dc or signal (ac) ground.

CA3097E

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
n-p-n TRANSISTORS Q3, Q5 (TERMINALS 6 and 9 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = 10 V, I_E = 0		–	–	1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = 10 V, I_B = 0		–	–	10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = 100μA, I_B = 0		30	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0		50	–	–	V
COLLECTOR-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0		50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = 100μA, I_C = 0		5	7.5	10	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE(SAT)}$	I_C = 50mA, I_B = 5mA	5	–	–	0.65	V
		I_C = 10mA, I_B = 1 mA		–	0.10	–	
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE(SAT)}$	I_C = 10mA, I_B = 1mA	2	–	0.76	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.73	0.85	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = 3V, I_C = 10mA	4	100	130	–	
		V_{CE} = 3V, I_C = 50mA		80	120	–	
p-n-p TRANSISTOR Q4 (TERMINALS 7 and 8 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = -10 V, I_E = 0		–	–	–1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = -10 V, I_B = 0		–	–	–10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = -100μA, I_B = 0		–40	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = -10μA, I_E = 0		–50	–	–	V
EMITTER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)EIO}$	I_{EI} = 10μA, I_B = 0, I_E = 0		–50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = –10μA, I_C = 0		–40	–	–	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE(SAT)}$	I_C = -1mA, I_B = -100μA	6	–	–	–0.33	V
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE(SAT)}$	I_C = -1mA, I_B = –100μA	7	–	–0.7	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = -3 V, I_C = –100μA	8	–0.5	–0.6	–0.7	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = – 3 V, I_C = –100μA	9	30	60	–	
		V_{CE} = –3 V, I_C = –1 mA		40	–	–	
n-p-n/p-n-p TRANSISTOR PAIR Q3, Q4							
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} (n-p-n) = 3V, I_C = 10mA	10	–	8000	–	
		V_{CE} (n-p-n) = 3V, I_C = 50mA	10	–	6500	–	

ELECTRICAL CHARACTERISTICS (Cont'd.)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
PROGRAMMABLE UNIJUNCTION TRANSISTOR (PUT), Q1							
OFFSET VOLTAGE	V_T*	V_S = 10V, R_G = 10kΩ	11,22[a]	0.2	–	0.7	V
		V_S = 10V, R_G = 1MΩ		0.2	–	0.7	
ANODE-TO-CATHODE ON-STATE VOLTAGE	V_F	I_F = 50mA	12	–	0.90	1.5	V
		I_F = 100mA		–	1	–	
PEAK OUTPUT VOLTAGE	V_{OM}	C = 0.22μF Anode Supply Voltage = 20V	13,23	–	10	–	V
PEAK-POINT CURRENT	I_P	V_S = 10V, R_G = 10kΩ	14,22[a]	–	0.55	1	μA
		V_S = 10V, R_G = 1MΩ	–	–	0.015	0.15	
VALLEY-POINT CURRENT	I_V	V_S = 10V, R_G = 10kΩ	17,15	4	40	–	μA
		V_S = 10V, R_G = 1MΩ	16	–	–	25	
GATE REVERSE CURRENT	I_{GAO}	V_S = 30V	22[c]	–	0.02	–	nA
GATE REVERSE CURRENT	I_{GKS}	Anode-To-Cathode Short, V_S, = 30V	22[d]	–	0.2	–	nA
OUTPUT PULSE RISE TIME	t_r	Anode-Supply Voltage = 20V C = 0.22 μF	23	–	60	–	ns
SILICON CONTROLLED RECTIFIER (SCR), Q2							
PEAK OFF-STATE CURRENT: FORWARD	I_{DXM}	V_{DRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	μA
REVERSE	I_{RXM}	V_{RRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	
FORWARD DC VOLTAGE DROP	V_T	I_T = 50 mA	18	–	0.90	1.5	V
GATE-TO-SOURCE TRIGGER CURRENT	I_{GS}	T_A = 25°C	26	–	33	100	μA
		T_A = −55°C	26	–	50	–	
DC GATE-TRIGGER VOLTAGE	V_{GT}	V_L = 10V, R_L = 100Ω	19	–	0.55	0.75	V
HOLDING CURRENT	I_{HO}	R_{GK} = 1kΩ	20,24	–	1.2	–	mA
CRITICAL RATE-OF-RISE OF OFF-STATE VOLTAGE	dv/dt	EXPONENTIAL RISE, R_{GK} = 1kΩ, V_{DRXM} = 30V	25	–	150	–	V/μs
GATE-CONTROLLED TURN-ON TIME	t_{gt}	See Fig. 33	33	–	50	–	ns
CIRCUIT-COMMUTATED TURN-OFF TIME	t_q	See Fig. 33	33	–	10	–	μs
ZENER DIODE, Z1							
ZENER VOLTAGE	V_Z	I_Z = 10mA	21	7.2	8	8.8	V
ZENER IMPEDANCE	Z_Z	I_Z = 10mA, f = 1kHz		–	15	25	Ω
ZENER VOLTAGE TEMPERATURE COEFFICIENT	$(\Delta V_Z/V_Z)/\Delta T$	I_Z = 10mA		–	+0.05	–	%/°C
	$\Delta V_Z/\Delta T$			–	+4	–	mV/°C
ZENER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)ZIO}$	I_Z = 100μA TERM. 5 TO SUBSTRATE		50	80	– –	V

* $V_T = V_P - V_S$ (Fig. 22)

CA3097E

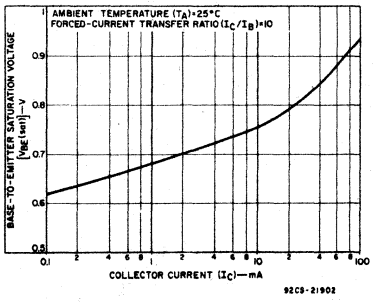


Fig. 2 – Base-to-emitter saturation voltage vs. collector current for n-p-n transistors Q3 & Q5.

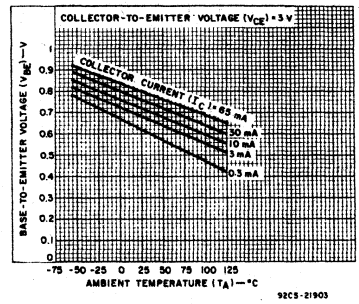


Fig. 3 – Base-to-emitter voltage vs. ambient temperature for n-p-n transistors Q3 & Q5.

TYPICAL CHARACTERISTICS

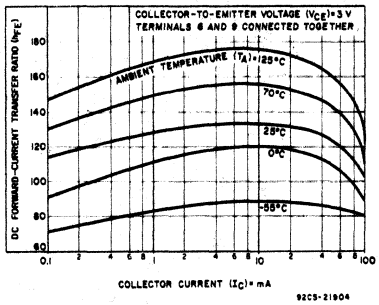


Fig. 4 – DC forward-current transfer ratio vs. collector current for n-p-n transistors Q3 & Q5.

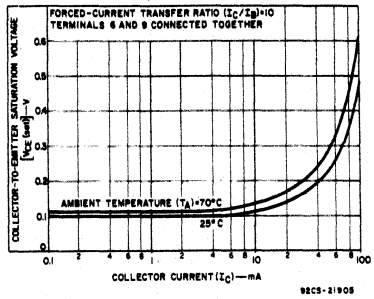


Fig. 5 – Collector-to-emitter saturation voltage vs. collector current for n-p-n transistors Q3 & Q5.

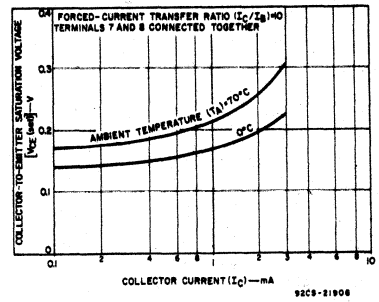


Fig. 6 – Collector-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.

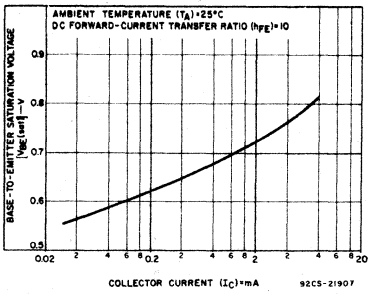


Fig. 7 – Base-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.

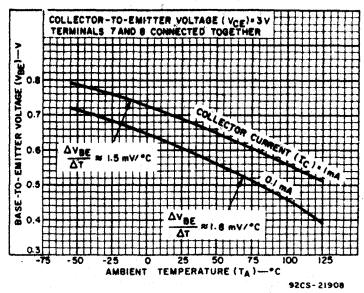


Fig. 8 – Base-to-emitter voltage vs. ambient temperature for p-n-p transistor Q4.

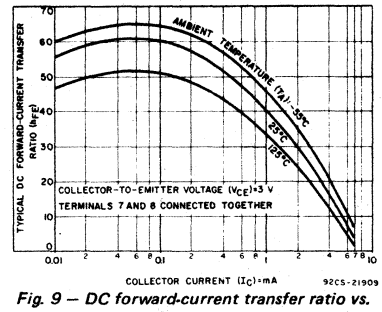


Fig. 9 – DC forward-current transfer ratio vs. collector current for p-n-p transistor Q4.

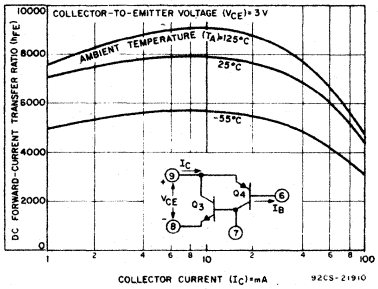


Fig. 10 – DC forward-current transfer ratio vs. collector current for transistor pair Q3, Q4.

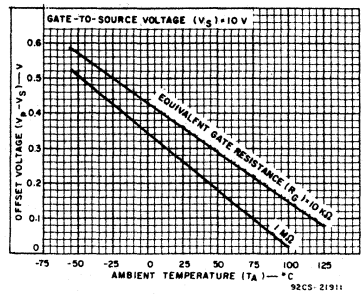


Fig. 11 – Offset voltage vs. ambient temperature for Q1 (PUT).

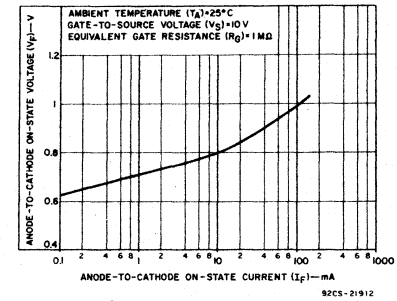


Fig. 12 – Anode-to-cathode on-state voltage vs. anode-to-cathode on-state current for Q1 (PUT).

TYPICAL CHARACTERISTICS (CONT'D)

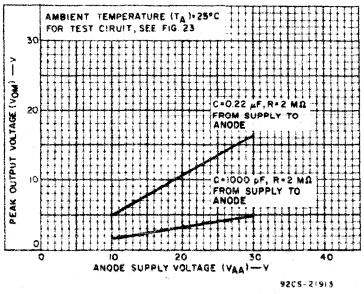


Fig. 13 – Peak output voltage vs. anode supply voltage for Q1 (PUT).

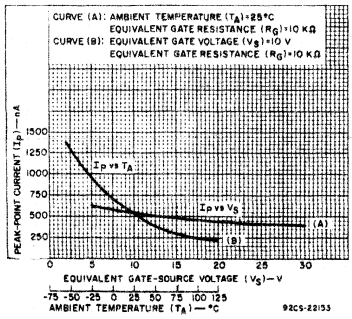


Fig.14 – Peak-point current vs. gate-source voltage and ambient temperature for Q1 (PUT).

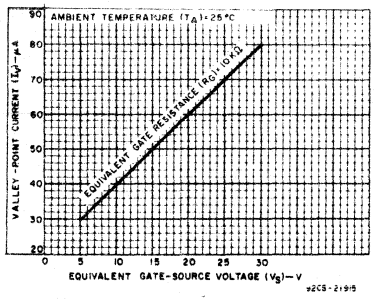


Fig.15 – Valley-point current vs. gate-source voltage for Q1 (PUT).

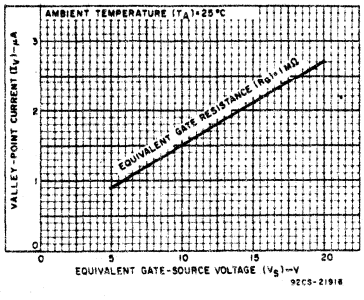


Fig.16 – Valley-point current vs. gate-source voltage for Q1 (PUT).

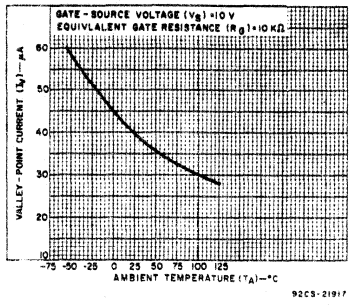


Fig. 17 – Valley-point current vs. ambient temperature for Q1 (PUT).

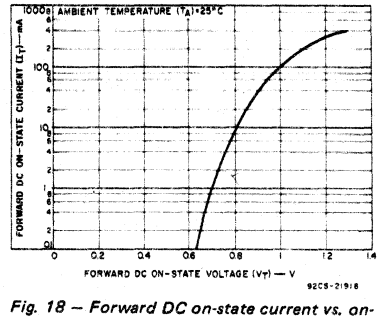


Fig. 18 – Forward DC on-state current vs. on-state voltage for Q2 (SCR).

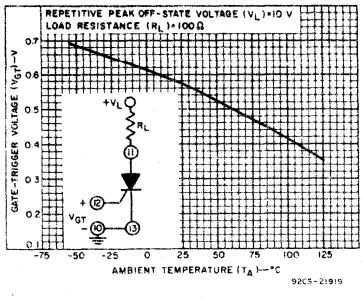


Fig. 19 – Gate-trigger voltage vs. ambient temperature for Q2 (SCR).

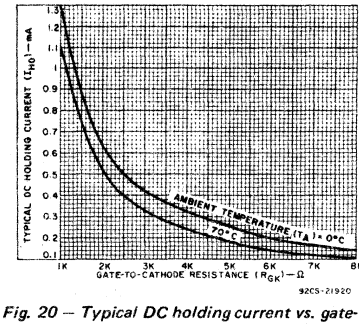


Fig. 20 – Typical DC holding current vs. gate-to-cathode resistance for Q2 (SCR).

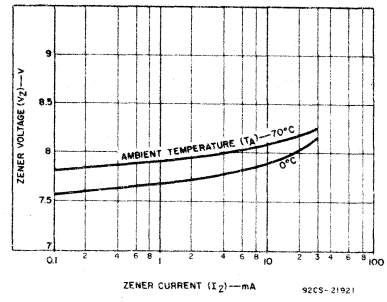


Fig. 21 – Zener voltage vs. zener current for Z1.

OPERATING CONSIDERATIONS FOR CA3097E

1. Composite p-n-p/n-p-n Transistors Q3, Q4 (See Fig. 3)

To use Q3 as an individual n-p-n transistor, join terminals no. 6 and no. 9 to disable p-n-p transistor Q4.

The appropriate terminal connections are then:

Collector..... terminal 9
Base ..... terminal 7
Emitter..... terminal 8

To use Q4 as an individual p-n-p transistor, join terminals no. 7 and no. 8 to disable n-p-n transistor Q3.

The appropriate terminal connections are then:

Collector..... terminal 7
Base ..... terminal 6
Emitter..... terminal 9

To use Q3 and Q4 as a composite use terminals 6, 7, 8, and 9 as required.

2. Programmable Unijunction Transistor Q1 (PUT)

The programmable unijunction transistor is essentially an anode-gate SCR. The volt-ampere characteristic of the device is shown in Fig. 22. When an equivalent Thevenin source (V_S, R_G), as shown in Fig. 22, is applied to the gate terminal the device will be "off" if the anode-voltage is negative with respect to the gate voltage. Under this condition, any current flow is exclusively leakage current. When the anode voltage becomes more positive than the gate voltage by an increment equal to the threshold voltage (V_T = 0.4 V typ.), the device can turn "on" only if the current available at the anode terminal **is greater** than the specified peak-point current. The PUT will then switch through its negative-resistance region to the "on" state (low anode-to-gate voltage). It should be noted that I_P is not the maximum current allowed through the device, but is the current required at the peak of the V-I curve. I_P is typically a very low value of current.

After the PUT has switched to its low-impedance state, the device will remain "on" if the anode-current (I_A) exceeds the valley-point current (I_V). If $I_A < I_V$, the PUT will switch back to its high-impedance "off" state. Thus, the PUT can be made to "latch" or recover, depending on I_V. Since I_V is a function of the "on"-state gate current (which depends on R_G and V_S) a choice of R_G and/or V_S will determine the operating mode, i.e., "off" state→"on" state or "off" state → "on" state → "off" state. The value of I_V increases directly as a function of V_G and inversely with R_G. The PUT in the CA3097E has a low I_P.....I_P = 15 nA at V_S = 10 V, R_G = 1 MΩ. This low value of I_P indicates that an extremely large value of anode-supply resistor, e.g. 60 MΩ (typ.), can be used in timing circuits requiring long RC time constants. This becomes important when considering the size of the external

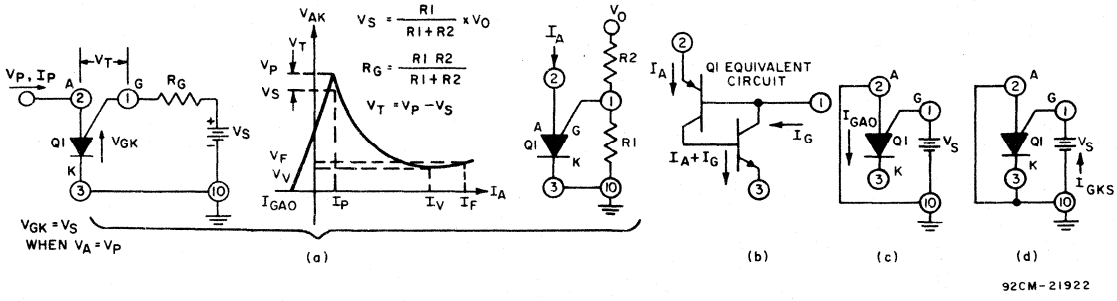


Fig. 22 – General anode characteristics for Q1 (PUT).

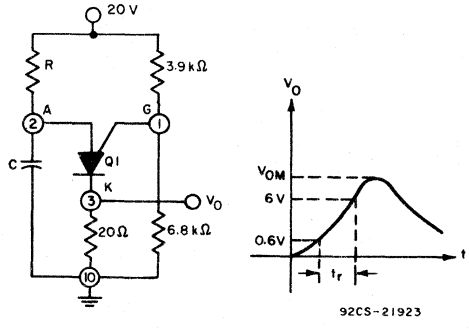


Fig. 23 – Output pulse characteristics for Q1 (PUT).

OPERATING CONSIDERATIONS (CONT'D)

timing capacitor to be used. Consequently, the use of the PUT in the CA3097E is advantageous since it has a lower I_P than most discrete PUT's.

Temperature Compensation of Switching Point

As described previously, the PUT will switch to its low-impedance state when its anode voltage is approximately a diode-drop above the gate voltage. Since the anode-to-gate threshold voltage vs. temperature characteristic is similar to that of a typical silicon-diode junction, a compensating series diode such as used in the circuit of Fig. 29 (Z1 connected as forward-biased diode) considerably reduces the effect of temperature on the switching point.

Bypassing Anode Current

If the PUT gate equivalent source is such that $I_A > I_V$, the PUT will remain "on". A method for turning the PUT off is by shunting current away from the anode until $I_A < I_V$. An example of this technique is the oscillator circuit of Fig. 29. Q3 transistor is turned "on" after the PUT fires and shunts current away from the anode, thereby forcing $I_A < I_V$. The PUT then turns "off" allowing C_T to recharge through R_T, to repeat the cycle.

Protecting The PUT Against Discharge Current Of The Capacitor

A current-limiting resistor in series with the PUT is normally required to dissipate capacitive discharge energy (see Figs. 23 and 29).

Silicon Controlled Rectifier, Q2 (SCR)

The SCR should be used with a 1 kΩ (or less) resistor connected between the cathode and gate terminals if the SCR is to be subjected to its maximum forward and reverse voltage ratings (V_{DXM} and V_{RXM}). Selecting a value for R_{GK} of 1 kΩ (or lower) increases the capability of the device to withstand greater dv/dt and increases the noise immunity of the SCR against false triggering at the gate. Practical considerations such as available current drive from the triggering devices (e.g., a PUT) will determine the lowest value of R_{GK} at which the SCR will fire with a $V_{GK} \approx 0.55$ V. With a value of 500Ω for R_{GK}, the trigger source must be capable of supplying 1.1 mA. R_{GK} should be non-inductive within the frequency band of the noise transients normally encountered in a particular application.

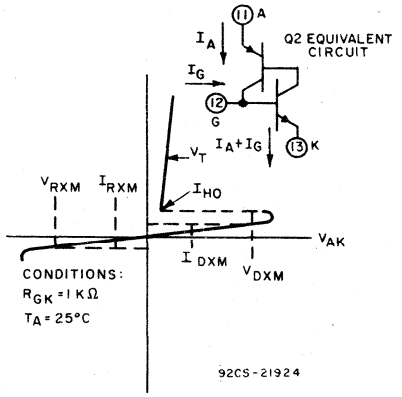


Fig. 24 – Principle voltage-current characteristics for Q2 (SCR).

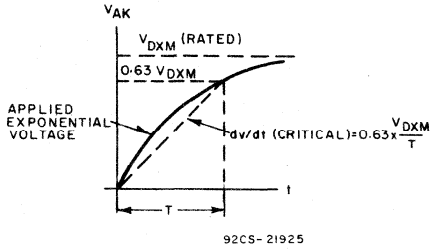
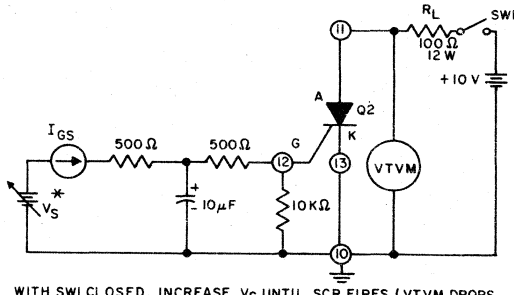


Fig. 25 – Definition of critical rate of rise of off-state voltage for Q2 (SCR).



WITH SWI CLOSED, INCREASE V_S UNTIL SCR FIRES (VTVM DROPS FROM 10V TO APPROXIMATELY 1V). I_{GS} (TRIGGER) IS MEASURED JUST PRIOR TO THIS TRIGGERING POINT. NOTE THAT I_{GS} MAY DECREASE AS V_S IS INCREASED DUE TO CURRENT DRAWN OUT OF THE GATE TERMINAL OF THE SCR AS IT TURNS ON. TO UNLATCH THE SCR OPEN SWI.

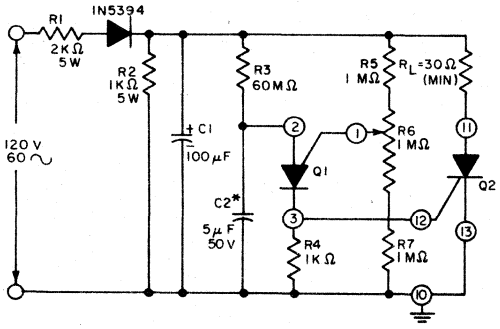
* V_S SHOULD BE CAPABLE OF SUPPLYING MILLIVOLT INCREMENTS NEAR THE TRIGGER POINT

92CS-21926

Fig. 26 – Test circuit for determining I_{GS} in Q2 (SCR).

CA3097E

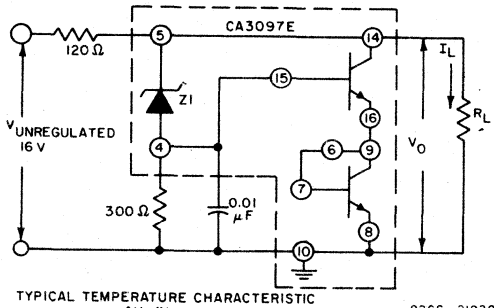
APPLICATIONS CIRCUITS



TIMING PERIOD ≈ 200 SEC. WITH 1 MΩ POT CENTERED
TIMING CYCLE BEGINS WHEN AC IS APPLIED
* SPRAGUE TYPE 4308, 5 μF AT 50 V
SPRAGUE TYPE 6308, 5 μF AT 50 V
OR EQUIVALENT

92CS-21927

Fig. 27 – AC line-operated one-shot timer.



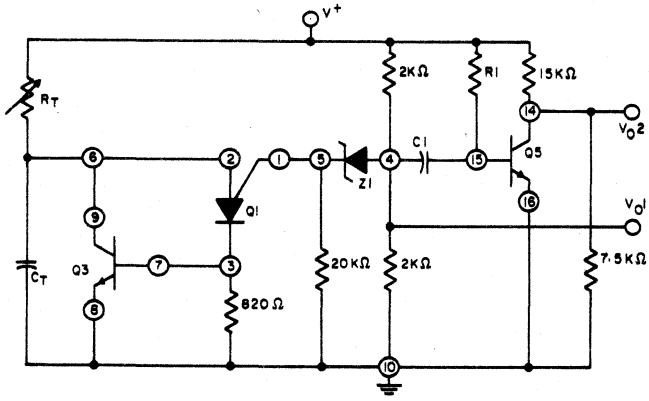
TYPICAL TEMPERATURE CHARACTERISTIC
@ $R_L = 330\,\Omega$, $\frac{\Delta V_O/V_O}{\Delta T} \times 100 = \pm 0.01\,\%/°C$

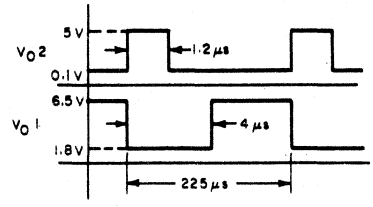
92CS-21928

TYP. LOAD REGULATION @ $I_L = 0$ TO 40 mA, $(\Delta V_O/V_O) \times 100 = -3\,\%$ (NO LOAD TO FULL LOAD)

TYP. LINE REGULATION @ $R_L = 330\,\Omega$, $\frac{\Delta V_O/V_O}{\Delta V_{UNREG.}} \times 100 = \pm 0.55\,\%/V$

Fig. 28 – Temperature-compensated shunt regulator.





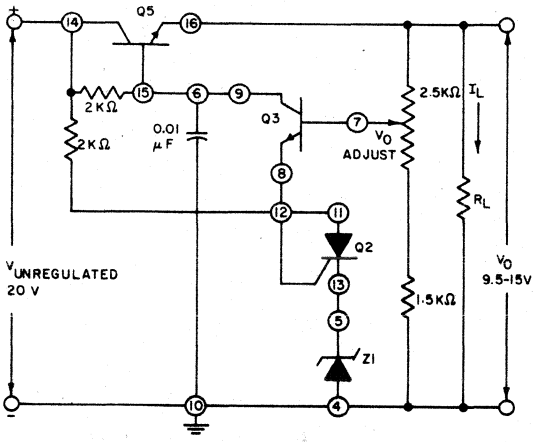
PULSE RATE ADJUSTED BY VARYING R_T OR C_T.
OUTPUT PULSE WIDTH ADJUSTED BY R_1C_1 DIFFERENTIATING TIME CONSTANT

TYPICAL OPERATION FOR:
$V^+ = 15$ V, $C_T = 0.1\,\mu F$, $R_T = 4.3\,K\Omega$
$C_1 = 82$ pF, $R_1 = 60K\Omega$

92CM-21929

Fig. 29 – Pulse generator.

APPLICATIONS CIRCUITS



TYPICAL LOAD REGULATION @ V_O = 12 V, I_L = 0 TO 40 mA

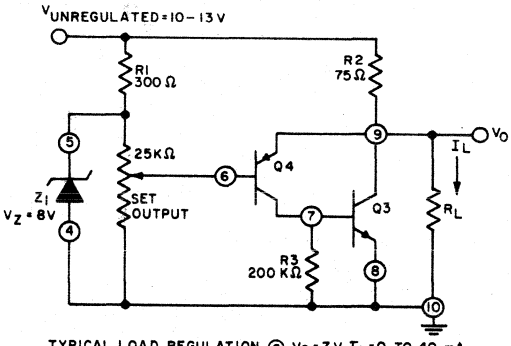
$$\frac{\Delta V_O}{V_O} \times 100 = \pm 0.4\ \%$$ (NO LOAD TO FULL LOAD)

TYPICAL LINE REGULATION @ V_O = 12 V

$$\frac{\Delta V_O / V_O}{\Delta V_{UNREG.}} \times 100 = \pm 0.45\ \%/V$$

92CS-21930

Fig. 30 – Series voltage regulator.



TYPICAL LOAD REGULATION @ V_O = 7 V, I_L = 0 TO 40 mA

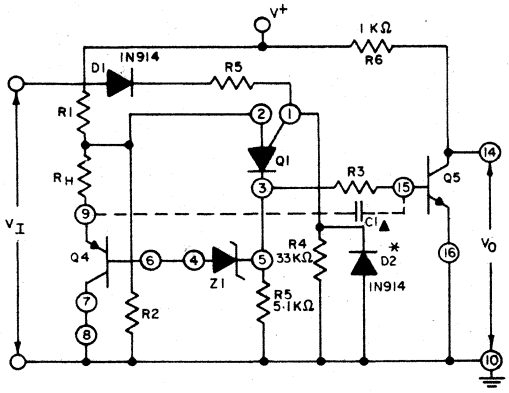
$$\frac{\Delta V_O}{V_O} \times 100 = -1.1\ \%$$

TYPICAL LINE REGULATION @ V_O = 7 V, I_L = 20 mA

$$\frac{\Delta V_O}{\Delta V_{UNREGULATED}} = \pm 0.85\ \%/VOLT$$

92CS-21931

Fig. 31 – 5 to 7.5 V shunt regulator.

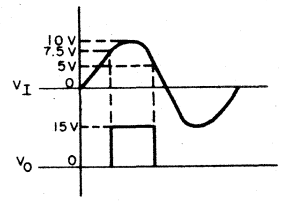


▲ OPTIONAL SPEED-UP CAPACITOR
* REQUIRED IF V_I SWINGS BELOW GROUND

TYPICAL OPERATING CONDITIONS:
FREQUENCY IN = 0 – 10 KHz
SUPPLY VOLTAGE (V^+) = 15 V
R1, R2, R_H = 5.1 KΩ
R3 = 6.2 KΩ, R_S = 300 Ω
C_I = 820 pF
$V_{TH}U$ = 7.5 V, $V_{TH}L$ = 5 V
HYSTERESIS VOLTAGE = 2.5 V
UPPER THRESHOLD VOLTAGE ($V_{TH}U$) $\approx V^+ \frac{R2}{R1+R2}$

LOWER THRESHOLD VOLTAGE ($V_{TH}L$) $\approx \frac{(V^+)\left(\frac{R2\,R_H}{R2+R_H}\right)}{\frac{R2\,R_H}{R2+R_H}+R1}$

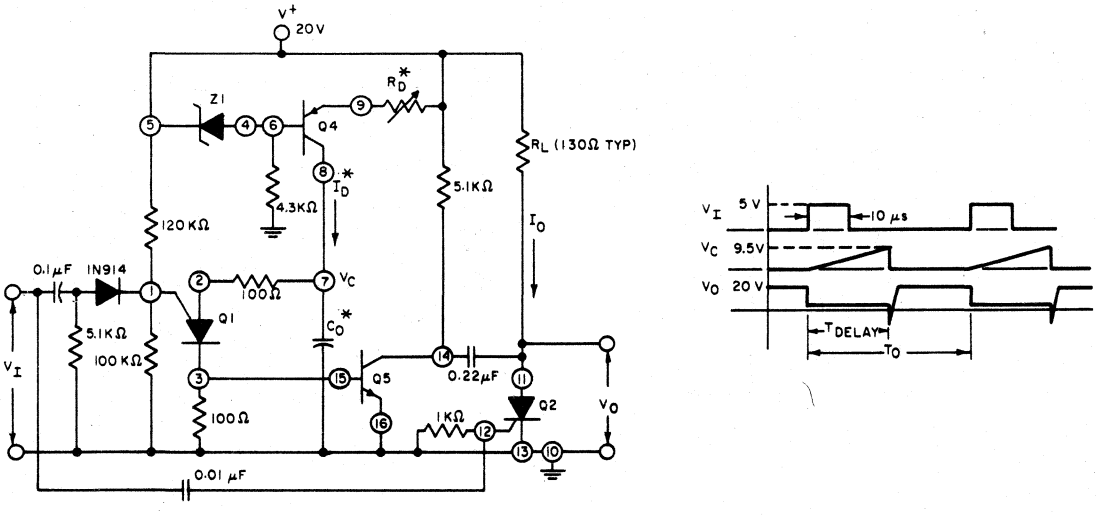
HYSTERESIS VOLTAGE = $V_{TH}U - V_{TH}L$



92CM-21932

Fig. 32 – Schmitt trigger.

APPLICATIONS CIRCUITS (CONT'D)

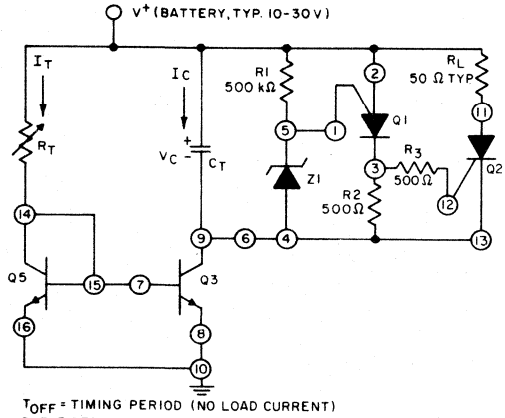


*MONOSTABLE DELAY TIME SET BY ADJUSTMENT OF I_D (VARY R_D) OR BY $C_D.I_D$ MUST BE GREATER THAN I_V OF Q1 (PUT) FOR MONOSTABLE OPERATION.

Q2 (SCR) SWITCHING TIMES:
GATE-CONTROLLED TURN-ON TIME (t_{gt}) = 50 ns (TYP.)
CIRCUIT-COMMUTATED TURN-OFF TIME (t_q) = 10 μs (TYP)

92CM-21933

Fig. 33 – Monostable multivibrator with variable delay.



T_{OFF} = TIMING PERIOD (NO LOAD CURRENT)
PUT FIRES WHEN $V_C \approx 8$ V

$V_C = \frac{I_C (T_{OFF})}{C_T}$, $I_C \approx I_T$ (Q3, Q5 MATCHED)

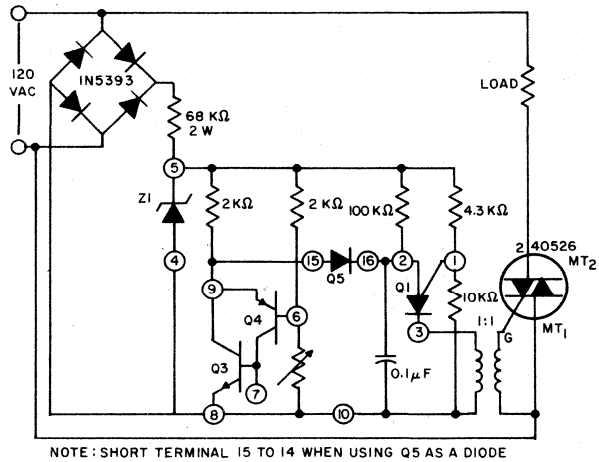
I_T SET BY ADJUSTING R_T, $I_T \approx \frac{V^+ - 0.7}{R_T}$

T_{ON} = CAPACITOR DISCHARGE TIME THROUGH LOAD. LOAD TURNS OFF WHEN SCR ANODE CURRENT FALLS BELOW HOLDING CURRENT (I_{HO}). TYPICAL I_{HO} = 1.2 mA

EXAMPLE: FOR TIMING PERIOD OF 8.3 MIN
C_T = 1000 μF, I_T = 16 μA
$R_T = \frac{V^+ - 0.7}{I_T}$ (FOR V^+ = 16 V, $R_T \approx$ 1 MΩ)

92CS-21934

Fig.34 – Low-current-drain battery-operated long interval astable timer.



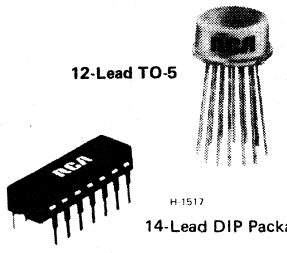
NOTE: SHORT TERMINAL 15 TO 14 WHEN USING Q5 AS A DIODE

92CS-22178

Fig.35 – Phase control circuit.

CA3118, CA3146, CA3183 Types

High-Voltage Transistor Arrays



Applications

- General use in signal processing systems in DC through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- Lamp and relay drivers (CA3183AE, E)
- Thyristor firing (CA3183AE, E)

Features

- Matched general-purpose transistors
- V_{BE} matched ±5mV max.
- Operation from DC to 120 MHz (CA3118AT, T; CA3146AE, E)
- Low-noise figure: 3.2dB typ. at 1kHz (CA3118AT, T; CA3146AE, E)
- High I_C: 75mA max. (CA3183AE, E)

RCA-CA3118AT, CA3118T, CA3146AE, CA3146E, CA-3183AE, and CA3183E* are general-purpose high-voltage silicon n-p-n transistor arrays on a common monolithic substrate.

Types CA3118AT and CA3118T consist of four transistors with two of the transistors connected in a Darlington configuration. These types are well suited for a wide variety of applications in low-power systems in the DC through VHF range. Both types are supplied in a hermetically sealed 12-lead TO-5 type package and operate over the full military temperature range. (CA3118AT and CA3118T are high-voltage versions of the popular predecessor type CA3018.

Types CA3146AE and CA3146E consist of five transistors with two of the transistors connected to form a differentially-connected pair. These types are recommended for low-power applications in the DC through VHF range. Both types are supplied in a 14-lead dual-in-line plastic package and operate over the ambient temperature range of −40°C to +85°C. (CA3146AE and CA3146E are high-voltage versions of the popular predecessor type CA3046.)

Types CA3183AE and CA3183E consist of five high-current transistors with independent connections for each transistor. In addition two of these transistors (Q1 and Q2) are matched at low-current (i.e. 1mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design. Both types are supplied in a 16-lead dual-in-line plastic package and operate over the ambient temperature range of −40°C to +85°C. (CA3183AE and CA3183E are high-voltage versions of the popular predecessor type CA3083.)

The types with an "A" suffix are premium versions of their non-"A" counterparts and feature tighter control of breakdown voltages making them more suitable for higher voltage applications.

For detailed application information, see companion Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated Circuit Transistor Array."

*Formerly Developmental Types Nos.

CA3118AT	– TA6091	CA3146E	– TA6181
CA3118T	– TA6182	CA3183AE	– TA6094
CA3146AE	– TA6084	CA3183E	– TA6183

TYPE	P_T● max. mW	I_C max. mA	V_{CEO} max. V	V_{CBO} max. V	$V_{CE\ sat.}$ at 10 mA typ. V	h_{FE} at 1mA, & V_{CE}=5V typ.	V_{IO} Diff. Pair at 1mA max. mV	I_{IO} Diff. Pair at 1mA max. μA	T_A Range (Operating) °C
VALUES APPLY FOR EACH TRANSISTOR									
CA3118AT	300	50	40	50	0.33	95	±5	2	−55 – +125
CA3118T	300	50	30	40	0.33	95	±5	2	−55 – +125
CA3146AE	300	50	40	50	0.33	95	±5	2	−40 – +85
CA3146E	300	50	30	40	0.33	95	±5	2	−40 – +85
CA3183AE	500	75	40	50	0.16	75	±5	2.5	−40 – +85
CA3183E	500	75	30	40	0.16	75	±5	2.5	−40 – +85

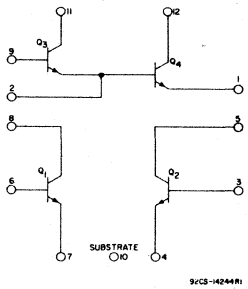
● Caution on Total Package Power Dissipation: The maximum total package dissipation rating for the CA3118 Series circuits is 450 mW at temperatures up to +85°C, then derate linearly at 5 mW°C. The maximum total package dissipation rating for the CA3146 and CA3183 Series circuits is 750 mW at temperatures up to +55°C, then derate linearly at 6.67 mW°C.

CA3118, CA3146, CA3183 Types

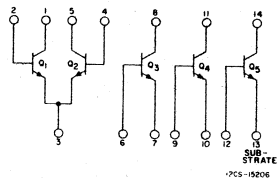
MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:		
Any one transistor –		
CA3118AT, CA3118T, CA3146AE, CA3146E	300	mW
CA3183AE, CA3183E	500	mW
Total package –		
Up to 85°C (CA3118AT, CA3118T)	450	mW
Up to 55°C (CA3146AE, CA3146E, CA3183AE, CA3183E)	750	mW
Above 85°C (CA3118AT, CA3118T)	derate linearly 5	mW/°C
Above 55°C (CA3146AE, CA3146E, CA3183AE, CA3183E)	derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating –		
CA3118AT, CA3118T	–55 to +125	°C
CA3146AE, CA3146E, CA3183AE, CA3183E	–40 to +85	°C
Storage (all types)	–65 to +150	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO}):		
CA3118AT, CA3146AE, CA3183AE	40	V
CA3118T, CA3146E, CA3183E	30	V
Collector-to-Base Voltage (V_{CBO}):		
CA3118AT, CA3146AE, CA3183AE	50	V
CA3118T, CA3146E, CA3183E	40	V
Collector-to-Substrate Voltage (V_{CIO}): ■		
CA3118AT, CA3146AE, CA3183AE	50	V
CA3118T, CA3146E, CA3183E	40	V
Emitter-to-Base Voltage (V_{EBO}) all types	5	V
Collector Current –		
CA3118AT, CA3118T, CA3146AE, CA3146E	50	mA
CA3183AE, CA3183E	75	mA
Base Current (I_B) – CA3183AE, CA3183E	20	mA

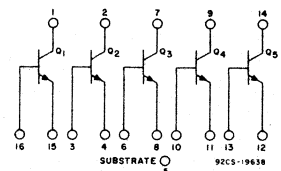
■ The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.



CA3118AT, CA3118T



CA3146AE, CA314E



CA3183AE, CA3183E

Fig. 1 – Schematic diagrams of high-voltage arrays.

COMPARISON OF RELATED PREDECESSOR TYPE WITH TYPES IN THIS DATA BULLETIN

	DATA FILE NO.	V_{CEO} min.	V_{CBO} min.	V_{CE} sat. typ. V	V_{BE} typ. V	I_C max. mA	C_{CB} typ. pF	C_{CI} typ. pF	C_{EB} typ. pF
				I_C=10 mA	I_C=1 mA				
CA3018	338	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3018A	338	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3118AT		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3118T		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C=10 mA	I_C=1 mA				
CA3046	341	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3146AE		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3146E		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C=50 mA	I_C=10 mA				
CA3083	481	15	20	0.4	0.74	100	–	–	–
CA3183AE		40	50	1.7	0.75	75	–	–	–
CA3183E		30	40	1.7	0.75	75	–	–	–

NOTE: Related predecessor types are shown in shaded areas.

STATIC ELECTRICAL CHARACTERISTICS — CA3118 and CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS $T_A = 25^oC$	Typ. Char. Curve Fig. No.	LIMITS CA3118AT, CA3146AE Min.	CA3118AT, CA3146AE Typ.	CA3118AT, CA3146AE Max.	CA3118T, CA3146E Min.	CA3118T, CA3146E Typ.	CA3118T, CA3146E Max.	UNITS
For Each Transistor:										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	–	50	72	–	40	72	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	–	40	56	–	30	56	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 10\mu A$, $I_B = 0$, $I_E = 0$	–	50	72	–	40	72	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$	–	5	7	–	5	7	–	V
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	2	–	see curve	5	–	see curve	5	μA
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	3	–	0.002	100	–	0.002	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=5V, I_C=10 mA	4	–	85	–	–	85	–	–
		V_{CE}=5V, I_C=1 mA	4	30	100	–	30	100	–	–
		V_{CE}=5V, I_C=10μA	4	–	90	–	–	90	–	–
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3V$, $I_C = 1mA$	5	0.63	0.73	0.83	0.63	0.73	0.83	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	$I_C = 10mA$, $I_B = 1mA$	6	–	0.33	–	–	0.33	–	V
For transistors Q3 and Q4 (Darlington Configeration):										
Collector-Cutoff Current (CA3118AT and CA3118T only)	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	–	–	–	5	–	–	–	μA
DC Forward-Current Transfer Ratio (CA3118AT and CA3118T only)	h_{FE}	$V_{CE} = 5V$, $I_C = 1mA$	7	1500	9000	–	1500	9000	–	–
Base-to-Emitter (Q3 to Q4)	V_{BE}	V_{CE}=5V, I_E=10mA	8	–	1.46	–	–	1.46	–	V
		V_{CE}=5V, I_E=1mA	8,9	–	1.32	–	–	1.32	–	V
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\lvert\frac{\Delta V_{BE}}{\Delta T}\right\rvert$	$V_{CE} = 5V$, $I_E = 1mA$	–	–	4.4	–	–	4.4	–	mV/°C
For transistors Q1 and Q2 (AS a Differential Amplifier):										
Magnitude of Input Offset Voltage $\lvert V_{BE1} = V_{BE2}\rvert$	$\lvert V_{IO}\rvert$	$V_{CE} = 5V$, $I_E = 1mA$	10,11	–	0.48	5	–	0.48	5	mV
Magnitude of h_{FE} Ratio (CA3118AT and CA3118T only)		$V_{CE} = 5V$, $I_{C1} = I_{C2} = 1mA$	–	0.9	1.0	1.1	0.9	1.0	1.1	–
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\lvert\frac{\Delta V_{BE}}{\Delta T}\right\rvert$	$V_{CE} = 5V$, $I_E = 1mA$	–	–	1.9	–	–	1.9	–	mV/°C
Magnitude of V_{IO} ($V_{BE1} - V_{BE2}$) Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO}}{\Delta T}\right\rvert$	$V_{CE} = 5V$, $I_{C1} = I_{C2} = 1mA$	–	–	1.1	–	–	1.1	–	μV/°C
Magnitude of Input Offset Current $\lvert I_{IO_1} - I_{IO_2}\rvert$ (CA3146AE and CA3146E only)	I_{IO}	$V_{CE} = 5V$, $I_{C_1} = I_{C_2} = 1$ mA	12	–	0.3	2	–	0.3	2	μA

CA3118, CA3146, CA3183 Types

DYNAMIC ELECTRICAL CHARACTERISTICS – CA3118 and CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C	Typ. Char. Curve Fig.No.	CA3118AT CA3146AE			CA3118T CA3146E			UNITS
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Low Frequency Noise Figure	NF	f = 1kHz, V_{CE} = 5V, I_C = 100μA, Source resistance = 1 kΩ	14	–	3.25	–	–	3.25	–	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Foward-Current Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	16	–	100	–	–	100	–	–
Short-Circuit Input Impedance	h_{ie}		16	–	2.7	–	–	3.5	–	kΩ
Open-Circuit Output Impedance	h_{oe}		16	–	15.6	–	–	15.6	–	μmho
Open-Circuit Reverse Voltage Transfer Ratio	h_{re}		16	–	$1.8x10^{-4}$	–	–	$1.8x10^{-4}$	–	–
Admittance Characteristics:										
Foward Transfer Admittance	Y_{fe}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	17	–	31-j1.5	–	–	31-j1.5	–	mmho
Input Admittance	Y_{ie}		18	–	0.35+j0.04	–	–	0.3+j0.04	–	mmho
Output Admittance	Y_{oe}		19	–	0.001+j0.03	–	–	0.001+j0.03	–	mmho
Reverse Transfer Admittance	Y_{re}		20		See curve			See curve		mmho
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 3mA	21	300	500	–	300	500	–	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 5V, I_E = 0	22	–	0.70	–	–	0.70	–	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 5V, I_C = 0	22	–	0.37	–	–	0.37	–	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 5V, I_C = 0	22	–	2.2	–	–	2.2	–	pF

STATIC ELECTRICAL CHARACTERISTICS – CA3183 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C	Typ. Char Curve Fig. No.	LIMITS CA3183AE			CA3183E			UNITS
				Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each Transistor:										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=100μA, I_E=0	–	50	–	–	40	–	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	–	40	–	–	30	–	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI}=100μA, I_B=0, I_E = 0	–	50	–	–	40	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	–	5	–	–	5	–	–	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	23	–	–	10	–	–	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	24	–	–	1	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}= 3 V, I_C = 10mA	25,26	40	–	–	40	–	–	–
		V_{CE} = 5V, I_C = 50mA	–	40	–	–	40	–	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	27	0.65	0.75	0.85	0.65	0.75	0.85	V
Collector-to-Emitter Saturation Voltage	*V_{CEsat}	I_C = 50mA, I_B = 5mA	28	–	1.7	3.0	–	1.7	3.0	V
For Transistors Q1 and Q2 (As a Differential Amplifier):										
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	29	–	0.47	5	–	0.47	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		30	–	0.78	2.5	–	0.78	2.5	μA

* A maximum dissipation of 5 transistors x 150mW = 750mW is possible for a particular application.

TYPICAL STATIC CHARACTERISTICS CURVES – CA3118 and CA3146 SERIES

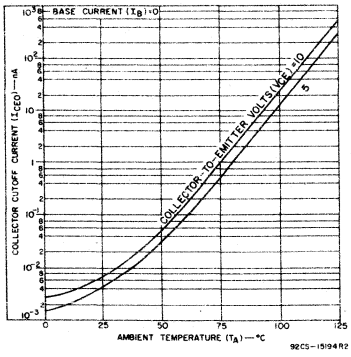


Fig. 2 – I_{CEO} vs. T_A for any transistor.

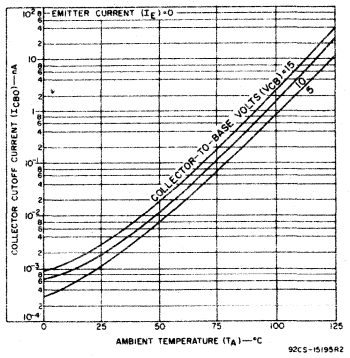


Fig. 3 – I_{CBO} vs. T_A for any transistor.

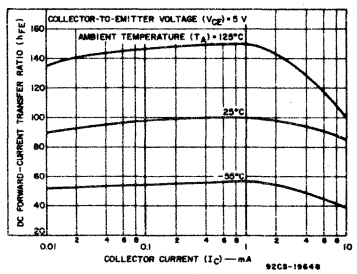


Fig. 4 – h_{FE} vs. I_C for any transistor.

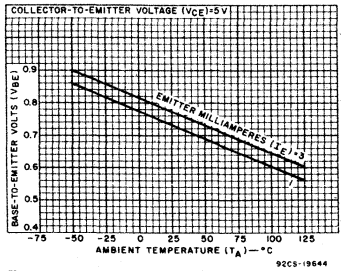


Fig. 5 – V_{BE} vs. T_A for any transistor.

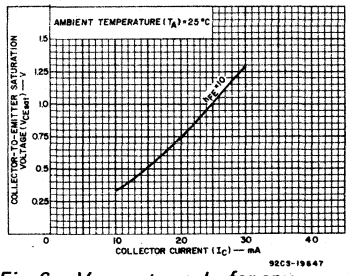


Fig. 6 – $V_{CE\ sat}$ vs. I_C for any transistor.

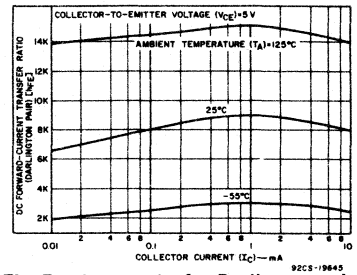


Fig. 7 – h_{FE} vs. I_C for Darlington pair (Q3 and Q4) for types CA3118AT and CA3118T.

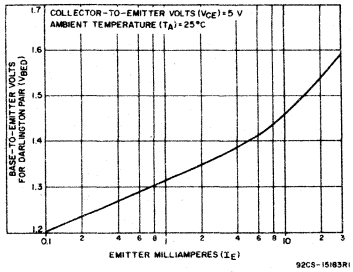


Fig. 8 – V_{BE} vs. I_E for Darlington pair (Q3 and Q4).

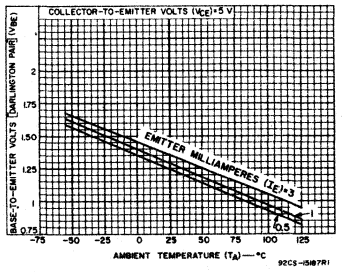


Fig. 9 – V_{BE} vs. T_A for Darlington pair (Q3 and Q4).

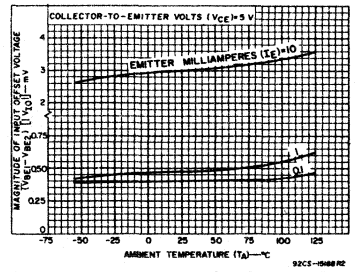


Fig. 10 – V_{IO} vs. T_A for Q1 and Q2.

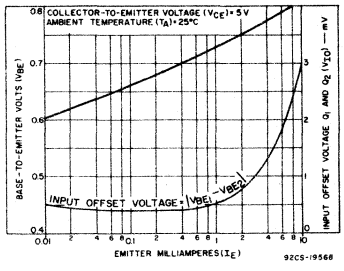


Fig. 11 – V_{BE} and V_{IO} vs. I_E for Q1 and Q2.

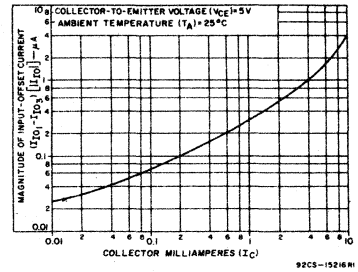


Fig. 12 – I_{IO} vs. I_C (Q1 and Q2) for types CA3146AE and CA3146E.

CA3118, CA3146, CA3183 Types

TYPICAL DYNAMIC CHARACTERISTICS CURVES (FOR ANY TRANSISTOR) – CA3118, CA3146 SERIES

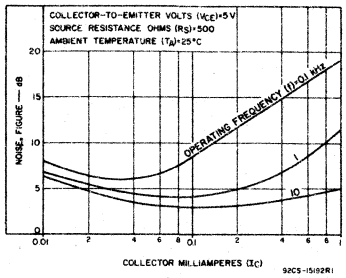


Fig. 13 – NF vs. I_C @ R_S = 500Ω.

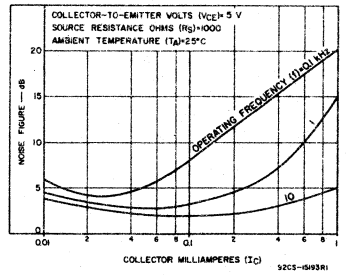


Fig. 14 – NF vs. I_C @ R_S = 1kΩ.

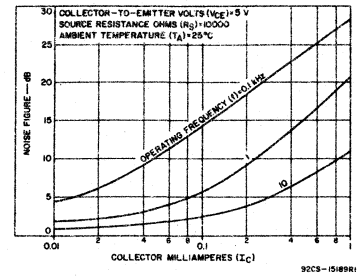


Fig. 15 – NF vs. I_C @ R_S = 10kΩ.

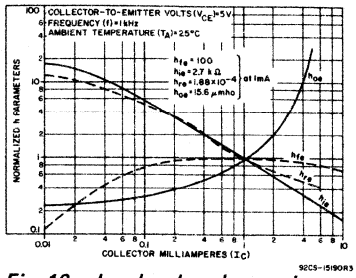


Fig. 16 – h_{fe}, h_{ie}, h_{oe}, h_{re} vs. I_C.

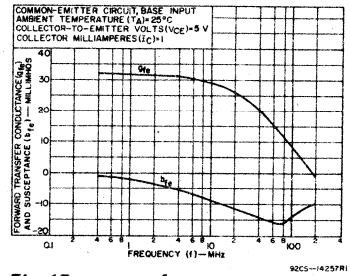


Fig. 17 – y_{fe} vs. f.

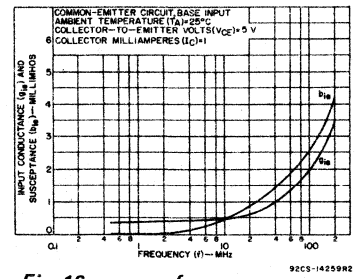


Fig. 18 – y_{ie} vs. f.

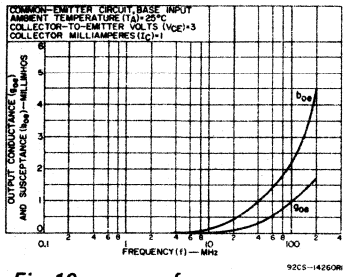


Fig. 19 – y_{oe} vs. f.

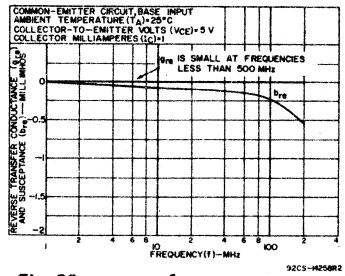


Fig. 20 – y_{re} vs. f.

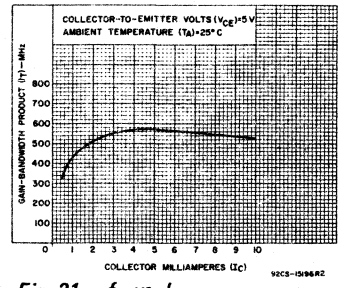


Fig. 21 – f_T vs. I_C.

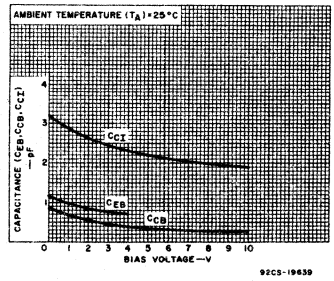


Fig. 22 – C_{EB}, C_{CB}, C_{CI} vs. bias voltage

TYPICAL STATIC CHARACTERISTICS CURVES – CA3183 SERIES

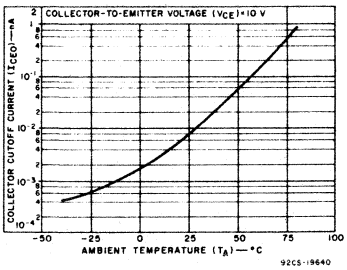


Fig. 23 – I_{CEO} vs. T_A for any transistor.

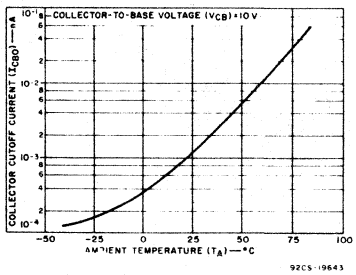


Fig. 24 – I_{CBO} vs. T_A for any transistor.

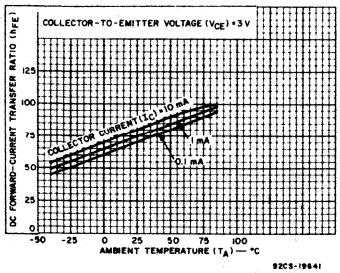


Fig. 25 – h_{FE} vs. T_A for any transistor.

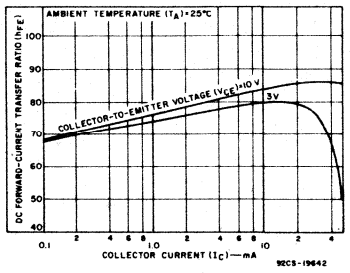


Fig. 26 – h_{FE} vs. I_C for any transistor.

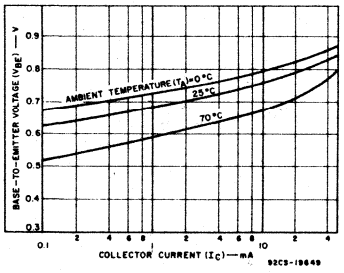


Fig. 27 – V_{BE} vs. I_C for any transistor.

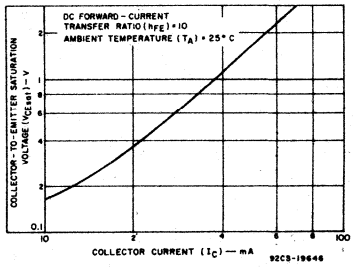


Fig. 28 – $V_{CE\ sat}$ vs. I_C for any transistor.

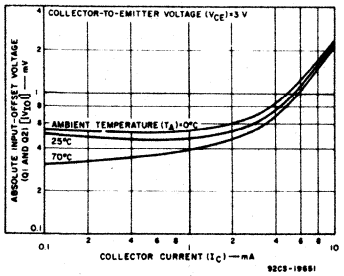


Fig. 29 – $|V_{IO}|$ vs. I_C for differential amplifier (Q1 and Q2).

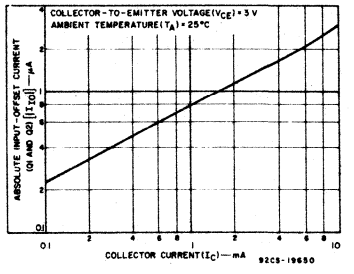
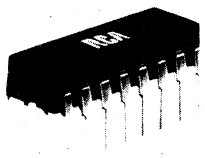


Fig. 30 – $|I_{IO}|$ vs. I_C for differential amplifier (Q1 and Q2).

CA3127E



16-Lead Dual-In-Line Plastic Package H-1622

High-Frequency N-P-N Transistor Array

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- *Gain-bandwidth product (f_T) > 1 GHz*
- *Power gain = 30 dB (typ.) at 100 MHz*
- *Noise figure = 3.5 dB (typ.) at 100 MHz*
- *Five independent transistors on a common substrate*

Applications:

- *VHF amplifiers*
- *Multifunction combinations - RF/mixer/oscillator*
- *Sense amplifiers*
- *Synchronous detectors*
- *VHF mixers*
- *IF converter*
- *IF amplifiers*
- *Synthesizers*
- *Cascade amplifiers*

RCA-CA3127E* consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1 GHz, making the CA3127E useful from dc to 500 MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127E provides close electrical and thermal matching of the five transistors.

The CA3127E is supplied in a 16-lead dual-in-line plastic package and operates over the full military temperature range of −55 to +125° C.

*Formerly RCA Dev. No. TA6206.

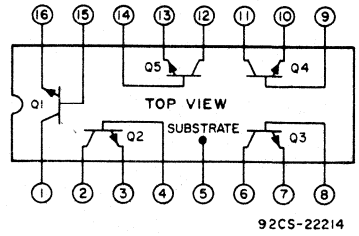


Fig. 1 — Schematic diagram of CA3127E.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

POWER DISSIPATION, P_D:

Any one transistor ..... 85 mW

Total Package:

For T_A up to 75° C ..... 425 mW

For T_A > 75° C Derate Linearly at ..... 6.67 mW/° C

AMBIENT TEMPERATURE RANGE:

Operating ..... −55 to +125° C

Storage ..... −65 to +125° C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265° C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO} ..... 15 V

Collector-to-Base Voltage, V_{CBO} ..... 20 V

Collector-to-Substrate Voltage, V_{CIO}* ..... 20 V

Collector Current, I_C ..... 20 mA

*The collector of each transistor of the CA3127E is isolated from the substrate by an integral diode. The substrate (terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	TEST CONDITIONS		LIMITS			UNITS
			Min.	Typ.	Max.	
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$I_C = 10\,\mu A$, $I_E = 0$		20	32	–	V
Collector-to-Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$		15	24	–	V
Collector-to-Substrate Breakdown Voltage	$I_{C1} = 10\,\mu A$, $I_B = 0$, $I_E = 0$		20	60	–	V
Emitter-to-Base Breakdown Voltage*	$I_E = 10\,\mu A$, $I_C = 0$		4	5.7	–	V
Collector-Cutoff-Current	$V_{CE} = 10$ V, $I_B = 0$		–	–	0.5	μA
Collector-Cutoff-Current	$V_{CB} = 10$ V, $I_E = 0$		–	–	40	nA
DC Forward-Current Transfer Ratio	$V_{CE} = 6$ V	$I_C = 5$ mA	35	88	–	
		$I_C = 1$ mA	40	90	–	
		$I_C = 0.1$ mA	35	85	–	
Base-to-Emitter Voltage	$V_{CE} = 6$ V	$I_C = 5$ mA	0.71	0.81	0.91	V
		$I_C = 1$ mA	0.66	0.76	0.86	
		$I_C = 0.1$ mA	0.60	0.70	0.80	
Collector-to-Emitter Saturation Voltage	$I_C = 10$ mA, $I_B = 1$ mA		–	0.26	0.50	V
Magnitude of Difference in V_{BE}	Q_1 & Q_2 Matched		–	0.5	5	mV
Magnitude of Difference in I_B	$V_{CE} = 6$ V, $I_C = 1$ mA		–	0.2	3	μA

*When used as a zener for reference voltage, the device must not be subjected to more than 0.1 millijoule of energy from any possible capacitance or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10 mA.

DYNAMIC CHARACTERISTICS at $T_A = 25^\circ C$

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
I/F Noise Figure	f = 100 kHz, $R_S = 500\,\Omega$, $I_C = 1$ mA	–	1.8	–	dB
Gain-Bandwidth Product	$V_{CE} = 6$ V, $I_C = 5$ mA	–	1.15	–	GHz
Collector-to-Base Capacitance	$V_{CB} = 6$ V, f = 1 MHz	–	See	–	pF
Collector-to-Substrate Capacitance	$V_{CI} = 6$ V, f = 1 MHz	–	Fig.	–	pF
Emitter-to-Base Capacitance	$V_{BE} = 4$ V, f = 1 MHz	–	5	–	pF
Voltage Gain	$V_{CE} = 6$ V, f = 10 MHz, $R_L = 1\,k\Omega$, $I_C = 1$ mA	–	28	–	dB
Power Gain	Cascode Configuration, f = 100 MHz, $V^+ = 12$ V	27	30	–	dB
Noise Figure	$I_C = 1$ mA	–	3.5	–	dB
Input Resistance	Common-Emitter	–	400	–	Ω
Output Resistance	Configuration	–	4.6	–	$k\Omega$
Input Capacitance	$V_{CE} = 6$ V	–	3.7	–	pF
Output Capacitance	$I_C = 1$ mA	–	2	–	pF
Magnitude of Forward Transadmittance	f = 200 MHz	–	24	–	mmho

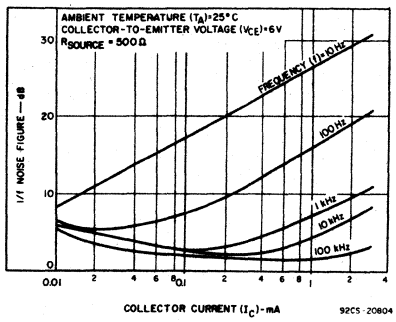


Fig. 2 – 1/f noise figure as a function of collector current at R_{SOURCE} = 500 Ω.

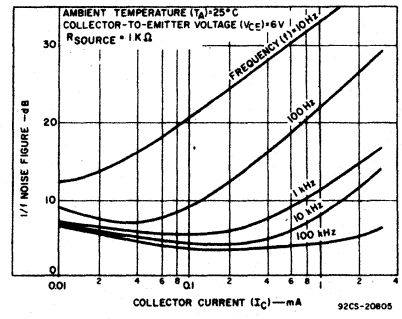


Fig. 3 – 1/f noise figure as a function of collector current at R_{SOURCE} = 1 kΩ.

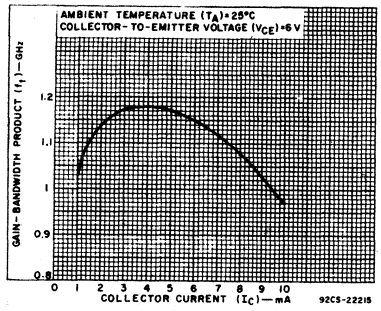


Fig. 4 – Gain-bandwidth product as a function of collector current.

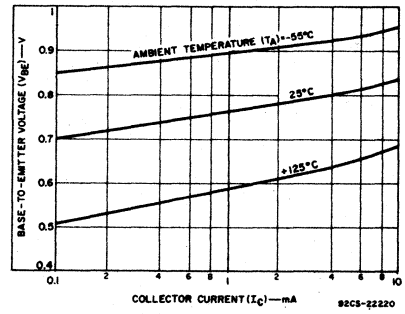


Fig. 5 – Base-to-emitter voltage as a function of collector current.

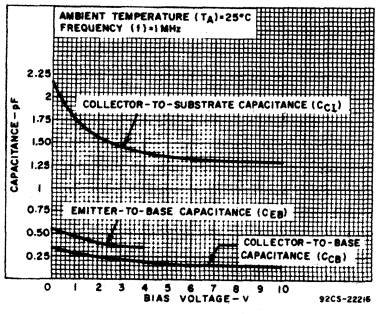


Fig. 6(a) – Capacitance as a function of bias voltage for Q_2.

Transistor	Capacitance (pF)							
	C_{CB}		C_{CE}		C_{EB}		C_{CI}	
	Pkg.	Total	Pkg.	Total	Pkg.	Total	Pkg.	Total
Bias Voltage	–	6 V	–	6 V	–	4 V	–	6 V
Q1	0.025	0.190	0.090	0.125	0.365	0.610	0.475	1.65
Q2	0.015	0.170	0.225	0.265	0.130	0.360	0.065	1.35
Q3	0.040	0.200	0.215	0.240	0.360	0.625	0.210	1.40
Q4	0.040	0.190	0.225	0.270	0.365	0.610	0.085	1.25
Q5	0.010	0.165	0.095	0.115	0.140	0.365	0.090	1.35

Fig. 6(b) – Typical capacitance values at f = 1 MHz. Three terminal measurement. Guard all terminals except those under test.

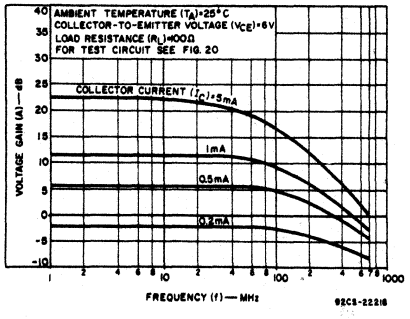


Fig. 7 – Voltage gain as a function of frequency at R_L = 100 Ω.

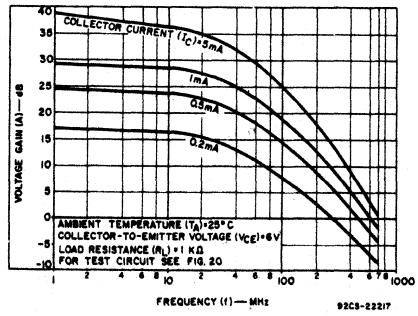


Fig. 8 – Voltage gain as a function of frequency at R_L = 1 kΩ.

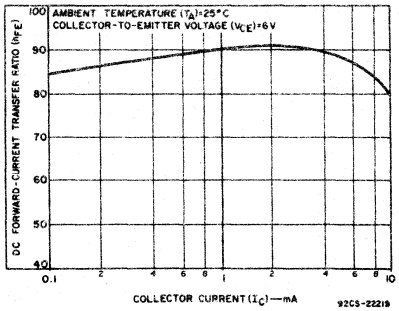


Fig. 9 – DC forward-current transfer ratio as a function of collector current.

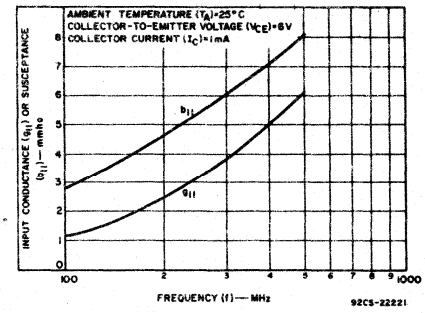


Fig. 10 – Input admittance (Y_{11}) as a function of frequency.

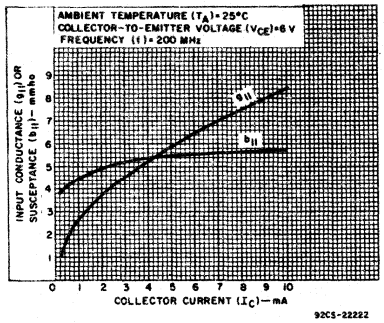


Fig. 11 – Input admittance (Y_{11}) as a function of collector current.

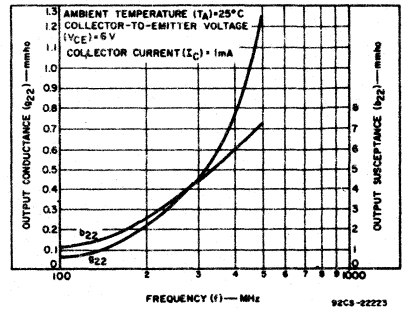


Fig. 12 – Output admittance (Y_{22}) as a function of frequency.

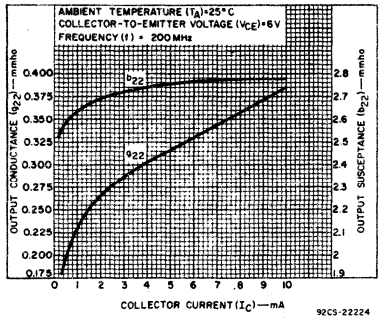


Fig. 13 – Output admittance (Y_{22}) as a function of collector current.

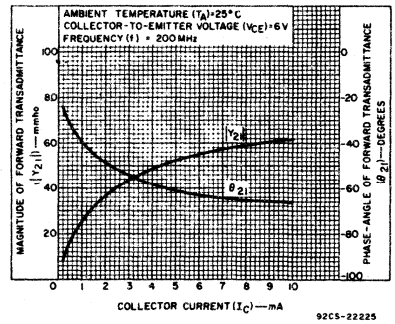


Fig. 14 – Forward transadmittance (Y_{21}) as a function of collector current.

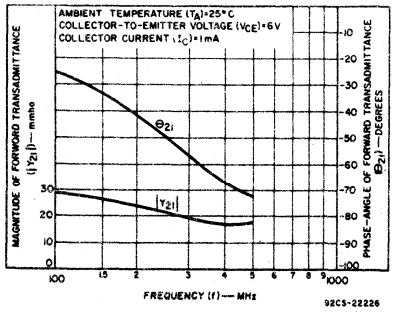


Fig. 15 – Forward transadmittance (Y_{21}) as a function of frequency.

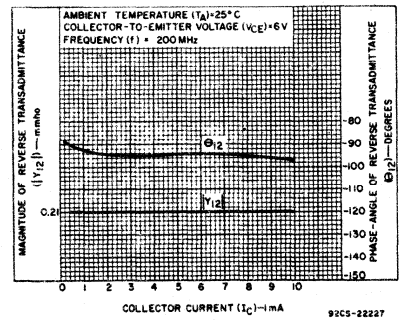


Fig. 16 – Reverse transadmittance (Y_{12}) as a function of collector current.

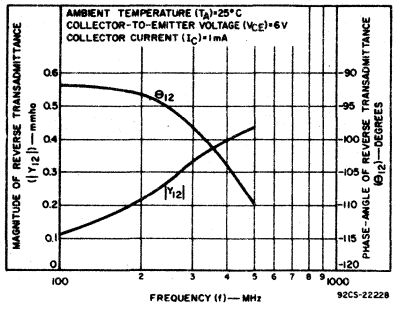


Fig. 17 – Reverse transadmittance (Y_{12}) as a function of frequency.

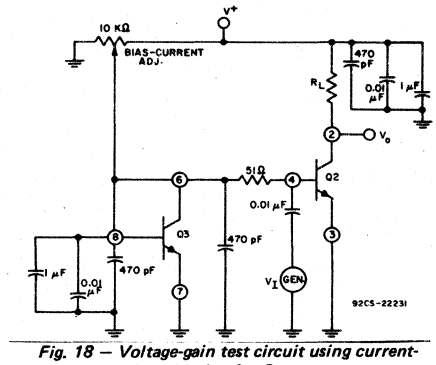
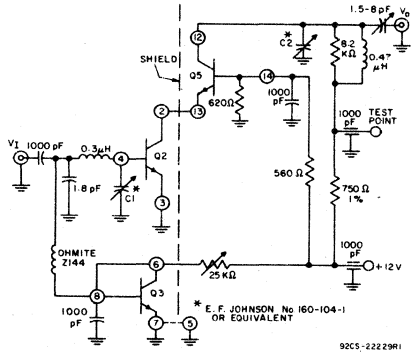


Fig. 18 – Voltage-gain test circuit using current-mirror biasing for Q_2.



This circuit was chosen because it conveniently represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q3 in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.

Fig. 19 – 100-MHz power-gain and noise-figure test circuit.

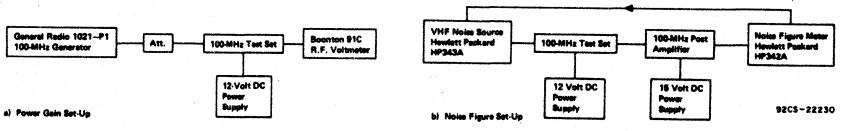
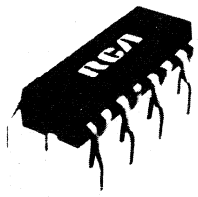


Fig. 20 – Block diagrams of power-gain and noise-figure test set-ups.

CA3128Q

TV Chroma Processor for PAL Systems



16-lead Quad-in-line palstic package

H-1706

Features:

- *Phase-locked subcarrier regeneration utilizes sample-and-hold techniques in the automatic frequency phase control [AFPC] servo loop*
- *Automatic chrominance control [ACC]/killer detector employs sample-and-hold techniques*
- *Supplementary ACC with an overload detector to prevent oversaturation of the picture tube*
- *Sinusoidal subcarrier output*
- *Keyed chroma output*
- *Emitter-follower buffered outputs for low output impedance*
- *Linear dc saturation control*
- *PAL indentification output*
- *Only the initial crystal filter tuning is required . . . no killer and ACC adjustments required at any time*
- *Few external components required*
- *Compensation for temperature and supply variations*
- *All terminals protected against short circuits*

The RCA-CA3128Q is a monolithic silicon integrated circuit designed primarily for PAL chroma processing applications in color TV receivers. For a circuit description of the CA3128Q and an explanation of this device in PAL systems, refer to "A New Chroma Processing IC Using Sample-and-Hold Techniques" by L.A. Harwood (ST6144).

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25°C$*

DC SUPPLY VOLTAGE (Between Terms. 12 and 15) ..... 13.2 V

DC VOLTAGE (Term. 9):

Positive Value ..... +3 V

Negative Value ..... −5 V

DEVICE DISSIPATION:

Up to $T_A = 55°C$ ..... 750 mW

Above $T_A = 55°C$ ..... derate linearly at 7.9 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... −40 to +85 °C

Storage ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At a distance not less than 1/32" (0.79 mm) from case for 10 seconds max. ..... +265°C

TYPICAL STATIC CHARACTERISTICS at T_A = 25°C:

DC Supply Current (I_{12}) with V_{12} = 11.2 V dc ..... 25 mA

TYPICAL DYNAMIC CHARACTERISTICS at T_A = 25°C with a Burst-to-Chroma Ratio of 46.5%:

100% Chroma Output Voltage at $V_{II(p-p)} = 0.5$ V ..... 3.5 V_{p-p}

Oscillator-Level Output Voltage ..... 1 V_{p-p}

Killer Threshold Input Voltage ..... 0.018 V_{p-p}

Pull-in Frequency ..... 500 Hz

PAL Identification Output Voltage ..... 1 V_{p-p}

CA3128Q

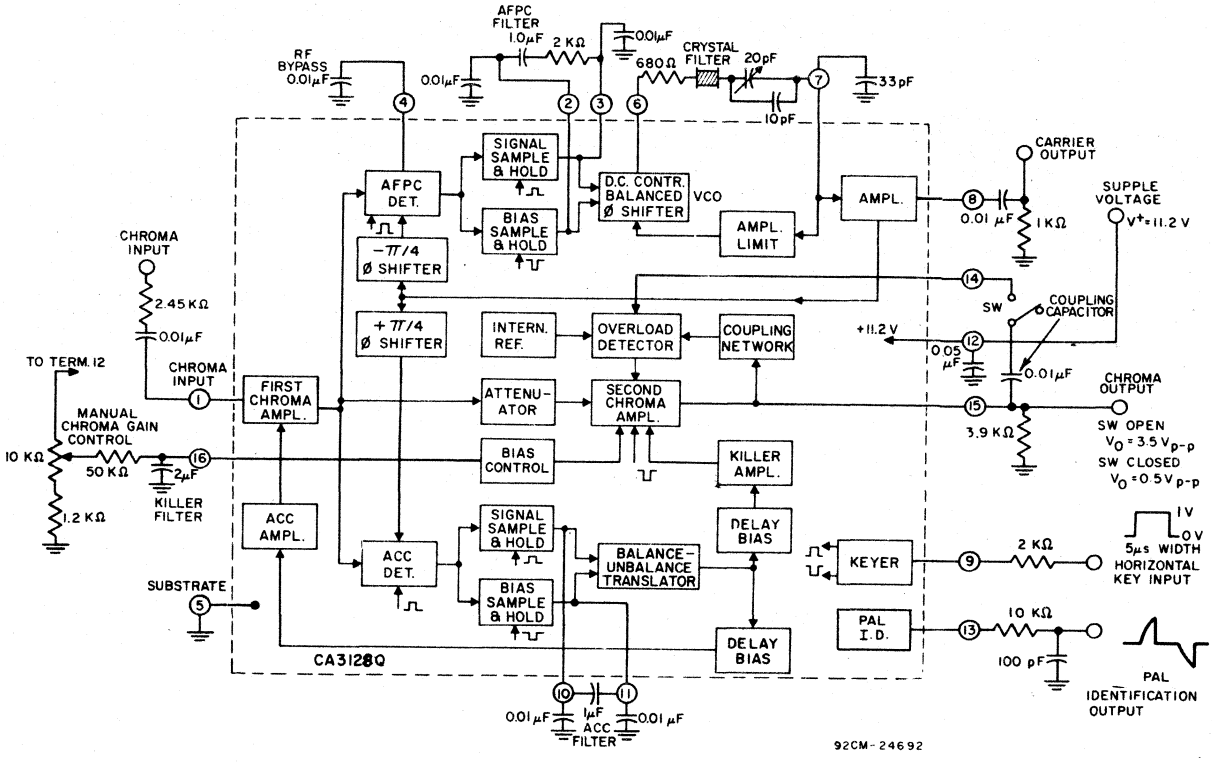
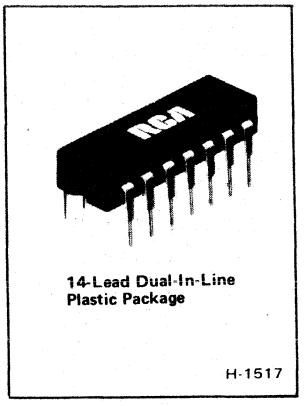


Fig. 1 — Block diagram of CA3128Q TV Chroma Processor.

CA3138E, CA3138AE



14-Lead Dual-In-Line Plastic Package

H-1517

High-Current, High-Beta N-P-N Transistor Arrays

For Industrial, Commercial, and Military Applications

Four Isolated Discrete Sealed-Junction High-Current N-P-N Transistors

Features:

- **High Current –1 A**
- **High Beta – 95 min. at I_C = 500 mA, V_{CE} = 5 V**
- **Low V_{CE}(SAT) –0.4 V max. at I_C = 500 mA, I_B = 12.5 mA**
- **Silicon Nitride Passivated**
- **Platinum Silicide Ohmic Contacts**

The RCA-CA3138 and CA3138A are high-current n-p-n transistor arrays containing four isolated (discrete) sealed-junction high-current n-p-n transistors. They are intended for high-current, high-speed switching and driver applications.

The CA3138A has all the features and characteristics of the CA3138 but is intended for applications requiring premium grade specifications — higher rating for V_{CBO} of 25 volts and limits established for I_{CEO}, I_{EBO}, and h_{FE} at 10 mA.

The CA3138 and CA3138A are supplied in a 14-lead dual-in-line plastic package and operate over the full military temperature range of –55°C to +125°C.

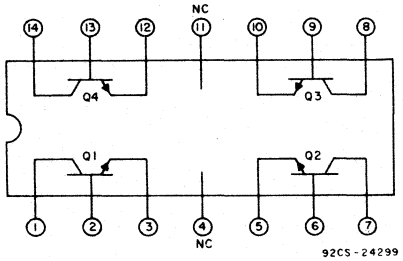


Fig. 1 – Terminal diagram (top view).

Applications:

- **High-Current LED Driver**
- **Relay and Solenoid Driver**
- **Lamp Driver**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE ..... With Base Open (V_{CEO})	15	V
COLLECTOR-TO-BASE VOLTAGE With Emitter Open (V_{CBO})		
CA3138	20	V
CA3138A	25	V
EMITTER-TO-BASE VOLTAGE ..... With Collector Open (V_{EBO})	5	V
COLLECTOR CURRENT (I_C)	1	A
POWER DISSIPATION (P_D):		
At T_A up to 25°C:		
For Each Transistor	1	W
Total Package	2	W
At T_A above 25°C derate linearly	20	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	–55 to +125	°C
Storage	–65 to +150	°C
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

CA3138E, CA3138AE

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Characteristic		Test Conditions	LIMITS						Units
			CA3138			CA3138A			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector-to-Emitter Sustaining Voltage, $V_{CEO}(sus)$*		I_C = 1 mA, I_B = 0	15	20	–	15	20	–	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$		I_C = 10 μA	20	55	–	25	60	–	V
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$		I_C = 10 μA, I_E = 0	20	55	–	25	60	–	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$		I_E = 10 μA, I_C = 0	5	7.2	–	5	7.2	–	V
Base-to-Emitter Saturation Voltage, $V_{BE}(sat)$*		I_C = 500 mA, I_B = 12.5 mA	0.7	0.81	1.1	0.7	0.81	1.1	V
Collector-to-Emitter Saturation Voltage, $V_{CE}(sat)$*		I_C=500 mA, I_B = 12.5 mA	–	0.26	0.4	–	0.26	0.4	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 15 V	–	0.03	1	–	0.02	0.1	μA
	I_{CEO}	V_{CE} = 10 V	–	0.5	–	–	0.3	1.0	
	I_{EBO}	V_{EB} = 4 V	–	0.01	–	–	0.01	0.1	
Static Forward-Current Transfer Ratio (Beta), h_{FE}*		I_C=10 mA, V_{CE} = 5 V	–	–	–	35	140	–	
		I_C = 100 mA, V_{CE} = 5 V	80	160	450	80	160	450	
		I_C = 500 mA, V_{CE} = 5 V	95	170	500	95	170	500	
		I_C = 1 A, V_{CE} = 5 V	40	170	–	40	170	–	
Small-Signal Forward Current Transfer Ratio, h_{fe}		I_C = 50 mA, V_{CE} = 10 V, f = 100 MHz	2	–	–	2	–	–	
Collector-to-Base Capacitance, C_{CB}		V_{CB} = 10 V, I_E = 0	–	18	–	–	18	–	pF
Emitter-to-Base Capacitance, C_{EB}		V_{EB} = 0.5 V, I_C = 0	–	77	–	–	77	–	pF
Rise Time (See Test Ckt. Fig. 6), t_r		I_C = 570 mA	–	6	–	–	6	–	ns
Fall Time (See Test Ckt. Fig. 6), t_f		I_{B1} = 30 mA	–	100	–	–	100	–	ns
Delay Time (See Test Ckt. Fig. 6), t_d		I_{B2} = 0	–	7.5	–	–	7.5	–	ns
Storage Time (See Test Ckt. Fig. 6), t_s			–	850	–	–	850	–	ns

*Pulse Conditions: width = 300 μs; duty cycle = 1%.

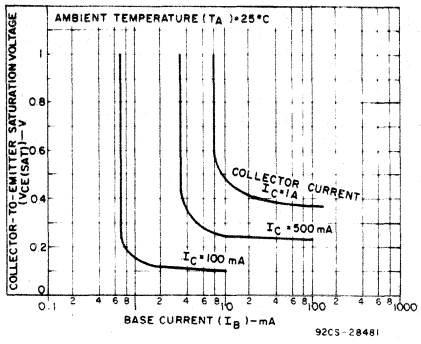


Fig. 2 – $V_{CE(sat)}$ vs I_B

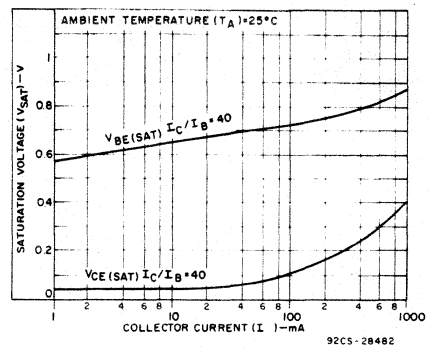


Fig. 3 – V_{sat} vs I_C

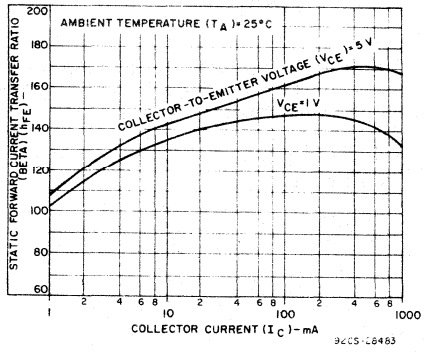


Fig. 4 – h_{FE} vs I_C

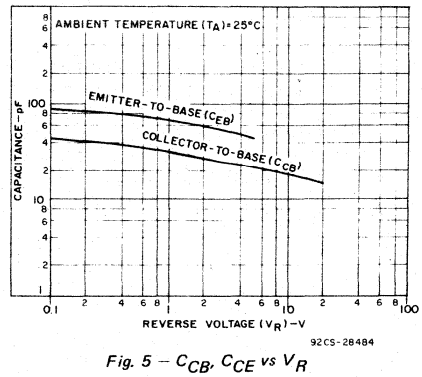


Fig. 5 – C_{CB}, C_{CE} vs V_R

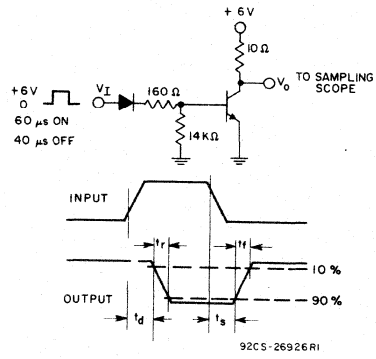
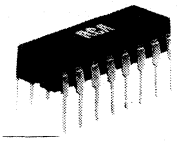


Fig. 6 – Switching time test circuit and waveforms.

CA3227E, CA3246E

CA3227E



H-1622

16-Lead Dual-In-Line Plastic Package

CA3246E

H-1517

14-Lead Dual-In-Line Plastic Package

High-Frequency N-P-N Transistor Arrays

For Low-Power Applications at Frequencies up to 1.5 GHz

Features:

- *Gain-bandwidth product (f_T) > 3 GHz*
- *Five transistors on a common substrate*

Applications:

- *VHF amplifiers*
- *VHF mixers*
- *Multifunction combinations - RF/mixer/oscillator*
- *IF converter*
- *IF amplifiers*
- *Sense amplifiers*
- *Synchronous detectors*
- *Synthesizers*
- *Cascade amplifiers*

The RCA-CA3227E and CA3246E* consist of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the transistors exhibits a value of f_T in excess of 3 GHz, making them useful from dc to 1.5 GHz. The monolithic construction of these devices provides close electrical and thermal matching of the five transistors.

The CA3227E is supplied in a 16-lead dual-in-line plastic package and the CA3246E is supplied in a 14-lead dual-in-line plastic package.

*Formerly RCA Developmental Nos. TA10854 and TA10855, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25°C:*

POWER DISSIPATION, P_D:

Any one transistor	85 mW
Total Package:	
For T_A up to 75°C	425 mW
For T_A > 75°C Derate Linearly at	6.67 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating	−55 to +125°C
Storage	−65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

The following ratings apply for each transistor in the device.

Collector-to-Emitter Voltage, V_{CEO}	8 V
Collector-to-Base Voltage, V_{CBO}	12 V
Collector-to-Substrate Voltage, V_{CIO}§	20 V
Collector Current, I_C	20 mA

§The collector of each transistor of these devices is isolated from the substrate by an integral diode. The substrate (terminal 5/CA3227E and terminal 13/CA3246E) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

STATIC ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10 μA, I_E=0	12	20	—	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1 mA, I_B=0	8	10	—	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{C1}=10 μA, I_B=0, I_E=0	20	—	—	V
Emitter-Cutoff-Current*	I_{EBO}	V_{EB}=4.5 V, I_C=0	—	—	10	μA
Collector-Cutoff-Current	I_{CEO}	V_{CE}=5 V, I_B=0	—	—	1	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB}=8 V, I_E=0	—	—	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=6 V, I_C=10 mA	—	110	—	
		V_{CE}=6 V, I_C=1 mA	40	150	—	
		V_{CE}=6 V, I_C=0.1 mA	—	150	—	
Base-to-Emitter Voltage	V_{BE}	V_{CE}=6 V, I_C=1 mA	0.62	0.71	0.82	V
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C=10 mA, I_B=1 mA	—	0.13	0.50	V
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	I_C=10 mA, I_B=1 mA	0.74	—	0.94	V

*On small-geometry, high-frequency transistors, it is very good practice never to take the Emitter Base Junction into reverse breakdown. To do so may permanently degrade the h_{FE}. Hence, the use of I_{EBO} rather than $V_{(BR)EBO}$. These devices are also susceptible to damage by electrostatic discharge and transients in the circuits in which they are used. Moreover, CMOS handling procedures should be employed.

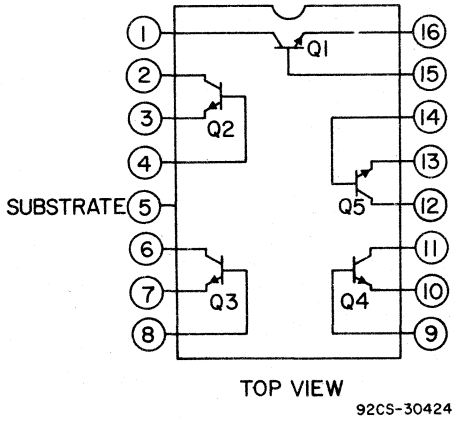


Fig. 1 - Schematic diagram of CA3227E.

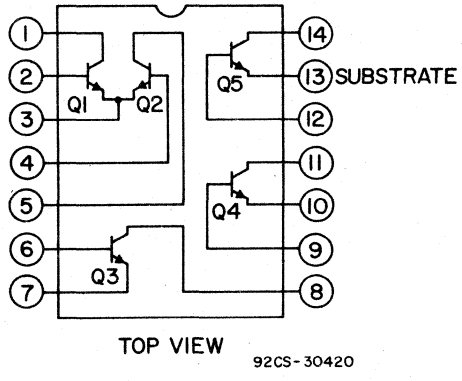


Fig. 2 - Schematic diagram of CA3246E.

CA3227E, CA3246E

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, 200 MHz, Common Emitter
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each Transistor			
Input Admittance, Y_{11} b_{11}	I_C=1 mA, V_{CE}=5 V	4	mmho
g_{11}		0.75	
Output Admittance, Y_{22} b_{22}		2.7	mmho
g_{22}		0.13	
Forward Transfer Admittance, Y_{21} Y_{21}		29.3	mmho
θ_{21}		−33	degrees
Reverse Transfer Admittance, Y_{12} Y_{12}		0.38	mmho
θ_{12}		−97	degrees
Input Admittance, Y_{11} b_{11}	I_C=10 mA, V_{CE}=5 V	4.8	mmho
g_{11}		2.85	
Output Admittance, Y_{22} b_{22}		2.75	
g_{22}		0.9	
Forward Transfer Admittance, Y_{21} Y_{21}		95	mmho
θ_{21}		−62	degrees
Reverse Transfer Admittance, Y_{12} Y_{12}		0.39	mmho
θ_{12}		−97	degrees
Small-Signal Forward Current Transfer Ratio h_{21}	I_C=1 mA, V_{CE}=5 V	7.1	
	I_C=10 mA, V_{CE}=5 V	17	
Typical Capacities @ 1 MHz, Three-Terminal Measurement			
Collector-to-Base Capacitance, C_{CB}	V_{CB}=6 V	0.3	pF
Collector-to-Substrate Capacitance, C_{CI}	V_{CI}=6 V	1.6	pF
Collector-to-Emitter Capacitance, C_{CE}	V_{CE}=6 V	0.4	pF
Emitter-to-Base Capacitance, C_{EB}	V_{EB}=3 V	0.75	pF

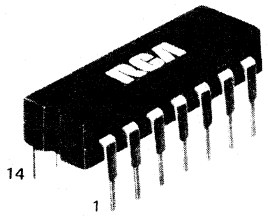
OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. **Operating**

   Operating Voltage

   During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{CC}—V_{EE} to exceed the absolute maximum rating.



14-Lead dual-in-line plastic package

H-1517

COS/MOS Transistor Array

For Linear Circuit Applications

Applications:

- High input impedance, general-purpose amplifiers
- Pre-amplifiers
- Differential amplifiers
- Op-amps and comparators
- Constant-current sources and current mirrors
- Micropower amplifiers and oscillators
- Control of lamps, LED's, relays, and thyristors
- Timers
- Choppers
- Mixers

RCA-CA3600E is an array of COmplementary-Symmetry MOS Field-Effect Transistors* on a monolithic silicon substrate. It is comprised of three n-channel and three p-channel enhancement-type MOS transistors arrayed as shown in Fig. 1, and specified and tested for linear circuit operation. These transistors are uniquely suitable for service in complementary-symmetry circuits at supply voltages in the range of 3 to 15 volts and are useful at frequencies up to 5 MHz (untuned). Each transistor in the CA3600E can conduct currents up to 10 mA. This device is supplied in the 14-lead dual-in-line plastic package.

Formerly RCA Dev. No. TA6368.

* The theory and construction of COS/MOS transistors are described in the "RCA COS/MOS Integrated Circuits Manual," RCA Solid State Division Technical Series Publication No. CMS-271.

Features:

- High input resistance . . . . . 100 GΩ (typ.)
- Low gate-terminal current . . . . 10 pA (typ.)
- Matched p-channel pair:
  Gate-voltage differential (I_D =-100 μA) ±20 mV (max.)
- No "Popcorn" (burst) noise
- Stable transfer characteristics over an operating temperature range of −55°C to +125°C when operated in complementary circuit configuration at supply voltages in the 5 to 15 volt range (see Fig. 14)
- Integrated integral gate-protection system (see Fig. 34)
- High voltage gain (see Fig. 11). . . up to 53 dB (typ.) per COS/MOS stage
- Individual MOS transistors have square-law characteristics, superior cross-modulation performance, and greater dynamic range than bipolar transistors

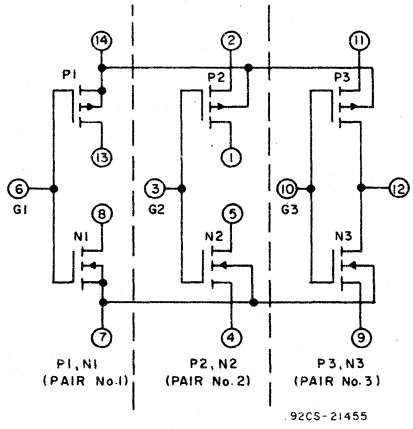


Fig.1 — Schematic diagram for CA3600E COS/MOS transistor array. (See Fig.34 for internal gate-and-channel-protection circuits)

1. Drain terminal, p-channel of pair no. 2
2. Source terminal, p-channel of pair no. 2
3. Common gate terminal of pair no. 2
4. Source terminal, n-channel of pair no. 2
5. Drain terminal, n-channel of pair no. 2
6. Common gate terminal of pair no. 1
7. Source terminal, n-channel of pair no. 1 and substrate connection for all n-channel transistors - - - V_{SS} terminal
8. Drain terminal, n-channel of pair no. 1
9. Source terminal, n-channel of pair no. 3
10. Common gate terminal of pair no. 3
11. Source terminal, p-channel of pair no. 3
12. Common drain terminal of pair no. 3
13. Drain terminal, p-channel of pair no. 1
14. Source terminal, p-channel of pair no. 1 and substrate connection for all p-channel transistors - - - V_{DD} terminal

Terminal Identification for Fig. 1.

CA3600E

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DISSIPATION:

Any one transistor at T_A up to 55°C	150 mW
Total package at T_A up to 55°C	750 mW
Above T_A = 55°C	derate linearly 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating	−55 to +125°C
Storage	−65 to +150°C

LEAD TEMPERATURE (During Soldering)

At distance not less than 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	265°C

The Following Ratings Apply for Each Transistor in the Device:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}:

n-channel	+15 V
p-channel	−15 V

DRAIN-TO-GATE VOLTAGE, V_{DG}:

n-channel	+15 V
p-channel	−15 V

SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}:

n-channel	+15 V
p-channel	−15 V

GATE-TO-SOURCE VOLTAGE, V_{GS}:

p-channel transistors (p_1, p_2, p_3)	0 V(min.),$-V_D$(max.)
n-channel transistors (n_1, n_2, n_3)	0 V(min.),$+V_D$(max.)
COS/MOS transistor-pairs (p_1-n_1, p_2-n_2, p_3-n_3)	0 V(min.),$+V_{DD}$(max.)

DRAIN CURRENT, $\|I_D\|$	10 mA
GATE CURRENT, $\|I_G\|$	100 μA

The Following Rating Applies for Each COS/MOS Transistor-Pair in the Device:

DC SUPPLY VOLTAGE ($V_{DD} - V_{SS}$)	+15 V

Rules for Maintaining Electrical Isolation Between Transistors and Monolithic Substrate

Terminal No. 14 must be maintained at the most positive potential (or equally positive potential) with respect to any other terminal in the CA3600E.

Terminal No. 7 must be maintained at the most negative potential (or equally negative potential) with respect to any other terminal in the CA3600E.

Violation of these rules will result in improper transistor operation, circuit "latching," and/or possible permanent damage to the CA3600E.

Note: Users should observe the "Considerations in Handling CA3600E Devices", discussed on page 13.

ELECTRICAL CHARACTERISTICS, *At T_A = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	TYPICAL CURVE OR CIRCUIT FIG. NO.	LIMITS			UNIT
				Min.	Typ.	Max.	
For Each p-Channel MOS Transistor							
Drain Current	I_D	V_{DS}=−10 V,V_{GS}=−3.6 V	2,3,4	−0.5	−1.1	−2.0	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	I_D=−10 μA	–	–	−1.75	–	V
Gate-to-Source Voltage Differential (p_1 vs. p_2)	$\lvert V_{GS1}-V_{GS2}\rvert$	I_D=−100 μA,V_{DS}=−10 V	5	–	±4	±20	mV
Forward Transconductance	g_{fs}	I_D=−1 mA,f=1 kHz	6	–	920	–	μmho
Low-Frequency Noise Voltage	e_N	I_D=−1 mA,f=1 kHz,R_s=0 Ω	7	–	0.03	–	μV $\sqrt{Hz}$
Low-Frequency Noise Current	i_N	I_D=−1 mA,f=1 kHz,R_s=1 MΩ	7	–	0.2	–	pA $\sqrt{Hz}$
Current-Mirror Transfer Ratio (p_1/p_2)	I_{MTR}	I_1=−100 μA,V_{DS}=−10 V	30	0.7	1.1	1.5	–
Gate-Terminal Current	I_{GT}	V_{DS}=−10 V,V_{GS}=−3.5 V	–	–	±0.015	−40	nA
Input Capacitance	C_I	–	–	–	6.3	–	pF
Output Capacitance	C_O	–	–	–	3	–	pF
Input-to-Output Capacitance	C_{I-O}	–	–	–	0.75	–	pF
For Each n-Channel MOS Transistor							
Drain Current	I_D	V_{DS}=+10 V,V_{GS}=+3.6 V	2,3,4	0.4	0.9	1.6	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	I_D=10 μA	–	–	1.5	–	V
Gate-to-Source Voltage Differential (n_1 vs n_2)	$\lvert V_{GS1}-V_{GS2}\rvert$	I_D=100 μA,V_{DS}=+10 V	5	–	±30	–	mV
Forward Transconductance	g_{fs}	I_D=1 mA,f=1 kHz	6	–	860	–	μmho
Low-Frequency Noise Voltage	e_N	I_D=1 mA,f=1 kHz,R_s=0 Ω	7	–	0.2	–	μV $\sqrt{Hz}$
Low-Frequency Noise Current	i_N	I_D=1 mA,f=1 kHz,R_s=1 MΩ	7	–	0.3	–	pA $\sqrt{Hz}$
Current-Mirror Transfer Ratio (n_1/n_2)	I_{MTR}	I_1=100 μA,V_{DS}=+10 V	29	0.7	1.3	2.0	–
Gate-Terminal Current	I_{GT}	V_{DS}=+10 V,V_{GS}=+3.7 V	–	–	±0.01	+40	nA
Input Capacitance	C_I	–	–	–	5.5	–	pF
Output Capacitance	C_O	–	–	–	2.0	–	pF
Input-to-Output Capacitance	C_{I-O}	–	–	–	0.35	–	pF
For Each COS/MOS Transistor Pair							
Drain Current	I_{DD}	V_{DD}=+10 V	9,10	1.0	2.2	4.0	mA
Drain-to-Source Cutoff Current	$I_{DD(off)}$	V_{DD}=+10 V,V_{SS}=0 V Gate Voltage(V_G)=+10 V or 0 V	8	–	0.5	100	nA
DC Output Voltage	V_O	V_{DD}=+10 V	10	4.2	5.0	5.8	V
Forward Transconductance	g_{fs}	V_{DD}=+10 V, f = 1 kHz	6	–	2300	–	μmho
Slew Rate (Open-Loop)	SR	V_{DD}=+15 V	10	–	95	–	V/μs
Amplifier Voltage Gain	A_{OL}	V_{DD}=+10 V,f=1 kHz,R_b=22 MΩ R_s=50 Ω	10,11	–	32	–	dB
Gate-Terminal Current	I_{GT}	V_{DD}=+10 V	10	–	±0.005	±20	nA
Broadband Output Noise Voltage	E_{ON}	V_{DD}=+10 V,R_b=22 MΩ,R_s=10 kΩ	10,11	–	500		μV
Input Capacitance	C_I	–	–	–	11.8		pF
Output Capacitance	C_O	–	–	–	5.0		pF
Input-to-Output Capacitance	C_{I-O}	–	–	–	1.1		pF

TYPICAL CHARACTERISTICS CURVES

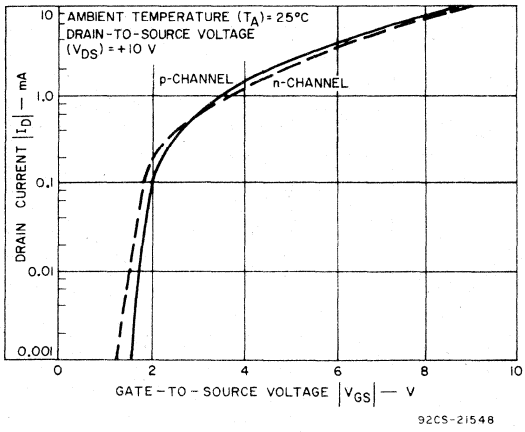


Fig. 2—Drain current vs. gate-to-source voltage.

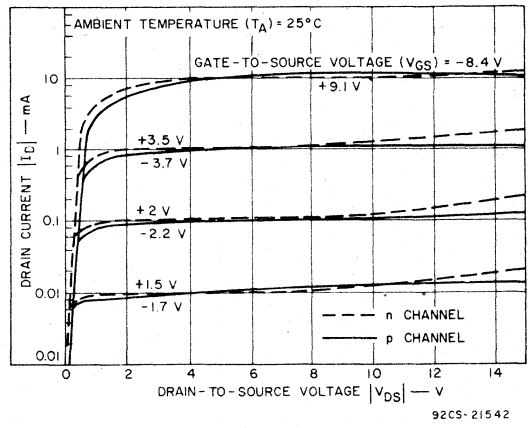


Fig. 3— Drain current vs. drain-to-source voltage.

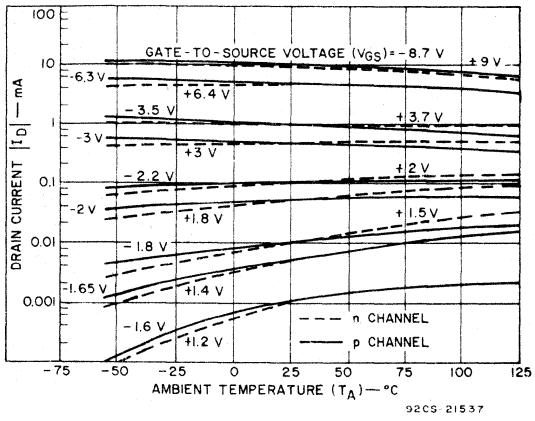


Fig. 4— Drain current vs. ambient temperature.

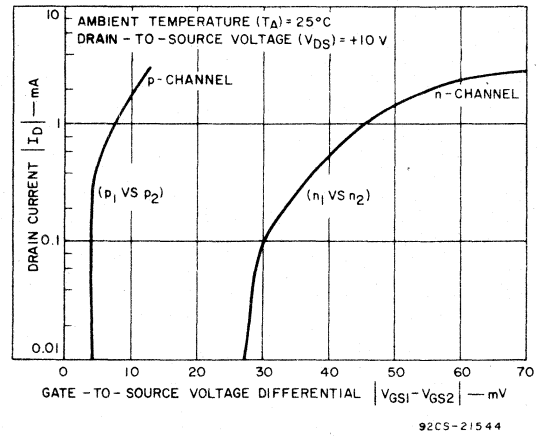


Fig. 5— Gate-to-source voltage differential vs. drain current.

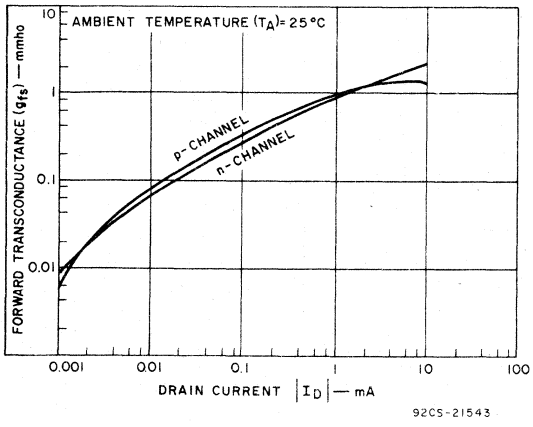


Fig. 6— Forward transconductance vs. drain current.

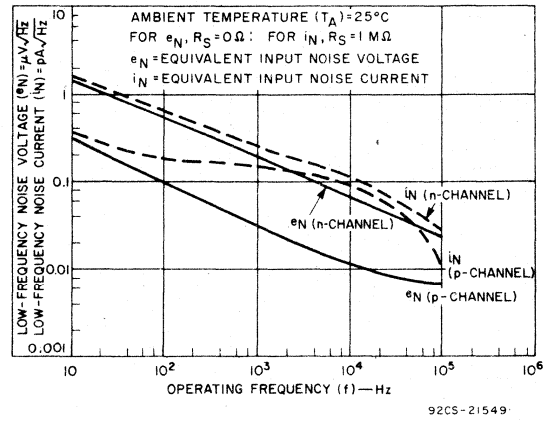


Fig. 7— Noise voltage and noise current vs. operating frequency.

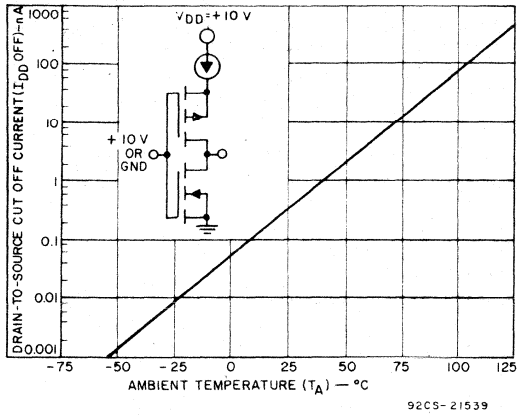


Fig. 8— Drain-to-source cutoff current vs. ambient temperature.

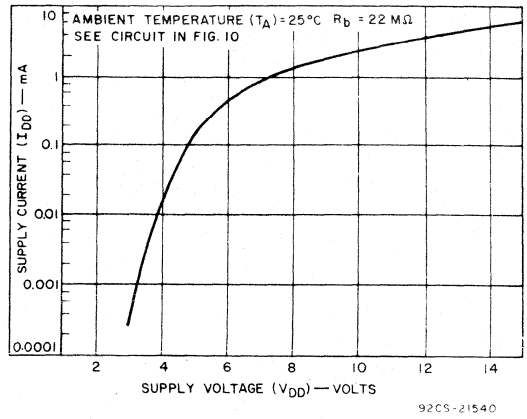


Fig.9 – Typical V_{DD} vs. I_{DD} characteristics for amplifier circuits of Fig.10 and Fig.15.

APPLICATIONS

The Basic COS/MOS Linear Amplifier

P-n-p and n-p-n bipolar transistors have been used for many years in the design of so-called "true-complementary" linear amplifier circuits[1]. Since mutually compatible p-channel and n-channel MOS/FET devices were not generally available, "true-complementary" amplifier circuits using MOS transistors were seldom used. Now, COS/MOS transistor technology[5] has made it possible to supply compatible p-channel/n-channel transistors in monolithic IC form such as the CA3600E COS/MOS transistor array shown in Fig. 1.

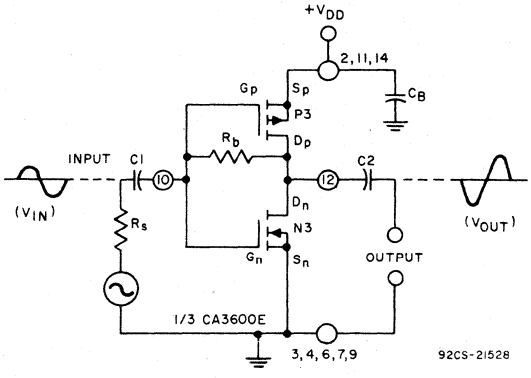


Fig. 10– COS/MOS transistor-pair biased for linear-mode operation.

A "True-Complementary" Linear Amplifier Using COS/MOS Transistors

Fig. 10 shows the schematic diagram of a single-stage "true-complementary" linear amplifier using one pair of the complementary MOS transistors in the CA3600E, connected in a common-source circuit. Resistor R_b is used to bias the complementary pair for Class A operation, as described subsequently, and R_s represents the source resistance of the signal source. This generic amplifier is suitable for operation with a single or split voltage supply in the range of 3 to 15 volts. Fig. 11 shows voltage gain as a function of operating frequency at various supply voltages for the single-stage amplifier. This amplifier is capable of producing very high output-swing voltages (V_{out}); for example, its output voltages can be swung to within several millivolts of either supply-voltage "rail". Fig. 9 shows typical supply voltage (V_{DD}) vs. supply current (I_{DD}) characteristics for the single-stage amplifier. The curves in Fig. 12 show the normalized amplifier supply current as a function of ambient temperature at various supply voltages. When the amplifier is operating at V_{DD} = 3 V, the supply current changes rapidly as a function of temperature because the MOS transistors are operating in the proximity of their individual gate-source threshold voltages.

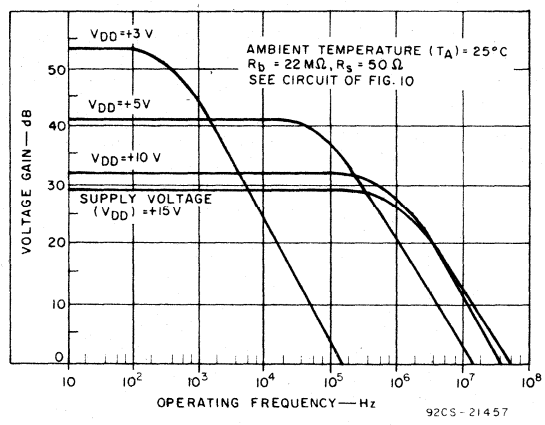


Fig. 11– Typical voltage gain vs. frequency characteristics for amplifier circuit of Fig. 10.

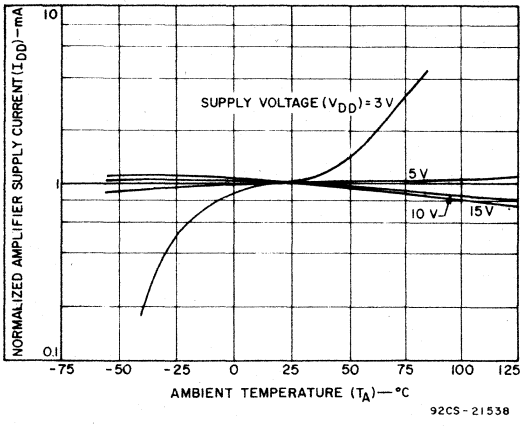


Fig. 12– Normalized amplifier supply current vs. ambient temperature characteristics for amplifier circuit of Fig. 10.

Voltage-Transfer Characteristics

Fig. 13 illustrates a voltage-transfer characteristic curve of a COS/MOS transistor pair connected in the amplifier circuit of Fig. 10, with a biasing resistor (R_b) connected between the drain and gate terminals (10,12). If the p- and n-channel transistors have identical characteristics, their channel resistances are equal, and the biasing method shown establishes a steady-state condition such that terminal 12 is at mid-potential between V_{DD} and ground. Thus, with negligibly small gate-source leakage resistances, under zero-signal conditions, the biasing resistor (R_b) establishes gate potential at the mid-point between V_{DD} and ground, i.e., $V_{in} = V_{out}$. Under these conditions the amplifier is biased for operation about the mid-point ("0") in the linear segment on the steep transition of the voltage-transfer characteristic as shown in Fig. 13. When the input signal (V_{in}) swings in the positive direction, there is a reduction in the instantaneous output voltage (V_{out}) with respect to ground. Negative-going input signals have inverse effects. Thus, phase-inversion occurs in the COS/MOS-pair amplifier. Power-supply current is constant during dynamic linear operation, i.e., Class A amplifier service. When the signal input-voltage level (V_{in}) becomes very large, the output signal (V_{out}) waveforms become distorted because the transistors are driven into the non-linear portions of their voltage-transfer characteristics. If the positive-going input-signal is sufficiently large, for example, the p-channel transistor can be driven to cutoff and the amplifier supply current (I_{DD}) is reduced to essentially zero.

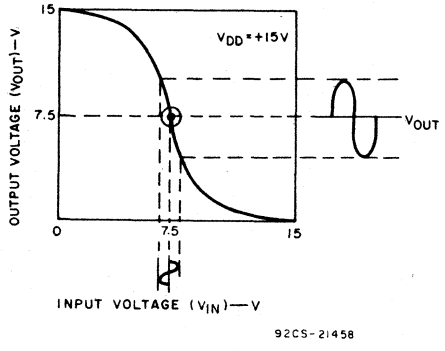


Fig. 13 – Representation of voltage-transfer characteristics for COS/MOS transistor pair.

Fig. 14 shows typical voltage-transfer characteristics of each COS/MOS pair in the CA3600E at several values of V_{DD}. The shape of these transfer characteristics is comparatively constant despite temperature changes from –55 to +125°C.

The biasing arrangement used in the circuit of Fig. 10 provides an easy method of establishing feedback for ac signals in accordance with the R_b/R_s ratio. When the feedback of ac signals is not desirable, the circuit of Fig. 15 may be used. The ac bypass capacitor (C_3) minimizes ac signal feedback.

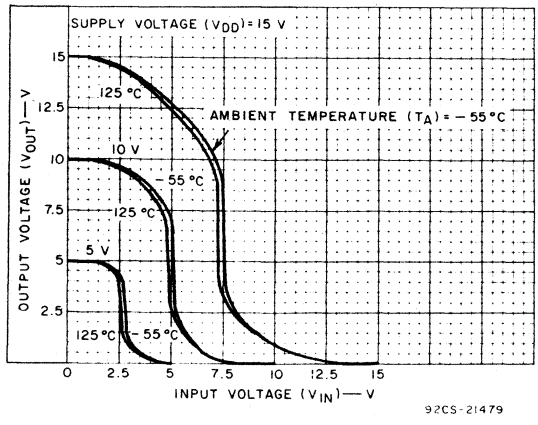


Fig. 14– Voltage transfer characteristics for COS/MOS transistor-pair amplifier in Fig. 10.

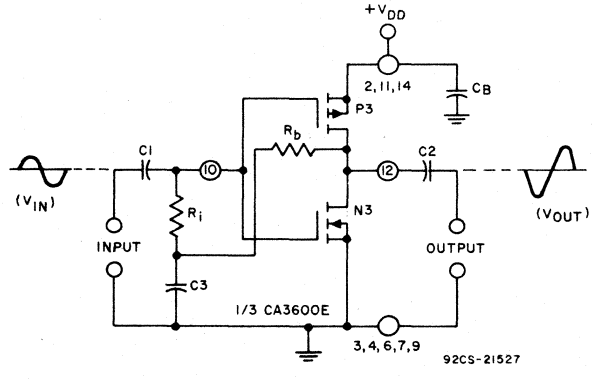


Fig. 15– Alternate method of biasing COS/MOS transistor-pair for linear-mode operation.

Cascading Amplifier Stages of COS/MOS Transistor Pairs

Ultra-high-gain amplifiers can be designed by cascading stages of COS/MOS transistor pairs as shown in Fig. 16. The biasing system used is similar to that described above in connection with Fig. 10. The supply current for the three-stage amplifier shown in Fig. 16 is typically three times the values shown in Fig. 9. Gain and frequency-response characteristics of the amplifier are shown in Fig. 17.

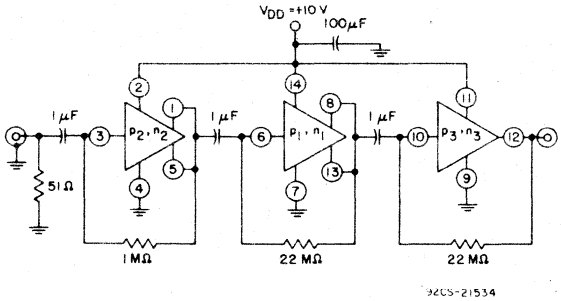


Fig. 16– High-gain amplifier uses cascaded COS/MOS transistor-pair in CA3600E.

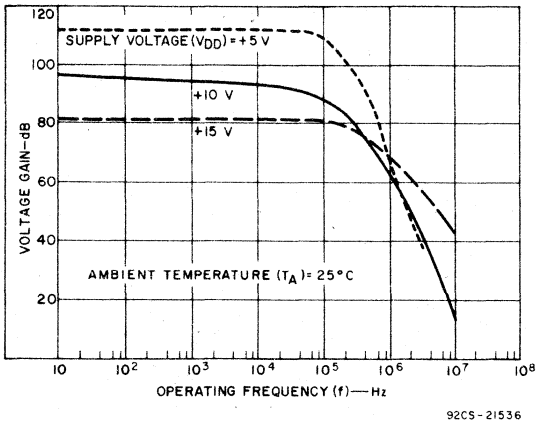


Fig. 17– Typical voltage gain vs. operating frequency characteristics for three-stage COS/MOS transistor-pair amplifier in Fig. 16.

Post-Amplifiers For Op-Amps

COS/MOS transistor-pairs can be advantageously applied as post-amplifiers for op-amps. Because the input impedance of the COS/MOS pair is comparatively high, the op-amp operates under essentially unloaded conditions. Each COS/MOS pair can sink and source output current up to about 10 mA. Additionally, the op-amp output can be directly coupled to bias the COS/MOS pair. A detailed description of the subject has been published previously.[2]

The schematic diagram in Fig. 18 shows a COS/MOS transistor-pair serving as a post-amplifier to an RCA-CA3080 Operational Transconductance Amplifier.[3] The approximate 30-dB gain in a single COS/MOS transistor-pair is an added increment to the 100-dB gain in the CA3080, yielding a total forward gain of about 130 dB. The open-loop slew rate of the circuit in Fig. 19 is approximately 65 V/μs. When compensated for the unity-gain voltage-follower mode shown in Fig. 19, the slew rate is about 1 V/μs. For greater current output, the two remaining transistor pairs of the CA3600E may be connected in parallel with the single stages shown in Figs. 18 and 19.

The use of the two-stage COS/MOS post-amplifier shown in Fig. 20 increases the total open-loop gain of the system to about 160 dB (100,000,000X). Open-loop slew rate remains at about 65 V/μs. A slew rate of about 1 V/μs is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Fig. 21. These circuits operate in concert with stability.

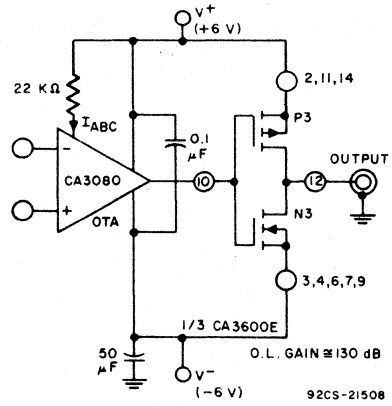


Fig. 18– COS/MOS transistor-pair used as post-amplifier to op-amp in open-loop circuit.

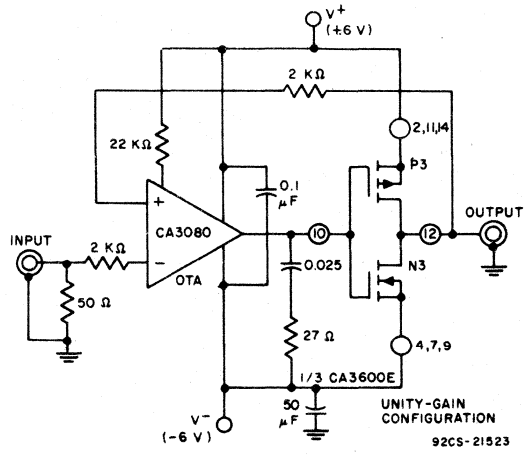


Fig. 19– COS/MOS transistor-pair used as post-amplifier to op-amp in unity-gain circuit.

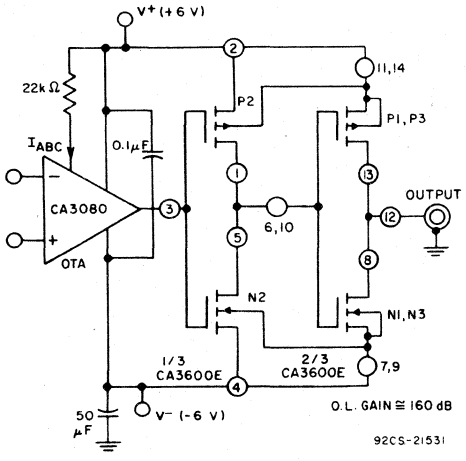


Fig. 20– COS/MOS transistor-pairs used as two-stage post-amplifier to op-amp in open-loop circuit.

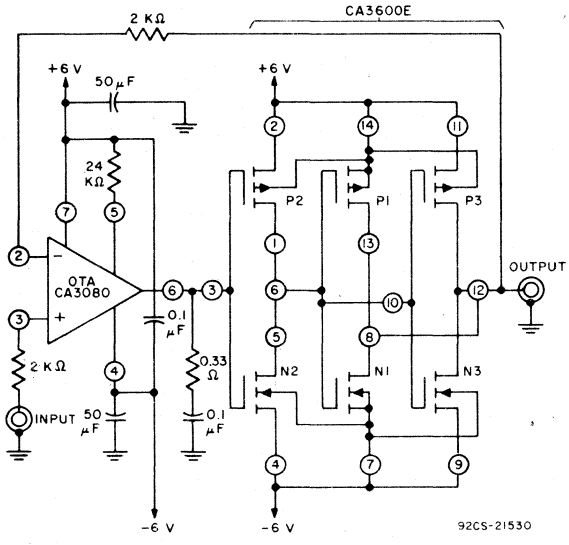


Fig. 21– Unity-gain amplifier uses COS/MOS transistor-pairs as two-stage post-amplifier to op-amp.

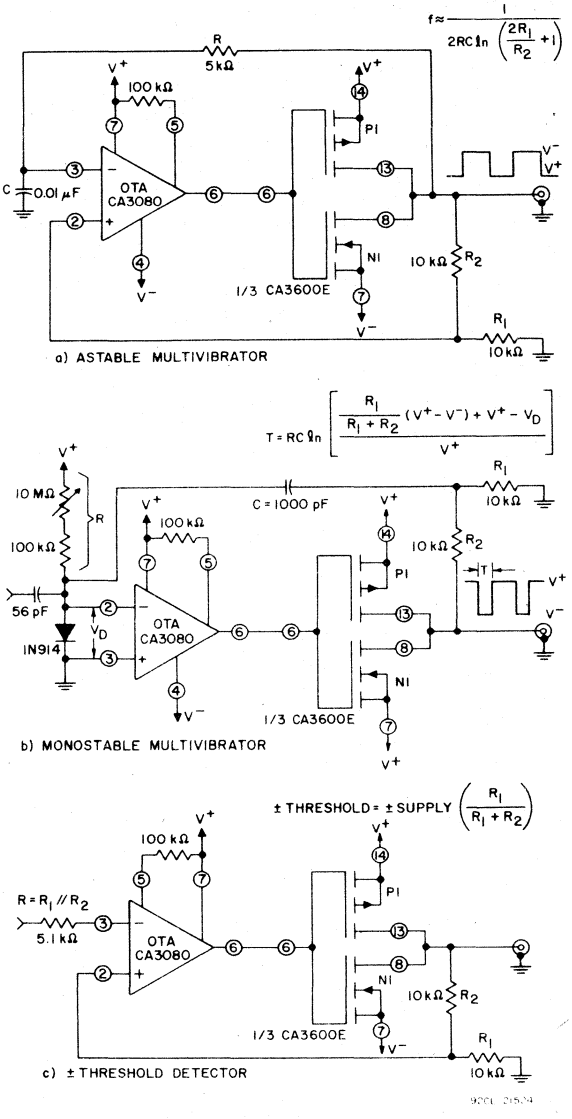


Fig. 22– Multistable circuits using COS/MOS transistor-pairs.

Multivibrators, Threshold Detectors, and Comparators

Descriptions of several circuits using COS/MOS transistor-pairs in both monostable and astable multivibrators have been published.[4,5] The characteristics of COS/MOS pairs are also ideal for mating with micropower op-amps in circuits such as the precision multistable circuits shown in Fig. 22. In these circuits precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080 Operational Transconductance Amplifier.[2,3] Moreover, speed vs. power consumption tradeoffs can be made by adjustment of the Amplifier-Bias-Current (I_{ABC}) supplied to terminal 5 of the CA3080. The quiescent power consumption of the circuits shown in Fig. 22 is typically 6 mW, but can be made to operate in the micropower region by suitable modifications.

The schematic diagram of a programmable micropower comparator, shown in Fig. 23 employs the combination of an op-amp (CA3080A) and COS/MOS transistor-pairs in the CA3600E. Quiescent power consumption of the circuit is about 10 μW(typ.). When the comparator is strobed "ON", transistor P1 is driven into conduction and the OTA becomes active. Under these conditions, the circuit consumes 420 μW and responds to a differential-input signal in about 8 μs. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150 ns but the power consumption is increased to 21 mW. The differential amplifier input common-mode range for this circuit is −1 V to +10.5 V. Voltage gain of this micropower comparator is typically 130 dB.

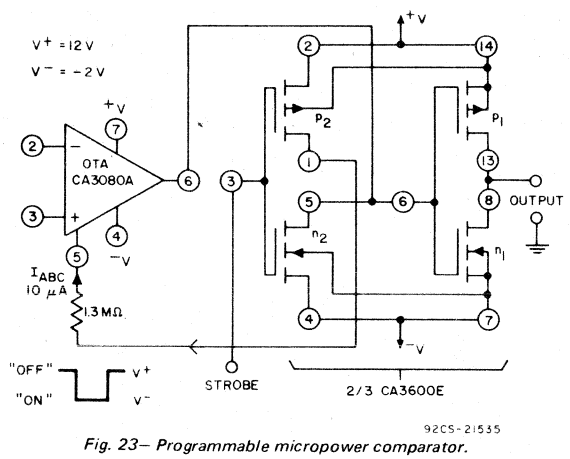


Fig. 23– Programmable micropower comparator.

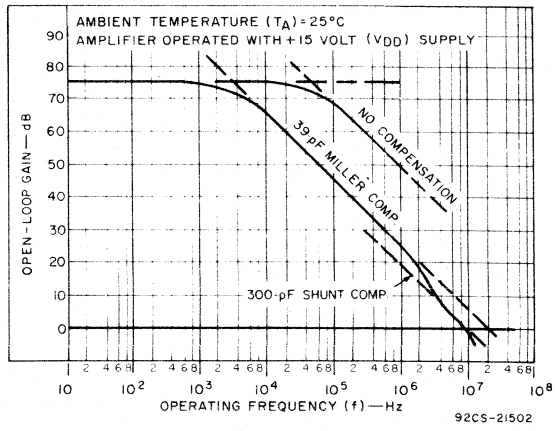


Fig. 25– Open-loop gain characteristic for op-amp in Fig. 24.

Operational Amplifiers

COS/MOS transistor-pairs can be used in conjunction with a bipolar transistor-array IC to build an op-amp as shown in Fig. 24. It is particularly suited for single-supply operation (e.g., mobile and aircraft service). The op-amp is unique in that it is responsive to small-signal ground-referenced inputs and the output stage can easily be driven within 1 mV of ground potential. Its open-loop gain characteristics are shown in Fig. 25; the open-loop slew rate is approximately 30 V/μs.

This circuit is ideal for use as a unity-gain voltage-follower and has been described for operation in connection with a 9-Bit Single-Supply Digital-to-Analog Converter (DAC) using COS/MOS transistors in the resistor-network switches.[6]

The op-amp in Fig. 24 has three stages; its first stage is a differential input circuit using two p-channel transistors (P_4,P_5) in a CA3600E. The second stage is an n-p-n

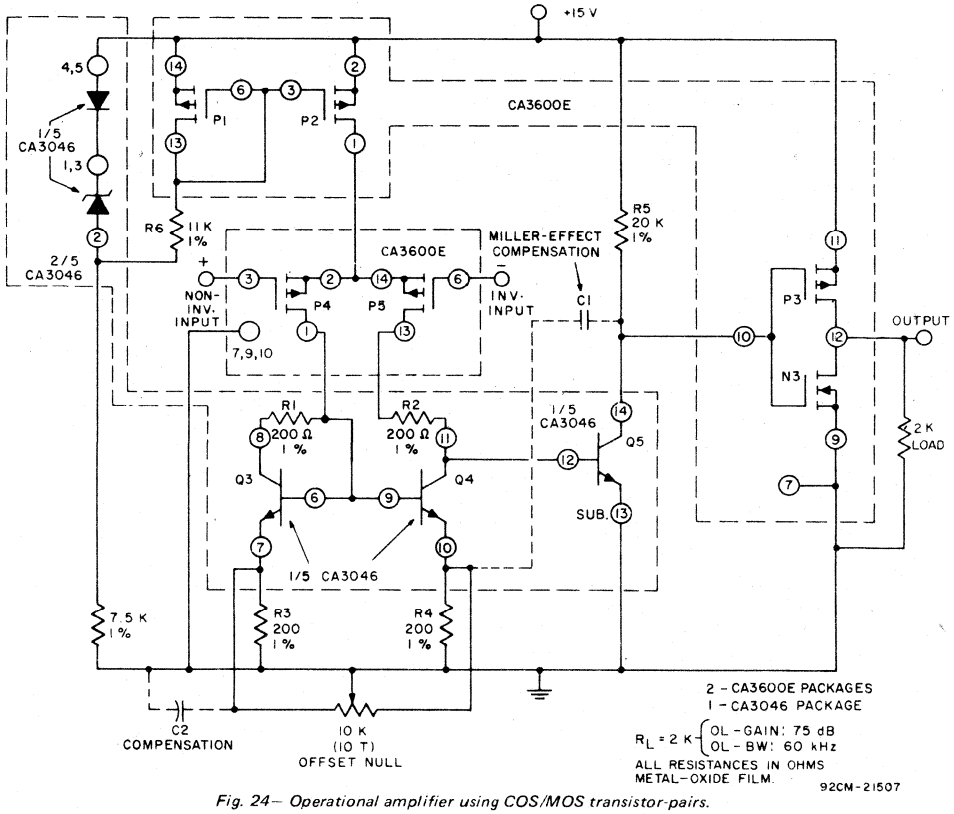


Fig. 24– Operational amplifier using COS/MOS transistor-pairs.

transistor (Q_5) and the output stage is a COS/MOS transistor-pair (P_3,N_3) operating in the manner described above. A constant current of about 400 μA is established in the differential input stage by the zener network in the upper-left portion of Fig. 24. The zener network energizes a current mirror comprised of two p-channel transistors (P_1,P_2) to establish constant-current flow in the differential amplifier stage (P_4,P_5). The drain load for the differential amplifier consists of resistors R_1R_4 and a current mirror (Q_3 Q_4) to optimize conditions for balanced operation of the differential amplifier. The operating theory of current-mirror circuits has been described in reference [2]. Amplifier voltage-offset is nulled with the 10-kilohm balance potentiometer. The second-stage current is established by R_5, and is selected to approximate the first-stage current level (400 μA), to assure similar positive and negative slew rates. The amplifier is shown driving a 2-kilohm load, a typical value used with monolithic op-amps. Voltage gain varies inversely with the choice of load resistance.

The amplifier can be compensated with a single capacitor (C_1), connected as shown by the dotted lines. However, optimum compensation for the unity-gain non-inverting mode is provided by two capacitors: Miller Effect feedback through a 39-pF capacitor C_1 (connected as shown), and a 300-pF capacitor connected between terminals 7 and 13 of the CA3046 transistor array to shunt one-half the driving current. Fig. 25 shows the open-loop gain characteristics with compensation for unity-gain operation. When the amplifier is operated as a voltage-follower, it is recommended that a 1-kilohm resistor, shunted with a 150-pF capacitor, be connected between the amplifier output terminal and terminal 6 of P_5 to avoid a potential latch situation involving the integral gate-protection network. The circuit can also be latched if either input terminal is driven more than about 0.7 volt below ground potential. This latch situation can be avoided by connecting a 1N914 diode from each input terminal to ground, with the diode anode grounded.

Analog Timer

The CA3600E is useful in the design of analog timer circuits. A typical circuit is shown in Fig. 26. For purposes of explanation, let it be assumed that capacitor C_1 initially is in a completely discharged condition; terminal 10, therefore, is initially at ground potential and transistor N_3 is non-conductive. The circuitry at the left of terminal 10 provides a source of constant-current flow through P_1 to charge capacitor C_1 increasingly positive with respect to ground. After the passage of time (T), capacitor C_1 is charged sufficiently in the positive direction so that transistor N_3 is driven into conduction by its gate and the lamp is lighted to signify the end of the time-delay period. The circuit is reset by momentarily closing switch S_1 to discharge capacitor C_1 through R_4.
Resistor-divider network R_1,R_2 establishes the supply voltage to a constant-current network comprised of resistor R_3 and the series-connected COS/MOS pair N_2,P_2, biased for linear operation by resistor R_b as previously described. This combination is connected to the gate terminal (No. 6) of transistor P_1 to form a current mirror, i.e., the current flowing through P_1 to charge C_1 will be essentially equal to the constant-current flow established through R_3, N_2, and P_2. A description of current-mirror operation with MOS transistors is given subsequently.

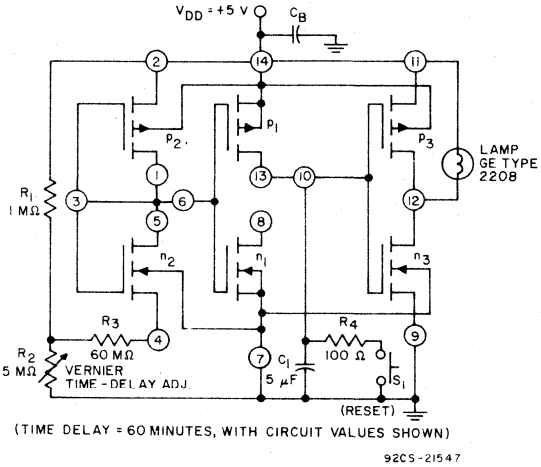


Fig. 26– Analog timer using CA3600E.

Oscillator Circuits

Oscillator circuits using COS/MOS transistor-pairs have been widely used for several years in clock and watch circuits because of their low power consumption and good frequency stability. Details of their operating theory and characteristics have been published.[5,7]

The design of COS/MOS oscillator circuits, like the design of any oscillator circuit, involves the provision of an amplifying section to operate compatibly with an appropriate feedback network. A single stage amplifier using a COS/MOS transistor-pair has already been described. A suitable feedback network to insure stable oscillator performance is easily added, as illustrated in connection with the crystal oscillator circuit shown in Fig. 27. The familiar pi-network has been connected between the input and output terminals, points "D" and "G", to provide the required 180° phase shift for stable oscillator performance. The frequency-determining crystal is an integral part of the pi-network feedback circuit. The resistors R_1 and R_2 decrease the total power consumption of the oscillator at a particular supply voltage and enhance the frequency stability. Variable frequency oscillators can be built by replacing the crystal with an appropriate inductance and tuning the pi-network by conventional means.

Current Mirrors Using MOS Transistors

Monolithic linear IC's using bipolar transistors frequently employ so-called "current-mirror" circuits. The theory and practical applications of current mirrors using bipolar transistors have been described in the literature.[2] As shown in

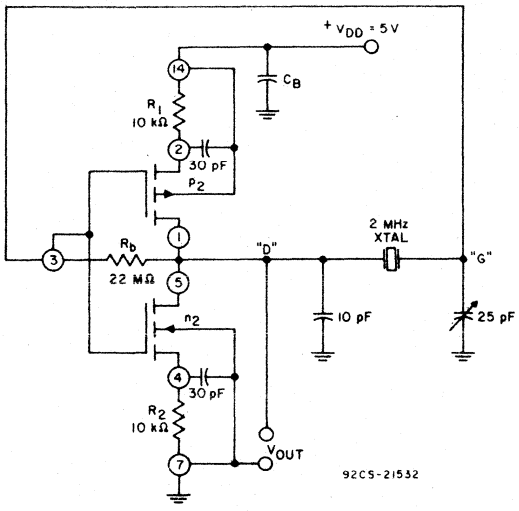


Fig. 27– Typical crystal-oscillator circuit using COS/MOS transistor-pair (1/3 CA3600E).

Fig. 28, a rudimentary form of "current-mirror" consists of a transistor Q_1 with a second transistor Q_2 connected as a diode. When both transistors have identical characteristics, a current I_1 forced to flow through Q_2 produces a current (I_2) of equal magnitude to flow in the collector of Q_1 (provided there is sufficient collector potential for Q_1). In a common form of application, a source of potential is used to force

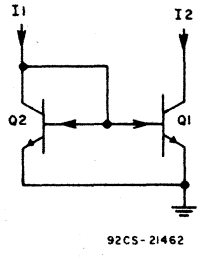


Fig. 28– Current mirror using n-p-n bipolar transistors.

constant-current flow I_1, and thus to establish the flow of constant current I_2 through Q_1. Arrangements of this generic current-mirror type are frequently used when Q_1 acts as the common-emitter impedance in a differential-amplifier circuit.

MOS transistors are also applicable as current mirrors, as shown in Fig. 29. The diode-connected MOS transistor N_2 functions as a transistor with 100 per-cent feedback. Therefore, the gate-to-source voltage (V_{GS}) in N_2 retains control of the drain current as in normal transistor action, i.e., $I_D \cong g_{fs}V_{GS}$, where g_{fs} is the forward transconductance of the device. If a current I_1 is forced into the diode-connected transistor (N_2), the gate-to-source voltage will rise until equilibrium is reached. Thus, a gate-to-source voltage is established in N_2 such that N_2 "sinks" the applied current I_1.

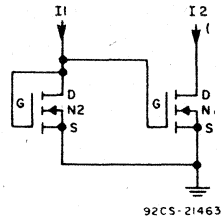


Fig. 29– Current mirror using n-channel MOS transistors.

If the gate and source terminals of another transistor (N_1) are connected in shunt with the gate and source terminals of N_2, as shown in Fig. 29, N_1 is also able to "sink" a mirror current approximately equal to that flowing in the drain lead of the diode-connected transistor N_2. It is assumed that both MOS transistors have identical characteristics, a prerequisite that is essentially established by the monolithic IC fabrication technology used in manufacturing the CA3600E COS/MOS transistor array.

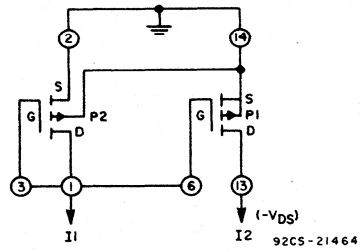


Fig. 30– Current mirror using p-channel MOS transistors in CA3600E.

Current mirrors can also be designed with p-channel MOS transistors as illustrated by the arrangement in Fig. 30 using transistors in the CA3600E. The characteristics of a current mirror using the p-channel transistors in the CA3600E are superior to those which can be achieved with a current mirror using the n-channel transistors because the characteristics of the p-channel transistors are more nearly matched. The data

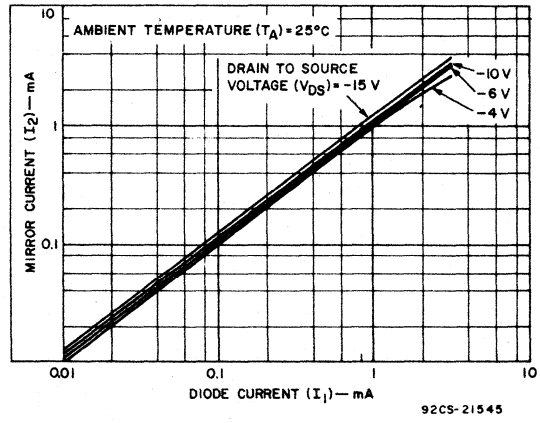


Fig. 31– Characteristics of current mirror circuit of Fig. 30 using p-channel transistors.

contained in Fig. 31 show the high degree of tracking between I_1 and I_2 for several values of drain voltage V_D. Fig. 32 also illustrates the fact that this high degree of tracking between I_1 and I_2 can be maintained to within about one per-cent despite wide variations in ambient temperature.

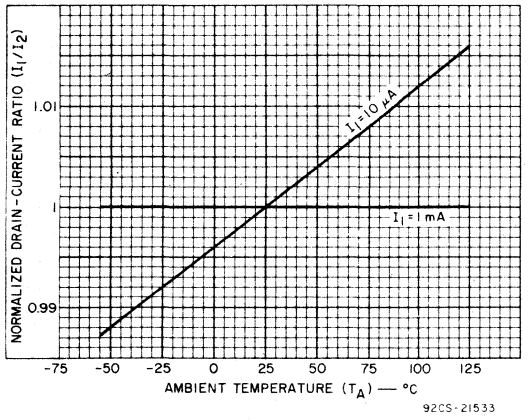


Fig. 32– Normalized drain current ratio vs. ambient temperature for typical current mirror using p-channel transistors (Fig. 30).

The op-amp circuit in Fig. 24 contains an illustrative example of a current-mirror circuit using two p-channel transistors in the CA3600E. Transistor P_2 serves as a constant-current source (≅ 400 μA) for the differential amplifier, consisting of transistors P_4 and P_5 and their drain-load network. Transistor P_2 is in a "mirrored" connection with transistor P_1. A stabilized source of supply potential is developed across the zener diode (terminals 11 and 12 of the CA3083) and drives about 400 μA of current through R_6 and P_1.

Complementary Current Mirrors Using COS/MOS Transistor-Pairs

COS/MOS transistor-pairs can be applied advantageously in the design of Complementary Current-Mirrors, as shown in Fig. 33. Transistors P_1 and N_1 are series-connected and biased for linear operation as previously described, so that there is a current flow I_{D1} through P_1 and N_1. The potential developed between terminals 13 and 14 is applied as gate-source (2,3) voltage for P_2, forcing "mirror" operation of P_2 to produce a current source I_{D2-P} equal to I_{D1}. Likewise, the potential developed between terminals 7 and 8 is applied as gate-source (3,4) voltage for N_2 forcing "mirror" operation of N_2 to produce a current-sink I_{D2-N} equal to I_{D1}.

A variant of this complementary current mirror is used in the analog timer circuit shown in Fig. 26. Transistors P_2 and N_2 are series-connected together with a 60-megohm resistor to establish their drain current at 5 nA. The potential developed across terminals 1 and 2 also appears as the gate-source voltage for transistor P_1, thereby establishing a mirror-current source of 5 nA at terminal 13 to charge capacitor C_1 linearily. In this circuit, the "mirrored" current-sink available at terminal 8 (transistor N_1) is unused. This type of current-mirror configuration is exceptionally stable with temperature variations.

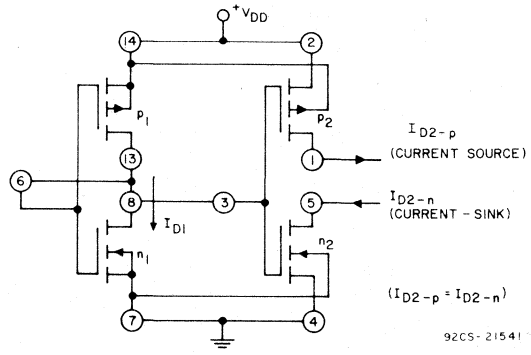


Fig. 33– Complementary current mirrors using COS/MOS transistor-pairs in CA3600E.

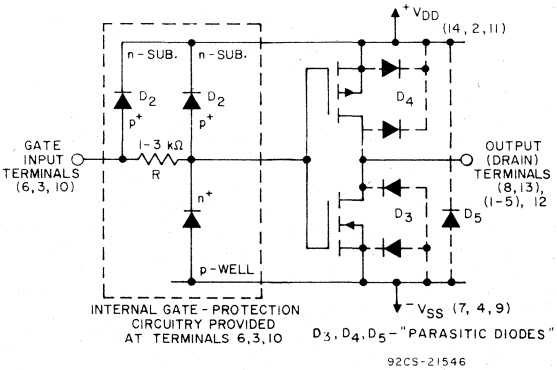


Fig. 34– Integral protection circuits used in CA3600E.

Considerations in Handling CA3600E Devices

Failure of the gate-channel oxide was a persistent problem in early MOS devices. The breakdown of the oxide is generally in the order of 100 volts, and the dc resistance is in the order of 10^{12} ohms. Because of this extremely high resistance, even a very-low-energy source (such as static charge) is capable of developing sufficient voltage to cause damage. Furthermore, the oxide can be punctured and damaged by a single voltage excursion beyond the breakdown limit.

Fig. 34 shows a protection circuit[5,8] which is incorporated at each gate-lead of the CA3600E. A typical value of 1 to 3 kilohms is used for the input resistor R, which functions in combination with the capacitance of the gate and the associated protective diode to integrate and clamp input voltages to a safe level. This circuit also shows the "substrate diodes" (D_3, D_4, and D_5) which provide protection to the MOS channels at the output terminals.

Although the gate-protection system is very effective in guarding against damage due to static charges, it is prudent to observe the following precautions:[5,9]

1. The leads of devices should be in contact with a conductive material, except when being tested or in actual operation. A conductive material such as "ECCOSORB LD26"* or equivalent is suggested for use during storage and/or handling. Devices should not be inserted in non-conductive containers such as conventional plastic "snow" or trays.
2. Soldering-iron tips, metal parts of fixtures and tools, and handling facilities should be grounded.
3. Devices should not be inserted into or removed from circuits with the power on because transient voltages may cause permanent damage.
4. Signals from low-impedance sources should not be applied to the gate terminals while the power supply is off. As a corollary, it follows that the power supply should not be turned off while a signal from a low-impedance source is being applied to any gate terminal. When the V_{DD} supply is off, the positive "back-bias" voltage is removed from the cathode of diode D_2 (see Fig. 34). Consequently, an input signal with positive-going polarity can drive D_2 into conduction. Under these conditions a low-impedance signal source can provide sufficient current to permanently damage D_2 and/or melt aluminum interconnection paths. Therefore, if, in any system design using the CA3600E, any gate input excursion is expected to exceed $+V_{DD}$ or fall below $-V_{SS}$, the current through the input diodes should be limited to 100 μA.
5. All unused gate-input terminals should be connected to V_{SS} (ground). When source terminals (e.g., Nos. 2 and 11) of p-channel transistors are unused in circuitry, they should be connected to terminal No. 14. Likewise, when source terminals (e.g., Nos. 4 and 9) of n-channel transistors are unused, they should be connected to terminal No. 7.
6. After CA3600E units have been mounted on circuit boards, proper handling precautions should still be observed. Until these subassemblies are inserted into a complete system, the board is no more than an extension of the device leads mounted on the board. It is a good practice to place conductive tape or jumpers on circuit-board terminals to "ground" gate terminals.
7. In some applications of the CA3600E separate positive and negative power supplies may be employed (e.g., see Fig.22). In such applications provisions must be made so that the positive supply voltage is applied prior to the application of negative supply voltage and vice versa on shutdown. This precaution is necessary to avoid possible damage due to "latching" involving the substrate and protective diode circuits.

* Trade Mark: Emerson and Cumming, Inc.

Power Control Circuits
Technical Data

CA3165

Mini-DIP
(E Suffix)
H-1817

14-Lead DIP
(E1 Suffix)
H-1517

Electronic Switching Circuit

FEATURES:

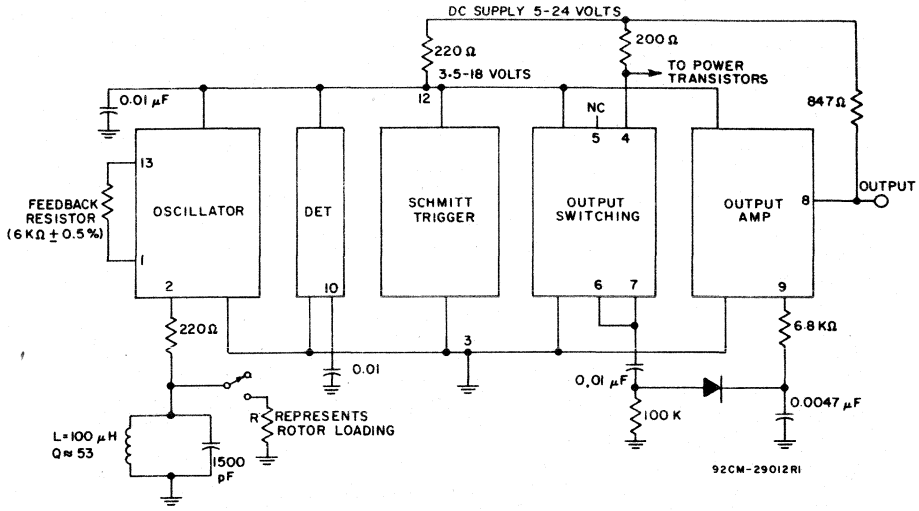
- *Switching initiated by damping of internal oscillator*
- *Proximity sensing of rotational motion*
- *Repeatable timing of switching states*
- *Five outputs — two complementary pairs and one non-inverting output (CA3165E1)*
- *Two outputs — one complementary pair (CA3165E)*

The RCA CA3165 is a single-chip electronic switching circuit intended primarily for ignition applications. It includes an oscillator that is amplitude-modulated by the rotor teeth of a distributor, a detector that develops the positive-going modulation envelope, a Schmitt trigger that eliminates switching uncertainties. Both types include two complementary high-current switched outputs for driving power transistors requiring up to 120 milliamperes. The CA3165E also includes two complementary low-current outputs that incorporate internal current limiting and a non-inverting output amplifier with uncommitted input capable of switching 27 milliamperes.

The CA3165 is supplied in the 8-lead dual-in-line plastic package (Mini-DIP, E suffix) and in the 14-lead dual-in-line plastic package (E1 suffix).

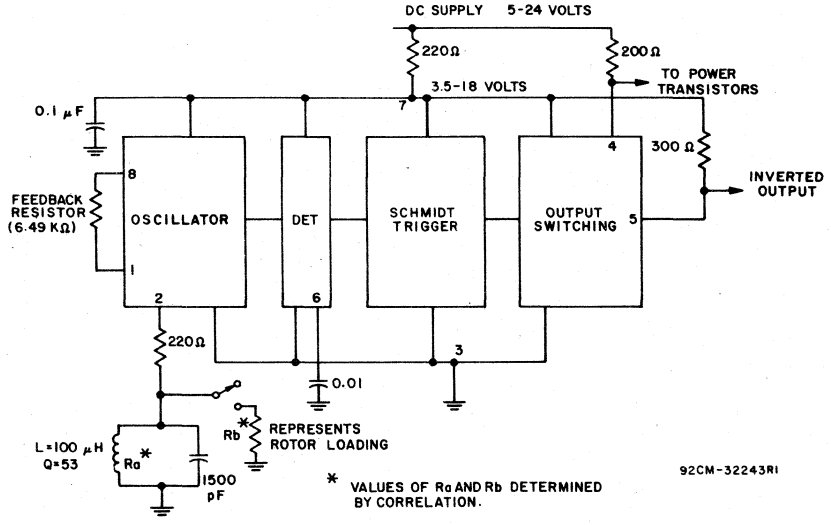
MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3165E1	CA3165E		
DC Voltage (With reference to terminal 3):				
Terminal	4,6,8	4,5	24	V
Terminal	5,7,12	7	18	V
Terminal	9	—	1.5	V
CURRENT (At terminals indicated):				
Terminal	4,6	4,5	120	mA
Terminal	5,7	—	-0.1 to 0.1	mA
Terminal	8	—	30	mA
DEVICE DISSIPATION:				
Up to T_A = 55° C			600	mW
Above T_A = 55°C		derate linearly at	6.67	mW/°C
AMBIENT TEMPERATURE RANGE:				
Operating			-40 to +85	°C
Storage			-65 to +150	°C
LEAD TEMPERATURE (During soldering):				
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.			265	°C



Oscillator Condition	Terminal 10	Terminal 4	Terminal 5	Terminal 6	Terminal 7	Terminal 8
Unloaded	Low	High	High	Low	Low	Low
Loaded	High	Low	Low	High	High	High

Fig. 1 - Functional block diagram for CA3165E1



Oscillator Condition	Terminal 4	Terminal 5	Terminal 6
Unloaded	High	High	Low
Loaded	Low	Low	High

Fig. 2 - Functional block diagram for CA3165E

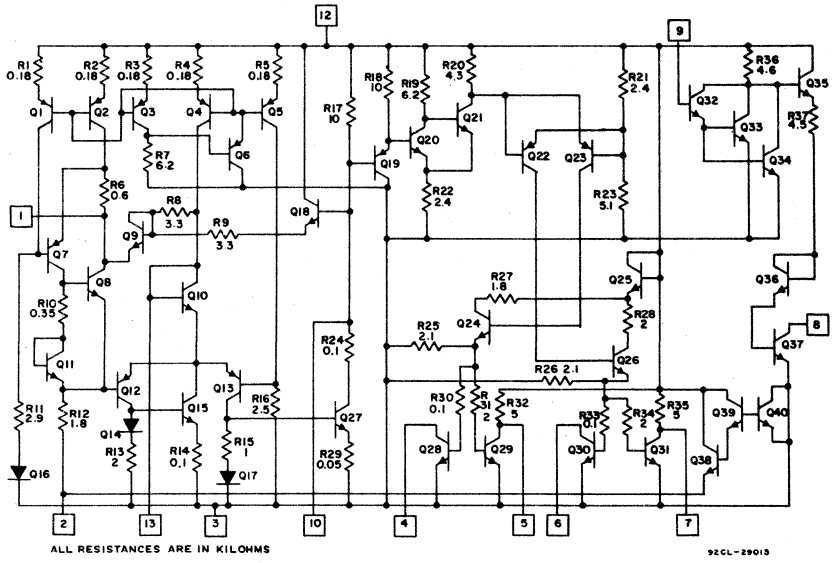


Fig. 3 - Schematic diagram for CA3165E1

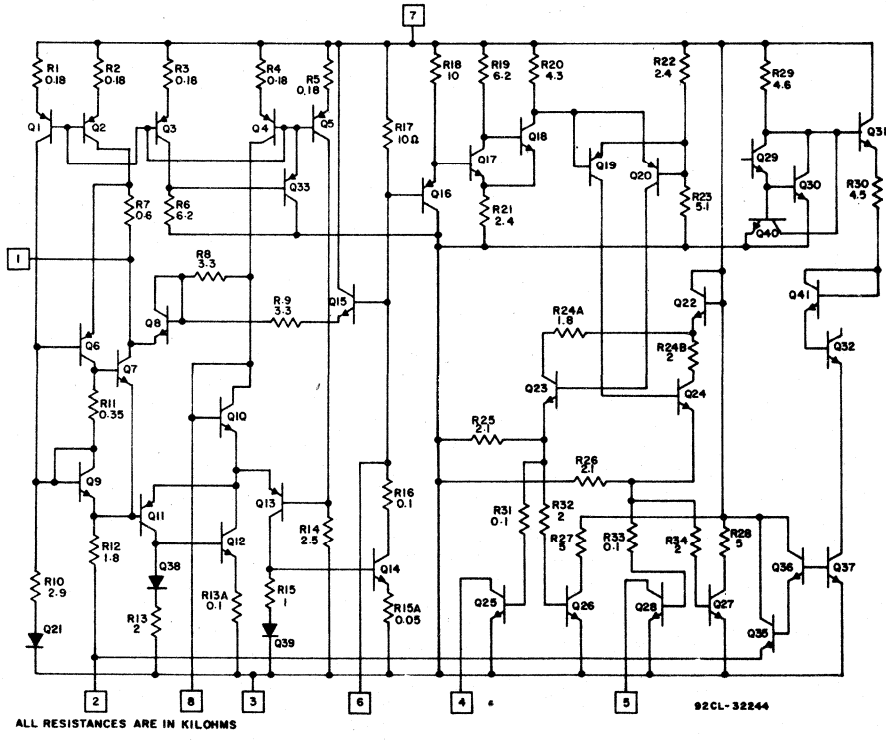


Fig. 4 - Schematic diagram for CA3165E

ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$, $V^* = 13$ V, Measured in the circuit of Fig. 5 (CA3165E1) or Fig. 6 (CA3165E)

CHARACTERISTIC	TEST PERIOD	LIMITS						UNITS
		CA3165E1			CA3165E			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Current at Term.* Δ	Dwell	—	18.4	—	—	18.4	—	mA
	Spark	—	17.5	—	—	17.5	—	
Output Voltage at Term. 4 V_4	Dwell	12.8	—	—	12.8	—	—	V
	Spark	—	—	0.5	—	—	0.5	
Output Voltage at Term. 7 V_7	Dwell	—	—	1	—	—	—	V
Output Voltage at Term. 8 V_8	Dwell Portion of Spark	—	—	0.9	—	—	—	V
		1.2	—	—				
Oscillator Voltage at Term. 2 V_2	Dwell	—	4.4	—	—	4.4	—	V_{p-p}
	Spark	—	0.6	—	—	0.6	—	

	*	Δ
CA3165E	7	I_7
CA3165E1	12	I_{12}

APPLICATION INFORMATION

Figs. 5 and 6 shows the application of the CA3165 in a typical ignition system.

TERMINAL DESCRIPTIONS		
Terminal		
CA3165E1	CA3165E	Function
1	1	Oscillator feedback resistor, R_f
2	2	220Ω protective resistor to tank circuit
3	3	Ground
4	4	Direct output — R_7 load resistor 200 ohms ± 5%, and R_8 to power Darlington 15 ohms ± 10%
5	—	Direct output — low current — not connected
6	5	Inverted high current output
7	—	Inverted low current output through C_1 (0.01 μF) to D_3 and R_3 (100 K ohm)
8	—	Output amplifier output — through R_6 and R_5 (27 ohms and 820 ohms to supply)
9	—	Output amplifier input — through R_4 (6800 ohms) to D_3 and C_5 (0.0047 μF)
10	6	Detector output — C_2 to ground (0.0022 μF)
11	—	No connection
12	7	Circuit supply voltage through R_1 (220 ohms protective resistor) to automotive supply
13	8	Oscillator feedback resistor R_f to terminal 1
14	—	No connection

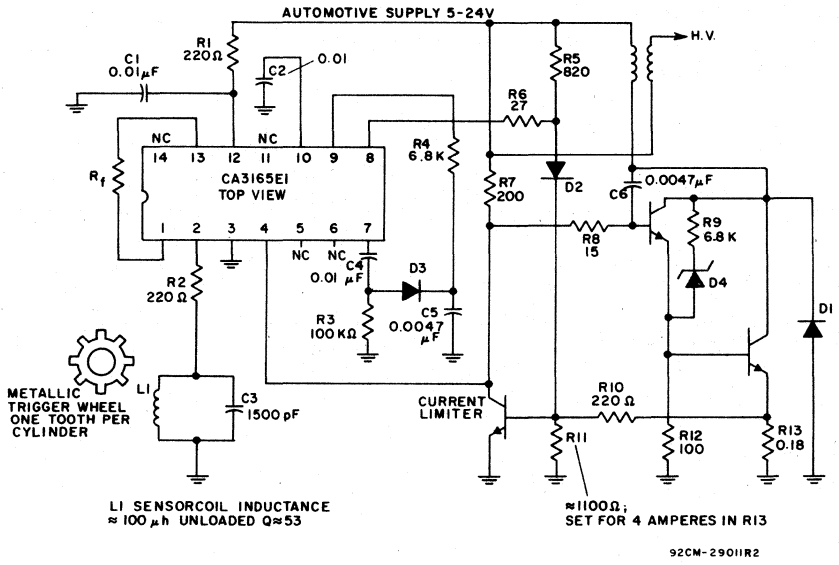


Fig. 5 - Typical ignition system using the CA3165E1

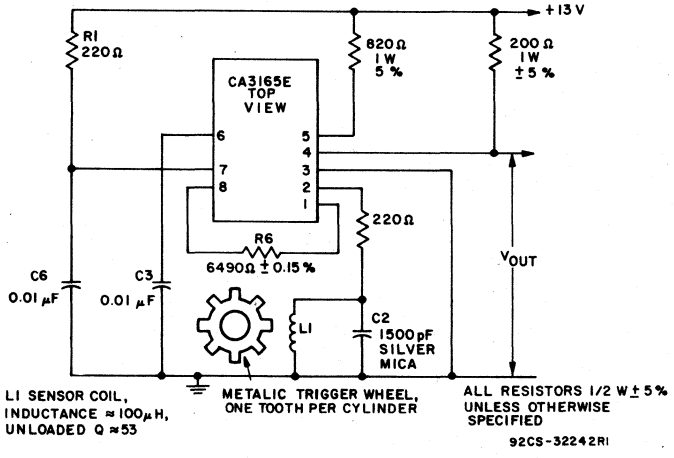


Fig. 6 - Typical ignition system using the CA3165E

APPLICATION INFORMATION

Figs. 5 and 6 shows the application of the CA3165 in a typical ignition system. The oscillator on the chip operates at about 400 kHz as determined by the tuned circuit L1, C3. The amplitude of the oscillation is detected on the chip and applied to a Schmitt trigger which sets the terminal voltage as shown in the chart in Figs. 1 and 2 for the unloaded condition of the oscillator. As a metallic tooth in the rotor passes the coil L1 eddy-current losses occur which reduce the Q of the resonant circuit and decrease the amplitude of the oscillations to a level below that of a reference in the detector circuit. The output terminals are then switched to states as shown in the chart in Figs. 1 and 2 for the loaded condition of the oscillator. The oscillation is maintained at this lower amplitude by switching in additional feedback in the oscillator circuit. The fact that the oscillator continues to operate at some minimum level during this dwell period eliminates timing variations which would occur if the oscillator had to be restarted by random noise.

Spark occurs as terminal 4 is switched from high to low. The output amplifier clamps terminal 4 low through the regulator during the duration of the spark.

The Dwell period represents the time that terminal 10 (CA3165E1) or terminal 6 (CA3165E) is high, terminal 4 is low, and the coil is charged.

The value of the oscillator feedback, resistor, R_f, is selected to set the dwell period. With a sintered-iron 8 f-tooth rotor, a typical value of R_f is 6500 ohms for 28.5 degrees of dwell out of a 45 degree cycle. For a star-type rotor and a particular coil in a typical distributor, the feedback resistor would be larger (typically 8800 ohms) depending on clearances, coil geometry and tooth shape.

Timing waveforms are shown in Fig. 7.

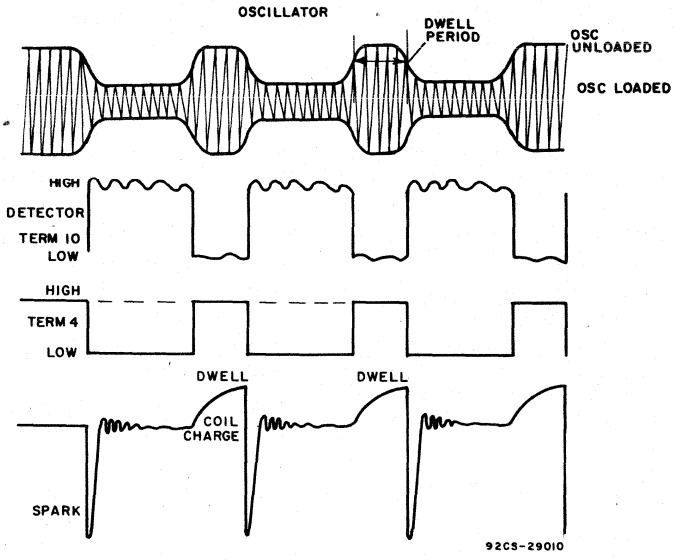
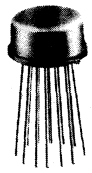


Fig. 7 - Timing sequence

CA3020, CA3020A



12-Lead TO-5

H-1528

Multipurpose Wide-Band Power Amplifiers

For Military, Industrial, and Commercial Equipment at Frequencies up to 8 MHz

Features:

- **High power output — class B amplifier. . . CA3020 — 0.5 W typ. at V_{CC} = +9 V CA3020A — 1.0 W typ. at V_{CC} = +12 V**
- **Wide frequency range. . . Up to 8 MHz with resistive loads**
- **High power gain. . .75 dB typ.**
- **Single power supply for class B operation with transformer. . . CA3020 — 3 to 9 V CA3020A — 3 to 12 V**
- **Built-in temperature-tracking voltage regulator provides stable operation over −55°C to +125°C temperature ran**

The RCA-CA3020 and CA3020A are integrated-circuit, multistage, multipurpose, wide-band power amplifiers on a single monolithic silicon chip. They employ a highly versatile and stable direct-coupled circuit configuration featuring wide frequency range, high voltage and power gain, and high power output. These features plus inherent stability over a wide temperature range make the CA3020 and CA3020A extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

The CA3020 and CA3020A are particularly suited for service as class B power amplifiers. The CA3020A can provide a maximum power output of 1 watt from a 12-volt dc supply with a typical power gain of 75 dB. The CA3020 provides 0.5-watt power output from a 9-volt supply with the same power gain.

These types are supplied in hermetically sealed TO-5 style 12-lead packages.

SCHEMATIC DIAGRAM FOR CA3020 AND CA3020A

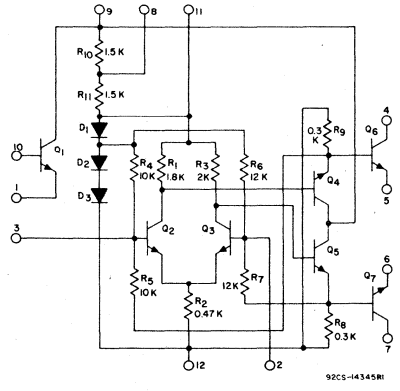


Fig.1

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ± 30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

Applications:

- **AF power amplifiers for portable and fixed sound and communications systems**
- **Servo-control amplifiers**
- **Wide-band linear mixers**
- **Video power amplifiers**
- **Transmission-line driver amplifiers (balanced and unbalanced)**
- **Fan-in and fan-out amplifiers for computer logic circuits**
- **Lamp-control amplifiers**
- **Motor-control amplifiers**
- **Power multivibrators**
- **Power switches**
- **Companion Application Note, ICAN-5766, "Application of CA3020 and CA3020A Integrated Circuit Multipurpose Wide-Band Power Amplifiers"**

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION:

WITHOUT HEAT SINK	WITH HEAT SINK
At T_A = 25°C . . . . . 1 W	At T_C = 25°C . . . . . 2 W
Above T_A = 25°C . . . . . derate linearly 6.7 mW/°C	At T_C = 25°C to T_C = 55°C . . . . . 2 W
	Above T_C = 55°C . . derate linearly 16.7 mW/°C

TEMPERATURE RANGE:

Operating . . . . . -55°C to +125°C
Storage . . . . . -65°C to +150°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to terminal 12 is 0 to +10 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
1		*	*	*	*	*	*	*	▲ 0 -10/-12	+3 Note 1	*	+10 0
2			*	*	*	*	*	*	*	*	*	+2 -2
3				*	*	*	*	*	*	*	*	+2 -2
4					▲ +18/+25 0	*	*	*	*	*	*	▲ +18/+25 0
5						*	*	*	*	*	*	+3 Note 2
6							▲ 0 -18/-25	*	*	*	*	+3 Note 2
7								*	*	*	*	▲ +18/+25 0
8									Note 3	*	*	Note 3 0
9										+10 0	Note 1 0	+10/+12 0
10											*	+10 0
11												*
12												REF. SUB-STRATE

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	-	20
2	-	-
3	-	-
4	300	-
5	-	300
6	-	300
7	300	-
8	-	-
9	20	-
10	1	-
11	20	-
12	-	-

Note 1: This voltage is established by the maximum current rating.

Note 2: The emitters of Q_6 and Q_7 may be returned to a negative voltage supply through emitter resistors. Current into terminal No.9 should not be exceeded and the total device dissipation should not be exceeded.

Note 3: Terminal No.8 may be connected to terminals Nos.9, 11, or 12.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

▲ Higher value is for CA3020A.

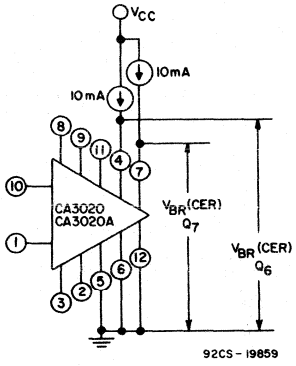
CA3020, CA3020A

ELECTRICAL CHARACTERISTICS AT $T_A = 25°C$

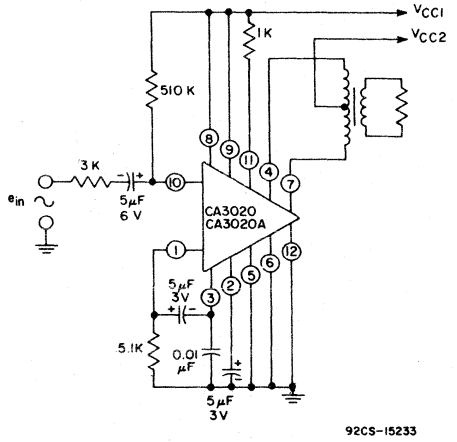
CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			LIMITS CA3020			LIMITS CA3020A			UNITS
		CIRCUIT AND PROCEDURE	DC SUPPLY VOLTAGE								
		FIG.	V_{CC1}	V_{CC2}	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Collector-to-Emitter Breakdown Voltage, Q_6 & Q_7 at 10 mA	$V_{(BR)CER}$	2a	-	-	18	-	-	25	-	-	V
Collector-to-Emitter Breakdown Voltage, Q_1 at 0.1 mA	$V_{(BR)CEO}$	-	-	-	10	-	-	10	-	-	V
Idle Currents, Q_6 & Q_7	I_4 IDLE I_7 IDLE	8	9.0	2.0	-	5.5	-	-	5.5	-	mA
Peak Output Currents, Q_6 & Q_7	I_4PK I_7PK	8	9.0	2.0	140	-	-	180	-	-	mA
Cutoff Currents, Q_6 & Q_7	I_4 CUTOFF I_7 CUTOFF	8	9.0	2.0	-	-	1.0	-	-	1.0	mA
Differetial Amplifier Current Drain	I_{CC1}	8	9.0	9.0	6.3	9.4	12.5	6.3	9.4	12.5	mA
Total Current Drain	I_{CC1} + I_{CC2}	8	9.0	9.0	8.0	21.5	35.0	14.0	21.5	30.0	mA
Differential Amplifier Input Terminal Voltages	V_2 V_3	8	9.0	2.0	-	1.11	-	-	1.11	-	V
Regulator Terminal Voltage	V_{11}	8	9.0	2.0	-	2.35	-	-	2.35	-	V
Q, Cutoff (Leakage) Currents: Collector-to-Emitter	I_{CEO}	-	10.0	-	-	-	100	-	-	100	μA
Emitter-to-Base	I_{EBO}		3.0	-	-	-	0.1	-	-	0.1	
Collector-to-Base	I_{CBO}		3.0	-	-	-	0.1	-	-	0.1	
Forward Current Transfer Ratio, Q_1 at 3 mA	h_{FE1}	-	6.0	-	30	75	-	30	75	-	
Bandwidth at -3 dB Point	BW	9	6.0	6.0	-	8	-	-	8	-	MHz
Maximum Power Output	$P_{O(MAX)}$	10	6.0	6.0	200	300[a]	-	200	300[a]	-	mW
			9.0	9.0	400	550[a]	-	400	550[a]	-	
			9.0	12.0	-	-	-	800	1000[b]	-	
Sensitivity for $P_{OUT} = 400$ mW	e_{IN}	10	9.0	9.0	-	35[a]	55	-	-	-	mV
Sensitivity for $P_{OUT} = 800$ mW	e_{IN}	10	9.0	12.0	-	-	-	-	50[b]	100	mV
Input Resistance---- Terminal 3 to Ground	R_{IN3}	11	6.0	6.0	-	1000	-	-	1000	-	Ω
Junction-to-Case Thermal Resistance	θ_{J-C}	-	-	-	-	-	60	-	-	60	°C/W

a $R_{CC} = 130\,\Omega$

b $R_{CC} = 200\,\Omega$



a. Collector-to-Emitter Breakdown Voltage (Q_6 and Q_7) Circuit



b. Typical Audio Amplifier Circuit Utilizing the CA3020 or CA3020A As An Audio Preamplifier and Class B Power Amplifier

Fig.2

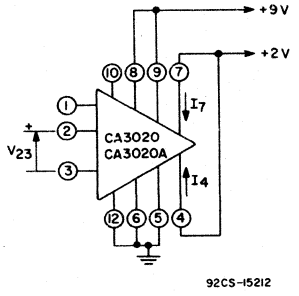
TYPICAL PERFORMANCE DATA*

An External Radiator is Recommended for High Ambient Temperature Operation

CHARACTERISTICS	SYMBOLS	CA3020	CA3020A	UNITS
Power Supply Voltage	V_{CC_1}	9.0	9.0	V
	V_{CC_2}	9.0	12.0	
Zero Signal Current Diff. Ampl.	I_{CC_1}	15	15	mA
Zero Signal Current Output Ampl.	I_{CC_2}	24	24	
Maximum Signal Current Diff. Ampl.	I_{CC_1}	16	16.6	mA
Maximum Signal Current Output Ampl.	I_{CC_2}	125	140	
Maximum Power Output at THD = 10%	P_O	550	1000	mW
Sensitivity	e_{IN}	35	45	mV
Power Gain	G_P	75	75	dB
Input Resistance	R_{IN}	55	55	kΩ
Efficiency	η	45	55	%
Signal-to-Noise Ratio	S/N	70	66	dB
THD at 150 mW level		3.1	3.3	%
Test Signal Frequency from 600Ω Generator		1000	1000	Hz
Equivalent Collector-to-Collector Load Resistance	R_{CC}	130	200	Ω

* Refer to Figs.8 through 12 for Measurement and Symbol Information.

TYPICAL TRANSFER CHARACTERISTICS



a. Test Setup

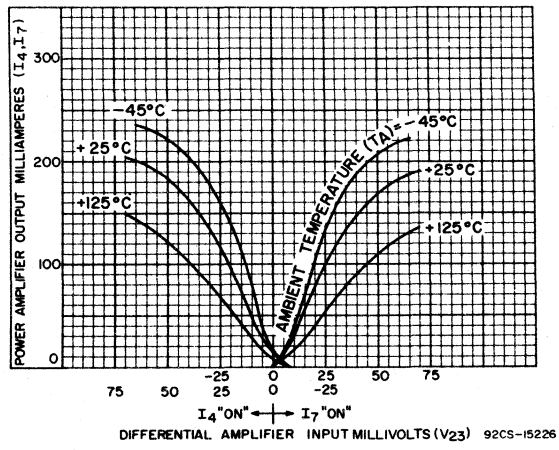
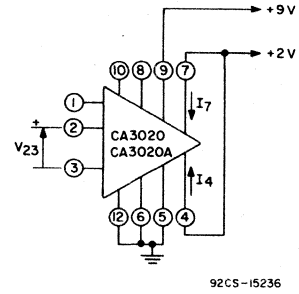


Fig.3 b. Characteristics with R_{10} shorted out



a. Test Setup

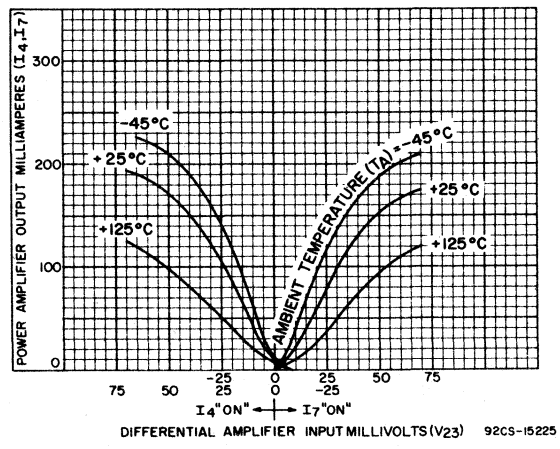
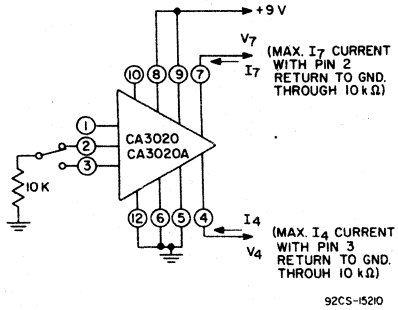


Fig.4 b. Characteristics with R_{10} in circuit

"MINIMUM DRIVE" TYPICAL CURRENT-VOLTAGE SATURATION CURVE



a. Test Setup

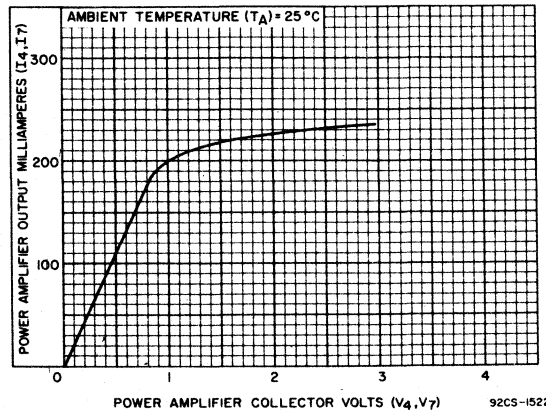
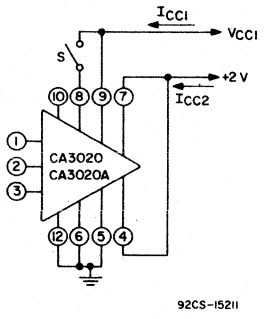
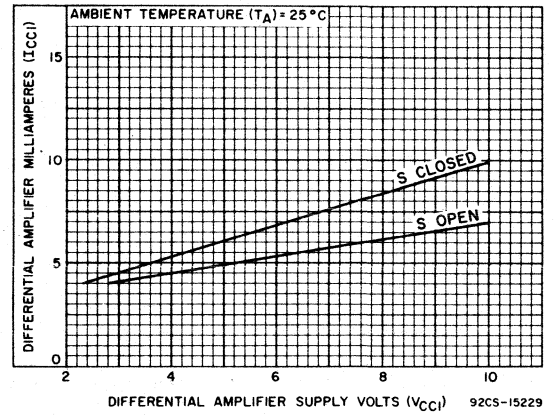


Fig.5 b. Characteristic

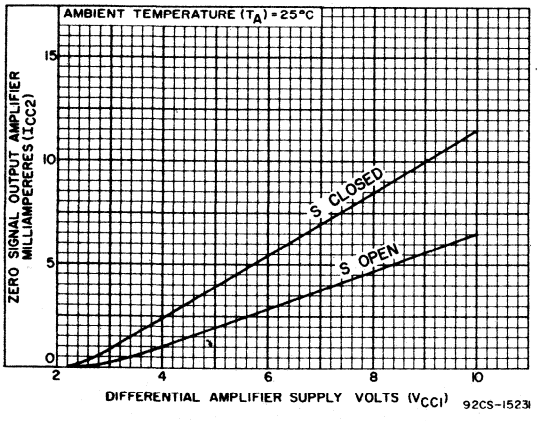
ZERO SIGNAL AMPLIFIER CURRENT vs DIFFERENTIAL AMPLIFIER SUPPLY VOLTAGE



a. Test Setup



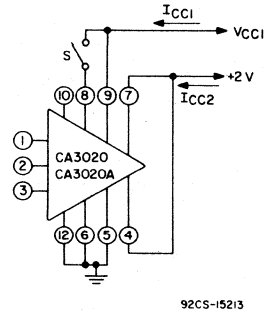
b. Differential Amplifier Characteristics



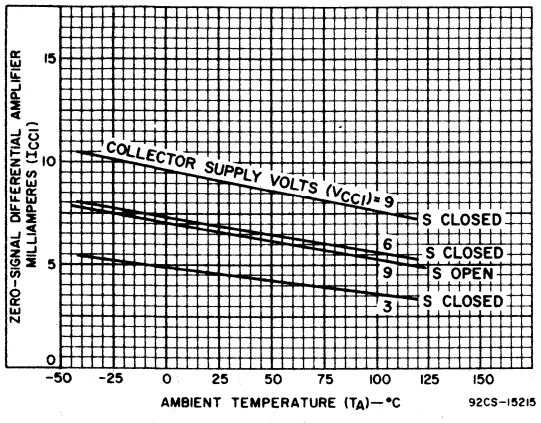
c. Output Amplifier Characteristics

Fig.6

ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE

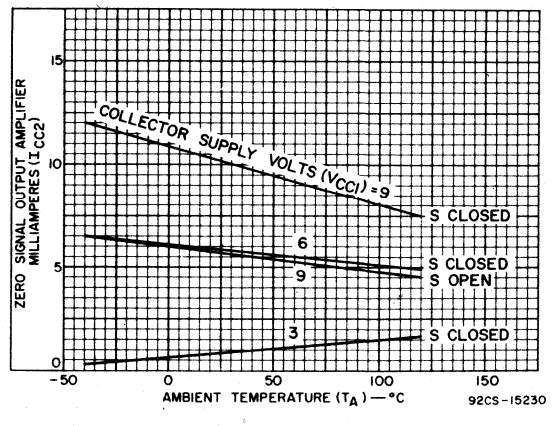


a. Test Setup



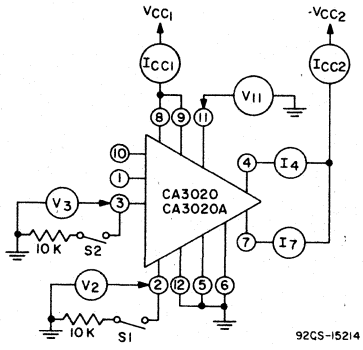
b. Differential Amplifier Characteristics

Fig.7



c. Output Amplifier Characteristics

STATIC CURRENT AND VOLTAGE TEST CIRCUIT



CURRENTS OR VOLTAGES	S1	S2
$I_{4\text{-IDLE}}$	open	open
$I_{7\text{-IDLE}}$	open	open
$I_{4\text{-PEAK}}$	open	close
$I_{7\text{-PEAK}}$	close	open
$I_{4\text{-CUTOFF}}$	close	open
$I_{7\text{-CUTOFF}}$	open	close

CURRENTS OR VOLTAGES	S1	S2
I_{CC1}	open	open
I_{CC2}	open	open
V_2	open	open
V_3	open	open
V_{11}	open	open

Fig.8

MEASUREMENT OF BANDWIDTH AT -3 dB POINTS

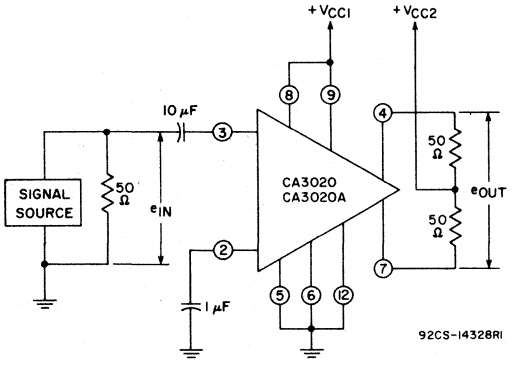
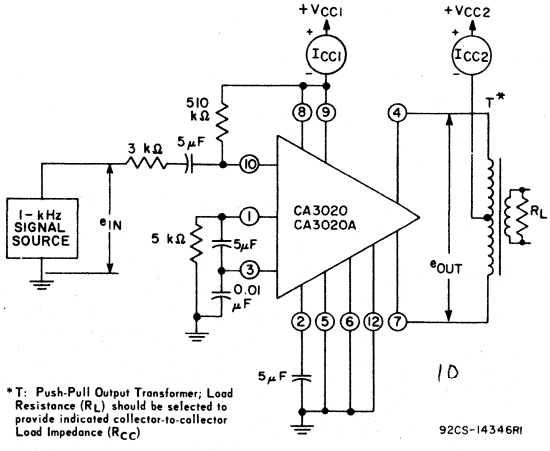


Fig.9

PROCEDURES:

1. Apply desired value of V_{CC_1} and V_{CC_2}
2. Apply 1 kHz input signal and adjust for e_{IN} = 5 mV (rms)
3. Record the resulting value of e_{OUT} in dB (reference value)
4. Vary input-signal frequency, keeping e_{IN} constant at 5 mV, and record frequencies above and below 1 kHz at which e_{OUT} decreases 3 dB below reference value.
5. Record bandwidth as frequency range between -3 dB points.

MEASUREMENTS OF ZERO-SIGNAL DC CURRENT DRAIN, MAXIMUM-SIGNAL DC CURRENT DRAIN, MAXIMUM POWER OUTPUT, CIRCUIT EFFICIENCY, SENSITIVITY, AND TRANSDUCER POWER GAIN



*T: Push-Pull Output Transformer; Load Resistance (R_L) should be selected to provide indicated collector-to-collector Load Impedance (R_{CC})

Fig.10

PROCEDURES:

Zero-Signal DC Current Drain

1. Apply desired Value of V_{CC_1} and V_{CC_2} and reduce e_{IN} to 0V
2. Record resulting values of I_{CC_1} and I_{CC_2} in mA as Zero-Signal DC Current Drain.

Maximum-Signal DC Current Drain, Maximum Power Output, Circuit Efficiency, Sensitivity, and Transducer Power Gain

1. Apply desired value of V_{CC_1} and V_{CC_2} and adjust e_{IN} to the value at which the Total Harmonic Distortion in the output of the amplifier = 10%
2. Record resulting value of I_{CC_1} and I_{CC_2} in mA as Maximum-Signal DC Current Drain
3. Determine resulting amplifier power output in watts and record as Maximum Power Output (P_{OUT})
4. Calculate Circuit Efficiency (η) in % as follows:

$$\eta = 100\,\frac{P_{OUT}}{V_{CC_1}I_{CC_1}+V_{CC_2}I_{CC_2}}$$

where P_{OUT} is in watts, V_{CC_1} and V_{CC_2} are in volts, and I_{CC_1} and I_{CC_2} are in amperes.

5. Record value of e_{IN} in mV^2 (rms) required in Step 1 as Sensitivity (e_{IN})
6. Calculate Transducer Power Gain (G_p) in dB as follows:

$$G_p = 10\log_{10}\frac{P_{OUT}}{P_{IN}}$$

where P_{IN} (in mW) $= \dfrac{e_{IN}^2}{3000 + R_{IN(10)}}$

MEASUREMENT OF INPUT RESISTANCE

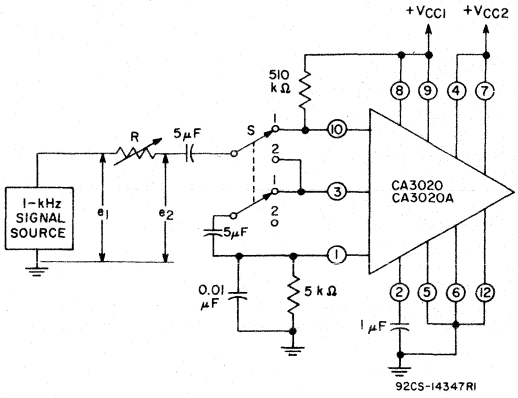


Fig.11

PROCEDURES:

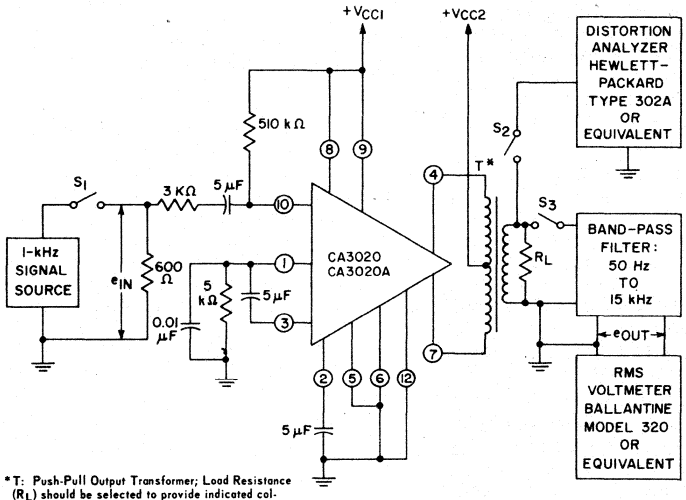
Input Resistance Terminal 10 to Ground ($R_{IN_{10}}$)

1. Apply desired value of V_{CC_1} and V_{CC_2} and set S in Position 1
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as $R_{IN_{10}}$

Input Resistance Terminal 3 to Ground (R_{IN_3})

1. Apply desired value of V_{CC_1} and V_{CC_2} set S in Position 2
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as R_{IN_3}

MEASUREMENT OF SIGNAL-TO-NOISE RATIO AND TOTAL HARMONIC DISTORTION



*T: Push-Pull Output Transformer; Load Resistance (R_L) should be selected to provide indicated collector-to-collector Load Impedance (R_{CC})

PROCEDURES:

Signal-to-Noise Ratio

1. Close S_1 and S_3; open S_2
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for an amplifier output of 150mW and record resulting value of E_{OUT} in dB as e_{OUT_1} (reference value)
4. Open S_1 and record resulting value of e_{OUT} in dB as e_{OUT_2}
5. Signal-to-Noise Ratio (S/N) = $20\log_{10}\frac{e_{OUT_1}}{e_{OUT_2}}$.

Total Harmonic Distortion

1. Close S_1 and S_2; open S_3
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for desired level amplifier output power
4. Record Total Harmonic Distortion (THD) in %

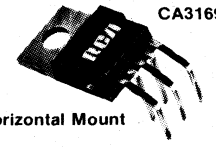
Fig.12

CA3169

CA3169

Vertical Mount H-1893

CA3169M



Horizontal Mount

VERSA-VI TO-220-Style Plastic Packages H-1894

Solenoid and Motor Driver (1/2 H Driver)

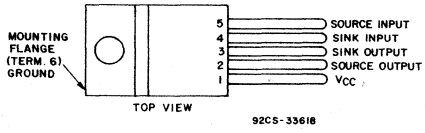
Features:
- *Chip encapsulated in a 5-lead plastic TO-220-style package (VERSA-VI)*
- *Output short-circuit protection*
- *Thermal overload protection*
- *Solenoid inductive "kick" protection with internal-clamp diodes*
- *Output sink and source capacity of 600-mA minimum overtemperature*
- *Horizontal and vertical mounting packages available*
- *Separate sink circuit and source circuit, each individually controlled*
- *Inputs can be driven by TTL logic levels and CMOS logic levels*
- *Low $V_{CE}(sat)$*

Applications:
- *Latching solenoid driver (single and multiple)*
- *Non-latching solenoid driver*
- *Relay driver*
- *Lamp controller*
- *Lamp driver*
- *Motor controller (forward and reverse)*
- *Stepper motor controller*
- *On-off logic controllers (TTL logic)*
- *Intermediate power driver*
- *Triac, SCR, and transistor drivers*

The RCA-CA3169 is a monolithic integrated circuit capable of driving lamps and other devices that can be changed between two states (on or off). Transistors, SCR's, and triacs are some of the solid-state devices that can be controlled by the CA3169. This device can also control relays, solenoids (latching or non-latching), motors (DC - forward and reverse) and DC stepping motors.

The CA3169 contains a separate source-driver circuit with internal current-limiting protection and a separate sink-driver circuit. The sink driver contains an energy-absorbing diode to protect the device against any inductive "kick" during state changes. The CA3169 is protected against overvoltage conditions on the output drivers and overtemperature conditions (thermal-shutdown protection).

The input operating levels are TTL compatible. The source and sink outputs are in their off condition (non-conducting) when their respective inputs are in a HI state, or open-circuited. The outputs are in their on state (conducting) when their respective inputs are LO. The VERSA-VI package is available with two lead configurations. The CA3169 has a vertical-mount lead form, and the CA3169M has a horizontal-mount lead form.



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY VOLTAGE (Pin 1 to GND) ..... Positive . . .41 V DC
Negative . . .1.4 V DC
SINK CURRENT ..... 1.9 A
SOURCE CURRENT ..... Controlled by Internal Current Limiting
INPUT VOLTAGE:
SINK INPUT (Pin 4 to GND) ..... 17 V
SOURCE INPUT (Pin 5 to GND) ..... 17 V
MAXIMUM FORWARD CURRENT—Diode D1 ..... 2.5 A
MAXIMUM FORWARD CURRENT—Diode D2 ..... 3 A
POWER DISSIPATION, P_D at T_A=90°C ..... 15 W
THERMAL RESISTANCE, JUNCTION TO CASE ..... 4°C/W
JUNCTION TEMPERATURE ..... 150°C
OPERATING TEMPERATURE ..... -40° to +85°C
STORAGE TEMPERATURE ..... -55° to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)
from case for 10 s max. ..... 265°C

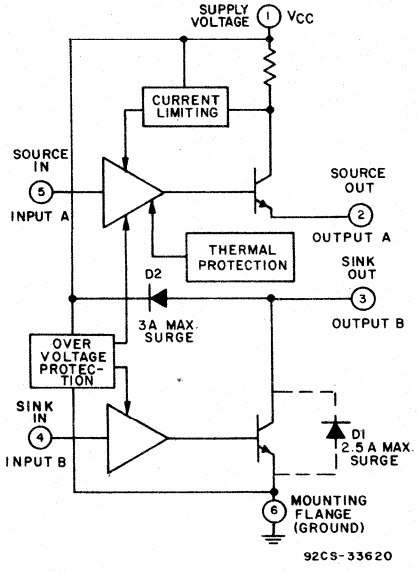
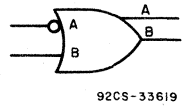


Fig. 1 - 1/2 H driver function diagram.

TRUTH TABLE FOR SOLENOID DRIVER
TTL Logic Conditions: $0 \leq V_L \leq 0.8$, $1.9 \leq V_H \leq 5.5$

INPUT A SOURCE IN	INPUT B SINK IN	OUTPUT A SOURCE OUT	OUTPUT B SINK OUT
V_L	V_L	HIGH (ON)	LOW (ON)
V_L	V_H	HIGH (ON)	(OFF)
V_H	V_L	(OFF)	LOW (ON)
V_H	V_H	(OFF)	(OFF)



CA3169

ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=10.5 V to 18 V
Unless otherwise specified

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Output Leakage Current, Pin 2 See Fig. 6	Inputs Open V_{CC}=4 V to 18 V Source and Sink Loads=20 Ω	-110	±0.5	110	μA
Output Leakage Current, Pin 3 See Fig. 6	Inputs Open V_{CC}=4 V to 18 V Source and Sink Loads=20 Ω	-110	±0.5	110	μA
Thermal Resistance, Junction to Case θ_{JC}		—	3	4	°C/W
Quiescent Current, Pin 1 See Fig. 5	Device "ON" Input Terminals Shorted, V_{CC}=14 V	—	70	100	mA
Quiescent Current, Pin 1 See Fig. 4	Device "OFF" Input Terminals Open, V_{CC}=14 V	—	17	40	mA
Thermal Shutdown Temperature	R_L=Short Circuit	128	140	162	°C
Overvoltage Shutdown-Circuit Upper Trip Point, Pin 1 Voltage See Fig. 8	R_L=20 Ω	20	25	27	V
Overvoltage Shutdown-Circuit Lower Trip Point, Pin 1 Voltage See Fig. 8	R_L=20 Ω	18	21.4	23	V
Input Logic Levels; Source Input - Pin 5, Sink Input - Pin 4					
Input Low Threshold Sink or Source V_{IL}	V_{CC}=14 V **See Note 1**	—	0.4	0.8	V
Input High Threshold Sink or Source V_{IH}	V_{CC}=14 V **See Note 2**	1.9	2.4	—	V
Input Low Current Sink or Source I_{LL}	$V_{IN} \leq$ 0.4 V	−0.9	−0.3	—	mA
Input High Current Sink or Source I_{IH}	$V_{IN} \leq$ 5.5 V	−110	−23	110	μA

NOTE 1: I_{SOURCE} or $I_{SINK} \leq$ 600 mA, $V_{OS} \leq$ 1.5 V, $V_{SINK} \leq$ 0.75 V.
NOTE 2: I_{SOURCE} or $I_{SINK} \leq$ 100 μA, V_{SOURCE} = GND, for V_{SINK} 20 Ω to V_{CC}.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Source Outputs					
Output Voltage, V_{OS} Pin 2 **See Note 3** See Fig. 7	Referenced to V_{CC} with I_{SOURCE}= 600 mA	—	1	1.6	V
Short-Circuit Current Limit, Pin 2 to Ground		0.65	1.11	2.6	A
Turn-On Delay to Output-On, Pin 2	C_L=100 pF, R_L=33 Ω	—	0.45	5.6	μs
Turn-Off Delay to Output-Off Pin 2	C_L=100 pF, R_L=33 Ω	—	5	55	μs
Sink Outputs					
Output Saturation Voltage V_3 **See Note 3** See Fig. 10	I_{SINK}=600 mA, $V_{IN} \leq$ 0.4 V	—	0.3	0.85	V
Output Saturation Voltage V_3 **See Note 3** See Fig. 10	I_{SINK}=1000 mA $V_{IN} \leq$ 0.4 V	—	0.8	1.65	V
Turn-On Delay to Output-On Pin 3 (T_{ON})	C_L=100 pF, R_L=33 Ω to V_{CC}	—	0.45	5.6	μs
Turn-Off Delay to Output-Off Pin 3 (T_{OFF})	C_L=100 pF, R_L=33 Ω to V_{CC}	—	0.95	25	μs

NOTE 3: Measured over temperature range of −40°C to 85°C.

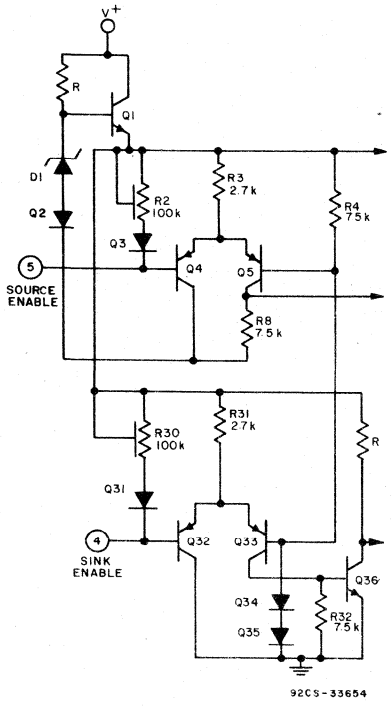


Fig. 2 - Detailed schematic of the input circuit for CA3169.

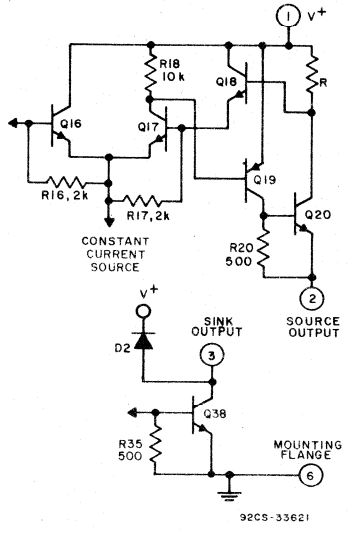


Fig. 3 - Detailed schematic of the output circuit for CA3169.

TEST CIRCUITS
(V_{CC} = V_{IN} = PIN 1 VOLTAGE)

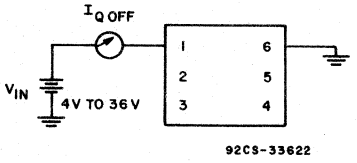


Fig. 4 - Quiescent current device "OFF".

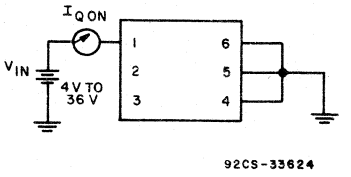


Fig. 5 - Quiescent current device "ON".

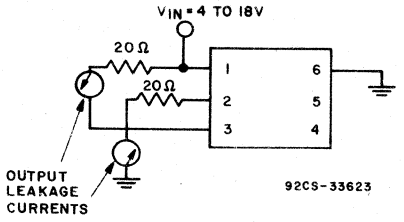


Fig. 6 - Output leakage currents.

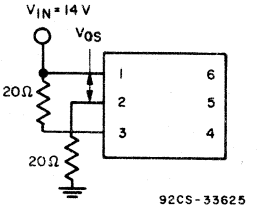
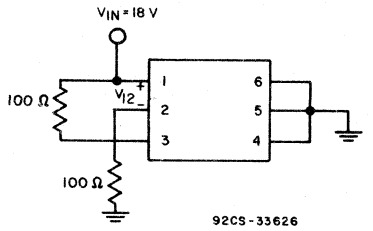


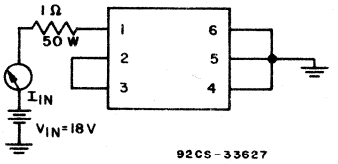
Fig. 7 - Output source voltage (referenced to V_{CC}).



PROCEDURE

1. Measure V_{12}.
2. Increase V_{CC} until $V_{12} \geq 2$ V.
3. Measure V_{CC}; this voltage is the high trip point. Pin 2 should be off; i.e., pin 3 should be high.
4. Observe and measure the voltage at pin 3.
5. Decrease V_{CC} until pin 3 switches, i.e., ≤ 18 V. The supply voltage will be the low trip point voltage.

Fig. 8 - Overvoltage protection.



When V_{CC} is turned on, I_{IN} should be equal to or greater than 1 A. Thermal shutdown will operate properly if the input current drops below 0.5 A (0.3 A typ.) in 10 to 15 seconds. Cover the unit during this test in the event that the thermal shutdown is not operating properly.

Fig. 9 - Thermal shutdown.

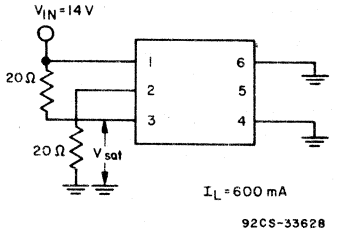
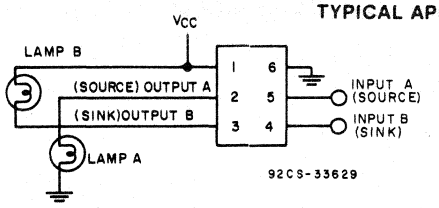


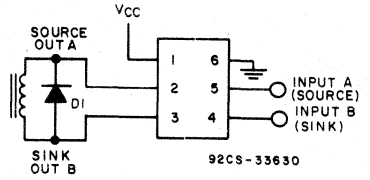
Fig. 10 - Output saturation voltage.

TYPICAL APPLICATIONS



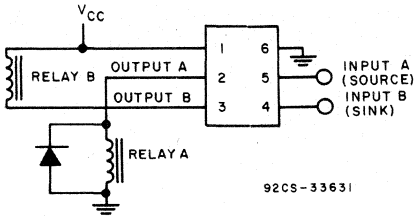
When input A goes low, lamp A will light.
When input B goes low, lamp B will light.

Fig. 11 - Lamp driver.



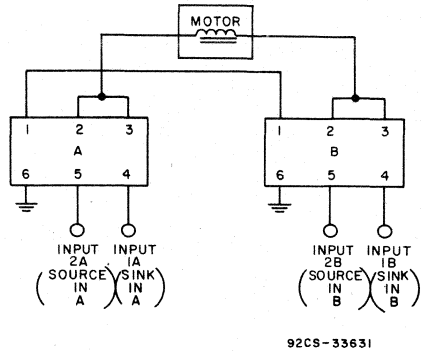
Input A and input B must both be low for the solenoid to switch.

Fig. 12 - Non-latching solenoid.



Relay A will close when input A goes low. Relay B will close when input B goes low. Both relays will close when both inputs go low.

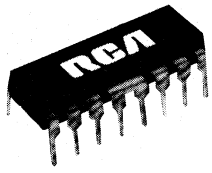
Fig. 13 - Relay driver.



When opposing inputs go low, the motor will switch direction; if source input A and sink input B both go low, current will flow from A to B. If source input B and sink input A both go low, current will flow from B to A.

Fig. 14 - Motor driver or latching solenoid driver.

CA3219E



H-1918

16-Lead Dual-In-Line Webbed Plastic Package ("E" Suffix)

Quad-Power NAND Driver

For Interfacing Low-Level Logic to High Current Loads

Features:

- *Driven outputs capable of switching 600 mA load currents without spurious changes in output state*
- *Inputs compatible with TTL or 5-volt CMOS logic*
- *Suitable for resistive or inductive loads*

The RCA CA3219E• quad power NAND driver contains four NAND gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters, incandescent displays, and vacuum fluorescent displays.

Diodes in the outputs protect the IC against voltage transients due to switching inductive loads.

To allow for maximum heat transfer from the chip, the two center leads are directly connected to the die substrate and to the ground bond pads. In free air, junction-to-air thermal resistance (θJ-A) is 50°C/W* (typical).

The CA3219E is supplied in the 16-lead dual-in-line plastic package with webbed-lead construction.

* This coefficient can be lowered to 40°C/W (typical) by suitable design of the PC board to which the CA3219E is soldered.

•Formerly RCA Dev. Type No. TA10982.

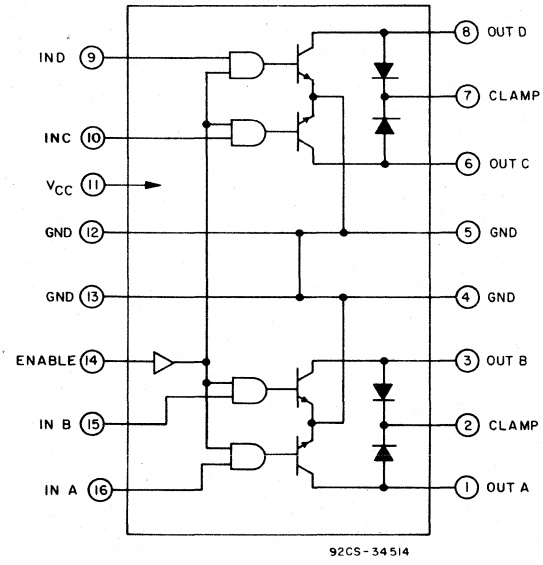


Fig. 1 - Block diagram for the CA3219E.

TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C:*

Logic Supply Voltage (V_{CC}) ..... 7 V
Logic Input Voltage (V_{IN}) ..... 15 V
Output Voltage (V_{CEX}) ..... 50 V_{DC}
Output Sustaining Voltage (V_{CC})sus ..... 35 V_{DC}
Output Current (I_O) ..... 1 ADC
Power Dissipation (P_D)
  Up to 55° C ..... 1.5 W
  Above 55° C ..... derate linearly at 16.6 mW/° C
  Up to 90° C with heat sink ..... derate linearly at 25 mW/° C
Ambient Temperature Range:
  Operating ..... -40 to +85° C
  Storage ..... -55 to +150° C
Maximum Junction Temperature ($T_{\theta J}$) ..... +150° C
Maximum Thermal Resistance
  Junction-to-Air (θ_{J-A}) ..... 60° C/W
  Junction-to-Case (θ_{J-C})
    to pins 4, 5, 12, 13 at seat ..... 12° C/W

ELECTRICAL CHARACTERISTICS at T_A = 25° C, V_{CC} = 5 V

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Output Leakage Current (I_{CEX}) V_{CE} = 50 V V_{IN} = 0.8 V	—	100	μA
Output Sustaining Voltage $V_{CE(sus)}$ I_C = 100 mA V_{IN} = 0.8 V	25	—	V
Collector Emitter Saturation Voltage $V_{CE(sat)}$			
I_C = 100 mA V_{IN} = 2.4 V	—	0.3	V
I_C = 400 mA V_{IN} = 2.4 V	—	0.5	V
I_C = 600 mA V_{IN} = 2.4 V	—	0.7	V
Input Low Voltage V_{IL}	—	0.8	V
Input Low Current I_{IL} V_{IN} = 0.8 V	—	+10	μA
Input High Voltage V_{IH} I_C = 600 mA	2	—	V
Input High Current I_{IH} I_C = 700 mA; V_{IN} = 5.5 V	—	40	μA
Supply Current — All Outputs ON, $I_{CC(ON)}$ I_C = 700 mA; V_{CC} = V_{IH} = 5.5 V	—	80	mA
Supply Current — All Outputs OFF, $I_{CC(OFF)}$	—	5	mA
Clamp Diode Leakage Current I_R V_R = 50 V	—	100	μA
Clamp Diode Forward Voltage V_F			
IF = 1 A	—	1.5	V
IF = 1.5 A	—	2	V
Turn-On Delay t_{PHL} Turn-Off Delay t_{PLH}		30	μs

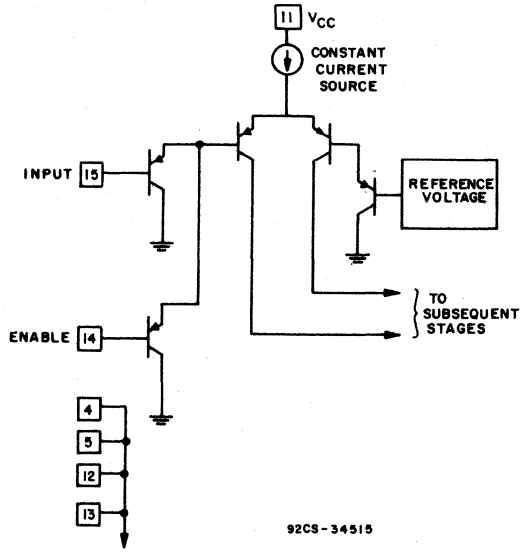
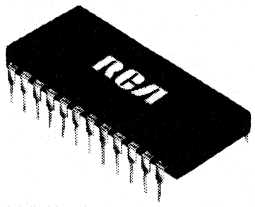


Fig. 2 - Schematic of one input section.



H-1855

24-Lead Dual-In-Line Plastic Package

Speed-Control System

Features

- *Low power dissipation*
- *I^2L control logic*
- *Power-ON reset*
- *On-chip oscillator for system time reference*
- *Single line command*
- *Amplitude encoded control signals*
- *Transient compensated input commands*
- *Controlled acceleration mode*
- *Internal redundant brake and low speed disable*
- *Braking disable*

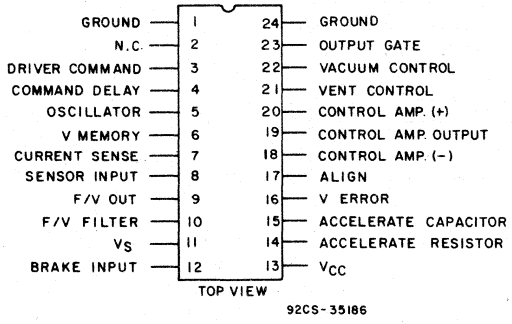
The RCA-CA3228 is a monolithic I^2L integrated circuit designed as an automotive speed-control system.

The system monitors vehicle speed and compares it to a set reference speed. Any deviation in vehicle speed causes a servo mechanism to open or close the engine throttle as required to eliminate the speed error. The reference speed is set by the driver to hold the existing speed and stored in a 9-bit counter.

The reference speed can be altered by the ACCEL and COAST driver commands. The ACCEL command causes the vehicle to accelerate at a controlled rate while the COAST command causes the servo to relax completely forcing the vehicle to slow down. Application of the brake causes the servo to relax immediately and places the system into the standby mode while the RESUME command returns the vehicle to the last stored speed.

Vehicle speed and driver commands are input into the integrated circuit via external sensors. Actuators are needed to convert the output signals into the mechanical action necessary to control vehicle speed.

The CA3228 is supplied in a 24-lead plastic package (E suffix).



TERMINAL ASSIGNMENT

CA3228

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25°C*

DC SUPPLY VOLTAGE RANGE (V_{DD}) ..... 7.4 to 9 V
DC SUPPLY CURRENT RANGE (I_{DD}) ..... 7.5 to 25 mA
POWER DISSIPATION PER PACKAGE:
For T_A=−40°C to 55°C ..... 125 mW
For T_A=55°C to 70°C ..... Derate linearly at 3.3 mW/°C
TEMPERATURE RANGE:
OPERATING ..... −40 to +85°C
STORAGE ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

SWITCHING CHARACTERISTICS, *T_A=25°C, V_{DD}=7.4 to 9 V*

ACCEL Input Hold Time ..... 50 ms
COAST Input Hold Time ..... 50 ms
RESUME Input Hold Time ..... 330 ms
ON Input Hold Time ..... 50 ms
OFF Input Hold Time ..... 50 ms
INTERNAL OSCILLATOR FREQUENCY:
C=0.005 μF at Pin 5 ..... 10,000 Hz
Speed Input Frequency ..... 32 to 222 Hz

SYSTEM PERFORMANCE, *T_A=25°C, V_{DD}=8.2 V, f_M=10 kHz, f_S=2.22 Hz/mph*

SPEED RESOLUTION ..... 0.45 mph
MINIMUM OPERATING SPEED ..... 25 mph
MAXIMUM STORED SPEED ..... 100 mph
REDUNDANT BRAKE SPEED ..... 11 mph

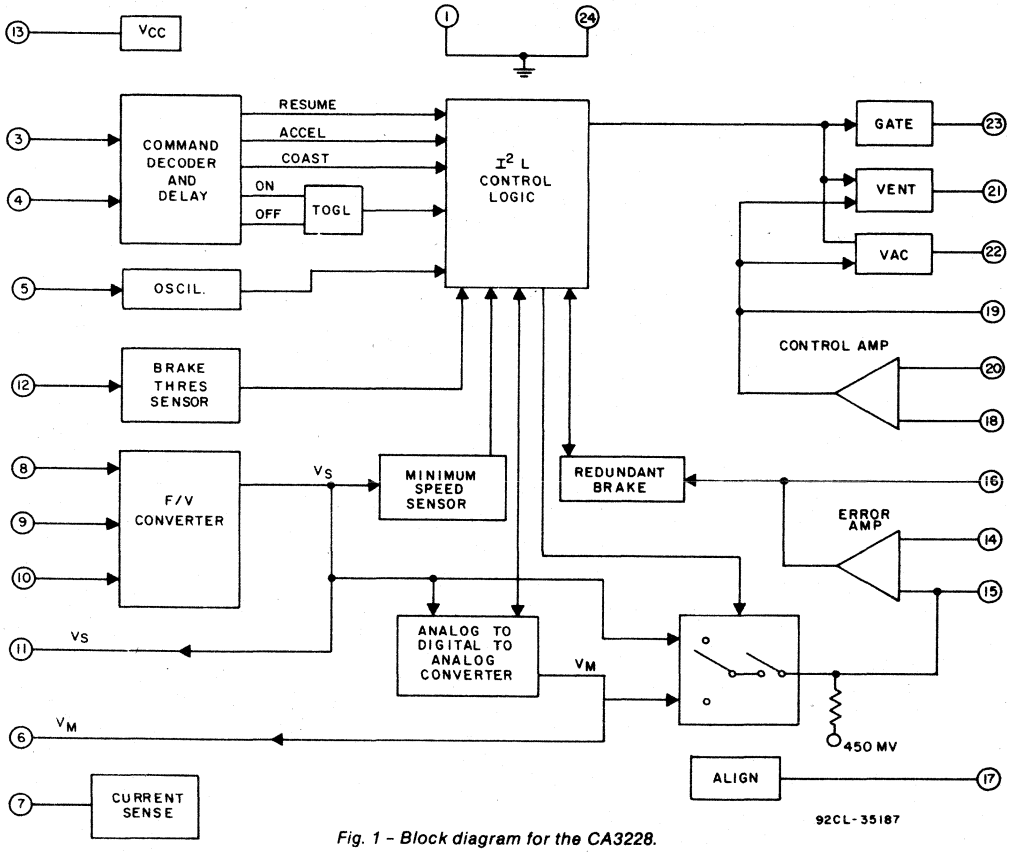


Fig. 1 - Block diagram for the CA3228.

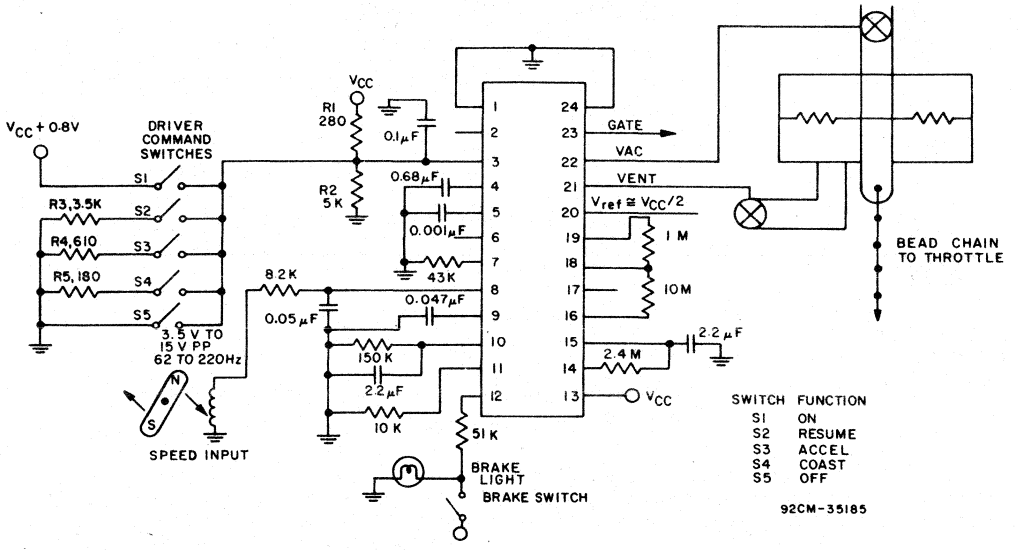


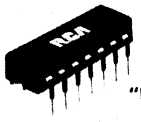
Fig. 2 - Typical automotive speed-control application.

CA723, CA723C Types

"T" Suffix

10-Lead TO-5

H-1384



"E" Suffix

14-Lead Dual-In-Line Plastic Package

H-1517

Voltage Regulators

For Regulated Output Voltages Adjustable from 2 V to 37 V at Output Currents up to 150 mA Without External Pass Transistors

Features:

- *Up to 150 mA output current*
- *Positive and negative voltage regulation*
- *Regulation in excess of 10A with suitable pass transistors*
- *Input and output short-circuit protection*
- *Load and line regulation: 0.03%*
- *Direct replacement for 723 and 723C industry types*
- *Adjustable output voltage: 2 to 37 V*

Applications:

- *Series and shunt voltage regulator*
- *Floating regulator*
- *Switching voltage regulator*
- *High-current voltage regulator*
- *Temperature controller*

RCA-CA723 and CA723C are silicon monolithic integrated circuits designed for service as voltage regulators at output voltages ranging from 2 to 37 volts at currents up to 150 milliamperes.

Each type includes a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and a current-limiting circuit. They also provide independently accessible inputs for adjustable current limiting and remote shutdown and, in addition, feature low standby current drain, low temperature drift, and high ripple rejection.

The CA723 and CA723C may be used with positive and negative power supplies in a wide variety of series, shunt, switching, and floating regulator applications. They can provide regulation at load currents greater than 150 milliamperes and in excess of 10 amperes with the use of suitable n-p-n or p-n-p external pass transistors.

The CA723 and CA723C are supplied in the 10-lead TO-5-style package (T suffix), and the 14-lead dual-in-line plastic package (E suffix), and are direct replacements for industry types 723, 723C, μA723, and μA723C in packages with similar terminal arrangements. They are also available in chip form ("H" suffix).

All types are rated for operation over the full military-temperature range of −55°C to +125°C.

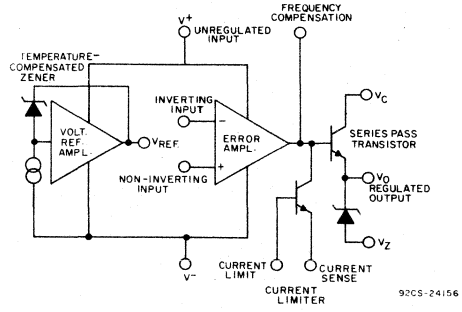


Fig. 1 — Functional diagram of the CA723 and CA723C.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (Between V^+ and V^- Terminals)	40	V
PULSE VOLTAGE FOR 50-ms PULSE WIDTH (Between V^+ and V^- Terminals)	50	V
DIFFERENTIAL INPUT–OUTPUT VOLTAGE	40	V
DIFFERENTIAL INPUT VOLTAGE: Between Inverting and Non-Inverting Inputs	±5	V
Between Non-Inverting Input and V^-	8	V
CURRENT FROM ZENER DIODE TERMINAL (V_Z)	25	mA
CURRENT FROM VOLTAGE REFERENCE TERMINAL (V_{REF})	15	mA

DEVICE DISSIPATION:		
Up to T_A = 25°C –		
CA723T, CA723CT	800	mW
CA723E, CA723CE	1000	mW
Above T_A = 25°C –		
CA723T, CA723CT Derate linearly	6.3	mW/°C
CA723E, CA723CE Derate linearly	8.3	mW/°C
AMBIENT TEMPERATURE RANGE (All Types):		
Operating	–55 to +125	°C
Storage	–65 to +150	°C
LEAD TEMPERATURE (During Soldering): At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

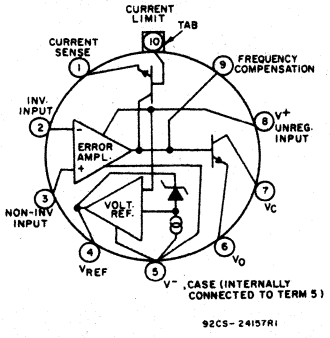


Fig. 2 – Terminal arrangement of the CA723T and CA723CT in the TO-5 style package.

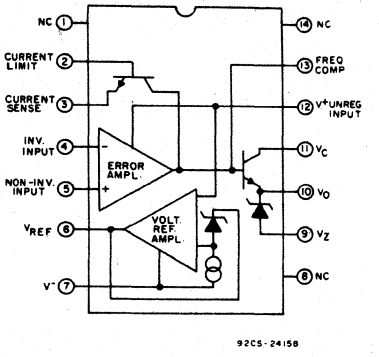


Fig. 3 – Terminal arrangement of the CA723E and CA723CE in the dual-in-line plastic package.

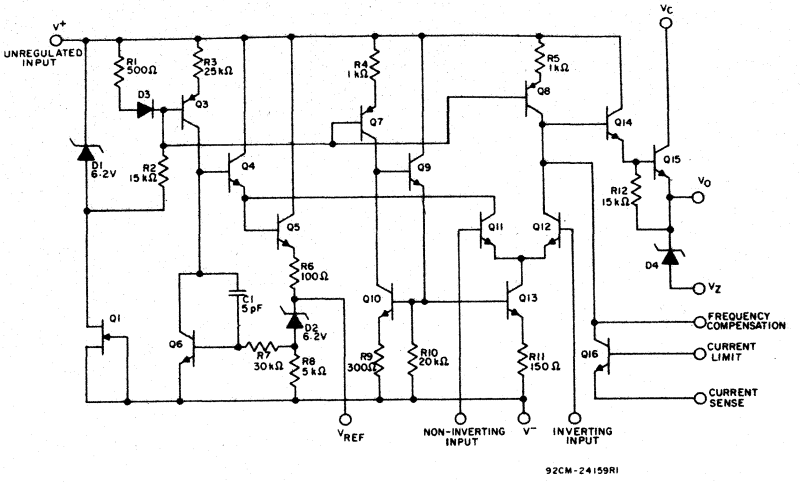


Fig. 4 – Equivalent schematic diagram of the CA723 and CA723C.

CA723, CA723C Types

ELECTRICAL CHARACTERISTICS at T_A = 25 C, $V^+ = V_C = V_I$ = 12 V, V^- = 0, V_O = 5 V, I_L = 1 mA, C_1 = 100 pF, C_{REF} = 0, R_{SCP} = 0, unless otherwise specified. Divider impedance $\frac{R_1R_2}{R_1+R_2}$ at non-inverting input, Term. 5, = 10 kΩ (see Fig. 23).

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA723			CA723C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Quiescent Regulator Current, I_Q	I_L = 0, V_I = 30 V	–	2.3	3.5	–	2.3	4	mA
Input Voltage Range, V_I		9.5	–	40	9.5	–	40	V
Output Voltage Range, V_O		2	–	37	2	–	37	V
Differential Input-Output Voltage, V_I-V_O		3	–	38	3	–	38	V
Reference Voltage, V_{REF}		6.95	7.15	7.35	6.8	7.15	7.5	V
Line Regulation (See Note 1)	V_I = 12 to 40 V	–	0.02	0.2	–	0.1	0.5	%V_O
	V_I = 12 to 15 V	–	0.01	0.1	–	0.01	0.1	
	V_I = 12 to 15 V, T_A = −55 to +125°C	–	–	0.3	–	–	–	
	V_I = 12 to 15 V, T_A = 0 to 70°C	–	–	–	–	–	0.3	
Load Regulation (See Note 1)	I_L = 1 to 50 mA	–	0.03	0.15	–	0.03	0.2	%V_O
	I_L = 1 to 50 mA, T_A = −55 to +125°C	–	–	0.6	–	–	–	
	I_L = 1 to 50 mA, T_A = 0 to 70°C	–	–	–	–	–	0.6	
Output-Voltage Temp. Coefficient, ΔV_O	T_A = −55 to +125°C	–	0.002	0.015	–	–	–	%/°C
	T_A = 0 to 70°C	–	–	–	–	0.003	0.015	
Ripple Rejection (See Note 2)	f = 50 Hz to 10 kHz	–	74	–	–	74	–	dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF	–	86	–	–	86	–	

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA723			CA723C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Short-Circuit Limiting Current, I_{LIM}	R_{SCP} = 10 Ω, V_O = 0	–	65	–	–	65	–	mA
Equivalent Noise RMS Output Voltage, V_N (See Note 2)	BW = 100 Hz to 10 kHz, C_{REF} = 0	–	20	–	–	20	–	μV
	BW = 100 Hz 10 kHz, C_{REF} = 5 μF	–	2.5	–	–	2.5	–	

Note 1: Line and load regulation specifications are given for condition of a constant chip temperature. For high-dissipation conditions, temperature drifts must be separately taken into account.

Note 2: For C_{REF}, see Fig. 23.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723

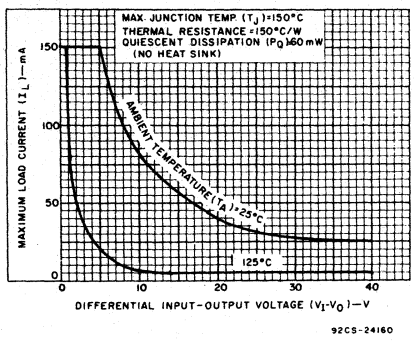


Fig. 5 – Max. load current vs differential input-output voltage.

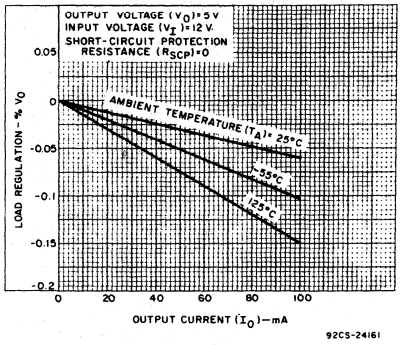


Fig. 6 – Load regulation without current limiting.

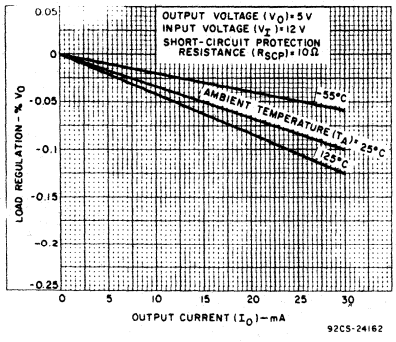


Fig. 7 – Load regulation with current limiting.

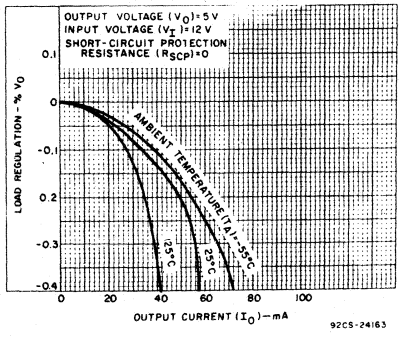


Fig. 8 – Load regulation with current limiting.

CA723, CA723C Types

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723 (Cont'd)

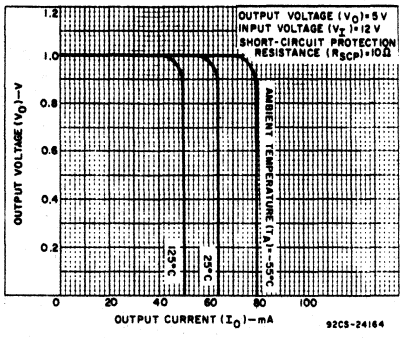


Fig. 9 – Current limiting characteristics.

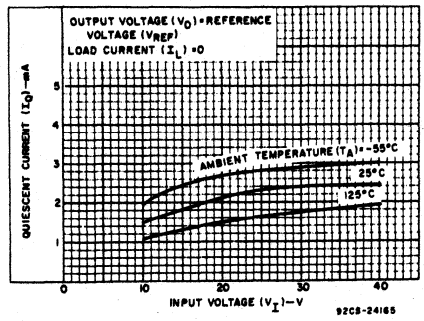


Fig. 10 – Quiescent current vs. input voltage.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723C

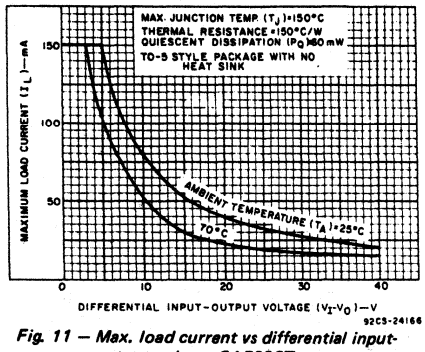


Fig. 11 – Max. load current vs differential input-output voltage CA723CT.

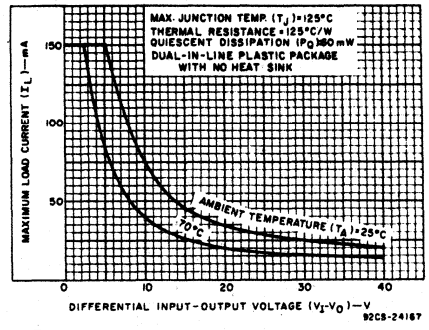


Fig. 12 – Max. load current vs differential input-output voltage for CA723CE.

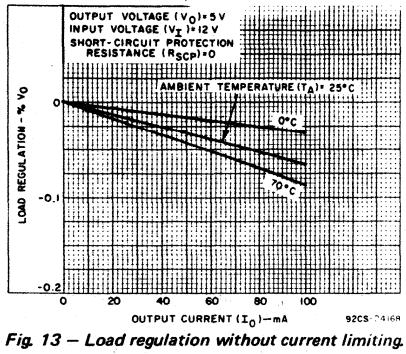


Fig. 13 – Load regulation without current limiting.

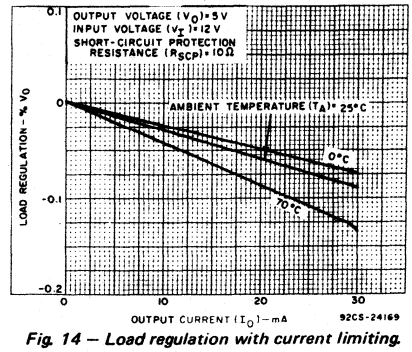


Fig. 14 – Load regulation with current limiting.

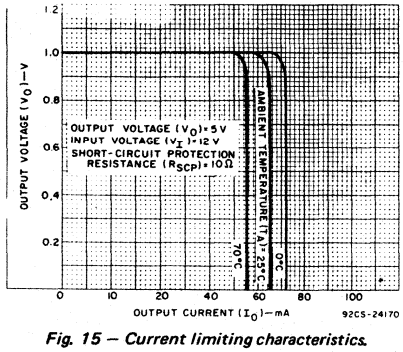


Fig. 15 – Current limiting characteristics.

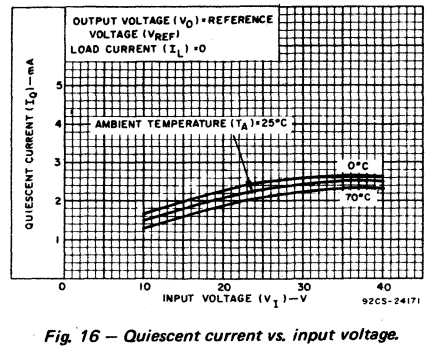


Fig. 16 – Quiescent current vs. input voltage.

TYPICAL CHARACTERISTICS CURVES FOR TYPES CA723 AND CA723C

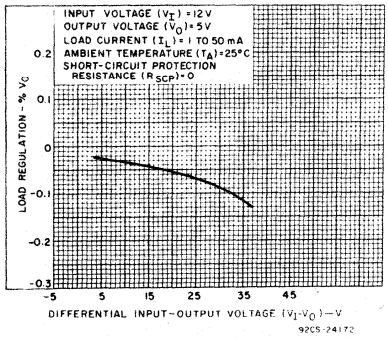


Fig. 17 – Load regulation vs. differential input-output voltage.

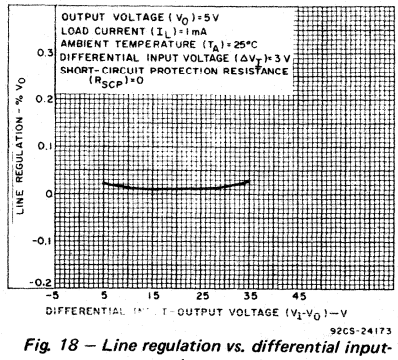


Fig. 18 – Line regulation vs. differential input-output voltage.

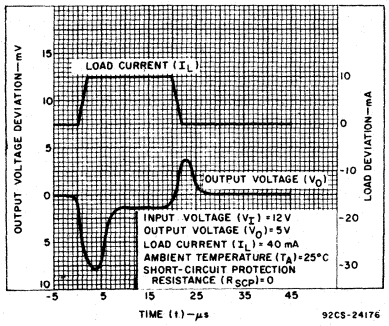


Fig. 19 – Line transient response.

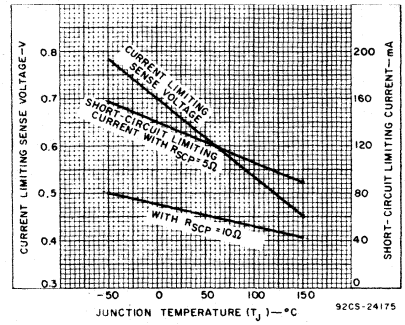


Fig. 20 – Current limiting characteristics vs. junction temperature.

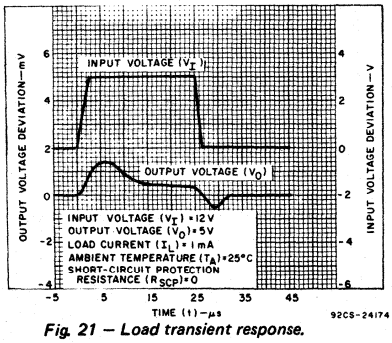


Fig. 21 – Load transient response.

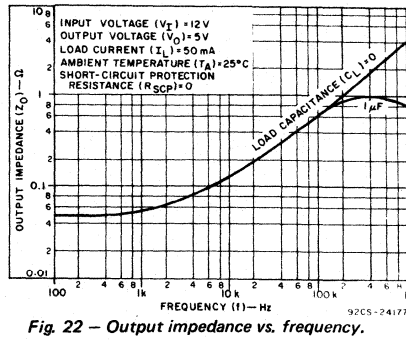


Fig. 22 – Output impedance vs. frequency.

TYPICAL APPLICATION CIRCUITS

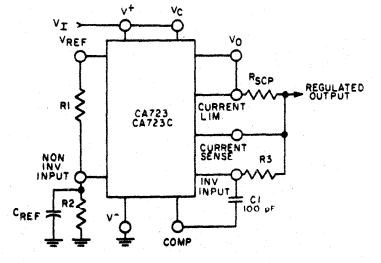


Fig. 23 – Low-voltage regulator circuit (V_O = 2 to 7 volts).

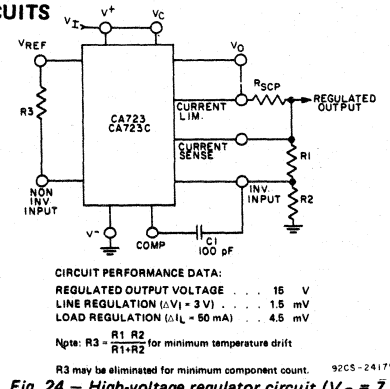
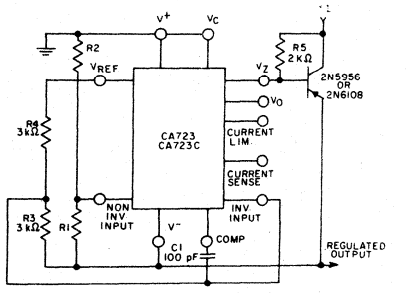


Fig. 24 – High-voltage regulator circuit (V_O = 7 to 37 volts).

TYPICAL APPLICATION CIRCUITS (Cont'd)



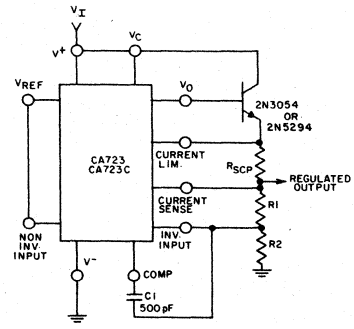
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	−15 V
LINE REGULATION (ΔV_I = 3 V)	1 mV
LOAD REGULATION (ΔI_L = 100 mA)	2 mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

92CS-24180R1

Fig. 25 – Negative-voltage regulator circuit.

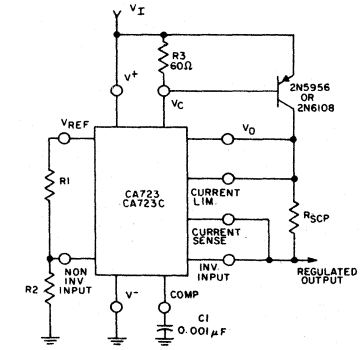


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	15 V
LINE REGULATION (ΔV_I = 3 V)	1.5 mV
LOAD REGULATION (ΔI_L = 1 A)	15 mV

92CS-24181R1

Fig. 26 – Positive-voltage-regulator circuit (with external n-p-n pass transistor).

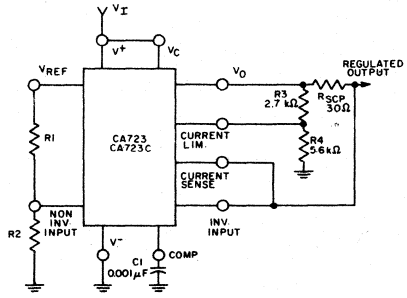


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 1 A)	5 mV

92CS-24182R1

Fig. 27 – Positive voltage-regulator circuit (with external p-n-p pass transistor).

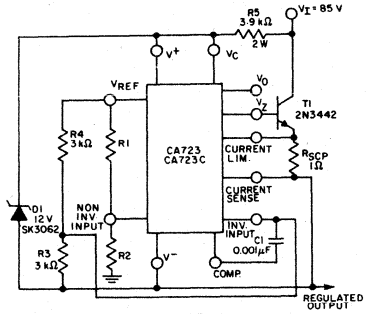


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 10 mA)	1 mV
SHORT-CIRCUIT CURRENT	20 mA

92CS-24183

Fig. 28 – Foldback current-limiting circuit.



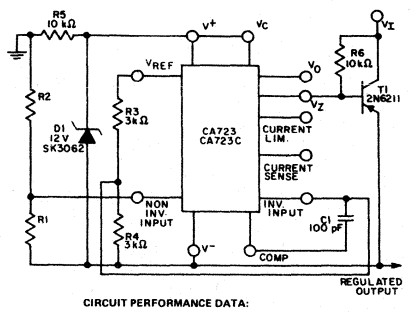
Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	50 V
LINE REGULATION (ΔV_I = 20 V)	15 mV
LOAD REGULATION (ΔI_L = 50 mA)	20 mV

92CS-24184

Fig. 29 – Positive-floating regulator circuit.



CIRCUIT PERFORMANCE DATA:

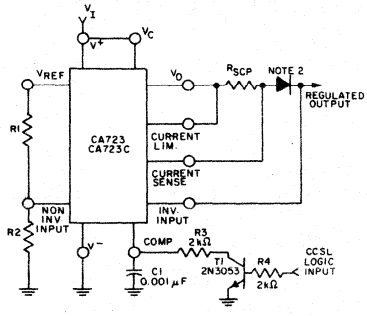
REGULATED OUTPUT VOLTAGE	−100 V
LINE REGULATION (ΔV_I = 20 V)	30 mV
LOAD REGULATION (ΔI_L = 100 mA)	20 mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

92CS-24185

Fig. 30 – Negative-floating regulator circuit.

TYPICAL APPLICATION CIRCUITS (Cont'd)



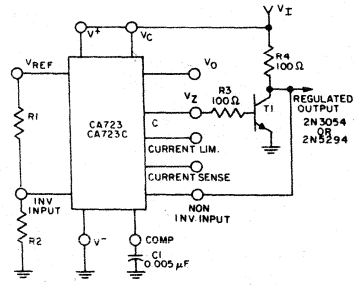
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 50 mA)	1.5 mV

Note 1: A current limiting transistor may be used for shutdown if current limiting is not required.
Note 2: Add a diode if V_O > 10 V.

92CS-24186R1

Fig. 31 – Remote shutdown regulator circuit with current limiting.



CIRCUIT PERFORMANCE DATA:

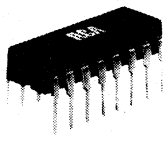
REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 10 V)	0.5 mV
LOAD REGULATION (ΔI_L = 100 mA)	1.5 mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

92CS-24187R1

Fig. 32 – Shunt regulator circuit.

CA1524, CA2524, CA3524 Types



16-Lead Dual-In-Line Plastic Package

H-1611

Regulating Pulse Width Modulator

Features:

- *Complete PWM power control circuitry*
- *Separate outputs for Single-ended or push-pull operation*
- *Line and load regulation of 0.2% typ.*
- *Internal reference supply with 1% max. oscillator and reference voltage variation over full temperature range*
- *Standby current of less than 10 mA*
- *Frequency of operation beyond 100 kHz*
- *Variable output dead time of 0.5 to 5 μs*
- *Low $V_{CE(sat)}$ over the temperature range*

The RCA-CA1524, CA2524, and CA3524 are silicon monolithic integrated circuits designed to provide all the control circuitry for use in a broad range of switching regulator circuits.

The CA1524, CA2524, and CA3524 have all the features of the industry types SG1524, SG2524, and SG3524 respectively. A block diagram of the CA1524 Series is shown in Fig. 1. The circuit includes a zener voltage reference, transconductance error amplifier, precision R-C oscillator, pulse-width modulator, pulse-steering flip-flop, dual alternating output switches, and current-limiting and shutdown circuitry. This device can be used for switching regulators of either polarity, transformer-coupled dc-dc converters, transformerless voltage doublers, dc-ac power inverters, highly efficient variable power supplies, and polarity converters, as well as other power-control applications.

The CA1524 is specified for the military temperature range of −55°C to +125°C.

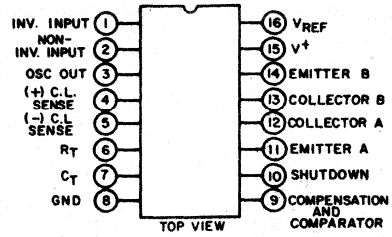
Applications:

- *Positive and negative regulated supplies*
- *Dual-output regulators*
- *Flyback converters*
- *DC-DC transformer-coupled regulating converters*
- *Single-ended DC-DC converters*
- *Variable power supplies*

The CA2524 and CA3524 are specified for the commercial temperature range of 0°C to 70°C. All types operate over a supply voltage range of 8 to 40 V, have a rated operating temperature range of −55°C to +125°C, and are supplied in 16-lead dual-in-line plastic packages (E suffix). The CA3524 is available in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

INPUT VOLTAGE (BETWEEN V_{IN} AND GROUND TERMINALS)	40 V
OPERATING VOLTAGE RANGE (V_{IN} TO GROUND)	8 to 40 V
OUTPUT CURRENT EACH OUTPUT: (TERMINALS 11,12 or 13,14)	100 mA
OUTPUT CURRENT (REFERENCE REGULATOR)	50 mA
OSCILLATOR CHARGING CURRENT	5 mA
DEVICE DISSIPATION:	
Up to T_A = 25°C	1 W
Above T_A = 25°C	Derate linearly 8 mW/°C
OPERATING TEMPERATURE RANGE	−55 to +125°C
STORAGE TEMPERATURE RANGE	−65 to +150°C



TOP VIEW
TERMINAL ASSIGNMENT

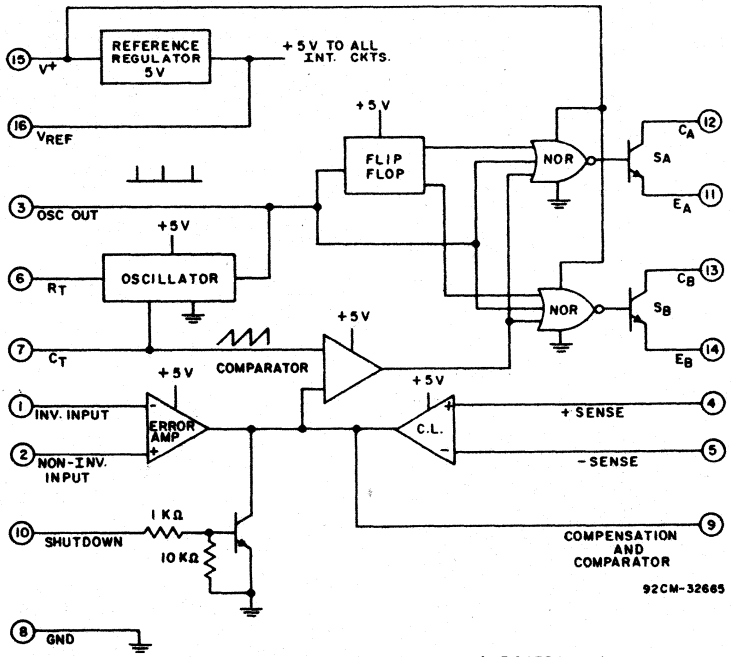


Fig. 1-Functional block diagram of CA1524 series.

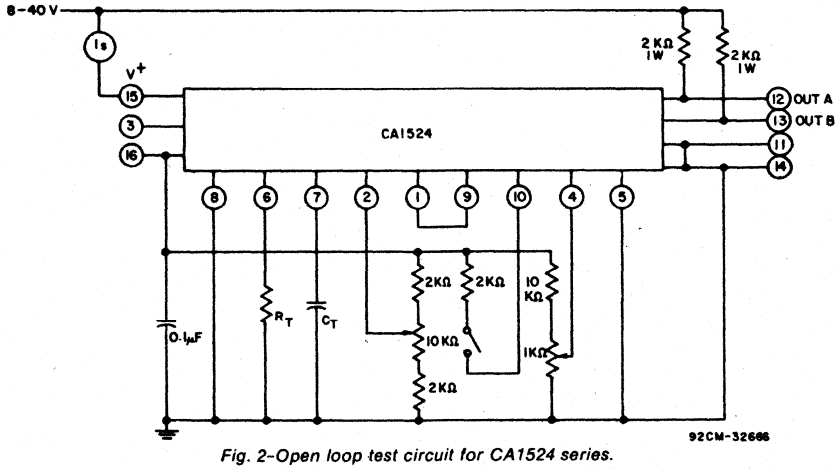


Fig. 2-Open loop test circuit for CA1524 series.

CIRCUIT DESCRIPTION

Voltage Reference Section (see Fig. 3).

The CA1524 Series contains an internal series voltage regulator employing a zener reference to provide a nominal 5 volts output, which is used to bias all internal timing and control circuitry. The output of this regulator is available at terminal 16 and is capable of supplying up to 50 mA. output current. For higher currents, the circuit of Fig. 3 may be used with an external p-n-p transistor and bias resistor. The internal regulator may be bypassed for operation from a fixed 5 volt supply by connecting both terminals 15 and 16 to the input voltage, which must not exceed 6 volts.

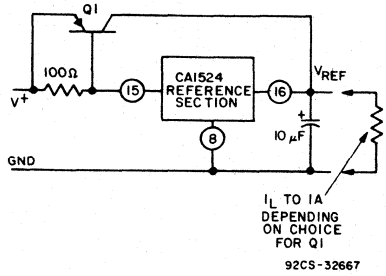


Fig. 3—Circuit for expanding the reference current capability.

Fig. 4 shows the temperature variation of the reference voltage with supply

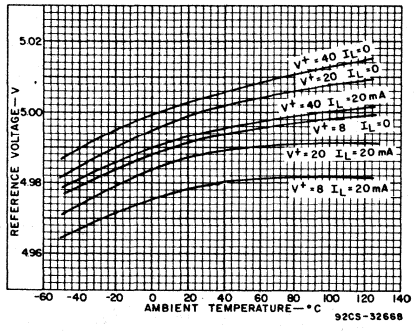


Fig. 4—Typical reference voltage as a function of ambient temperature.

voltages of 8 to 40 volts and load currents up to 20 mA. Load regulation and line regulation curves are shown in Figs. 5 and 6, respectively.

Oscillator Section (see Fig. 3)

Transistors Q42, Q43 and Q44, in conjunction with an external resistor R_T, establishes a constant charging current into an external capacitor C_T to provide a linear ramp voltage at terminal 7. The ramp voltage has a value that ranges from 0.6 to 3.5 volts and is used as the reference for the comparator in the device. The charging current is equal to (5 — $2V_{BE}$)/R_T or approximately 3.6/R_T and should be kept within the range of 30 μA to 2 mA by varying R_T. The discharge time of C_T determines the pulse width of the oscillator output pulse at terminal 3. This pulse has a practical range of 0.5 μs to 5μs for a capacitor range of 0.001 to 0.1 μF. The pulse has two internal uses: as a dead-time control or blanking pulse to the output stages to assure that both outputs

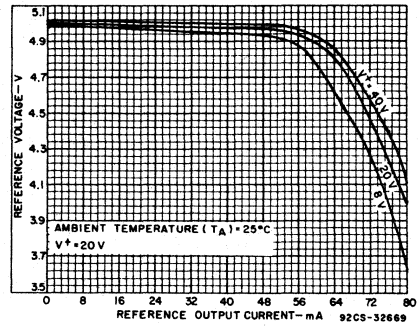


Fig. 5—Typical reference voltage as a function of reference output current.

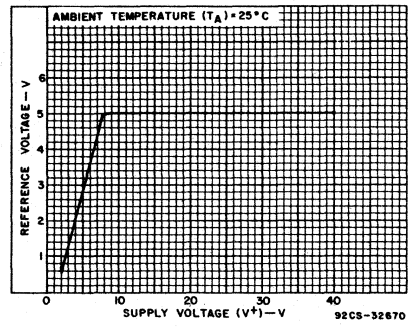


Fig. 6—Typical reference voltage as a function of supply voltage.

cannot be on simultaneously and as a trigger pulse to the internal flip-flop which controls the switching of the output between the two output channels. The output dead-time relationship is shown in Fig. 7. Pulse widths less than 0.5 μs may allow false triggering of one output by removing the blanking pulse prior to a stable state in the flip-flop.

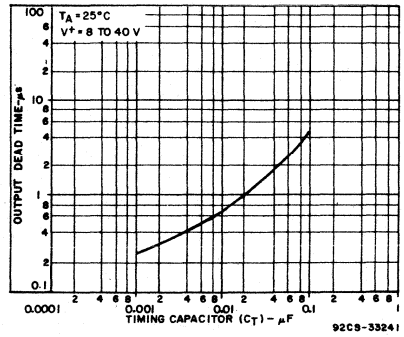


Fig. 7—Typical output stage dead time as a function of timing capacitor value.

ELECTRICAL CHARACTERISTICS *at T_A=-55 to +125°C for CA1524, 0 to +70°C for the CA2524 and CA3524; V^+=20 V and f=20 kHz, unless otherwise stated.*

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA1524, CA2524			CA3524			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section:								
Output Voltage:		4.8	5.0	5.2	4.6	5.0	5.4	V
Line Regulation	V+ = 8 to 40 Volts	—	10	20	—	10	30	mV
Load Regulation	I_L = 0 to 20 mA	—	20	50	—	20	50	mV
Ripple Rejection	f = 120Hz, T_A = 25°C	—	66	—	—	66	—	dB
Short Circuit Current Limit	V_{REF} = 0, T_A = 25°C	—	100	—	—	100	—	mA
Temperature Stability	Over Operating Temperature Range	—	0.3	1	—	0.3	1	%
Long Term Stability	T_A = 25°C	—	20	—	—	20	—	mV/khr
Oscillator Section:								
Maximum Frequency	C_T = 0.001 μF, R_T = 2 KΩ	—	300	—	—	300	—	kHz
Initial Accuracy	R_T and C_T constant	—	5	—	—	5	—	%
Voltage Stability	V+ = 8 to 40 Volts, T_A = 25°C	—	—	1	—	—	1	%
Temperature Stability	Over Operating Temperature Range	—	—	2	—	—	2	%
Output Amplitude	Term.3, T_A = 25°C	—	3.5	—	—	3.5	—	V
Output Pulse Width	C_T = 0.01 μF, T_A = 25°C	—	0.5	—	—	0.5	—	μs
Error Amplifier Section:								
Input Offset Voltage	V_{CM} = 2.5 Volts	—	0.5	5	—	2	10	mV
Input Bias Current	V_{CM} = 2.5 Volts	—	1	10	—	1	10	μA
Open Loop Voltage Gain		72	80	—	60	80	—	dB
Common Mode Voltage	T_A = 25°C	1.8	—	3.4	1.8	—	3.4	V
Common Mode Rejection Ratio	T_A = 25°C	—	70	—	—	70	—	dB
Small Signal Bandwidth	A_V = OdB, T_A = 25°C	—	3	—	—	3	—	MHz
Output Voltage	T_A = 25°C	0.5	—	3.8	0.5	—	3.8	V

If a small value of C_T must be used, the pulse width can be further expanded by the addition of a shunt capacitor in the order of 100 pF but no greater then 1000 pF, from terminal 3 to ground. When the oscillator output pulse is used as a sync input to an oscilloscope, the cable and input capacitances may increase the pulse width slightly. A 2 kΩ resistor at terminal 3 will usually provide sufficient decoupling of the cable. The upper limit of the pulse width is determined by the maximum duty cycle acceptable. To provide an expansion of the dead time without loading the oscillator, the circuit of Fig. 8 may be used.

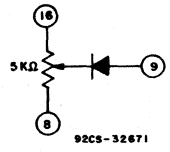


Fig. 8—Circuit for expansion of dead time.

The oscillator period is determined by R_T and C_T, with an approximate value of $t = R_T C_T$, where R_T is in ohms, C_T is in μF, and t is in μs. Excess lead lengths, which produce stray capacitances, should be avoided in connecting R_T and

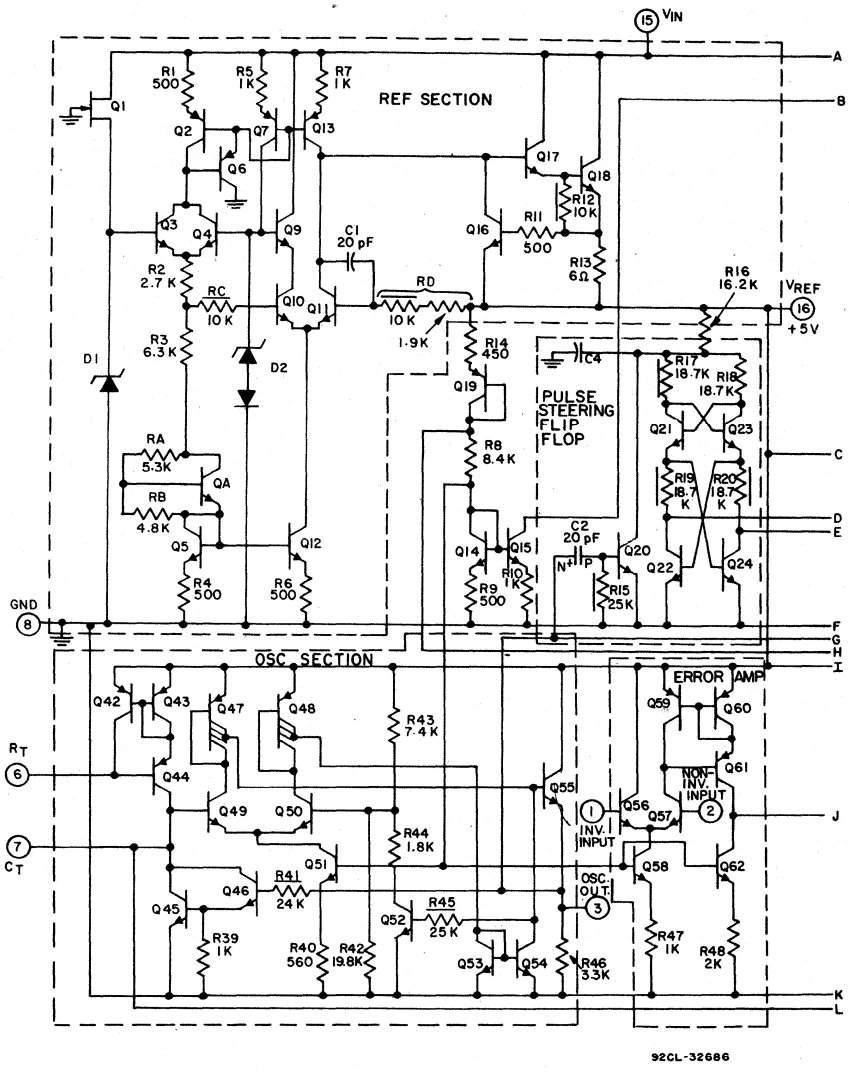


Fig. 9–Schematic diagram (continued on next page).

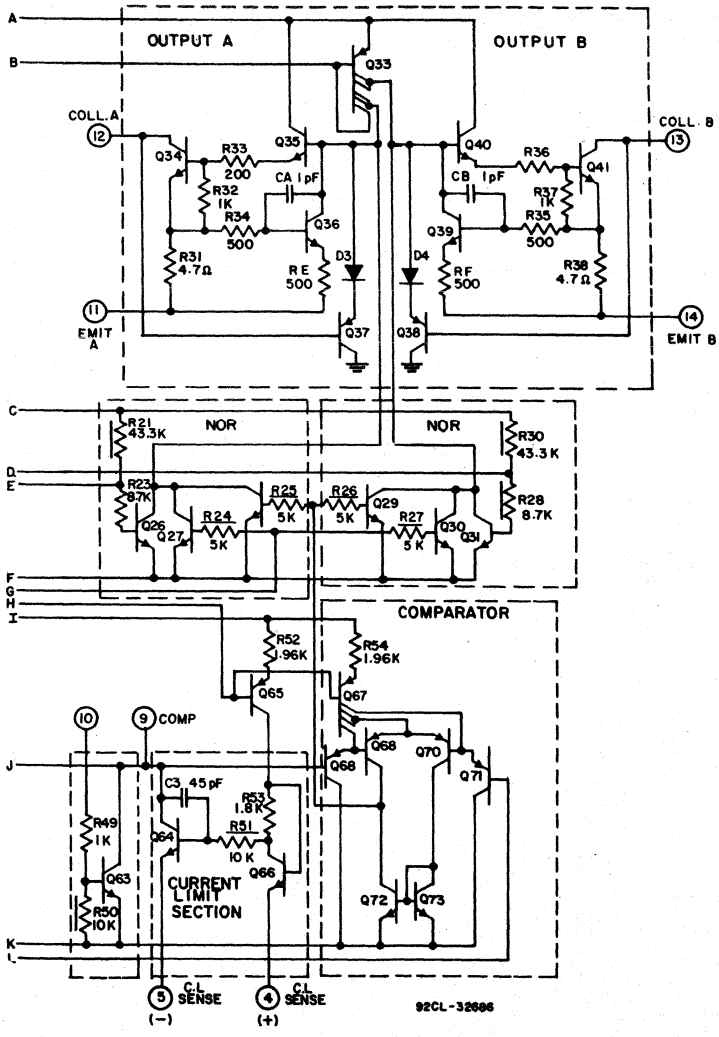


Fig. 9–Schematic diagram (continued from previous page).

ELECTRICAL CHARACTERISTICS *at T_A=-55 to +125°C for CA1524, 0 to +70°C for the CA2524 and CA3524; V^+=20 V and f=20 kHz, unless otherwise stated.*

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA1524, CA2524			CA3524			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Comparator Section:								
Duty Cycle	% Each Output On	0	—	45	0	—	45	%
Input Threshold	Zero Duty Cycle	—	1	—	—	1	—	V
Input Threshold	Max. Duty Cycle	—	3.5	—	—	3.5	—	V
Input Bias Current		—	1	—	—	1	—	μA
Current Limiting Section:								
Sense Voltage	Term. 9 = 2 V with Error Amplifier Set for Max Out, T_A = 25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.		—	0.2	—	—	0.2	—	mV/°C
Common Mode Voltage		-1	—	+1	-1	—	+1	V
Output Section: (Each Output)								
Collector-Emitter Voltage		40	—	—	40	—	—	V
Collector Leakage Current	V_{CE} = 40 V	—	0.1	50	—	0.1	50	μA
Saturation Voltage	V^+ = 40 V, I_C = 50 mA	—	0.8	2	—	0.8	2	V
Emitter Output Voltage	V^+ = 20 V	17	18	—	17	18	—	V
Rise Time	R_C = 2 KΩ T_A = 25°C	—	0.2	—	—	0.2	—	μs
Fall Time	R_C = 2 KΩ T_A = 25°C	—	0.1	—	—	0.1	—	μs
Total Standby Current: *Is	V^+ = 40 V	—	4	10	—	4	10	mA

* Excluding oscillator charging current, error and current limit dividers, and with outputs open.

C_T to their respective terminals. Fig. 10 provides curves for selecting these values for a wide range of oscillator periods. For series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle with the output stage frequency the same as the oscillator frequency. Since the outputs are separate, push-pull and flyback applications are possible. The flip-flop divides the frequency such that the duty cycle of each output is 0-45% and the overall frequency is half that of the oscillator. Curves of the output duty cycle as a function of the voltage at terminal 9 are shown in Fig. 11. To synchronize two or more CA1524's, one must be designated as master, with R_TC_T set for the correct period. Each of the remaining units (slaves) must have a C_T of 1/2 the value used in the master and approximately a 10% longer R_TC_T period than the master. Connecting terminal 3 together on all units assures that the master output pulse, which occurs first and has a wider pulse width, will reset the slave units.

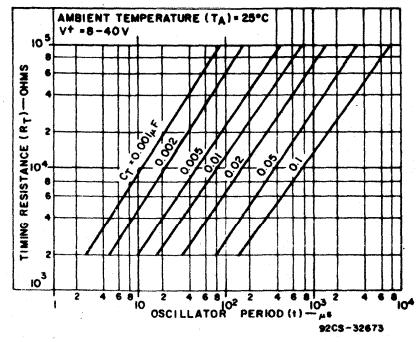


Fig. 10-Typical oscillator period as a function of R_T and C_T.

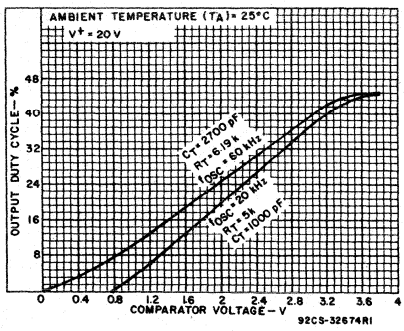


Fig. 11—Typical duty cycle as a function of comparator voltage (at terminal 9).

Error Amplifier Section (see Fig. 9)

The error amplifier consists of a differential pair (Q56, Q57) with an active load (Q61 and Q62) forming a differential transconductance amplifier. Since Q61 is driven by a constant current source, Q62, the output impedance R_{out}, terminal 9, is very high (≅5 MΩ).
The gain is:

$$A_V = g_m R = 8\, I_C\, R / 2KT = 10^4,$$

where $R = \dfrac{R_{out}\, R_L}{R_{out} + R_L}$, $R_L = \infty$, $A_V \cong 10^4$

Since R_{out} is extremely high, the gain can be easily reduced from a nominal 10^4 (80 dB) by the addition of an external shunt resistor from terminal 9 to ground as shown in Fig. 12.

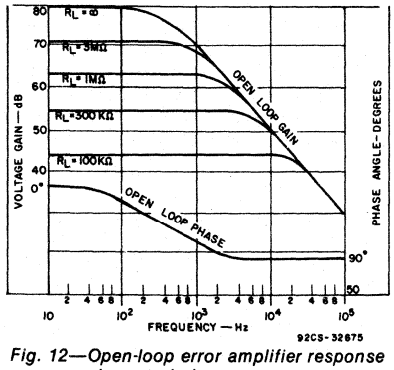


Fig. 12—Open-loop error amplifier response characteristics.

The output amplifier terminal is also used to compensate the system for ac stability. The frequency response and phase shift curves are shown in Fig. 12. The uncompensated amplifier has a single pole at approximately 250 Hz and a unity gain cross-over at 3 MHz.

Since most output filter designs introduce one or more additional poles at a lower frequency, the best network to stabilize the system is a series RC combination at terminal 9 to ground. This network should be designed to introduce a zero to cancel out one of the output filter poles. A good starting point to determine the external poles is a 1000 pF capacitor and a variable series 50 kΩ potentiometer from terminal 9 to ground. The compensation point is also a convenient place to insert any programming signal to override the error amplifier. Internal shutdown and current limiting are also connected at terminal 9. Any external circuit that can sink 200 μA can pull this point to ground and shut off both output drivers.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and will be stable in either the inverting or non-inverting mode. Input common-mode limits must be observed; if not, output signal inversion may result. The internal 5-volt reference can be used for conventional regulator applications if divided as shown in Fig. 13. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

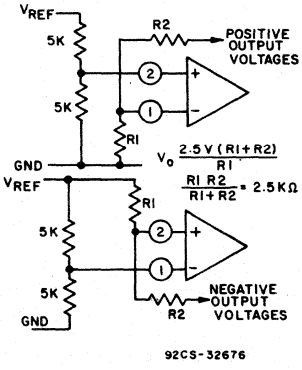


Fig. 13—Error amplifier biasing circuits.

Current Limiting Section (see Fig. 9)

The current limiting section consists of two transistors (Q64, Q66) connected to the error amplifier output terminal. By matching the base-to-emitter voltages of Q64 and Q66 and assuming negligible voltage drop across R51:

$$V_{THRESHOLD} = V_{BE(Q64)} + I_{(Q65)} R_{53} - V_{BE(Q66)}$$
$$= I_{(Q65)} R_{53} \cong 200\ mV$$

Although this circuit provides a small threshold with a negligible temperature coefficient, some limitations to its use must be considered. The circuit has a ±1 volt common mode range which requires sensing in the ground line. The other factor to consider is that the frequency compensation provided by $R_{51}C_3$ and Q64 produces a roll-off pole at approximately 300 Hz.

Due to the low gain of this circuit, there is a transition region as the current-limit amplifier takes over pulse width control from the error amplifier. For testing purposes, the threshold is defined as the input voltage to the current-limiting amplifier to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, terminals 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur (see Fig. 23). Another application is to ground terminal 5 and use terminal 4 as an additional shutdown terminal: i.e. the output will be off with terminal 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Fig. 14. This circuit can reduce the short-circuit current (I_{SC}) to approximately 1/3 the maximum available output current (I_{MAX}).

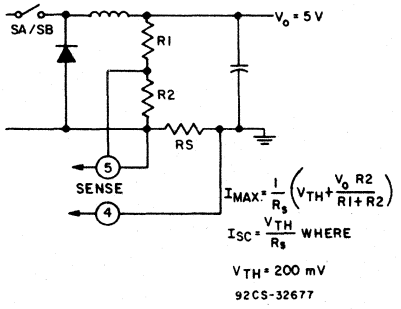


Fig. 14—Foldback current limiting circuit used to reduce power dissipation under shorted output conditions.

Output Section (see Fig. 9)

The CA1524 Series outputs are two identical n-p-n transistors with both collectors and emitters uncommitted. Each output transistor has antisaturation circuitry that enables a fast transient response for the wide range of oscillator frequencies. Current limiting of the output section is set at 100 mA for each output and 100 mA total if both outputs are paralleled. Having both emitters and collector available provides the versatility to drive either n-p-n or p-n-p external transistors. Curves of the output saturation voltage as a function of temperature and output current are shown in Figs. 15 and 16 respectively.

There are a number of output configurations possible in the application of the CA1524 to voltage regulator circuits which fall into three basic classifications:

1. Capacitor-diode coupled voltage multipliers
2. Inductor-capacitor single-ended circuits
3. Transformer-coupled circuits

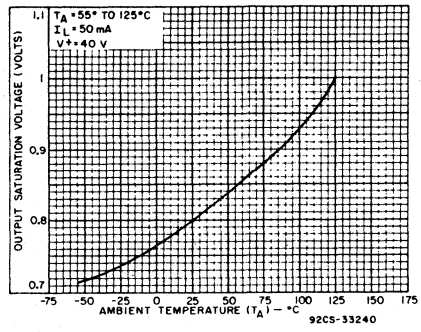


Fig. 15—Typical output saturation voltage as function of ambient temperature.

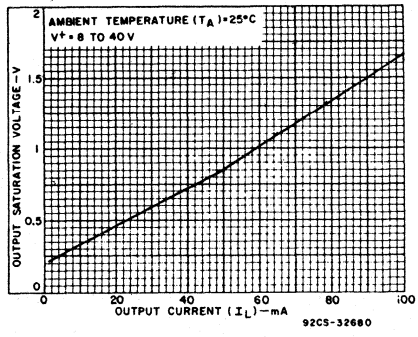


Fig. 16—Typical output saturation voltage as a function of output current.

Examples of these configurations are shown in Fig. 17, 18, and 19. In each case, the switches can be either the output transistors in the CA1524 or added external transistors, depending on the load current requirements.

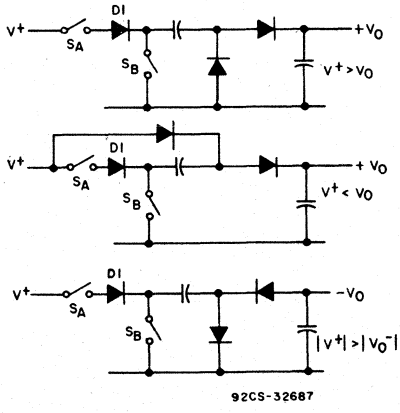


Fig. 17—Capacitor-diode coupled voltage multiplier output stages. (Note: Diode D1 is necessary to prevent reverse emitter-base breakdown of transistor switch S_A).

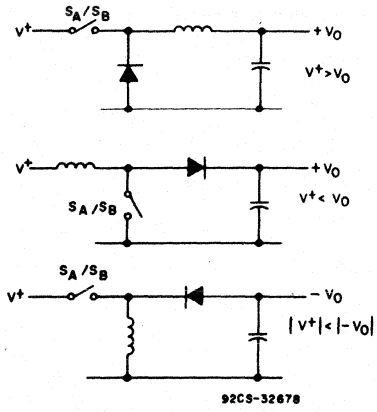


Fig. 18—Single-ended inductor circuits where the two outputs of the 1524 are connected in parallel.

TABLE I - Input vs. Output voltage, and Feedback Resistor Values for I_L = 40 mA. (For capacitor-diode output circuit in Fig. 20)

V_O (V)	R2 (kΩ)	V+ (min.) (V)
-0.5	6	8
-2.5	10	9
-3	11	10
-4	13	11
-5	15	12
-6	17	13
-7	19	14
-8	21	15
-9	23	16
-10	25	17
-11	27	18
-12	29	19
-13	31	20
-14	33	21
-15	35	22
-16	37	23
-17	39	24
-18	41	25
-19	43	26
-20	45	27

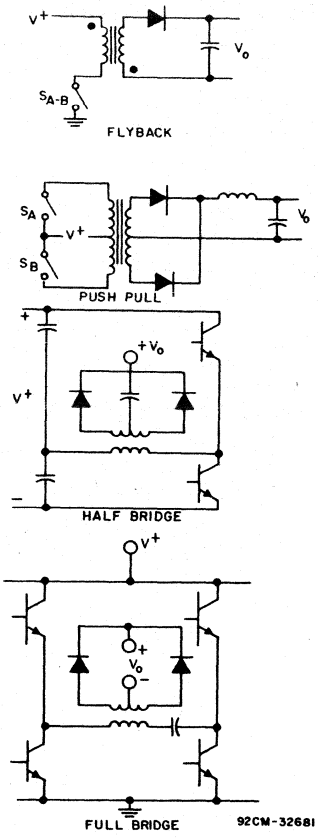


Fig. 19—Transformer-coupled outputs.

APPLICATIONS

Capacitor-Diode Output Circuit

A capacitor-diode output filter is used in Fig. 20 to convert +15 Vdc to −5 Vdc at output currents up to 50 mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table I gives the required minimum input voltage and feedback resistor values, R_2, for an output voltage

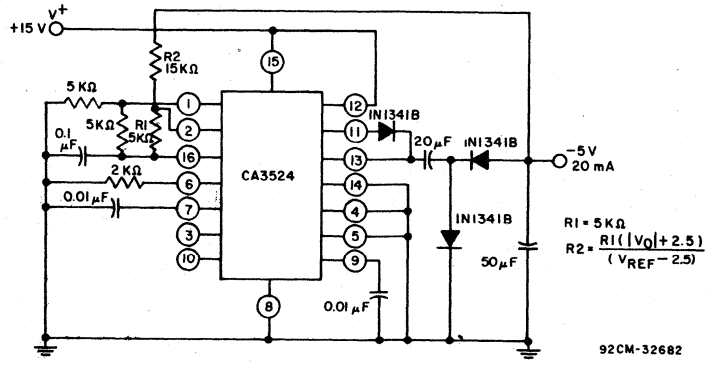


Fig. 20—Capacitor-diode output circuit.

range of −0.5 V to −20 V with an output current of 40 mA.

Single-Ended Switching Regulator

The CA1524 in the circuit of Fig. 21 has both output stages connected in parallel to produce an effective 0-90% duty cycle. Transistor Q1 is pulsed on and off by these output stages. Regulation is achieved from the feedback provided by R1 and R2 to the error amplifier which adjusts the on-time of the output transistors according to the load current being drawn. Various output voltages can be obtained by adjusting R1 and R2. The use of an output inductor requires an R-C phase compensation network to stabilize the system. Current limiting is set at 1.9 amperes by the sense resistor R3.

Flyback Converter

Fig. 22 shows a flyback converter circuit for generating a dual 15-volt output at 20 mA from a 5-volt regulated line. Reference voltage is provided by the input and the internal reference generator is unused. Current limiting in this circuit is accomplished by sensing current in the primary line and resetting the soft-start circuit.

Push-Pull Converter

The output stages of the CA1524 provide the drive for transistors Q1 and Q2 in the push-pull application of Fig. 23. Since the internal flip-flop divides the oscillator frequency by two, the oscillator must be set at twice the output frequency. Current limiting for this circuit is done in the primary of transformer T1 so that the pulse width will be reduced if transformer saturation should occur.

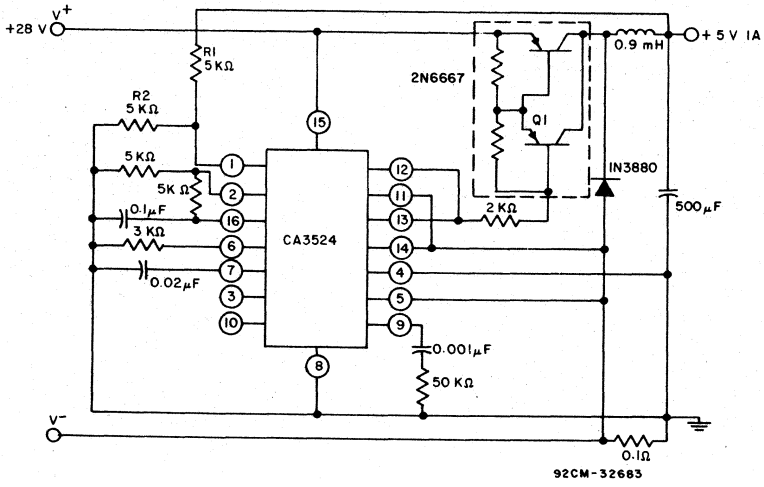


Fig. 21—Single-ended LC switching regulator circuit.

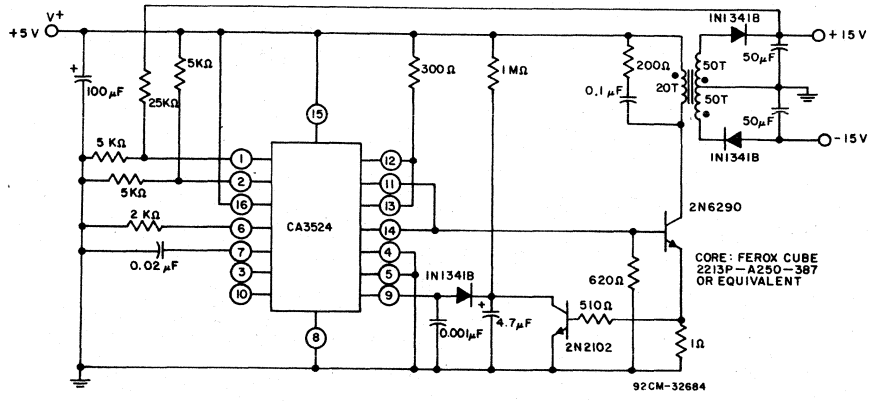


Fig. 22—Flyback converter circuit.

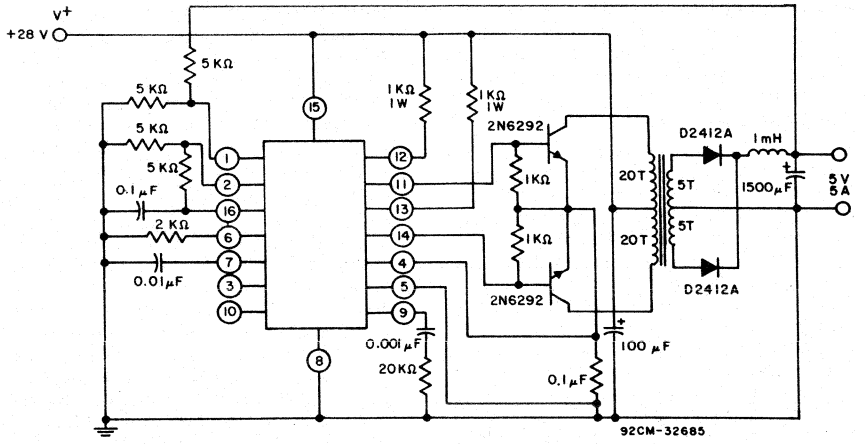


Fig. 23-Push-pull transformer-coupled converter.

Low-Frequency Pulse Generator

Fig. 24 shows the CA1524 being used as a low-frequency pulse generator. Since all components (error amplifier, oscillator, oscillator reference regulator, output transistor drivers) are on the IC, a regulated 5 V (or 2.5 V) pulse of 0%-45% (or 0%-90%) on time is possible over a frequency range of 150 to 500 Hz. Switch S_1 is used to go from a 5-V output pulse (S_1 closed) to a 2.5-V output pulse (S_1 open) with a duty cycle range of 0% to 45%. The output frequency will be roughly half of the oscillator frequency when the output transistors are not connected in parallel (75 Hz to 250 Hz respectively). Switch S_2 will allow both output stages to be paralleled for an effective duty cycle of 0%-90% with the output frequency range from 150 to 500 Hz. The frequency is adjusted by R_1; the duty cycle is controlled by R_2.

Efficient Laboratory Power Supply

The CA1524 as a highly-efficient laboratory supply is shown in Fig. 25. The output voltage can range from 7 to 30 volts for an input voltage range from 33 to 40 volts. Output current of up to 5 amperes is possible. The circuit operates as follows: The two output transistors of the CA1524 are connected in parallel to achieve a maximum duty cycle of 90%. They drive the 2N6650 p-n-p Darlington transistor. The error amplifier's input terminal, pin 1, is first adjusted to 3.4 volts through divider R_3, R_4 and R_5. R_4 is provided so the maximum output can be varied. For this application, the maximum output voltage is 30 volts. The internal reference level of the CA1524's reference regulator is varied, via R_7, over the amplifier's input span. This in turn varies the comparator voltage at pin 9 from a level of 0.5 to 3.8 volts, thus moving the

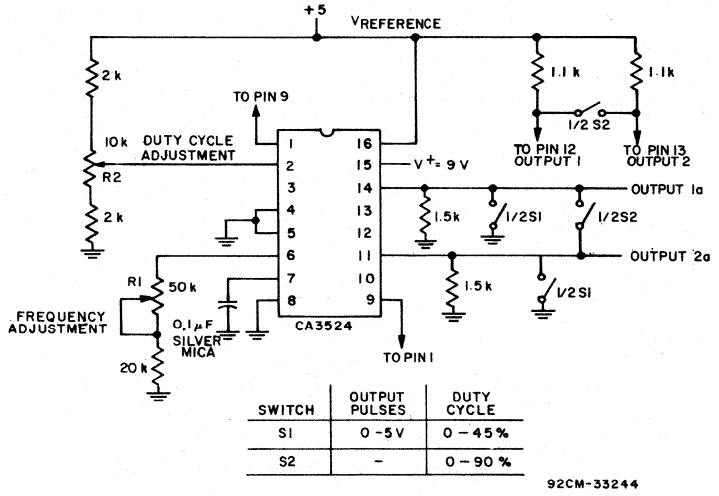


Fig. 24-Low-frequency pulse generator.

output section's on time. Since the reference level is varied, the feedback voltage will track that level and cause the output voltage to change respectively in track with the reference's change at pin 2.

Digital Readout Scale

The CA1524 can be used as the driving source for an electronic scale application. The circuit shown in Figs. 26 and 27 uses half (Q_2) of the CA1524 output in a low-voltage switching regulator (2.2 V) application to drive the LED's displaying the weight. The remaining output stage (Q_1) is used as a driver for the sampling plates PL1 and PL2. Since the CA1524 contains a 5-volt internal regulator and a wide operating range of 8 to 40 volts, a single 9-volt battery can power the total system. The two plates, PL1 and PL2, are driven with opposite phase signals (frequency held constant but duty cycle may change) from the pulse-width modulator IC (1524). The sensor, S, is located between the two plates. Plates PL1, S and PL2 form an effective capacitance bridge-type divider network. As plate S is moved according to the object's weight, a change in capacitance is noted between PL1, S and PL2. This change is reflected as a voltage to the ac amplifier (CA3160). At the null position the signals from PL1 and PL2 as detected by S are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal at S becomes greater. The CA3160 ac amplifier provides a buffer for the small signal change noted at S. The output of the CA3160 is converted to a dc voltage by a peak-to-peak detector. A peak-to-peak detector is needed, since the duty cycle of the sampled waveform is subject to change. The detector output is filtered further and displayed via the CA3161E and CA3162E digital readout system, indicating the weight on the scale.

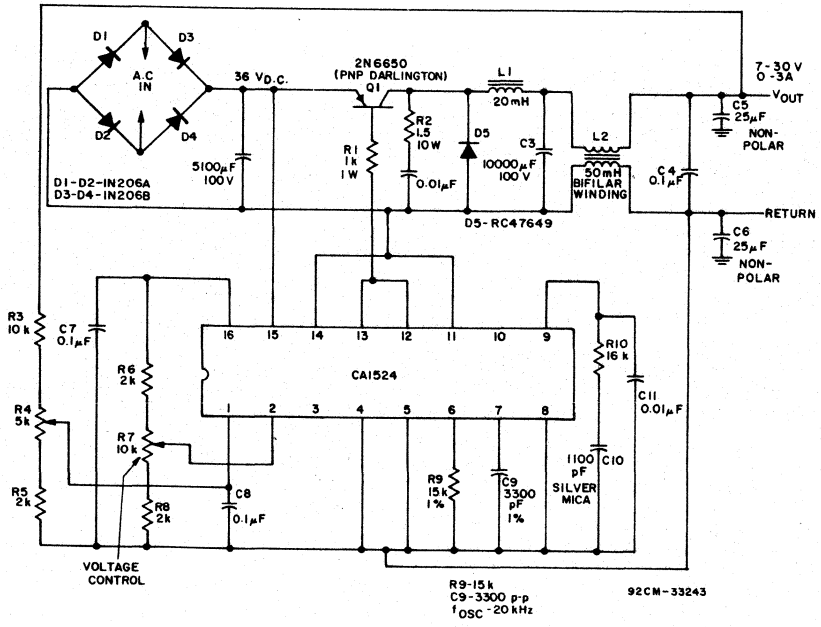


Fig. 25-The CA1524 used as a OA-5A, 7-30-V laboratory supply.

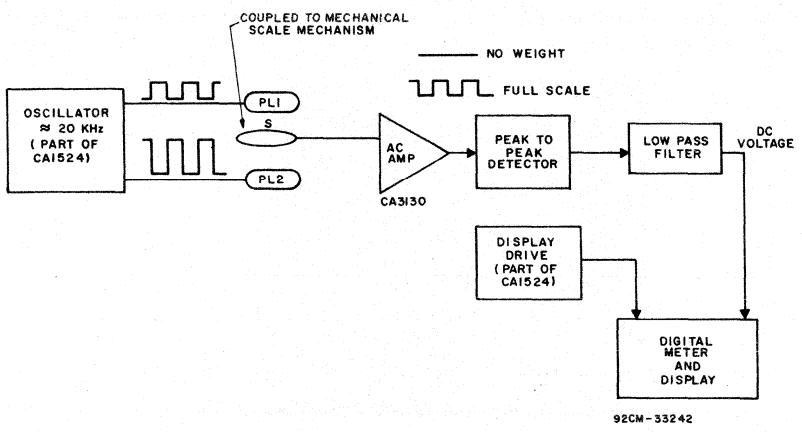


Fig. 26-Basic digital readout scale.

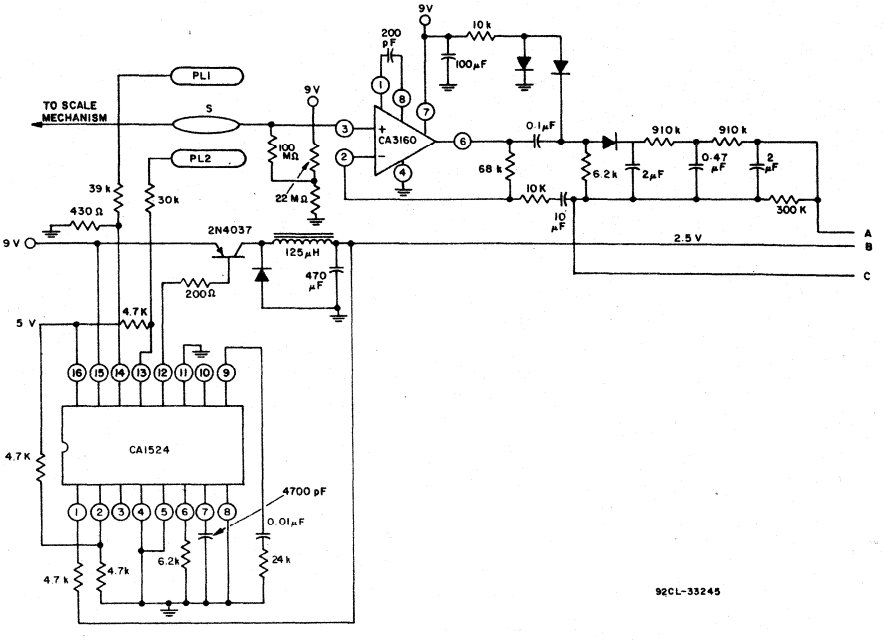
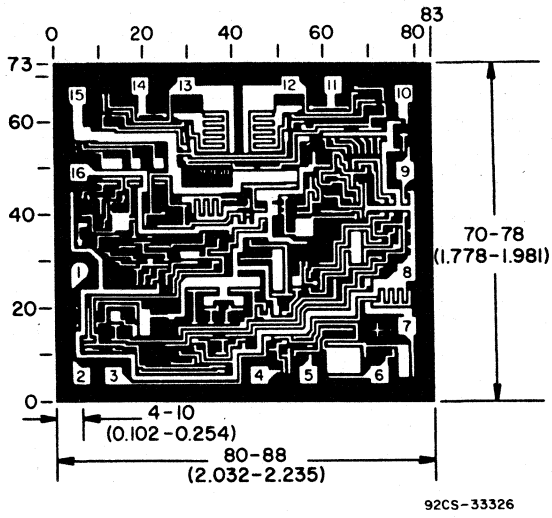


Fig. 27-Schematic diagram of digital readout scale.



Dimensions and pad layout for CA3524H chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

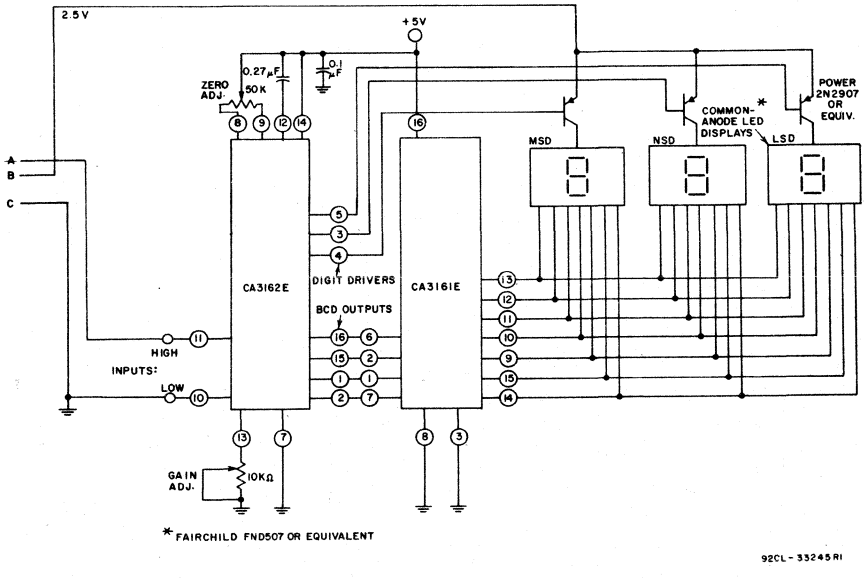
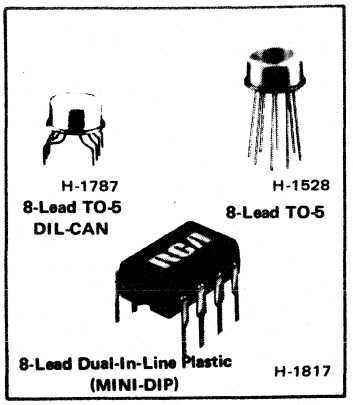


Fig. 27-Schematic diagram of digital readout scale.



Positive Voltage Regulators

For Regulated Voltages from 1.7 V to 46 V
at Currents up to 100 mA

Features

- Up to 100 mA output current
- Input and output short-circuit protection
- Load and line regulation: 0.025%
- Pin compatible with LM100 Series
- Adjustable output voltage

Applications

- Shunt voltage regulator
- Current regulator
- Switching voltage regulator
- High-current voltage regulator
- Combination positive and negative voltage regulator
- Dual tracking regulator

RCA-CA3085, CA3085A, and CA3085B are silicon monolithic integrated circuits designed specifically for service as voltage regulators at output voltages ranging from 1.7 to 46 volts at currents up to 100 milliamperes.

A block diagram of the CA3085 Series is shown in Fig. 1. The diagram shows the connecting terminals that provide access to the regulator circuit components. The voltage regulators provide important features such as: frequency compensation, short-circuit protection, temperature-compensated reference voltage, current limiting, and booster input. These devices are useful in a wide range of applications for regulating high-current, switching, shunt, and positive and negative voltages. They are also applicable for current and dual-tracking regulation.

The CA3085A and CA3085B have output current capabilities up to 100 mA and the CA3085 up to 12 mA without the use of external pass transistors. However, all the devices can provide voltage regulation at load currents greater than 100 mA with the use of suitable external pass transistors. The CA3085 Series has an unregulated input voltage ranging from 7.5 to 30 V (CA3085), 7.5 to 40 V (CA3085A), and 7.5 to 50 V (CA3085B) and a minimum regulated output voltage of 26 V (CA3085), 36 V (CA3085A), and 46 V (CA3085B).

The CA3085A is unilaterally interchangeable with the CA3055.

These types are supplied in the 8-lead TO-5 style package (CA3085, CA3085A, CA3085B, and the 8-lead TO-5 with dual-in-line formed leads ("DIL-CAN", CA3085S, CA3085AS, CA3085BS). The CA3085 is also supplied in the 8-lead dual-in-line plastic package ("MINI-DIP", CA3085E), and in chip form (CA3085H).

Type	V_{IN} Range V	V_{OUT} Range V	Max. I_{OUT} mA	Max. Load Regulation % V_{OUT}
CA3085	7.5 to 30	1.8 to 26	12*	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

* This value may be extended to 100 mA; however, regulation is not specified beyond 12 mA.

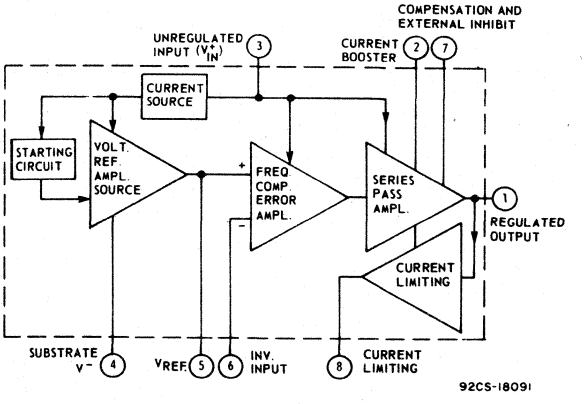


Fig. 1—Block diagram of CA3085 Series.

CA3085, CA3085A, CA3085B Types

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES at T_A = 25°C

POWER DISSIPATION: WITHOUT HEAT SINK

up to T_A = 55°C ..... 630 mW

above T_A = 55°C derate linearly @6.67 mW/°C

WITH HEAT SINK (TO-5 ONLY)

up to T_C = 55°C .... 1.6 W

above T_C = 55°C .... derate linearly at 16.7 mW/°C

TEMPERATURE RANGE:

Operating ..... −55 to +125°C

Storage ..... −65 to +150°C

UNREGULATED INPUT VOLTAGE:

CA3085 ..... 30 V

CA3085A ..... 40 V

CA3085B ..... 50 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal No. 7 and horizontal Terminal No. 1 is +3 to −10 volts.

MAXIMUM VOLTAGE RATINGS

TERMINAL No.	5	6	7	8	1	2	3	4
5	–	+5 −5	•	•	•	•	•	+10 0
6	–	–	•	•	•	•	•	•
7	–	–	–	+3 −10	+3 −10	•	•	+‡ 0
8	–	–	–	–	+5 −1	•	•	•
1	–	–	–	–	–	10 −‡	0 −‡	+‡ 0
2	–	–	–	–	–	–	0 –	+‡ 0
3	–	–	–	–	–	–	–	+‡ 0
4	–	–	–	–	–	–	–	Substrate & Case

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

‡30 V for CA3085
40 V for CA3085A
50 V for CA3085B

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
5	10	1.0
6	1.0	−0.1
7	1.0	−1.0
8	0.1	10
1	20	150
2	150	60
3	150	60
4	–	–

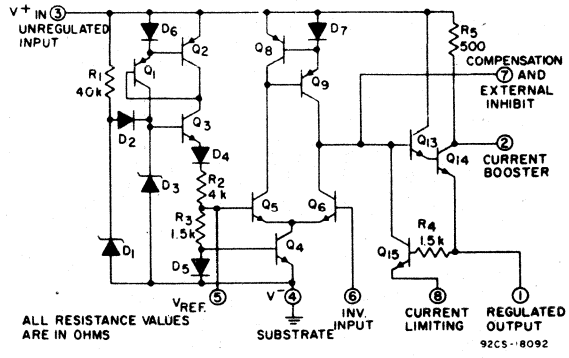


Fig.2—Schematic diagram of CA3085 Series.

CA3085, CA3085A, CA3085B Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: Test Circuit Fig. No.	TEST CONDITIONS: T_A = 25°C [Unless indicated otherwise]		CA3085 MIN.	CA3085 TYP.	CA3085 MAX.	CA3085A MIN.	CA3085A TYP.	CA3085A MAX.	CA3085B MIN.	CA3085B TYP.	CA3085B MAX.	UNITS
Reference Voltage	V_{REF}	4	V^+_{IN} = 15V		1.4	1.6	1.8	1.5	1.6	1.7	1.5	1.6	1.7	V
Quiescent Regulator Current	$I_{quiescent}$	4	V^+_{IN} = 30V		–	3.3	4.5	—	–	–	–	–	–	mA
			V^+_{IN} = 40V		–	–	–	–	3.65	5	–	–	–	
			V^+_{IN} = 50V		–	–	–	–	–	–	–	4.05	7	
Input Voltage Range	$V_{IN(range)}$	–	–		7.5	–	30	7.5	–	40	7.5	–	50	V
Maximum Output Voltage	$V_{O(max.)}$	4	V^+_{IN} = 30,40,50V#; R_L = 365 Ω; Term. No. 6 to Gnd.		26	27	–	36	37	–	46	47	–	V
Minimum Output Voltage	$V_{O(min.)}$	4	V^+_{IN} = 30V		–	1.6	1.8	–	1.6	1.7	–	1.6	1.7	V
Input-Output Voltage Differential	V_{IN}-V_{OUT}	–	–		4	–	28	4	–	38	3.5	–	48	V
Limiting Current	I_{LIM}	7	V^+_{IN} = 16V, V^+_{OUT} = 10V R_{SCP}* = 6 Ω		–	96	120	–	96	120	–	96	120	mA
Load Regulation●	–	–	I_L = 1 to 100mA, R_{SCP} = 0		–	–	–	–	0.025	0.15	–	0.025	0.15	%V_{OUT}
		–	I_L = 1 to 100mA, R_{SCP} = 0 T_A = 0°C to +70°C		–	–	–	–	0.035	0.6	–	0.035	0.6	
		–	I_L = 1 to 12mA, R_{SCP} = 0		–	0.003	0.1	–	–	–	–	–	–	
Line Regulation▲	–	–	I_L = 1 mA, R_{SCP} = 0		–	0.025	0.1	–	0.025	0.075	–	0.025	0.04	%/V
		–	I_L = 1mA, R_{SCP} = 0 T_A = 0°C to +70°C		–	0.04	0.15	–	0.04	0.1	–	0.04	0.08	
Equivalent Noise Output Voltage	V_{NOISE}	11	V^+_{IN} = 25V	C_{REF} = 0	–	0.5	–	–	0.5	–	–	0.5	–	mV p-p
				C_{REF} = 0.22μF	–	0.3	–	–	0.3	–	–	0.3	–	
Ripple Rejection	–	12	V^+_{IN} = 25V f = 1kHz	C_{REF} = 0	–	50	–	–	50	–	45	50	–	dB
				C_{REF} = 2μF	–	56	–	–	56	–	50	56	–	
Output Resistance	r_o	12	V^+_{IN} = 25V, f = 1kHz		–	0.075	1.1	–	0.075	0.3	–	0.075	0.3	Ω
Temperature Coefficient of Reference and Output Voltages	ΔV_{REF}, ΔV_o	–	I_L = 0, V_{REF} = 1.6V		–	0.0035	–	–	0.0035	–	–	0.0035	–	%/°C
Load Transient Recovery Time: Turn On	t_{ON}	16	V^+_{IN} = 25V, +50mA Step		–	1	–	–	1	–	–	1	–	μs
Turn Off	t_{OFF}		V^+_{IN} = 25V, −50mA Step		–	3	–	–	3	–	–	3	–	μs
Line Transient Recovery Time: Turn On	t_{ON}	–	V^+_{IN} = 25V, f = 1kHz, 2V Step		–	0.8	–	–	0.8	–	–	0.8	–	μs
Turn Off	t_{OFF}	–			–	0.4	–	–	0.4	–	–	0.4	–	μs

30V (CA3085), 40V(CA3085A), 50V(CA3085B)

* RSCP: Short-circuit protection resistance

● Load Regulation = $\frac{\Delta V_{OUT}}{V_{OUT(initial)}} \times 100\%$

▲ Line Regulation = $\frac{(\Delta V_{OUT})}{[V_{OUT(initial)}]\ (\Delta V_{IN})} \times 100\%$

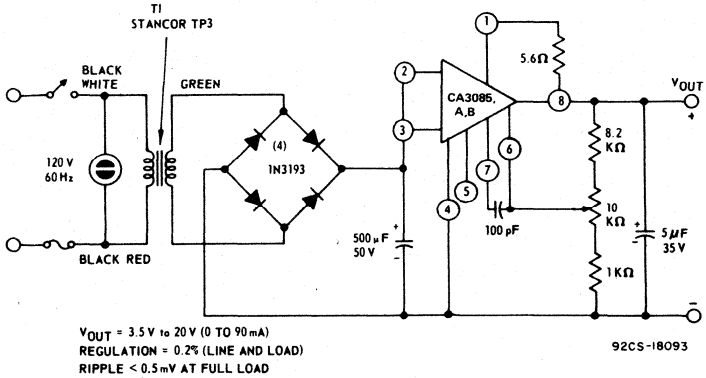
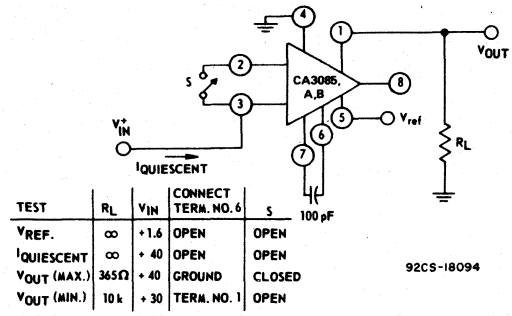


Fig.3—Application of the CA3085 Series in a typical power supply.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES



TEST	R_L	V_{IN}	CONNECT TERM. NO. 6	S
$V_{REF.}$	∞	+1.6	OPEN	OPEN
$I_{QUIESCENT}$	∞	+40	OPEN	OPEN
V_{OUT} (MAX.)	365Ω	+40	GROUND	CLOSED
V_{OUT} (MIN.)	10k	+30	TERM. NO. 1	OPEN

Fig.4—Test circuit for V_{REF}, $I_{quiescent}$, $V_{OUT(max.)}$, $V_{OUT(min.)}$.

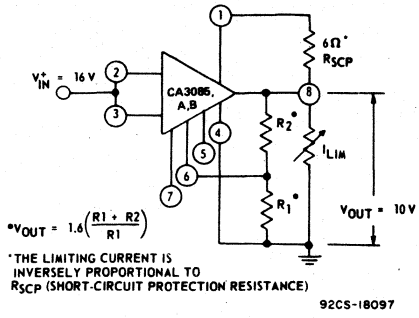


Fig.7—Test circuit for limiting current

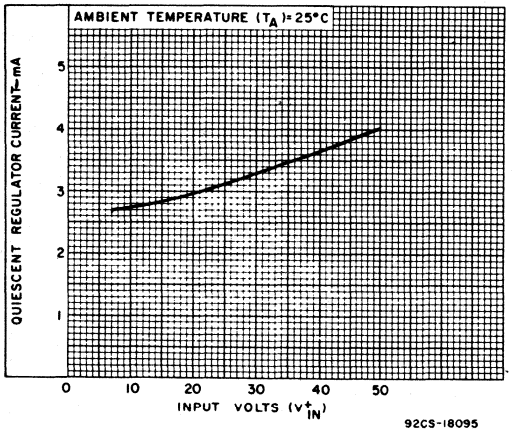


Fig.5—$I_{quiescent}$ vs. V^+_{IN}.

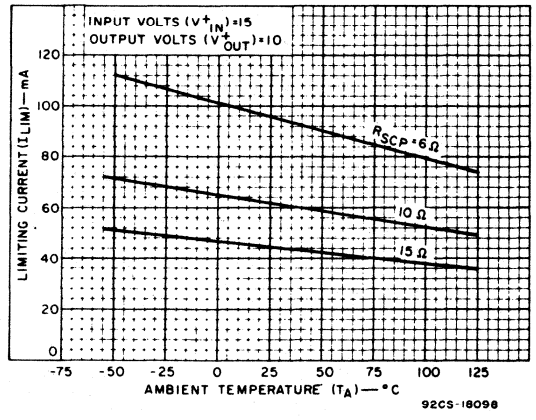


Fig.8—I_{LIM} vs. T_A.

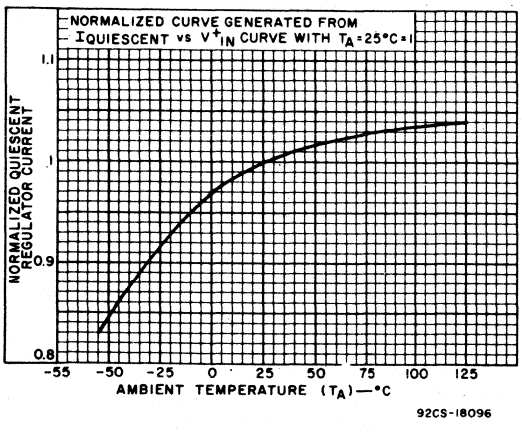


Fig.6—Normalized $I_{quiescent}$ vs. T_A.

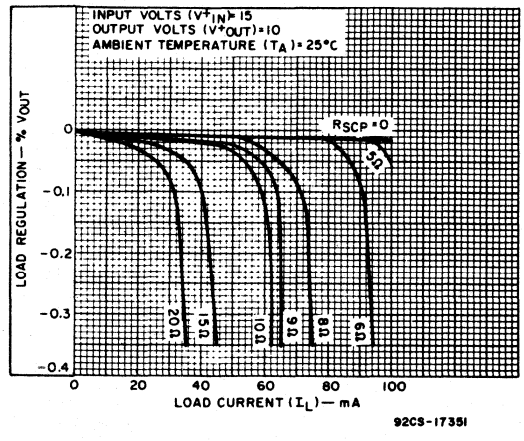


Fig.9—Load regulation characteristics.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES

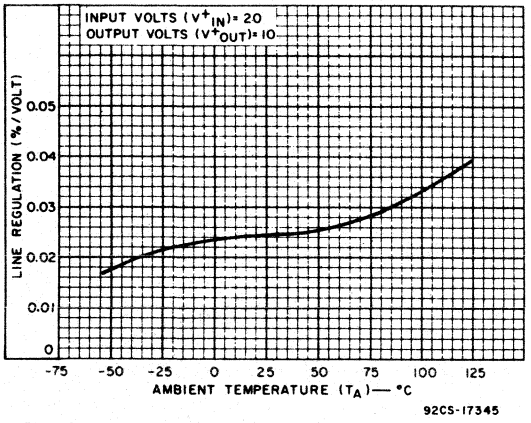


Fig.10—Line regulation temperature characteristics.

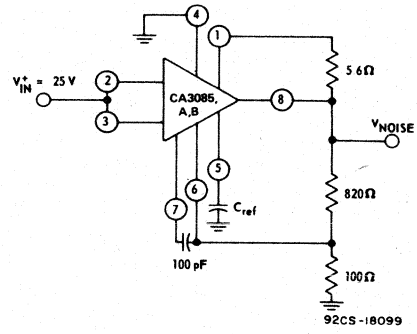


Fig.11—Test circuit for noise voltage.

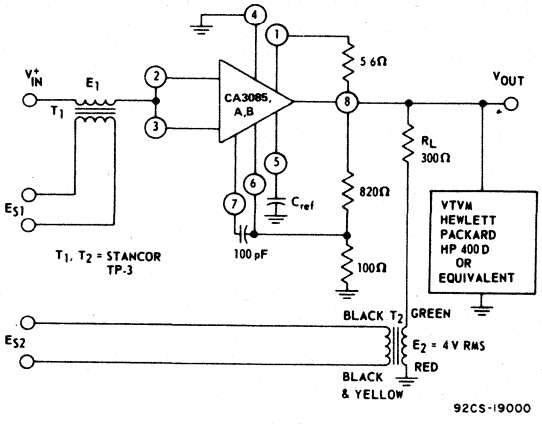


Fig.12—Test circuit for ripple rejection and output resistance.

TEST PROCEDURES FOR TEST CIRCUIT FOR RIPPLE REJECTION AND OUTPUT RESISTANCE

Output Resistance

Conditions:

1. V_{IN} = +25V, C_{REF} = 0, Short E_1
2. Set E_{S2} at 1 kHz so that E_2 = 4V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate R_{OUT} from $R_{OUT} = V_{OUT}(R_L/E_2)$

Ripple Rejection — I

Conditions:

1. V_{IN} = +25V, C_{REF} = 0, Short E_2
2. Set E_{S1} at 1 kHz so that E_1 = 3V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate Ripple Rejection from 20 log (E_1/V_{OUT})

Ripple Rejection — II

Conditions:

1. Repeat Ripple Rejection I with C_{REF} = 2 μF

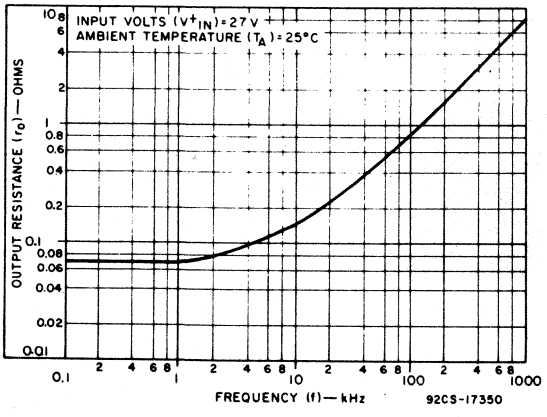


Fig.13—r_O vs. f.

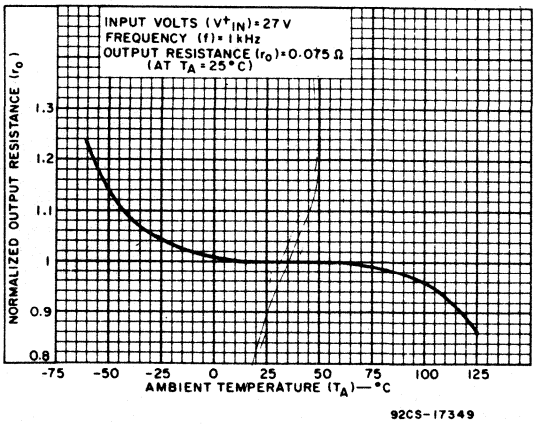


Fig.14—Normalized r_O vs. T_A.

CA3085, CA3085A, CA3085B Types

TEST CIRCUIT AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES

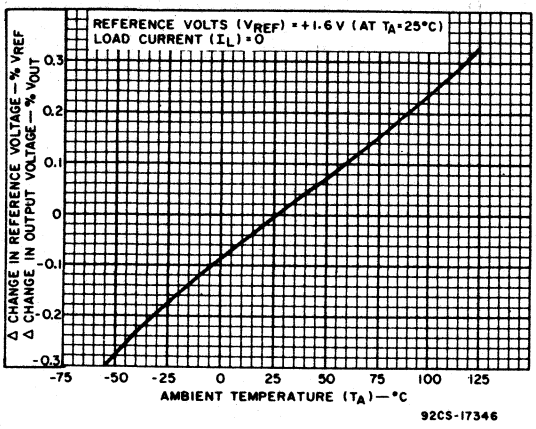


Fig.15—Temperature coefficient of V_{REF} and V_{OUT}.

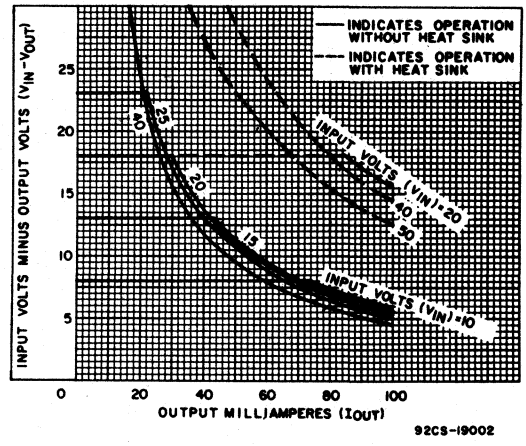
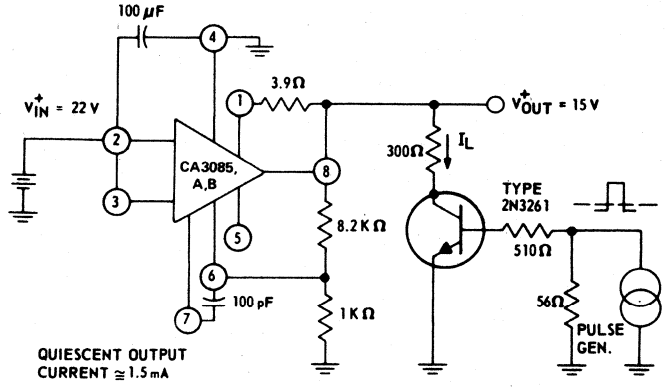


Fig.17—Dissipation limitation (V_{IN}—V_{OUT} vs. I_{OUT}).



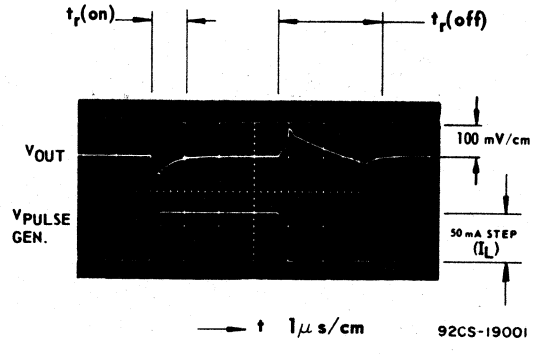


Fig.16—Turn-on and turn-off recovery time test circuit with associated waveforms.

TYPICAL REGULATOR CIRCUITS USING THE CA3085 SERIES

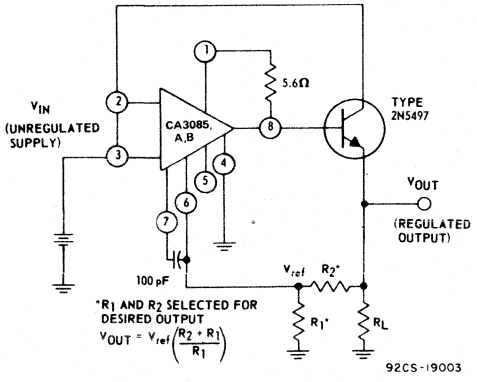


Fig.18—Typical high-current voltage regulator circuit.

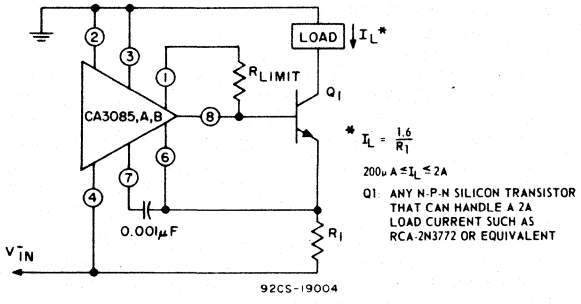
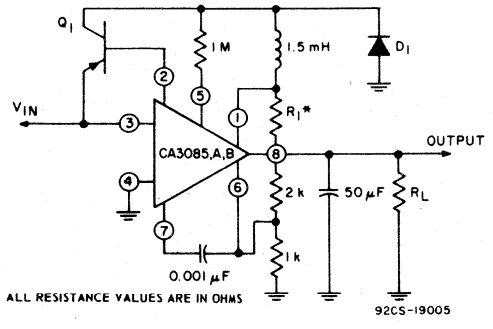
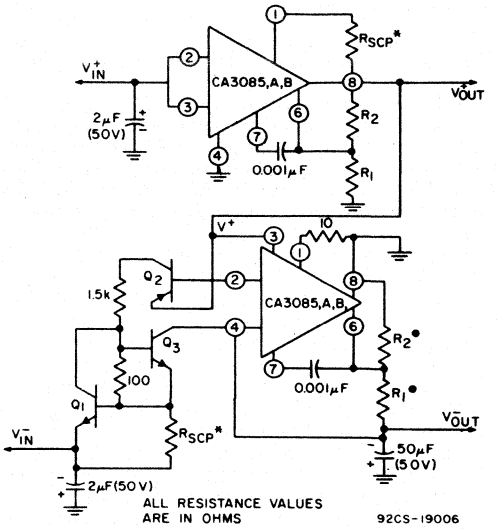


Fig.19—Typical current regulator circuit.



D1: RCA-1N1763A OR EQUIVALENT
Q1: RCA-2N5322 OR EQUIVALENT
*R1 = 0.7 I_L (MAX.)

Fig.20—Typical switching regulator circuit.



ALL RESISTANCE VALUES ARE IN OHMS

Q1: RCA-2N2102 OR EQUIVALENT
Q2: ANY P-N-P SILICON TRANSISTOR (RCA-2N5322 OR EQUIVALENT)
Q3: ANY N-P-N SILICON TRANSISTOR THAT CAN HANDLE THE DESIRED LOAD CURRENT (RCA-2N3772 OR EQUIVALENT)

*$V_{OUT} = \left(\frac{R_1 + R_2}{R_1}\right)$

*R_{SCP}: SHORT-CIRCUIT PROTECTION RESISTANCE

Fig.21—Combination positive and negative voltage regulator circuit.

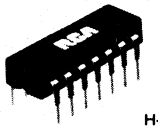
CA3058, CA3059, CA3079

CA3058

H-1553

14-Lead Dual-In-Line Ceramic Package

CA3059
CA3079



H-1517

14-Lead Dual-In-Line Plastic Package

Zero-Voltage Switches

For 50/60 and 400 Hz Thyristor Control Applications

Applications:

- *Relay control*
- *Valve control*
- *Synchronous switching of flashing lights*
- *On-off motor switching*
- *Differential comparator with self-contained power supply for industrial applications*
- *Photosensitive control*
- *Power one-shot control*
- *Heater control*
- *Lamp control*

The RCA-CA3058, CA3059, and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24 V, 120 V, 208/230 V, and 277 V at 50/60 and 400 Hz. Each of the zero-voltage switches incorporates 4 functional blocks (see Fig. 1) as follows:

1. Limiter-Power Supply — Permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier — Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.
3. Zero-Crossing Detector — Synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point; thereby eliminating radio-frequency interference (RFI) when used with resistive loads.
4. Triac Gating Circuit — Provides high-current pulses to the gate of the power controlling thrysistor.

In addition, the CA3058 and CA3059 provide the following important auxiliary functions (see Fig. 1):

1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

For an explanation of these functions see Operating Considerations, page 11. For detailed application information, see companion Application Note, ICAN-6182, "Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3058, CA3059, and CA3079)".

The CA3058 is supplied in a hermetic 14-lead dual-in-line ceramic package. Types CA3059 and CA3079 are supplied in 14-lead dual-in-line plastic packages. The CA3079 is also available in chip form (H suffix).

Features	CA3058	CA3059	CA3079
24V, 120V, 208/230V, 277V at 50 60, or 400 Hz operation	√	√	√
Differential Input	√	√	√
Low Balance Input Current (max.) -μA	1	1	2
Built-in Protection Circuit for opened or shorted sensor (Term. 14)	√	√	
Sensor Range (Rx) - kΩ	2 to 100	2 to 100	2 to 50
DC Mode (Term 12)	√	√	
External Trigger (Term 6)	√	√	
External Inhibit (Term 1)	√	√	
DC Supply Volts (max.)	14	14	10
Operating Temperature Range - °C		-55 to +125	

MAXIMUM RATINGS,
Absolute-Maximum Values at $T_A = 25^oC$

DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 7):
- CA3058, CA3059 ..... 14 V
- CA3079 ..... 10 V

DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 8):
- CA3058, CA3059 ..... 14 V
- CA3079 ..... 10 V

PEAK SUPPLY CURRENT (TERMS. 5 AND 7) ..... ±50 mA

OUTPUT PULSE CURRENT (TERM. 4) ..... 150 mA

POWER DISSIPATION:
- Up to T_A=75°C – CA3058 ..... 700 mW
- Up to T_A=55°C – CA3059,CA3079 ... 700 mW
- Above T_A=75°C – CA3058 ..... Derate Linearly 8 mW/°C
- Above T_A=55°C – CA3059,CA3079 ..... Derate linearly 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating ..... –55 to +125°C
- Storage ..... –65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
- At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL NO.	1 Note 3	2	3	4	5 Note 1	6 Note 3	7	8	9	10	11	12 Note 3	13	14 Note 2,3	MAXIMUM CURRENT RATINGS I_{IN} mA	I_{OUT} mA
1 Note 3		*	*	*	*	15 0	10 -2	*	*	*	*	*	*	*	10	0.1
2			0 -15	0 -15	2 -14	0 -14	0 -14▲	0 -14▲	0 -14	0 -14	0 -14	* .	0 -14	0 -14	150	10
3				0 -15	*	*	*	*	*	*	*	*	*	*	*	*
4					*	2 -10	*	*	*	*	*	*	*	*	0.1	150
5 Note 1						*	7 -7	*	*	*	*	*	*	*	50	10
6 Note 3							14 0	*	*	*	*	*	*	*	*	*
7								*	14 0	*	20 0	2.5 -2.5	14 0	6 -6	*	*
8									10 0	*	*	*	*	*	0.1	2
9										*	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12 Note 3													*	*	50	50
13														*	*	*
14 Note 3															2	2

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to –10 volts.

Note 1 – Resistance should be inserted between Terminal 5 and external supply or line voltage for limiting current into Terminal 5 to less than 50 mA.

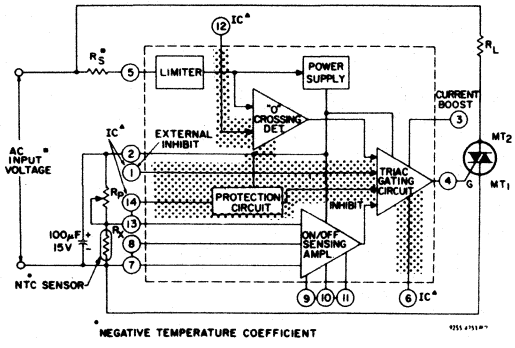
Note 2 – Resistance should be inserted between Terminal 14 and external supply for limiting current into Terminal 14 to less than 2 mA.

Note 3 – For the CA3079 indicated terminal is internally connected and, therefore, should not be used.

▲For CA3079 (0 to –10 V).

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

CA3058, CA3059, CA3079



AC Input Voltage (50/60 or 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE:

Circuitry, within shaded areas, not included in CA3079

■ See chart

▲ IC = Internal Connection - - DO NOT USE (Terminal Restriction applies only to CA3079).

Fig. 1–Functional block diagram of CA3058, CA3059, and CA3079.

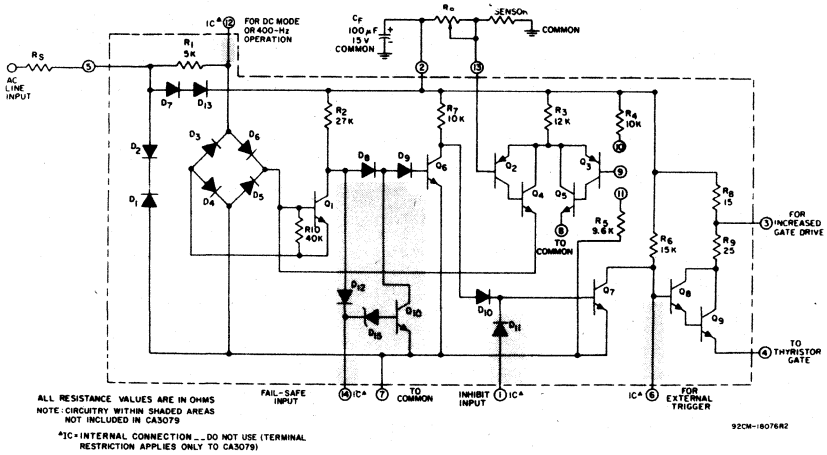


Fig. 2–Schematic diagram of CA3058, CA3059, and CA3079.

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise)

All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS T_A = 25°C (Unless Indicated Otherwise)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)●					
DC Supply Voltage, V_S					
Inhibit Mode					
At 50/60 Hz	R_S = 8 kΩ, I_L = 0	6.1	6.5	7	V
At 400 Hz	R_S = 10 kΩ, I_L = 0	–	6.8	–	V
At 50/60 Hz	R_S = 5 kΩ, I_L = 2 mA	–	6.4	–	V
Pulse Mode					
At 50/60 Hz	R_S = 8 kΩ, I_L = 0	6	6.4	7	V
At 400 Hz	R_S = 10 kΩ, I_L = 0	–	6.7	–	V
At 50/60 Hz	R_S = 5 kΩ, I_L = 2 mA	–	6.3	–	V
At 50/60 Hz (CA3058) *See Fig. 3*	R_S = 8 kΩ, I_L = 0; T_A = –55 to +125°C	5.5	–	7.5	V

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise) (Cont'd)
All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS T_A = 25°C (Unless Indicated Otherwise)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)●					
Gate Trigger Current, I_{GT}(4) *See Figs. 4, 5(a)*	Terms. 3 and 2 connected, V_{GT} = 1 V	–	105	–	mA
Peak Output Current (Pulsed), I_{OM}(4) With Internal Power Supply	Term. 3 open, Gate Trigger Voltage (V_{GT}) = 0	50	84	–	mA
	Terms. 3 and 2 connected, Gate Trigger Voltage (V_{GT})=0	90	124	–	mA
With External Power Supply	Term. 3 open, V^+=12 V, V_{GT}=0	–	170	–	mA
See Figs. 5, 6	Terms. 3 and 2 connected, V^+=12 V, V_{GT} = 0	–	240	–	mA
Inhibit Input Ratio, V_9/V_2 All Types	Voltage Ratio of Term. 9 to 2	0.465	0.485	0.520	–
CA3058 *See Fig. 7*	T_A = –55 to +125°C	0.450	–	0.520	–
Total Gate Pulse Duration:* For positive dv/dt, t_P 50-60 Hz	C_{EXT} = 0	70	100	140	μs
400 Hz	C_{EXT} = 0, R_{EXT} = ∞	–	12	–	μs
For negative dv/dt, t_N 50-60 Hz	C_{EXT} = 0	70	100	140	μs
400 Hz *See Fig. 8*	C_{EXT} = 0, R_{EXT} = ∞	–	10	–	μs
Pulse Duration After Zero Crossing (50-60 Hz): For positive dv/dt, t_{P1}	C_{EXT} = 0	–	50	–	μs
For negative dv/dt, t_{N1} *See Fig. 8*	R_{EXT} = ∞	–	60	–	μs
Output Leakage Current, I_4 Inhibit Mode: All Types		–	0.001	10	μA
CA3058 *See Fig. 9*	T_A = –55 to +125°C	–	–	20	μA
Input Bias Current, I_I CA3058, CA3059		–	220	1000	nA
CA3079 *See Fig. 10*		–	220	2000	nA
Common-Mode Input Voltage Range, V_{CMR}	Terms. 9 and 13 connected	–	1.5 to 5	–	V
Sensitivity, $\Delta V_{13}^{\neq}$ (Pulse Mode) *See Figs. 5(a), 12*	Term. 12 open	–	6	–	mV

≠Required voltage change at Term. 13 to either turn OFF the triac when ON or turn ON the triac when OFF.

*Pulse duration in 50 Hz applications is approximately 15% longer than shown in Fig. 8(b).

● The values given in the Electrical Characteristics Chart at 120 V also apply for operation at input voltages of 24 V, 208/230 V, and 277 V, except for Pulse Duration. However, the series resistor (R_S) must have the indicated value, shown in the chart in Fig. 1, for the specified input voltage.

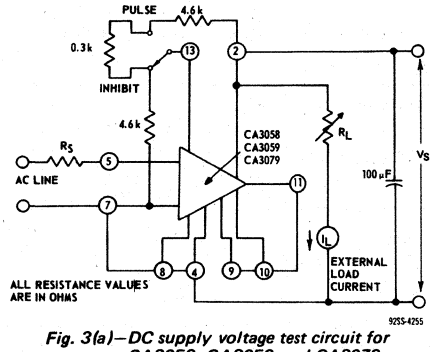


Fig. 3(a)—DC supply voltage test circuit for CA3058, CA3059, and CA3079.

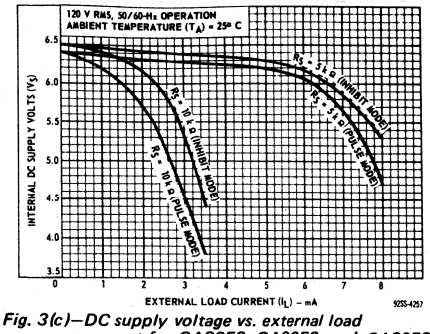


Fig. 3(c)—DC supply voltage vs. external load current for CA3058, CA3059, and CA3079.

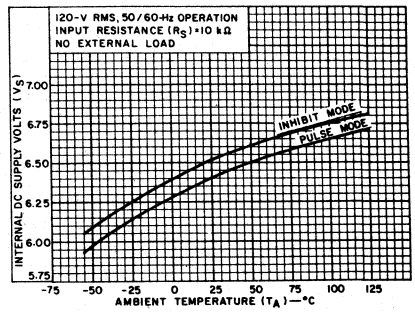


Fig. 3(b)—DC supply voltage vs. ambient temperature for CA3058, CA3059, and CA3079.

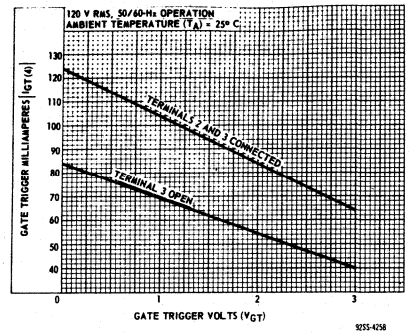


Fig. 4—Gate trigger current vs. gate trigger voltage for CA3058, CA3059, and CA3079.

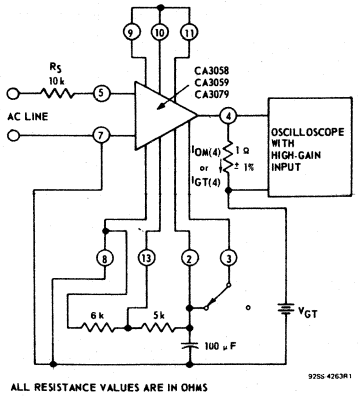


Fig. 5(a)—Peak output (pulsed) and gate trigger current with internal power supply test circuit for CA3058, CA3059, and CA3079.

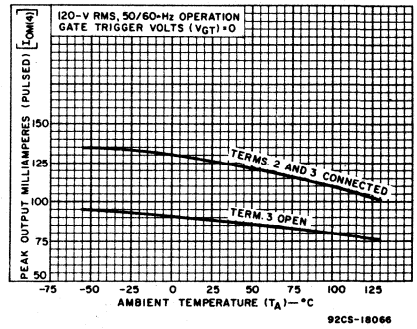


Fig. 5(b)—Peak output current (pulsed) vs. ambient temperature for CA3058, CA3059, and CA3079.

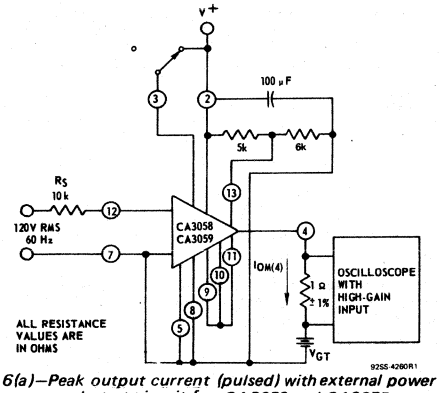


Fig. 6(a)—Peak output current (pulsed) with external power supply test circuit for CA3058 and CA3059.

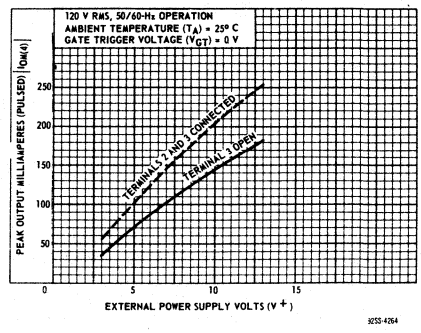


Fig. 6(b)—Peak output current (pulsed) vs. external power supply voltage for CA3058 and CA3059.

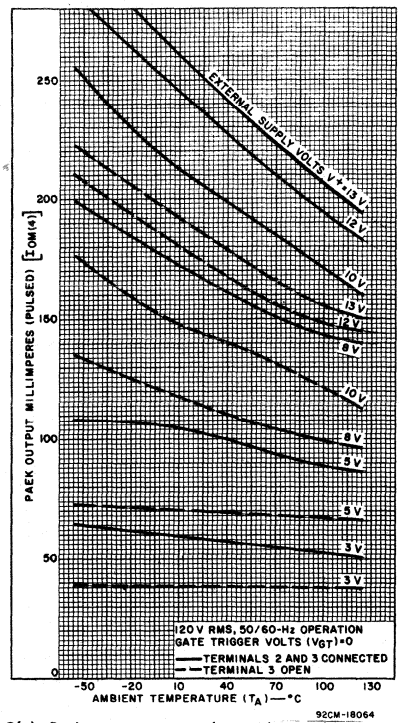


Fig. 6(c)—Peak output current (pulsed) vs. ambient temperature for CA3058 and CA3059.

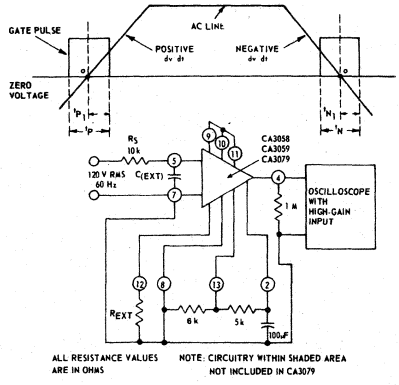


Fig. 8(a)—Gate pulse duration test circuit with associated waveform for CA3058, CA3059, and CA3079.

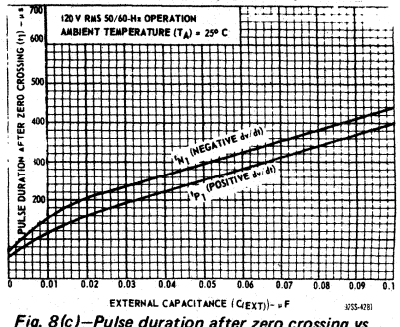


Fig. 8(c)—Pulse duration after zero crossing vs. external capacitance for CA3058, CA3059, and CA3079.

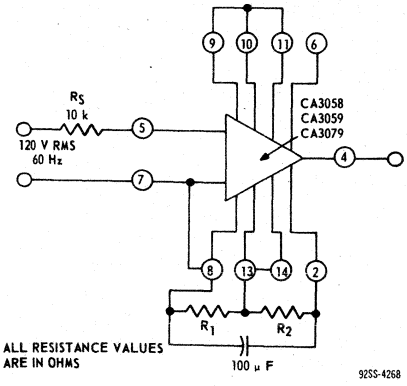


Fig. 7(a)—Input inhibit voltage ratio test circuit for CA3058, CA3059, and CA3079.

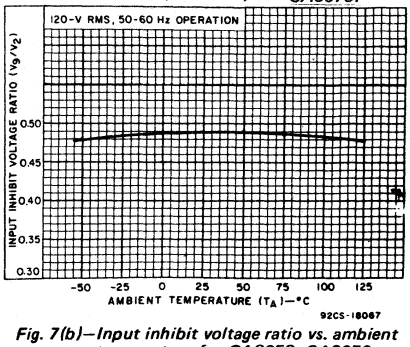


Fig. 7(b)—Input inhibit voltage ratio vs. ambient temperature for CA3058, CA3059, and CA3079.

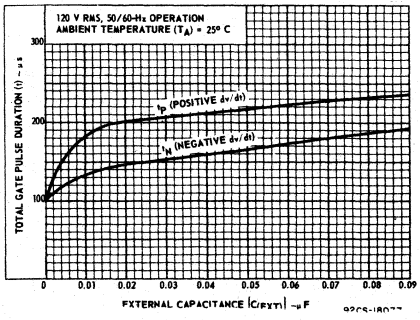


Fig. 8(b)—Total gate pulse duration vs. external capacitance for CA3058, CA3059, and CA3079.

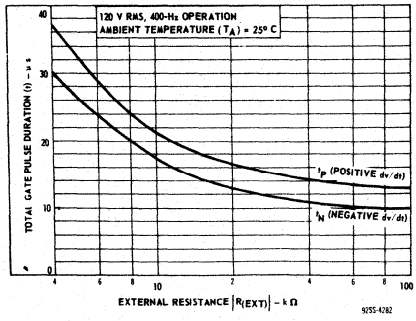


Fig. 8(d)—Total gate pulse duration vs. external resistance for CA3058 and CA3059.

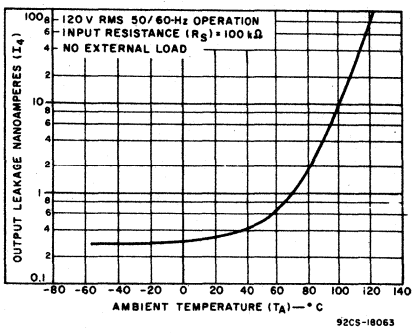


Fig. 9—Output leakage current (inhibit mode) vs. ambient temperature for CA3058, CA3059, and CA3079.

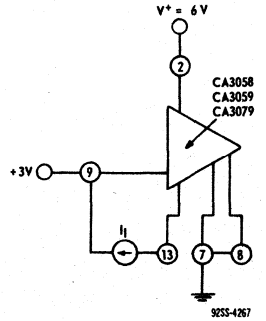
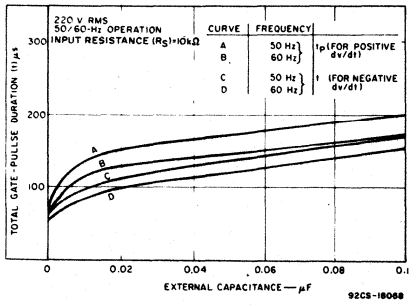
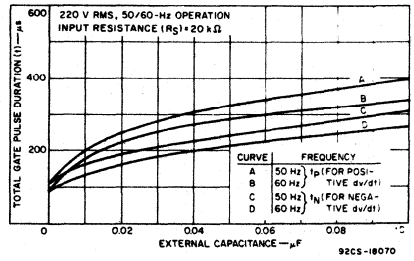


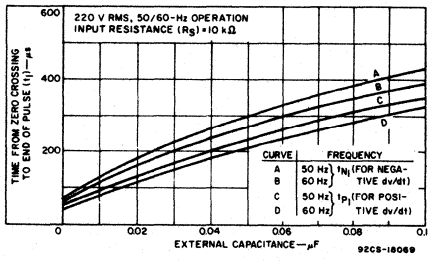
Fig. 10—Input bias current test circuit for CA3058, CA3059, and CA3079.



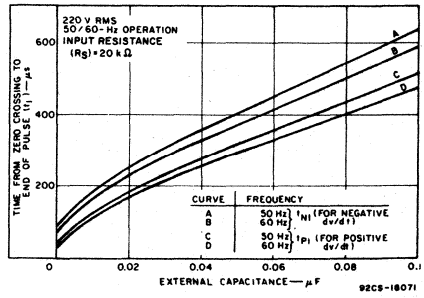
(a)



(b)



(c)



(d)

Fig. 11—Relative pulse width and location of zero crossing for 220-volt operation for CA3058, CA3059, and CA3079.

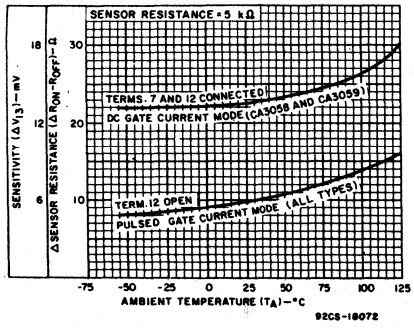


Fig. 12—Sensitivity vs. ambient temperature for CA3058, CA3059, and CA3079.

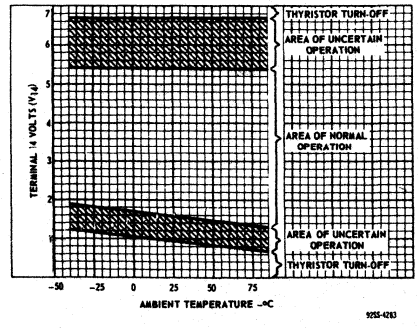


Fig. 13—Operating regions for built-in protection circuit for CA3058 and CA3059.

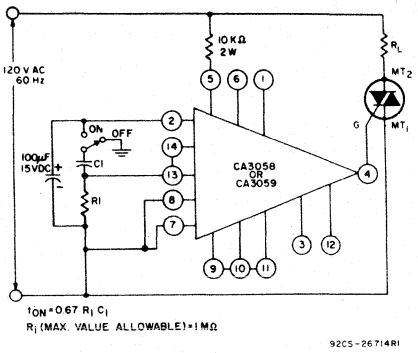


Fig. 14—Line-operated one-shot timer.

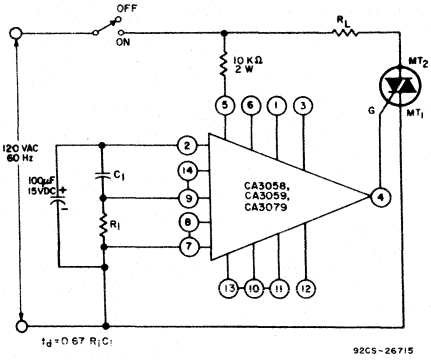


Fig. 15—Line-operated thyristor control time delay turn-on circuit.

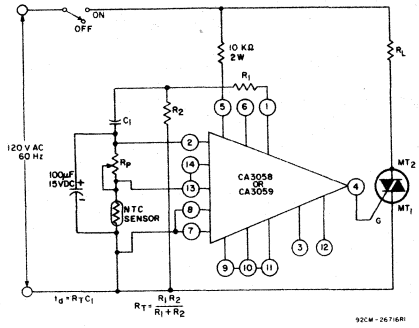


Fig. 16—On/off temperature control circuit with delayed turn-on.

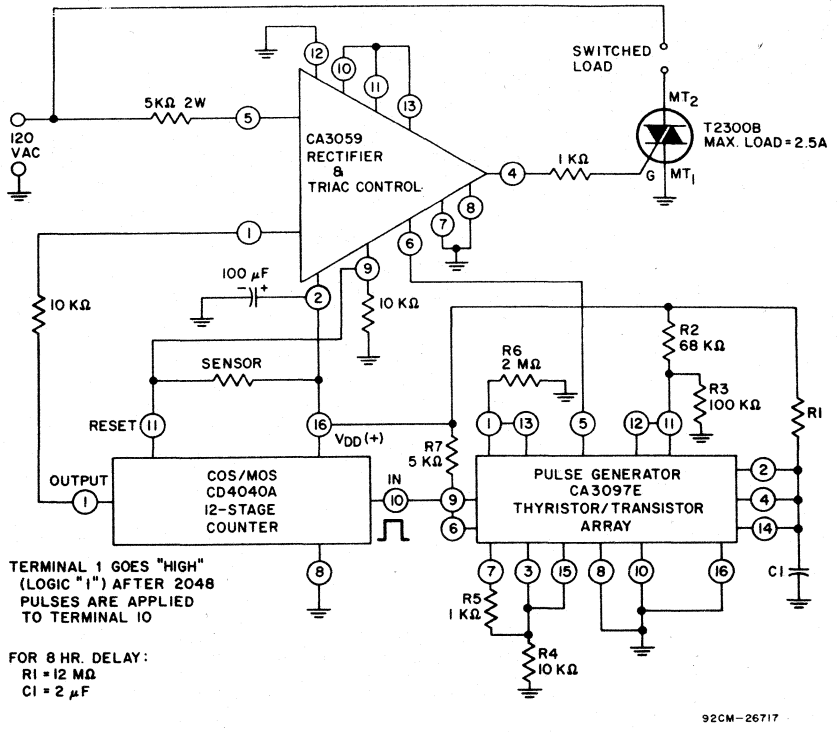


Fig. 17(a)—Line-operated IC timer for long time periods.

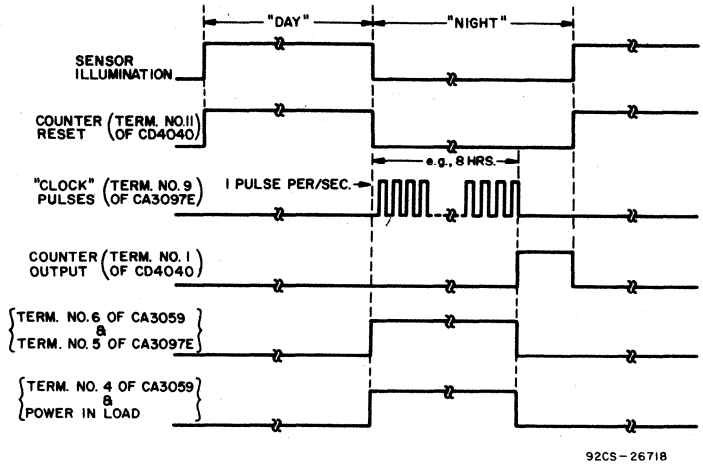


Fig. 17(b)—Timing diagram for Fig. 17(a).

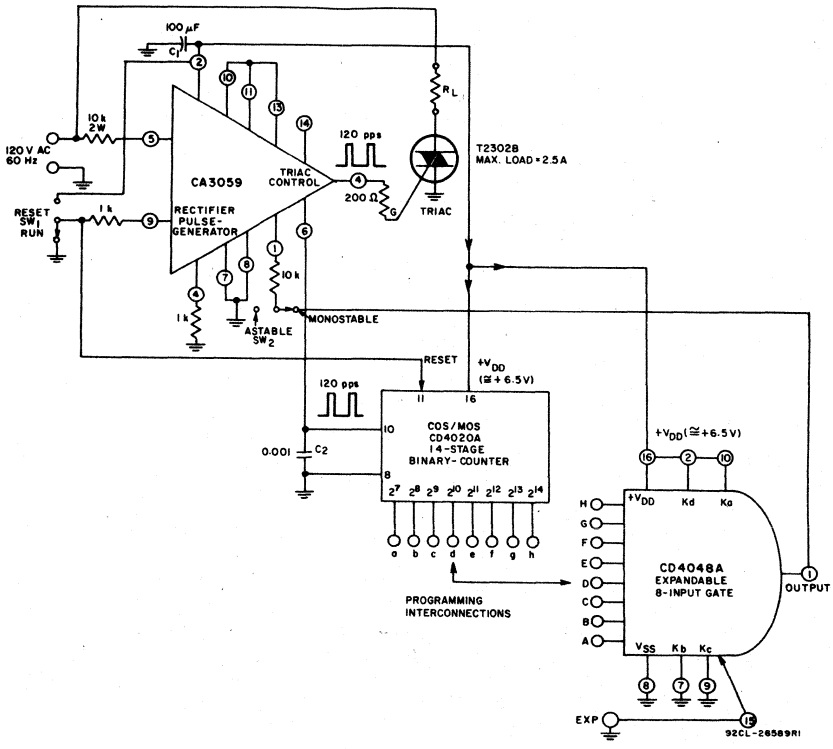


Fig. 18(a)—Programmable ultra-accurate line-operated timer. (Programmable over the range from 0.5333 seconds to 2 minutes, 16 seconds in 0.5333-second increments)

Time Periods (t = 0.5333 s)	1 t	2 t	4 t	8 t	16 t	32 t	64 t	128 t	t_o
Terminals									
CD4020A	a	b	c	d	e	f	g	h	
CD4048A	A	B	C	D	E	F	G	H	
	C	NC	NC	NC	NC	NC	NC	NC	1 t
	NC	C	NC	NC	NC	NC	NC	NC	2 t
	C	C	NC	NC	NC	NC	NC	NC	3 t
	NC	NC	C	NC	NC	NC	NC	NC	4 t
	C	NC	C	NC	NC	NC	NC	NC	5 t
	NC	C	C	NC	NC	NC	NC	NC	6 t
	C	C	C	NC	NC	NC	NC	NC	7 t
	NC	NC	NC	C	NC	NC	NC	NC	8 t
	C	NC	NC	C	NC	NC	NC	NC	9 t
	NC	C	NC	C	NC	NC	NC	NC	10 t
	C	C	NC	C	NC	NC	NC	NC	11 t
	NC	NC	C	C	NC	NC	NC	NC	12 t
	C	NC	C	C	NC	NC	NC	NC	13 t
	NC	C	C	C	NC	NC	NC	NC	14 t
	C	C	C	C	NC	NC	NC	NC	15 t
	C	C	C	C	NC	C	C	NC	111 t
	NC	NC	NC	NC	C	C	C	NC	112 t
	C	NC	NC	NC	C	C	C	NC	113 t
	C	C	C	C	C	C	C	C	255 t

Notes:

t_o = Total time delay = $n_1 t + n_2 t + \ldots n_n t$.

C = Connect. For example, interconnect terminal a of the CD4020A and terminal A of the CD4048A.

NC = No Connection. For example, terminal b of the CD4020A open and terminal B of the CD4048A connected to $+V_{DD}$ bus.

Fig. 18(b)—"Programming" table for Fig. 18(a).

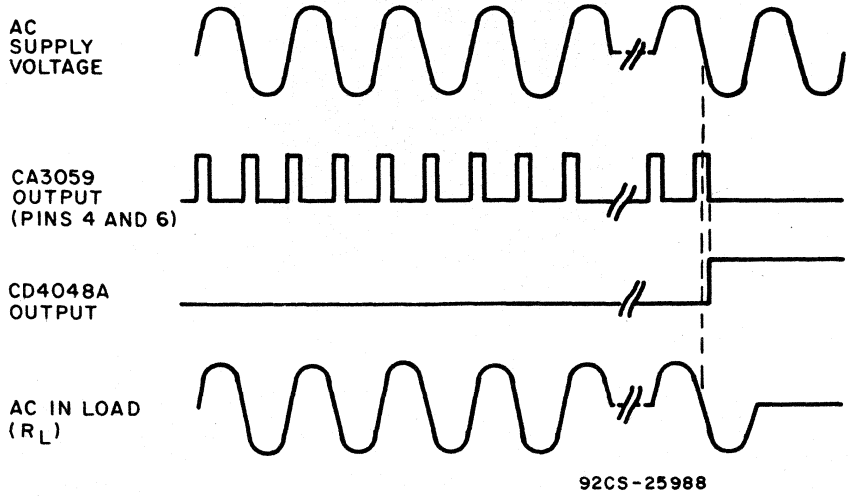


Fig. 18(c)—Timing diagram for Fig. 18(a).

OPERATING CONSIDERATIONS

Power Supply Considerations for CA3058, CA3059, and CA3079

The CA3058, CA3059, and CA3079 are intended for operation as self-powered circuits with the power supplied from an AC line through a dropping resistor. The internal supply is designed to allow for some current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figs. 3(b) and 3(c).

Power Supply Considerations for CA3058 and CA3059

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Fig. 5 for the peak output current characteristics). When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Fig. 5(a).

Operation of Built-in Protection for the CA3058, CA3059

A special feature of the CA3058 and CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in Fig. 1. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2 mA with a 5 kΩ dropping resistor.
2. Set the value of R_P and sensor resistance (R_X) between 2 kΩ and 100 kΩ.
3. The ratio of R_X to R_P, typically, should be greater than 0.33 and less than 3. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series or shunt resistor must be added to avoid undesired activation of the circuit.

If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Fig. 13.

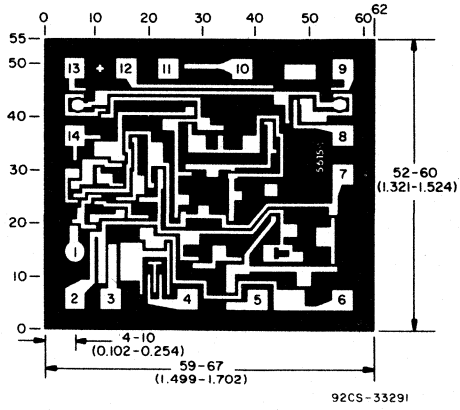
External Inhibit Function for the CA3058 and CA3059

A priority inhibit command may be applied to Terminal 1. The presence of at least +1.2 V at 10 μA will remove drive from the thyristor. This required level is compatible with DTL or T^2L logic. A logical 1 activates the inhibit function.

DC Gate Current Mode for the CA3058 and CA3059

Connecting Terminals 7 and 12 disables the zero-crossing detector and permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be exercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.

For a list of RCA thyristors, see RCA Thyristor Data Bulletin, File No. 406, dated 5-75.



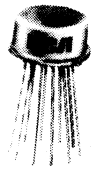
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid gradations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CA3059H.

Differential Amplifiers
Technical Data

CA3000



10-Lead TO-5

H-1384

DC Amplifier

Features:

- *Designed for use in Communication, Telemetry, Instrumentation, and Data-Processing Equipment*
- *Balanced differential-amplifier configuration with controlled constant-current source to provide outstanding versatility*
- *Built-in temperature stability for operation from −55°C to +125°C*
- *Companion Application Note, ICAN 5030 "Applications of RCA CA3000 Integrated Circuit DC Amplifier" covers characteristics of different operating modes, frequency considerations, 10 MHz narrow band tuned amplifier design, crystal oscillator design, and many other application aids*
- *Input impedance - 195 kΩ typ.*
- *Voltage gain - 37 dB typ.*
- *Common-mode rejection ratio - 98 dB typ.*
- *Input offset voltage - 1.4 mV typ.*
- *Push-pull input and output*
- *Frequency capability - DC to 30 MHz (with external C and R)*
- *Wide AGC range - 90 dB typ.*

Applications

- *Schmitt trigger*
- *RC-coupled feedback amplifier*
- *Mixer*
- *Comparator*
- *Modulator*
- *Crystal oscillator*
- *Sense amplifier*

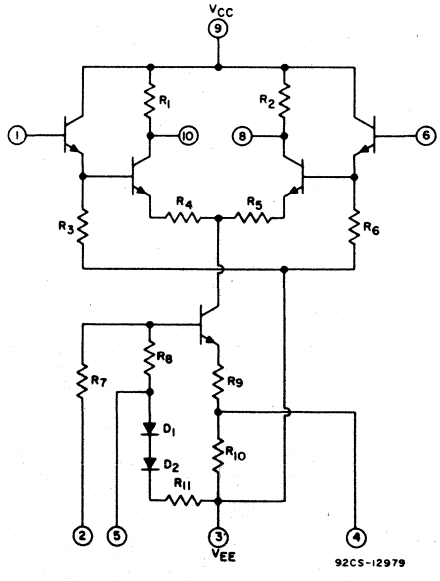


Fig. 1 — Schematic Diagram

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_A = 25°C

Indicated voltage limits for each terminal can be used under specified voltage conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2	+2	2	0
			3	-6
			6	0
			9	+6
2	-8	0	1	0
			3	-8
			6	0
			9	+6
3	-10	0	1	0
			2	0
			6	0
			9	+6
4	-8	0	1	0
			2	0
			6	0
			9	+6
5	-6	0	1	0
			2	0
			3	-6
			6	0
			9	+6

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
6	-2	+2	1	0
			2	0
			3	-6
			9	+6
7	NO CONNECTION			
8	0	+6	1	0
			2	0
			3	-6
			6	0
9	0	+10	1	0
			2	0
			3	-6
			6	0
10	0	+6	1	0
			2	0
			3	-6
			6	0
CASE	Internally Connected to Terminal No.3 (Substrate) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE	-55°C to +125°C
STORAGE-TEMPERATURE RANGE	-65°C to +150°C
LEAD TEMPERATURE (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	± 4 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	± 2 V
MAXIMUM DEVICE DISSIPATION:	
From -55°C to 85°C	450
Above 85°C	Derate 5 mW/°C

CA3000

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V_{CC} = +6V, V_{EE} = -6V, unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 & No.5 Not Connected Unless Specified		TEST CIRCUITS	LIMITS TYPE CA3000				TYPICAL CHARACTERISTICS CURVES
				Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS									
Input Offset Voltage	V_{IO}				-	1.4	5	mV	2
Input Offset Current	I_{IO}				-	1.2	10	μA	2
Input Bias Current	I_{IB}				-	23	36	μA	3
Quiescent Operating Voltage	V_8 or V_{IO}	TERMINALS 4	5						
		NC	NC		-	2.6	-	V	4
		NC	VEE		-	4.2	-	V	4
		VEE	NC		-	-1.5	-	V	4
		VEE	VEE		-	0.6	-	V	4
Device Dissipation	P_D	NC	NC		-	30	-	mW	NONE
DYNAMIC CHARACTERISTICS									
Differential Voltage Gain Single-Ended Input	A_{DIFF}	Single-Ended Output f = 1 kHz		9	28	32	-	dB	5
		Double-Ended Output f = 1 kHz		9	-	38	-	dB	5
Bandwidth at -3 dB Point	BW	V_I = 10 mV, R_S = 1 kΩ			-	650	-	kHz	7
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	f = 1 kHz		9	-	6.4	-	V(P-P)	NONE
Common-Mode Rejection Ratio	CMRR	f = 1 kHz		13	70	98	-	dB	8
Single-Ended Input Impedance	Z_{IN}	f = 1 kHz		15	70K	195K	-	Ω	10
Single-Ended Output Impedance	Z_{OUT}	f = 1 kHz		17	5.5K	8K	10.5K	Ω	12
Total Harmonic Distortion	THD	R_S=1kΩ f = 1 kHz V_O=42V_{p-p}			-	0.2	5	%	14
AGC Range (Maximum Voltage Gain to Complete Cutoff)	AGC	f = 1 kHz		20	80	90	-	dB	NONE

STATIC CHARACTERISTICS

INPUT OFFSET VOLTAGE AND CURRENT vs TEMPERATURE

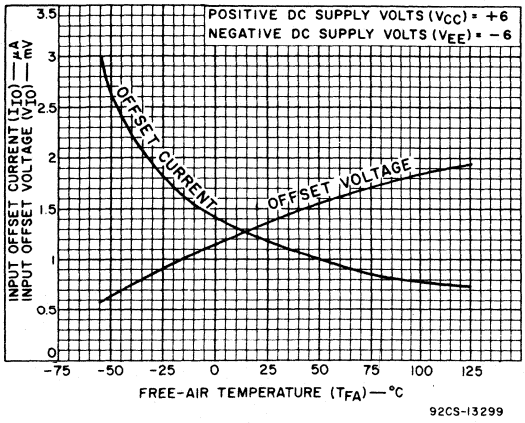


Fig.2

INPUT BIAS CURRENT vs TEMPERATURE

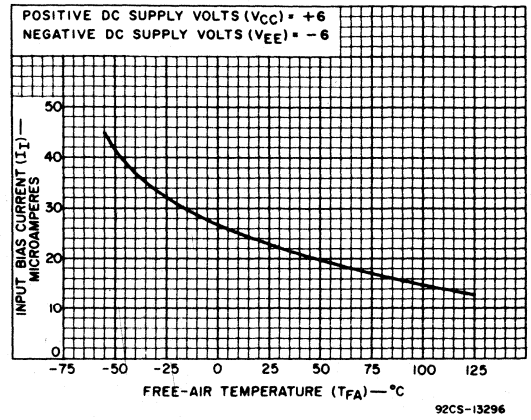


Fig.3

STATIC CHARACTERISTICS

QUIESCENT OPERATING VOLTAGE vs TEMPERATURE

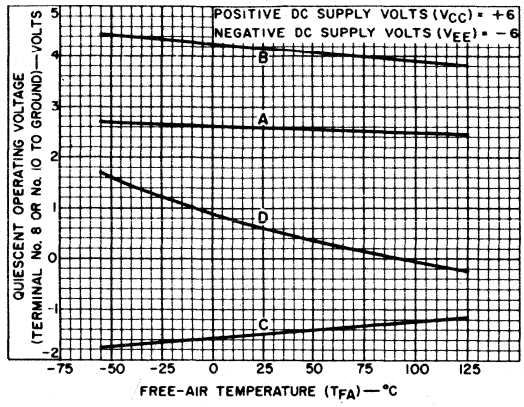


Fig. 4

DYNAMIC CHARACTERISTICS AND TEST CIRCUIT FOR TYPE CA3000

DIFFERENTIAL VOLTAGE GAIN vs TEMPERATURE

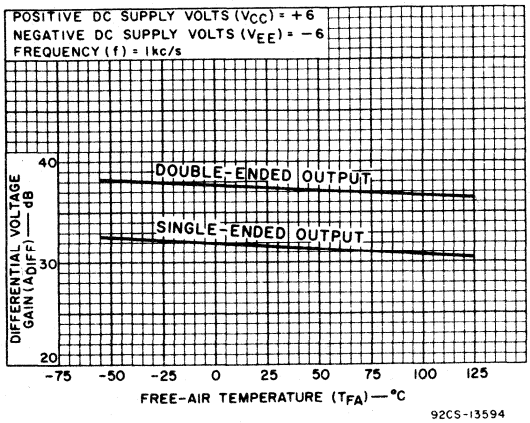


Fig. 5

DIFFERENTIAL VOLTAGE GAIN AND MAXIMUM OUTPUT VOLTAGE SWING TEST CIRCUIT

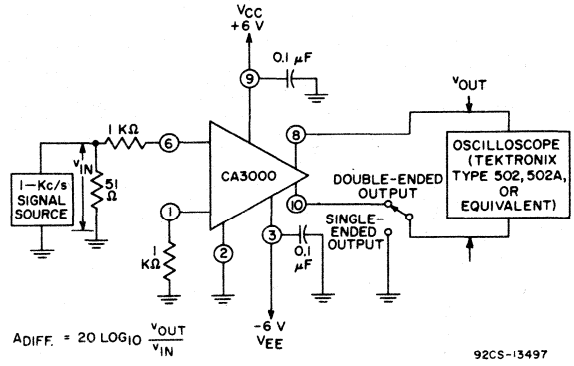


Fig. 6

DYNAMIC CHARACTERISTICS AND TEST CIRCUIT

BANDWIDTH AT -3 dB POINT vs TEMPERATURE

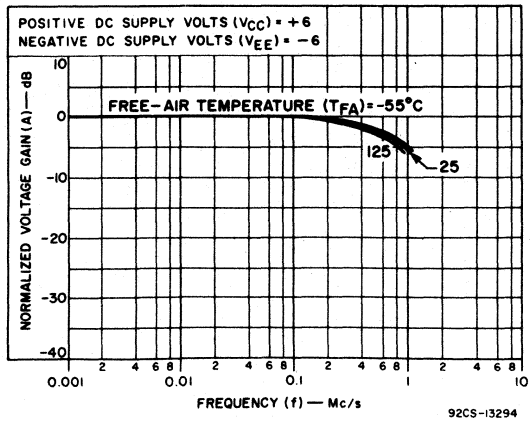


Fig. 7

COMMON-MODE REJECTION RATIO vs TEMPERATURE

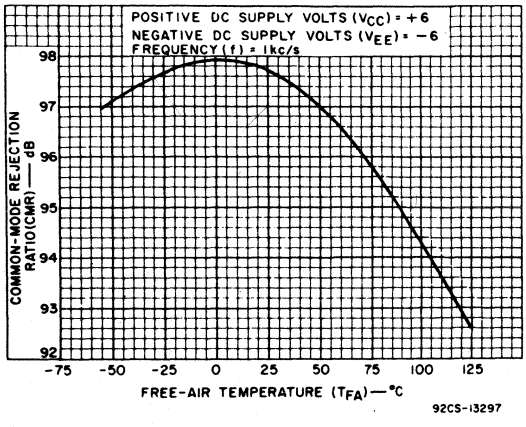
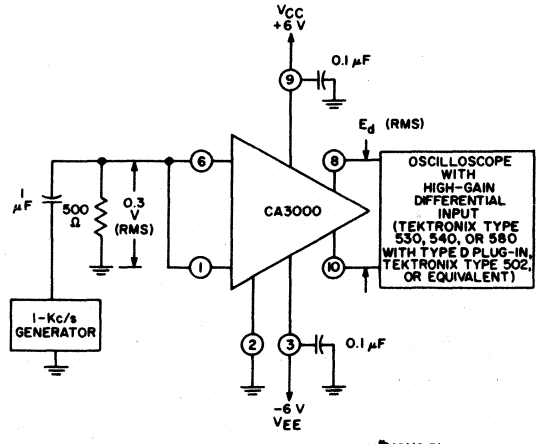


Fig. 8

COMMON-MODE REJECTION RATIO TEST CIRCUIT



COMMON-MODE REJECTION RATIO (CMR) = 20 log $\frac{(A^*)(2)(0.3)}{E_{d\,(RMS)}}$

*A = SINGLE-ENDED VOLTAGE GAIN

92CS-12983RI

Fig. 9

DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3000

SINGLE-ENDED INPUT IMPEDANCE vs TEMPERATURE

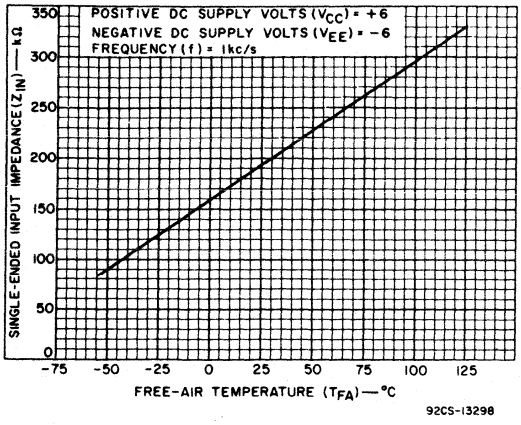


Fig. 10

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

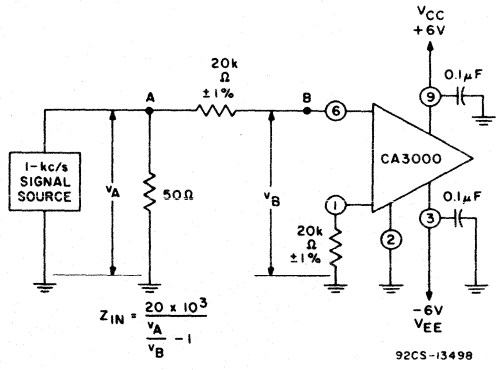


Fig. 11

SINGLE-ENDED OUTPUT IMPEDANCE vs TEMPERATURE

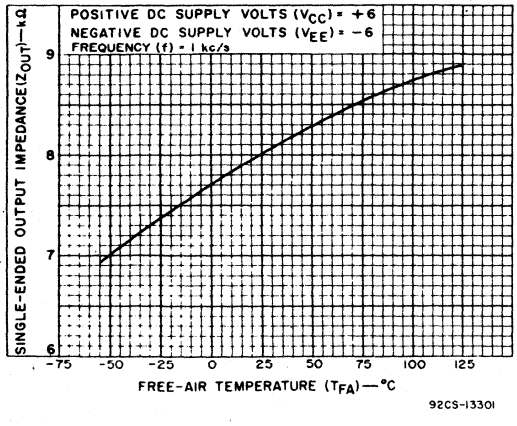
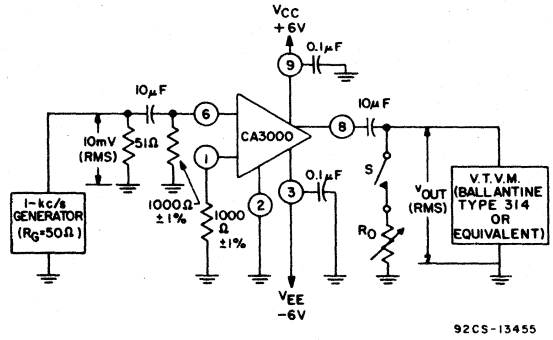


Fig. 12

SINGLE-ENDED OUTPUT IMPEDANCE TEST CIRCUIT



1. With Switch S open, record reference voltage V_{OUT}(rms).
2. Close Switch S, and adjust R_O until
$$V_{OUT} = \frac{\text{Reference Voltage}}{2}$$
3. Record value of R_O as Z_{OUT}.

Fig. 13

DYNAMIC CHARACTERISTICS AND TEST CIRCUIT

TOTAL HARMONIC DISTORTION vs TEMPERATURE

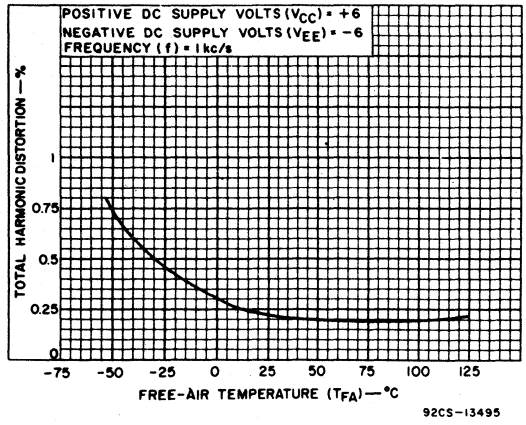
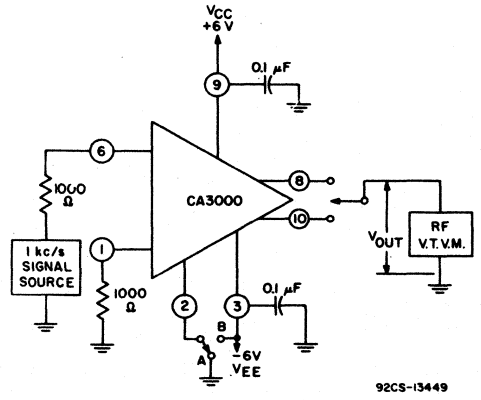


Fig. 14

AGC RANGE TEST CIRCUIT



$$\text{AGC Range} = 20 \log_{10} \frac{\text{A with S in Position A}}{\text{A with S in Position B}}$$

Fig. 15

12-Lead TO-5 Package

H-1463

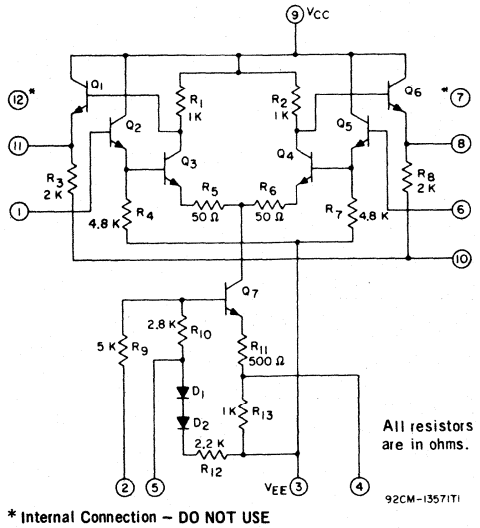
Video and Wide-band Amplifier

Features:

- *Designed for use in video systems and communication equipment*
- *Balanced differential amplifier configuration with controlled constant-current source provides outstanding versatility*
- *Built-in temperature stability for operation from −55° C to +125° C*
- *Emitter follower input & output*
- *Companion Application Note ICAN5038 "Application of the RCA-CA3001 Integrated-Circuit Video Amplifier", covers different operating modes, gain control, distortion, swing capability, 3 stage amplifier design, and a Schmitt trigger study.*
- *Push-pull input & output*
- *AGC range - 60 dB typ.*
- *Bandwidth - 29 MHz*
- *Input resistance - 150 kΩ typ.*
- *Output resistance - 45 Ω typ.*
- *Voltage gain - 19 dB typ.*
- *Input offset voltage - 1.5 mV typ.*

Applications

- *Schmitt trigger*
- *Mixer*
- *Modulator*
- *DC, IF & video amplifier*



* Internal Connection – DO NOT USE

Fig. 1 — Schematic Diagram.

CA3001

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS at T_A = 25°C

Indicated voltage or current limits for each terminal can be applied under the specified conditions for other terminals.
All Voltages are with respect to ground (common terminal of Positive and Negative DC Supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2, 6 3, 10 9	0 -6 +6
2	-8.5	0	1, 6 3, 10 9	0 -8.5 +6
3	-10	0	1, 2, 6 9 10	0 +6 -6
4	-8.5	0	1, 2, 6 9 10	0 +6 -6
5	-6	0	1, 2, 6 3, 10 9	0 -6 +6
6	-2.5	+2.5	1, 2 3, 10 9	0 -6 +6
7	INTERNAL CONNECTION DO NOT USE			

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.8 & No.10	0 -6 +6
9	0	+10	1, 2, 6, 10 3	0 -6
10	-10	0	1, 2, 6 3 9	0 -6 +6
11	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.10 & No.11	0 -6 +6
12	INTERNAL CONNECTION DO NOT USE			
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

OPERATING TEMPERATURE RANGE ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE ..... -65°C to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ±1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. ..... +265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE ..... ± 4 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE ..... ± 2.5 V
MAXIMUM DEVICE DISSIPATION:
-55 to 85°C ..... 450 mW
Above 85°C ..... Derate linearly 5 mW/°C

ELECTRICAL CHARACTERISTICS, AT T_A = 25°C, V_{CC} = +6V, V_{EE} = -6V

CHARACTERISTICS (See Page 2 for Definitions of Terms)	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 and No.5 Not Connected Unless Specified	TEST CIRCUITS	LIMITS TYPE CA3001				TYPICAL CHARACTERISTICS CURVES
			Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS:								
Input Offset Voltage	V_{IO}		4	-	1.5	-	mV	2
Input Offset Current	I_{IO}		5	-	1	10	μA	2
Input Bias Current	I_I		5	-	16	36	μA	3
Output Offset Voltage	V_{OO}	R_S = 1 kΩ		-	54	300	mV	6
Quiescent Operating Voltage	V_8 OR V_{11}	TERMINALS MODE A: 4 = NC, 5 = NC		3.8	4.4	5	V	7
		MODE B: 4 = NC, 5 = V_{EE}		-	4.8	-	V	7
		MODE C: 4 = V_{EE}, 5 = NC		-	2.7	-	V	7
		MODE D: 4 = V_{EE}, 5 = V_{EE}		-	4	-	V	7
Device Dissipation	P_D	A: 4 = NC, 5 = NC		60	78	120	mW	8
		B: 4 = NC, 5 = V_{EE}		-	71	-	mW	8
		C: 4 = V_{EE}, 5 = NC		-	110	-	mW	8
		D: 4 = V_{EE}, 5 = V_{EE}		-	86	-	mW	8
DYNAMIC CHARACTERISTICS:								
Differential Voltage Gain (Single-ended input and output)	A_{DIFF}	f = 1.75 MHz f = 20 MHz		16 10	19 14	- -	dB dB	9 A, 9 B 9 B
Bandwidth at -3 dB Point	BW	R_S = 50Ω		16	29	-	MHz	NONE
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	R_S = 50Ω f = 1.75 MHz		-	5	-	V_{P-P}	NONE
Noise Figure	NF	f = 1.75 MHz, R_S = 1 KΩ	14	-	5	8	dB	10
		f = 11.7 MHz, R_S = 1 KΩ	14	-	7.7	-	dB	10
Common-Mode Rejection Ratio	CMRR	f = 1 KHz	16	70	88	-	dB	12
Input Impedance Components:								
Parallel Input Resistance	R_{IN}	f = 1.75 MHz		50	140	-	KΩ	14
Parallel Input Capacitance	C_{IN}	f = 1.75 MHz		-	3.4	7	pF	14
Output Resistance	R_{OUT}	f = 1.75 MHz		-	45	70	Ω	NONE
AGC Range (Maximum voltage gain to complete cutoff)	AGC	f = 1.75 MHz	19	55	60	-	dB	NONE

TYPICAL STATIC CHARACTERISTICS

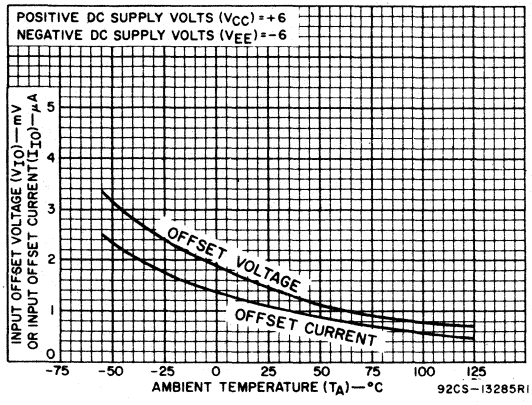


Fig.2 - Input offset voltage and current vs. temperature.

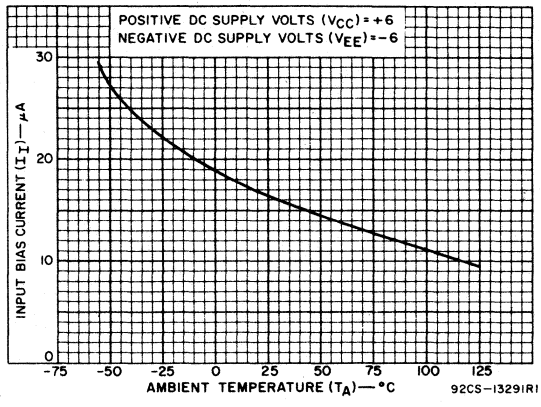
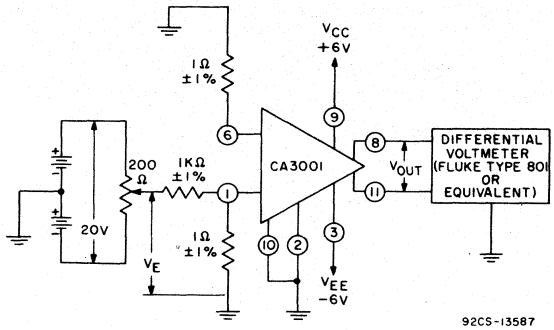


Fig.3 - Input bias current vs. temperature.

CA3001

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS



1. Adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ V 2. Measure V_E and record input offset voltage (V_{IO}) in mV as $V_{IO} = \frac{V_E}{1000}$

Fig.4 - Input offset voltage test circuit.

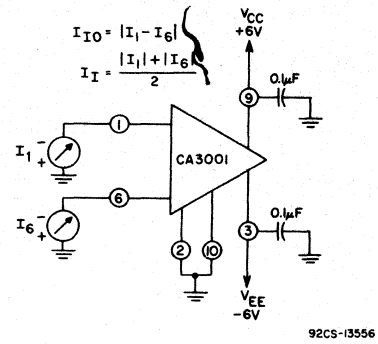


Fig.5 - Input offset current and input bias current test circuit.

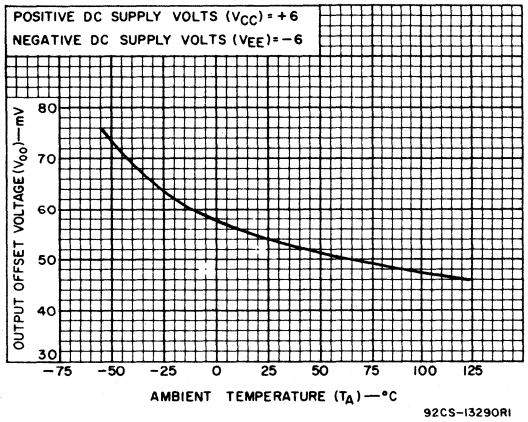


Fig.6 - Output offset voltage vs. temperature.

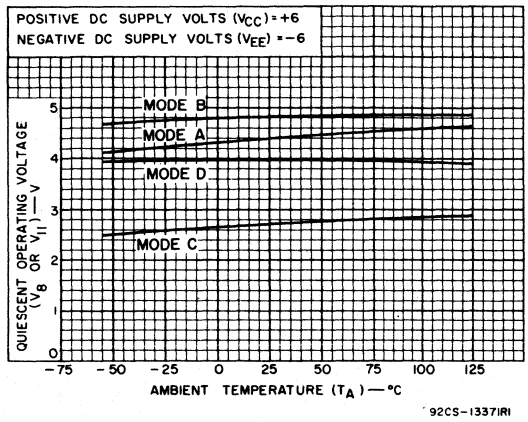


Fig.7 - Quiescent operating voltage vs. temperature.

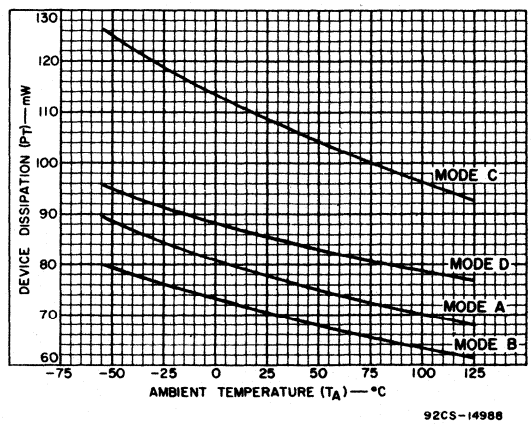


Fig.8 - Device dissipation vs. temperature.

TYPICAL DYNAMIC CHARACTERISTICS

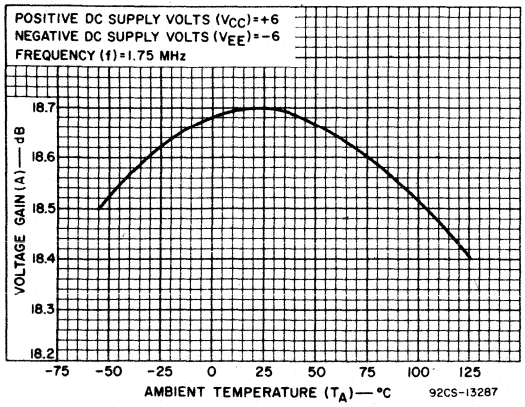


Fig.9a - Differential voltage gain vs. temperature.

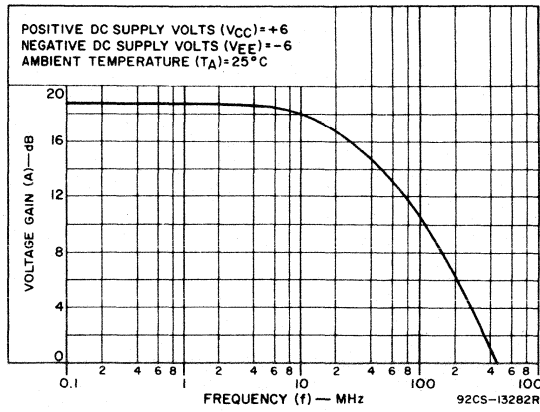


Fig.9 b - Differential voltage gain vs. frequency.

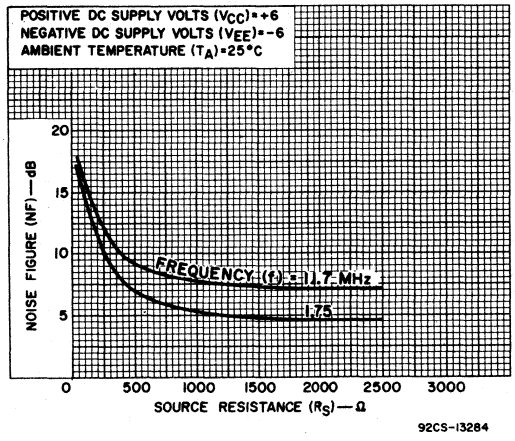
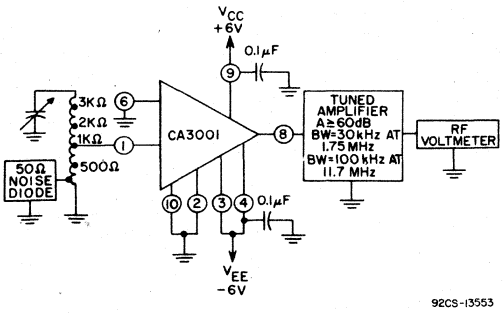


Fig.10 - Noise figure vs. source resistance and frequency.

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS



* Separate tuned input circuits are used for 1.75 MHz and 11.7 MHz. Source-resistance matching taps adjusted with circuit tuned to resonance and with 50-ohm resistor connected to simulate noise diode.

Fig.11 - Noise figure test circuit.

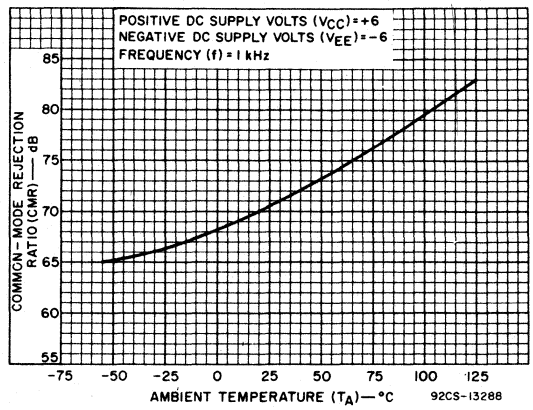
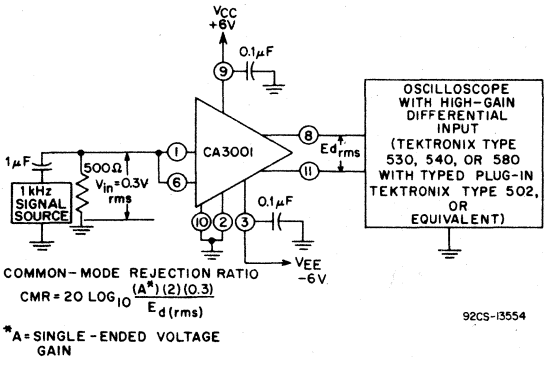


Fig.12 - Common-mode rejection ratio vs. temperature.



*A = SINGLE-ENDED VOLTAGE GAIN

Fig.13 - Common-mode rejection ratio test circuit.

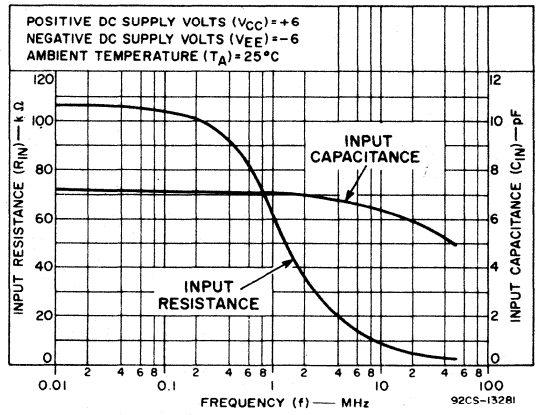


Fig.14 - Input impedance components vs. frequency.

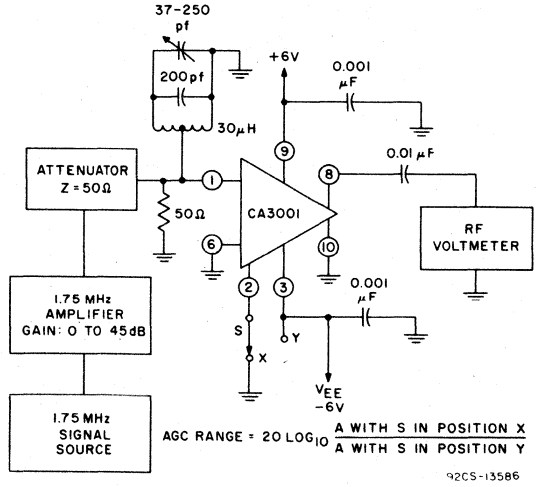


Fig.15 - AGC range test circuit.

12-Lead TO-5

H-1463

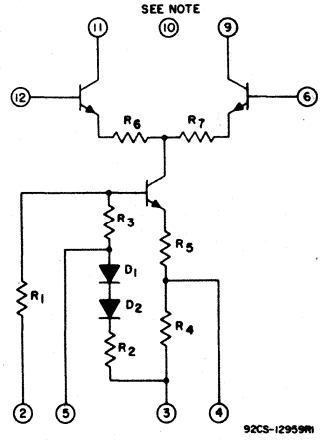
RF Amplifier

Features:

- *Designed for use in communications equipment*
- *Balanced differential-amplifier configuration with controlled constant-current source provides unexcelled versatility*
- *Built-in temperature stability for operation from −55° C to +125° C*
- *Similar to RCA CA3005 and CA3006, plus emitter-degeneration resistors to provide more linear transfer characteristic and increased input-signal handling capability*
- *Companion Application Note ICAN 5022 "Application of RCA CA3004, CA3005, and CA3006 Integrated Circuit RF Amplifiers", covers characteristics of different operating modes, noise performance, cross-modulation, mixer, AGC, limiter, detector, and amplifier design considerations.*

Applications:

- *Push-pull input and output*
- *Wide and narrow-band amplifier*
- *AGC*
- *Detector*
- *Operation from DC to 100 MHz*
- *Mixer*
- *Limiter*
- *Modulator*
- *RF, IF and video frequency capability*



NOTE: Connect Terminal No. 10 to most positive dc supply voltage used for circuit.

Fig. 1 — Schematic Diagram for CA3004

CA3004

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_{FA} = 25°C

Voltage limits shown for each terminal can be applied under the indicated circuit conditions for other terminals. All voltages are with respect to GROUND (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	NO CONNECTION			
2	-9.5	0	6	0
			12	0
			3	-9.5
			9	+6
			10	+6
			11	+6
3	-12	0	2	0
			6	0
			9	+6
			10	+6
			11	+6
			12	0
4	-12	0	2	0
			6	0
			9	+6
			10	+6
			11	+6
			12	0
5	-6	0	2,6,12	0
			3	-6
			9	+6
			10	+6
			11	+6
6	-3.5	+3.5	2	0
			3	-6
			9	+6
			10	+6
			11	+6
			12	0

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
7	NO CONNECTION			
8	NO CONNECTION			
9	0	+12	2	0
			3	-6
			6	0
			10	+6
			11	+6
			12	0
10	0	+12	2	0
			3	-6
			6	0
			9	+6
			11	+6
			12	0
11	0	+12	2	0
			3	-6
			6	0
			10	+6
			11	+6
			12	0
12	-3.5	+3.5	2	0
			3	-6
			6	0
			9	+6
			10	+6
			11	+6
CASE	INTERNALLY CONNECTED TO TERMINAL NO.3 (SUBSTRATE) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE . . . . . -55°C to +125°C

STORAGE-TEMPERATURE RANGE . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

MAXIMUM SINGLE-ENDED INPUT-
SIGNAL VOLTAGE . . . . . ±3.5 V

MAXIMUM COMMON-MODE INPUT-
SIGNAL VOLTAGE . . . . . -2.5 V, +3.5 V

MAXIMUM DEVICE DISSIPATION . . . . . 300 mW

ELECTRICAL CHARACTERISTICS, at T_{FA} = 25° C, V_{CC} = +6V, V_{EE} = -6 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 and No.5 Open Unless Otherwise Specified		TEST CIRCUIT	LIMITS TYPE CA3004				TYPICAL CHARACTERISTICS CURVES
				Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS									
Input Offset Voltage	V_{IO}			Fig.4	–	1.7	5	mV	Fig.2
Input Offset Current	I_{IO}			Fig.5	–	0.125	5	μA	Fig.2
Input Bias Current	I_I			Fig.5	–	21	40	μA	Fig.3
		TERMINALS							
		4	5						
Quiescent Operating Current	I_9 or I_{11}	NC	NC	Fig.8	–	1	–	mA	Fig.6
		V_{EE}	NC	Fig.8	–	2.7	–	mA	Fig.6
		NC	V_{EE}	Fig.8	–	0.45	–	mA	Fig.6
		V_{EE}	V_{EE}	Fig.8	–	1.25	–	mA	Fig.6
Quiescent Operating Current Ratio	I_9/I_{11}			Fig.8	–	1.1	–	–	Fig.7
Device Dissipation	P_T			Fig.8	–	26	–	mW	NONE
DYNAMIC CHARACTERISTICS									
Power Gain	G_P	f = 100 Mc/s		Fig.11	10	12	–	dB	Fig.9
Noise Figure	NF	f = 100 Mc/s		Fig.11	–	6.3	9	dB	Fig.10
Common Mode Rejection Ratio	CMR	f = 1 Kc/s		Fig.13	–	98	–	dB	Fig.12
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 Mc/s		Fig.14	-60	–	–	dB	NONE

DEFINITIONS OF TERMS

Input Offset Voltage

The difference in the dc voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

Input Offset Current

The difference in the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Bias Current

The average value (one-half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Quiescent Operating Current

The average (dc) value of the current in either output terminal.

Quiescent Operating Current Ratio

The ratio of the Quiescent operating currents in the two output terminals.

Device Dissipation

The total power drain of the device with no signal applied and no external load current.

Power Gain

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

Noise Figure

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

Common-Mode Rejection Ratio

The ratio of the full differential voltage gain to the common-mode voltage gain.

Common-Mode Voltage Gain

The ratio of the signal voltages developed between the two output terminals to the signal voltage applied to the two input terminals connected in parallel for ac.

Differential Voltage Gain

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at ac ground.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device.

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3004

INPUT OFFSET VOLTAGE AND CURRENT VS TEMPERATURE

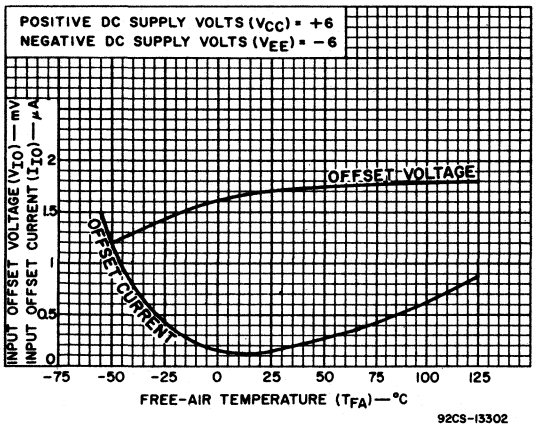


Fig.2

INPUT BIAS CURRENT VS TEMPERATURE

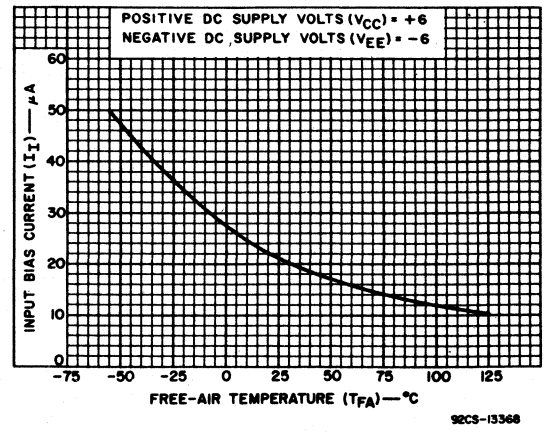


Fig.3

INPUT OFFSET VOLTAGE TEST CIRCUIT

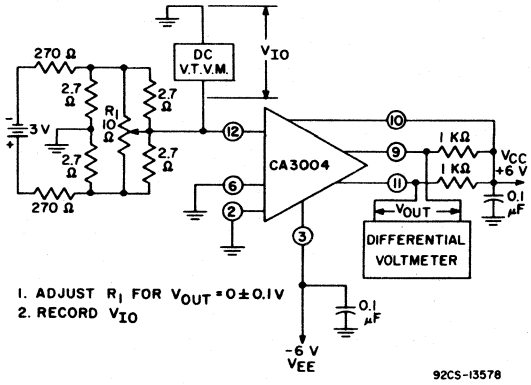


Fig.4

INPUT OFFSET CURRENT AND BIAS CURRENT TEST CIRCUIT

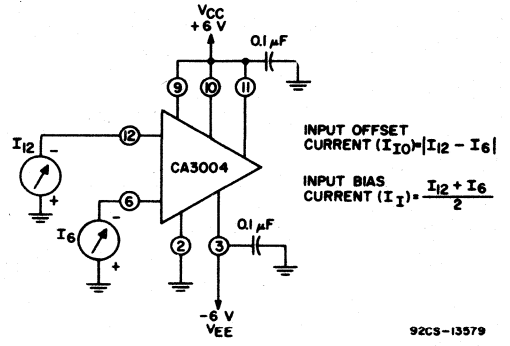


Fig.5

QUIESCENT OPERATING CURRENT VS TEMPERATURE

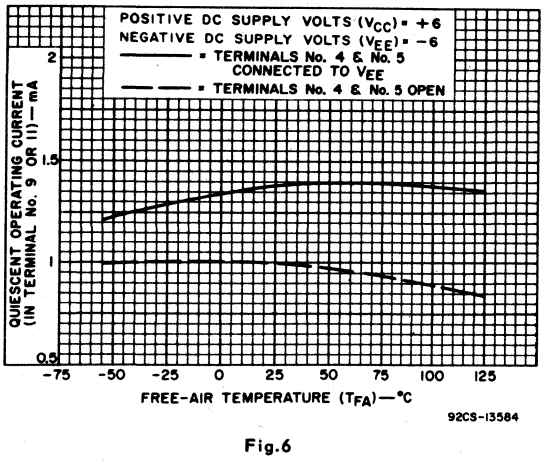


Fig.6

QUIESCENT OPERATING CURRENT RATIO VS TEMPERATURE

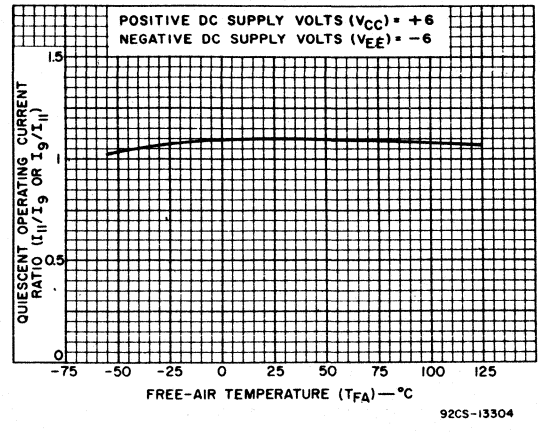
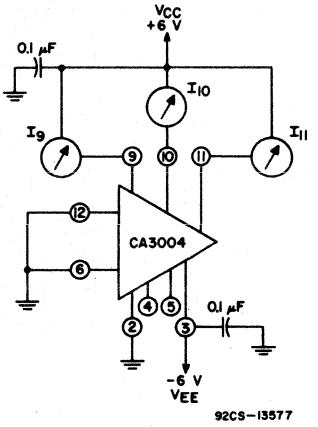


Fig.7

TEST CIRCUIT FOR TYPE CA3004

QUIESCENT OPERATING CURRENT, QUIESCENT OPERATING CURRENT RATIO, AND DEVICE DISSIPATION TEST CIRCUIT



$$P_T = V_{CC}(I_9 + I_{10} + I_{11}) + V_{EE} I_3$$

Fig.8

TYPICAL DYNAMIC CHARACTERISTICS FOR TYPE CA3004

POWER GAIN VS FREQUENCY

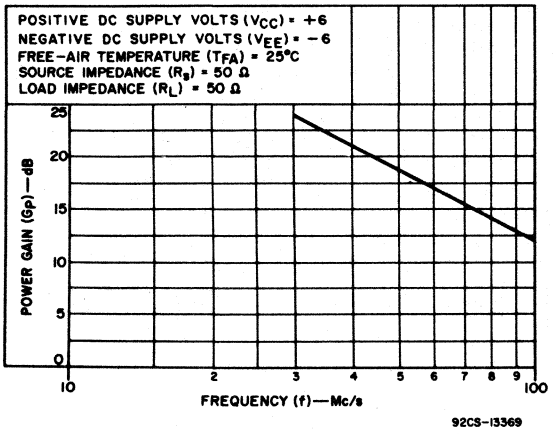


Fig.9

NOISE FIGURE VS FREQUENCY

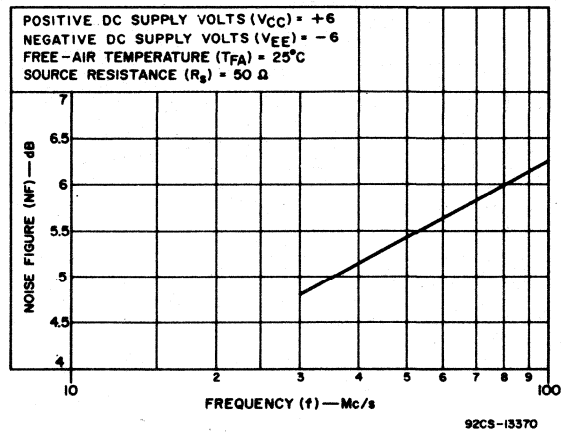


Fig. 10

CA3004

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3004

100 Mc/s POWER GAIN AND NOISE FIGURE TEST CIRCUIT

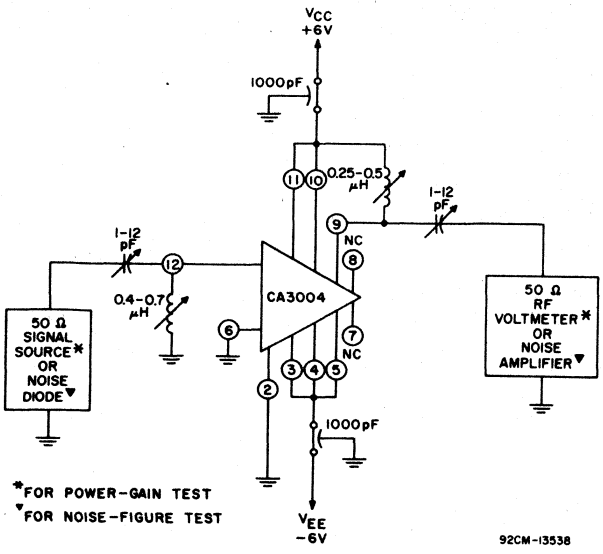


Fig. 11

COMMON-MODE REJECTION RATIO VS TEMPERATURE

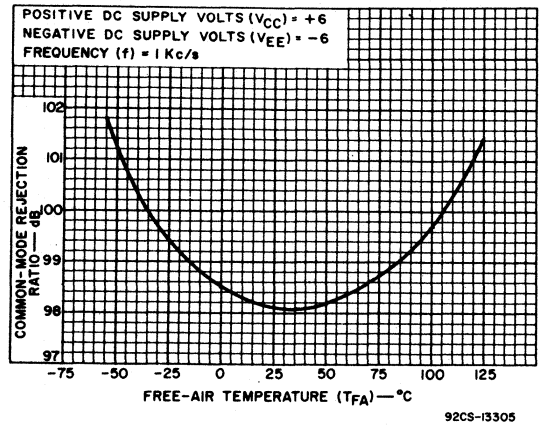


Fig. 12

COMMON-MODE REJECTION RATIO TEST CIRCUIT

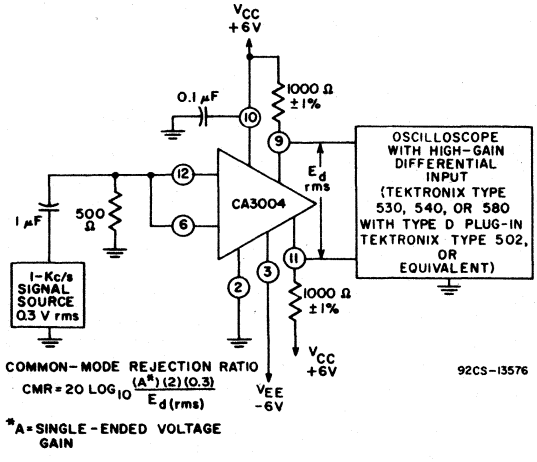


Fig. 13

AGC RANGE TEST CIRCUIT

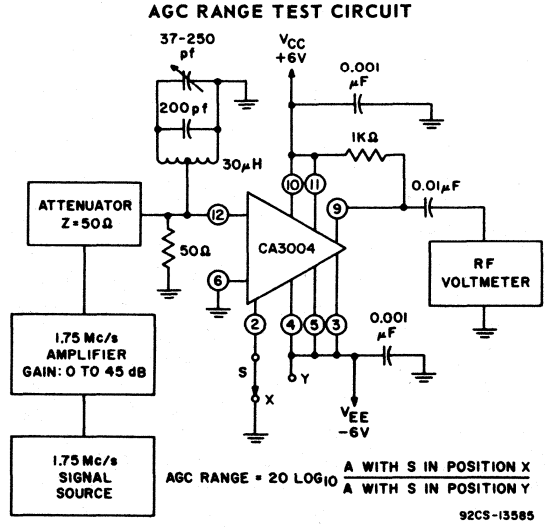


Fig. 14

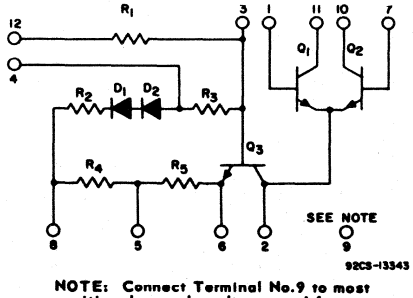
12-Lead TO-5

H-1463

RF Amplifiers

Features:

- *Designed for use in communications equipment*
- *Balanced differential amplifier configuration with controlled constant-current source to provide unexcelled versatility*
- *Built-in temperature stability for operation from −55° C to +125° C*
- *Companion Application Note, ICAN 5022 "Application of RCA CA3004, CA3005, and CA3006 Integrated Circuit RF Amplifiers", covers characteristics of different operating modes, noise performance, cross-modulation, mixer, AGC limiter, detector, and amplifier design considerations.*



NOTE: Connect Terminal No.9 to most positive dc supply voltage used for circuit.

Fig. 1 — Schematic Diagram for CA3005 and CA3006.

Applications:

- *Push-pull input and output*
- *Wide and narrow band amplifier*
- *AGC*
- *Detector*
- *RF, IF, and video frequency capability*
- *Operation from DC to 100 MHz*
- *Mixer*
- *Limiter*
- *Modulator*
- *Cascade Amplifier*

CA3005, CA3006

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_{FA} = 25°C

Voltage limits shown for each terminal can be applied under the indicated voltage conditions for other terminals.
All voltages are with respect to GROUND (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-3.5	+3.5	7 8 9 10 11 12	0 -6 +6 +6 +6 0
2	TEST POINT: DO NOT APPLY VOLTAGE FROM EXTERNAL SOURCE			
3	-9.5	0	1 7 8 9 10 11 12	0 0 -9.5 +6 +6 +6 0
4	-6	0	1 7 8 9 10 11 12	0 0 -6 +6 +6 +6 0
5	-12	0	1 7 9 10 11 12	0 0 +6 +6 +6 0
6	-6	0	1 7 9 10 11 12	0 0 +6 +6 +6 -6
7	-3.5	+3.5	1 8 9 10 11 12	0 -6 +6 +6 +6 0

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	-12	0	1 7 9 10 11 12	0 0 +6 +6 +6 0
9	0	+12	1 7 8 10 11 12	0 0 -6 +6 +6 0
10	0	+12	1 7 8 9 11 12	0 0 -6 +6 +6 0
11	0	+12	1 7 8 9 10 12	0 0 -6 +6 +6 0
12	-9.5	0	8 9 10 11	-9.5 +6 +6 +6
CASE	Internally connected to Terminal No.8 (substrate) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE . . . . . -55°C to +125°C

STORAGE-TEMPERATURE RANGE . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

MAXIMUM SINGLE-ENDED INPUT-
SIGNAL VOLTAGE . . . . . ±3.5 V

MAXIMUM COMMON-MODE INPUT-
SIGNAL VOLTAGE . . . . . -2.5 V, +3.5 V

MAXIMUM DEVICE DISSIPATION . . . . . 300 mW

ECTRICAL CHARACTERISTICS, at $T_A = 25^oC$, $V_{CC} = +6V$, $V_{EE} = -6V$

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.3,4,5, and 6 Not Connected Except Where Noted	TEST CIRCUITS	LIMITS							TYPICAL CHARAC-TERISTICS CURVES
				TYPE CA3005			TYPE CA3006				
			Fig.	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
ATIC CHARACTERISTICS											
ut Offset Voltage	V_{IO}		Fig.3	–	2.6	5	–	0.8	1	mV	Fig.2
ut Offset Current	I_{IO}		Fig.4	–	1.4	–	–	1.4	–	μA	Fig.2
ut Bias Current	I_{IB}		Fig.4	–	19	40	–	19	40	μA	Fig.5
escent erating rrent	I_{10} or I_{11}	TERMINALS 4 / 5: NC / NC	Fig.8	–	1	–	–	1	–	mA	Fig.6
		NC / -V_{EE}	Fig.8	–	2.7	–	–	2.7	–	mA	NONE
		-V_{EE} / NC	Fig.8	–	0.45	–	–	0.45	–	mA	NONE
		-V_{EE} / -V_{EE}	Fig.8	–	1.25	–	–	1.25	–	mA	Fig.6
escent Operating rrent Ratio	$\frac{I_{10}}{I_{11}}$		Fig.8	–	1.05	–	–	1.05	–	–	Fig.7
ice Dissipation	P_T		Fig.8	–	26	–	–	26	–	mW	NONE
NAMIC CHARACTERISTICS											
wer Gain	G_p	f = 100 MHz, Cascode Configuration	Fig.10	16	20	–	16	20	–	dB	Fig.9
		f = 100 MHz, Differential-Ampl. Configuration	Fig.12	14	16	–	14	16	–	dB	Fig.11
se Figure	NF	f = 100 MHz, Cascode Configuration	Fig.10	–	7.8	9	–	7.8	9	dB	Fig.13
		f = 100 MHz, Differential Ampl. Configuration	Fig.12	–	7.8	9	–	7.8	9	dB	Fig.14
mmon-Mode ejection Ratio	CMR	f = 1 kHz	Fig.16	–	101	–	–	101	–	dB	Fig.15
C Range (Max. Voltage ain to Complete Cutoff)	AGC	f = 1.75 MHz	Fig.17	-60	–	–	-60	–	–	dB	NONE

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPES CA3005 AND CA3006

INPUT OFFSET VOLTAGE AND CURRENT

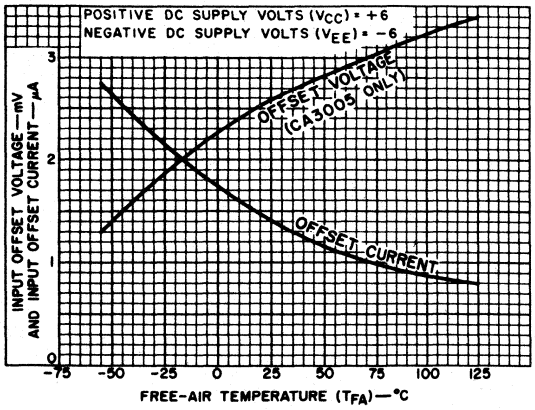


Fig.2

INPUT OFFSET VOLTAGE TEST CIRCUIT

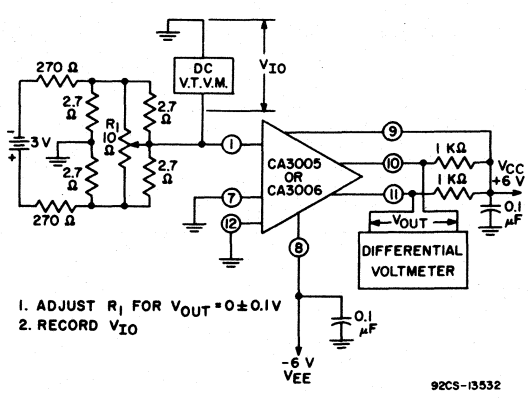


Fig.3

INPUT BIAS CURRENT

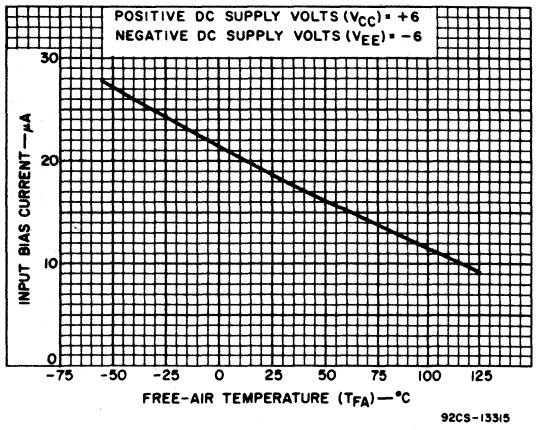


Fig. 4

QUIESCENT OPERATING CURRENT

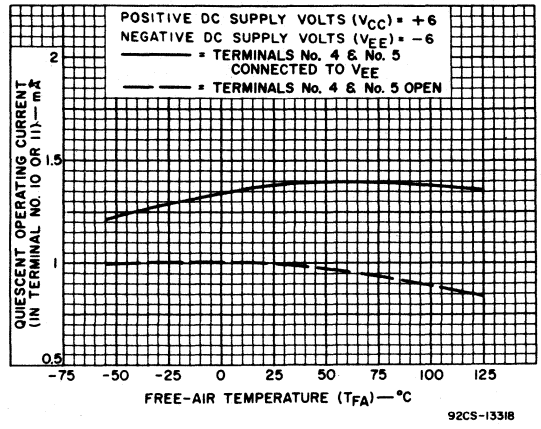


Fig.5

QUIESCENT OPERATING CURRENT RATIO

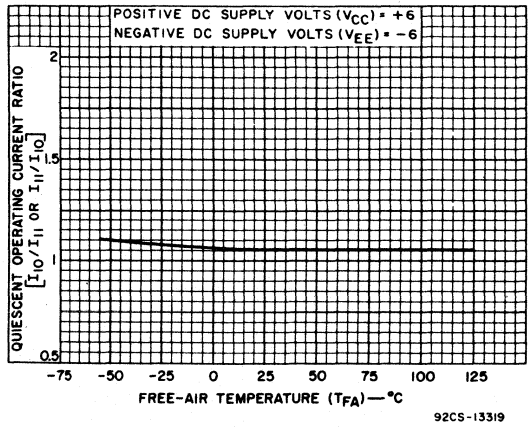


Fig.6

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPES CA3005 AND CA3006

POWER-GAIN (CASCODE CONFIGURATION)

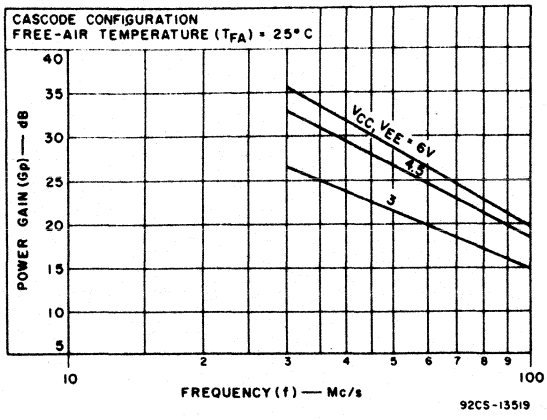


Fig.7

POWER-GAIN (DIFFERENTIAL-AMPLIFIER CONFIGURATION)

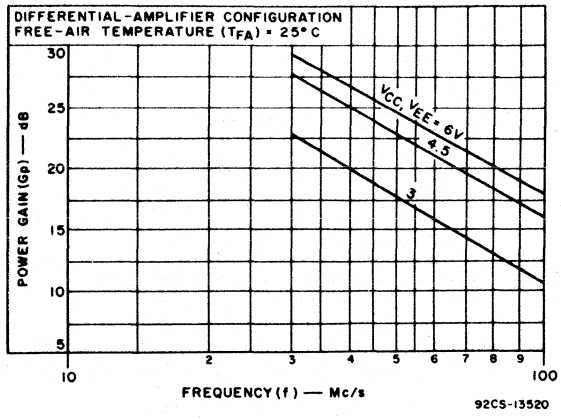
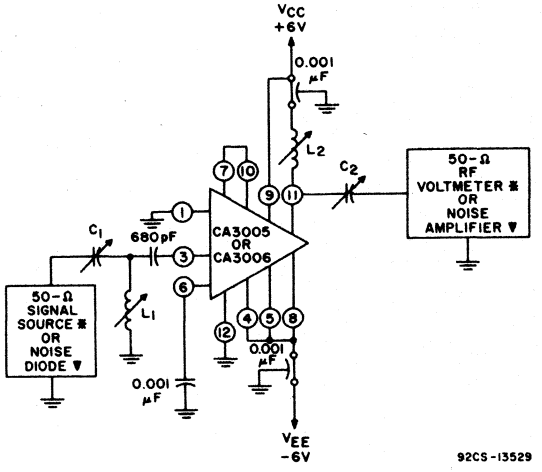


Fig.9

NOISE FIGURE AND POWER GAIN TEST CIRCUIT (CASCODE CONFIGURATION)



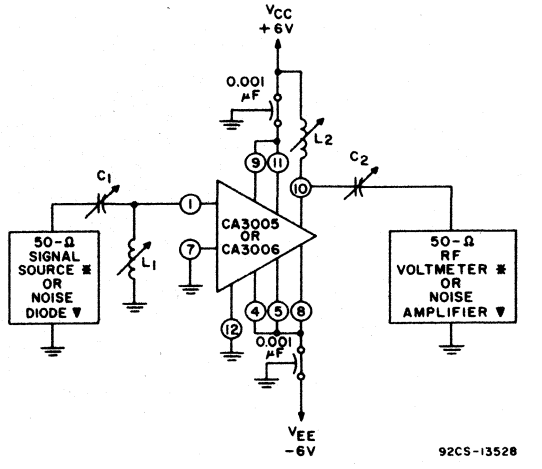
f Mc/s	C_1 pF	C_2 pF	L_1 μH	L_2 μH
30	14-150	5-40	0.3-0.6	0.8-1.4
100	5-40	5-40	0.07-0.12	0.15-0.3

* FOR POWER-GAIN TEST

▼ FOR NOISE-FIGURE TEST

Fig. 8

NOISE FIGURE AND POWER-GAIN TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION)



f Mc/s	C_1 pF	C_2 pF	L_1 μH	L_2 μH
30	5-40	1.5-20	1.2-2	1.2-2
100	1-12	1-12	0.4-0.7	0.25-0.5

* FOR POWER-GAIN TEST

▼ FOR NOISE-FIGURE TEST

Fig. 10

TYPICAL DYNAMIC CHARACTERISTICS FOR TYPES CA3005 AND CA3006

100-Mc/s NOISE FIGURE VS. V_{EE} (CASCODE CONFIGURATION)

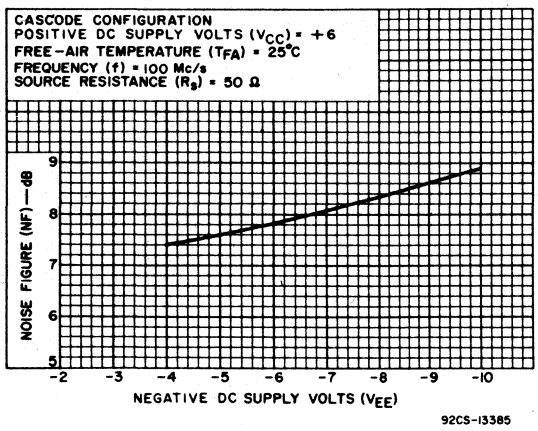


Fig. 11

100 Mc/s NOISE FIGURE VS. V_{EE} (DIFFERENTIAL AMPLIFIER CONFIGURATION)

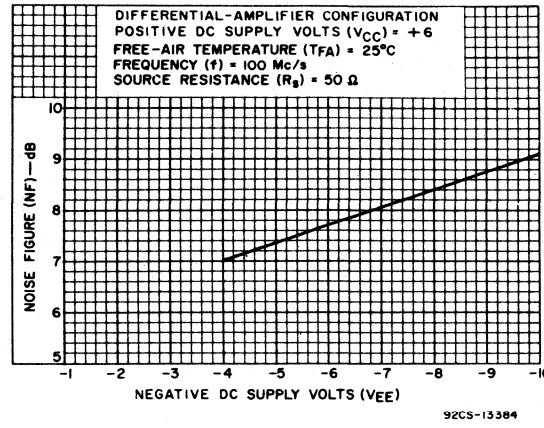


Fig. 12

COMMON-MODE-REJECTION RATIO

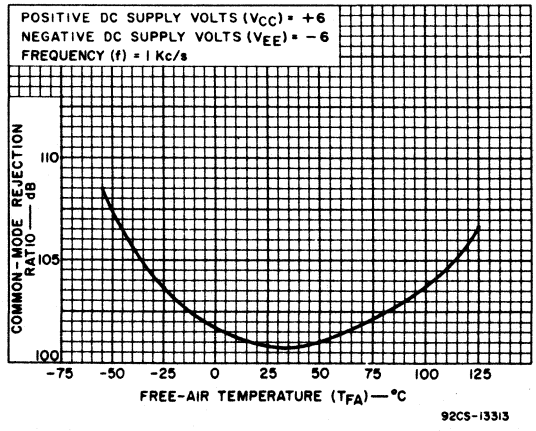


Fig. 13

TYPICAL DYNAMIC TEST CIRCUITS FOR TYPES CA3005 AND CA3006

COMMON-MODE REJECTION RATIO TEST CIRCUIT

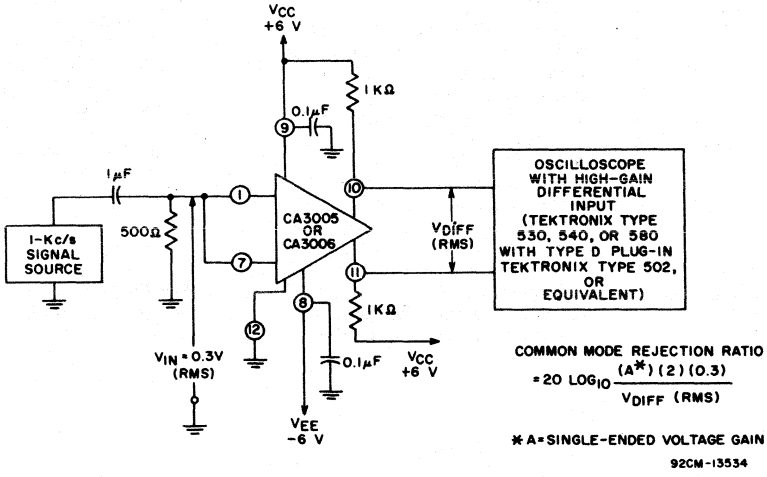


Fig. 14

AGC RANGE TEST CIRCUIT

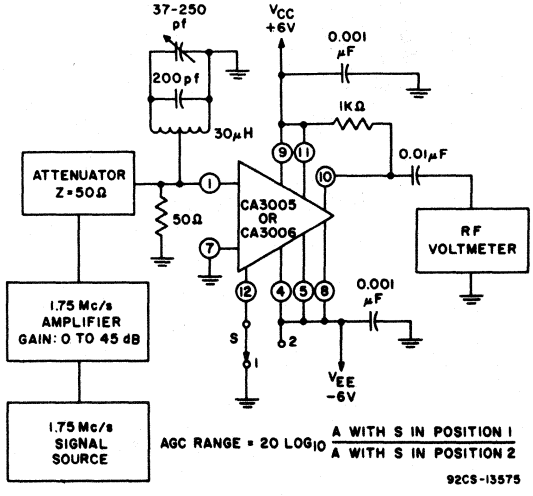


Fig. 15

CA3007

12-Lead TO-5

H-1463

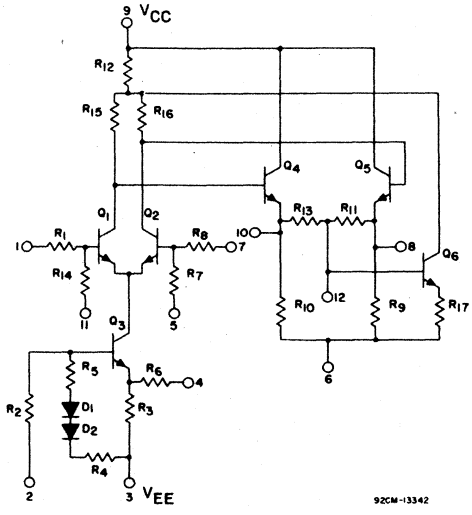
AF Amplifier

Features:

- *Input impedance - 4 kΩ typ.*
- *Output impedance - 60 Ω typ.*
- *Power gain - 22 dB typ.*
- *Push-pull input & output*
- *Direct coupling to class B audio output stage*
- *Designed for use in sound systems and communication equipment*
- *Balanced differential-amplifier configuration with controlled constant-current source provides for both audio amplification and phase inversion*
- *Built-in temperature stability for operation from −55° C to +125° C*
- *Eliminates need for audio driver transformer*
- *Companion Application Note, ICAN 5037 "Application of the RCA-CA3007 Integrated Circuit Audio Driver" covers design of a dual supply audio driver in a direct-coupled audio amplifier, and a single supply audio driver in a capacitor-coupled audio amplifier*

Applications

- *Audio amplifier*
- *Audio driver*



SCHEMATIC DIAGRAM

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_A = 25° C

Indicated voltage limits for each terminal can be applied under the specified operating conditions for other terminals. All voltages are with respect to ground (-V_{CC}, +V_{EE}, or common terminal of Positive and Negative DC supplies).

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
2	-8	0	3	-8
			6	0
			7	0
			9	+6
			11	0
3	-10	0	6	0
			7	0
			9	+6
			11	0
4	-8.5	0	6	0
			7	0
			9	+6
			11	0
5	-2.5	+2.5	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
6	-3	0	2	0
			3	-6
			7	0
			9	+6
			11	0
7	-2.5	+2.5	1	0
			2	0
			3	-6
			5	0
			6	0
			9	+6
8	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
9	0	+10	2	0
			3	-6
			6	0
			7	0
			11	0
10	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
11	-2.5	+2.5	1	0
			2	0
			3	-6
			6	0
			7	0
			9	+6
12	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE . . . . . -55°C to +125°C

STORAGE-TEMPERATURE RANGE . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

MAXIMUM SINGLE-ENDED INPUT-
SIGNAL VOLTAGE . . . . . ±2.5 V

MAXIMUM COMMON-MODE INPUT-
SIGNAL VOLTAGE . . . . . ±2.5 V

MAXIMUM DEVICE DISSIPATION . . . . . 300 mW

CA3007

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V_{CC} = +6 V, V_{EE} = -6 V,

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Pin 4 Not Connected Unless Otherwise Noted	TEST CIRCUITS	LIMITS TYPE CA3007				TYPICAL CHARACTERISTICS CURVES
			Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS								
Input Unbalance Voltage	V_{IU}		3	–	0.57	5	mV	2
Input Unbalance Current	I_{IU}		3	–	0.57	5	μA	2
Input Bias Current	I_I		3	–	11	34	μA	4
Quiescent Operating Voltage	V_8 or V_{10}		3	–	0.87	–	V	5
Device Dissipation	P_T		3	–	30	–	mW	NONE
DYNAMIC CHARACTERISTICS								
Power Gain	G_P	f = 1 kHz	6	20	22	–	dB	NONE
Total Harmonic Distortion	THD	f = 1 kHz	6	–	0.28	–	%	NONE
Input Impedance	Z_{IN}	f = 1 kHz	7	–	4K	–	Ω	NONE
Common-Mode Rejection Ratio	CMR	f = 1 kHz	9(A) 9(B)	–	77	–	dB	8

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUIT FOR CA3007

INPUT UNBALANCE VOLTAGE AND CURRENT vs TEMPERATURE

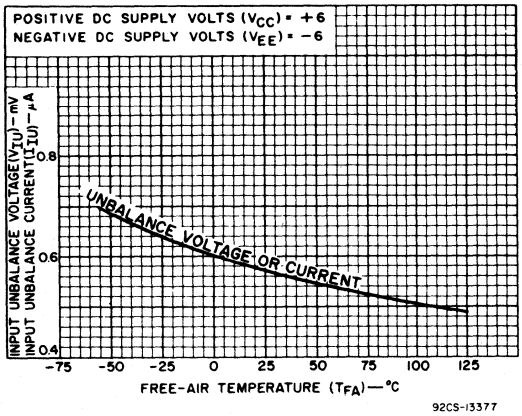
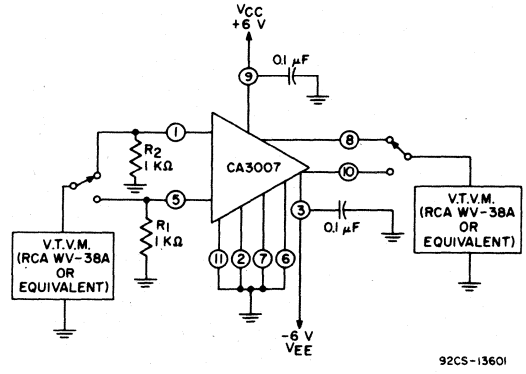


Fig.2

INPUT UNBALANCE VOLTAGE & CURRENT, INPUT BIAS CURRENT, QUIESCENT OPERATING VOLTAGE, AND DEVICE DISSIPATION TEST CIRCUIT



R_1 and R_2 matched to ± 1%.

$P_T = V_{CC}I_9 + V_{EE}I_3$

I_9 = Direct Current into Terminal No.9

I_3 = Direct Current out of Terminal No.3

Fig.3

INPUT BIAS CURRENT vs TEMPERATURE

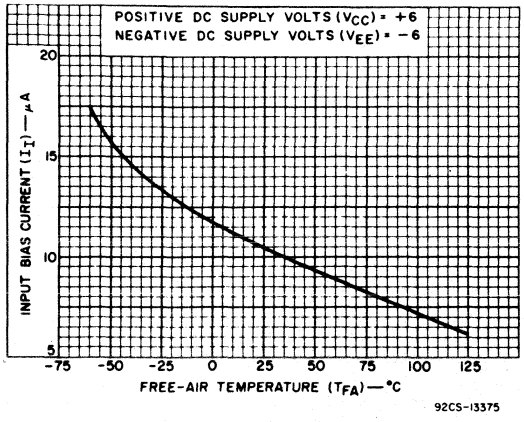


Fig.4

QUIESCENT OPERATING VOLTAGE vs TEMPERATURE

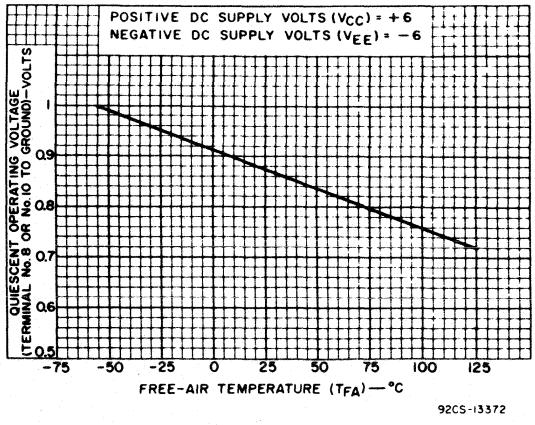
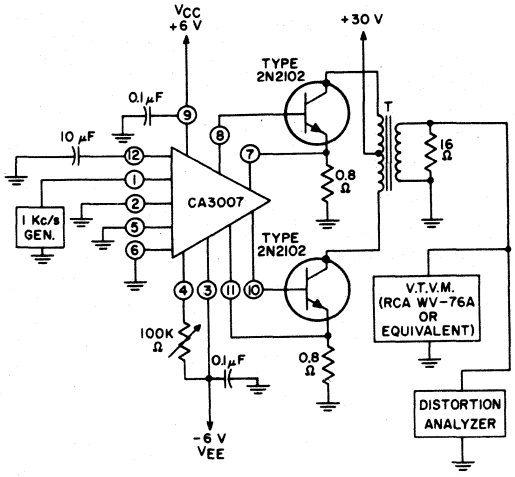


Fig.5

TYPICAL DYNAMIC TEST CIRCUITS FOR CA3007

POWER GAIN AND TOTAL HARMONIC DISTORTION TEST CIRCUIT



T (Output Transformer):
Primary Impedance = 2000 Ω C.T.
Secondary Impedance = 16 Ω
Efficiency = 45% approx.
(STANCOR TYPE TA-10 OR EQUIVALENT)

Fig.6

INPUT IMPEDANCE TEST CIRCUIT

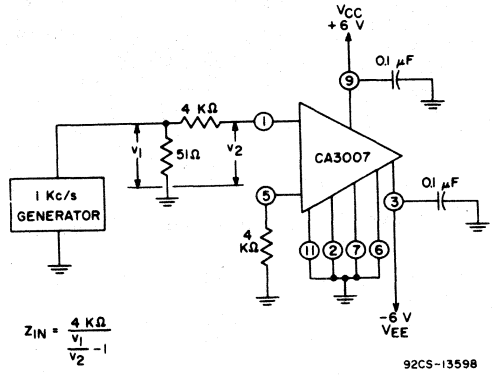


Fig.7

TYPICAL DYNAMIC CHARACTERISTIC AND TEST CIRCUITS FOR CA3007

COMMON-MODE REJECTION RATIO vs TEMPERATURE

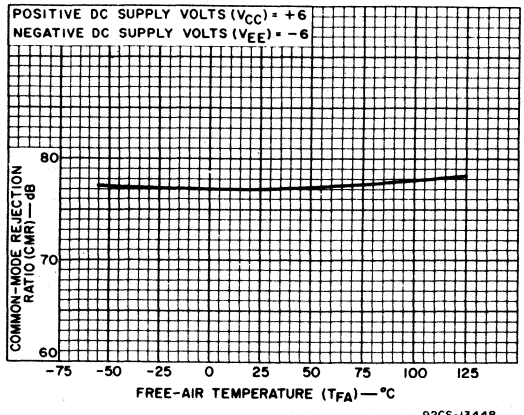
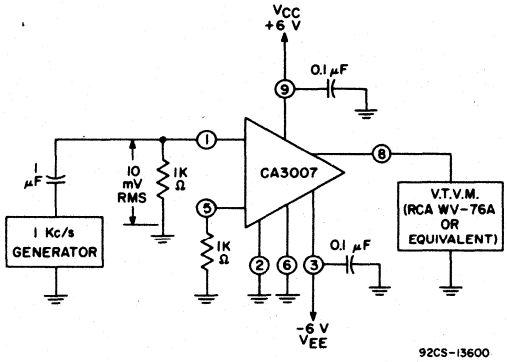


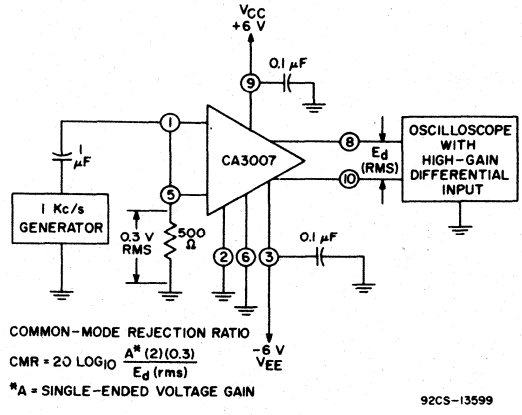
Fig.8

COMMON-MODE REJECTION-RATIO TEST CIRCUITS

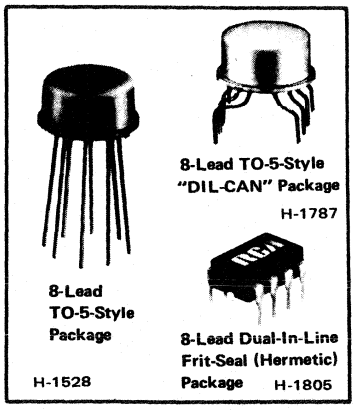


(A) Single-Ended Differential Voltage Gain

Fig.9



(B) Common-Mode Voltage Gain



DIFFERENTIAL/CASCODE AMPLIFIERS

For Communications and Industrial Equipment at Frequencies from DC to 120 MHz

FEATURES

- Controlled for Input Offset Voltage, Input Offset Current, and Input Bias Current (CA3028 Series only)
- Balanced Differential Amplifier Configuration with Controlled Constant-Current Source
- Single- and Dual-Ended Operation
- Operation from DC to 120 MHz
- Balanced-AGC Capability
- Wide Operating-Current Range

The CA3028A and CA3028B are differential/cascode amplifiers designed for use in communications and industrial equipment operating at frequencies from dc to 120 MHz.

The CA3028B is like the CA3028A but is capable of premium performance particularly in critical dc and differential amplifier applications requiring tight controls for input offset voltage, input offset current, and input bias current.

The CA3053 is similar to the CA3028A and CA3028B but is recommended for IF amplifier applications.

The CA3028A, CA3028B, and CA3053 are supplied in a hermetic 8-lead TO-5-style package. The "F" versions are supplied in a frit-seal TO-5 package, and the "S" versions in formed-lead (DIL-CAN) packages.

APPLICATIONS

- RF and IF Amplifiers (Differential or Cascode)
- DC, Audio, and Sense Amplifiers
- Converter in the Commercial FM Band
- Oscillator • Mixer • Limiter
- Companion Application Note, ICAN 5337 "Application of the RCA CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges." This note covers characteristics of different operating modes, noise performance, mixer, limiter, and amplifier design considerations.

The CA3028A, CA3028B, and CA3053 are available in the packages shown below. When ordering these devices, it is important to add the appropriate suffix letter to the device.

Package 8-Lead TO-5	Suffix Letter	CA3028A	CA3028B	CA3053
TO-5	T	√	√	√
With Dual-In-Line Formed Leads (DIL-CAN)	S	√	√	√
Frit-Seal Ceramic	F	√	√	√
Beam-Lead	L	√		
Chip	H	√		

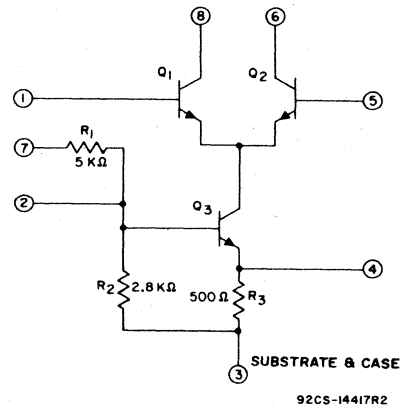


Fig.1 - Schematic diagram for CA3028A, CA3028B and CA3053.

CA3028A, CA3028B, CA3053 Types

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

DISSIPATION:

At T_A up to 55°C
(CA3028AF, CA3028BF, CA3053F) ..... 750 mW

At T_A > 55°C
(CA3028AF, CA3028BF, CA3053F) ..... Derate linearly 6.67 mW/°C

At T_A up to 85°C
(CA3028A, CA3028B, CA3053) ..... 450 mW

At T_A > 85°C
(CA3028A, CA3028B, CA3053) Derate linearly 5 mW/°C

AMBIENT-TEMPERATURE RANGE:

Operating ..... −55°C to +125°C

Storage ..... −65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL No.	1	2	3	4	5	6	7	8
1		0 to -15▲	0 to -15▲	0 to -15▲	+5 to -5	*	*	+20⊕ to 0
2			+5 to -11	+5 to -1	+15♦ to 0	*	+15♦ to 0	*
3‡				+10 to 0	+15♦ to 0	+30● to 0	+15♦ to 0	+30● to 0
4					+15♦ to 0	*	*	*
5						+20⊕ to 0	*	*
6							*	*
7								*
8								

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal terminal 4 with respect to terminal 2 is -1 to +5 volts.

‡ Terminal #3 is connected to the substrate and case.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.

▲ Limit is -12V for CA3053

⊕ Limit is +15V for CA3053

♦ Limit is +12V for CA3053

● Limit is +24V for CA3028A and +18V for CA3053

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CIRCUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A			LIMITS TYPE CA3028B			LIMITS TYPE CA3053			UNITS	TYPICAL CHARACTERISTICS CURVES Fig.
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
STATIC CHARACTERISTICS															
			$+V_{CC}$	$-V_{EE}$											
Input Offset Voltage	V_{IO}	2	6V 12V	6V 12V	- -	- -	- -	- -	0.98 0.89	5 5	- -	- -	- -	mV	4
Input Offset Current	I_{IO}	3a	6V 12V	6V 12V	- -	- -	- -	- -	0.56 1.06	5 6	- -	- -	- -	μA	4
Input Bias Current	I_I	3a	6V 12V	6V 12V	- -	16.6 36	70 106	- -	16.6 36	40 80	- -	- -	- -	μA	5a
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	29 36	85 125		5b
Quiescent Operating Current	I_6 or I_8	3a	6V 12V	6V 12V	0.8 2	1.25 3.3	2 5	1 2.5	1.25 3.3	1.5 4	- -	- -	- -	mA	6a 7
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	1.2 2.0	2.2 3.3	3.5 5.0		6b
AGC Bias Current (Into Constant-Current Source Terminal No.7)	I_7	8a	12V 12V	V_{AGC} =+9 V_{AGC} = +12	- -	1.28 1.65	- -	- -	1.28 1.65	- -	- -	- -	- -	mA	8b
		-	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	1.15 1.55	- -		-
Input Current (Terminal No.7)	I_7	-	6V 12V	6V 12V	0.5 1	0.85 1.65	1 2.1	0.5 1	0.85 1.65	1 2.1	- -	- -	- -	mA	-
Device Dissipation	P_T	3a	6V 12V	6V 12V	24 120	36 175	54 260	24 120	36 175	42 220	- -	- -	- -	mW	9
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	50 100	80 150		-

ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A Min.	Typ.	Max.	LIMITS TYPE CA3028B Min.	Typ.	Max.	LIMITS TYPE CA3053 Min.	Typ.	Max.	UNITS	TYPICAL CHARAC-TERISTICS CURVE Fig.
DYNAMIC CHARACTERISTICS															
Power Gain	G_P	10a	f = 100 MHz	Cascode	16	20	-	16	20	-	-	-	-	dB	10b
		11a,d	V_{CC} = +9V	Diff.-Ampl.	14	17	-	14	17	-	-	-	-		11b,e
		10a	f = 10.7 MHz	Cascode	35	39	-	35	39	-	35	39	-	dB	10b *
		11a	V_{CC} = +9V	Diff.-Ampl.	28	32	-	28	32	-	28	32	-		11b *
Noise Figure	NF	10a	f = 100 MHz	Cascode	-	7.2	9	-	7.2	9	-	-	-	dB	10c
		11a,d	V_{CC} = +9V	Diff.-Ampl.	-	6.7	9	-	6.7	9	-	-	-		11c,e
Input Admittance	Y_{11}	-	f = 10.7 MHz V_{CC} = +9V	Cascode				-	0.6 + j 1.6	-				mmho	12
		-		Diff.-Ampl.				-	0.5 + j 0.5	-					13
Reverse Transfer Admittance	Y_{12}	-		Cascode				-	0.0003 - j0	-				mmho	14
		-		Diff.-Ampl.				-	0.01 - j0.0002	-					15
Forward Transfer Admittance	Y_{21}	-		Cascode				-	99 - j18	-				mmho	16
		-		Diff.-Ampl.				-	-37 + j0.5	-					17
Output Admittance	Y_{22}	-		Cascode				-	0. + j0.08	-				mmho	18
		-		Diff.-Ampl.				-	0.04 + j0.23	-					19
Power Output (Untuned)	P_o	20a	f = 10.7 MHz	Diff.-Ampl. 50 Ω Input-Output	-	5.7	-	-	5.7	-	-	-	-	μW	20b
AGC Range (Max. Power Gain to Full Cutoff)	AGC	21a	V_{CC} = +9V	Diff.-Ampl.	-	62	-	-	62	-	-	-	-	dB	21b
Voltage Gain at f = 10.7 MHz	A	22a	f = 10.7 MHz	Cascode	-	40	-	-	40	-	-	40	-	dB	22b
		22c	V_{CC} = +0V R_L = 1 kΩ	Diff. Ampl.	-	30	-	-	30	-	-	30	-		22d
Voltage Gain Differential at f = 1 kHz		23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	35	38	42	-	-	-	dB	-
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	-	-	40	42.5	45	-	-	-		
Max. Peak-to-Peak Output Voltage at f = 1 kHz	V_o(P-P)	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	7	11.5	-	-	-	-	V_{P-P}	-
			V_{CC} = +12V, V_{EE} = -12V R_L = 1.6 kΩ		-	-	-	15	23	-	-	-	-		
Bandwidth at -3 dB point	BW	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	-	7.3	-	-	-	-	MHz	-
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	-	-	-	8	-	-	-	-		
Common-Mode Input-Voltage Range	V_{CMR}	24	V_{CC} = +6V, V_{EE} = -6V		-	-	-	-2.5	(-3.2 - 4.5)	4	-	-	-	V	-
			V_{CC} = +12V, V_{EE} = -12V		-	-	-	-5	(-7 - 9)	7	-	-	-		
Common-Mode Rejection Ratio	CMR	24	V_{CC} = +6V, V_{EE} = -6V		-	-	-	60	110	-	-	-	-	dB	-
			V_{CC} = +12V, V_{EE} = -12V		-	-	-	60	90	-	-	-	-		
Input Impedance at f = 1 kHz	Z_{IN}		V_{CC} = +6V, V_{EE} = -6V		-	-	-	-	5.5	-	-	-	-	kΩ	-
			V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	3	-	-	-	-		
Peak-to-Peak Output Current	I_{P-P}		V_{CC} = +9V	f = 10.7 MHz	2	4	7	2.5	4	6	2	4	7	mA	-
			V_{CC} = +12V	e_{in} = 400 mV Diff.-Ampl.	3.5	6	10	4.5	6	8	3.5	6	10		

* Does not apply to CA3053

CA3028A, CA3028B, CA3053 Types

DEFINITIONS OF TERMS

AGC Bias Current

The current drawn by the device from the AGC-voltage source, at maximum AGC voltage.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device.

Common-Mode Rejection Ratio

The ratio of the full differential voltage gain to the common-mode voltage gain.

Device Dissipation

The total power drain of the device with no signal applied and no external load current.

Input Bias Current

The average value (one-half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Offset Current

The difference in the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Offset Voltage

The difference in the dc voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

Noise Figure

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

Power Gain

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

Quiescent Operating Current

The average (dc) value of the current in either output terminal.

Voltage Gain

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at ac ground.

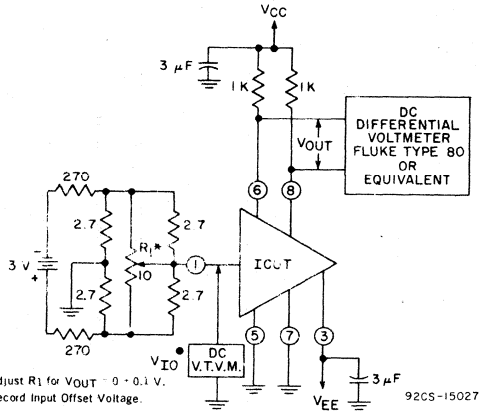


Fig.2 - Input offset voltage test circuit for CA3028B.

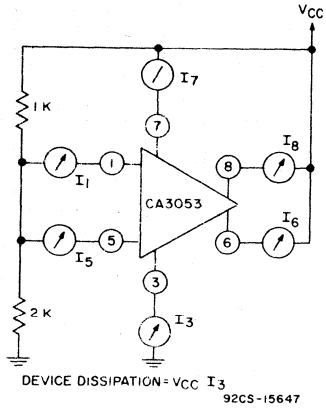


Fig.3b - Input bias current, device dissipation, and quiescent operating current test circuit for CA3053.

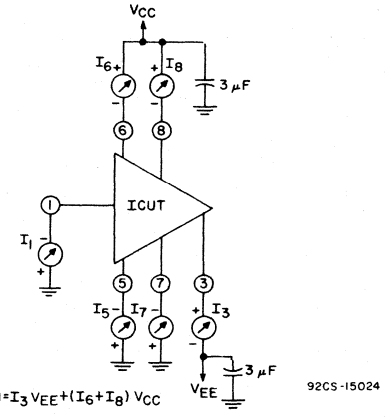


Fig.3a - Input offset current, input bias current, device dissipation, and quiescent operating current test circuit for CA3028A and CA3028B.

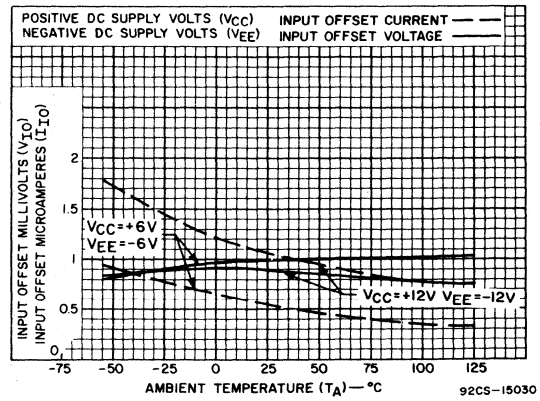


Fig.4 - Input offset voltage and input offset current for CA3028B.

TYPICAL CHARACTERISTICS

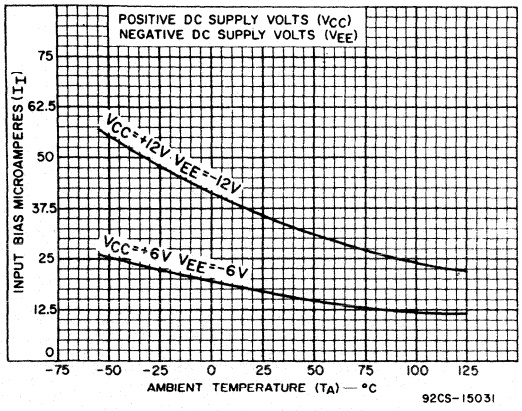


Fig.5a - Input bias current vs. ambient temperature for CA3028A and CA3028B.

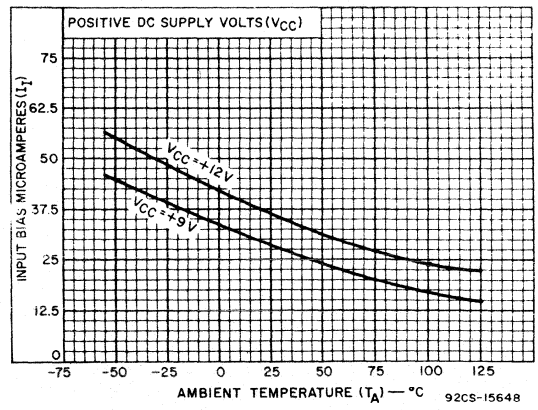


Fig.5b - Input bias current vs. ambient temperature for CA3053.

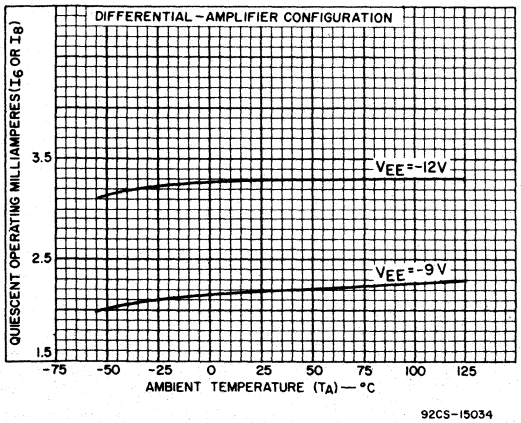


Fig.6a - Quiescent operating current vs. ambient temperature for CA3028A and CA3028B.

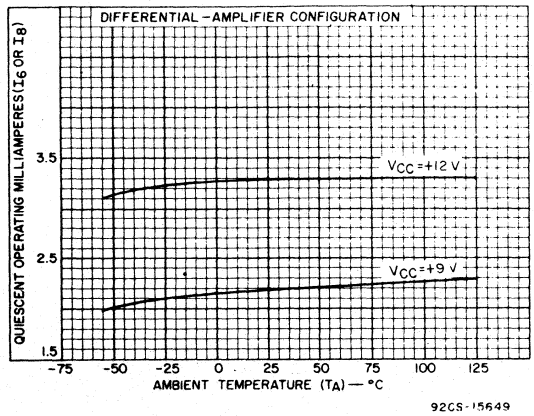


Fig.6b - Quiescent operating current vs. ambient temperature for CA3053.

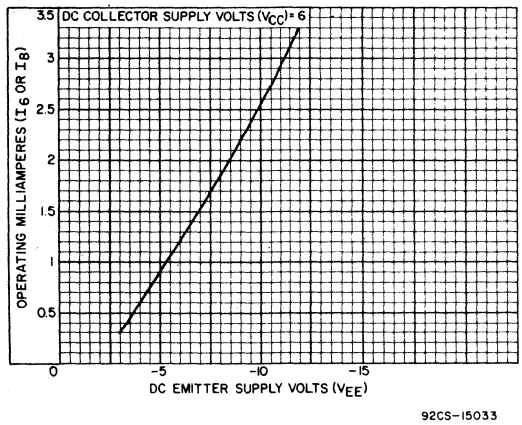


Fig.7 - Operating current vs. V_{EE} voltage for CA3028A and CA3028B.

TYPICAL CHARACTERISTICS AND TEST CIRCUITS

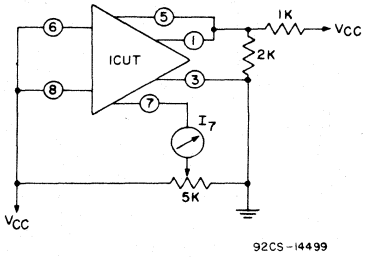


Fig.8a - AGC bias current test circuit (differential-amplifier configuration) for CA3028A and CA3028B.

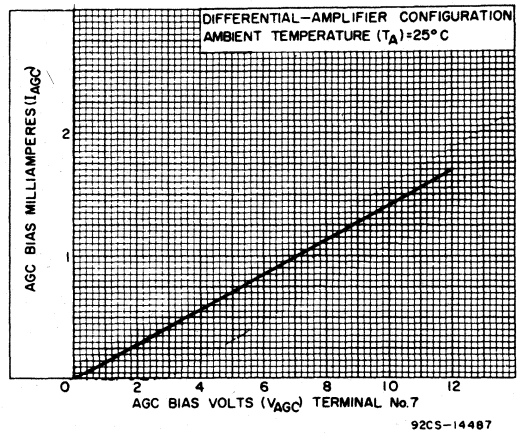


Fig.8b - AGC bias current vs. bias volts (terminal No.7) for CA3028A and CA3028B.

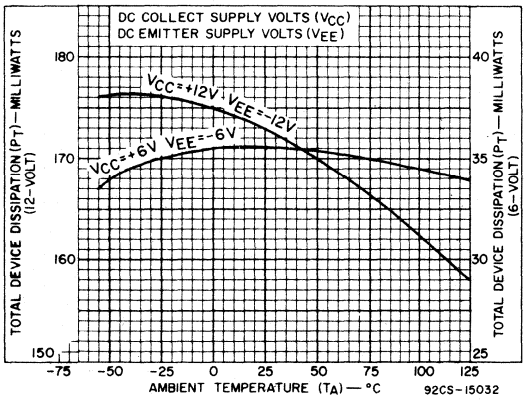
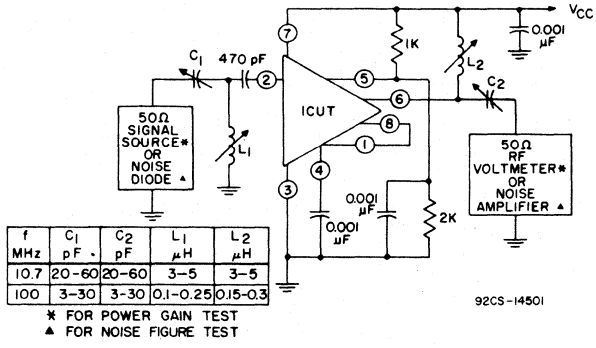


Fig.9 - Device dissipation vs. temperature for CA3028A and CA3028B.



f MHz	C1 pF	C2 pF	L1 µH	L2 µH
10.7	20-60	20-60	3-5	3-5
100	3-30	3-30	0.1-0.25	0.15-0.3

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig.10a - Power gain and noise figure test circuit (cascode configuration) for CA3028A, CA3028B and CA3053.*

* 10.7 MHz Power Gain Test Only.

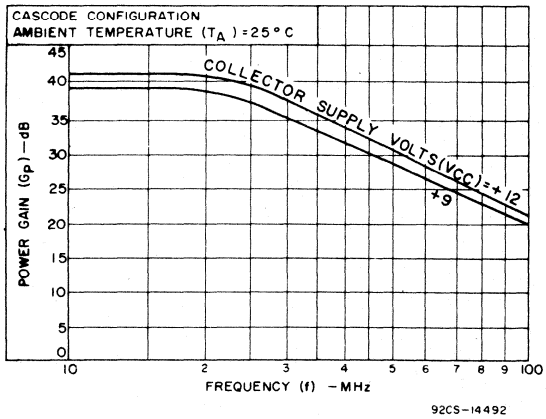


Fig.10b - Power gain vs. frequency (cascode configuration) for CA3028A and CA3028B.

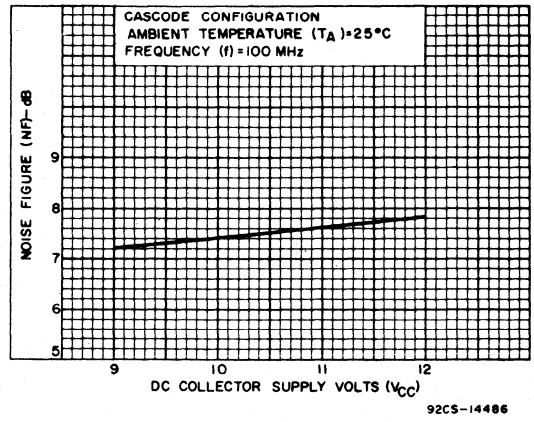
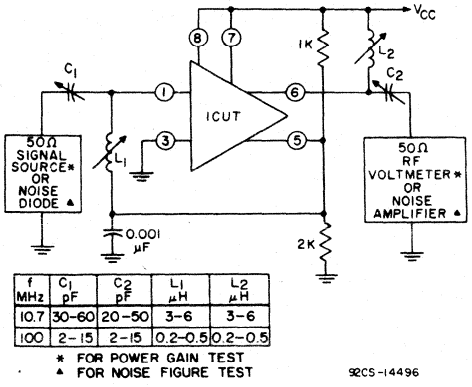


Fig.10c - 100 MHz noise figure vs. collector supply volts (cascode configuration) for CA3028A and CA3028B.

TYPICAL NOISE FIGURE AND POWER GAIN TEST CIRCUITS AND CHARACTERISTICS



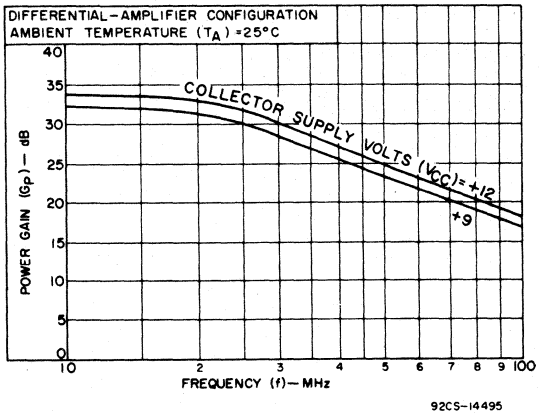
f MHz	C_1 pF	C_2 pF	L_1 μH	L_2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

92CS-14496

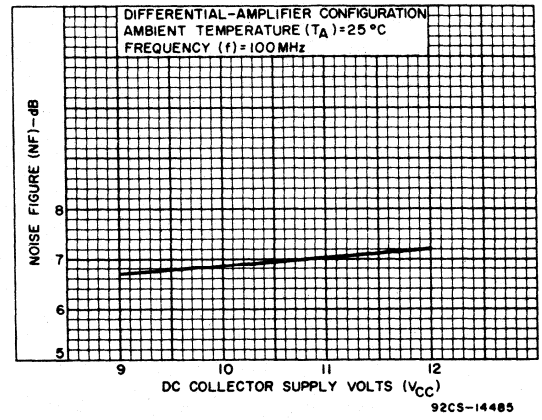
Fig.11a - Power gain and noise figure test circuit (differential-amplifier configuration and terminal No.7 connected to V_{CC}) for CA3028A, CA3028B and CA3053.*

* 10.7 MHz Power Gain Test Only.



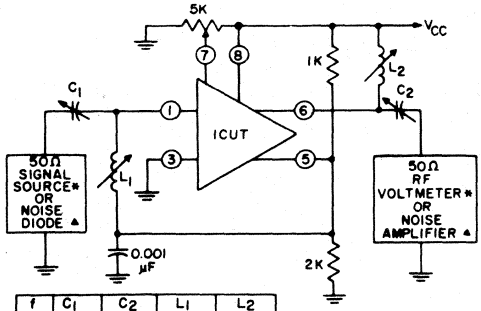
92CS-14495

Fig.11b - Power gain vs. frequency (differential-amplifier configuration) for CA3028A and CA3028B.



92CS-14485

Fig.11c - 100 MHz noise figure vs. collector supply voltage (differential-amplifier configuration) for CA3028A and CA3028B.

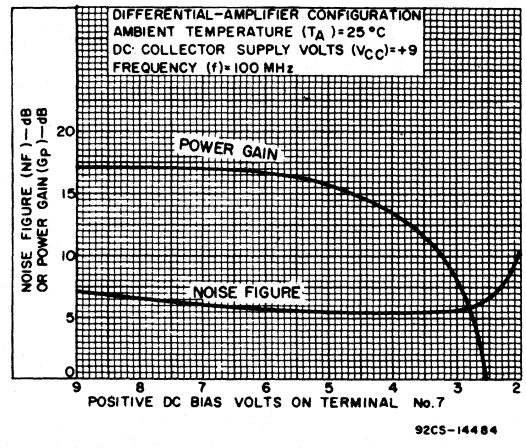


f MHz	C_1 pF	C_2 pF	L_1 μH	L_2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

92CS-14516

Fig.11d - Power gain and noise figure test circuit (differential-amplifier configuration for CA3028A and CA3028B.



92CS-14484

Fig.11e - 100 MHz noise figure and power gain vs. base-to-emitter bias (terminal No.7) for CA3028A and CA3028B.

TYPICAL ADMITTANCE PARAMETERS

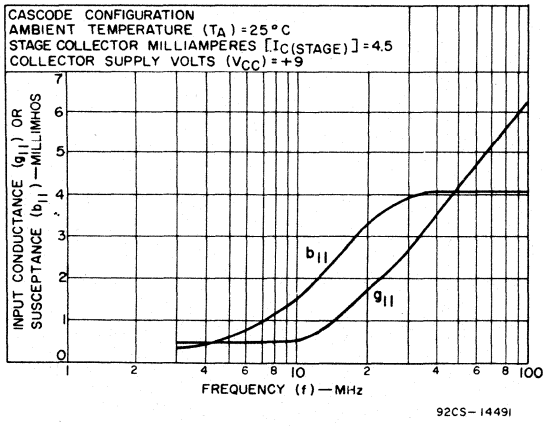


Fig.12 - Input admittance (Y_{11}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

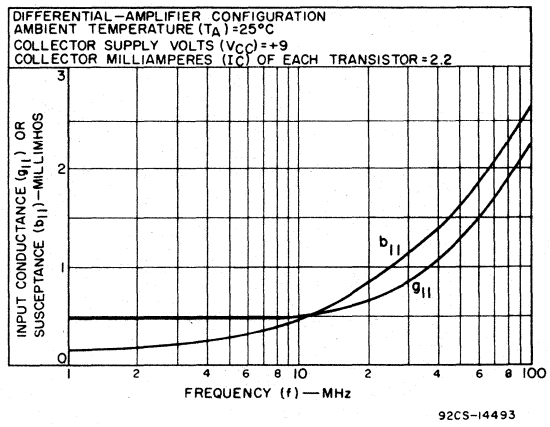


Fig.13 - Input admittance (Y_{11}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

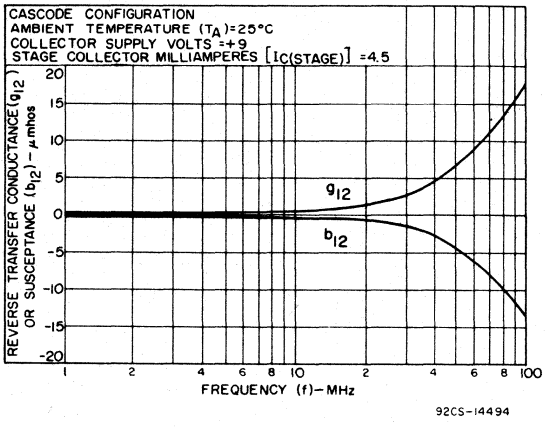


Fig.14 - Reverse transadmittance (Y_{12}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

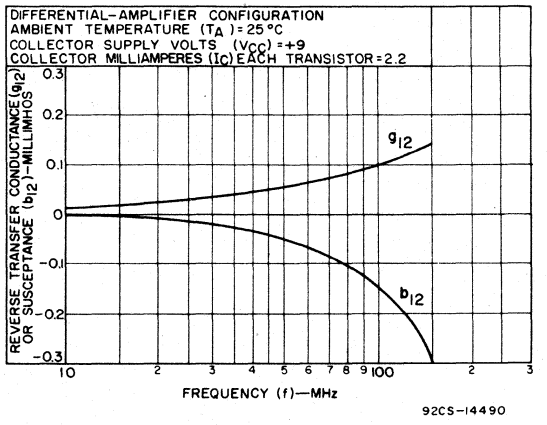


Fig.15 - Reverse transadmittance (Y_{12}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

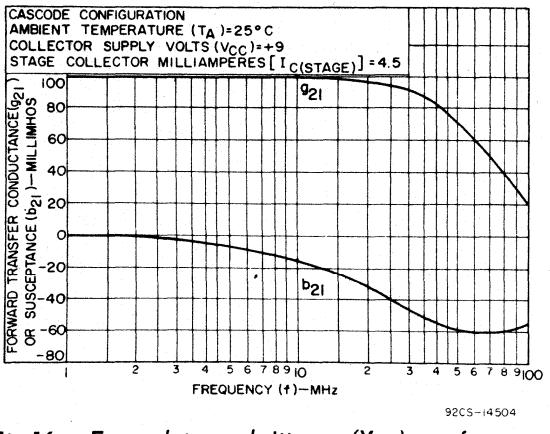


Fig.16 - Forward transadmittance (Y_{21}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

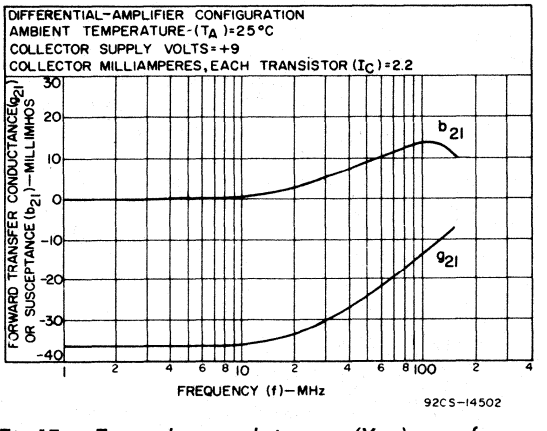


Fig.17 - Forward transadmittance (Y_{21}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

TYPICAL ADMITTANCE PARAMETERS

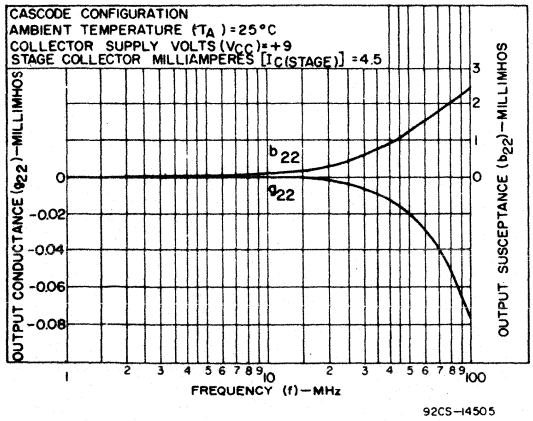


Fig.18 - Output admittance (Y_{22}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

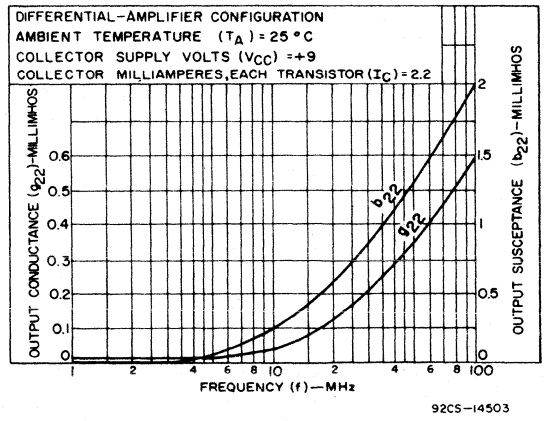


Fig.19 - Output admittance (Y_{22}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

TYPICAL TEST CIRCUITS AND CHARACTERISTICS

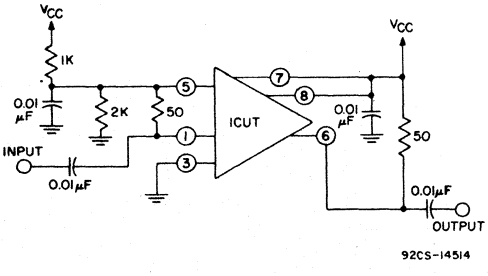


Fig.20a - Output power test circuit for CA3028A and CA3028B.

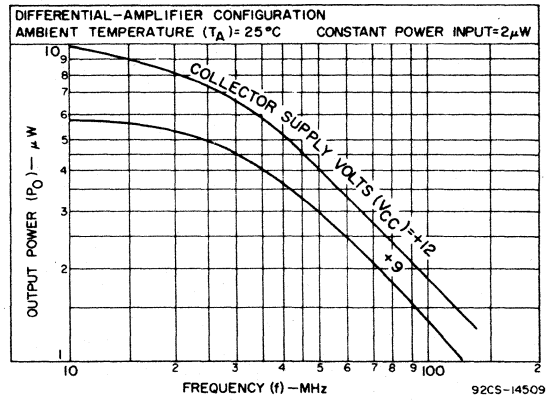
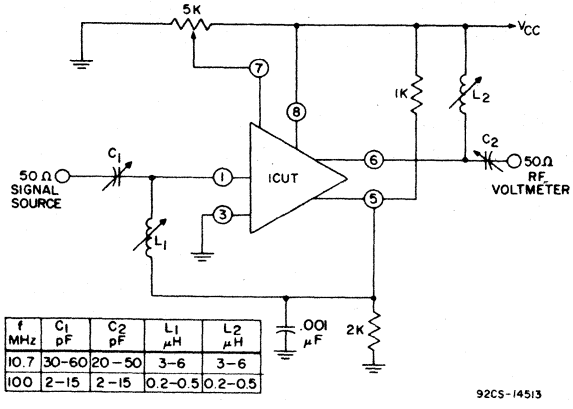


Fig.20b - Output power vs. frequency — 50 Ω input and 50 Ω output (differential-amplifier configuration) for CA3028A and CA3028B.



f MHz	C1 pF	C2 pF	L1 μH	L2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

Fig.21a - AGC range test circuit (differential amplifier) for CA3028A and CA3028B.

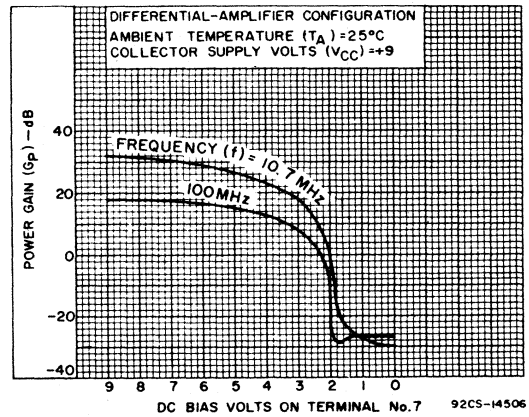


Fig.21b - AGC characteristics for CA3028A and CA3028B.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS

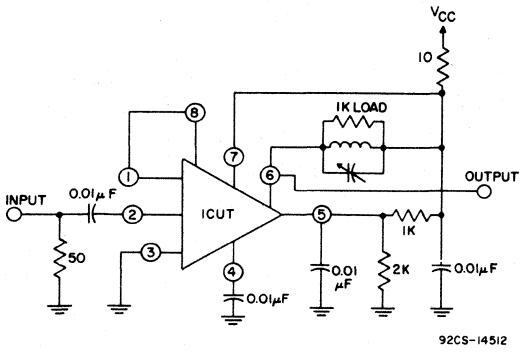


Fig.22a - Transfer characteristic (voltage gain) test circuit (10.7 MHz) cascode configuration for CA3028A, CA3028B and CA3053.

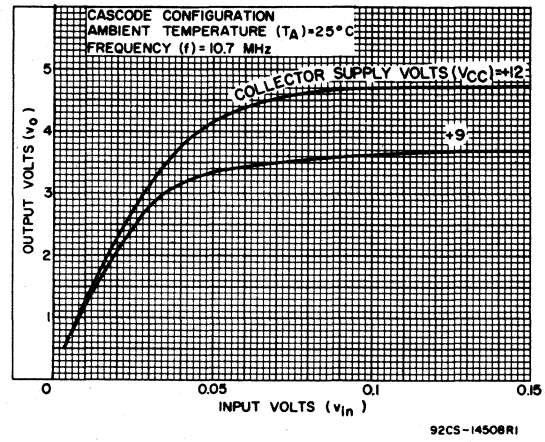


Fig.22b - Transfer characteristics (cascode configuration) for CA3028A, CA3028B and CA3053.

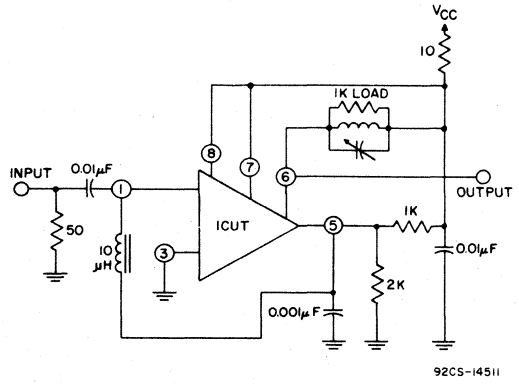


Fig.22c - Transfer characteristic (voltage gain) test circuit (10.7 MHz) differential-amplifier configuration for CA3028A, CA3028B and CA3053.

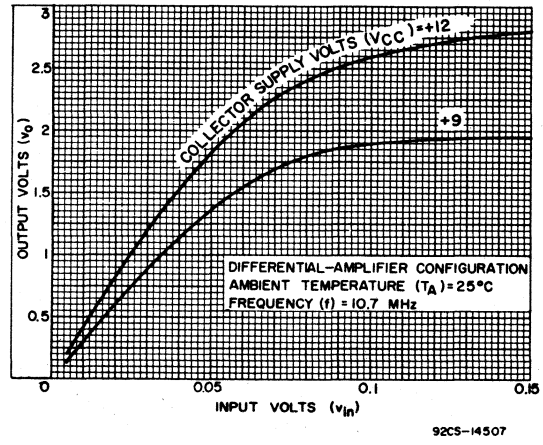
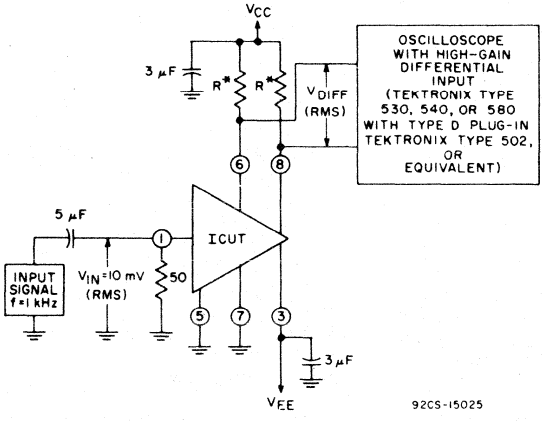
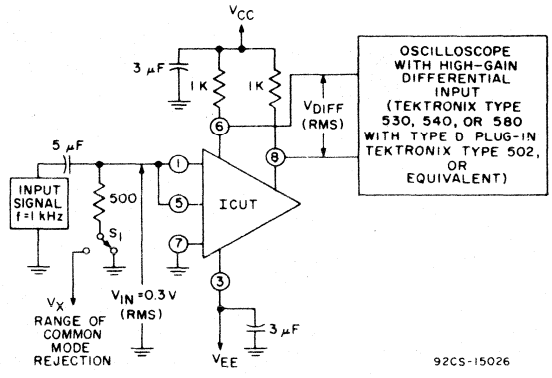


Fig.22d - Transfer characteristics (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.



* For R = 1.6 kΩ – (V_{CC} = 12V, V_{EE} = -12V)
For R = 2 kΩ – (V_{CC} = 6V, V_{EE} = -6V)

Fig.23 - Differential voltage gain, maximum peak-to-peak output voltage, and bandwidth test circuit for CA3028B.



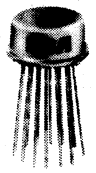
For CMR test: S_1 to ground
For input common-mode voltage range test: S_1 to V_X

Common mode rejection ratio = $20 \log_{10} \frac{(A^*)\ (2)\ (0.3)}{V_{DIFF}\ (RMS)}$

* A = Single-ended voltage gain.

Fig.24 - Common-mode rejection ratio and common-mode input-voltage range test circuit for CA3028B.

CA3040



12-Lead TO-5 Style

H-1463

Video and Wide-band Amplifier

For Industrial and Commercial Equipment at Frequencies up to 200 MHz

Features:

- *High differential push-pull voltage gain - 37 dB typ.*
- *Single-ended voltage gain - 31 dB typ.*
- *Wide [3dB] bandwidth - 55 MHz typ.*
- *Balanced input and output*
- *High input resistance - 150 kΩ typ.*
- *Low output resistance - 125 Ω typ.*
- *Bias options for temperature compensation:*
  Bias Mode A: "Constant" Voltage
  Bias Mode B: "Constant" Gain

Applications

- *Video amplifier*
- *Schmitt trigger*
- *Modulator*
- *IF Amplifier*
- *Mixer*
- *DC Amplifier*
- *Sense Amplifier*

The RCA CA3040 is a monolithic silicon integrated circuit designed to meet the requirements of a wide variety of applications requiring high gain and wide bandwidth. The cascode-connected differential amplifier achieves a double-ended gain of 37 dB with a typical 3 dB bandwidth of 55 MHz. Emitter-Follower input and output stages provide the desirable high input impedance and output impedance for coupling to other circuits.

The CA3040 includes two biasing options, allowing the user to optimize his design over the entire military temperature range of −55 to +125° C. **Bias Mode A** yields a substantially constant voltage at the output terminals for applications using DC coupling to succeeding stages or requiring maximum dynamic range over the temperature range. DC output voltage varies less than 0.1 volt (typically) over the entire temperature range while gain varies ± 2 dB. **Bias Mode B** provides extremely stable gain over the temperature range. Gain variation is 0 dB (typically) in this Bias Mode. DC variation is ± 0.8 volt.

Provisions are also made for stabilizing the operating point for either single or split power supplies.

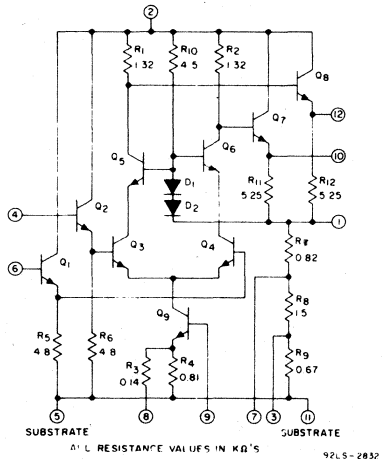


Fig. 1 — Schematic Diagram for CA3040.

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION * . . . . . 450 mW
Derating factor for T_A > 85°C . . . . . 5 mW/°C
TEMPERATURE RANGE:
Operating . . . . . -55°C to +125°C
Storage . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

* Limitation imposed by the thermal resistance of package.

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 2 with respect to terminal 11 is 0 to +14 volts.

TERMINAL No.	1	2	3	4	5▲	6	7	8	9	10	11▲	12
1		0 -14	*	*	+14 0	*	+10 -10	*	*	*	+14 0	*
2			*	+14 0	+14 0	+14 0	*	*	*	+14 0	+14 0	+14 0
3				*	+5 -3	*	*	*	*	*	+5 -3	*
4					*	+3 -3	*	*	*	*	*	*
5▲					▲	*	+10 -3	*	+3 -7	*	0 Note 1	*
6							*	*	*	*	*	*
7								*	*	*	+10 -3	*
8									+3 -3	*	*	*
9										*	+7 -3	*
10											*	*
11▲											▲	*
12												

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	5
2	-	-
3	5	5
4	1	0.1
5	-	-
6	1	0.1
7	5	5
8	5	5
9	1	0.1
10	-	10
11	-	-
12	-	10

▲ Reference Substrate

Note 1: External connection required for proper operation.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

CA3040

ELECTRICAL CHARACTERISTICS AT T_A = 25°C Unless Otherwise Specified

Characteristics	Symbols	Test Circuits	Special Test Conditions	Limits CA3040			Units	Typical Characteristics Curves
		Fig.		Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS	V_{CC} = +6V, V_{EE} = -6V							
Output Voltage	V_{10} or V_{12}	2(a) 2(b)	Bias Mode Switch A or B: Closed	1.4	2.7	3.7	V	9
Base Bias Voltage	V_9	2(a)	Bias Mode A Switch Closed	-	-1.7	-	V	-
		2(b)	Bias Mode B Switch Closed	-	-1.7	-	V	-
Input Bias Reference Voltage	V_1	2(a) 2(b)	Bias Mode Switch A or B: Open	-1	-	+1	V	9
Input Bias Current	I_4, I_6	2(a) 2(b)	Bias Mode Switch A or B: Closed	-	15	45	μA	-
Input Unbalance Current	$\lvert I_6-I_4 \rvert$	2(a) 2(b)	Bias Mode Switch A or B: Closed	-	-	6	μA	-
Power Supply Current Drain	I_2 or I_5+I_{11}	2(a)	Mode A Switch open or closed	4.7	8.5	15.5	mA	10
	I_2 or $I_5+I_8+I_{11}$	2(b)	Mode B Switch open or closed					
DYNAMIC CHARACTERISTICS	V_{CC} = +12V, V_{EE} = 0, Split Voltage Supply (Optional) = +6V							
Differential Voltage Gain								-
Single-Ended Input Differential Output	$A_{DIFF(DE)}$	3(a)	f = 1 MHz R_S = 50 Ω	34	37	-	dB	-
Single-Ended Input and Output	$A_{DIFF(SE)}$	3(a)	f = 1 MHz R_S = 50 Ω	28	31	-	dB	4,5
-3 dB Bandwidth	BW	3(a)	R_S = 50 Ω	40	55	-	MHz	4,7
Differential Voltage Gain Balance	$A_{DIFF(SE)10}$ $-A_{DIFF(SE)12}$	3(a)	f = 1 MHz	-1	0	+1	dB	-
Output Voltage Swing	V_8 or V_{10} RMS	3(a)	f = 1 MHz R_S = 50 Ω	-	0.5	-	V_{RMS}	7
Noise Figure	NF	3(a)	(Note 1) f = 30 MHz R_S = 400 Ω	-	7.5	9	dB	8
Parallel Input Resistance	R_I	3(a)	f = 1 MHz	-	150	-	kΩ	-
Parallel Input Capacitance	C_I	3(a)		-	2.2	-	pF	-
Output Resistance	R_O	3(a)		-	125	-	Ω	-
TEMPERATURE DEPENDENT CHARACTERISTICS Temperature coefficients for ambient temperature: -55°C ≤ T_A ≤ + 125°C								
Output Voltage	$\frac{\Delta V_{10} \text{ or } \Delta V_{12}}{°C}$	3(a)	Bias Mode A	-	0	-	mV/°C	9
		3(b)	Bias Mode B	-	6.4	-	mV/°C	
Power Supply Current Drain	$\Delta I_2/°C$	3(a)	Bias Mode A	-	5	-	μA/°C	11
Differential Voltage Gain	$A_{DIFF}/°C$	3(a)	Bias Mode A	-	0.0166	-	dB/°C	12
		3(b)	Bias Mode B	-	0	-		

Note 1: Replace 1-kΩ resistors between Term. 1 and 4 and Te .. 1 and 6 with suitable chokes so that reactance at 30 MH_z exceeds 5kΩ

STATIC CHARACTERISTICS TEST CIRCUITS FOR CA3040

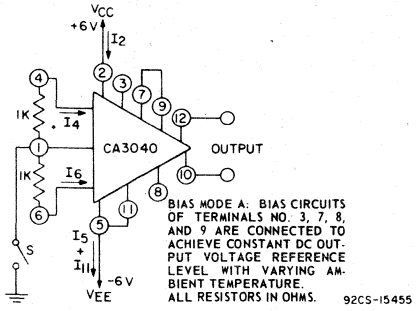


Fig.2(a) - Bias Mode A

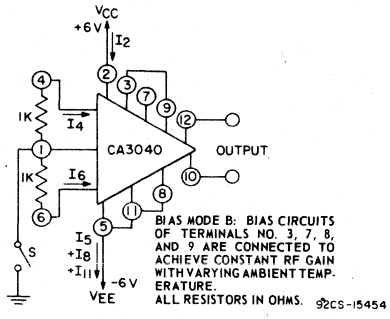
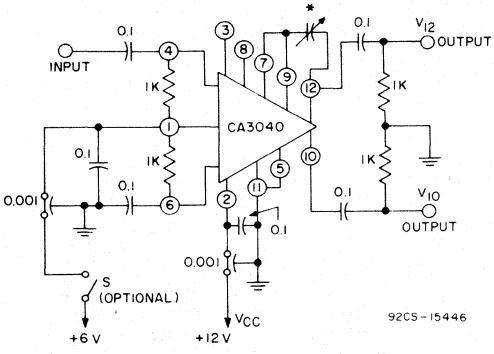


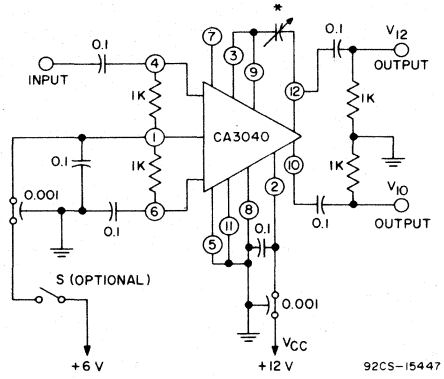
Fig.2(b) - Bias Mode B

DYNAMIC CHARACTERISTICS TEST CIRCUITS FOR CA3040



* VARIABLE CAPACITANCE (0.5 – 1.0 μF) ADJUSTMENT FOR EQUAL 3dB BANDWIDTH AT AMPLIFIER OUTPUTS, TERMINALS 10 AND 12.
ALL RESISTORS IN OHMS.
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED).
BIAS MODE A IS AS DEFINED IN FIG. 2(a)

Fig.3(a) - Bias Mode A



* SEE FIG 3(a)
BIAS MODE B IS AS DEFINED IN FIG 2(b)
ALL RESISTORS IN OHMS.
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED).

Fig.3(b) - Bias Mode B

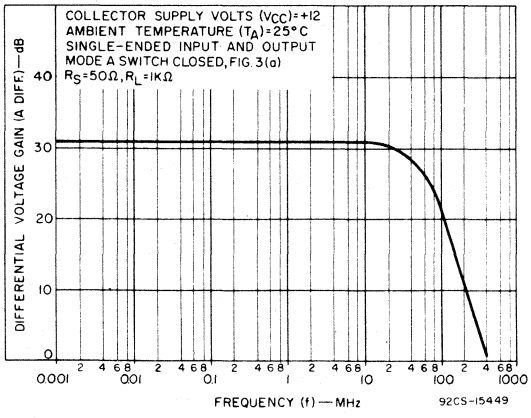


Fig.4 - Differential Voltage Gain vs Frequency

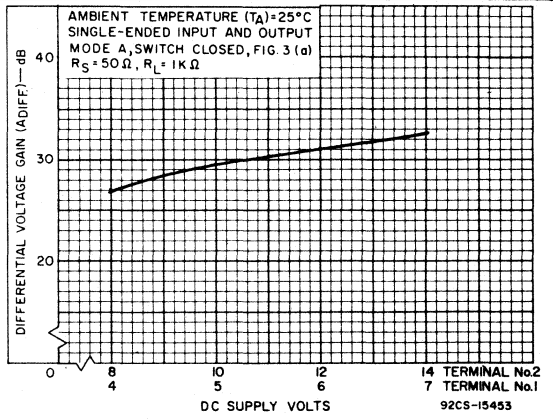


Fig.5 - Differential Voltage Gain vs DC Supply Voltages

CA3040

OPERATING CONSIDERATIONS

General

The CA3040 is designed to provide flexibility in the selection of power supply configurations and to provide the circuit designer the choice between two modes of temperature-compensated performance. Mode A, which provides constant DC output voltage, is recommended for most applications. The control of the operating point provided by this mode maintains the dynamic range of the device while gain variation over most of the range is less than ±1 dB. Mode B provides constant gain for applications where this consideration is critical, but will exhibit a reduction of dynamic range at the temperature extremes.

Power Supply Considerations

Figures 2 and 3 illustrate the use of the CA3040 with balanced dual supplies and single power supplies, respectively. Both figures demonstrate that the inputs may be directly referenced to the center point of the supply (ground in Fig.2) by closing the included switch. This is the natural connection in Fig.2. This connection is optional, however, and need not be made. Use of this connection in Fig.3 implies the presence of another DC supply or a "stiff" bleeder. If such a source is present its use is suggested in order to maintain maximum common mode range. Dynamic performance and dynamic range of the output circuit are unaffected by the choice of biasing scheme used so that in most cases direct connection of Terminal No.1 to the center point of the supply is not required. Where direct connection is not used, Terminals No.4 and No.6 must be biased from Terminal No.1 for proper operation.

High-Frequency Considerations

Stable high-frequency operation requires that proper high-frequency construction techniques be followed. The photograph of Fig.6 illustrates the precautions taken in the construction of the test circuit of Fig.3.

Extreme caution is required because of the extended gain bandwidth capability of the device. Oscillations have been observed in the 400-to-800 MHz range when precautions were not taken. In addition to normal considerations of shielding, parts layout, and isolation, the following specific suggestions are made:

1. Use sockets only when necessary. Sockets, when used, must provide shielding within the pin circle. The socket shown in the chassis of Fig.6 is a Barnes MG-1201, or equivalent, modified by drilling a 1/8" hole in the center and inserting a grounded brass pin.
2. Do not bypass Terminal No.9 in normal operation. Fig.3 shows the use of neutralization between Terminal No.9 and one output to balance the amplifier at high frequencies. Experience shows that stable operation, while possible, is difficult to achieve if Terminal No.9 is bypassed to ground.
3. In DC testing, 1 kΩ, 1/4 W carbon resistors should be soldered directly to the socket Terminals No.4 and No.6 to suppress parasitic oscillations. All current carrying connections are made at the other end of the resistors. Direct sensing of Terminal No.4 or No.6 voltage should not be attempted.

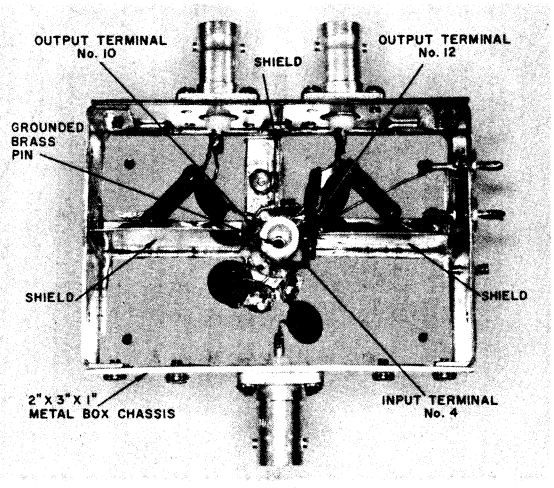


Fig.6 - Test Circuit Layout

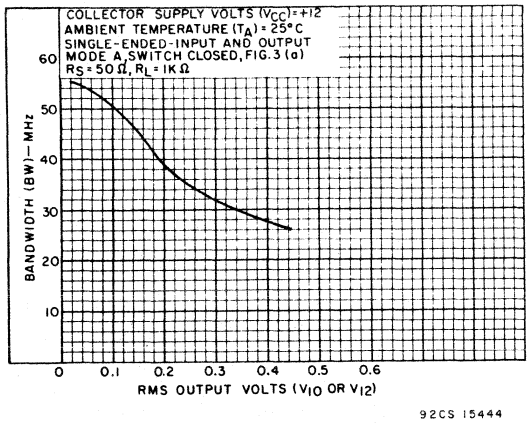


Fig.7 -3dB Bandwidth vs Single-Ended Output Voltage

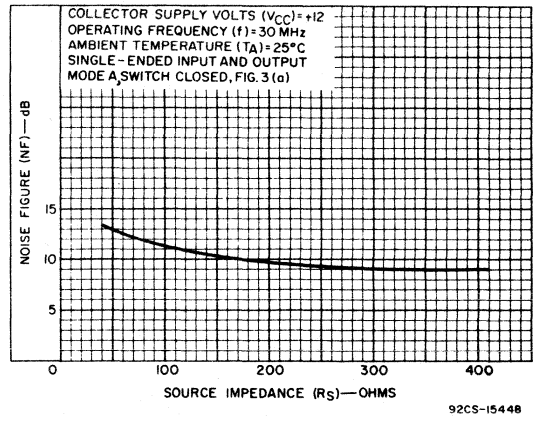


Fig.8 -Noise Figure (NF) vs Source Impedance

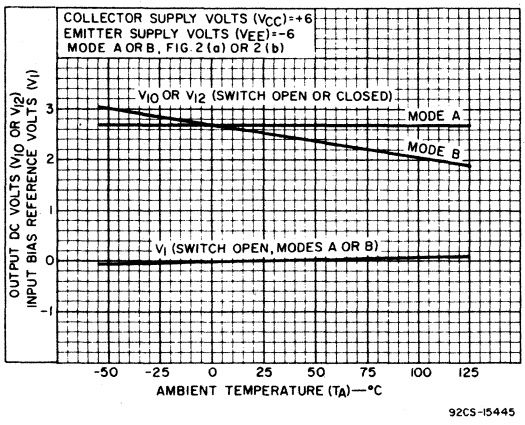


Fig.9 - Output Volts or Input Bias Reference Volts vs Ambient Temperature

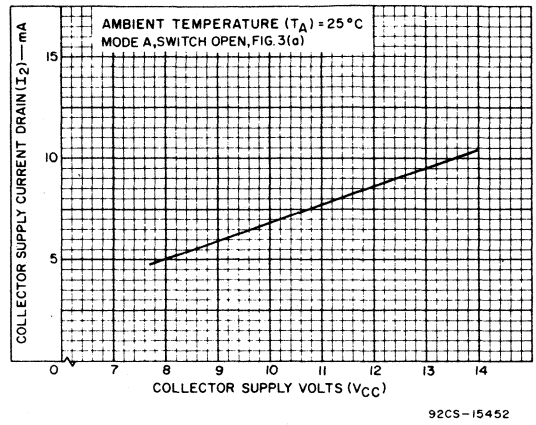


Fig.10 -Collector Supply Current Drain (I_2) vs Collector Supply Voltage (V_{CC})

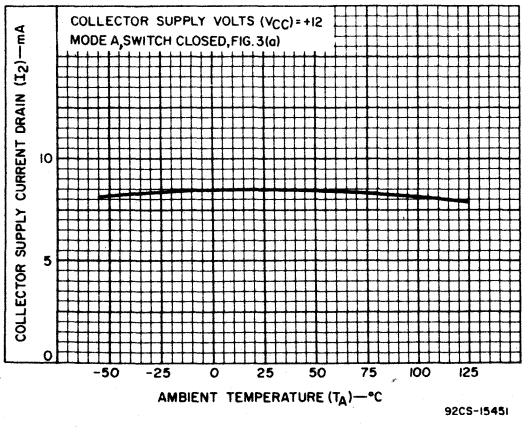


Fig.11 - Collector Supply Current Drain (I_2) vs Ambient Temperature

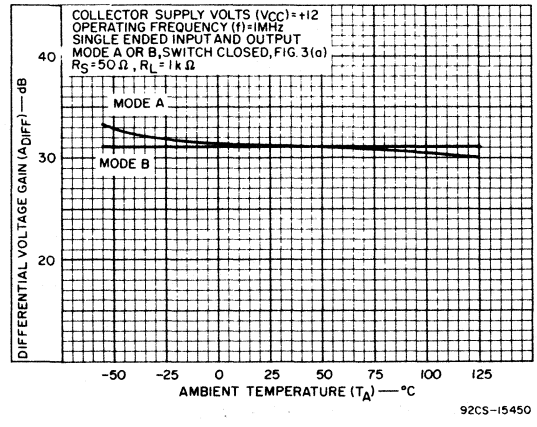


Fig.12 - Single-Ended Differential Voltage Gain vs Ambient Temperature

Special Function Circuits
Technical Data

Automotive Circuits

Broadband (Video) Amplifiers

Four Quadrant Multiplier

Prescalers

Single-Chip Detector Alarm Systems

Timer

*BIMOS types

CA3002

10-Lead TO-5

H-1384

IF Amplifier

For Use in Communication Equipment

Features:

- *Input resistance - 100 kΩ typ.*
- *Output resistance - 70 Ω typ.*
- *Voltage gain - 24 dB typ. @ 1.75 MHz*
- *Push-pull input, single-ended output*
- *-3 dB bandwidth - 11 MHz typ.*
- *AGC range - 80 dB typ.*
- *Useful frequency range DC to 15 MHz.*

Applications:

- *Product detector*
- *IF & video amplifier*
- *AM detector*
- *Schmitt trigger*

The RCA-CA3002 integrated-circuit IF amplifier is a balanced differential amplifier that can be used with either a single-ended or a push-pull input and can provide either a direct-coupled or a capacitance-coupled single-ended output. Its applications include RC-coupled IF amplifiers that use the internal silicon output-coupling capacitor, video amplifiers that use an external coupling capacitor, envelope detectors, product detectors, and various trigger circuits.

The CA3002 is supplied in the 10-lead hermetic TO-5 style package.

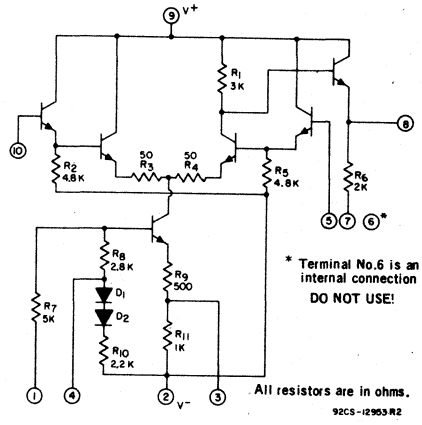


Fig. 1 — Schematic diagram.

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, *at* $T_A = 25°C$

COMMON-MODE INPUT SIGNAL VOLTAGE . . . . . ±2 V
MAXIMUM POWER SUPPLY VOLTAGE . . . . . 16 V or ±8 V
OPERATING-TEMPERATURE RANGE . . . . . −55°C to +125°C
STORAGE-TEMPERATURE RANGE . . . . . −65°C to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265°C
MAXIMUM INPUT-SIGNAL VOLTAGE . . . . . ±4 V
MAXIMUM DEVICE DISSIPATION:
−55 to 85°C . . . . . 450 mW
Above 85°C . . . . . Derate linearly 5 mW/°C

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$, $V_{CC} = +6$ V, $V_{EE} = -6$ V

CHARACTERISTICS	SPECIAL TEST CONDITIONS TERMINALS No. 3 & No.4 NOT CONNECTED UNLESS OTHERWISE NOTED	TEST CIRCUITS	LIMITS CA3002			UNITS
		Fig.	Min.	Typ.	Max.	
STATIC CHARACTERISTICS						
Input Unbalance Voltage V_{IU}		4	–	2.2	–	mV
Input Unbalance Current I_{IU}		5	–	2.2	10	μA
Input Bias Current I_I		5	–	20	36	μA
Quiescent Operating Voltage	MODE: TERMINAL 2 / TERMINAL 4					
	A: V_{EE} / NC	7a	–	2.8	–	V
	B: V_{EE} / V_{EE}	8b	–	3.9	–	V
Device Dissipation P_T		4	–	55	–	mW
DYNAMIC CHARACTERISTICS						
Differential Voltage Gain A_{DIF} (Single-Ended Input and Output)	f = 1.75 MHz	10	19	24	–	dB
Bandwith at −3 dB Point BW	–	10	–	11	–	MHz
Maximum Output Voltage Swing $V_{OUT(P-P)}$	–	10	–	5.5	–	V_{P-P}
Noise Figure NF	f = 1.75 MHz R_S = 1 kΩ	12	–	4	8	dB
Input Impedance Components: Parallel Input Resistance R_{IN}	f = 1.75 MHz	None	–	100k	–	Ω
Parallel Input Capacitance C_{IN}	f = 1.75 MHz	None	–	4	–	pF
Output Resistance R_{OUT}	f = 1.75 MHz	14	–	70	–	Ω
3rd Harmonic Intermodulation Distortion IMD	–	16	−30	−40	–	dB
AGC Range (Maximum Voltage Gain to Complete Cutoff AGC	f = 1.75 MHz	18	60	80	–	dB

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, *at* $T_A = 25°C$

Indicated voltage or current limits for each terminal can be applied under the specified operating conditions for other terminals.

All voltages are with respect to ground ($-V_{CC}$, $+V_{EE}$) or common terminal of Positive and Negative DC supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	−8 V	0 V	2, 7 5, 10 9	−8 0 +6
2	−10 V	0 V	1, 5, 10 9	0 +6
3	−8.5 V	0 V	1, 5, 10 7 9	0 −6 +6
4	−8 V	0 V	1, 5, 10 2, 7 9	0 −8 +6
5	−3.5 V	+3.5 V	1, 10 2, 7 9	0 −6 +6
6	INTERNAL CONNECTION DO NOT USE			
7	−12 V	0 V	1, 5, 10 2 9	0 −6 +6
8	20 mA		1, 5, 10 2 9 200 Ω Resistor Between Terminals 7 & 8	0 −6 +6
9	0 V	+10 V	1, 5, 10 2, 3, 7	0 −6
10	−3.5 V	+3.5 V	1, 5 2, 7 9	0 −6 +6
CASE	INTERNALLY CONNECTED TO TERMINAL No.2 (SUBSTRATE) DO NOT GROUND			

STATIC CHARACTERISTICS

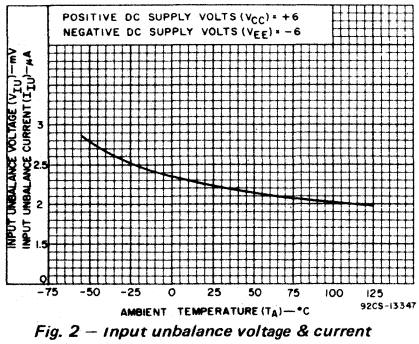


Fig. 2 — Input unbalance voltage & current vs temperature.

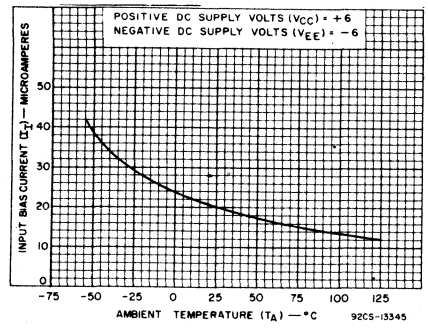


Fig. 3 — Input bias current vs temperature.

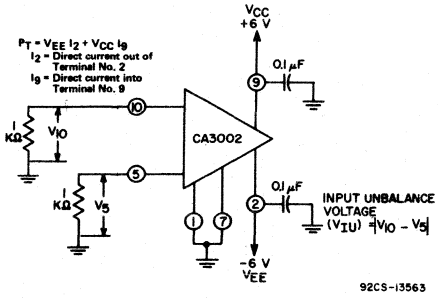


Fig. 4 – Input unbalance voltage and device dissipation test circuit.

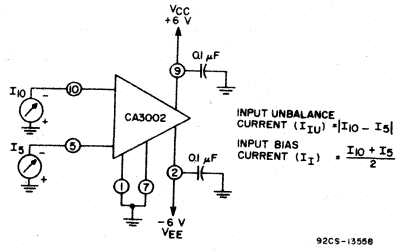


Fig. 5 – Input unbalance current & bias current test circuit.

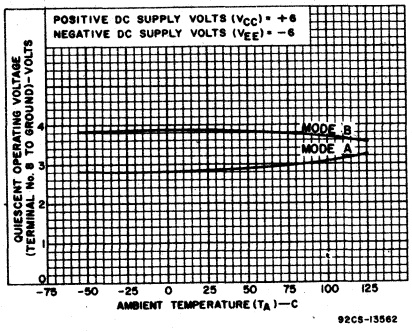


Fig. 6 – Quiescent operating voltage vs temperature.

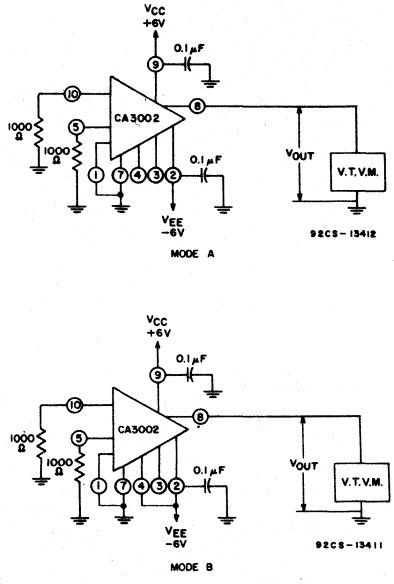


Fig. 7 – Quiescent operating voltage.

DYNAMIC CHARACTERISTICS

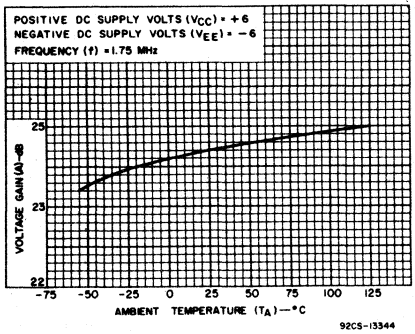


Fig. 8a – Differential voltage gain vs temperature.

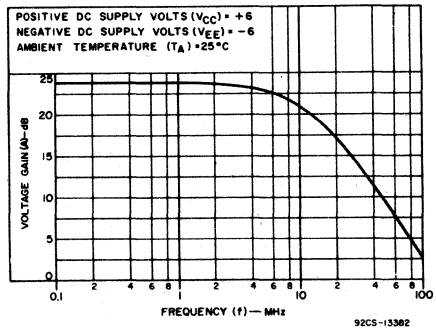


Fig. 8b – Differential voltage gain vs frequency.

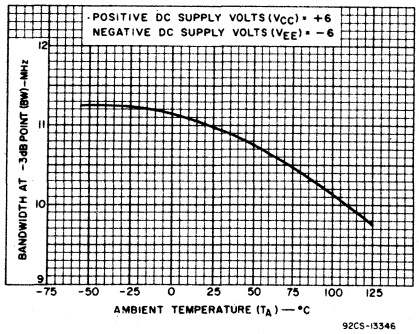


Fig. 9 — Bandwidth of −3 dB point vs temperature.

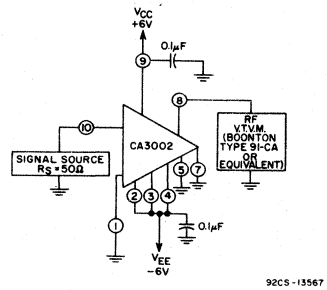


Fig. 10 — Differential voltage gain, −3 dB bandwidth, and maximum output voltage swing.

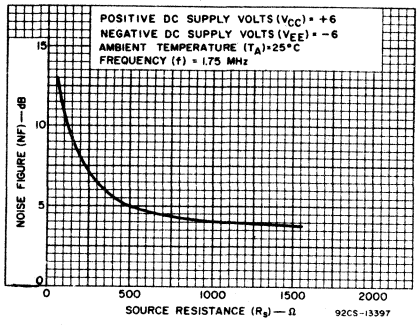
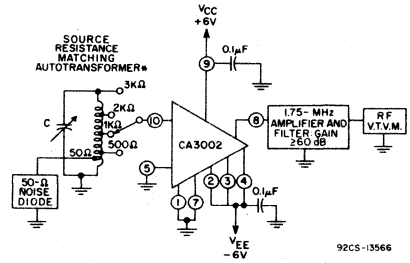


Fig. 11 — Noise figure vs source resistance.



* Taps are adjusted to provide indicated equivalent values of R_S with tank tuned to resonance at 1.75 MHz, and a 50-Ω resistor connected to simulate the noise diode.

Fig. 12 — Noise figure.

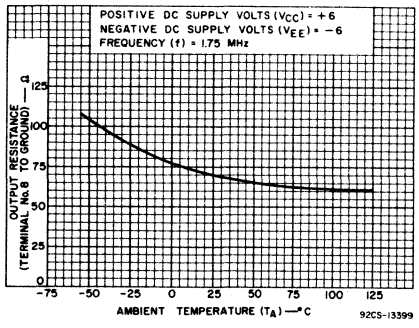


Fig. 13a — Output resistance vs temperature.

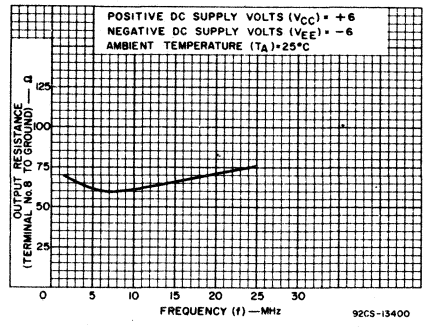


Fig. 13b — Output resistance vs frequency.

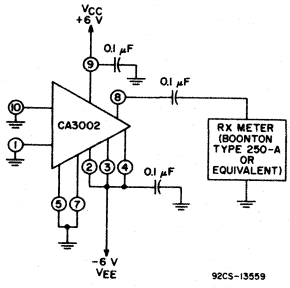


Fig. 14 — Output resistance.

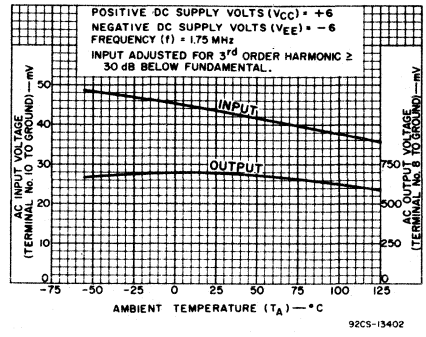
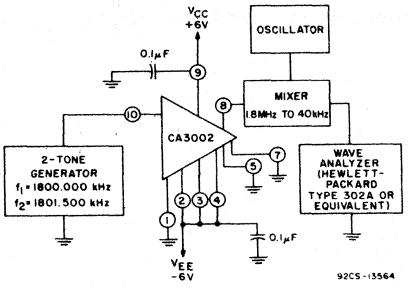


Fig. 15 — Input level for −30 dB intermodulation vs temperature.



1) Increase both input-signal tones until the $2f_2$-f1 and $2f_1$-f2 output-signal voltages are 30 dB below the f_1 and f_2 output-signal voltages.
2) Measure rms values of the input and output signal voltages.
3) The measured input signal voltage is that value when the 3rd-harmonic intermodulation products are 30 dB below the fundamental outputs.

Fig. 16 – Intermodulation circuit.

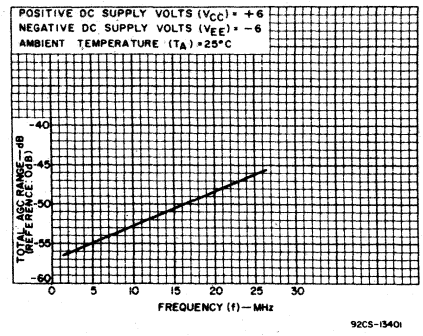
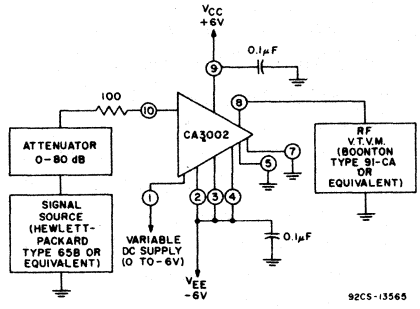


Fig. 17 – AGC range vs frequency.



1) Set attenuator at 80 dB attenuation.
2) Set variable dc supply voltage at 0 V.
3) Increase signal input voltage until RF V.T.V.M. indicates 5 mV output.
4) Set variable dc supply voltage at -6 V.
5) Adjust attenuator until RF V.T.V.M. again indicates 5 mV output.
6) Change in attenuator setting in dB is total AGC Range.

Fig. 18 – AGC range.

CA3091D

14-Lead Dual-In-Line Ceramic Package H-1553

Four-Quadrant Multiplier

Applications:

- **Multiplier** ■ **Divider** ■ **Squarer** ■ **Square Rooter**
- **Power-series approximator**
- **Full-wave rectifier**
- **Automatic level controller**
- **RMS converter**
- **Frequency discriminator**
- **Voltage-controlled filters and oscillators**

RCA-CA3091D*, a monolithic silicon integrated circuit, is a four-quadrant multiplier that provides an output voltage that is the product of two input (x and y) voltages.

This device functions as a multiplier, divider, squarer, square rooter, and power-series approximator. In addition, this device is useful in applications such as ideal full-wave rectifiers, automatic level controllers, RMS converters, frequency discriminators, and voltage-controlled filters and oscillators.

The CA3091D comprises five basic circuits (See Fig. 1), including: a multiplier block, two linearity compensators, a current converter, a current source for biasing, and a regulator (reference voltage). A brief description of the operation, functions and typical applications is given in the section "Operating Considerations". In addition there is a separate section on "Symbols, Terms, and Definitions" that defines the terms and symbols used throughout the data bulletin.

The CA3091D is supplied in 14-lead dual-in-line ceramic package and operates over the full military temperature range of -55°C to +125°C.

* Formerly Developmental Type TA5855A.

Features: ●

- **"Accuracy": ±4% (max.)**
- **"Linearity": 3.0% (max.)**
- **Feedthrough: 9 mV p-p (typ.)**
- **3-db bandwidth: 4.4 MHz**
- **Low power operation capability: ±6.0 V, 4 mW drain**
- **Low power-supply sensitivity: 36 mV/V typ.**
- **Smooth overload characteristics — no foldback if full-scale input signal is exceeded**
- **Negligible warm-up drift**
- **Broadband operation capability (flat to 1 MHz) — both inputs have similar characteristics for reduced high-frequency phase shift between the inputs**
- **Low-level linearity correction circuitry minimizes low-level feedthrough for improved small-signal accuracy**
- **All multiplication is performed with wideband circuitry — this permits two signals of frequencies much higher than the -3 db frequency of the multiplier to produce a difference frequency that is within the multiplier's bandwidth**
- **High immunity to parasitic oscillation**
- **Essentially free from excess peaking — provides improved frequency response**
- **Requires no level shifting at the output — current-source operation at the output permits output signal to be referenced to ground or other levels within the output voltage swing capabilities of the multiplier**
- **Internal bias regulator**

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DC Supply Voltages:		
Between Terms. 12 and 1	+18	V
Between Terms. 4 and 1	−18	V
DC Supply Currents:		
At Term. 12 with DC Supply Voltage = +15 V	4	mA
At Term. 4 with DC Supply Voltage = −15 V	16	mA
Bias Current (At Term. 3)	1	mA
* Input Current	±1	mA
Output Short-Circuit Duration	No limitation	
Voltage Reference Current	10	mA
Linearity Correction Currents:		
At Terminals 7 and 8	10	mA
Device Dissipation (Up to 125°C)	200	mW
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (during soldering):		
At distance not less than 1/32 inch (0.79 mm) from case for 10 seconds max.	+265	°C

* External resistance is required to limit the current to the indicated ±1 mA value.

ELECTRICAL CHARACTERISTICS, For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: T_A = 25°C, I_{IB} = 0.5 mA, V^+ = 15 V, V^- = -15 V	Circuit and/or Char. Curve	LIMITS: Min.	Typ.	Max.	UNITS
STATIC CHARACTERISTICS							
INPUT CIRCUIT							
Input Balance (Correction) Currents:							
At x Input	I_{IC}	x = 0	–	−20	−2.1	+20	μA
At y Input		y = 0	–	−20	−8.7	+20	μA
Feedthrough Linearity Balance (Correction) Current	I_{OC}		–	−34	−2.9	+34	μA
OUTPUT CIRCUIT							
Output Offset Current	I_{OO}	x & y = O,	–	−10	−0.23	+10	μA
Output Offset Voltage	V_{OO}	I_{OO} thru R_L = 33kΩ	–	−0.330	−0.0076	+0.330	V
Output Peak Current Swing	$\|I_O\|$	Thru R_L = 24kΩ	3	0.41	0.45	–	mA
Output Peak Voltage Swing	$\|V_O\|$	Across R_L = 33kΩ	4	12	12.9	–	V
DC SUPPLIES & BIASING							
Current Drain (Idling):							
At Term. 4		V^- = -15 V	–	–	2.9	4.5	mA
At Term. 12		V^+ = +15 V	–	–	2.0	3.0	mA
Reference Voltage	V_{ref}	Measured across Terms. 6 & 4 at I = 1mA	–	5.5	6.1	6.7	V
DYNAMIC CHARACTERISTICS							
Output Current	I_O	With I = 0.2mA at each input	–	–	0.21	0.32	mA
Normalized k Factor $\left(k_N = \frac{k}{k_r}\right)$			11	0.69	1.0	1.7	
Accuracy		Worst case at 25°C	–	–	2.6	4.0	% of 10 V
Linearity				–	1.7	3.0	
Feedthrough Voltage:							
At y = 20V p-p, x = O			–	–	9	20	mV p-p
At x = 20V p-p, y = O			–	–	9	20	

NOTE: See page 7 for "Symbols, Terms and Definitions".

ELECTRICAL CHARACTERISTICS, Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: T_A = 25°C, I_{IB} = 0.5 mA, V^+ = 15 V, V^- = −15 V	Circuit and/or Char. Curve	TYPICAL VALUES	UNITS
STATIC CHARACTERISTICS					
INPUT CIRCUIT					
Input Resistance:					
At x Input	R_I	$\lvert I_x \rvert \leq 0.2$ mA	5	1.3	kΩ
At y Input		$\lvert I_y \rvert \leq 0.2$ mA		0.5	kΩ
Input Capacitance:					
At x Input	C_I	at 1 MHz	–	5.8	pF
At y Input				5.8	pF
OUTPUT CIRCUIT					
Output Resistance	R_O		6	1.0	MΩ
Output Capacitance:	C_O	at 1 MHz		4.0	pF
DC Supply Voltage Sensitivity:					
At Term. 4	$\frac{\Delta V_O}{\Delta V^-}$		11	26	mV/V
At Term. 12	$\frac{\Delta V_O}{\Delta V^+}$			36	mV/V
DYNAMIC CHARACTERISTICS					
Bandwidth (At -3dB point):					
Through x Input	BW		8, 10	4.8	MHz
Through y Input			8, 9	4.4	MHz
3° Error Frequency:					
Through x Input			–	360	kHz
Through y Input				310	kHz
Maximum Slew Rate	SR	7pF in parallel with 10 MΩ load	7	27	V/μs
Temperature Coefficients:					
Output Offset Current	$\Delta I_{OO}/\Delta T$	x & y = 0	–	−0.021	μA/°C
x-Input Balance Current	$\Delta I_{IC}/\Delta T$	x = 0	–	−0.063	μA/°C
y-Input Balance Current		y = 0	–	−0.063	μA/°C
Normalized k Factor $\left(k_N = \frac{k}{k_r}\right)$	k_N		–	−0.76	%/%/°C
Accuracy			–	0.11	%/°C
Linearity			–	0.06	%/°C
Feedthrough:					
At x = 0			–	5.6	mV/°C
At y = 0				5.7	mV/°C

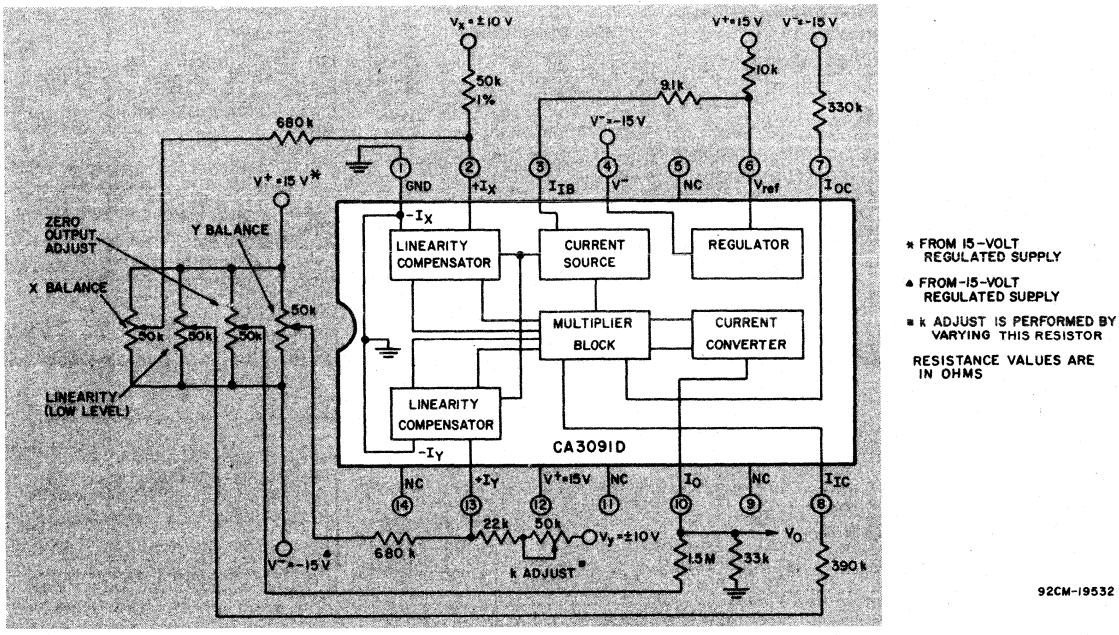


Fig.1—Functional block diagram of CA3091D with typical multiplier outboard (peripheral) circuitry.

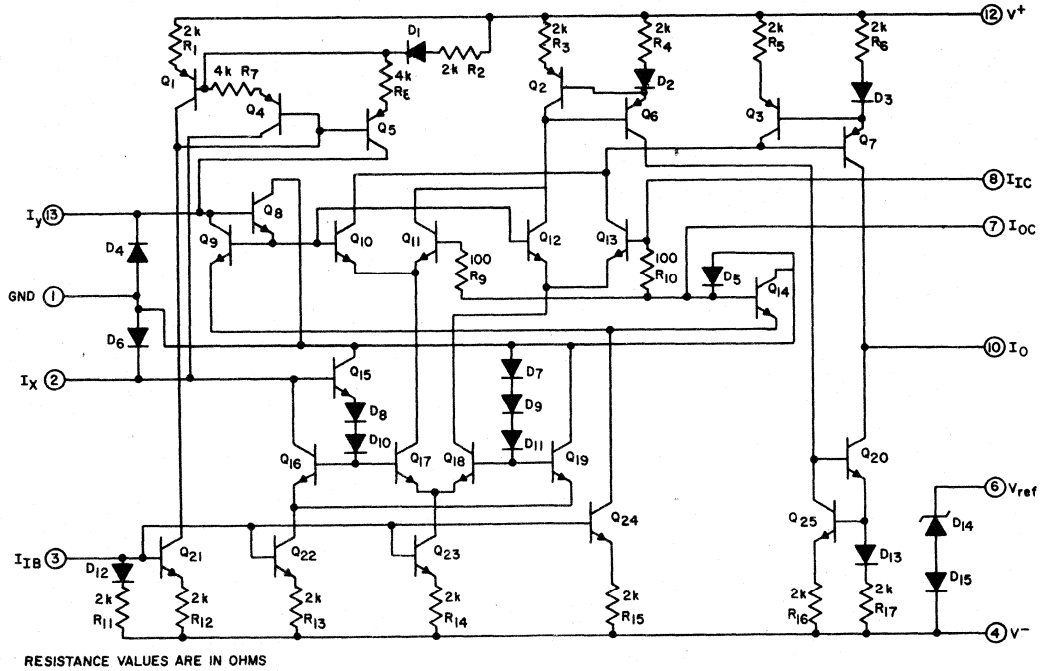


Fig.2—Schematic diagram of the CA3091D.

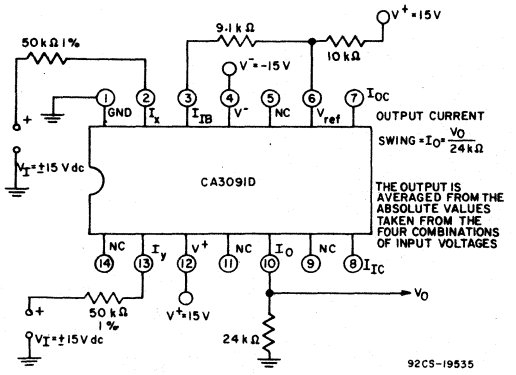


Fig.3—Test circuit for measurement of output current swing capability.

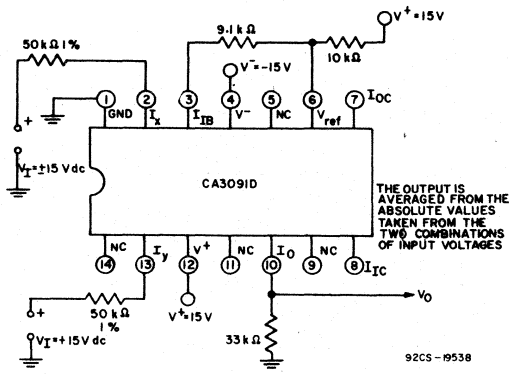


Fig.4—Test circuit for measurement of output voltage swing capability.

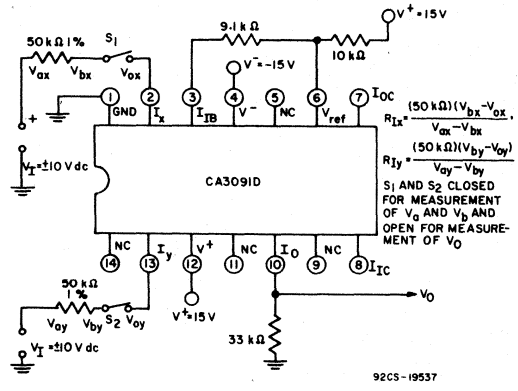


Fig.5—Test circuit for measurement of input resistance.

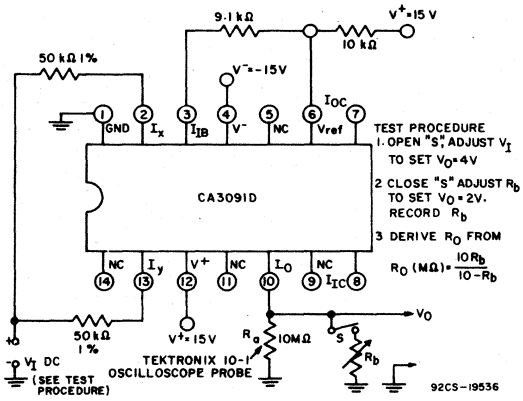


Fig.6—Test circuit for measurement of output resistance.

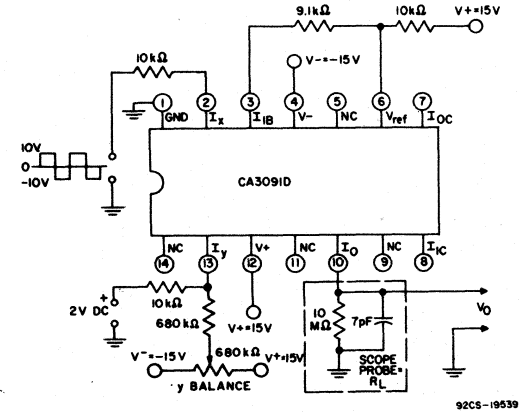


Fig.7—Test circuit for measurement of maximum slew rate.

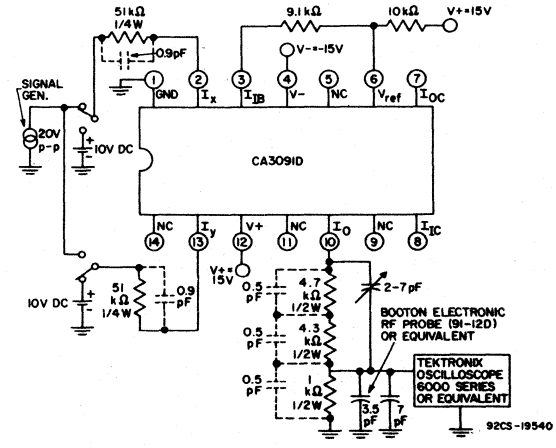


Fig.8—Test circuit for measurement of frequency response.

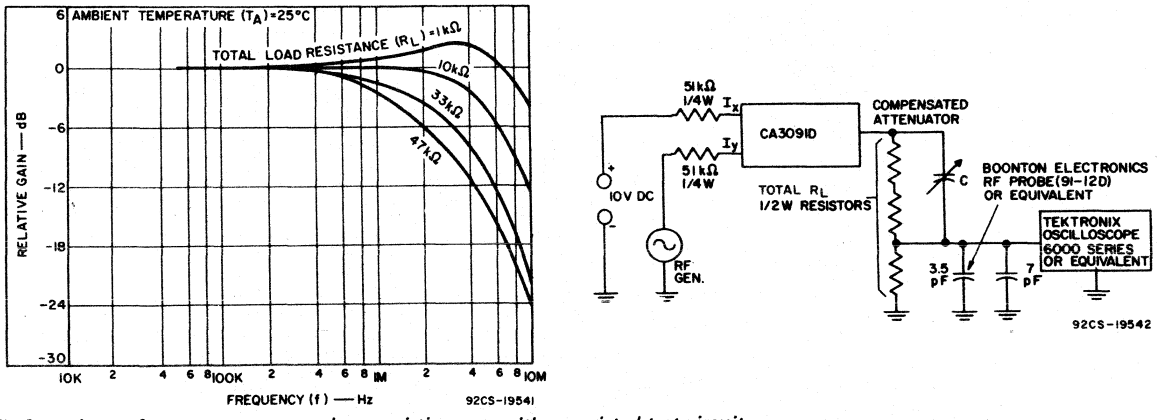


Fig.9- y—input frequency response characteristic curve with associated test circuit.

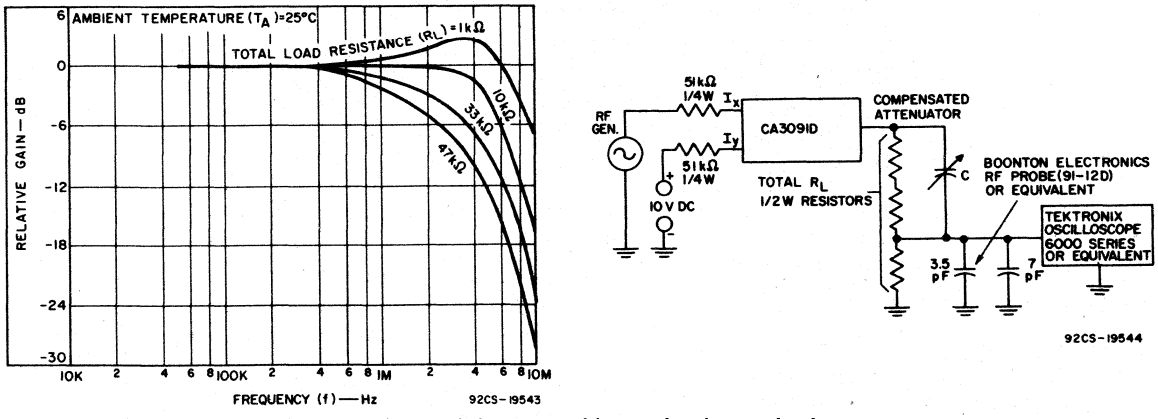


Fig.10- x—input frequency response characteristic curve with associated test circuit.

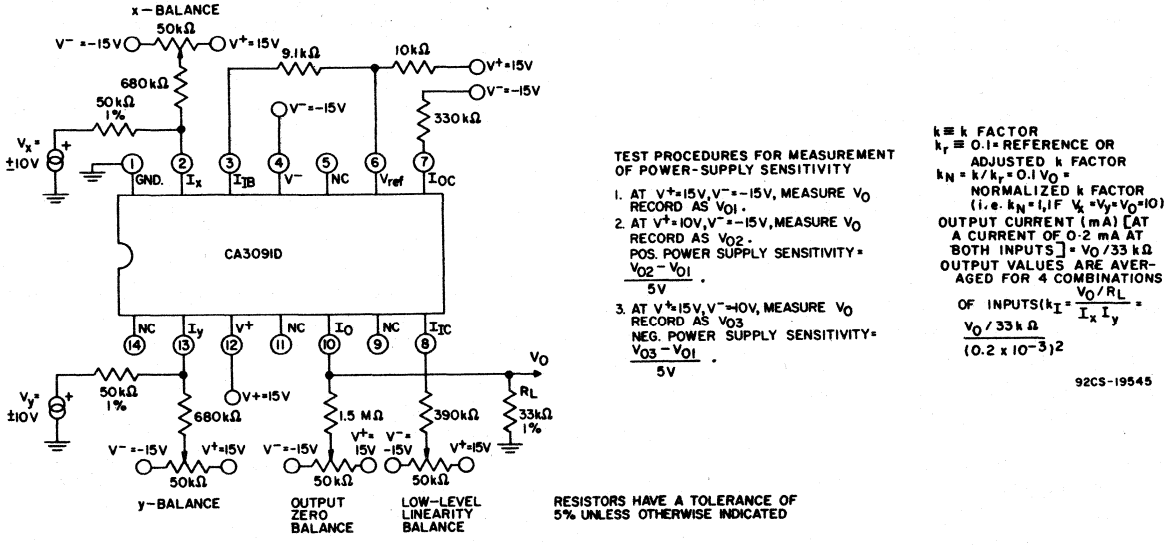
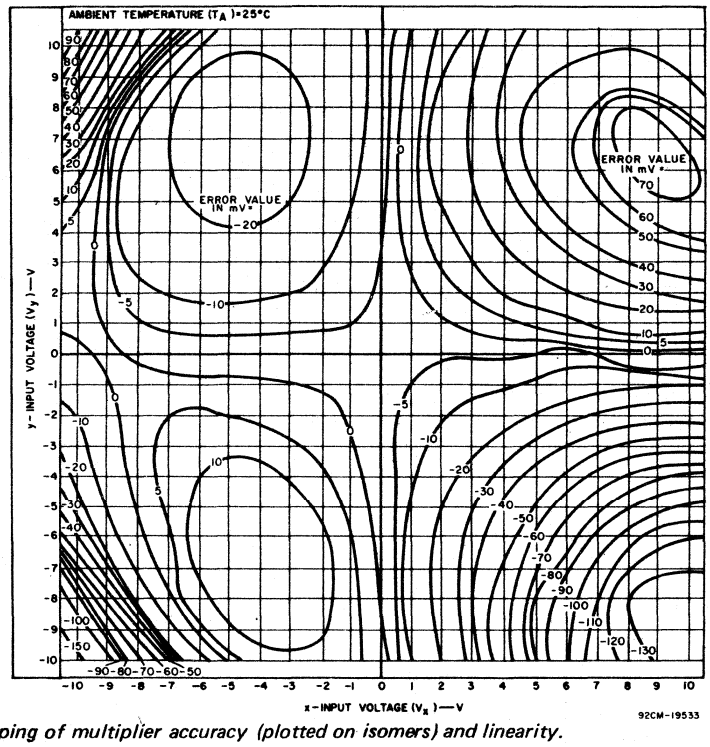


Fig.11—Test circuit for measurement of current gain and power-supply sensitivity.



Note: See "Contour Map" in "Symbols, Terms and Definitions" Section.

Fig.12—Contour mapping of multiplier accuracy (plotted on isomers) and linearity.

SYMBOLS, TERMS AND DEFINITIONS

Output Offset Current
The multiplier output current produced when both of the multiplier input signals are in the zero state.

Output Zero
Sets the output at the zero level when the x and y inputs are in the zero state. (It is implied that all other zeroing adjustments have been effected.)

R_I
Input Resistance — Converts the input voltage to an input current.

R_L
Output (Load) Resistance — Converts the output current to a voltage.

R_O
Output Resistance — See V_O and I_O for the equations associated with these properties.

Regulator Diode
A temperature compensated Zener diode, included in the multiplier circuit, to provide a stable I_{IB}.

Scale Factor or k factor (k)
Represents the basic gain of the multiplier as expressed in the equation $V_O = kV_XV_Y$

The equation indicates the ideal transfer function for the multiplier. The normalized k factor is expressed by $k_N = k/k_{ref}$ where k_{ref} is the ideal or reference k factor. The ideal factor, k_{ref} is the value at which the k factor is set when the k-factor adjust control is trimmed. Optimum operation of the CA3091D is achieved when the k-factor is 0.1.

V_{IM}
The maximum ac sine-wave voltage to be applied to the multiplier; a 20-volt p-p sine wave is the nominal maximum swing voltage recommended for use with 50-kilohm input resistors.

V_{MID}
An ac or dc voltage that approximately satisfies the equation

$$V_{MID} = V_{IM}/\sqrt{2.}$$

V_O
The output product voltage derived from the expression

$$(kV_XV_Y = V_O)$$

$V_{ref.}$
Temperature compensated zener connected to the −15 volt supply to provide a reference voltage as an aid in setting up a stable I_{IB}.

V_X, V_Y
The input voltages to be multiplied.

x-Balance Circuit
Sets the output to the zero level when the x-input is in the zero state.

y-Balance Circuit
Sets the output to the zero level when the y-input is in the zero state.

SYMBOLS, TERMS AND DEFINITIONS — continued

Accuracy
Accuracy defines the degree of error encountered in the operation of the multiplier. It is portrayed on a contour map by isomers (contour lines). Isomers with the highest values indicate "less-accurate" operation of the multiplier. (See illustrative Contour Map in Fig. 12.)

Contour Map
The contour map, shown in Fig. 12, is a graphical portrayal of the multiplier errors in the x, y input plane. Each contour line, termed "isomer", connects those points whose error values (in millivolts) are equal in magnitude. For example, a −20 mV contour line with points at $V_X = 5V$ and $V_Y = -3V$ indicates that the output voltage is 20 mV less than the theoretical output product (kV_XV_Y). This error voltage, presented in percent of full-scale input (±10 V), defines the "accuracy" of the device. Thus, a 20-mV error voltage represents an "accuracy" of 0.2% as derived from the equation:

$$\text{Accuracy} = 20\,\text{mV}/10 \times 100\% = 0.2\%.$$

A contour map provides a true indication of multiplier performance in each of the four quadrants. Each CA3091D is comprehensively tested and must provide the specified accuracy in the four quadrants.

Current Converter
This portion of the IC combines the multiplier's differential-amplifier output currents and converts them to a single-ended output current.

Current Sources
These circuits provide the biasing currents for the various circuits in the IC. The I_{IB} terminal provides the control current for the current-source circuit.

Feedthrough
Feedthrough occurs when an output signal is produced even though one of the input signals is zero. Consequently, feedthrough signal characteristics constitute a source of error in the operation of a multiplier. In the CA3091D, for example, the feedthrough signal output is specified to be less than 20 mV p-p when either terminal is set at 20 V p-p and the other terminal is set to zero.

I_{IB}
Circuit biasing control current.

I_{IC}
See I_{OC}.

I_O
Output product current ($k_I I_X I_Y = I_O$), where $k_I = kR_I^2 / R_L$

I_{OC}, I_{IC}
Compensatory input and output currents required to correct unlinearity along the x axis. (Optional for low-level signal use.)

I_X, I_Y
Input currents to be multiplied.

k
Voltage Scale Factor (determines the gain of the multiplier).

k_I
Current Scale Factor (k_I) = $(R_I^2 / R_L)k$.

k adjust
Scale-Factor Adjustment.

Linearity
"Linearity" indicates the degree of multiplier error (i.e. deviation from "straight-line" characteristics) along each of the four boundaries of the input x, y field. These boundaries are formed when one input is held at one of the two maximum values (10 volts or −10 volts) and the other input is swept through the voltage range. (See Contour Map for additional information.)

Linearity Adjust
An external circuit to provide vernier adjustment for optimum linearity. This control should be adjusted before adjusting the y-balance control.

Linearity Balance Circuit (Low-Level)
This circuit makes the multiplier's transfer function linear for low-level x-input signals.

Linearity Compensator
Internal circuitry that converts input current into a non-linear voltage, a requisite for producing a linear output in the differential amplifiers of the multiplier circuit.

Multiplier Circuitry
Provides the product of the two input voltages.

Multiplier Transfer Function
This function mathematically describes the interaction of the two inputs and the resulting output signal. The basic transfer function for a multiplier is

$$k(V_X + V_{Xe})(V_Y + V_{Ye}) = V_O + V_{Oe}$$

where: k = k factor and represents the basic gain of the multiplier

V_X, V_Y = the external inputs to be multiplied

V_O = the desired value of the product output signal

V_{Xe}, V_{Ye} = the "effective" errors that occur at the inputs of the multiplier and cause an output signal when either input is in a zero state.

V_{Oe} = the error voltage that develops at the output of the multiplier

DC correction factors are added to the multiplier inputs and output to compensate for the errors and offset variations. A complex linearity error term appears in the transfer function; however, this term is not included in the above equation for the purpose of clarity.

OPERATING CONSIDERATIONS

Operation of a Multiplier

A multiplier is, essentially, a gain-controlled amplifier (See Fig. 13) that multiplies the input signal (V_X) with the external gain controlling signal (V_Y) to produce the resultant output (V_O). The gain is externally adjustable by a coefficient (k). Stated simply, a multiplier produces an output voltage that is the linear product of two input voltages.

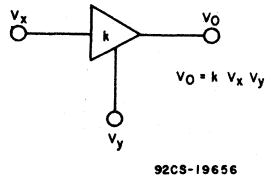
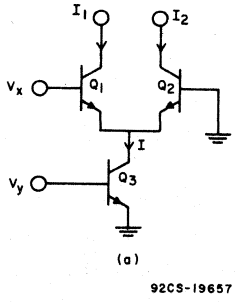
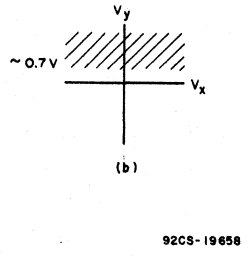


Fig.13—Gain-controlled amplifier.

The basic multiplier, shown in Fig. 14a, is a two-quadrant multiplier. The input signal (V_X) may have either a positive or negative polarity whereas, the external gain-controlling signal (V_Y) must be positive and greater than the base-to-emitter voltage (Fig. 14b). The output current ($I_1 - I_2$) of the differential amplifier, comprised of transistors Q1 and Q2, is related to both the input signal (V_X) and the current source (I). Since the current source (I) is related to the gain controlling signal (V_Y) the output current ($I_1 - I_2$), therefore, is related to both V_X and V_Y.





a) Basic circuit.

b) Multiplier functional only in shaded region.

Fig.14—Two-quadrant multiplier.

This relationship is essentially non-linear; thus an appropriate linearization circuit must be provided in the input stage to achieve the following linear relationship:

$$I_1 - I_2 = k' V_X V_Y \qquad \text{(Eq. 1)}$$

where k' is a constant

Figure 15 shows a typical arrangement of three differential amplifiers to form a four-quadrant multiplier. This arrangement incorporates the operating principles of the two-quadrant multiplier, but, in addition, it permits both of the input signals (V_X and V_Y) to have positive or negative polarities (or zero). When either input is zero, the output current ($I_1 - I_2$) must, theoretically, be zero as is shown by the following:

1. Assume $V_X = 0$,
   then $i_1 = i_2$ and $i_3 = i_4$
   therefore $i_1 + i_4 = i_2 + i_3$.
   Since $I_1 = i_1 + i_4$ and $I_2 = i_2 + i_3$,
   then $I_1 = I_2$.
   This equality is independent of V_Y
2. Now assume $V_Y = 0$,
   then $i_5 = i_6$.
   Sine $i_5 = i_1 + i_2$ and $i_6 = i_3 + i_4$,
   then $i_1 + i_2 = i_3 + i_4$.
   Since $i_1 = i_3$ and $i_2 = i_4$
   then $i_1 + i_4 = i_3 + i_2$.
   Therefore $I_1 = I_2$.
   This equality is independent of V_X.

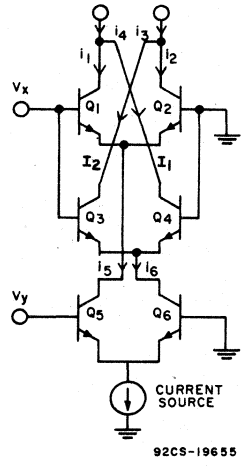


Fig.15—Basic four-quadrant multiplier.

The multiplying operation discussed in the previous section applies when neither V_X nor V_Y is zero. The output current ($I_1 - I_2$) then satisfies Equation 1,

$$I_1 - I_2 = k' V_X V_Y.$$

The multiplying action of the four-quadrant multiplier is dependent on current unbalance in the three differential amplifiers. Ideally, the multiplying operation should not occur if either V_X or V_Y is O. However, in practical applications slight current unbalances do exist. It is necessary, therefore, to null out such unbalances with external potentiometers prior to operation.

TYPICAL OPERATING CONSIDERATIONS

The RCA-CA3091D, shown in Fig. 2, is a four-quadrant multiplier that incorporates the basic multiplier principle, previously discussed in "Operation of a Multiplier". Because the design of this multiplier is based on the multiplication of two input currents to produce an output current it is necessary to convert the input voltages to input currents and the output current to an output voltage by inserting resistors at both input and output terminals. Fig. 1 shows the four-quadrant multiplier with its peripheral circuitry for nulling current unbalances.

The Bias Current (I_{IB}) at Term. 3 sets the operating current level for the entire multiplier circuit by means of a current-source circuit. Therefore, it is essential that this bias current level remain constant under all operating conditions. To maintain this steady state, a temperature compensated zener diode is provided on the chip and connected to the Reference Voltage (Term.6).

Linearity of the differential amplifier transconductance function is accomplished by linearity compensators as shown in Fig. 1. To correct low-level signal unbalances that may occur between Differential Amplifiers A and B, an external potentiometer is connected to Terminals 7 and 8 (See Fig. 1). The Current Converter circuit, which consists of a set of current mirrors, supplies the output current ($I_1 - I_2$). It is important that circuit unbalances be corrected prior to operation. Table I describes the alignment procedures for correcting these unbalances.

A multifunctional circuit board (Figs. 16 and 17) is available for performing the four basic applications, such as, multiplying, dividing, squaring and taking the square root.

When the CA3091D is used as a multiplier (Fig. 18) or as a squarer (Fig. 18) only the basic pheripheral circuitry on the multifunctional circuit board is utilized and the general-purpose operational amplifier (CA3741T) is disabled from operation. Follow the ac alignment procedures for these two applications before operating the circuit.

When the CA3091D is used as a divider (Fig. 20), the operational amplifier is required in order to provide the proper negative feedback. The limitations for operation as a divider are that $O < V_Y \leqslant 10V$ and $-10V \leqslant V_Z \leqslant 10V$. Note, the range of V_Y is limited to the positive polarity; if V_Y was permitted to go negative, the feedback loop would go positive and, thereby, create an unstable operating condition.

Alignment of the divider (Fig. 19) differs from multiplier and squarer alignment because of the additional variances introduced by the operational amplifier. A coupling capacitor is

Table I

AC Alignment Procedures For CA3091D, Four-Quadrant Multiplier

(Refer to Fig. 16, for circuit pertaining to following alignment procedures.)

Step No.	Voltage Setting		Control Adjust	Test Equipment Used	Measure	Notes
	V_X	V_Y				
1	–	–	–	–	–	Set all potentiometers to center of range.
2	O	V_{IM}	x Balance	AC VM	V_O	Adjust for a minimum reading.
3	O	V_{IM}	Linearity	AC VM	V_O	Adjust for a minimum reading.
4	–	–	–	–	–	Repeat Steps 1 and 2 until no further improvement is noted.
5	V_{IM}	O	y Balance	AC VM	V_O	Adjust for a minimum reading.
6	O	O	Zero Output	DC VM	V_O	Adjust for zero output.
7	V_{MID}	V_{MID}	R_k	AC/DC VM	V_O	Adjust for $V^2_{MID}/10$ at the output.
8	–	–	–	–	–	Check multiplier for alignment in all four quadrants.

V_{IM} – Is the maximum AC swing of the sine wave that will be applied to the multiplier. A 20-volt p-p value is the nominal maximum swing of the AC sine wave with input resistors of 50 kilohms.

V_{MID} – An AC or DC voltage that approximately satisfies the equation $V_{MID} = V_{IM}/\sqrt{2}$. For example, if a 50-kilohm resistor is used with a 7-volt input, then R_k should be adjusted for a 4.9-volt output.

provided at the output of the divider alignment circuit in order to separate the ac signal from the dc signal and, thus, avoid interaction between the calibrating potentiometers.

The alignment procedure for the square-rooter function (Fig. 21) is identical to the alignment procedure for the divider function. The input voltage range is limited to $0 < V_I \leqslant 10V$. This limitation is necessary in order to prevent the output voltage (V_O) from latching to the negative output saturation voltage of the operational amplifier. Table II describes the divider alignment procedure.

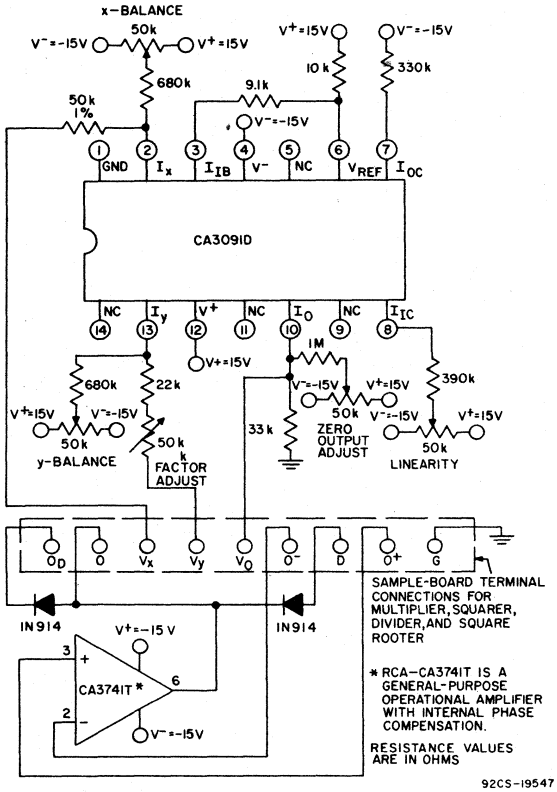
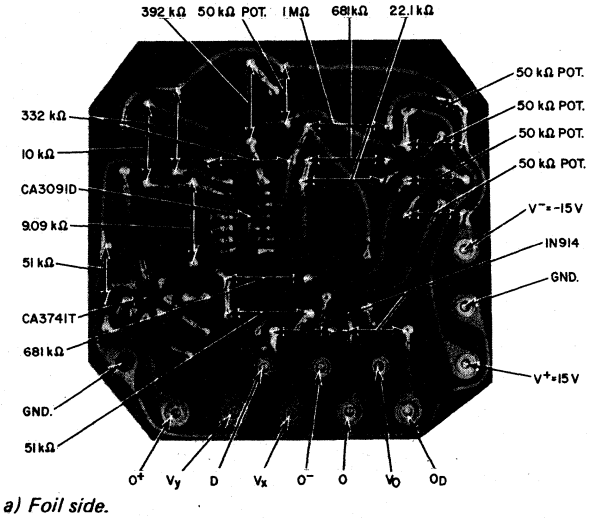
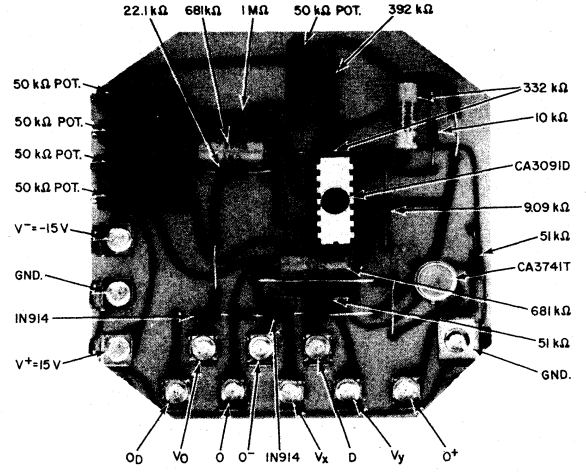


Fig.16—Typical multifunction circuit arrangement utilizing the CA3091D and CA3741T.



a) Foil side.

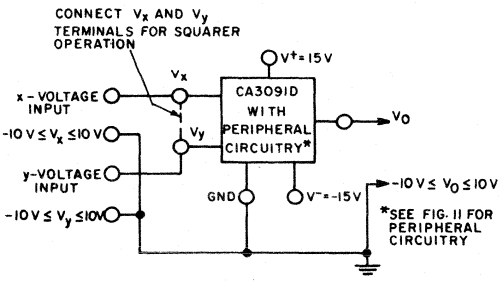


b) Component side.

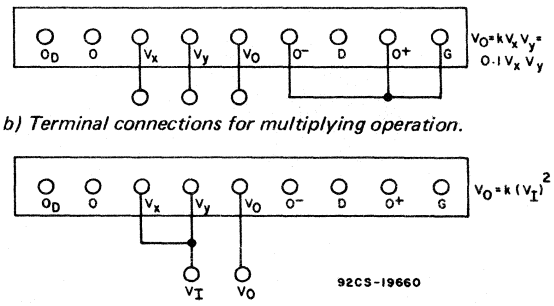
Fig.17—Photographs of a printed-circuit board for multifunction applications (multiplier, squarer, divider, square rooter) utilizing the CA3091D and CA3741T.

Table II — Divider Alignment Procedure

Step No.	Set V_z V	Set V_y V	Measure	Output Coupling	Test Equipment Used	Adjust	Notes
1	—	—	—	—	—	—	Set all potentiometers to center of range.
2	0	V_S	V_O	ac	ac — VM	O_{zero}	Adjust for minimum reading.
3	0	10V dc	V_O	dc	dc — VM	$x_{balance}$	Adjust for OV dc output.
4	V_S	V_S	V_O	ac	ac — VM	$y_{balance}$	Adjust for minimum reading.
5	5V dc	5V dc	V_O	dc	dc — VM	k_{adjust}	Adjust for 10V dc output.



a) Circuit arrangement for multiplier or squarer operation.



b) Terminal connections for multiplying operation.

c) Terminal connections for squarer operation.

Fig.18—Multifunction circuit-board arrangement with terminal connections for multiplier and squarer operation.

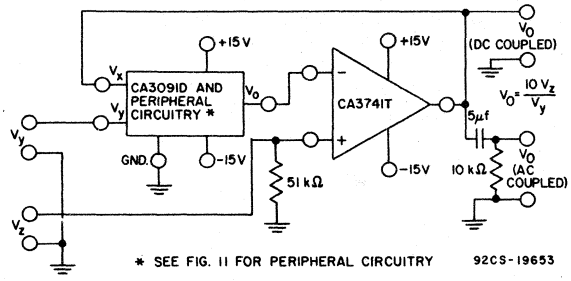


Fig.19—(a) Divider alignment circuit.

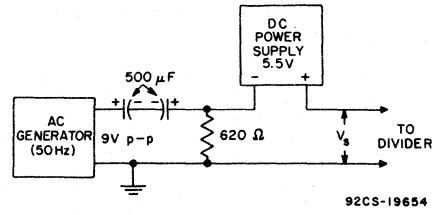
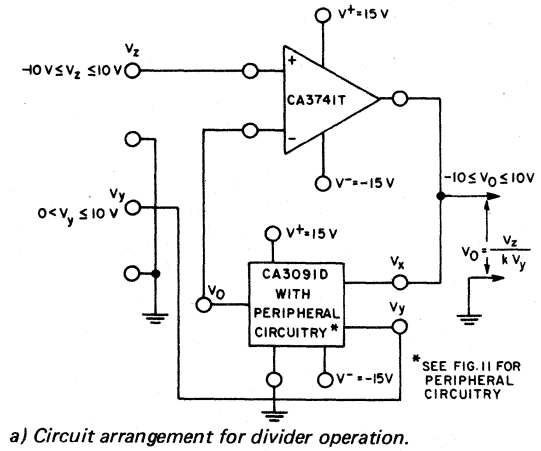
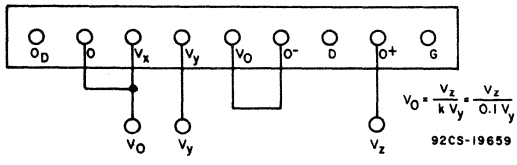


Fig.19—(b) Circuit to provide offset ac signal for use in divider alignment procedure.

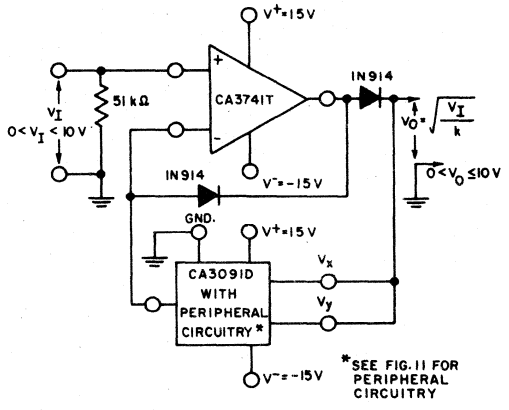


a) Circuit arrangement for divider operation.

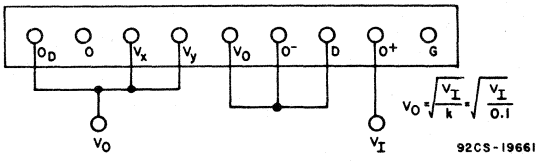


b) Terminal connections for divider operation.

Fig.20—Multifunction circuit-board arrangement with terminal connections for divider operation.



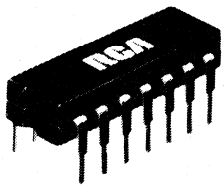
a) Circuit arrangement for square-rooter operation.



b) Terminal connections for square-rooter operation.

Fig.21—Multifunction circuit-board arrangement with terminal connections for square-rooter operation.

CA3179E



14-Lead Dual-In-Line
Plastic Package
"E"-Suffix Type H-1517

1.25 GHz Prescaler

For Industrial Applications

FEATURES:
- *Broadband operation - DC to 1.25 GHz*
- *High sensitivity*
- *Standard T^2L or ECL power supply*
- *Dual mode operation - VHF/UHF (÷ 64/ ÷ 256)*
- *Complementary ECL outputs*
- *Independent VHF and UHF input terminals*

The RCA-CA3179E is an integrated-circuit prescaler intended for use in communications and instrumentation systems. It performs division by 256 in the uhf mode and division by 64 in the vhf mode.

The mode of operation is selected by means of the bandswitch and the separate uhf and vhf input terminals provided. Either single- or double-ended inputs can be applied. These inputs are normally ac coupled, but dc coupling can be used if the specified bias levels are maintained. The output is a complementary emitter-coupled stage capable of driving a 33-pF or equivalent load. The harmonic output is reduced above 40 MHz by limiting output-signal rise and fall times and by maintaining a balanced load.

In the uhf mode, which is activated by applying a high level (logical 1) to the bandswitch input terminal, all eight divider stages are operative, resulting in division by 256. In the vhf mode, activated by a low level (logical 0) at the vhf input terminal, two divider stages are bypassed, resulting in division by 64. An internal amplifier/multiplexer provides this control while isolating both inputs, amplifying the input signal, and improving sensitivity.

The CA3179E is supplied in the 14-lead dual-in-line plastic package.

Applications:
- *Digital frequency synthesizers for:*
  - *VHF/UHF receivers*
  - *Satellite communications*
  - *Instrumentation*
- *High-frequency divider for:*
  - *UHF frequency counters*
  - *UHF timers*
  - *High-speed computers*
  - *Frequency standards*
  - *SHF second IF local-oscillator injection*
  - *PCM communications*
  - *Satellite communications*
  - *Radar ranging systems*
- *High-frequency up-converters*

Table of Absolute-Maximum Ratings

Term. No.	Min. Volts	Max. Volts	Max. I_{IN} (mA)	Max. I_{OUT} (mA)
1 & 2*	0	5.5	110	0
3	−0.3	20	1	1
4 & 5	—	—	0.1	10
9, 10, 13, 14▲	—	4	0.1	1

*Terms. 1 & 2 tied together.
▲Maximum rf drive = 500 mVRMS.
Terms. 7 & 8 are system ground and tied together.
Terms. 6, 11, 12 = no connection.

CA3179E

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE ..... 5.5 V
DC BANDSWITCH VOLTAGE ..... 20 V
RMS INPUT VOLTAGE ..... 0.5 V
DEVICE DISSIPATION:
  UP TO T_A = 70 °C ..... 700 mW
  ABOVE T_A = 70 °C ..... derate linearly at 11.1 mW/ °C
AMBIENT TEMPERATURE RANGE:
  OPERATING ..... 0 to 85 °C
  STORAGE ..... −55 to +150 °C
LEAD TEMPERATURE (DURING SOLDERING):
  AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)
  FROM CASE FOR 10 SECONDS MAX. ..... +265 °C

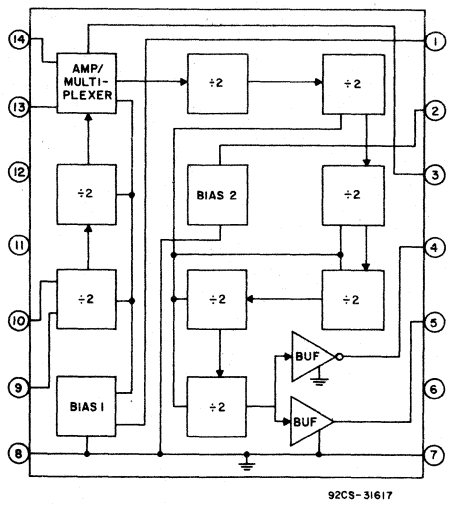


Fig. 1 - CA3179G block diagram.

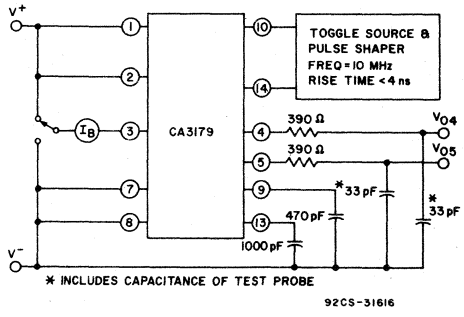


Fig. 2 - DC characteristics test circuit.

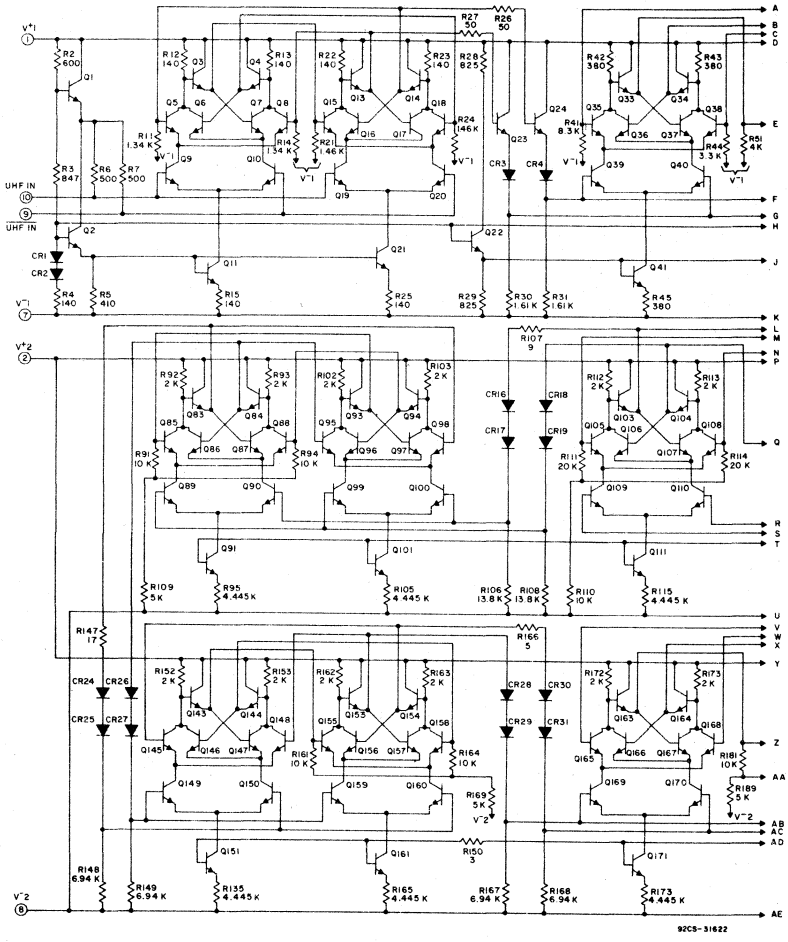


Fig. 3 - Schematic diagram (cont'd on next page).

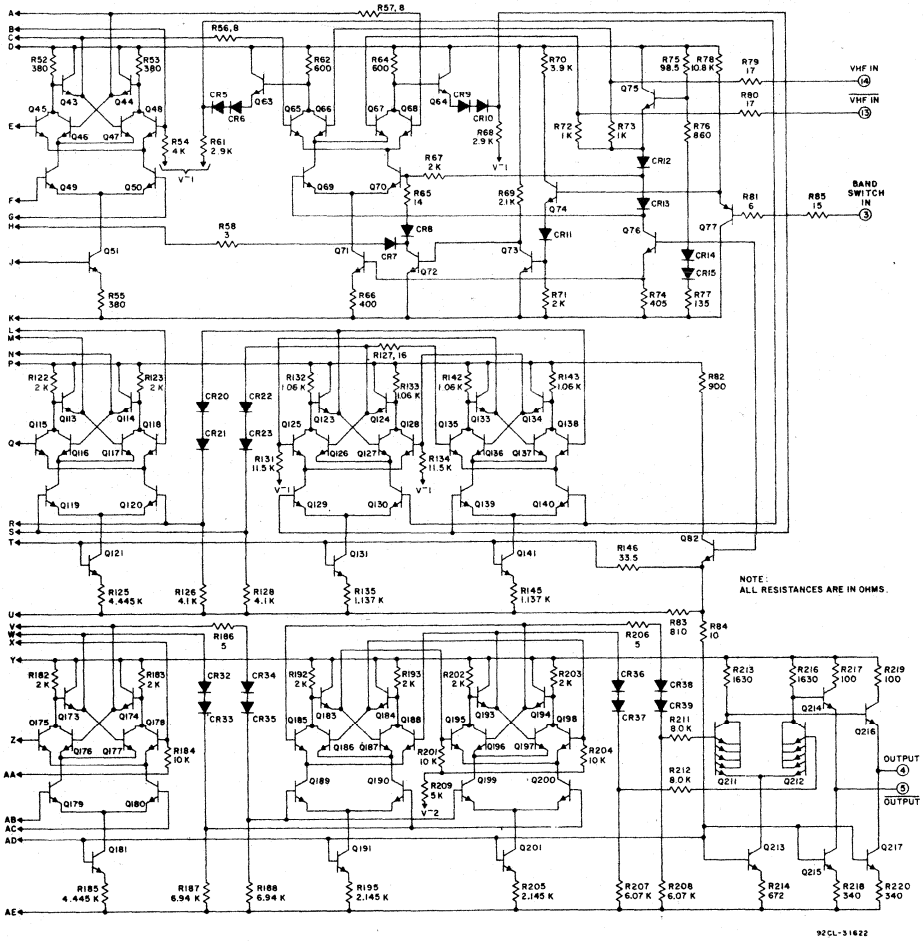


Fig. 3 - Schematic diagram (cont'd from previous page).

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V+ = 5 V, V− = 0 V

CHARACTERISTIC	TEST CONDITIONS	LIMITS Min.	Typ.	Max.	UNITS
Static (See Fig. 2)					
Supply Current, I+	Terms. 1 & 2	30	65	100	mA
Bandswitch Voltage: Low, V_{BL}	Term. 3	2.4	—	—	V
Bandswitch Voltage: High, V_{BH}	Term. 3	—	—	0.8	V
Bandswitch Current: Low, I_{BL}	V3 = 0 V	−1	—	—	mA
Bandswitch Current: High, I_{BH}	V3 = 20 V	—	—	0.5	mA
Dynamic (See Fig. 4)					
Sine Wave Sensitivity (Single-ended)	f_{IN} = 450 to 950 MHz, V3 = 5 V	0	30	80	mVRMS
Sine Wave Sensitivity (Single-ended)	f_{IN} = 80 to 450 MHz, V3 = 5 V	—	50	160	mVRMS
Sine Wave Sensitivity (Single-ended)	f_{IN} = 90 to 275 MHz, V3 = 0 V	—	5	40	mVRMS
Output Voltage: High, V_{OH}	Term. 4 or 5	—	4.2	—	V
Output Voltage: Low, V_{OL}	Term. 4 or 5	—	3	—	V
Output Voltage: Peak-to-Peak, V_{OP-P}	Term. 4 or 5	0.65	1.1	1.6	V
Output Rise or Fall Time, t_r,t_f		40	70	110	ns
Internal Bias	Term. 13 or 14	(V_{DD} − 1)			V
Internal Bias	Term. 9 or 10	(V_{DD} − 2.7)			V
DC Input Resistance, R_I	Term. 13 to 14	2000			Ω
DC Input Resistance, R_I	Term. 9 to 10	1000			Ω
Complex Input Impedance	Term.9 to 10, V_{IN} = 100 mV, f_{IN} = 950 MHz	20			Ω
Complex Input Impedance	Term.9 to 10, V_{IN} = 100 mV, f_{IN} = 450 MHz	30 - j80			Ω
Complex Input Impedance	Term.13 to 14, V_{IN} = 100mV, f_{IN} = 275 MHz	35 - j100			Ω

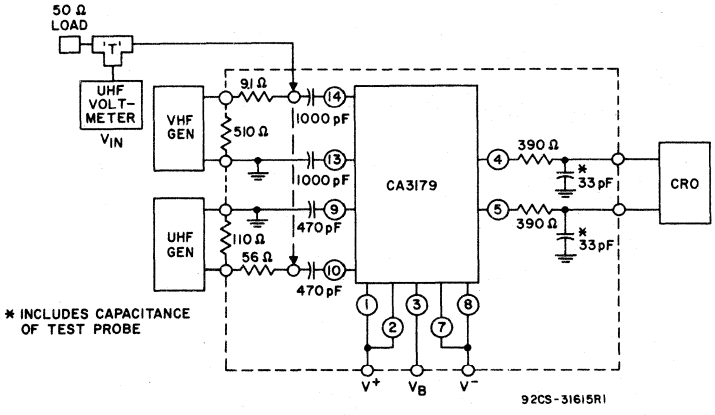


Fig. 4 - AC characteristics test circuit.

CA3179E

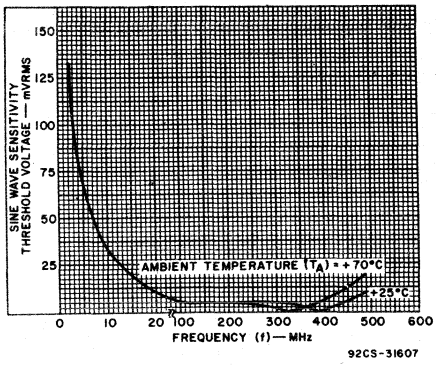


Fig. 5 - Typical threshold sensitivity in the ÷64 VHF mode.

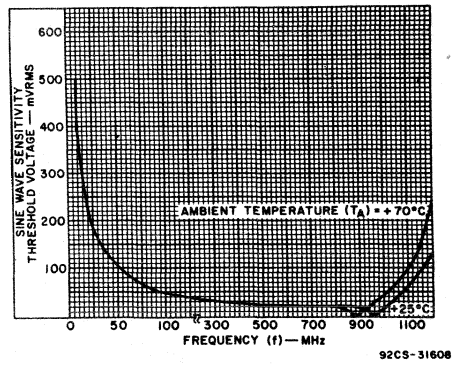


Fig. 6 - Typical threshold sensitivity in the ÷256 UHF mode.

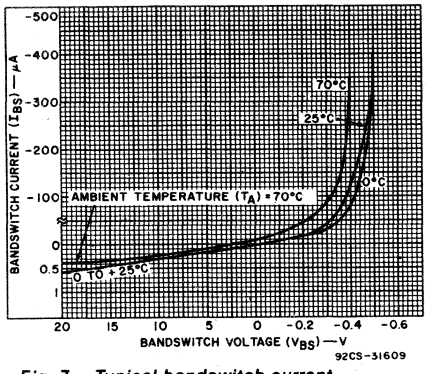


Fig. 7 - Typical bandswitch current as a function of bandswitch voltage and ambient temperature.

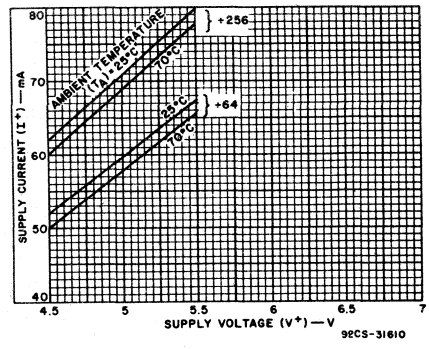


Fig. 8 - Supply current as a function of supply voltage and ambient temperature.

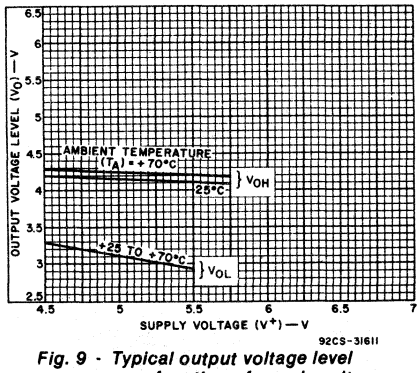


Fig. 9 - Typical output voltage level as a function of supply voltage and ambient temperature.

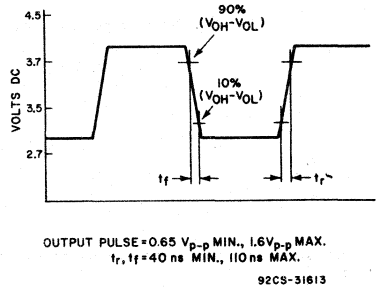


Fig. 10 - Output pulse characteristics.

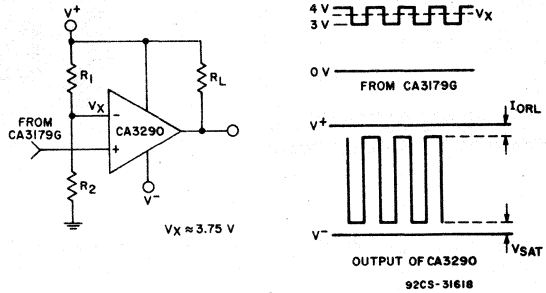


Fig. 11 - Typical bipolar interface circuit.

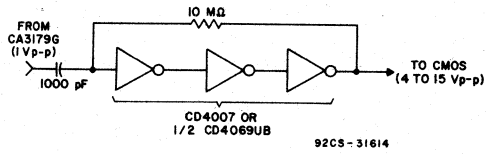
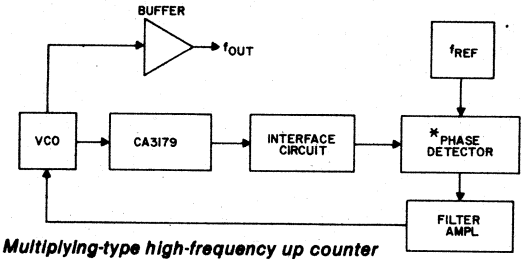
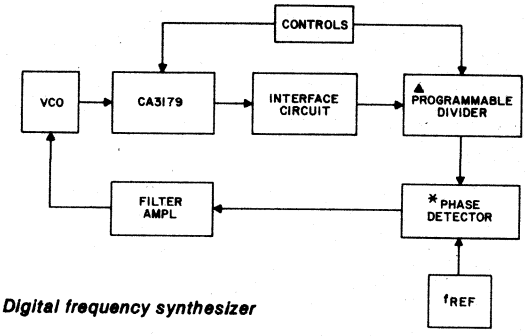


Fig. 12 - Typical CMOS interface circuit.



a) Multiplying-type high-frequency up counter



b) Digital frequency synthesizer

Fig. 13 - Typical system configuration.

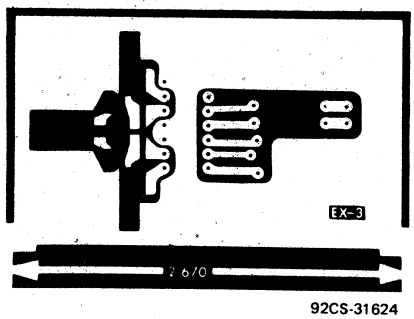


Fig. 14 - Printed-circuit board for the dynamic test circuit.

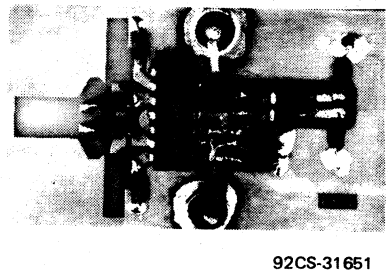
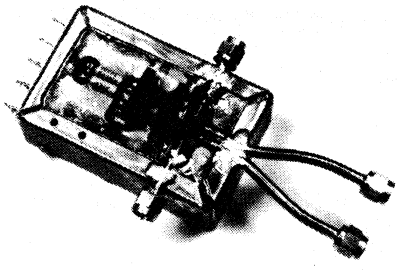


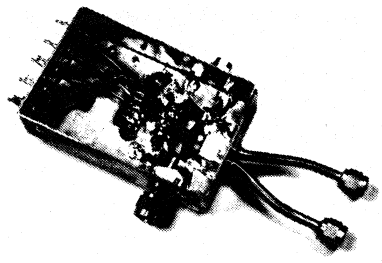
Fig. 15 - Printed-circuit board for the dynamic test circuit with components.

CA3179E



TOP VIEW

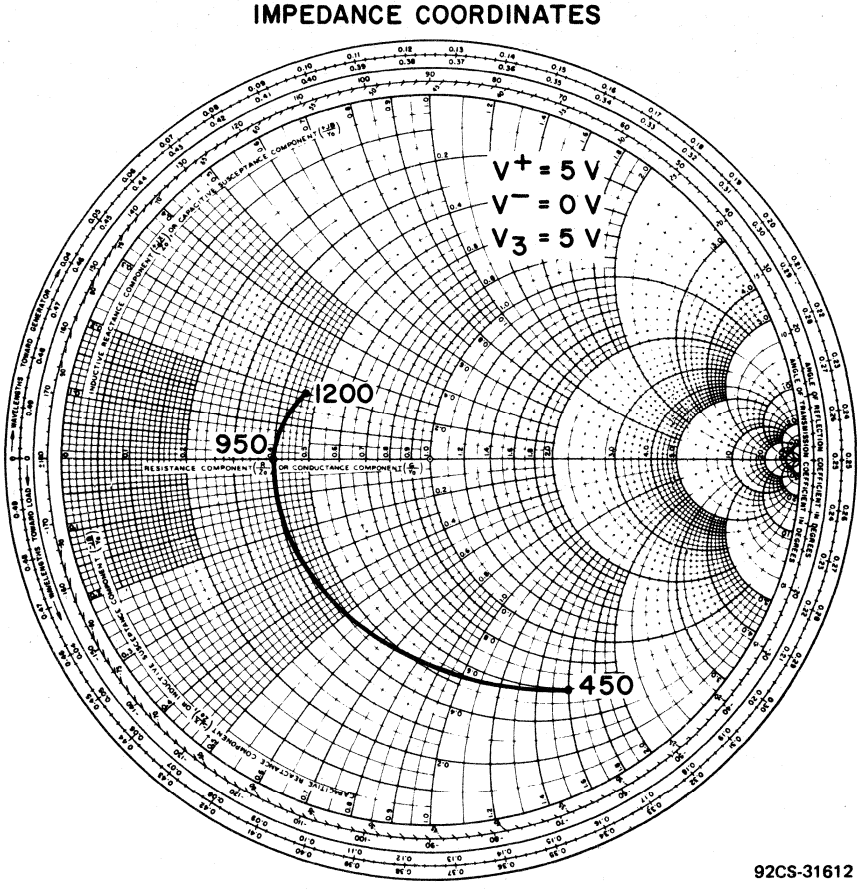
92CS-31652



BOTTOM VIEW

92CS-31653

Fig. 16 - Dynamic test circuit fixture.



92CS-31612

Fig. 17 - Impedance as a function of frequency.

High-frequency construction and design techniques must be followed if the operation of the CA3179G test circuit is to be stable and if the results of repeated tests are to be consistent. The dynamic test circuit is shown in Fig. 4, and a photo of the test fixture that houses it is shown in Fig. 16. Listed below are some precautionary construction considerations for the circuit and test fixture.

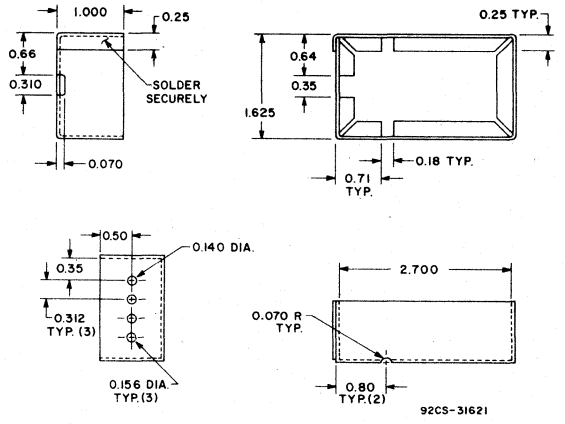
1. Supply the ground plane with frequent ground connections.
2. Use 50-Ω coaxial cable for input connections
3. Use a "dead bug" type socket to minimize lead lengths and reduce series inductances
4. Use input pads that reduce impedance mismatch at the generator-test and meter-test input interfaces
5. Use leadless ceramic disc capacitors wherever possible
5. Provide capacitor by-passing near active terminals where ac grounds are required

Specific applications may require changes in the procedures listed above. The socket, for instance, can be eliminated by soldering the device directly to the p.c. board or by using individual board-mounted socket pins. Input and output interface connections and circuitry will also vary according to specific circuit requirements.

Partial Parts List for the Dynamic Test Circuit and Fixture:

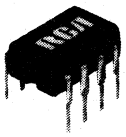
4 Pasternac PE3493-6 SMA cable connectors and semi-rigid coaxial cable
1 Chassis
1 P.C. board
1 14-lead socket
2 1000-pF capacitors, Stettner Trush Inc. No. TEFIC-7
3 470-pF disc capacitors
3 1000-pF disc capacitors
2 33-pF feedthrough capacitors
3 1000-pF feedthrough capacitors
3 Ferrite beads, 0.375 x 0.187 x 0.250
2 Resistors, 390-Ω, ¼-W, 2%
1 Resistor, 56-Ω, 1/8-W, 5%
1 Resistor, 110-Ω, 1/8-W, 5%
1 Resistor, 9.1-Ω, 1/8-W, 5%
1 Resistor, 510-Ω, 1/8-W, 5%

Dimensions of Test Fixture



CA3199E

VHF/UHF ÷ 4 Prescaler



8-Lead Dual-In-Line Plastic (Mini-DIP)

H-1817

Features:

- *Broadband operation - DC to 1.3 GHz*
- *High sensitivity*
- *Standard T^2L or ECL power supply of 5 V ± 0.5 V*
- *Complementary ECL outputs*

Applications:

- *Digital frequency synthesizers for:*
  VHF/UHF receivers
  Satellite communications
  Instrumentation
- *High-frequency divider for:*
  UHF frequency counters
  UHF timers
  High-speed computers
  Frequency standards
  SHF second IF local-oscillator injection
  PCM communications
  Satellite communications
  Radar ranging systems
- *High-frequency up-converters*

The CA3199E* is a bipolar integrated fixed-ratio (divide-by-four) counter which operates over the VHF/UHF frequency band (DC to 1.3 GHz). It accepts either single or double-ended ac-coupled input signals and provides complementary emitter follower outputs at standard ECL logic levels.

The CA3199E is supplied in an 8-lead dual-in-line plastic (Mini-DIP) package, and operates over an ambient temperature range of 0 to +85°C.

*Formerly RCA Dev. Type No. TA10853.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE ..... 5.5 V

RMS INPUT VOLTAGE ..... 0.5 V

DEVICE DISSIPATION:

UP TO T_A = 70°C ..... 630 mW

ABOVE T_A = 70°C ..... derate linearly at 7.7 mW/°C

AMBIENT TEMPERATURE RANGE:

OPERATING ..... 0 to 85°C

STORAGE ..... −55 to −150°C

LEAD TEMPERATURE (DURING SOLDERING):

AT DISTANCE 1/16 ± 1/32 IN. (1.59 ± 0.79 mm) FROM CASE FOR 10 SECONDS MAX. ..... −265°C

CA3199E

STATIC CHARACTERISTICS (T_A=25° C, V_{CC}=+5.0 V, V_5=Ground)

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
"1" Output Voltage, V_{OH}	Outputs Unloaded	—	4.2	—	V
"0" Output Voltage, V_{OL}	Outputs Unloaded	—	3.4	—	V
Internal Bias Voltage, V_{BIAS}	Pin #4 Left Floating	—	2.4	—	V
Power Supply Current Drain, I_D		35	60	85	mA

DYNAMIC CHARACTERISTICS (T_A=25° C, V_{CC}=+5.0 V, V_5=Ground)

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Input Frequency Range (sinusoidal), V_{IN}	Single-Ended Input, 1000 MHz	—	—	400	mVpp
Output Voltage Swing, V_6, V_7		0.6	0.8	—	Vpp
"1" Transition Time, t_{-+}	Output Unloaded	—	0.6	—	ns
"0" Transition Time, t_{+-}	Output Unloaded	—	0.6	—	ns
Input Capacitance, C_{IN}		—	2.5	—	pF
Input Resistance, R_{IN}		—	400	—	Ω

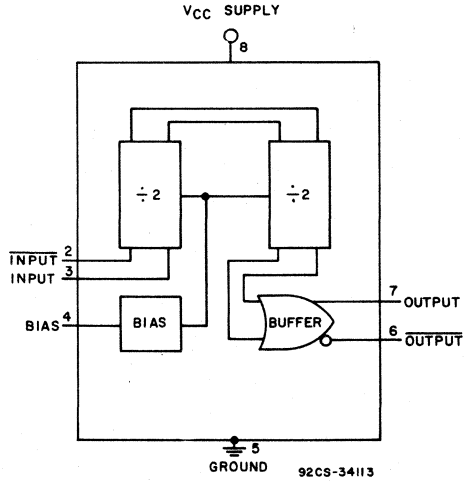


Fig. 1 - Logic diagram for divide-by-four counter.

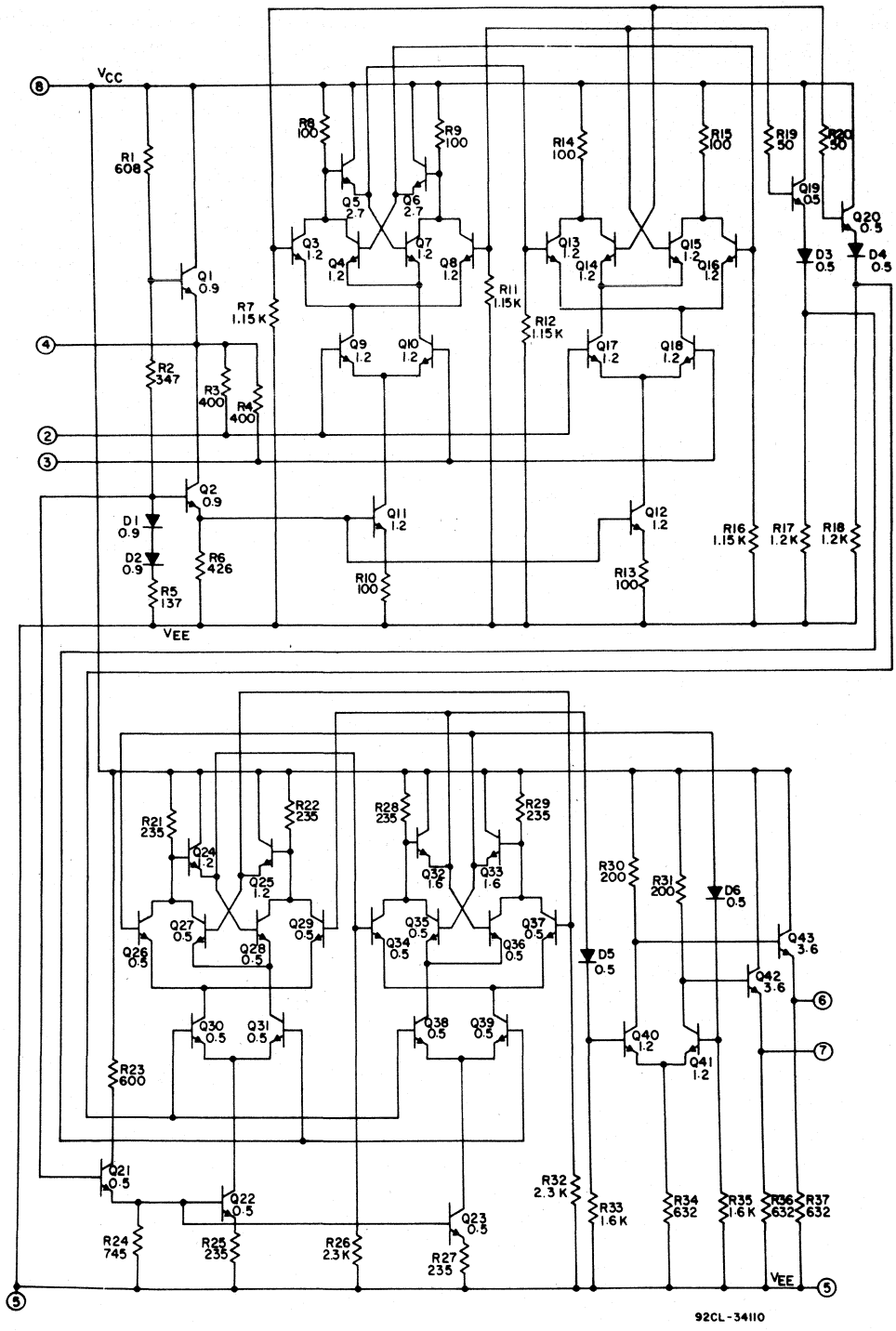


Fig. 6 - Schematic diagram for CA3199E.

CA3199E

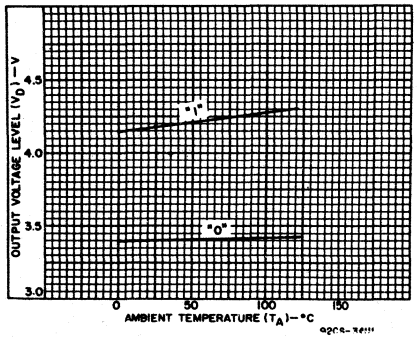


Fig. 2 - Typical output levels as a function of ambient temperature.

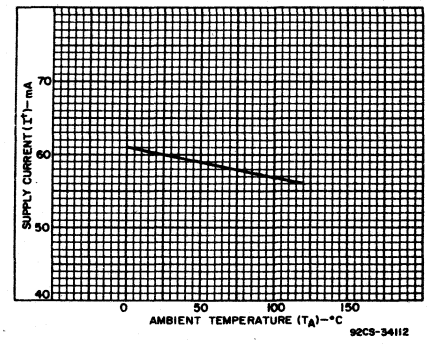


Fig. 3 - Typical power-supply current as a function of ambient temperature.

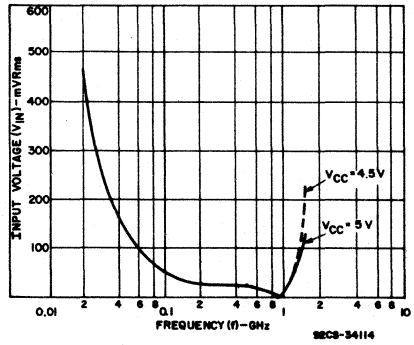


Fig. 4 - Sinusoidal input sensitivity.

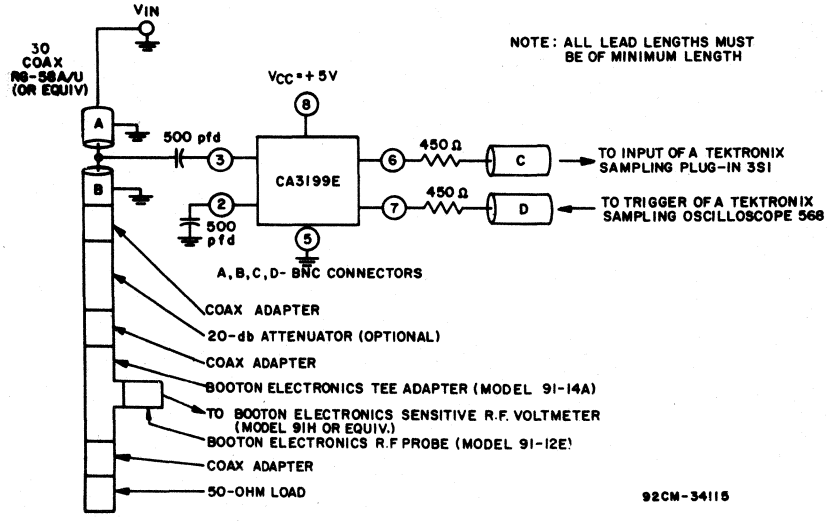
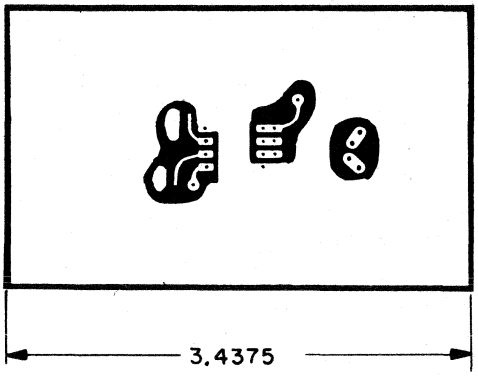


Fig. 5 - Test circuit for CA3199E.



92CS-34146

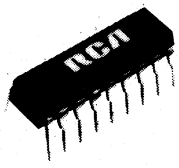
Fig. 7 - Printed-circuit board for the test circuit.

Application and Test Notes

1. Both complementary inputs and outputs are provided. When driven single-ended, normally at pin 3, the unused input (pin 2) should be ac by-passed (500 pF) to ground for best performance.
2. Internal bias monitor, pin 4, is normally left floating or ac by-passed to ground.
3. Device inputs should be ac coupled to the signal source. 500-pF coupling capacitors are adequate above 50 MHz.
4. Input signal voltage (sinusoidal) required is 100 mV RMS (typical) over the frequency range of 100-1000 MHz
5. When the input signal voltage is a square wave, a rise time of ≤5 ns is required. The signal should be 400-800 mV peak-to-peak over the frequency range from dc-1000 MHz. This corresponds to an input slew rate minimum of 62.5 V/μs.
6. All test data are for the 8-pin dual-in-line packaged circuit as mounted in a standard IC socket. Somewhat improved higher frequency performance can be obtained by attaching directly to a suitable PC board.
7. High-frequency construction and design techniques must be followed if the operation of the test circuit is to be stable and if the results of repeated tests are to be consistent. Listed below are some precautionary construction considerations for the circuit and test fixture.
    1. Supply the ground plane with frequent ground connections.
    2. Use 50-Ω coaxial cable for input connections.
    3. Use a "dead bug" type socket to minimize lead lengths and reduce series inductances.
    4. Use input pads that reduce impedance mismatch at the generator-test and meter-test input interfaces.
    5. Use leadless ceramic disc capacitors wherever possible.
    6. Provide capacitor by-passing near active terminals where ac grounds are required.

Specific applications may require changes in the procedures listed above. The socket, for instance, can be eliminated by soldering the device directly to the PC board or by using individual board-mounted socket pins. Input and output interface connections and circuitry will also vary according to specific circuit requirements.

CA3211E



H-1899

18-Lead Dual-In-Line Plastic Package E Suffix

VHF/UHF Prescaler

Features

- *Divide by 256*
- *Input frequency to 1 GHz*
- *Dual input ports electrically selectable*
- *Input sensitivity*
  < 10 μW typical
  (Generator available power into a 50-Ω load)
- *5-V power supply*
- *Balanced output ports*

The RCA-CA3211E* is an integrated-circuit prescaler intended for use in TV frequency synthesis tuning systems over an input frequency range of 90 to 1000 MHz. It performs division by 256 in the UHF and VHF mode.

The mode of operation can be selected by means of the bandswitch and the separate UHF and VHF input terminals provided. The output is a complementary emitter-coupled stage with controlled slew rate for harmonic suppression.

The CA3211E is supplied in a 18-lead dual-in-line plastic package.

*Formerly RCA Developmental No. TA11355.

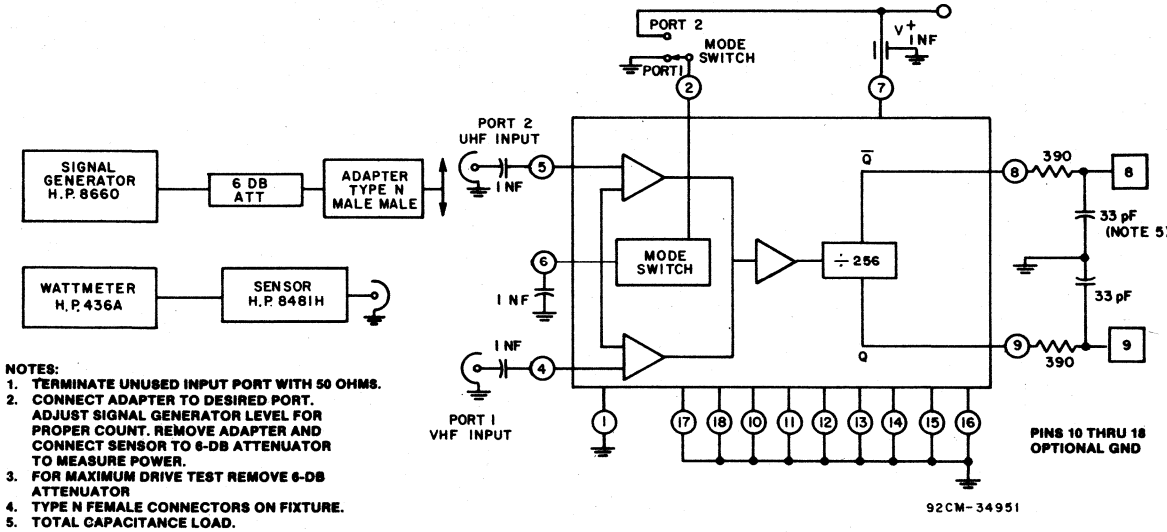


Fig. 1 - Block diagram and test circuit of the CA3211E.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE ..... 6 V
DC BANDSWITCH VOLTAGE ..... 20 V
RMS INPUT VOLTAGE ..... 0.5 V
DEVICE DISSIPATION:
To 70°C ..... 890 mW
Above 70°C ..... Derate linearly at 11.1 mW/°C
AMBIENT TEMPERATURE:
Operating ..... −40 to +85°C
Storage ..... −65 to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 in. (1.59 mm ± 0.79 mm) from case for 10 s max. ..... 265°C

ELECTRICAL CHARACTERISTICS, T_A=25° C, V+=5.0 V

CHARACTERISTIC	LIMITS			UNITS
	Min.	Typ.	Max.	
Supply Current, Terminal 7	30	65	110	mA
Band Change Voltage:				
Port 1 Select (VHF)	−0.5	0	0.6	V
Port 2 Select (UHF)	3	5	18	
Band Change Current, Terminal 2:				
At 0 Volts	—	—	−1	mA
At 18 Volts	—	—	2	
Divide Ratio, $f_{IN} \div f_{OUT}$:				
Port 1, f_{IN} 80-500 MHz	—	256	—	Ratio
Port 2, f_{IN} 80-1000 MHz	—	256	—	
Input Sensitivity, f_{IN}:				
40 MHz	—	15	—	mV rms
80 MHz	—	10	35	
150-800 MHz	—	10	20	
900 MHz	—	10	35	
1000 MHz	—	15	45	
Maximum Drive Level:				
80-1000 MHz	500	—	—	mV rms
Output at Terminal 9 or 8:				
Mean Value	—	3.5	—	V dc
Peak-Peak Swing	0.75	1	—	V_{p-p}
Rise or Fall Time	—	70	—	ns
Internal Bias at Terminal 6	—	2	—	V dc
Internal Bias, Terminal 2=5 V:				
At Terminal 4	—	0.07	—	V dc
At Terminal 5	—	2	—	

CA3211E

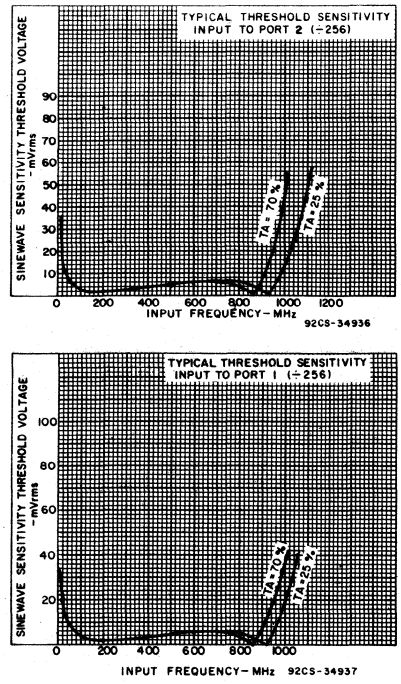
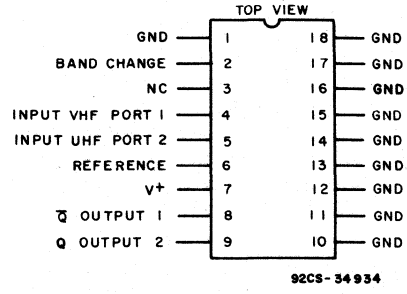
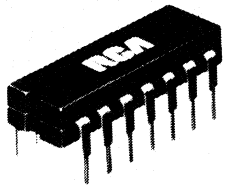


Fig. 2 - Sinewave sensitivity threshold voltage as a function of input frequency.



TERMINAL DIAGRAM



14-Lead Dual-In-Line Plastic Package H-1517

BiMOS Single-Chip Detector/Alarm System

With Integral Drivers for Mechanical and Piezoelectric Horn Alarms

Features:

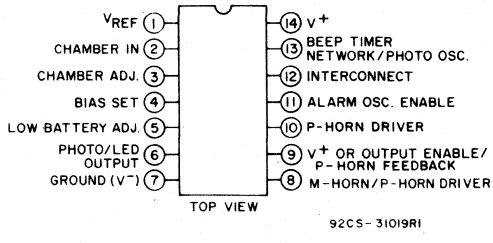
- *Interfaces directly with high Z sensors — no external buffer FET required*
- *Low input current: 1 pA max.*
- *Gate-protected input terminals*
- *On-chip beep oscillator for low battery indication*
- *Self-contained low-battery-voltage detection circuit*
  - *(a) Fixed or adjustable trip point available*
  - *(b) Dynamic battery test when filter capacitor = 2 μF*

The RCA-CA3164E is a monolithic BiMOS integrated circuit designed to meet the stringent system requirements of a battery- or line-operated alarm circuit. When used with an ionization chamber and electromechanical or piezoelectric horn, it provides a one-chip approach to smoke detection. No external active devices are required to interface with either the chamber input or horn output terminals. The CA3164E can also be used with photoelectric chambers by the addition of several external components.

The CA3164E is supplied in the 14-lead dual-in-line plastic package.

- *Chamber trigger voltage independent of battery supply voltage (less than 150 mV over temperature and supply variations)*
- *Reference source current available = 5 μA (typ.)*
- *Low standby battery current = 8 μA (typ.)*
- *Can be used with photoelectric sensors by using a minimum of external passive components in combination with the RCA-CA3078 micropower op-amp*
- *Multiple-unit interconnect terminal controls a common annunciator circuit*
  - *(a) A fault to ground doesn't prevent local operation*
  - *(b) The low battery alarm signal triggers only the local unit*
- *LED output indicates status of smoke-detector circuit*
- *Operates from 11 V (max.) supply (either battery or line)*
- *Battery reversal protection feature*

TERMINAL ASSIGNMENT



92CS-31019RI

CA3164E

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE, V+ ..... +11 V
DEVICE DISSIPATION, P_D:
Up to $T_A = 25°C$ ..... 600 mW
Above $T_A = 25°C$ derate linearly at ..... 6.7 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating ..... 0 to +50°C
Storage ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, V+ = 9 V

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Operating Voltage		7	9	11	V
Common-Mode Input Voltage Range, V_{ICR}	(V+ − 2 V) = 7 V	0	—	7	V
Low-Battery Trigger Voltage	External adjust (increase only)	7.3	7.7	7.9	V
Horn Driver V_{CE}(sat)	Term. 8 = 100 mA	—	—	0.5	V
	Term. 8 = 300 mA	—	—	1.1	
Reference Voltage	Term. 1	6.1	6.5	6.9	V
Input Leakage Current, I_L	Term. 2	—	—	1	pA
	Term. 2 at 50°C	—	—	2.5	
	Term. 3	—	—	50	
Standby Current (10 MΩ from Term. 4 to gnd)	No LED connected	—	8*	14	μA
	LED connected - 20 mA for 30 ms every 60 s	—	18	—	
	Photoelectric operation - LED photocurrent = 0.6 A (5-second rate)	—	13	—	
Reference Source Current		5	—	—	μA
LED Driver Sink Current	Term. 6	20	50	—	mA
Output Sink Current — Term. 8	Term. 8 = 1.1 V	200	300	—	mA
Output Sink Current — Term. 8	Term. 8 = 0.5 V	100	150	—	
Output Sink Current — Term. 10	Term. 10 = 2 V	20	25	—	
Output Source Current — Term. 8	Term. 8 = V+ − 2 V	20	25	—	mA
Output Source Current — Term. 10	Term. 10 = V+ − 2 V	20	25	—	
Interconnect Current Source	$V_O = 0$ V	1.5	3.5	6	mA
Interconnect Current Sink	$V_O = 9$ V	—	45	65	μA
Remote Fan-Out		20	—	—	
Low-Battery Adjust, Term.5 Input Current		50	70	225	nA
Timing Current	Term. 13	10	—	62	nA
LED Blink Period	Adjustable	—	—	1	PPM
LED Pulse Width	Fixed	—	30	—	ms
Alarm Pulse Duty Cycle (4.7 MΩ from Term. 11 to gnd)	On-time	—	95	—	%
	On-time = 95%	—	0.5	—	sec.
	Off-time = 5%	—	0.026	—	

*Adjustable to 5 μA.

OPERATING MODE TRUTH TABLE

CONDITION	BATTERY	LED TERM. 6	ALARM HORN TERMS. 8, 9, 10	SYSTEM REMOTE OUTPUT TERM. 12	REMOTE UNIT ALARM STATUS
No Smoke In Chamber	NORMAL	BLINK[1]	OFF	LOW	OFF
No Smoke In Chamber	LOW	BLINK[1]	BEEP[1]	LOW	OFF
Smoke In Chamber	X	ON	ON[2]	HIGH	ON
Remote Alarm On, No Smoke In Local Chamber	X	BLINK[1]	ON[2]	HIGH[3]	ON

X = Don't Care

1. 30-ms pulse every 50 seconds (typ.).
2. Alarm horn may be programmed for continuous sound by connecting terminal 11 to V+. The alarm may be pulsed by connecting terminal 11 to ground through a resistor (from 3.9 to 10 MΩ). The typical duty cycle is 95% ON, and is determined by the size of the resistor.
3. Signal received from activated remote alarm.

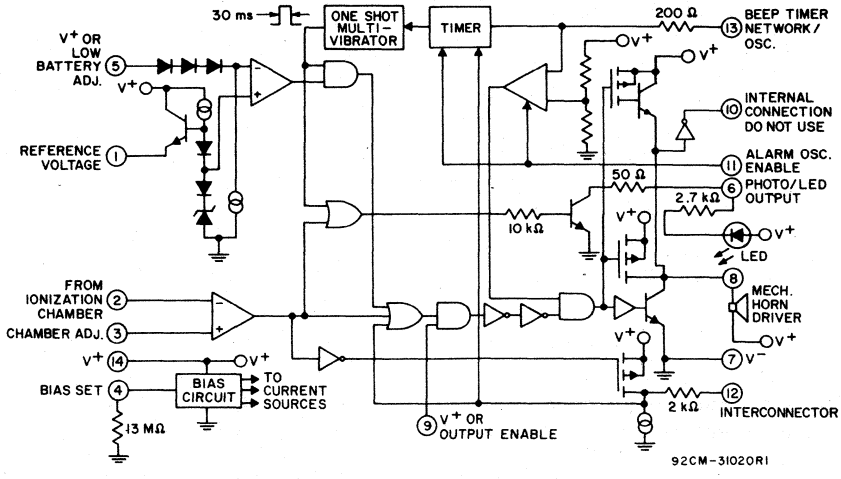


Fig. 1 - Simplified functional diagram for CA3164E.

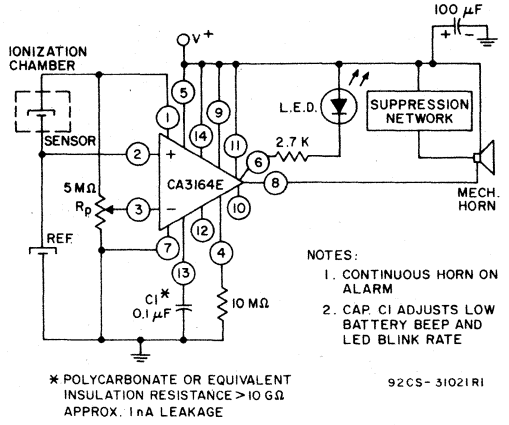


Fig. 2 - Basic ionization detector with electromechanical horn.

CA3164E

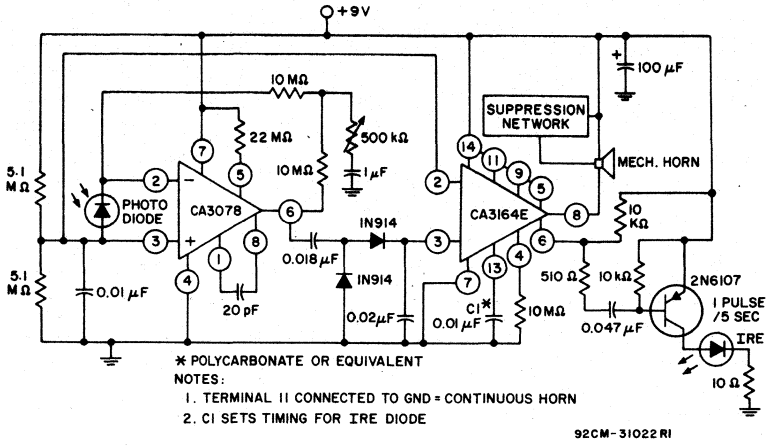


Fig. 3 - Typical photoelectric system using CA3164E.

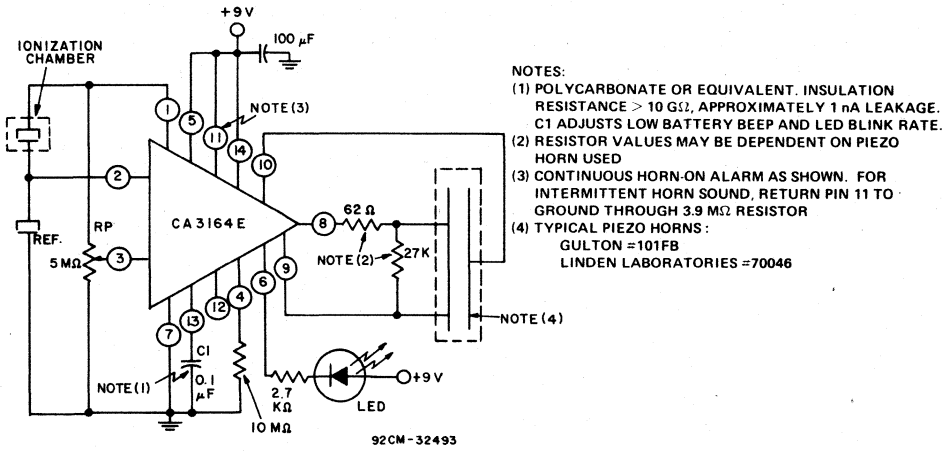
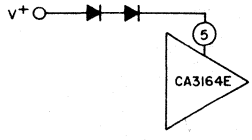


Fig. 4 - Basic ionization detector with piezoelectric horn.

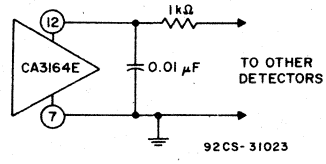
Connections for Optional Functions

1. **Low Battery Adjustment - Terminal 5**
   Add diodes as shown below to increase the low-battery trigger point.



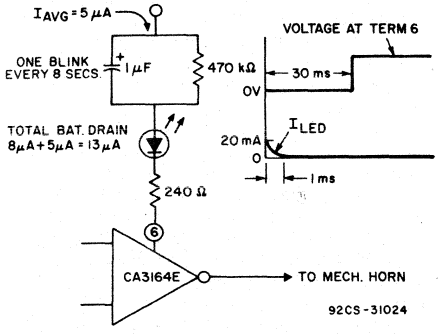
2. **Sounder Operating Mode**
   Continuous sound on alarm - connect terminal 11 to V+.
   Pulsed sound on alarm - connect a 3.9-MΩ resistor between terminal 11 and ground.

3. **Remote (Interconnect)**
   Connect terminal 12 to same terminal on all other units (fan out = 20 units). When interconnecting units for the remote-alarm function, the extremely low currents involved make it extremely important that a provision be made for limiting externally induced transients into the remote terminal. For example, inadvertent contact with external power sources or electrical storm activity may cause triggering of the remote alarm function. The circuit below will reduce the possibility of such occurrences.



4. LED On-Time Adjustment

The CA3164E is designed to provide a fixed LED on-time of approximately 30 ms. For applications requiring a reduction in on-time, the following circuit is recommended:



This circuit reduces the LED on-time but does not affect the horn on-time of 30 ms. When using this configuration during the continuous-alarm mode (smoke in chamber), the LED will be off instead of on, as shown in the truth table. If the horn is pulsed during the alarm mode, the LED will blink at the pulse rate.

Cleaning Procedure

To insure leakage currents of less than 1 pA, the following procedure is recommended:

(a) degrease in trichlorethylene
(b) rinse in de-ionized water

Circuit Description

Basic Functions - The CA3164E is designed to interface directly with an ionization-chamber type of smoke detector. Upon being triggered by a decreasing voltage at the ionization-chamber output, the IC operates a mechanical transducer. In addition to this basic smoke-detector function, another circuit monitors and compares the battery voltage to an internal reference-voltage source. Once the battery voltage drops below a defined level, a short 30-ms beep sound is produced in synchronism with an LED indicator every 50 seconds. This rate is determined by a programming resistor connected between terminal 4 and ground and an external 0.1-μF capacitor connected between terminal 13 and ground.

A buffered output voltage is available from the reference supply that may be used to operate the ionization chamber. This voltage helps maintain constant sensitivity with decreasing supply voltage.

There are two alarm modes and two conditions that will sound the alarm. The first alarm condition is the normal smoke in the ionization chamber; the other condition is a high level to the remote input/output terminal of the IC.

The first alarm mode is the customary continuous sound. The second alarm mode is an interrupted or pulsed sound.

Operation - The CA3164E is current programmable by placing a resistor from terminal 4 to ground. This resistor establishes the operating current levels for all the current sources within the IC including the timing circuits.

An operational amplifier configuration is used for the ionization chamber input. P-channel MOS field-effect transistors are used on this input in the bootstrap configuration shown in Fig. 5 to drive the protection diodes and maintain the sub-picoampere input current.

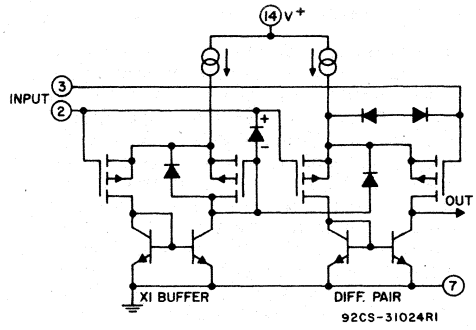


Fig. 5 - Schematic of ionization-chamber amplifier.

A conventional bipolar amplifier is used for the battery monitor circuit. The zener diode is biased at about 3 μA. This zener voltage is raised one V_{AK} and then applied to the base of an emitter-follower transistor to buffer and reflect the zener voltage to the outside reference terminal. By providing an additional input terminal (terminal 5), where three level-shifting diodes are available, an additional external means is provided to raise the voltage level at which the CA3164E goes into the low-voltage alarm mode.

An integrating type of timer is used to generate the one-minute LED power-monitor and battery-function indicator pulse. Fig. 6 shows the system. A constant-current source charges the external 0.1-μF timing capacitor C_T, which subsequently triggers the 30-ms one-shot multivibrator composed of n-channel MOS transistor N_3 and n-p-n transistor Q1.

N_3 is then cut off and its drain climbs to the supply rail, linearly charging capacitor C_{PULSE}. When the drain of N_3 reaches the supply rail, the charging current ceases, cutting off the base current of Q1 and discharging the capacitor.

A open-collector n-p-n transistor is used to drive the optional external LED power monitor and battery-condition indicator (Fig. 1).

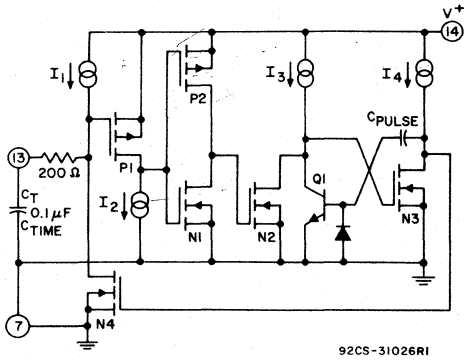


Fig. 6 - Schematic of timer and one-shot multivibrator.

The schematic diagram of the drive circuit for a mechanical horn (M-horn) and a piezoelectric horn (P-horn) is shown in Fig. 7. For M-horn operation, the output of the driver at terminal 8 is used. A large n-p-n transistor Q3 with an active pull-up transistor Q2 provide over 300 mA of drive current. In the M-horn mode, terminal 9 must be returned directly to V+. P-horn operation requires the output from a second inverting amplifier at terminal 10, as well as the output from terminal 8. For P-horn operation, terminal 9 is connected to the feedback terminal of the horn.

The horn output, on alarm, can be continuous or pulsed. The mode is determined by the connection of terminal 11. When this terminal is connected to V+, the alarm sound is continuous, and when it is connected to ground through a programming resistor, as shown in Fig. 7, the alarm is pulsed. The pulse rate is determined by the sum of the current through the programming resistor connected to terminal 11 and the current from the basic timer-current source. Thus, when the detector goes into the alarm mode, the nominal 50-second time period is decreased to a nominal 0.5-second period. This 0.5-second period is set by the external 3.9-MΩ resistor. PMOS transistor P4 and bipolar transistor Q6 provide the on-off switching of NMOS transistor N4 in the driver circuit to provide the pulsed output from the horn.

Terminal 12, the interconnect terminal, is both an input and output for the circuit. When connected by two wires to other units, alarm in any one unit will activate the other units. A small sinking current of only 10 μA keeps the line impedance down while a sourcing current of over 2 mA is available in the alarm mode. This current is more than sufficient to trigger over 20 additional units.

Other Applications of the CA3164E

Although the primary function of the CA3164E is smoke detection, it may also be used in many other circuits that require high front-end sensitivity and the very high input resistance of MOS transistors. The internal circuitry of the CA3164E requires a minimum of external components, and the low battery drain eliminates the need for ac power in most circuits.

A few of the possible uses are: humidity sensor, where two metal electrodes replace the ionization chamber; intrusion alarm; P-horn driver; controller for a dc-to-dc converter such as might be used in an electronic photoflash unit; or with a photodiode as an automatic switch for turning on night lights.

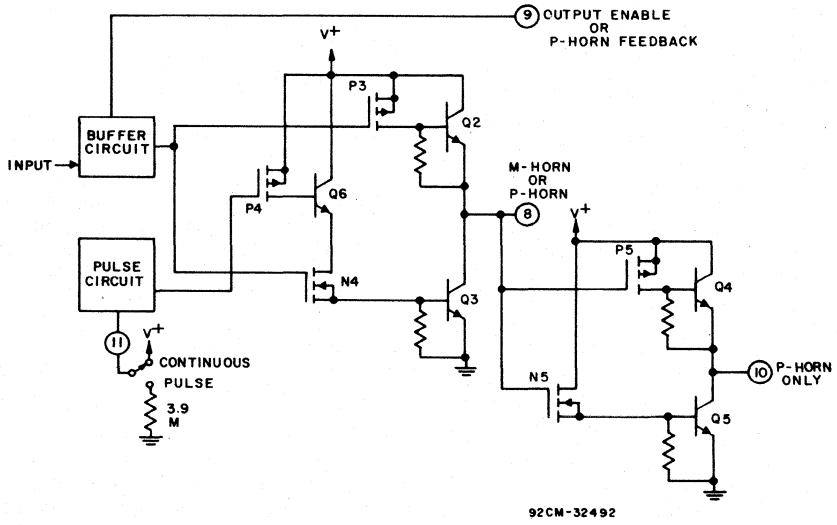
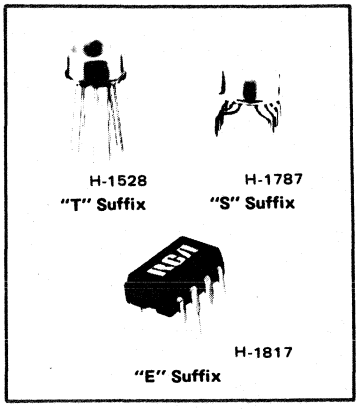


Fig. 7 - Schematic of mechanical and piezoelectric horn drivers.



Timers

For Timing Delays & Oscillator Applications in Commercial, Industrial, and Military Equipment

CA555T, CA555CT:	Standard 8-Lead TO-5 Style Package
CA555S, CA555CS:	Standard 8-Lead TO-5 Style Package With Formed Leads (DIL-CAN)
CA555E, CA555CE:	8-Lead Dual-In-Line Plastic Package (MINI-DIP)

Features:

- *Accurate timing from microseconds through hours*
- *Astable and monostable operation*
- *Adjustable duty cycle*
- *Output capable of sourcing or sinking up to 200 mA*
- *Output capable of driving TTL devices*
- *Normally ON and OFF outputs*
- *High-temperature stability - 0.005%/°C*
- *Directly interchangeable with SE555, NE555, MC1555, and MC1455*

Applications

- *Precision timing*
- *Sequential timing*
- *Time-delay generation*
- *Pulse generation*
- *Pulse-width and position modulation*
- *Pulse detector*

The RCA-CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours. These devices are also useful for astable oscillator operation and can maintain an accurately controlled free-running frequency and duty cycle with only two external resistors and one capacitor.

The circuits of the CA555 and CA555C may be triggered by the falling edge of the wave-form signal, and the output of these circuits can source or sink up to a 200-milliampere current or drive TTL circuits.

The CA555 and CA555C are supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead TO-5 style packages with dual-in-line formed leads (DIL-CAN, S suffix), 8-lead dual-in-line plastic packages (MINI-DIP, E suffix), and in chip form (H suffix). These types are direct replacement for industry types in packages with similar terminal arrangements e.g. SE555 and NE555, MC1555 and MC1455, respectively. The CA555 type circuits are intended for applications requiring premium electrical performance. The CA555C type circuits are intended for applications requiring less stringent electrical characteristics.

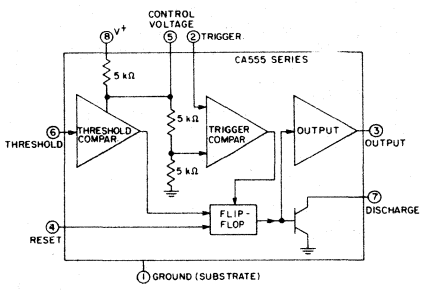


Fig. 1 — Functional diagram of the CA555 series.

CA555, CA555C Types

ELECTRICAL CHARACTERISTICS, *At $T_A = 25^oC$, $V^+ = 5$ to 15 V unless otherwise specified*

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA555			CA555C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
DC Supply Voltage, V^+		4.5	–	18	4.5	–	16	V
DC Supply Current (Low State)*, I^+	$V^+ = 5$ V, $R_L = \infty$	–	3	5	–	3	6	mA
	$V^+ = 15$ V, $R_L = \infty$	–	10	12	–	10	15	mA
Threshold Voltage, V_{TH}		–	(2/3)V^+	–	–	(2/3)V^+	–	V
Trigger Voltage	$V^+ = 5$ V	1.45	1.67	1.9	–	1.67	–	V
	$V^+ = 15$ V	4.8	5	5.2	–	5	–	
Trigger Current		–	0.5	–	–	0.5	–	μA
Threshold Current▲, I_{TH}		–	0.1	0.25	–	0.1	0.25	μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current		–	0.1	–	–	0.1	–	mA
Control Voltage Level	$V^+ = 5$ V	2.9	3.33	3.8	2.6	3.33	4	V
	$V^+ = 15$ V	9.6	10	10.4	9	10	11	V
Output Voltage Drop: Low State, V_{OL}	$V^+ = 5$ V, $I_{SINK} = 5$ mA	–	–	–	–	0.25	0.35	V
	$I_{SINK} = 8$ mA	–	0.1	0.25	–	–	–	
	$V^+ = 15$ V, $I_{SINK} = 10$ mA	–	0.1	0.15	–	0.1	0.25	V
	$I_{SINK} = 50$ mA	–	0.4	0.5	–	0.4	0.75	
	$I_{SINK} = 100$ mA	–	2.0	2.2	–	2.0	2.5	
	$I_{SINK} = 200$ mA	–	2.5	–	–	2.5	–	
High State, V_{OH}	$V^+ = 5$ V, $I_{SOURCE} = 100$ mA	3.0	3.3	–	2.75	3.3	–	V
	$V^+ = 15$ V, $I_{SOURCE} = 100$ mA	13.0	13.3	–	12.75	13.3	–	
	$I_{SOURCE} = 200$ mA	–	12.5	–	–	12.5	–	
Timing Error (Monostable): Initial Accuracy	R_1, R_2 = 1 to 100 kΩ, C = 0.1 μF, Tested at $V^+ = 5$ V, $V^+ = 15$ V	–	0.5	2	–	1	–	%
Frequency Drift with Temperature		–	30	100	–	50	–	p/m/^oC
Drift with Supply Voltage		–	0.05	0.2	–	0.1	–	%/V
Output Rise Time, t_r		–	100	–	–	100	–	ns
Output Fall Time, t_f		–	100	–	–	100	–	ns

* When the output is in a high state, the dc supply current is typically 1 mA less than the low-state value.

▲ The threshold current will determine the sum of the values of R_1 and R_2 to be used in Fig. 16 (astable operation): the maximum total $R_1 + R_2 = 20$ MΩ.

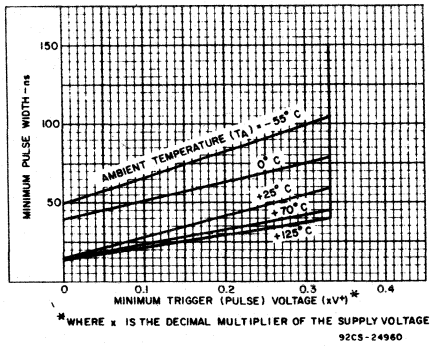


Fig.2 – Minimum pulse width vs. minimum trigger voltage.

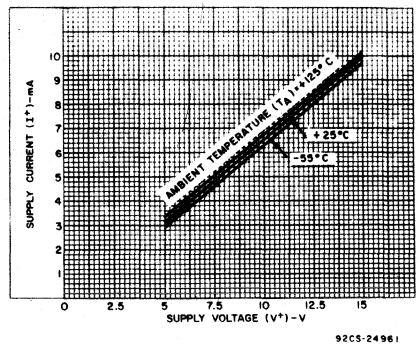


Fig.3 – Supply current vs. supply voltage.

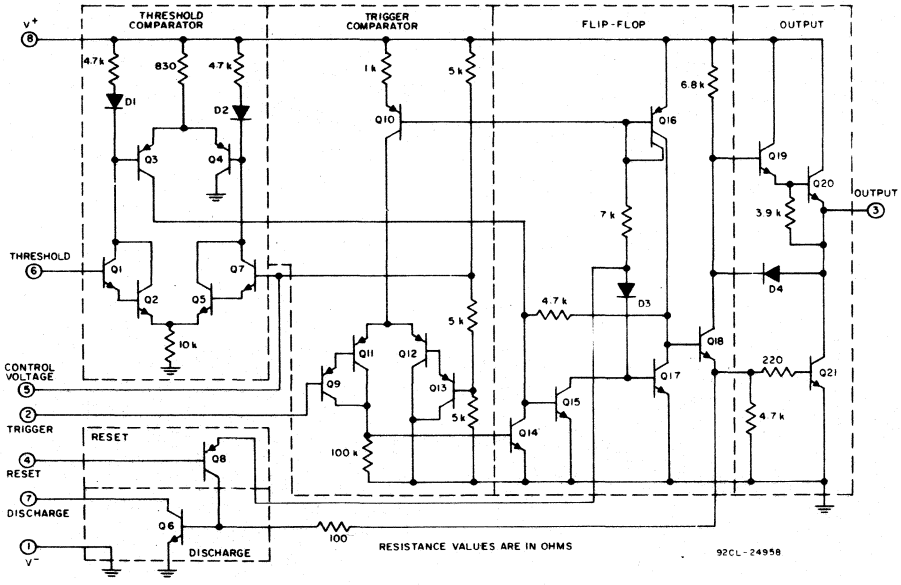
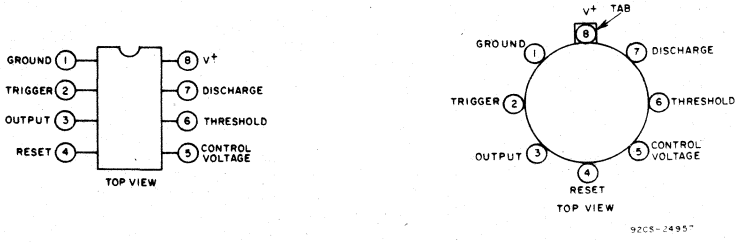


Fig.4 – Schematic diagram of the CA555 and CA555C.



a. MINI-DIP plastic package
TO-5 style package with formed leads

b. TO-5 style package

Fig.5 – Terminal assignment diagrams.

CA555, CA555C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE . . .	18	V
DEVICE DISSIPATION:		
Up to T_A = 55°C	600	mW
Above T_A = 55°C Derate linearly	5	mW/°C
AMBIENT TEMPERATURE RANGE (All Types):		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. . . .	+265	°C

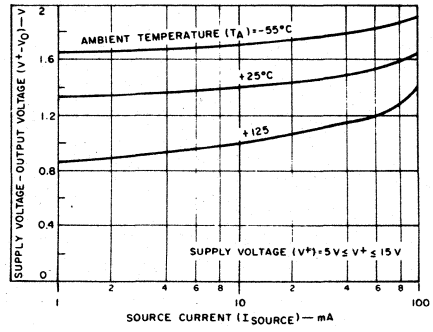


Fig.6 — Output voltage drop (high state) vs. source current.

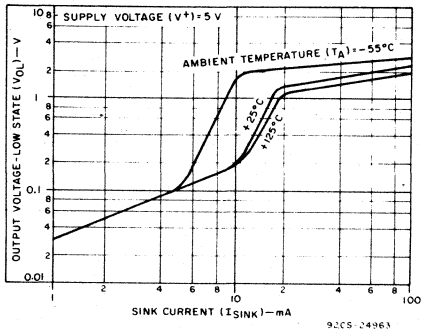


Fig.7 — Output voltage-low state vs. sink current at V^+ = 5 V.

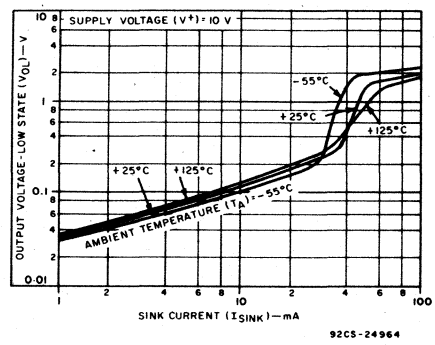


Fig.8 — Output voltage-low state vs. sink current at V^+ = 10 V.

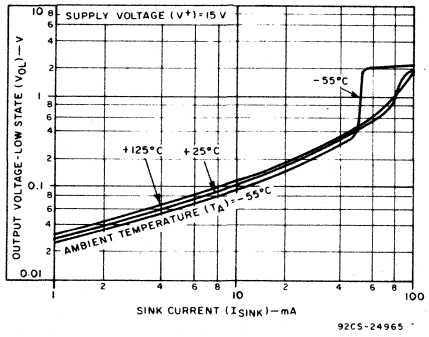


Fig.9 — Output voltage-low state vs. sink current at V^+ = 15 V.

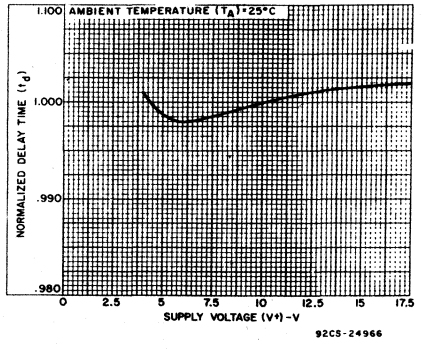


Fig.10 — Delay time vs. supply voltage.

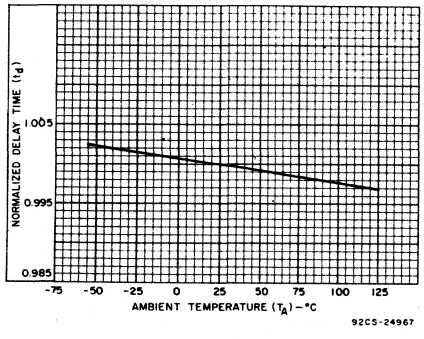


Fig.11 — Delay time vs. temperature.

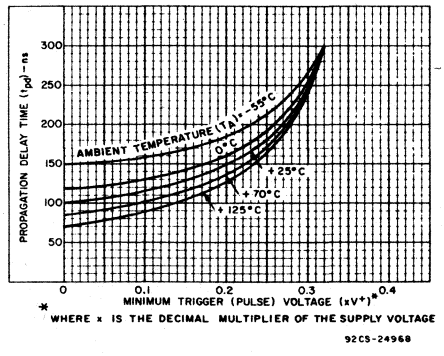


Fig.12 — Propagation delay time vs. trigger voltage.

TYPICAL APPLICATIONS

Reset Timer (Monostable Operation)

Fig.13 shows the CA555 connected as a reset timer. In this mode of operation capacitor C_T is initially held discharged by a transistor on the integrated circuit. Upon closing the "start" switch, or applying a negative trigger pulse to terminal 2, the integral timer flip-flop is "set" and releases the short circuit across C_T which drives the output voltage "high" (relay energized). The action allows the voltage across the capacitor to increase exponentially with the time constant $t = R_1C_T$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state.

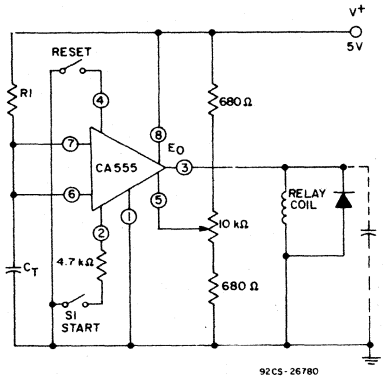


Fig.13 – Reset timer (monostable operation).

Since the charge rate and threshold level of the comparator are both directly proportional to V^+, the timing interval is relatively independent of supply voltage variations. Typically, the timing varies only 0.05% for a 1 volt change in V^+.

Applying a negative pulse simultaneously to the reset terminal (4) and the trigger terminal (2) during the timing cycle discharges C_T and causes the timing cycle to restart. Momentarily closing only the reset switch during the timing interval discharges C_T, but the timing cycle does not restart.

Fig.14 shows the typical waveforms generated during this mode of operation, and Fig.15 gives the family of time delay curves with variations in R_1 and C_T.

Repeat Cycle Timer (Astable Operation)

Fig.16 shows the CA555 connected as a repeat cycle timer. In this mode of operation, the total period is a function of both R_1 and R_2;

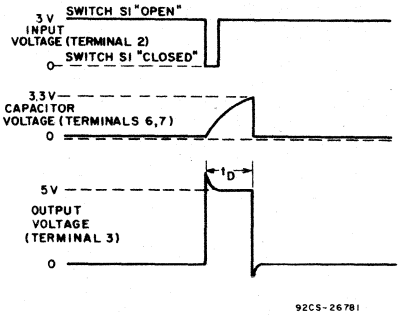


Fig.14 – Typical waveforms for reset timer.

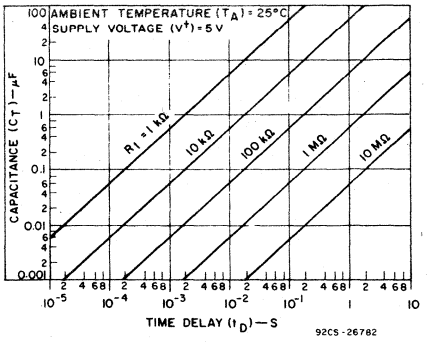


Fig.15 – Time delay vs. resistance and capacitance.

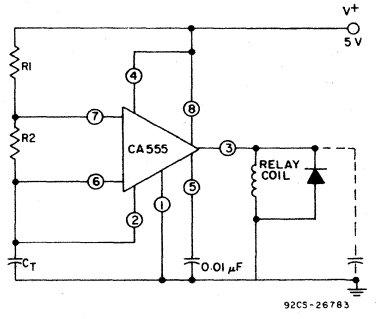


Fig.16 – Repeat cycle timer (astable operation).

$$T = 0.693(R_1 + 2R_2)C_T = t_1 + t_2$$

where $t_1 = 0.693(R_1 + R_2)\,C_T$

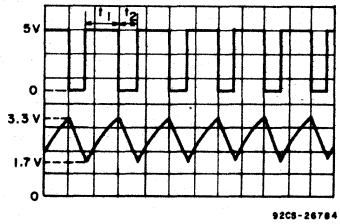
and $t_2 = 0.693(R_2)C_T$

The duty cycle is:

$$\frac{t_2}{t_1 + t_2} = \frac{R_2}{R_1 + 2R_2}$$

Typical waveforms generated during this mode of operation are shown in Fig. 17. Fig. 18 gives the family of curves of free running frequency with variations in the value of $(R_1 + 2R_2)$ and C_T.

CA555, CA555C Types



Top Trace: Output voltage (2V/div. and 0.5 ms/div.)
Bottom Trace: Capacitor voltage (1 V/div. and 0.5 ms/div.)

Fig.17 – Typical waveforms for repeat cycle timer.

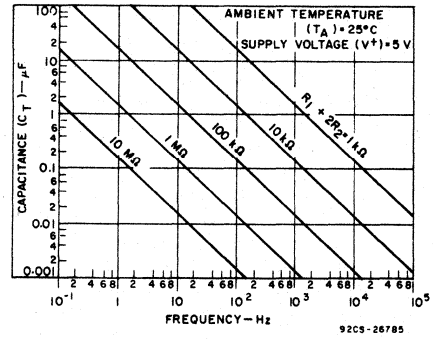
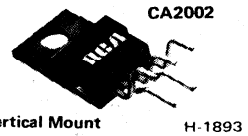


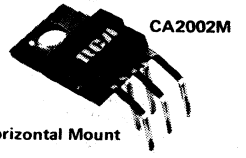
Fig.18 – Free running frequency of repeat cycle timer with variation in capacitance and resistance.

Audio Circuits
Technical Data

CA2002, CA2002M



Vertical Mount H-1893



Horizontal Mount

VERSA-V TO-220-Style Plastic Packages H-1894

8-Watt Audio Power Amplifier

Especially suited for automobile and other mobile applications

FEATURES:

- *Output short-circuit and thermal overload protection*
- *Drives load impedance as low as 1.6Ω*
- *Load dump voltage surge protection*
- *Output current capability of up to 3.5A*
- *Few external components*
- *Versa-V power transistor package-requires no electrical insulation*

The RCA-CA2002 is a monolithic silicon class B audio power amplifier designed for driving loads as low as 1.6Ω. It provides a high output current capability (up to 3.5A), very low harmonic and cross-over distortion, and load-dump voltage-surge protection.

The maximum operating supply-voltage of the CA2002 is 18 V, and internal protection is provided for peaks of up to 40 V, as shown in Fig. 18. Supply-voltage peaks of more than 40 V will require an LC network between the supply and terminal 5. An LC network, such as the one shown in Fig. 18, provides protection against supply-voltage surges of up to 120 V for 2 ms. This type of protection is ON when the supply voltage (pulsed or dc exceeds 18 V).

Thermal shut-down occurs if the output overloads (temporary or permanent), the ambient temperature is excessive, or the junction temperature is excessive. None of these conditions results in device damage. They merely cause a temporary automatic reduction of output power and drain current, as shown in Figs. 16 and 17.

A heater fan motor run-down hysteresis circuit is included for automotive applications. Typical starting voltage is 10 volts; typical drop-out voltage is 6.5 volts.

The CA2002 is supplied in a 5-lead plastic TO-220-style VERSA-V package. All leads (except term. 3) are electrically insulated from the mounting flange, eliminating the need for insulating hardware. The VERSA-V package is available with two lead configurations. The CA2002 has a vertical-mount lead form, and the CA2002M has a horizontal-mount lead form.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

PEAK SUPPLY VOLTAGE (50 ms)	40 V
DC SUPPLY VOLTAGE	28 V
OPERATING SUPPLY VOLTAGE	18 V
OUTPUT PEAK CURRENT:	
REPETITIVE	3.5 A
NON-REPETITIVE	4.5 A
POWER DISSIPATION, P_D at $T_A = 90°C$	15 W
THERMAL RESISTANCE, JUNCTION TO CASE	4° C/W
AMBIENT-TEMPERATURE RANGE:	
OPERATING	**See Figures 16 & 17**
STORAGE	-40 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 12 s max.	260° C

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 14.4 V
Unless otherwise specified (See Figure 2)

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
			Min.	Typ.	Max.	
Supply Voltage, V^+			11	–	18	V
Quiescent Output Voltage, V_O	Measure at Term. 4		6.4	7.2	8	V
Quiescent Drain Current, I_D	Measure at Term. 5		–	45	80	mA
Output Power, P_O	THD = 10%, A = 40 dB, f = 1 KHz					
	V^+ = 14.4V	R_L = 4 Ω	4.8	5.2	–	W
		R_L = 2 Ω	7	8	–	
	V^+ = 16 V	R_L = 4 Ω	–	6.5	–	
		R_L = 2 Ω	–	10	–	
Input Saturation Voltage, $V_{I(RMS)}$			400	–	–	mV
Input Sensitivity, e_I	A = 40 dB, f = 1 KHz					
		P_O = 0.5 W, R_L = 4 Ω	–	15	–	mV
		P_O = 0.5 W, R_L = 2 Ω	–	11	–	
		P_O = 5.2 W, R_L = 4 Ω	–	55	–	
		P_O = 8 W, R_L = 2 Ω	–	50	–	
Frequency Response (−3 dB)	R_L = 4 Ω (See Fig. 19)			25000		Hz
Input Resistance, R_I (Term. 1)	f = 1 KHz		70	150	–	KΩ
Open-Loop Voltage Gain, A_{OL}	R_L = 4 Ω, f = 1 KHz		–	80	–	dB
Closed-Loop Voltage Gain, A	R_L = 4Ω, f = 1 KHz		39.5	40	40.5	dB
Input Noise Voltage, e_N	Freq. Resp. = 40 to 15,000 Hz (−3 dB)		400	4	–	μV
Input Noise Current, i_N	Freq. Resp. = 40 to 15,000 Hz (−3 dB)		–	60	–	pA
Efficiency, η	A = 40 dB, f = 1 KHz					
		P_O = 5.2 W, R_L = 4 Ω	–	68	–	%
		P_O = 8 W, R_L = 2 Ω	–	58	–	
Power Supply Rejection Ratio, PSRR	R_L = 4 Ω, A = 40 dB, Rg = 10 KΩ, f_{ripple} = 100 Hz, V_{ripple} = 0.5 V		30	35	–	dB

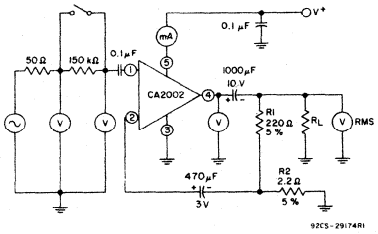


Fig. 1 – Test circuit.

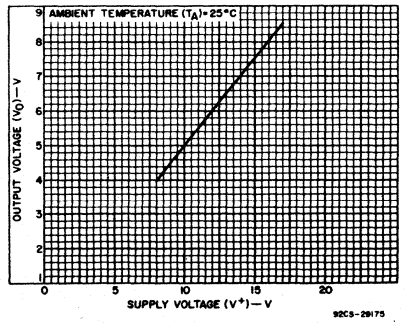


Fig. 2 – Typical quiescent output voltage as a function of supply voltage.

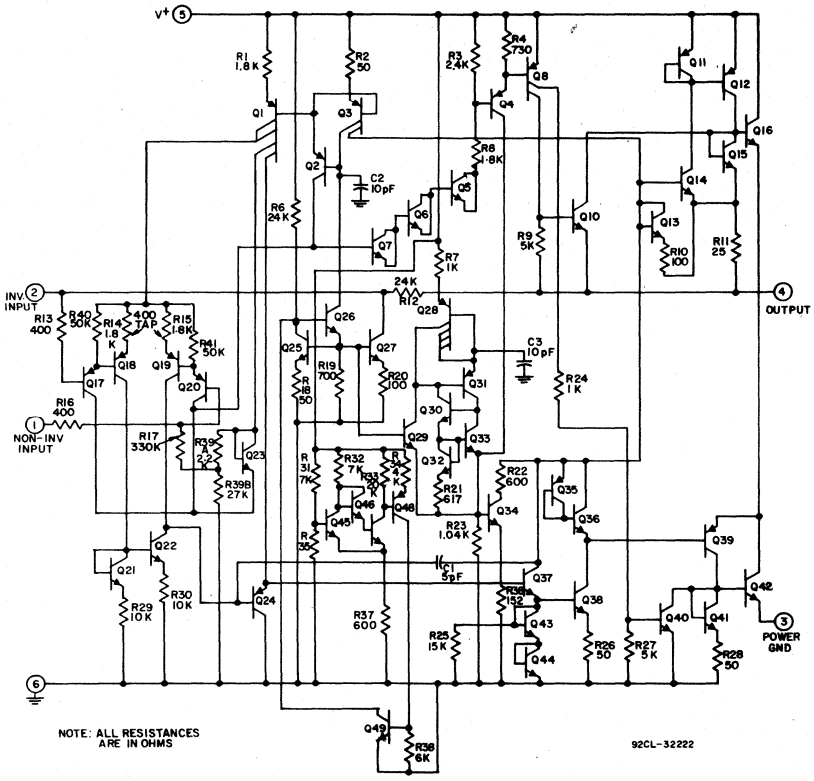


Fig. 3 – Schematic diagram.

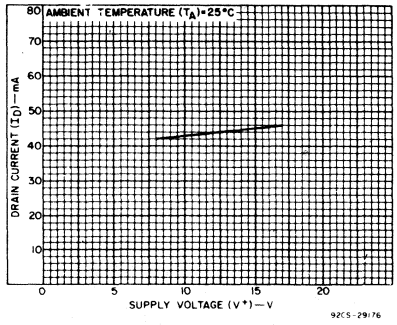


Fig. 4 – Typical quiescent drain current as a function of supply voltage.

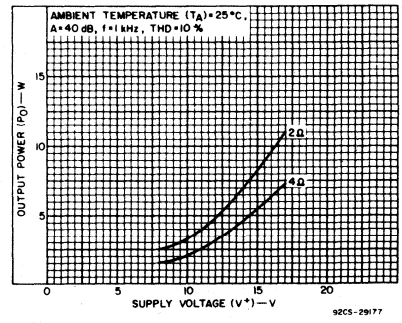


Fig. 5 – Typical output power as a function of supply voltage.

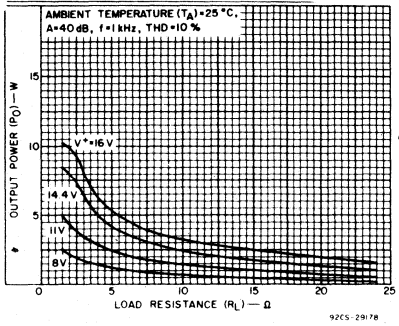


Fig. 6 – Typical output power as a function of load resistance.

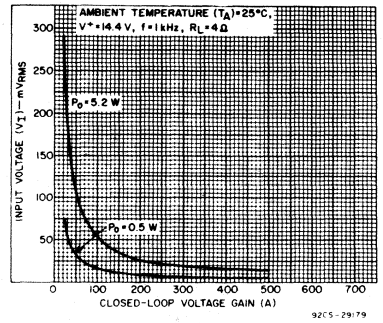


Fig. 7 – Typical input voltage as a function of closed-loop voltage gain.

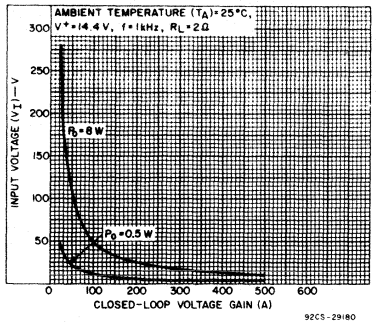


Fig. 8 — Typical input voltage as a function of closed-loop voltage gain.

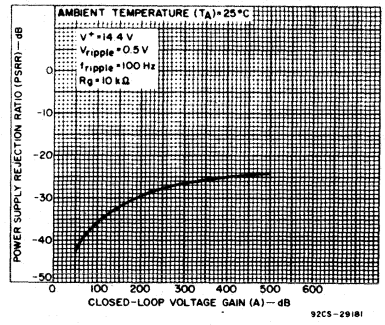


Fig. 9 — Typical power supply rejection ratio as a function of closed-loop voltage gain.

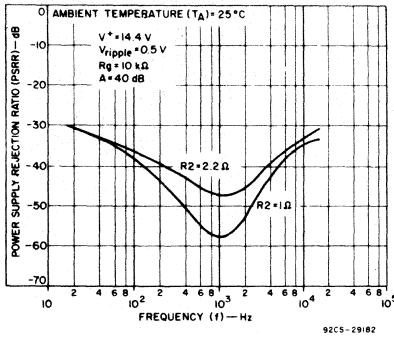


Fig. 10 — Typical power supply rejection ratio as a function of frequency.

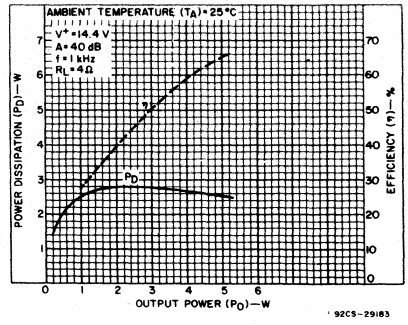


Fig. 11 — Typical power dissipation and efficiency as a function of output power.

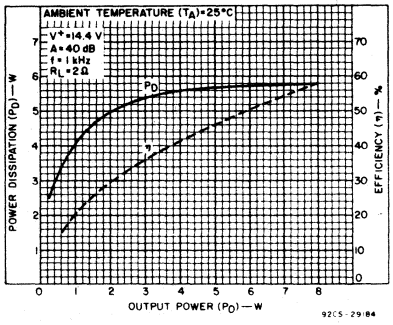


Fig. 12 — Typical power dissipation and efficiency as a function of output power.

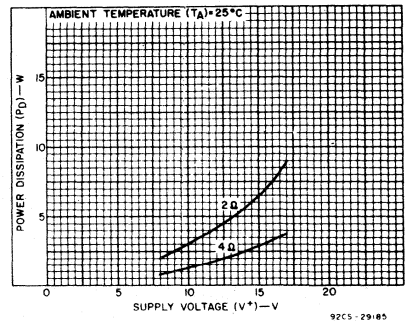


Fig. 13 — Maximum power dissipation as a function of supply voltage (sine-wave operation).

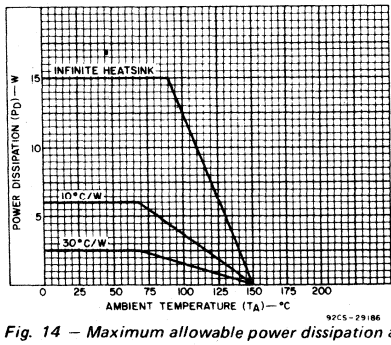


Fig. 14 — Maximum allowable power dissipation as a function of ambient temperature.

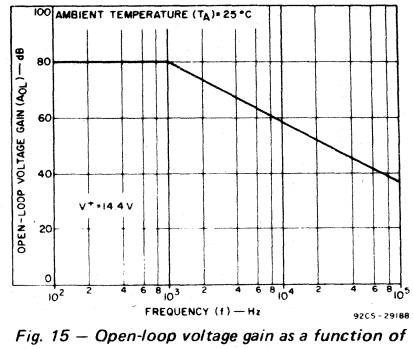


Fig. 15 — Open-loop voltage gain as a function of frequency.

Load-Dump Voltage-Surge Protection

The maximum operating supply-voltage of the CA2002 is 18 V, and internal protection is provided for peaks of up to 40 V, as shown in Fig. 18. Supply-voltage peaks of more than 40 V will require an LC network between the supply and terminal 5. An LC network, such as the one shown in Fig. 18, provides protection against supply-voltage surges of up to 120 V for 2 ms. This type of protection is ON when the supply voltage (pulsed or dc) exceeds 18 V.

Thermal Shut-Down

Thermal shut-down occurs if the output overloads (temporary or permanent), the ambient temperature is excessive, or the junction temperature is excessive. None of these conditions results in device damage. They merely cause a temporary automatic reduction of output power and drain current, as shown in Figs. 16 and 17.

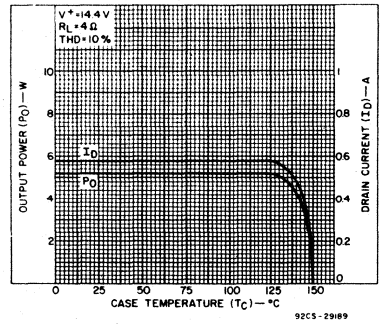


Fig. 16 – Output power and drain current as a function of case temperature.

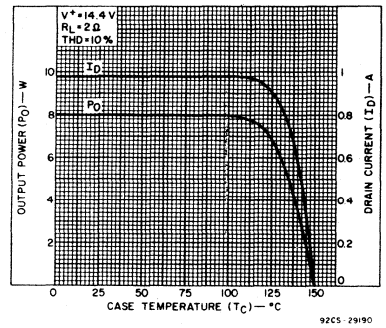


Fig. 17 – Output power and drain current as a function of case temperature.

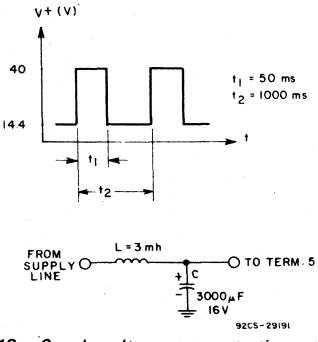


Fig. 18 – Supply-voltage surge protection network and timing diagram.

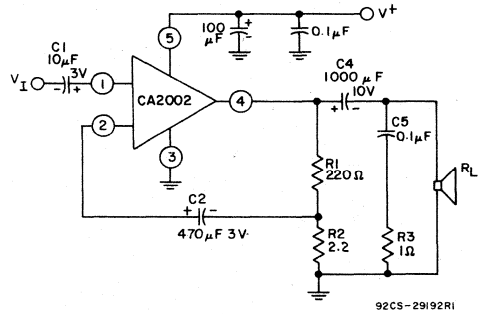


Fig. 19 – Typical application.

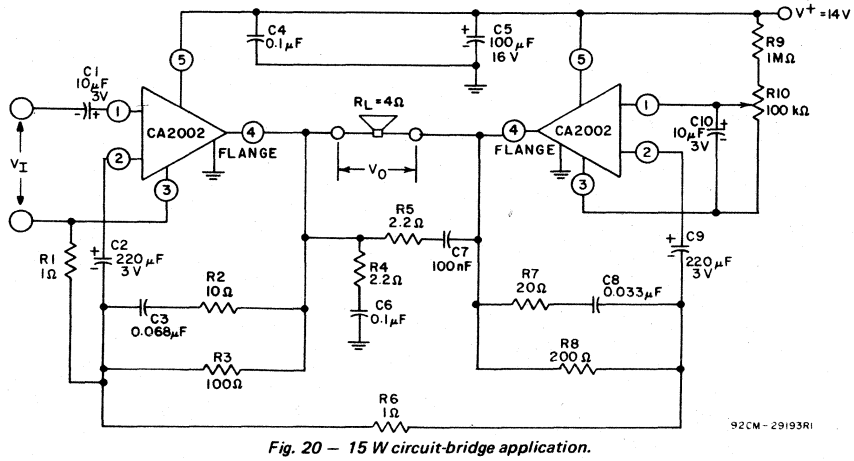
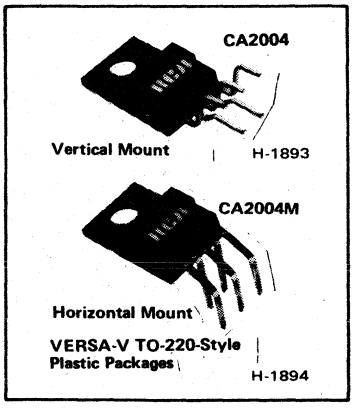


Fig. 20 – 15 W circuit-bridge application.

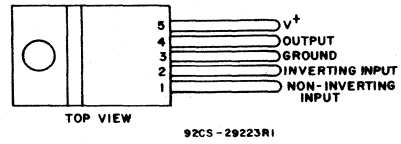


12-Watt Audio Power Amplifier

FEATURES:
- *VERSA-V 5-lead plastic TO-220-style package (insulation not required)*
- *Thermal overload protection*
- *Drives load impedance as low as 3.2Ω*
- *Deflection amplifier capability*
- *Output current capability of up to 3.5 A*
- *Few external components*

The RCA-CA2004 is a monolithic silicon class B audio power amplifier designed for driving loads as low as 3.2Ω. It provides a high output current capability (up to 3.5A), and very low harmonic and cross-over distortion.

The CA2004 is supplied in a 5-lead plastic TO-220-style VERSA-V package. All leads (except term. 3) are electrically insulated from the mounting flange, eliminating the need for insulating hardware. The VERSA-V package is available with two lead configurations. The CA2004 has a vertical-mount lead form, and the CA2004M has a horizontal-mount lead form.



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE	28 V
OPERATING SUPPLY VOLTAGE	26 V
OUTPUT PEAK CURRENT:	
REPETITIVE	3.5 A
NON-REPETITIVE	4.5 A
POWER DISSIPATION, P_D at T_A = 90°C	15 W
THERMAL RESISTANCE, JUNCTION TO CASE	4°C/W
AMBIENT-TEMPERATURE RANGE:	
OPERATING	0 to +125°C
STORAGE	-40 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 12 s max.	260°C

CA2004, CA2004M

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 24 V
Unless otherwise specified (See Figure 1)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Voltage, V^+		8	–	26	V
Quiescent Output Voltage, V_O	Measure at Term. 4	11	12	13	V
Quiescent Drain Current, I_D	Measure at Term. 5	–	40	100	mA
Output Power, P_O	THD = 10%, A = 40 dB, f = 1 KHz, R_L = 4 Ω	10	12	–	W
	THD = 10%, A = 40 dB, f = 1 KHz, R_L = 8 Ω	–	8	–	W
Input Saturation Voltage, $V_{I(RMS)}$		400	–	–	mV
Input Resistance, R_I (Term.1)	f = 1 KHz	70	150	–	KΩ
Open-Loop Voltage Gain, A_{OL}	R_L = 8 Ω, f = 1 KHz	–	80	–	dB
Closed-Loop Voltage Gain, A	R_L = 8 Ω, f = 1 KHz	39.5	40	40.5	dB
Input Noise Voltage, e_N	Freq. Resp. = 40 to 15,000 Hz (–3 dB)	–	4	–	μV
Power Supply Rejection Ratio, PSRR	R_L = 4 Ω, A = 40 dB, Rg = 10 KΩ, f_{ripple} = 100 Hz, V_{ripple} = 0.5 V	30	35	–	dB

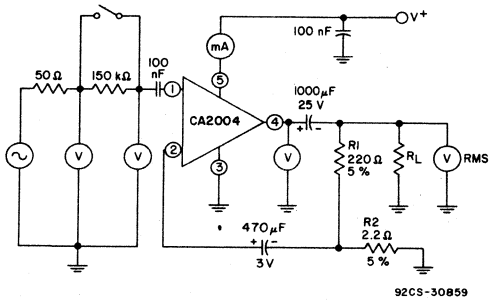


Fig. 1 – Test circuit.

Thermal Shut-Down

Thermal shut-down occurs if the output overloads (temporary or permanent), the ambient temperature is excessive, or the junction temperature is excessive. None of these conditions results in device damage. They merely cause a temporary automatic reduction of output power and drain current.

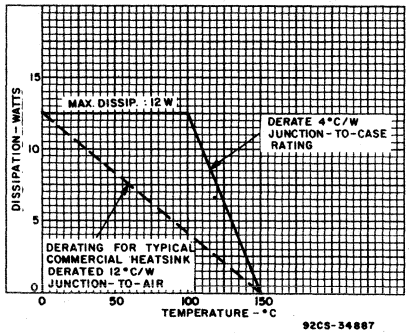


Fig. 2 —Derating curve

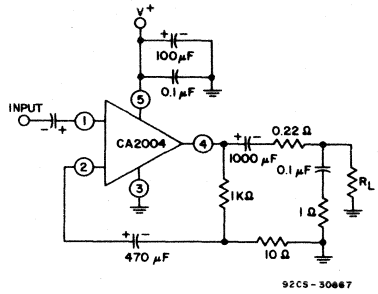


Fig. 3 — Typical application.

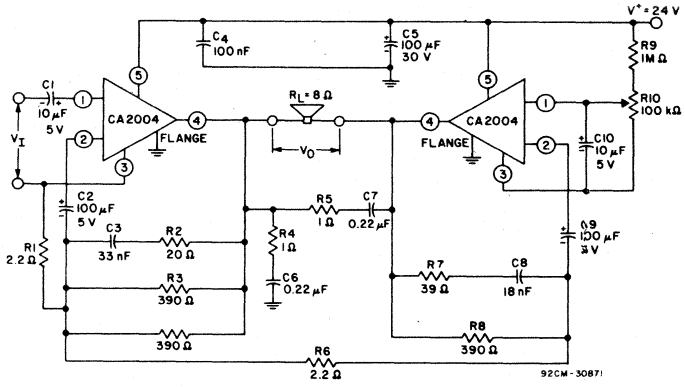


Fig. 4 — 25 W circuit-bridge application.

Radio Circuits
Technical Data

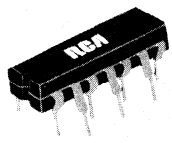
AM/FM Communications Circuits

FM IF Circuits

Gain Blocks

Subsystems

CA3075



14-lead dual-in-line plastic package, leads in quad-formed arrangement.

FM IF Amplifier - Limiter, Detector, and Audio Preamplifier

For FM IF Amplifier Applications Up To 20 MHz In Communications Receivers And High-Fidelity Receivers

Features:

- Good sensitivity: Input limiting voltage (knee) = 250 μV typ. at 10.7 MHz
- Excellent AM rejection: 55 dB typ. at 10.7 MHz
- Internal Zener diode regulation for the IF amplifier section
- Low harmonic distortion
- Differential peak detection: Permits simplified single-coil tuning
- Audio preamplifier voltage gain: 21 dB typ.
- Minimum number of external parts required

RCA CA3075 is an integrated circuit which provides, in a single monolithic chip, an FM IF subsystem for Communications and High-Fidelity Receivers. This device, shown in the schematic diagram (Fig. 2), consists of a multistage IF amplifier-limiter section with a Zener regulated power supply, an FM detector stage, and an AF preamplifier section. A typical application of the CA3075, in FM receiver circuits, is shown in the block diagram (Fig. 1).

The three-stage, emitter-follower-coupled IF amplifier section provides a 60-dB typ. voltage gain at an operating frequency of 10.7 MHz and features, because of its transistor constant-current sink, an output stage with exceptionally good limiting characteristics.

The FM detector section, which utilizes a differential-peak-detection circuit, requires only a single coil in the associated outboard detector circuit; hence, tuning the detector circuit is a simple procedure.

The audio preamplifier circuit provides a 21-dB voltage gain with low impedance output for driving subsequent audio amplifier stages.

The CA3075 utilizes a 14-lead dual-in-line plastic package with leads in a special quad-formed arrangement.

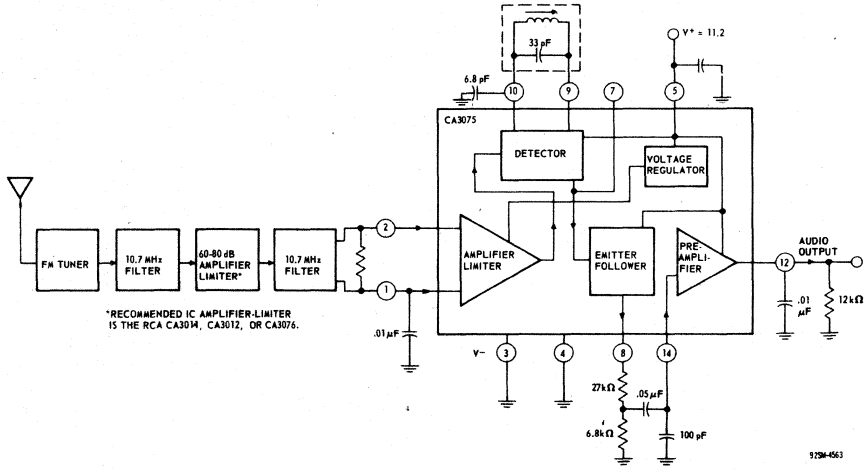


Fig. 1 - Block diagram of typical FM receiver utilizing the CA3075

MAXIMUM RATINGS, *Absolute-Maximum Values at* T_A = 25°C

DC Supply Voltage [between Terminals 5 (V^+) and 3 (V^-)]	12.5	V
DC Current (into Terminal 5)	30	mA
Device Dissipation:		
Up to T_A = 50°C	760	mW
Above T_A = 50°C	derate linearly 7.6	mW/°C
Ambient Temperature Range:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
Lead Temperature (During soldering for 10 s max.)	+260	°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CIRCUIT FIG. NO.
Static Characteristics							
DC Voltage:							
At Terminal 7	V_7	V^+ = 11.2 V	–	6.1	–	V	6
At Terminal 8	V_8		–	5.4	–	V	
At Terminal 12	V_{12}		–	5.2	–	V	
DC Current (into Terminal 5):							
At V^+ = 8.5 V	I_5	–	8.5	15	–	mA	6
At V^+ = 11.2 V			–	17.5	–	mA	
At V^+ = 12.5 V			–	19	29	mA	
Dynamic Characteristics at V^+ = 11.2							
IF AMPLIFIER Input Limiting Voltage (knee, − 3 dB point)	V_I(lim)	f_0 = 10.7 MHz f(Modulation) = 400 Hz Deviation = ±75 kHz	–	250	600	μV	3
AM Rejection	AMR	f_0 = 10.7 MHz f(Modulation) = 400 Hz FM: Deviation = ±75 kHz AM: Modulation = 30%	–	55	–	dB	5
Input Impedance Components:							–
Parallel Resistance	R_I	f_0 = 10.7 MHz	–	4.5	–	kΩ	
Parallel Capacitance	C_I	V_{IN} = 10 mV RMS	–	4.5	–	pF	
DETECTOR							3
Recovered AF Voltage (at Terminal 12)	V_O(AF)	f_0 = 10.7 MHz f(Modulation) = 400 Hz	–	1.5	–	V	
Total Harmonic Distortion	THD	Deviation = ± 75 kHz	–	1	2	%	
AUDIO PREAMPLIFIER							
Voltage Gain	A(AF)	V_{IN} = 100 mV, f_0 = 400 Hz	–	21	–	dB	4
Total Harmonic Distortion	THD	V_{OUT} = 2 V, f_0 = 400 Hz	–	1.5	5	%	4

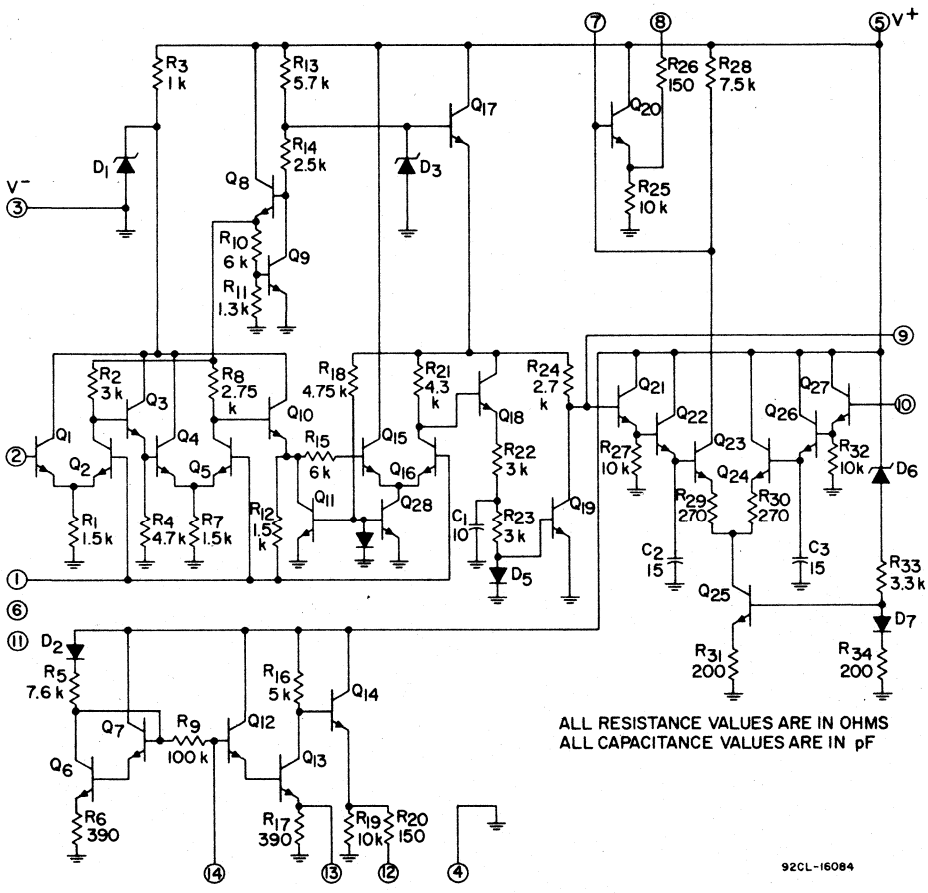


Fig. 2 - Schematic diagram of CA3075

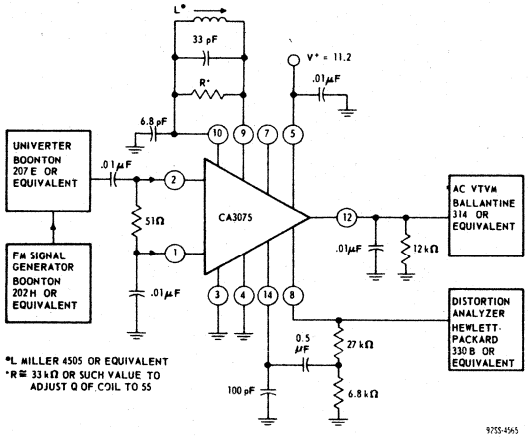


Fig. 3 - Test circuit for input limiting voltage, recovered AF voltage, and total harmonic distortion

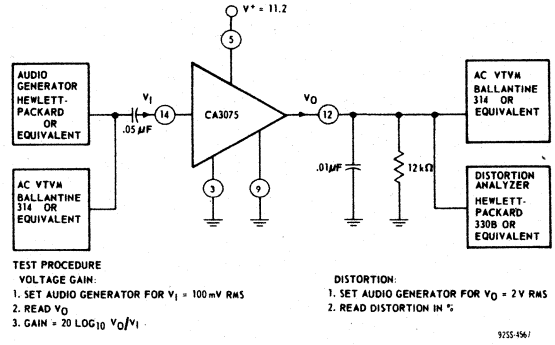


Fig. 4 - Test circuit for audio preamplifier voltage gain and total harmonic distortion

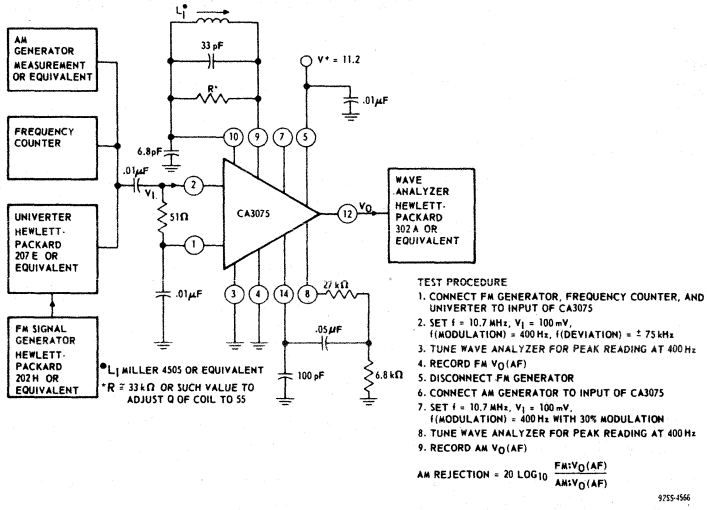


Fig. 5 - Test circuit for AM rejection

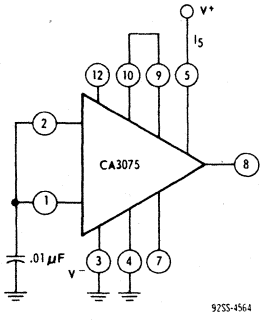
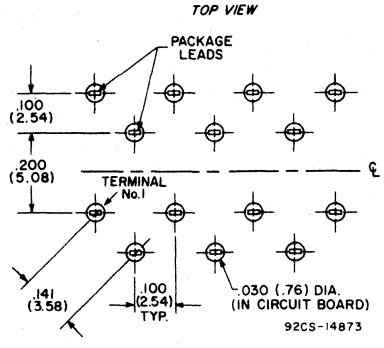


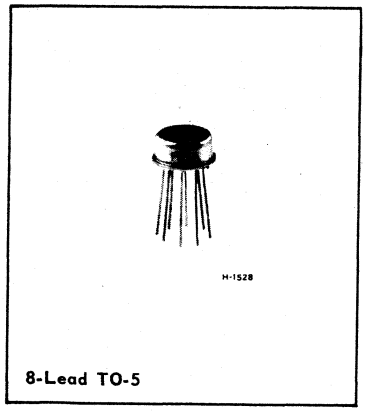
Fig. 6 - Test circuit for static characteristics

Recommended Mounting-Hole Dimensions and Spacings.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.

CA3076



High-Gain Wide-Band IF Amplifier-Limiter

For FM IF Amplifier Applications in Communications Receivers

Features:

- exceptionally good sensitivity: input limiting voltage (knee) = 50 μV typ. at 10.7 MHz
- high gain: 80 dB with 2-kilohm load
- internal voltage supply regulator
- wide frequency capability: > 20 MHz

RCA CA3076, monolithic integrated circuit, is a high-gain wide-band amplifier-limiter for use in the IF sections of Communications and High-Fidelity FM Receivers. The CA3076, shown in the schematic diagram (Fig. 2), consists of a four stage IF amplifier-limiter section with a voltage regulator section. A typical application of the CA3076 in FM receiver circuits is shown in the block diagram (Fig. 1).

The four-stage emitter-follower-coupled IF amplifier section provides an 80-dB voltage gain with a 2-kilohm load at a frequency of 10.7 MHz. The output stage has exceptionally good limiting characteristics because of its transistor constant-current sink. The voltage regulator section provides zener-regulated, decoupled voltages for the IF amplifier.

The CA3076 utilizes an hermetically-sealed 8-lead TO- package.

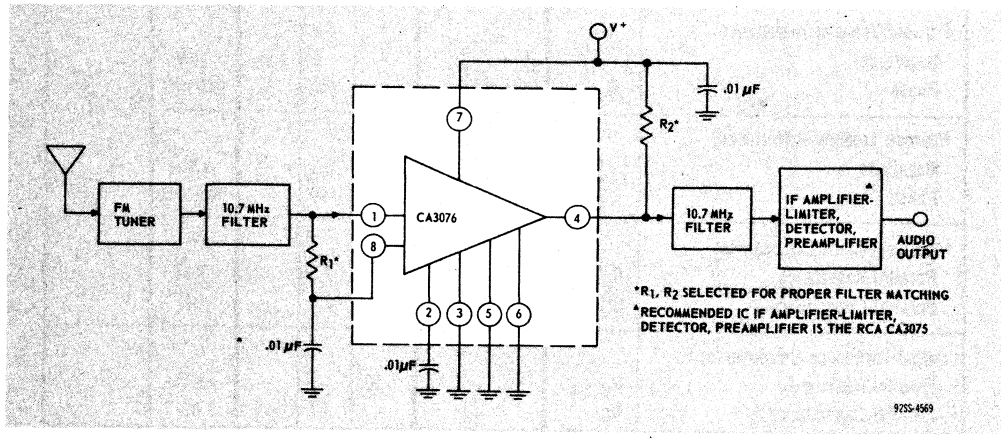


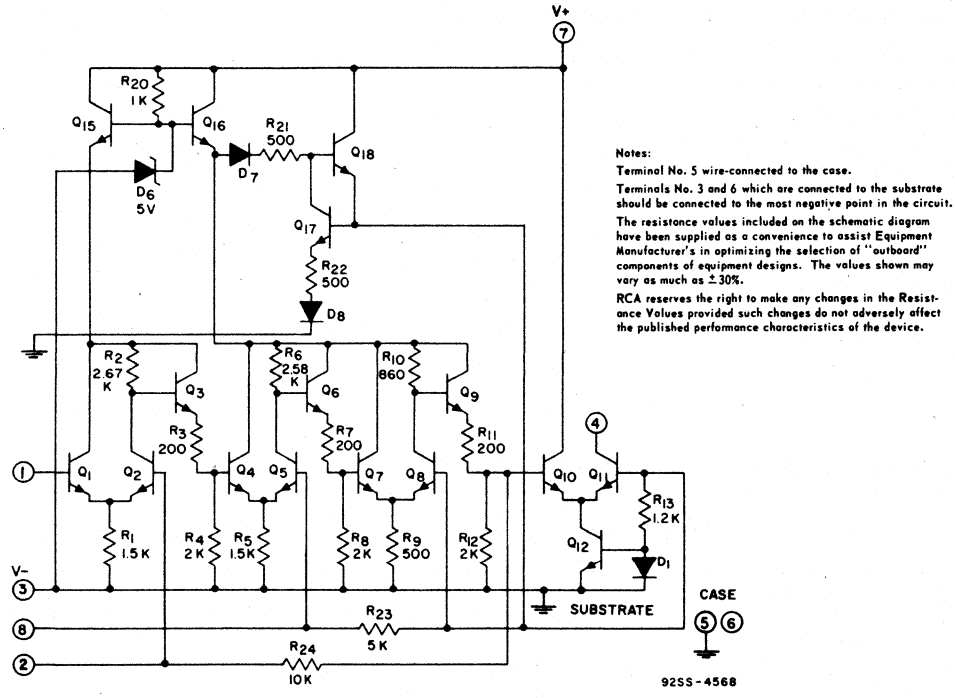
Fig. 1 - Block diagram of typical FM receiver utilizing the CA3076.

MAXIMUM RATINGS, *Absolute Maximum-Values at* T_A = 25°C

DC Supply Voltage [between Terminals 7 (V^+) and 3 (V^-)]	15	V
DC Current (into Terminal 7)	35	mA
Device Dissipation:		
Up to T_A = 50°C	500	mW
Above T_A = 50°C	derate linearly 5	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/32 in (3.17 mm) from seating plane for 10 s max	+260	°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	TEST CIRCUIT FIG. NO.
			MIN.	TYP.	MAX.		
Static Characteristics – V^+ = 8.5 V							
DC Current (into Term. 7)	I_7	–	10	15	24	mA	3
Quiescent Operating Current (into Term. 4)	I_4	–	–	0.65	–	mA	3
Dynamic Characteristics – V^+ = 8.5 V, f_O = 10.7 MHz							
Input Limiting Voltage (knee, −3 dB point)	V_I (lim.)	–	–	50	200	μV	–
Output Voltage	V_O	V_I = 20 μV	4	12	–	mV	5
Output Noise Voltage	V_N	V_I = 0	–	1	–	mV	5
Forward Transfer Admittance:							
Magnitude	$\lvert Y_{21} \rvert$	V_I =	–	6	–	mho	4
Phase	θ_{21}	10 μV	–	80	–	degrees	
Reverse Transfer Admittance:							
Magnitude	$\lvert Y_{12} \rvert$	–	–	0.1	–	μmho	–
Phase	θ_{12}		–	−90	–	degrees	
Input-Impedance Components:							
Parallel Resistance	R_I	–	–	7.5	–	kΩ	–
Parallel Capacitance	C_I		–	4	–	pF	
Output-Impedance Components:							
Parallel Resistance	R_O	–	50	–	–	kΩ	–
Parallel Capacitance	C_O		–	1.7	–	pF	



Notes:

Terminal No. 5 wire-connected to the case.

Terminals No. 3 and 6 which are connected to the substrate should be connected to the most negative point in the circuit.

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturer's in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

Fig. 2 - Schematic diagram of CA3076.

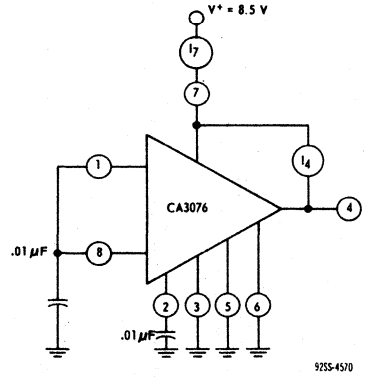


Fig. 3 - Test circuit for DC current (Terminal 7) and operating current (Terminal 4).

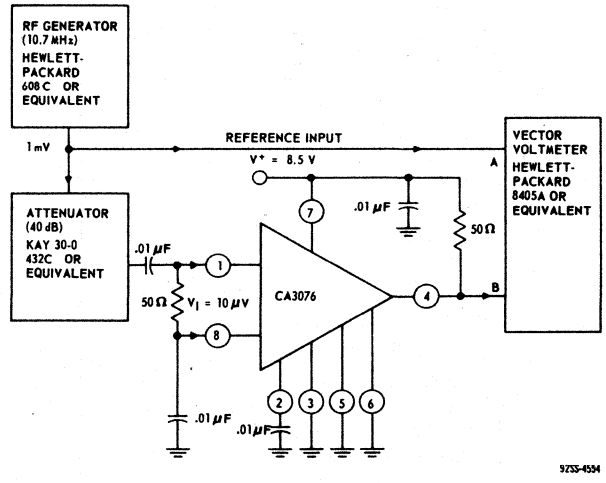
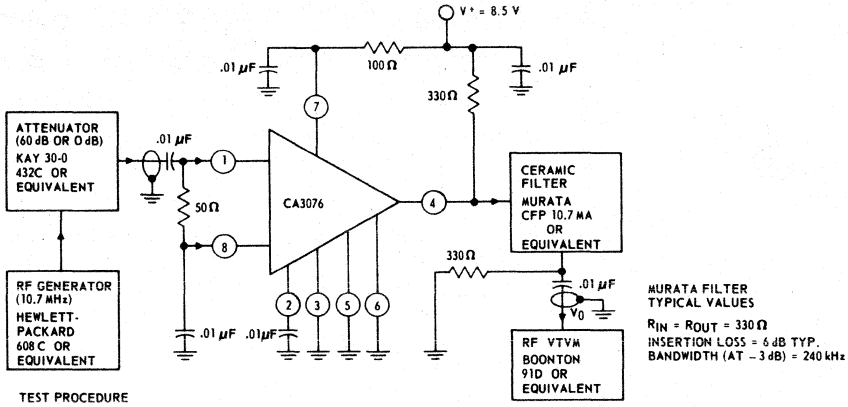


Fig. 4 - Forward transfer admittance (Y_{21}) test circuit



TEST PROCEDURE

OUTPUT VOLTAGE:

1. SET ATTENUATOR TO 0 dB
2. SET RF GENERATOR TO 20 μV CW
3. READ V_0 IN mV

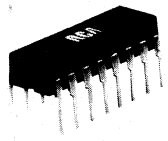
OUTPUT NOISE VOLTAGE:

1. SET ATTENUATOR TO 60 dB
2. READ V_0 IN mV

92SS-4571

Fig. 5 - 10.7 MHz voltage gain and noise test circuit

CA3088E



H-1622

16-Lead Dual-In-Line Plastic Package

AM Receiver Subsystem and General-Purpose Amplifier Array

Includes: AM Converter, IF Amplifiers, Detector and Audio Preamplifier

For Applications in a Variety of AM Broadcast and Communications Receivers and Applications Requiring an Array of Amplifiers

Features:

- **Excellent overload characteristics**
- **AGC for IF amplifier**
- **Buffered output signal for tuning meter**
- **Low harmonic distortion (THD)**
- **Delayed AGC for RF amplifier**
- **Terminals for optional inclusion of tone control**
- **Internal Zener diode provides voltage regulation**
- **Two IF amplifier stages**
- **Low-noise converter and first IF amplifier**
- **Operates from wide range of power supplies: V^+ = 6 to 16 volts**
- **Optional AC and/or DC feedback on wide-band amplifier**
- **Array of amplifiers for general-purpose applications**
- **Suitable for use with optional external RF stage, either MOS or bipolar**

RCA-CA3088E*, a monolithic integrated circuit, is an AM subsystem that provides the converter, IF amplifier, detector, and audio preamplifier stages for an AM receiver.

The CA3088E also provides internal AGC for the first IF amplifier stage, delayed AGC for an optional external RF amplifier, a buffer stage to drive a tuning meter, and terminals facilitating the optional use of a tone control.

Fig. 2 is a functional diagram of the CA3088E. The signal from the low-noise converter is applied to the first IF amplifier and is then coupled to the second IF amplifier. This IF signal is then detected and externally filtered. The resultant audio signal is applied to an audio preamplifier. Optionally, a tone control circuit may be connected at the junction of the detector circuit and the audio preamplifier. The gain of the first IF amplifier stage is controlled by an internal AGC circuit. The CA3088E supplies a delayed AGC signal output for use with an external RF amplifier. A buffered output signal is also available for driving a tuning meter. A DC voltage, internally regulated by a Zener diode, supplies the second IF amplifier, the AGC and tuning meter circuits and may also be used with any other stage.

The CA3088E features four independent transistor amplifiers, each incorporating internal biasing for temperature tracking. These amplifiers are particularly useful in general-purpose amplifier, oscillator, and detector applications in a wide variety of equipment designs.

The CA3088E utilizes a 16-lead dual-in-line plastic package and operates over an ambient temperature range of −40°C to +85°C.

*Formerly Developmental Type TA5842.

MAXIMUM RATINGS, *Absolute Maximum Values, at T_A = 25°C*

DC SUPPLY VOLTAGE:		
Across Term. 5 and Terms. 3, 6, 13, 16, respectively	16	V
DC CURRENT:		
At Terms. 3, 6, 13, 16, respectively	10	mA
At Term. 10	30	mA
DEVICE DISSIPATION:		
Up to T_A = 50°C	760	mW
Above T_A = 50°C	derate linearly 7.6	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V^+ = 12 V.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
			TEST CIRCUIT FIG. NO.		
Static (DC) Characteristics					
DC Voltages:					
Terms. 1, 4, 9, 11	$V_{1, 4, 9, 11}$		1	0.7	V
Terms. 2, 7, 8	$V_{2, 7, 8}$			1.4	V
Term. 10	V_{10}			5.6	V
Term. 12	V_{12}			0	V
Term. 15	V_{15}			3.5	V
DC Current:					
Term. 3	I_3		1	0.35	mA
Term. 6	I_6			1.0	mA
Term. 10	I_{10}			20	mA
Term. 13	I_{13}			0	mA
Term. 16	I_{16}			1.2	mA
Dynamic Characteristics					
Detector Output		30% Modulation	4	75	mV RMS
Audio Amplifier Gain	A_{AF}	f = 1 kHz	4	30	dB
Audio Distortion		V_{OUT} = 100 mV	4	0.2	%
Sensitivity:		f_{IN} = 1 MHz			
At Converter Stage Input		Signal-to-Noise Ratio (S/N) = 20 dB	2	200	μV/m
At RF Stage Input			4	100	μV/m
Total Harmonic Distortion	THD	30% Modulation	4	1.0	%
Input Resistance:	R_{IN}				
At Transistor Q1				3500	Ω
At Transistor Q5		No AGC,		2000	Ω
Input Capacitance:	C_{IN}				
At Transistor Q1		Input signal frequency		17	pF
At Transistor Q5		(f_{IN}) = 1 MHz		12	pF
Feedback Capacitance:	C_{FB}				
At Transistor Q1				1.5	pF
At Transistor Q5				1.5	pF

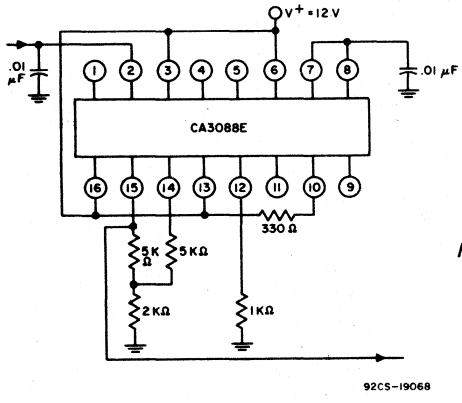


Fig.1—Test circuit for DC characteristics.

CA3088E

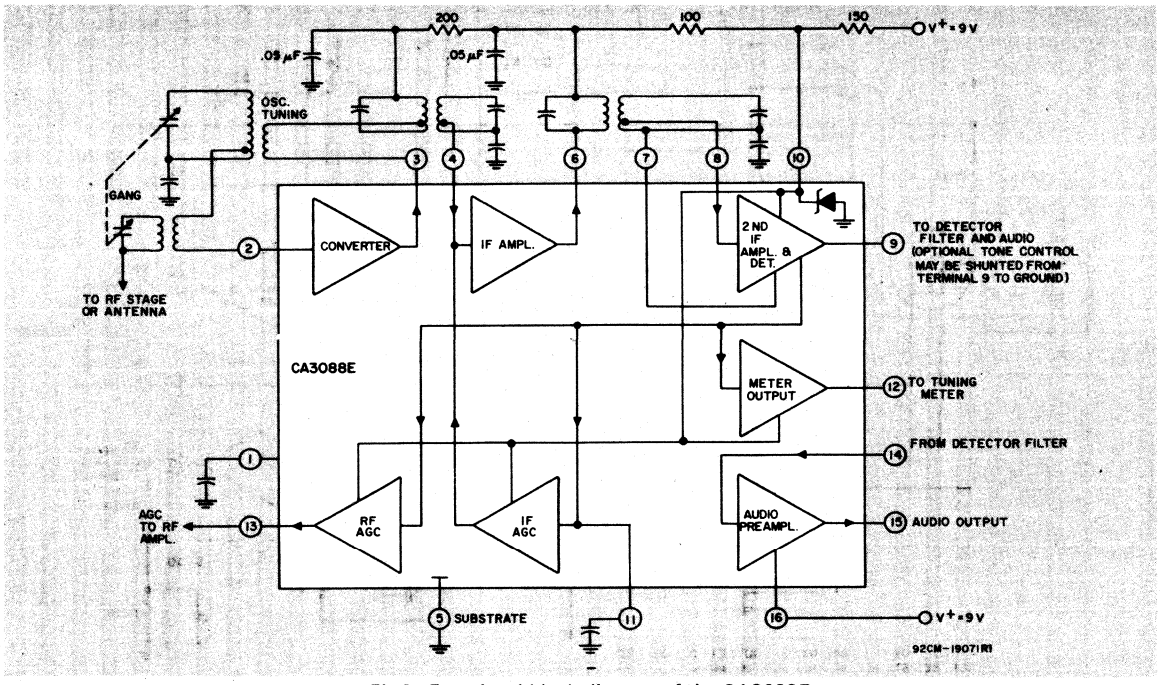


Fig.2—Functional block diagram of the CA3088E.

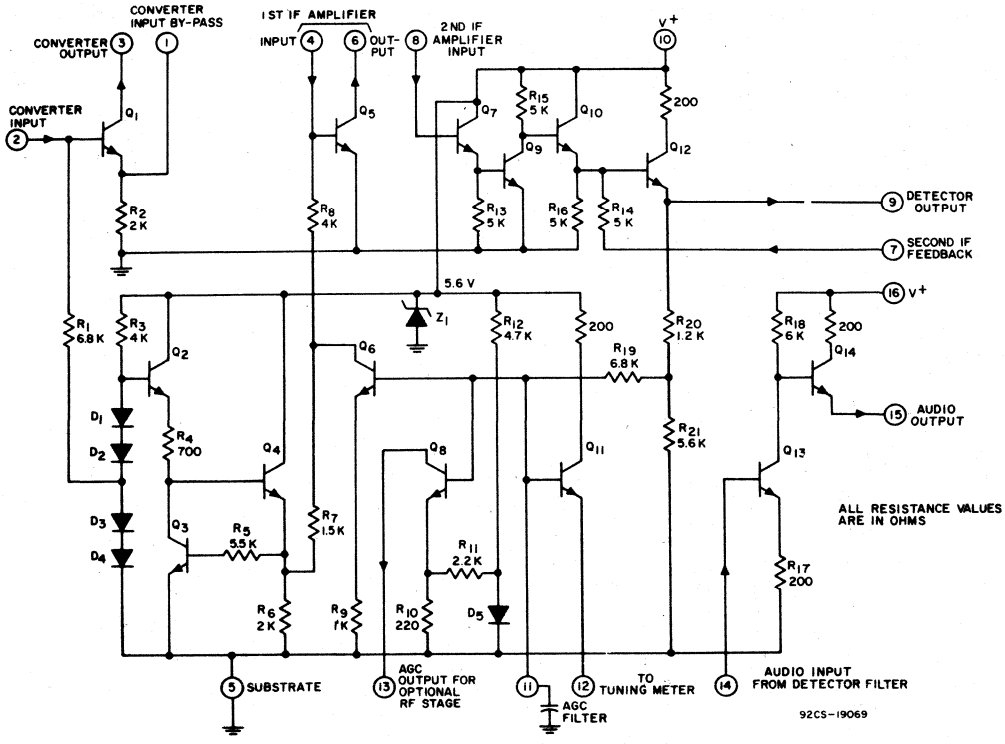


Fig.3—Schematic diagram of the CA3088E.

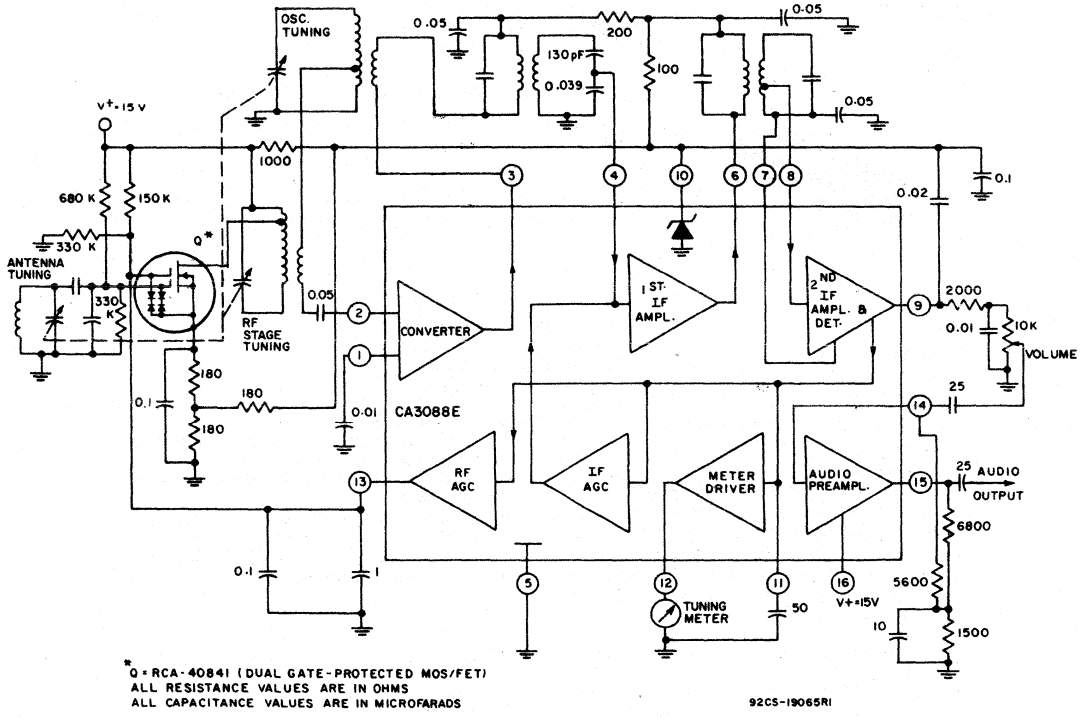
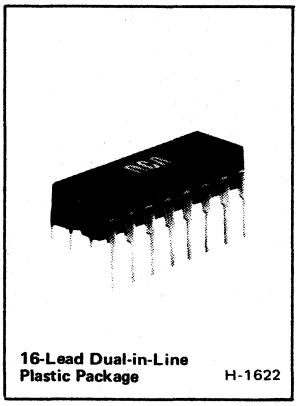


Fig.4—Typical AM broadcast receiver using the CA3088E with optional RF amplifier stage.

CA3089E



16-Lead Dual-in-Line Plastic Package H-1622

FM IF System

For FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers

Includes———IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Muting (Squelch), and Tuning Meter

Features:

- **Exceptional limiting sensitivity: 12 μV typ. at −3 dB point**
- **Low distortion: 0.1% typ. (with double-tuned coil)**
- **Single-coil tuning capability**
- **High recovered audio: 400 mV typ.**
- **Provides specific signal for control of inter-channel muting (squelch)**
- **Provides specific signal for direct drive of a tuning meter**
- **Provides delayed AGC voltage for RF amplifier**
- **Provides a specific circuit for flexible AFC**
- **Internal supply-voltage regulators**

RCA-CA3089E is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Fig. 1 is a block diagram showing the CA3089E features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as delayed AGC for the RF tuner, and AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5 to +16 volts.

The CA3089E is ideal for high-fidelity operation. Distortion in a CA3089E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089E utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of −40°C to +85°C.

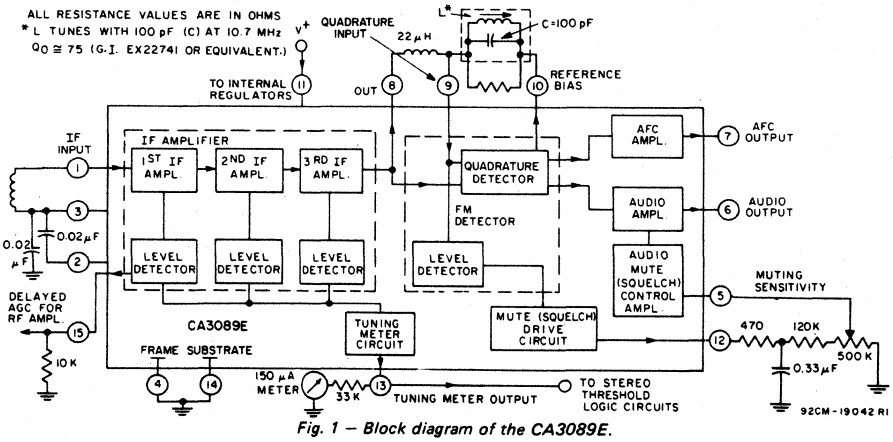


Fig. 1 – Block diagram of the CA3089E.

MAXIMUM RATINGS, *Absolute Maximum Values*

DC Supply Voltage:			
Between Terminals 11 and 4		16	V
Between Terminals 11 and 14		16	V
DC Current (out of Terminal 15)		2	mA
Device Dissipation:			
Up to $T_A = 60^\circ C$		600	mW
Above $T_A = 60^\circ C$	derate linearly	6.7	mW/°C
Ambient Temperature Range:			
Operating		−40 to + 85	°C
Storage		−65 to +150	°C
Lead Temperature (During Soldering):			
At distance not less than 1/32" (0.79mm) from case for 10 seconds max.		+265	°C

ELECTRICAL CHARACTERISTICS, at $T_A = 25^\circ C$, V+ = 12 Volts (See Figs. 5 and 6)

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
			Min.	Typ.	Max.	
Static (DC) Characteristics						
Quiescent Circuit Current	No signal input, Non muted		16	23	30	mA
DC Voltages:						
Terminal 1 (IF Input)			1.2	1.9	2.4	V
Terminal 2 (AC Return to Input)			1.2	1.9	2.4	V
Terminal 3 (DC Bias to Input)			1.2	1.9	2.4	V
Terminal 6 (Audio Output)			5.0	5.6	6.0	V
Terminal 10 (DC Reference)			5.0	5.6	6.0	V
Dynamic Characteristics						
Input Limiting Voltage (−3 dB point), V_1 (lim)	–	f_O = 10.7 MHz, $f_{mod.}$ = 400 Hz, Deviation = ±75 kHz	–	12	25	μV
AM Rejection (Term. 6), AMR	V_{IN} = 0.1V, AM Mod. = 30%		45	55	–	dB
Recovered AF Voltage (Term. 6) V_O (AF)	V_{IN} = 0.1 V		300	400	500	mV
Total Harmonic Distortion, THD:*						
Single Tuned (Term. 6)			–	0.5	1.0	%
Double Tuned (Term. 6)			–	0.1	–	%
Signal plus Noise to Noise Ratio (Term. 6)			60	67	–	dB

*THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8,9, and 10.

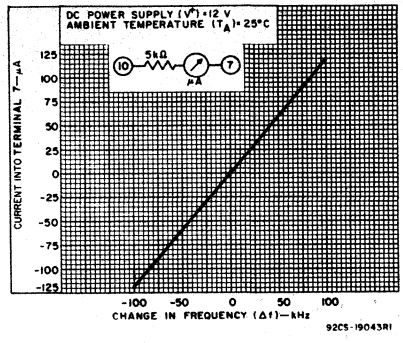


Fig. 2 — AFC characteristics (current at Term.7) as a function of change in frequency. (See test circuit Fig. 5.)

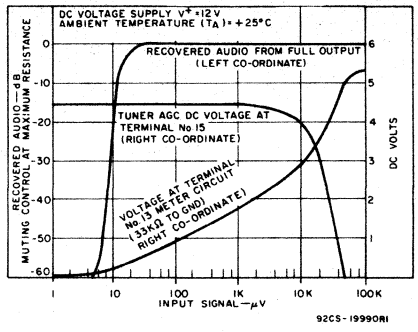


Fig. 3 — Muting action, tuner AGC, and tuning meter output as a function of input signal voltage. (See test circuit Fig.5.)

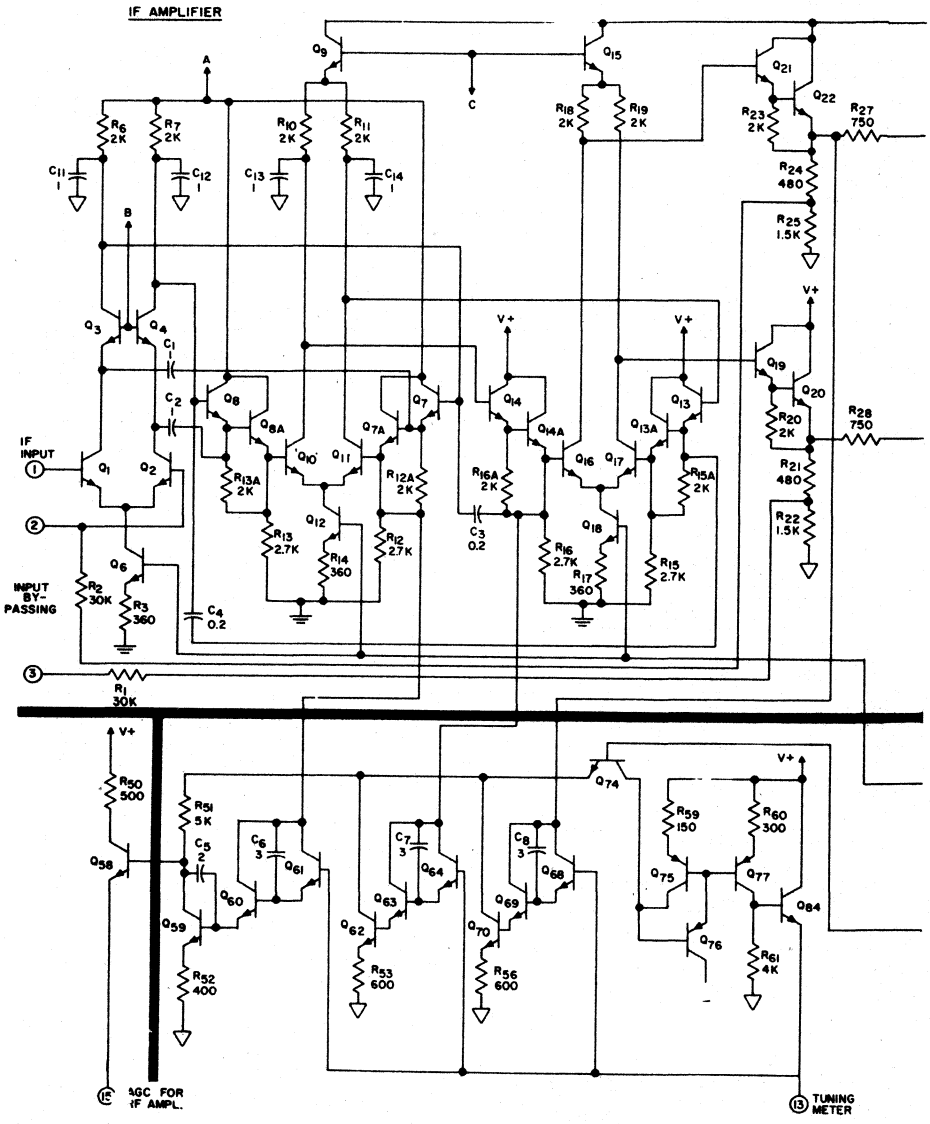


Fig. 4 – Schematic diagram of the CA3089E (cont'd on next page).

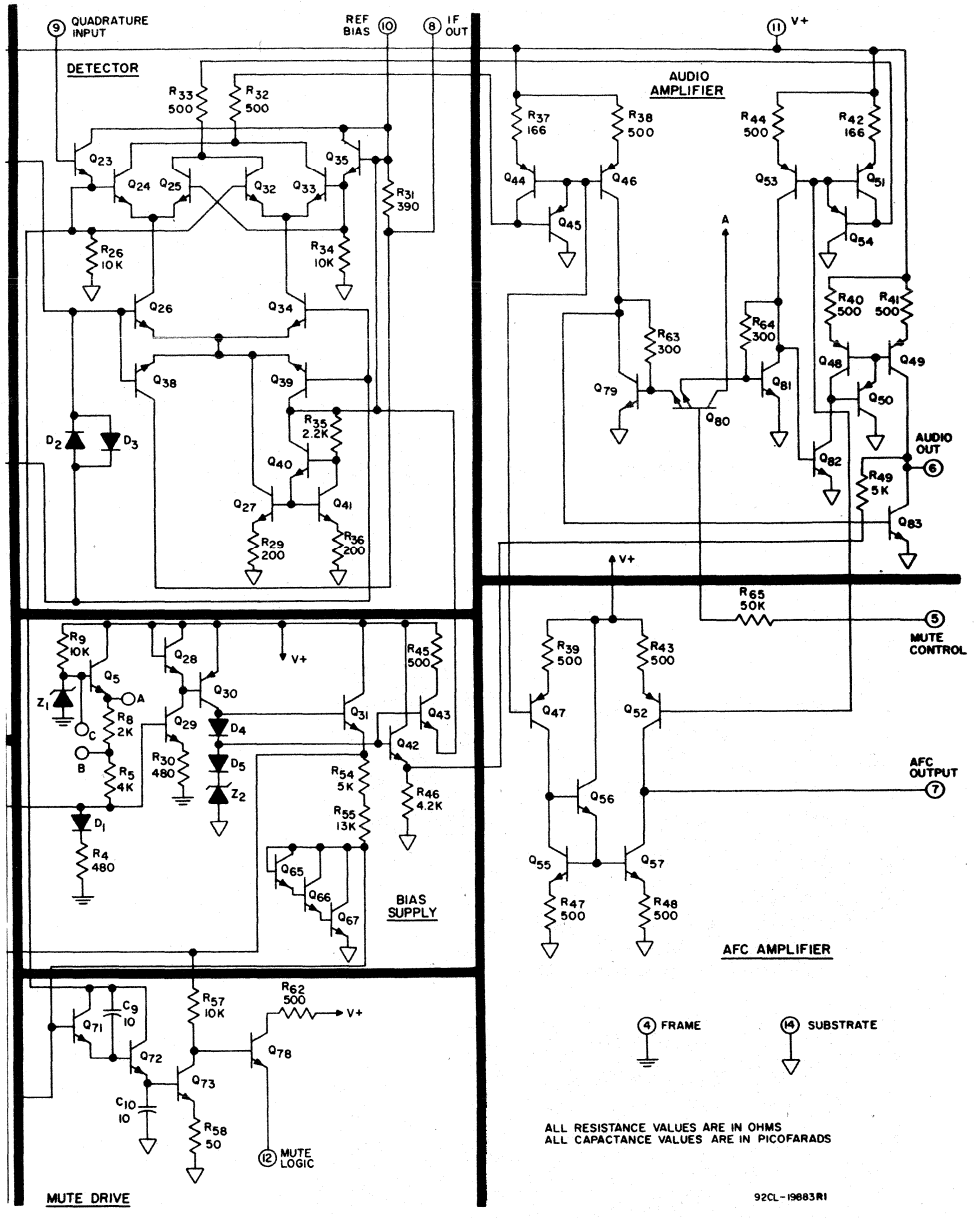
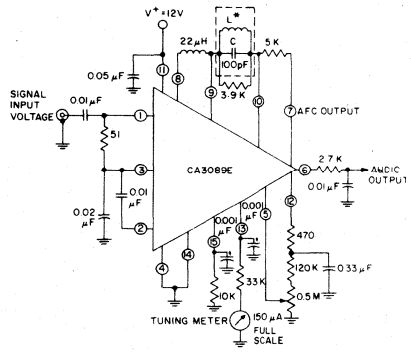


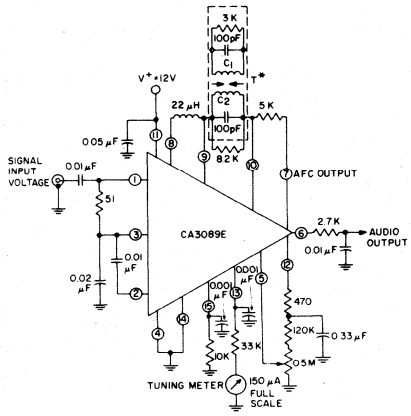
Fig. 4 - Schematic diagram of the CA3089E (cont'd from previous page).



ALL RESISTANCE VALUES ARE IN OHMS
*L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_0(UNLOADED) ≅ 75 (G.I. AUTOMATIC MFG. DIV. EX22741 OR EQUIVALENT)

92CM-19043-1

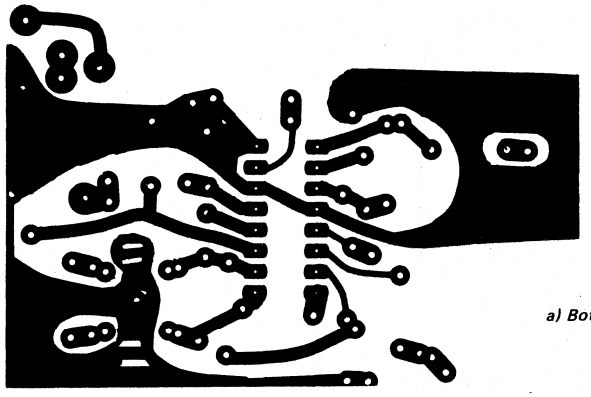
Fig. 5 — Test circuit for CA3089E using a single-tuned detector coil.



ALL RESISTANCE VALUES ARE IN OHMS
* T PRI. - Q_0(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C1) 20 t OF 34e ON 7/32" DIA FORM
SEC. - Q_0(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C2) 20 t OF 34e ON 7/32" DIA FORM
kQ (PER CENT OF CRITICAL COUPLING) ≅ 70%
(ADJUSTED FOR COIL VOLTAGE V_C) = 150 mV
ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT
"E" TYPE SLUGS, SPACING 4 mm

92CM-19044-1

Fig. 6 — Test circuit for CA3089E using a double-tuned detector coil.

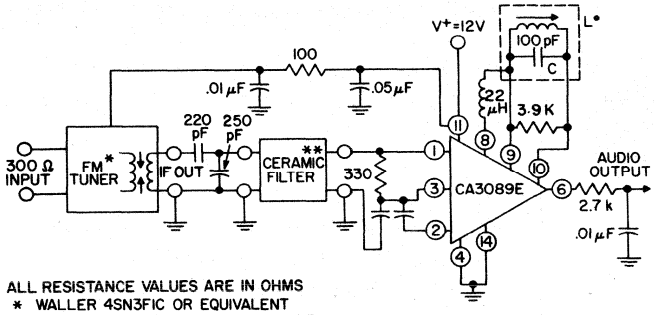


a) Bottom view of printed-circuit board.

b) Component side — top view.

92CS-30376

Fig. 7 - Actual size photographs of the CA3089E and outboard components mounted on a printed-circuit board.



ALL RESISTANCE VALUES ARE IN OHMS
* WALLER 4SN3FIC OR EQUIVALENT
** MURATA SFG 10.7 MA OR EQUIVALENT
• L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_O UNLOADED ≠75 (G.I EX22741 OR EQUIVALENT)

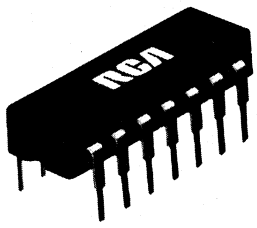
92CS-19045

Performance data at f_o = 98 MHz, f_{MOD} = 400 Hz, Deviation = ±75 kHz:

-3dB Limiting Sensitivity	2μV (Antenna Level)
20dB Quieting Sensitivity	1μV (Antenna Level)
30dB Quieting Sensitivity	1.5μV (Antenna Level)

Fig. 8 – Typical FM tuner using the CA3089E with a single-tuned detector coil.

CA3123E



14-Lead Dual-in-Line Plastic Package

H-1517

AM Radio Receiver Subsystem

Includes RF Amplifier, IF Amplifier, Mixer, Oscillator, AGC Detector, and Voltage Regulator

Features:

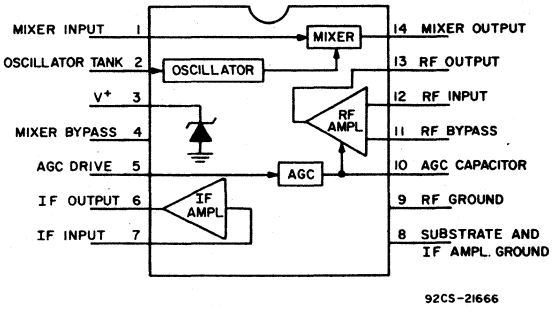
- **Low-noise, low-R_b' rf stage in cascode connection — eliminates Miller-Effect regeneration and allows controlled power rise by the choice of external components**
- **Mixer-oscillator stage with internal feedback — eliminates need for tapped or multi-winding oscillator coils**
- **Cascode if amplifier with controlled output impedance and negligible Miller Effect — eliminates regeneration and selectivity skewing**
- **Frequency-counter AGC circuit — allows control of AGC response by selection of the coupling capacitor**
- **Integral regulation with built-in surge protection**
- **Separately accessible amplifiers**

The CA3123E* is a monolithic silicon integrated circuit that provides an rf amplifier, if amplifier, mixer, oscillator, AGC detector, and voltage regulator on a single chip. It is intended for use in super-heterodyne AM radio receiver applications particularly in automobiles. The CA3123E is supplied in a 14-lead dual-in-line plastic package and operates over the temperature range of −55° to 125°C.

* Formerly RCA Dev. No. TA6155

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:	
At Terminal No. 3 (V^+)	9 V
At Terminal No. 6 (IF Output)	40 V
At Terminal No. 13 (RF Output)	20 V
At Terminal No. 14 (Mixer Output)	20 V
DC CURRENT:	
Into Terminal No. 3 (V^+)	35 mA
DEVICE DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16" ± 1/3" (1.59 mm ± 0.79 mm) from case for 10 s max.	265°C



Terminal assignment diagram.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Static Characteristics In Circuit of Fig. 3						
DC Voltage:						
At Terminals 1, 4	V_1, V_4			4.7		V
At Terminals 2, 3, 14	V_2, V_3, V_{14}			6.8		V
At Terminal 5	V_5			0.25		V
At Terminal 6	V_6			12		V
At Terminal 7	V_7			0.76		V
At Terminals 8, 9	V_8, V_9			0		V
At Terminals 10, 11	V_{10}, V_{11}			0.71		V
At Terminal 12	V_{12}			0.71		V
At Terminal 13	V_{13}			4.0		V
DC Current:						
Into Terminals 1, 4, 5, 7 8, 9, 10, 11, 12	$I_1, I_4, I_5, I_7, I_8, I_9, I_{10}, I_{11}, I_{12}$			0		mA
Into Terminal 2	I_2			1.2		mA
Into Terminal 3	I_3			15		mA
Into Terminal 6	I_6			4.3		mA
Into Terminal 13	I_{13}			4.5		mA
Into Terminal 14	I_{14}			0.170		mA
Performance Characteristics In Circuit of Fig. 3						
Sensitivity		Input Signal to Dummy Antenna at f_{IN}=1 MHz, 30% AM Modulation at f_{MOD}=400 Hz, for 11 mV output at V_O	–	2.3	5	μV
Signal-to-Noise Ratio	S/N	Ratio of Output at V_O with Modulation ON and then OFF, Input Signal=100 μV, 30% AM Modulation at f_{MOD}=400 Hz	34	43	–	dB
Overload Distortion		Input Signal set at 1 MHz, 90% AM Modulation, Distortion at V_O must be $\leq$ 10%	160000	400000	–	μV

Dynamic Characteristics For Indicated Stages In Circuit of Fig. 3

Stage	Parallel Capacitance		Parallel Resistance		Transconductance
	Input pF	Output pF	Input Ω	Output Ω	μmhos
RF Amplifier	80	6	750	2 x 10^6 min.	140000
IF Amplifier	35	3.5	950	10^4	80000
Mixer	6	2	2000	2 x 10^6 min.	2500 (Mixer) 3000 (Amplifier)

CA3123E

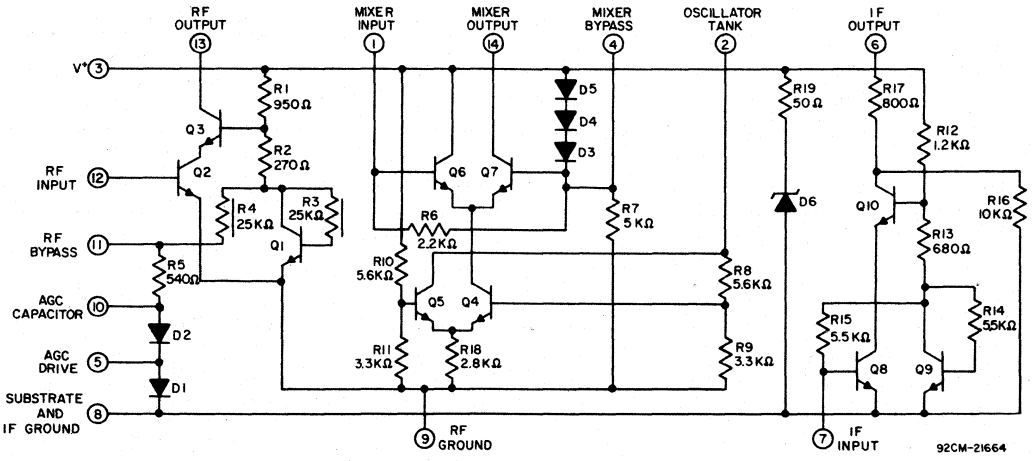
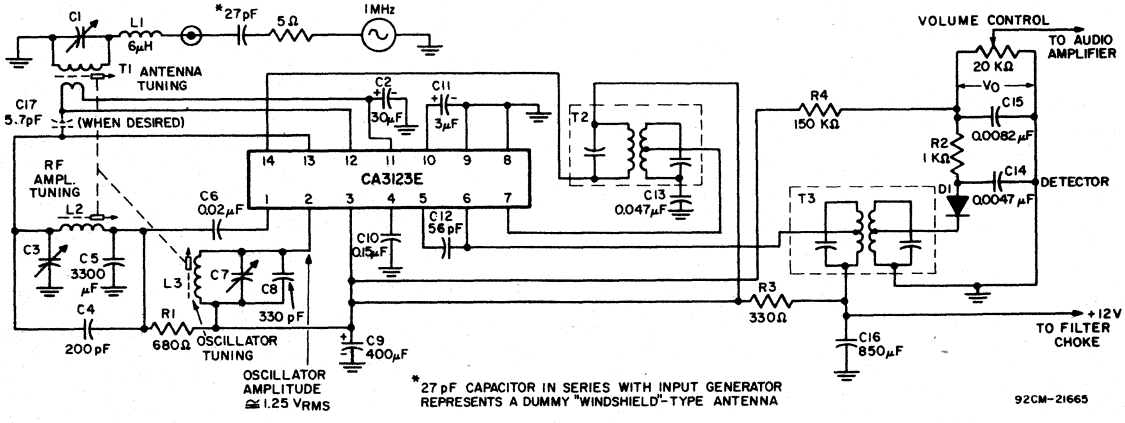


Fig. 2– Schematic diagram of CA3123E.



Transformer	Symbol	Frequency	Inductance μh (≈)	Capacitance pF (≈)	Q (≈)	Total Turns To Tap Turns Ratio	Coupling
First IF: Primary	T_2	262 kHz	2840	130	60	none	critical ≈0.017 ≈1/Q
Secondary			2840	130	60	or 30:1 31:1	
Second IF: Primary	T_3	262 kHz	2840	130	60	8.5:1	– critical ≈0.017 ≈1/Q
Secondary			2840	130	60	8.5:1	
Antenna: Primary	T_1	1 MHz	195	$(C_1)-130$	65		
Secondary		Adjusted to an impedance of 75 Ω with primary resonant at 1 MHz. Coupling should be as tight as practical. Wire should be would around end of coil away from tuning core.					
Coils	L_1	7.9 MHz	6		50		
	L_2	1 MHz	55		50		
	L_3	1.262 MHz	41		40		

Fig. 3– Schematic diagram of AM radio receiver using CA3123E.

TYPICAL CHARACTERISTICS

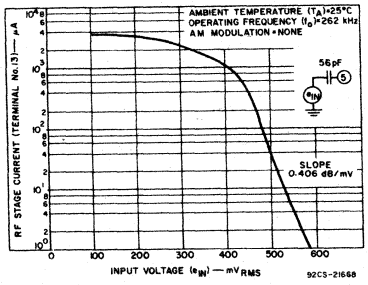


Fig. 4— Control of RF stage by signal into Terminal No. 5.

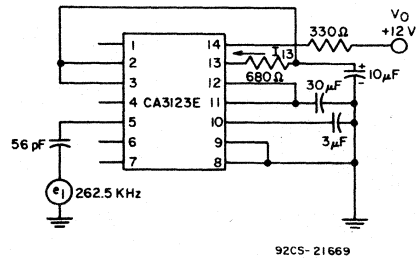


Fig. 5— Test circuit for Fig. 4.

PERFORMANCE CHARACTERISTICS IN CIRCUIT OF FIG. 3

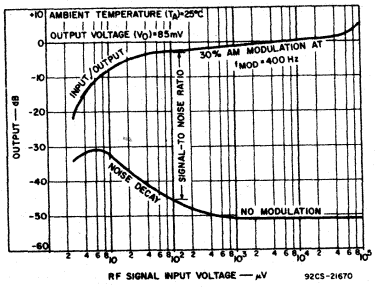


Fig. 6— Signal-to-noise performance.

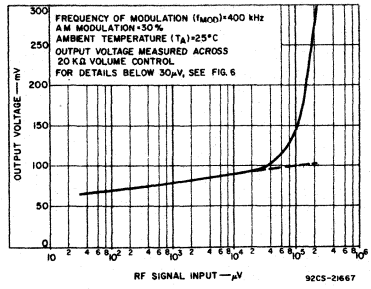


Fig. 7— AGC curve showing voltage rise (controlled by external capacitance of 5.7 pF: C_{17}, Fig. 3).

Change in slope in the vicinity of 40000 μV signal input voltage is the result of the use of C_{17} (5.7 pF) in Fig. 3. The dotted curve indicates expected performance if C_{17} = 0.

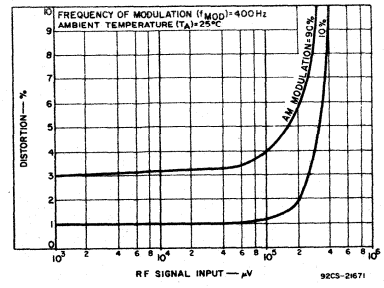
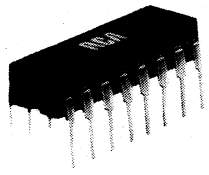


Fig. 8— Overload response.

CA3189E



16-Lead Dual-In-Line Plastic Package (E)

H-1622

FM IF System

Includes IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Tuning Meter, Deviation-Noise Muting, and ON Channel Detector

For FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers

Features:

- *Exceptional limiting sensitivity: 12μV typ. at −3 dB point*
- *Low distortion: 0.1% typ. (with double-tuned coil)*
- *Single-coil tuning capability*
- *Improved S + N/N Ratio*
- *Externally programmable recovered audio level*
- *Provides specific signal for control of interchannel muting (squelch)*
- *Provides specific signal for direct drive of a tuning meter*
- *On channel step for search control*
- *Provides programmable AGC voltage for RF amplifier*
- *Provides a specific circuit for flexible audio output*
- *Internal supply-voltage regulators*
- *Externally programmable "on" channel step width, and deviation at which muting occurs*

The RCA-CA3189E* is a monolithic intergrated circuit that provides all the functions of a comprehensive FM-IF system. Fig. 1 shows a block diagram of the CA3189E, which includes a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as programmable delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power-supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5 to +16 volts.

The CA3189E is ideal for high-fidelity operation. Distortion in a CA3189E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3189E has all the features of the CA3089E plus additions. See CA3189E features compared to the CA3089E in Table I.

The CA3189E utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of −40° C to +85° C.

*Formerly Developmental Type No. TA10038.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C:*

DC SUPPLY VOLTAGE (between Terms. 11 and 4) ..... 16 V

(between Terms. 11 and 14) ..... 16 V

DC CURRENT (Out of Term. 15) ..... 2 mA

DEVICE DISSIPATION:

Up to T_A = 85° C ..... 640 mW

Above T_A = 85° C ..... derate linearly at 9.9 mW/° C

AMBIENT TEMPERATURE RANGE:

Operating ..... −40 to +85° C

Storage ..... −65 to +150° C

LEAD TEMPERATURE (During soldering):

At distance not less than 1/32 inch (0.79 mm) from case for 10s max. ..... +265° C

ELECTRICAL CHARACTERISTICS, at $T_A = 25^oC$, $V^+ = 12$ Volts

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS			UNITS
				Circuit or Fig. No.	Min.	Typ.	Max.	
Static (DC) Characteristics								
Quiescent Circuit Current	I_{11}	No signal input, Non muted		3,4	20	31	40	mA
DC Voltages: Terminal 1 (IF Input)	V_1				1.2	1.9	2.4	V
Terminal 2 (AC Return to Input)	V_2				1.2	1.9	2.4	V
Terminal 3 (DC Bias to Input)	V_3				1.2	1.9	2.4	V
Terminal 15 (RF AGC)	V_{15}				7.5	9.5	11	V
Terminal 10 (DC Reference)	V_{10}				5	5.6	6	V
Dynamic Characteristics								
Input Limiting Voltage (−3 dB point)	V_I(lim)				–	12	25	μV
AM Rejection (Term. 6)	AMR	V_{IN} = 0.1 V, AM Mod. = 30%	f_O = 10.7 MHz,	3,4	45	55	–	dB
Recovered AF Voltage (Term. 6)	V_O(AF)				325	500	650	mV
Total Harmonic Distortion:* Single Tuned (Term. 6)	THD	V_{IN} = 0.1 V	$f_{mod.}$ = 400 Hz,	3	–	0.5	1	%
Double Tuned (Term. 6)	THD		Deviation ±75 kHz	4	–	0.1	–	%
Signal plus Noise to Noise Ratio (Term. 6)	S + N/N			3,4	65	72	–	dB
Deviation Mute Frequency	$f_{DEV.}$		$f_{mod.}$ = 0	3,6,7	–	±40	–	kHz
RF AGC Threshold	V_{16}			3,4	–	1.25	–	V
On Channel Step	V_{12}	V_{IN} = 0.1 V	$f_{DEV.}$ < ±40 kHz	3	–	0	–	V
			$f_{DEV.}$ > ±40 kHz		–	5.6	–	

*THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.

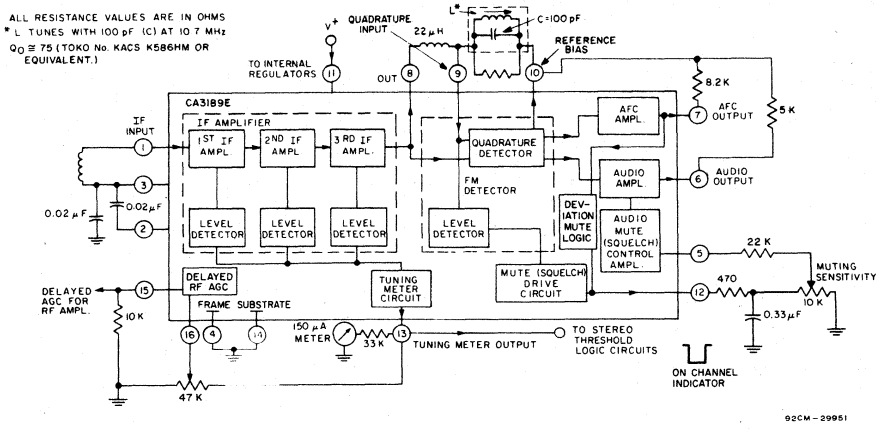


Fig. 1 – Block diagram of the CA3189E.

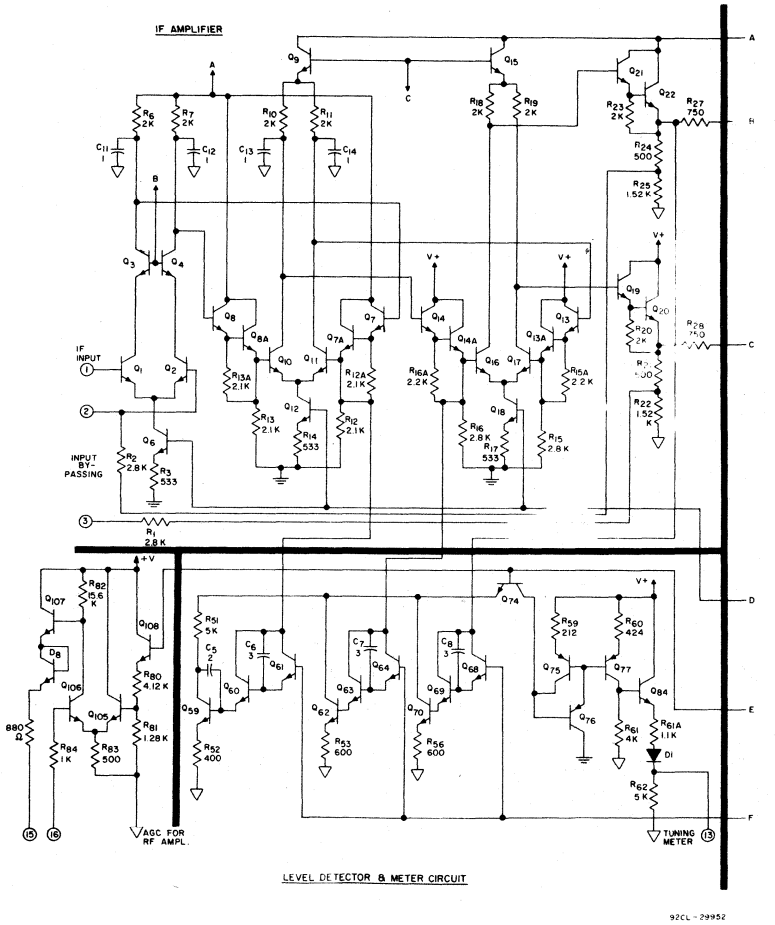


Fig. 2 – Schematic diagram of the CA3189E (cont'd on next page).

TABLE I – CA3189E Features Compared to CA3089E

FEATURES	CA3189E	CA3089E
Low Limiting Sensitivity (12 μV typ.)	Yes	Yes
Low Distortion	Yes	Yes
Single-coil Tuning Capability	Yes	Yes
Programmable Audio Level	Yes	No
S/N Mute	Yes	Yes
Deviation Mute	Yes	No
Flexible AFC	Yes	Yes
Programmable AGC Threshold and Voltage	Yes	No
Typical S + N/N > 70 dB	Yes	No
Meter Drive Voltage Depressed at Very-Low Signal Levels	Yes	No
On-Channel Step Control Voltage	Yes	No

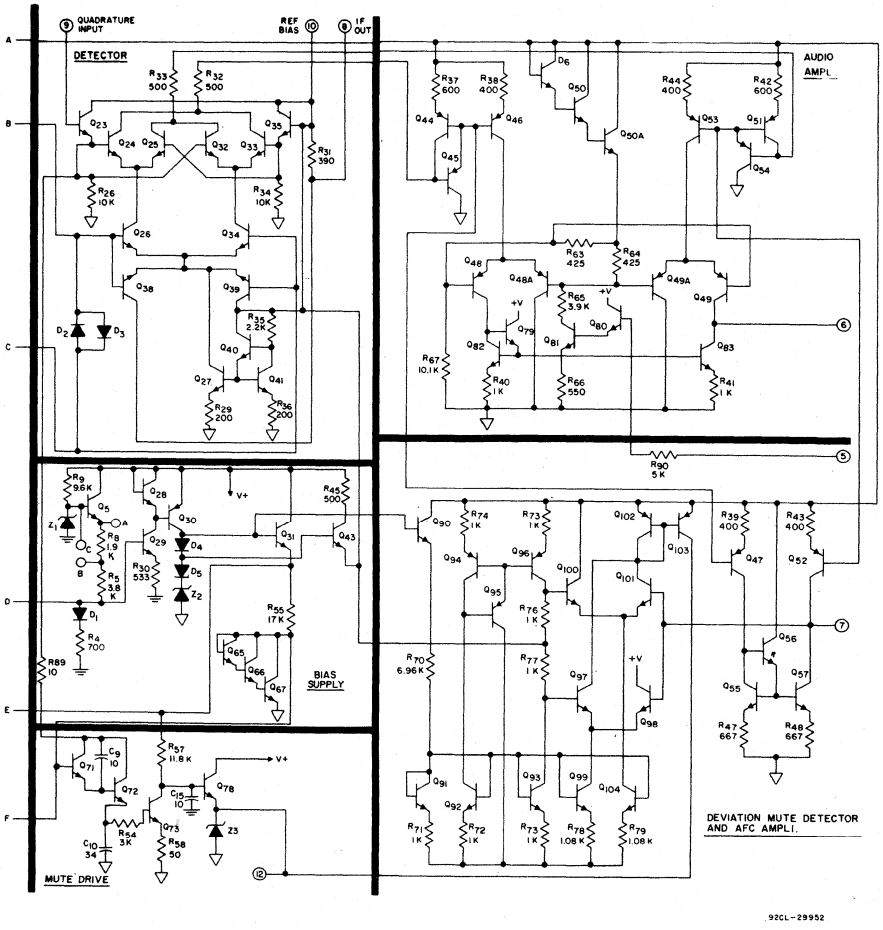
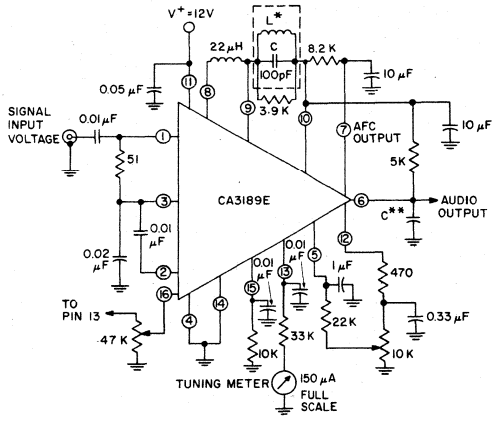


Fig. 2 - Schematic diagram of the CA3189E (cont'd from previous page).

CA3189E



ALL RESISTANCE VALUES ARE IN OHMS
*L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_0(UNLOADED)≅75 (TOKO No. KACS K586HM OR EQUIVALENT)
**C=0.01 μF FOR 50 μs DEEMPHASIS (EUROPE)
=0.015 μF FOR 75 μs DEEMPHASIS (USA)

92CM-29953

Fig. 3 – Test circuit for CA3189E using a single-tuned detector coil.

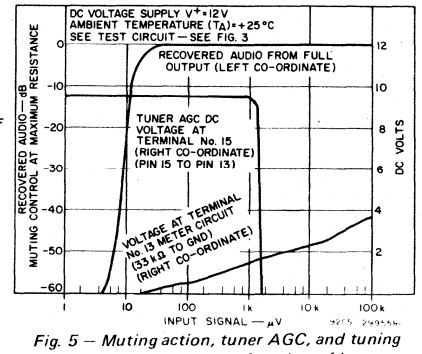


Fig. 5 – Muting action, tuner AGC, and tuning meter output as a function of input signal voltage.

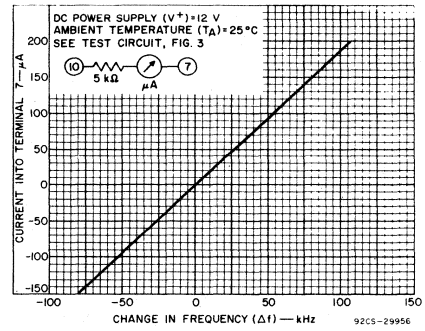
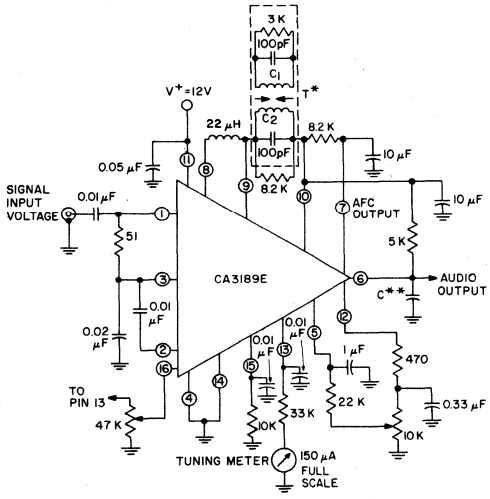


Fig. 6 – AFC characteristics (current at Term. 7 as a function of change in frequency).



ALL RESISTANCE VALUES ARE IN OHMS
*T: PRI.–Q_0(UNLOADED)≅75 (TUNES WITH 100 pF (C1) 20t OF 34e ON 7/32" DIA. FORM
SEC.–Q_0(UNLOADED)≅75 (TUNES WITH 100 pF (C2) 20t OF 34e ON 7/32" DIA. FORM
kQ (PER CENT OF CRITICAL COUPLING)≅70%
(ADJUSTED FOR COIL VOLTAGE V_C)=150 mV
ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT
"E" TYPE SLUGS, SPACING 4 mm
**C=0.01 μF FOR 50 μs DEEMPHASIS (EUROPE)
=0.015 μF FOR 75 μs DEEMPHASIS (USA)

Fig. 4 – Test circuit for CA3189E using a double-tuned detector coil.

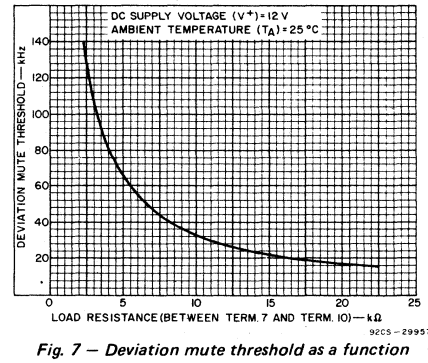


Fig. 7 – Deviation mute threshold as a function of load resistance (between Term. 7 and Term. 10).

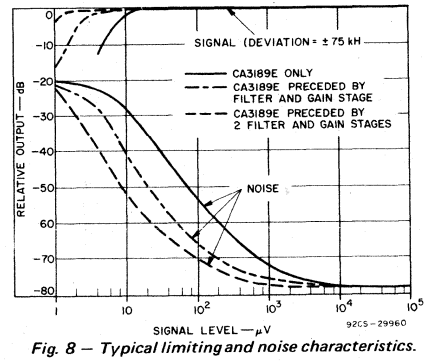


Fig. 8 – Typical limiting and noise characteristics.

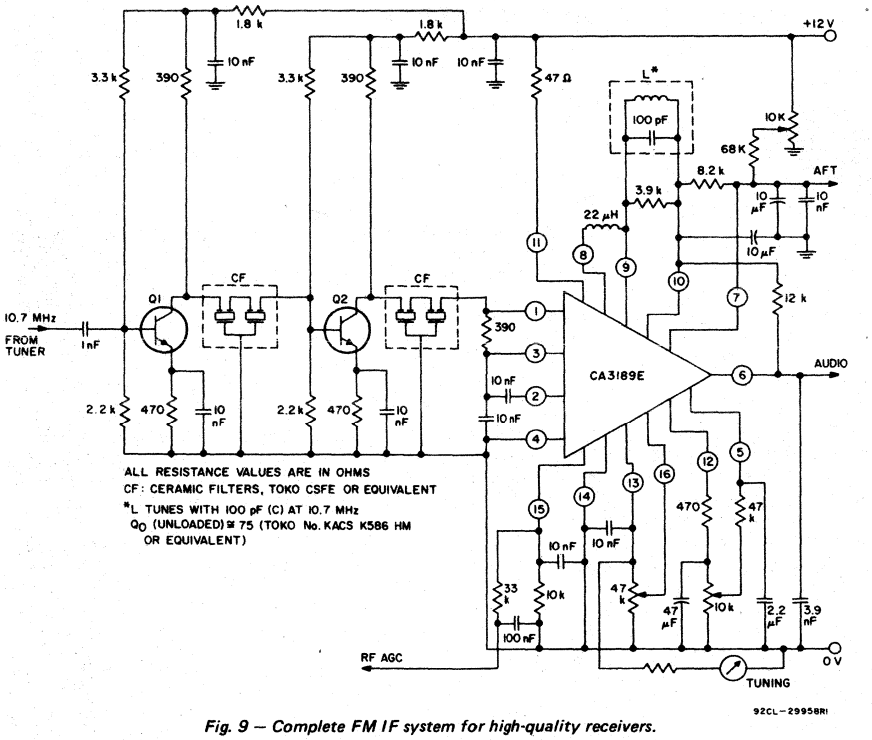
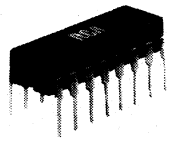


Fig. 9 — Complete FM IF system for high-quality receivers.

CA3209E



16-Lead Dual-In-Line Plastic Package

H-1622

FM-IF System

For Search and Scan

Features:

- *Exceptional limiting sensitivity: 12 μV typ. at -3 dB point*
- *Exceptional temperature stability of tuning and stop-pulse window*
- *Single-coil tuning capability*
- *Externally programmable stop-pulse window width*
- *Programmable level for AGC action*
- *Forward AGC for pin-diode or bipolar rf amplifier*
- *Required input level to generate a stop-pulse is programmable*

The RCA CA3209E• is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. It is intended for use in FM—IF amplifier applications in high-fidelity, automotive, and communications receivers where the synthesizer counter can be controlled by a stop-pulse for scan and search operation.

•Formerly Developmental Type No. TA10493B

Fig. 1 shows the CA3209E features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier.

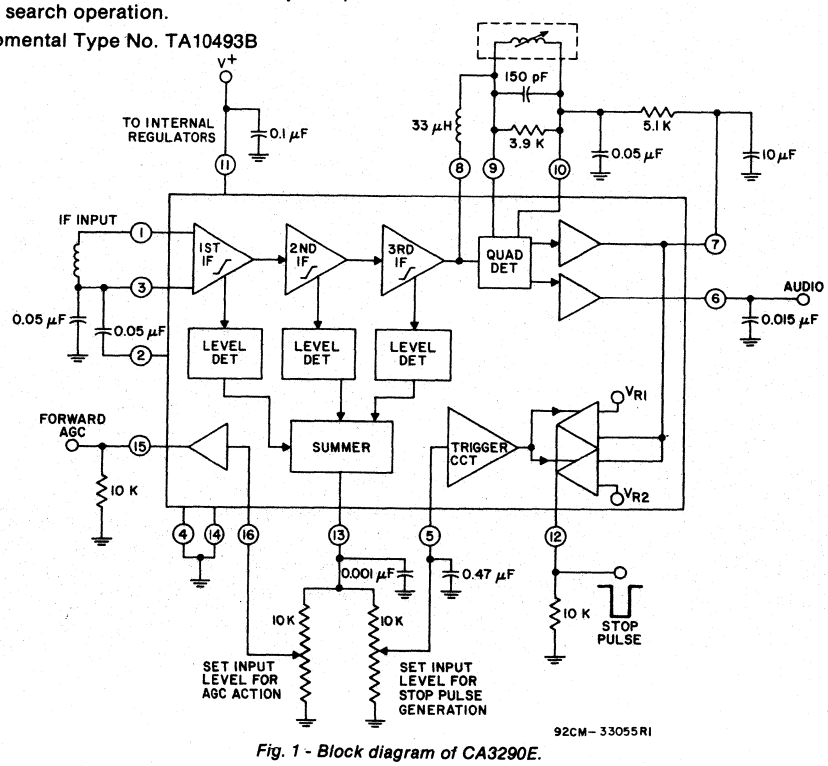


Fig. 1 - Block diagram of CA3290E.

CA3209E

The advanced circuit design of the if system includes desirable deluxe features such as delayed AGC for the rf tuner, and an output signal to drive a tuning meter and/or provide stereo switching logic control of stop pulse and AGC thyristors. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5 to +16 volts.

The CA3209E is ideal for high-fidelity operation. Distortion in a CA3209E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3209E utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of -40° C to +85° C.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
- Between terminals 11 and 4 ..... 16 V
- Between terminals 11 and 14 ..... 16 V

DC CURRENT (Out of Terminal 15) ..... 2 mA

DEVICE DISSIPATION:
- Up to T_A = 85° C ..... 735 mW
- Above T_A = 85° C ..... Derate linearly 11.4 mW/° C

AMBIENT TEMPERATURE RANGE:
- Operating ..... -40 to +85° C
- Storage ..... -65 to +150° C

LEAD TEMPERATURE (During Soldering):
- At distance not less than 1/32" (0.79 mm) from case for 10 seconds max. ..... +265° C

ELECTRICAL CHARACTERISTICS at T_A = 25° C, V+ = 12 Volts
(See Fig. 3 for Test Circuit)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Static (DC) Characteristics					
Quiescent Circuit Current		20	31	44	mA
DC Voltages:					
V_1, V_2, V_3		1.2	1.9	2.4	V
V_{10}		4.9	5.6	6.1	V
V_{15}	V_{16} = 0 V	—	0.005	0.4	V
V_{15}	V_{16} = 1.4 V	4.1	5.1	5.6	V
V_{16}	V_{15} = 1-2 V	—	1.22	—	V
V_{12}	$V_5 \leqq$ 0.24 V	4.3	5.7	6.6	V
V_{12}	$V_5 \geqq$ 0.53 V	—	0.06	0.4	V
V_5 to cause transition of trigger (V_{12}) high to low		—	0.45	—	V
V_5 to cause transition of trigger (V_{12}) low to high		—	0.40	—	V
Dynamic Characteristics					
Input Limiting Voltage (-3 dB point)		—	12	25	μV
Recovered Audio Voltage	400 Hz Input ≧ 1 mV ±75 kHz Deviation	350	520	700	mV
Frequency Window of Stop Pulse V_5 = 0.6 V Input = 100 μV	R_7 -10 = 5.1 K	70	120	200	kHz
	R_7 -10 = 8.2 K	45	75	125	
Total Harmonic Distortion, THD: *			0.50	1.0	%
AM Rejection	30% AM 100 mV Input	50	65	—	dB
	100 μV Input	35	42	—	
S/N Ratio **	100 mV Input	70	80	—	dB
	100 μV Input	55	65	—	
V_{13}	No Signal	0	0.2	0.8	V
	100 μV Input	1.4	2.2	3.2	
	100 mV Input	4.9	6.5	8.5	

* THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.

** Measured with a 30-kHz low-pass filter (-3 dB at 30 kHz, 18 dB/octave).

CA3209E

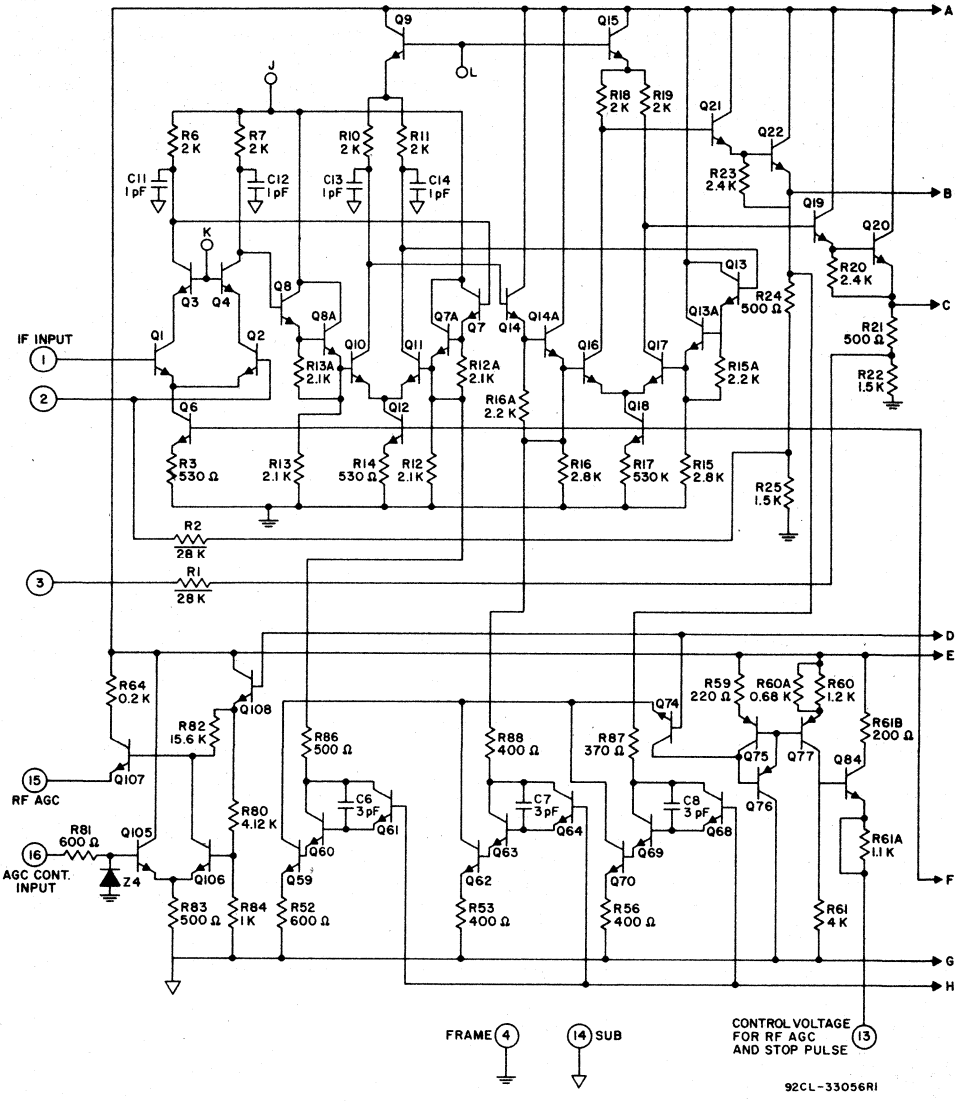


Fig. 2 - Schematic diagram of CA3209E
(continued on next page).

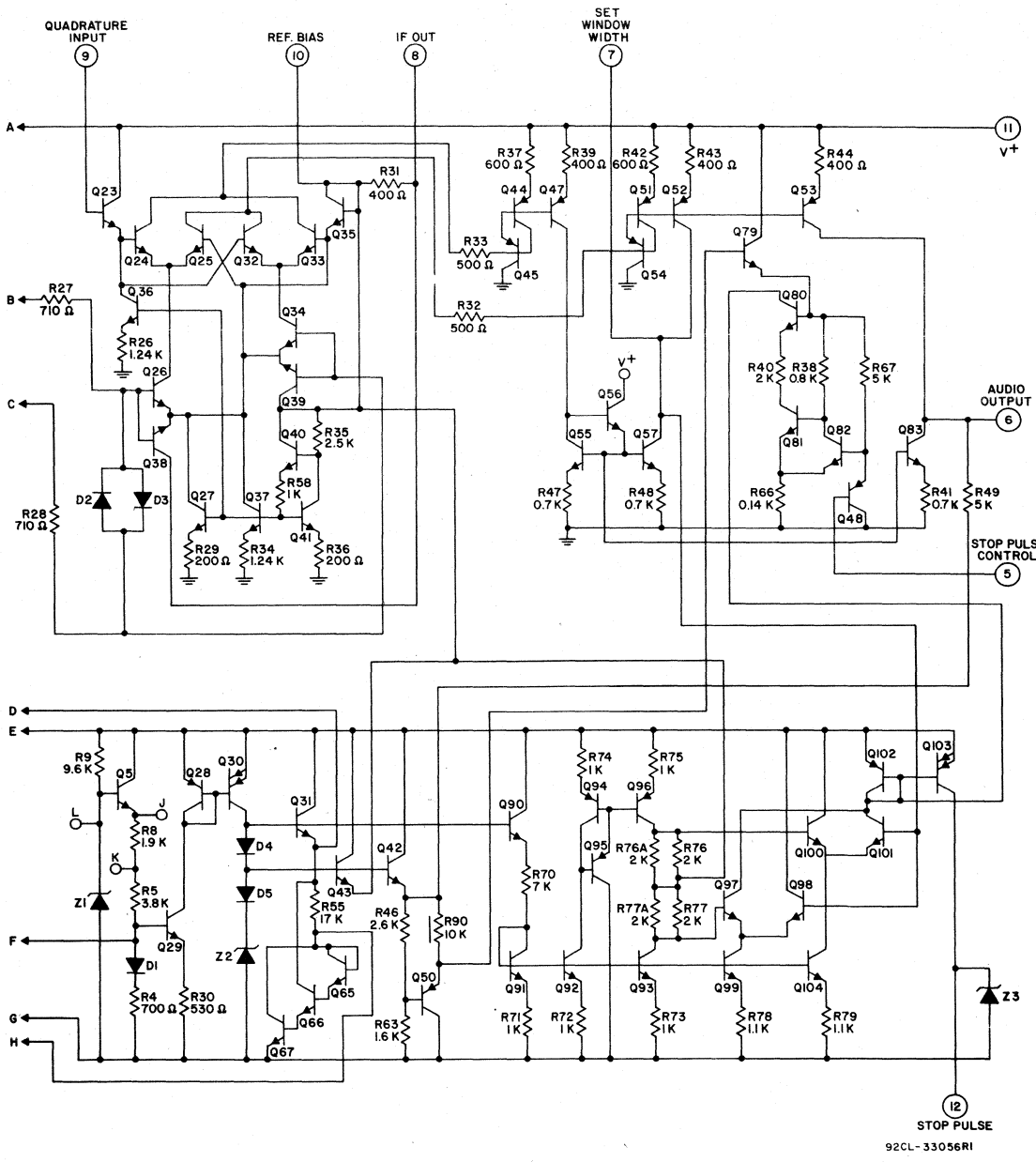


Fig. 2 - Schematic diagram of CA3209E (continued from previous page).

CA3209E

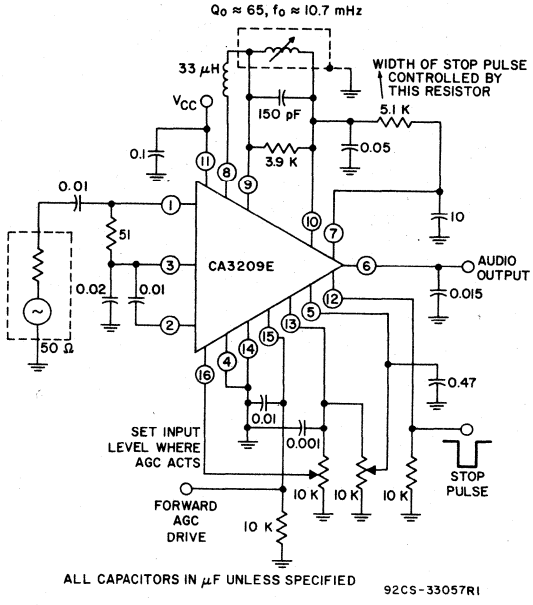


Fig. 3 - Test circuit.

MOS/FET Devices
Technical Data

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFET Story

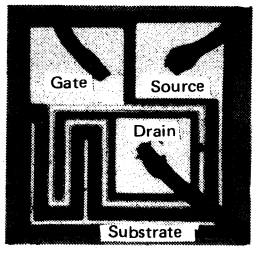
RCA MOS insulated-gate field-effect transistors are N-channel, depletion-type silicon devices, and are available in both single-gate and dual-gate types. Both types offer the advantages of extremely high input resistance, low input capacitance, very low feedback capacitance, high forward transconductance, and low noise at very high frequencies. Because of their insulated-gate construction, these devices have extremely low leakage currents which are relatively insensitive to temperature variations. In addition, their drain currents have a negative temperature coefficient which makes "thermal runaway" virtually impossible.

The extremely high input resistance of RCA MOS transistors permits the use of simple biasing techniques. It also makes these devices capable of handling relatively large positive and negative input-signal excursions without degradation of input impedance due to diode-current loading. Because of this capability, MOS transistors have considerably greater dynamic ranges than junction-type field-effect transistors and bipolar transistors of comparable ratings, and can provide superior performance in amplifier circuits utilizing automatic gain control. Furthermore, the extremely high input resistances of these devices impose virtually no loading on AGC voltage sources.

In addition to the features described above, RCA MOS transistors are notably superior to other solid-state devices in cross-modulation characteristics, and in their relative freedom from spurious responses. These transistors are also characterized by zero offset voltage—a feature which makes them especially desirable for chopper applications.

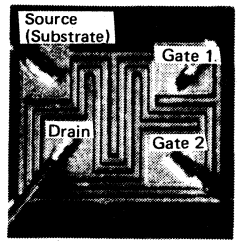
Applications

RCA Single-Gate MOS Transistors provide outstanding performance in applications requiring extremely high input impedance. They are also capable of providing high power gains at frequencies up to approximately 250 MHz. Typical applications for these devices include



rf-amplifier, mixer, and oscillator service in mobile and fixed communications equipment and in home entertainment equipment, and as audio and wide-band amplifiers, variable attentuators, choppers, and current limiters in industrial instrumentation and control equipment. *RCA single-gate MOS transistors also feature a separate terminal permitting connection to the bulk (substrate).*

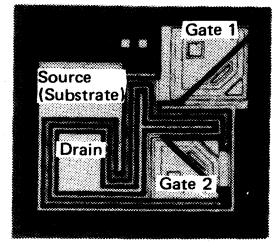
RCA Dual-Gate MOS Transistors feature a series arrangement of two separate channels, each channel having an independent control gate. This arrangement results in substantially lower feedback capacitance, greater gain, remote AGC capability in rf-amplifier applications, substantially better cross-modulation characteristics and lower spurious response than are provided by single-gate types. The availability of two independent control gates also offers unique advantages for chopper, clipper, and gated-amplifier service, and for applications involving the combination of two or



more signals, such as mixers, product detectors, color demodulators, and balanced modulators.

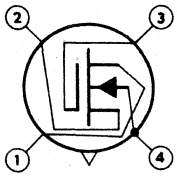
RCA Dual-Gate-Protected RF MOS Transistors incorporate back-to-back diodes for each gate within the same silicon MOSFET pellet. The major technical challenge in the development of these new MOSFETs was that gate protection must not significantly degrade the RF performance. Special back-to-back diodes were developed as the answer to this objective.

The back-to-back diodes are diffused directly into the MOS pellet and are electronically connected between each insulated gate and the FET's source; this arrangement permits the device to handle a wide dynamic signal swing and still provide excellent RF performance. The low junction capacitance of the diodes adds little to the total capacitance shunting the gate. Furthermore, the resistive components of these diodes are such that they do not materially affect the overall noise performance of the unit.

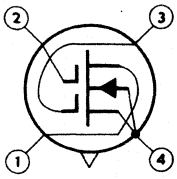


The net result is a MOSFET which protects against static discharge during handling operations without the need for external shorting mechanisms, protects against in-circuit transients, and is more rugged than any other solid-state amplifier providing comparable performance.

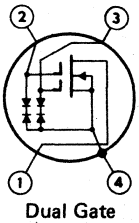
RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)



Single Gate



Dual Gate



Dual Gate
with gate protection

RCA Single-gate and dual-gate MOSFETs offer these features and benefits to the designer:

- Extremely high input resistance — imposes virtually no loading on AGC voltage source
- Very low feedback capacitance
- High forward transconductance
- Wide dynamic range — handle positive and negative input-signal excursions without diode-current loading
- Wide AGC range
- Virtually no AGC power required
- Very low gate leakage current — relatively insensitive to temperature variations
- Negative temperature coefficient of drain current — makes "thermal runaway" virtually impossible
- Zero offset voltage — especially desirable for chopper applications
- Bulk (substrate) terminal available on all single-gate types
- Substantially better cross-modulation characteristics and lower spurious response than junction-type FET's and bipolar transistors
- Operating-temperature range, all types: −65 to +175°C

RCA Dual-gate MOSFETs offer these additional features

- Extremely low feedback capacitance
- Reduced oscillator feedthrough
- Higher frequency capabilities
- Exceptionally high forward transconductance
- Higher vhf power gain
- No neutralization required
- Increased gain reduction with AGC
- Cross-modulation characteristics actually improve as device approaches cutoff
- Unique advantages for mixer, product-detector, remote gain control, color-demodulator, balanced-modulator, chopper, clipper, and gated-amplifier applications
- Can function as a triode equivalent device when the two gates are connected to a single terminal

Quick-Selection Guide

Application	Industrial Types													Consumer Types																	
	Single-Gate								Dual-Gate			Dual-Gate Protected		Single-Gate			Dual-Gate					Dual-Gate Protected									
	3N128	3N138	3N139	3N142	3N143	3N152	3N153	3N154	3N140	3N141	3N159	3N187	3N200	40819	40467A	40468A	40559A	40600	40601	40602	40603	40604	3N204	3N205	3N206	40673	3N211	3N212	3N213	40820	40821	40822	40823	40841
RF Amplifier, Mixer	■			■	■	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
Chopper		■					■																										■
General-Purpose Amplifier			■	■																■													■
Oscillator	■		■	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
Low-Noise						■					■	■	■										■	■			■	■						
Low-Leakage		■					■		■	■	■							■	■	■	■	■												
High-Gain						■			■		■	■	■										■	■	■		■	■	■					
Gain-Controlled									■	■	■	■	■	■				■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
Premium-Performance						■					■	■	■																				

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application and for instrumentation, chopper, and control application in industrial and military equipment

Description and Application				Absolute Maximum Ratings# At T_A = 25°C					
RCA Type	Description	Usable Frequency Range MHz	Circuits and End-Use Equipment	Drain-to-Source Volts V_{DS}		Gate 1-to-Source Volts V_{G1S}		Gate 2-to-Source Volts V_{G2S}	
				Neg.	Pos.	DC	Peak AC	DC	Peak AC
SINGLE-GATE DEVICES■									
For RF Applications									
3N128	High-Gain, Low-Noise RF Amplifier, IF Amplifier, Oscillator	to 250	High-Impedance Timing Circuits, Detectors, Frequency Multipliers, Phase Splitters, Pulse Stretchers, Voltage-Controlled Attenuators Electrometer Amplifiers, High-Impedance Differential Amplifiers in VHF Fixed and Mobile Communications Equipment and for Instrumentation and Navigation	0	+20	+1 to −8	±15	–	–
3N139	High-Gain RF Amplifier, Video Amplifier, IF Amplifier For Use With High Drain Supply Voltage (+35 V max.)	to 250		0	+35	±10	±14	–	–
3N142	High-Gain Low-Noise RF Amplifier and Oscillator	to 175		0	+20	+1 to −8	±15	–	–
3N143	Mixer and Oscillator	to 250		0	+20	+1 to −8	±15	–	–
3N152	Low-Noise, Premium-Performance RF Amplifier	to 250		0	+20	+1 to −8	±15	–	–
3N154	Low-Leakage Premium-Performance RF Amplifier	to 250		0	+20	+1 to −8	±15	–	–
For Chopper, Instrumentation, and Control Applications									
3N128	High-Gain DC Amplifier	to 250	Servo Amplifiers, Telemetry Amplifiers, Computer Operational Amplifiers, Sampling Circuits, Electrometer Amplifiers in Communications, Navigation, and Instrumentation Equipment and Control Circuits	0	+20	+1 to −8	±15	–	–
3N138	For Chopper and Multiplex Service to 60 MHz DC Amplifier	to 250		0	+35	±10	±14	–	–
3N139	DC Amplifier, Video Amplifier, RF Amplifier with High Drain Voltage Capability (+35 V max.)	to 250		0	+35	±10	±14	–	–
3N142	DC Amplifier	to 175		0	+20	+1 to −8	±15	–	–
3N153	For Chopper and Multiplex Service to 60 MHz DC Amplifier	to 250		0	+20	+6 to −8	±14	–	–
DUAL-GATE DEVICES WITH INTEGRAL GATE PROTECTION									
For RF Applications									
3N140	High-Gain, Low-Noise Gain-Controlled RF Amplifier, IF Amplifier	to 300	Communications Equipment	0	+20	+1 to −8	+20 to −8	−8 to 40% of V_{DS}	−8 to +20

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application and for instrumentation, chopper, and control application in industrial and military equipment

Electrical Characteristics at T_A = 25°C												
Typical Gate-Leakage (Input) Resistance r_{GS} Ohms	Offset Voltage V_O● Volts	Typical "ON" Resistance $r_{DS}(on)$ Ohms	Typical Power Gain G_{PS} dB	Typical Noise Figure NF dB	Noise Figure and Power Gain Test Frequency MHz	Typical Forward Transconductance g_{fs} umho	Max. Gate Leakage Current I_{GSS} nA	Typ. Input Capacitance C_{iss} pF	Typical Gate-to-Source Cutoff Volts V_{GS}	Typical Reverse Transfer Capacitance (Feedback) C_{rss} pF	Application Note and Data Sheet File No.	RCA Type
												SINGLE-GATE DEVICES■
												For RF Applications
–	–	–	16*	3.5	200	7500	5	5.5	–3	0.25	AN3193 AN3341 309	3N128
–	–	–	–	–	–	6000	1 0.1 nA Typ.	3	–6 max.	0.2	ST3703 284	3N139
–	–	–	16*	2.5	100	7500	1 0.1 pA Typ.	5.5	–3	0.22	ST3703 286	3N142
–	–	–	13.5 (conv.)	–	f_{IN}=200 f_{OUT}=30	7500	200	5.5	–3	0.25	AN3193 AN3341 309	3N143
–	–	–	16*	2.5	200	7500	1 0.1 pA Typ.	5.5	–3	0.25	ST3703 314	3N152
Closely Controlled Zero-Bias Drain Current (I_{DSS}), 10 to 25 mA			16*	3.5	200	7500	5 0.1 pA Typ.	5.5	–3	0.25	– 335	3N154
												For Chopper, Instrumentation, and Control Applications
10^{14}	0	200	16*	3.5	200	7500	5	5.5	–3	0.25	AN3193 AN3341 309	3N128
10^{14}	0	180#	–	–	–	6000	10 pA	3	–10 max.	0.2	AN3452 283	3N138
10^{14}	0	200	–	–	–	6000	1	3	–6 max.	0.2	ST3703 284	3N139
10^{12}	0	200	16*	2.5	100	7500	1 0.1 pA Typ.	5.5	–3	0.22	ST3703 286	3N142
10^{10}	0	200##	–	–	–	10000	50 pA	6	–2	0.34	– 320	3N153
												DUAL-GATE DEVICES WITH INTEGRAL GATE PROTECTION
												For RF Applications
–	–	–	–	3.5	18	10000	1▲	5.5	–2▲	0.02	– 285	3N140

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application and for instrumentation, chopper, and control application in industrial and military equipment—cont'd.

Description and Application				Absolute Maximum Ratings# At T_A = 25°C					
RCA Type	Description	Usable Frequency Range MHz	Circuits and End-Use Equipment	Drain-to-Source Volts V_{DS}		Gate 1-to-Source Volts V_{G1S}		Gate 2-to-Source Volts V_{G2S}	
				Neg.	Pos.	DC	Peak AC	DC	Peak AC
3N141	Mixer, Product Detector, Modulator	to 300	Aircraft and Marine Vehicular Receivers	0	+20	+1 to −8	+20 to −8	−8 to 40% VDS	−8 to +20
3N159	High-Gain, Very Low-Noise, Gain-Controlled RF Amplifier	to 300		0	+20	+1 to −8	+20 to −8	−8 to 40% V_{DS}	−8 to +20
3N187	RF Amplifier, Mixer, and IF Amplifier	to 300	CATV and MATV Equipment	−0.2	+20	+3 to −6	±6	−6 to 30% V_{DS}	±6
3N200	High-Gain RF Amplifier, Mixer, and IF Amplifier	to 500	Telemetry and Multiplex Equipment	−0.2	+20	+3 to −6	±6	−6 to 30% V_{DS}	±6
40819	RF Amplifier, Mixer, and IF Amplifier	to 300		−0.2	+25	+3 to −6	±6	−6 to 40% V_{DS}	±6
For Chopper, Instrumentation, and Control Applications									
3N140	DC Amplifier	to 300	See Choppers Instrumentation, and Control Applications on Page 4	0	+20	+1 to −8	+20 to −8	−8 to 40% V_{DS}	−8 to +20
3N141	DC Amplifier	to 300		0	+20	+1 to −8	+20 to −8	−8 to 40% V_{DS}	−8 to +20
40841	General-Purpose	to 500				−4.5 to +3		−4.5 to 40% V_{DS}	

For a Maximum Drain Current (I_D) = 50 mA, Device Dissipation (P_T) = 330 mW

■ Bulk (Substrate) is brought out as a separate terminal lead (connected to case internally).

RCA MOSFETs for RF application in consumer equipment

Description and Application				Absolute Maximum Ratings # at T_A = 25°C					
RCA Type	Description	Usable Frequency Range MHz	End-Use Equipment	Drain-to-Source Volts V_{DS}		Gate 1-to-Source Volts V_{G1S}		Gate 2-to-Source Volts V_{G2S}	
				Neg.	Pos.	DC	Peak AC	DC	Peak AC
SINGLE-GATE DEVICES■									
40467A	200-MHz General-Purpose RF Amplifier and Oscillator	to 220	VHF Amplifier Applications in Commercial and Industrial Electronic Equipment	0	+20	+1 to −8	±15	–	–

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application and for instrumentation, chopper, and control application in industrial and military equipment—cont'd.

Electrical Characteristics at T_A = 25°C												
Typical Gate-Leakage (Input) Resistance r_{GS} Ohms	Offset Voltage V_O● Volts	Typical "ON" Resistance $r_{DS(on)}$ Ohms	Typical Power Gain G_{PS} dB	Typical Noise Figure NF dB	Noise Figure and Power Gain Test Frequency MHz	Typical Forward Transconductance g_{fs} umho	Max. Gate Leakage Current I_{GSS} nA	Typ. Input Capacitance C_{iss} pF	Typical Gate-to-Source Cutoff Volts V_{GS}	Typ. Rev. Transfer Capacitance (Fdbk) C_{rss} pF	Application Note and Data Sheet File No.	RCA Type
–	–	–	17 (conv.)	–	f_{IN}= 200 f_{OUT}=30	10000	1▲	5.5	−2▲	0.02	– 285	3N141
–	–	–	16 min.	2.5	200	10000	1▲	5.5	−2▲	0.02	– 326	3N159
–	–	–	18	3.5	200	12000	50▲	6	−2▲	0.02	ST3703 AN4018 436	3N187
–	–	–	12.5	3.9	400	15000	50▲	6	−1▲	0.02	ST3703 AN4018 437 AN4431	3N200
–	–	–	18	3.5	200	12000	50▲	6	−2▲	0.02	ST3703 AN4018 463	40819
For Chopper, Instrumentation, and Control Applications												
10^{12}	0	–	–	–	–	10000	1▲	5.5	−2▲	0.02	– 285	3N140
10^{12}	0	–	–	–	–	10000	1▲	5.5	−2▲	0.02	– 285	3N141
–	–	–	32 24 (conv.)	0.46†	Gps at 44 MHz	12000	60▲	6.5	−2▲	0.20	– 498	40841

* Fixed Neutralization
#Typical "OFF" resistance $[r_{DS(off)}] = 10^{11}\ \Omega$
##Typical "OFF" resistance $[r_{DS(off)}] = 10^{10}\Omega$

●In measurements of Offset Voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings of 1 microvolt or more. These errors may be minimized by the use of solder having a low thermal e.m.f., such as Leeds & Northrup No. 107-1.0.1, or equivalent.

■Bulk (Substrate) is brought out as a separate terminal lead connected to case internally.

▲Value applies to each gate

†Audio spot at 1 kHz.

RCA MOSFETs for RF application in consumer equipment

Electrical Characteristics at T_A = 25°C										
Typical Power Gain G_{PS} dB	Typical Noise Figure NF dB	Noise Figure and Power Gain Test Frequency MHz	Typical Forward Transconductance g_{fs} umho	Max. Gate Leakage Current I_{GSS} mA	Typ. Input Capacitance C_{iss} pF	Typical Gate-to-Source Cutoff Volts		Typical Reverse Transfer Capacitance (Feedback) C_{rss} pF	Application Note and Data Sheet File No.	RCA Type
						Gate 1 V_{G1S}	Gate 2 V_{G2S}			
SINGLE-GATE DEVICES■										
16	3.5	200	7500	1	5.5	−8 max.	–	0.16	ST-2990A 324	40467A

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application in consumer equipment - cont'd.

Description and Application				Absolute Maximum Ratings # at T_A = 25°C					
RCA Type	Description	Usable Frequency Range MHz	End-Use Equipment	Drain-to-Source Volts V_{DS}		Gate 1-to-Source Volts V_{G1S}		Gate 2-to-Source Volts V_{G2S}	
				Neg.	Pos.	DC	Peak AC	DC	Peak AC
40468A	100-MHz RF Amplifier	to 125	FM and AM/FM Receivers	0	+20	+1 to −8	±15	–	–
40559A	100-MHz Oscillator or Mixer	to 125		0	+20	+1 to −8	±15	–	–
DUAL-GATE DEVICES									
40600	200-MHz Gain-Controlled RF Amplifier	to 250	VHF TV Tuners	0	+20	+1 to −8	+20 to −8	−8 to 40% to V_{DS}	−8 to +20
40601	200-MHz Mixer	to 250		0	+20	+1 to −8	+20 to −8	−8 to 40% of V_{DS}	−8 to +20
40602	44-MHz Gain-Controlled IF Amplifier	to 75	TV Receivers	0	+20	+1 to −8	+20 to −8	−8 to 40% of V_{DS}	−8 to +20
40603	100-MHz Gain-Controlled IF Amplifier	to 150	FM Receivers	0	+20	+1 to −8	+20 to −8	−8 to 40% of V_{DS}	−8 to +20
40604	100-MHz Mixer	to 150		0	+20	+1 to −8	+20 to −8	−8 to 40% of V_{DS}	−8 to +20
DUAL-GATE DEVICES WITH INTEGRAL GATE-PROTECTION									
3N204	Low-Noise	RF Amplifier	to 220	VHF TV Receivers	0	+25	P_T = 360 mW		
3N205		Mixer	to 220		0	+25	P_T = 360 mW		
3N206		IF Amplifier	to 220		0	+25	P_T = 360 mW		
3N211		RF Amplifier	to 220		0	+27	P_T = 360 mW		
3N212		Mixer	to 220		0	+27	P_T = 360 mW		
3N213		IF Amplifier	to 220		0	+35	P_T = 360 mW		

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application in consumer equipment - cont'd.

Electrical Characteristics at T_A = 25°C										
Typical Power Gain G_{PS} dB	Typical Noise Figure NF dB	Noise Figure and Power Gain Test Frequency MHz	Typical Forward Transconductance g_{fs} uMho	Max. Gate Leakage Current I_{GSS} mA	Typ. Input Capacitance C_{iss} pF	Typical Gate-to-Source Cutoff Volts: Gate 1 V_{G1S}	Typical Gate-to-Source Cutoff Volts: Gate 2 V_{G2S}	Typical Reverse Transfer Capacitance (Feedback) C_{rss} pF	Application Note and Data Sheet File No.	RCA Type
17	3.5	100	7500	1	5.5	−8 max.	–	0.16	AN-3453 323 AN-3535	40468A
22 (conv.)	–	f_{IN} = 100 f_{OUT}=10.7	2800 (conv.)	1	5.5	−8 max.	–	0.17	AN-3535 323	40559A
DUAL-GATE DEVICES										
20	3.5	200	10000	1	5.5	−3	−3	0.02	ST-3703 333	40600
14 (conv.)	–	200	2800 (conv.)	1	5.5	−3	−3	0.02	ST-3703 333	40601
28	–	44	10000	1	5.5	−3	−3	0.02	ST-3703 333	40602
24	3	100	10000	1	5.5	−3	−3	0.02	ST-3703 334	40603
23 (conv.)	–	f_{IN} = 100 f_{OUT}=10.7	2800 (conv.)	1	5.5	−3	−3	0.02	ST-3703 334	40604
DUAL-GATE DEVICES WITH INTEGRAL GATE-PROTECTION										
24 (Insertion)	2.5	200	14	10▲	5	−4 max.	−4 max.	0.03 max.	– 959	3N20[illegible]
23 (conv.)	–	200	14	10▲	5	−4 max.	−4 max.	0.03 max.	– 959	3N205
30 (Insertion)	3	45	12	10▲	5	−4 max.	−4 max.	0.03 max.	– 959	3N206
30 (Insertion)	2.5	–	30	10▲	7	−5.5 max.	−2.5 max.	0.05 max.	– 875	3N211
25 (conv.)	–	200	30	10▲	7	−4 max.	−4 max.	0.05 max.	– 875	3N212
31 (Insertion)	3	45	25	10▲	7	−5.5 max.	−4 max.	0.05 max.	– 875	3N213

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application in consumer equipment - cont'd.

Description and Application				Absolute Maximum Ratings # at T_A = 25°C					
RCA Type	Description	Usable Frequency Range MHz	End-Use Equipment	Drain-to-Source Volts V_{DS}		Gate 1-to-Source Volts V_{G1S}		Gate 2-to-Source Volts V_{G2S}	
				Neg.	Pos.	DC	Peak AC	DC	Peak AC
40673	200 MHz RF Amplifier, Mixer, and IF Amplifier	to 400	Aircraft and Marine Receivers CATV and MATV Equipment	−0.2	+20	+1 to −6	±6	−6 to 30% of V_{DS}	±6
40820	RF Amplifier	to 250	VHF TV Tuners	−0.2	+20	+3 to −6	±6	−6 to 40% of V_{DS}	±6
40821	RF Mixer	to 250		−0.2	+20	+3 to −4.5	±6	−4.5 to 40% of V_{DS}	±6
40822	RF Amplifier	to 250	FM Tuners	−0.2	+18	+3 to −6	±6	−6 to 40% of V_{DS}	±6
40823	RF Mixer	to 150		−0.2	+18	+3 to −4.5	±6	−4.5 to 40% of V_{DS}	±6

For a Maximum Drain Current (I_D) = 50 mA,
Device Dissipation (P_T) = 330 mW
Operating Temperature Range (T_A) = −65°C to +121°C

■ Bulk (Substrate) is brought out as a separate terminal lead (connected to case internally)

Handling of MOSFETs which do not include gate-protection circuits

Insulated-Gate Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in a MOSFET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

In some MOSFETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms.

MOSFETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

*Trademark: Emerson and Cumming, Inc.

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application in consumer equipment - cont'd.

Electrical Characteristics at T_A = 25°C										
Typical Power Gain G_{PS} dB	Typical Noise Figure NF dB	Noise Figure and Power Gain Test Frequency MHz	Typical Forward Transcond-uctance g_{fs} umho	Max. Gate Leakage Current I_{GSS} mA	Typ. Input Capac-itance C_{iss} pF	Typical Gate-to-Source Cutoff Volts		Typical Reverse Transfer Capacitance (Feedback) C_{rss} pF	Application Note and Data Sheet File No.	RCA Type
						Gate 1 V_{G1S}	Gate 2 V_{G2S}			
18	3.5	200	12000	50	6	−2	−2	0.02	ST-3703 381 AN-4018	40673
17	4.5	200	12000	50	6	−1	−1	0.02	ST-3703 464 AN4018	40820
11 (conv.)	–	f_{IN}=200 f_{OUT}=44	12000	50	6	−1	−1	0.02	ST-3703 464 AN-4018	40821
24	3.5	100	12000	50	6.5	−2	−2	0.02	ST-3703 465 AN-4018	40822
18 (conv.)	–	f_{IN} = 100 f_{OUT}=10.7	12000	50	6.5	−2	−2	0.02	ST-3703 465 AN4018	40823

■ Bulk (Substrate is brought out as a separete terminal lead (connected to case internally.

▲ Value applies to each gate

APPLICATION NOTES

No.	Title
AN3193	"Application Considerations for the RCA-3N128 VHF MOS Field-Effect Transistor"
AN3341	"VHF Mixer Design Using the RCA-3N128 MOS Transistor"
AN3435	"Cross-Modulation Effects in Single-Gate and Dual-Gate MOS FET Transistors"
AN3452	"Chopper Circuits Using RCA MOS Field-Effect Transistors"
AN3453	"An FM Tuner Using an RCA-40468 MOS-Transistor RF Amplifier"
AN3535	"An FM Tuner Using Single-Gate MOS Field-Effect Transistors as RF Amplifier and Mixer"
AN4018	"Design of Gate-Protected MOS Field-Effect Transistors"
AN4125	"MOS FET Biasing Techniques"
AN4431	"RF Applications of the Dual-Gate MOS FET up to 500 MHz"
AN4590	"Using MOS FET IC's in Linear Circuit Applications"
ST3486	"Application of Dual-Gate MOS Field-Effect Transistors in Practical Radio Receivers"
ST3520	"Insulated-Gate Field-Effect Transistors in Oscillator Circuits"

A copy of a Technical Bulletin for any of the MOSFET types or a copy of the Application Notes shown above, is available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876. To expedite receipt of the requested data, please refer to the Technical Bulletin File No. shown on the Characteristics Charts, or to the Application Note No.

Supplementary Information

RCA High-Reliability Bipolar IC's

RCA MIL-STD-883 Slash-Series Linear IC's

The RCA CA3000 slash-series of high-reliability linear integrated circuits includes a broad range of types for use in satellites and other aerospace, military, and critical industrial applications in which maintenance is extremely difficult. These integrated circuits are processed and screened in accordance with MIL-STD-883, Method 5004 format.

The RCA CA3000 slash-series types are supplied to three screening levels (/1, /3, and /3W) that meet the electrical, mechanical, and environmental test methods and procedures established for microelectronics in MIL-STD-883.

RCA CA3000-series IC products listed below are commercial products that can be supplied to standard RCA screening levels or to specialized customer requirements on a custom basis.

CA3000-Series Linear IC's and MOS/FET's

Type No.	Description	No. of Leads
CA101A	Operational Amplifiers	8
CA723	Voltage Regulators	10
CA741	Operational Amplifiers	8
CA747	Dual Operational Amplifiers	10
CA748	Operational Amplifiers	8
CA1558	Dual Operational Amplifiers	8
CA3000	Differential Amplifiers	10
CA3001	Differential Amplifiers	12
CA3002	Differential Amplifiers	10
CA3004	Differential Amplifiers (RF)	12
CA3006	Differential Amplifiers (RF)	12
CA3015A	Operational Amplifiers	12
CA3018A	Transistor Arrays	12
CA3019	Diode Arrays	10
CA3020A	Wide-Band Power Amplifiers	12
CA3026	Dual Differential Amplifier Arrays	12
CA3028B	Differential Amplifiers (RF)	8
CA3039	Diode Arrays	12
CA3045	Transistor Arrays	14
CA3049	Dual Differential Amplifier Arrays	12
CA3058	Zero-Voltage Switches	14
CA3078	Micropower Operational Amplifiers	8
CA3080	Variable Operational Amplifiers	8
CA3081	Transistor Arrays	16
CA3082	Transistor Arrays	16
CA3085	Voltage Regulators	8
CA3085A	Voltage Regulators	8
CA3085B	Voltage Regulators	8
CA3094	Programmable Power Switch/ Amplifier	8
CA3094A	Programmable Power Switch/ Amplifier	8
CA3094B	Programmable Power Switch/ Amplifier	8
CA3100	BiMOS Operational Amplifiers	8
CA3118	Transistor Arrays	12
CA3118A	Transistor Arrays	12
CA3130	BiMOS Operational Amplifiers	8
CA3130A	BiMOS Operational Amplifiers	8
CA3140	BiMOS Operational Amplifiers	8
CA3140A	BiMOS Operational Amplifiers	8
CA3160	BiMOS Operational Amplifiers	8
CA3160A	BiMOS Operational Amplifiers	8
CA3260T	BiMOS Operational Amplifier	8
CA3260AT	BiMOS Operational Amplifier	8
CA3290	BiMOS Dual Voltage Comparators	8

MOS/FET's

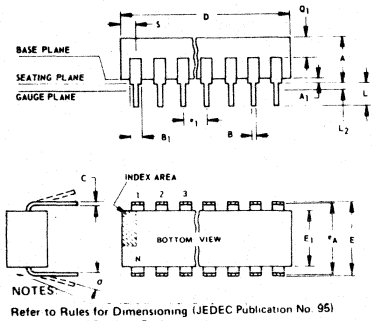
HR3N187	Dual-Gate MOS Field-Effect Transistor	4
HR3N200	Dual-Gate MOS Field-Effect Transistor	4

Note:
High-reliability versions of most commercially available CA3000-series linear IC's not listed above can also be supplied on a custom basis.

Screening Levels for RCA MIL-STD-883 Slash-Series Linear Integrated Circuits

RCA Levels	Screening Levels: MIL-STD-883, Method 5004 Format	Application	Description
For Packaged Devices (D, F, K, S, T, or V1 Suffix)			
/1	Class S with Condition B Precap Visual Inspection	Aerospace and Missiles	For devices intended for use where maintenance and replacement are impossible and reliability is imperative
/3	Class B	Military and Industrial For example, in Airborne Electronics	For devices intended for use where maintenance and replacement can be performed but are difficult and expensive
/3W	Class B with High- and Low-Temperature DC Testing omitted		
For Chips (H Suffix)			
/M	Condition B Precap Visual Inspection with Traceability and Certificate of Compliance Required	Military and Industrial	For general applications

CERAMIC DUAL-IN-LINE PACKAGES



NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(D) Suffix (JEDEC MO-001-AD) 14-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.065	0.090		1.66	2.28

92SS-4411R2

(D) Suffix (JEDEC MO-001-AE) 16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

92SS-4286R5

DUAL-IN-LINE PLASTIC, (E) SUFFIX AND FRIT-SEAL CERAMIC, (F) SUFFIX PACKAGES

(E) Suffix 8-Lead Plastic (Mini-DIP)

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.889	1.65
C	0.008	0.012	1	0.203	0.304
D	0.370	0.400		9.40	10.16
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.762
α	0	15	4	0	15
N	8		5	8	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.381	1.52

92CS-24026R1

(E) and (F) Suffixes (JEDEC MO-001-AB) 14-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

92SS-4296R3

(F) Suffix (JEDEC MO-001-AC) 16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-15967R4

(E) Suffix 18-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.845	0.885		21.47	22.47
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2,3	7.62 TP	
L	0.125	0.150		3.18	3.81
α	0°	15°	4	0°	15°
N	18		5	18	
N_1	0		6	0	
S	0.015	0.060		0.39	1.52

92CS-30630

(E) Suffix 22-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.015	0.020		0.381	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D		1.120			28.44
E	0.390	0.420		9.91	10.66
E_1	0.345	0.355		8.77	9.01
e_1	0.100 TP		2	2.54 TP	
e_A	0.400 TP		2, 3	10.16 TP	
L	0.125	0.150		3.18	3.81
L_2	0	0.030		0	0.762
α	2°	15°	4	2°	15°
N	22		5	22	
N_1	0		6	0	
Q_1	0.055	0.085		1.40	2.15
S	0.015	0.060		0.381	1.27

92CS-30830

(E) Suffix (JEDEC MO-015-AA) 24-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A_1	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B_1	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	1.20	1.29		30.48	32.76
E	0.600	0.625		15.24	15.87
E_1	0.515	0.580		13.09	14.73
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.200		2.54	5.00
L_2	0.000	0.030		0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.040	0.100		1.02	2.54

92CS26938R3

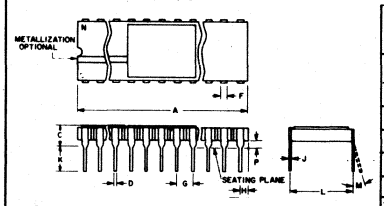
Dimensional Outlines

DUAL-IN-LINE PLASTIC PACKAGE (Cont'd)
(E) Suffix
28-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A_1	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B_1	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	1.400	1.490		35.56	37.85
E_1	0.515	0.580		13.09	14.73
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.200		2.54	5.00
L_2	0.000	0.030		0.00	0.76
α	0°	15°	4	0°	15°
N	28		5	28	
N_1	0		6	0	
Q_1	0.045	0.080		1.14	2.03
S	0.040	0.100		1.02	2.54

92CS-31862

DUAL-IN-LINE SIDE-BRAZED CERAMIC PACKAGE
(D) Suffix
18-Lead

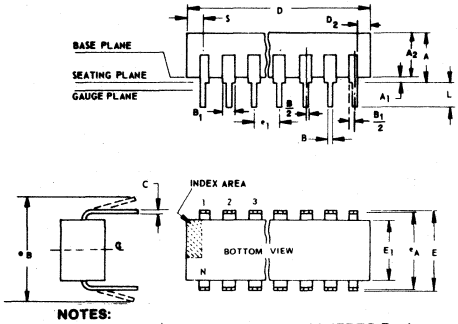


NOTES:
1. Leads within 0.005" (0.13 mm)-radius of True Position at maximum material condition.
2. Dimension "L" to center of leads when formed parallel.
3. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.890	0.915		22.606	23.241
C	—	0.200		—	5.080
D	0.015	0.021		0.381	0.533
F	0.054 REF.		1	1.371 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.035	0.065		0.889	1.651
J	0.008	0.012	3	0.203	0.304
K	0.125	0.150		3.175	3.810
L	0.290	0.310	2	7.366	7.874
M	0°	15°		0°	15°
P	0.025	0.045		0.635	1.143
N	18			18	

92CS-27231R1

(E) Suffix (JEDEC MS-001)
16-Lead Dual-In-Line Plastic Package

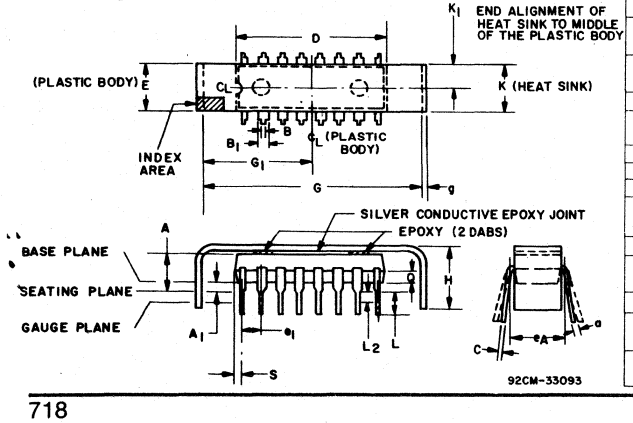


NOTES:
1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines.
2. Protrusions (flash) on the base plane surface shall not exceed .25 mm (.010 in.).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions 1, N, $\frac{N}{2}$, $\frac{N}{2}$ +1.
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed .25 mm (.010 in.).
5. This dimension is controlling when a particular combination of body length, lead width and lead spacing dimensions would allow lead material to overhang the ends of the package.
6. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
7. Dimension E_1 does not include mold flash or protrusions.
8. Package body and leads shall be symmetrical around center line shown in end view within .25 mm (.010 in.).
9. Lead spacing e_1 shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
10. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within .25 mm (.010 in.) diameter for dimension e_A.
11. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
12. N is the maximum number of lead positions.
13. Dimension S at the left end of the package must equal dimension S at the right end of the package within .76 mm (.030 in.).

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	—	0.210	10	—	5.33
A_1	0.015	—	10	0.39	—
A_2	0.115	0.195		2.93	4.95
B	0.014	0.022		0.356	0.558
B_1	0.045	0.070	3	1.15	1.77
C	0.008	0.015		0.204	0.381
D	0.745	0.840	4	18.93	21.33
D_2	0.005	—	5	0.13	—
E	0.300	0.325	6	7.62	8.25
E_1	0.240	0.280	7, 8	6.10	7.11
e_1	0.090	0.110	9	2.29	2.79
e_A	0.300 TP		10	7.62 TP	
e_B	—	0.410	11	—	10.41
L	0.115	0.150	10	2.93	3.81
N	16		12	16	
S	—	—	13	—	—

92CM-34834R1

(EM) Suffix
16-Lead Modified Dual-In-Line Plastic Package with "Power Slab"



92CM-33093

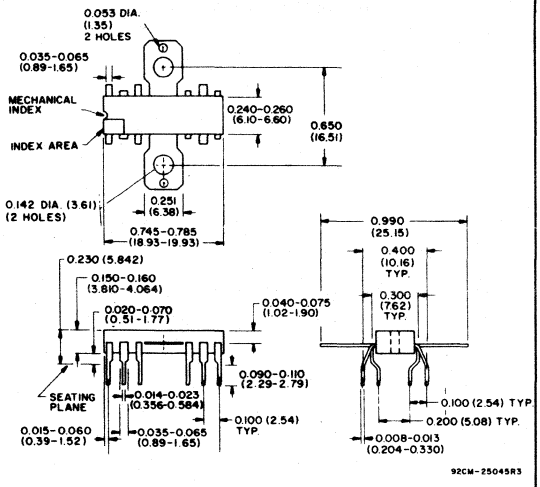
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2,3	7.62 TP	
G_1	0.537	0.587		13.64	14.91
G	1.125			28.58	
g	0.030	0.036		0.76	0.91
H	0.350			8.89	
K	0.250		7	6.35	
K_1	0.093	0.157		2.36	3.99
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.
7. Bulging to 0.280" (7.11 mm) permissible at points of debossing.

Dimensional Outlines

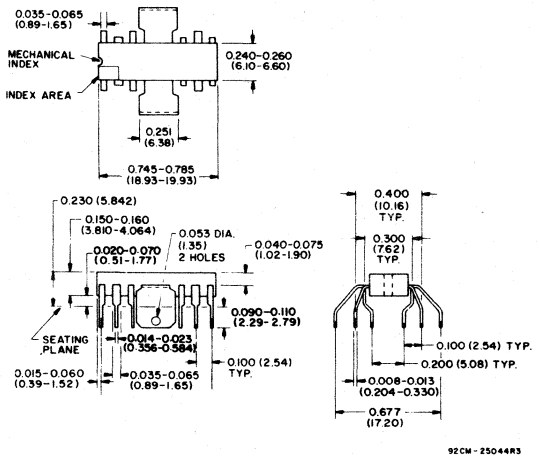
QUAD-IN-LINE PLASTIC PACKAGES

(QM) Suffix
Modified 16-Lead with Integral Flat Wing-Tab Heat Sink

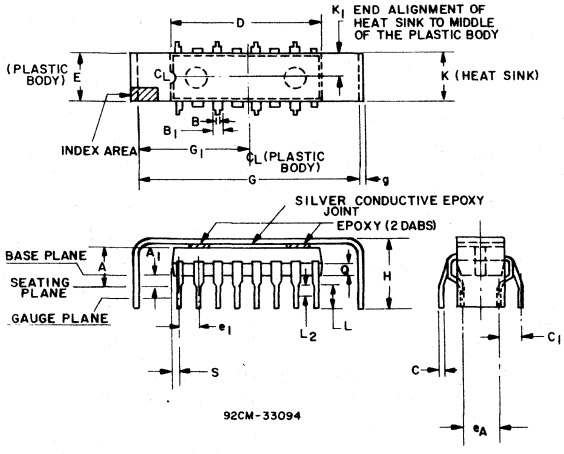


DIMENSIONS IN PARENTHESES ARE MILLIMETER EQUIVALENTS OF THE BASIC INCH DIMENSIONS

(Q) Suffix
Modified 16-Lead with Integral Bent Down Wing-Tab Heat Sink



(QM) Suffix, 16-Lead Quad-In-Line Plastic with "Power Slab"



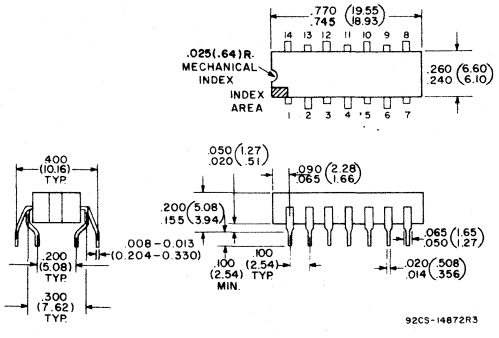
SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
C_1	0.095	0.105		2.41	2.67
D	0.745	0.785		18.93	19.93
E	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.200 TP		2,3	7.62 TP	
G	1.125 TP			2.858	
G_1	0.537	0.587		13.64	14.91
g	0.030	0.036		0.76	0.91
H	0.350			8.89	
K	0.250		7	6.35	
K_1	0.093	0.157		2.36	3.99
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for *Axial Lead Product Outlines*.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.
7. Bulging to 0.280" (7.11 mm) permissible at points of debossing.

QUAD-IN-LINE PLASTIC PACKAGES

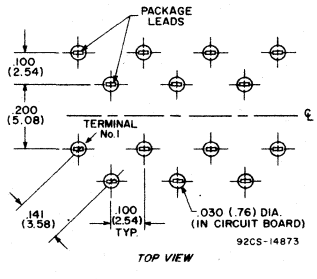
(W) Suffix, 14-Lead Staggered



NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

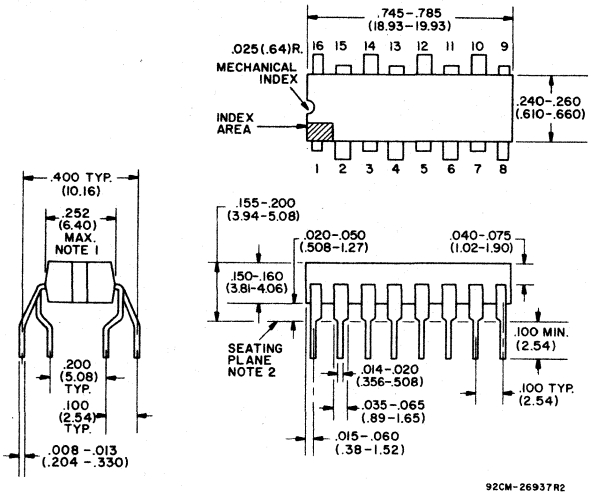
Recommended Mounting Hole Dimensions and Spacing



Dimensional Outlines

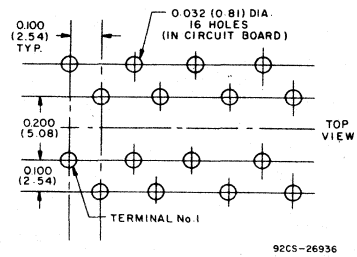
QUAD-IN-LINE PLASTIC PACKAGES

(W) Suffix, 16-Lead Staggered



92CM-26937R2

Recommended Mounting Hole Dimensions and Spacing

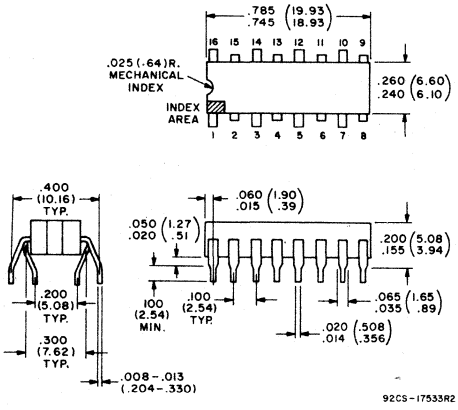


92CS-26936

NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

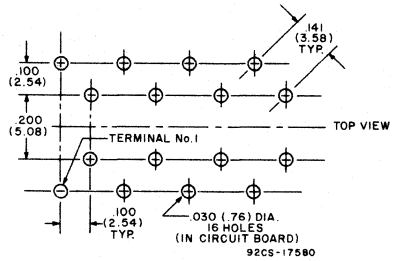
Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

(Q) Suffix, 16-Lead



92CS-17533R2

Recommended Mounting Hole Dimensions and Spacing

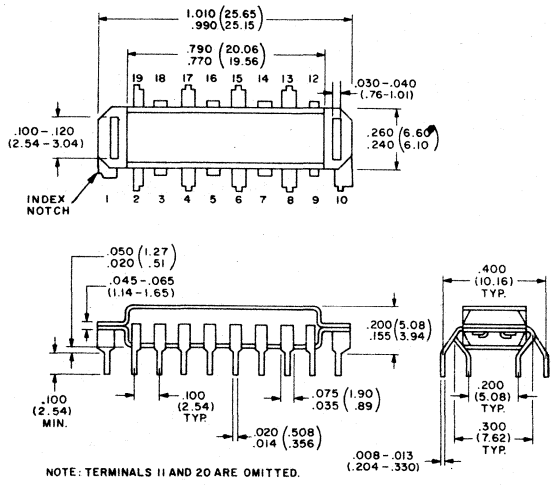


92CS-17580

NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

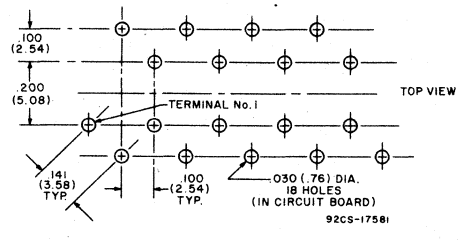
20-Lead Shielded Plastic Package



NOTE: TERMINALS 11 AND 20 ARE OMITTED.

92CS-17587R1

Recommended Mounting Hole Dimensions and Spacing



92CS-17581

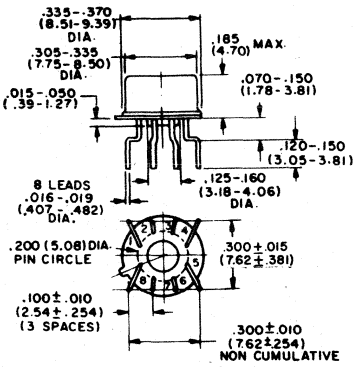
NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

Dimensional Outlines

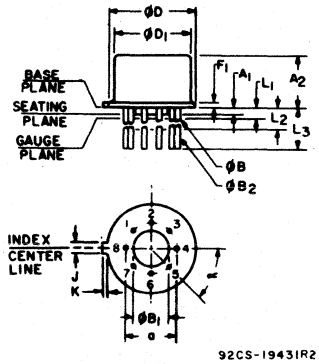
TO-5 STYLE PACKAGES

(S) Suffix, 8-Lead TO-5 Style with Dual-In-Line Formed Leads (DIL-CAN)



92CS-20296R3

(T) Suffix (JEDEC MO-002-AL), 8-Lead TO-5 Style



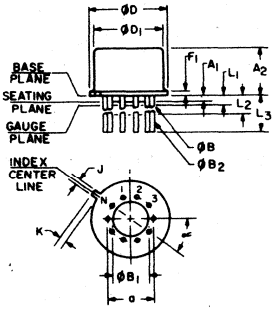
92CS-19431R2

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.200 TP		2	5.88 TP	
A_1	0.010	0.050		0.26	1.27
A_2	0.165	0.185		4.20	4.69
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0.125	0.160		3.18	4.06
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	45° TP			45° TP	
N	8		6	8	
N_1	3		5	3	

NOTES

1. Refer to JEDEC Publication No 95 for Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radium of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2 øB2 applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

(T) Suffix (JEDEC MO-006-AF), 10-Lead TO-5 Style

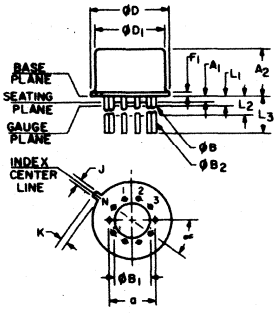


SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230 TP		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0	0		0	0
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	36° TP			36° TP	
N	10		6	10	
N_1	1		5	1	

NOTES:
1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2. $øB_2$ applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

92CS-15835

(T) Suffix (JEDEC MO-006-AG), 12-Lead TO-5 Style



92CS-19774

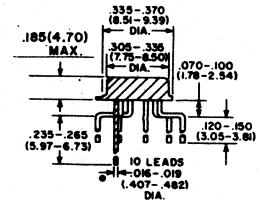
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0	0		0	0
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	30° TP			30 TP	
N	12		6	12	
N_1	1		5	1	

NOTES:
1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2. $øB_2$ applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

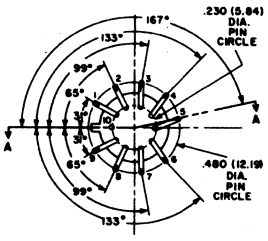
Dimensional Outlines

TO-5 STYLE PACKAGE (Cont'd)

(V) Suffix
10 Formed Leads Radially Arranged TO-5 Type (Available in 8 and 12-lead versions)

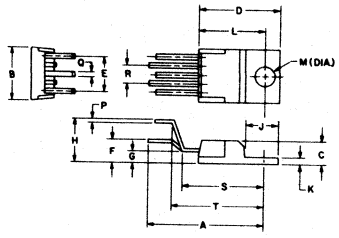


92CS-14638R2



TO-220 STYLE (VERSA-V) PLASTIC PACKAGE

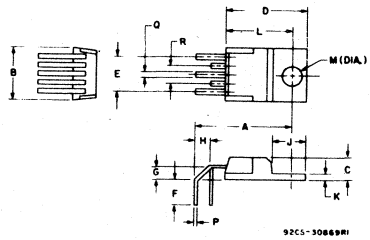
VERTICAL MOUNT



92CS-30868RI

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.876	0.896	22.25	22.75
B	0.396	0.408	10.06	10.36
C	0.173	0.182	4.395	4.622
D	0.604	0.619	15.35	15.72
E	0.263	0.273	6.681	6.934
F	0.168	0.188	4.268	4.775
G	0.100	0.104	2.540	2.641
H	0.320	0.340	8.128	8.638
J	0.246	0.254	6.249	6.451
K	0.046	0.054	1.169	1.371
L	0.496	0.508	12.60	12.90
M	0.140	0.150	3.556	3.810
N	5		5	
P	0.015	0.020	0.381	0.406
Q	0.033	0.040	0.839	1.016
R	0.129	0.139	3.277	3.530
S	0.600	0.630	15.24	16.00
T	0.680	0.710	17.27	18.03

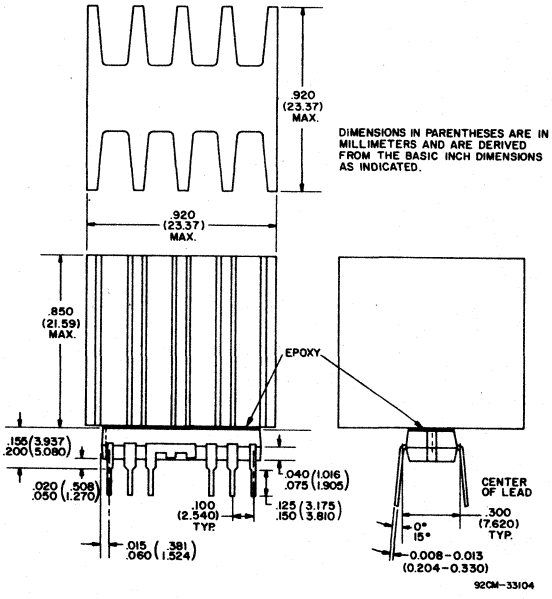
HORIZONTAL MOUNT (M Suffix)



92CS-30869RI

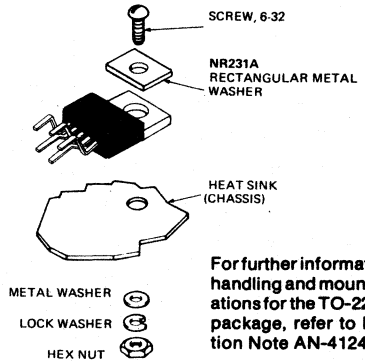
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.726	0.746	18.44	18.94
B	0.396	0.408	10.06	10.36
C	0.173	0.182	4.395	4.622
D	0.604	0.619	15.35	15.72
E	0.263	0.273	6.681	6.934
F	0.221	0.251	5.614	6.375
G	0.100	0.104	2.540	2.641
H	0.143	0.163	3.633	4.140
J	0.246	0.254	6.249	6.451
K	0.046	0.054	1.169	1.371
L	0.496	0.508	12.60	12.90
M	0.140	0.150	3.556	3.810
N	5		5	
P	0.015	0.020	0.381	0.406
Q	0.033	0.040	0.839	1.016
R	0.129	0.139	3.277	3.530

(EM) Suffix (Dual-In-Line)
Modified 16-Lead with Integral Heat Sink



92CM-33104

Suggested Hardware and Mounting Arrangement



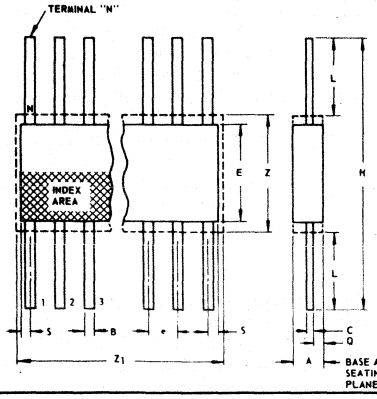
For further information regarding handling and mounting considerations for the TO-220 style plastic package, refer to RCA Application Note AN-4124.

NOTE: MAXIMUM TORQUE APPLIED TO MOUNTING FLANGE IS 8-in.-lb. (0.09 kgf-m)

92CS-29194RI

CERAMIC FLAT PACKS

(K) Suffix (JEDEC MO-004-AF), 14-Lead

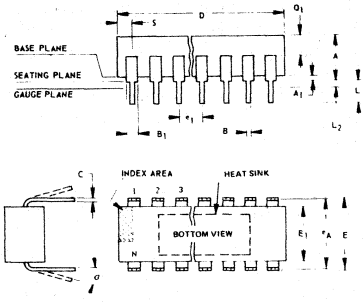


NOTES:
1. Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
2. Leads within .005" (.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92SS-4300R3

(P) Suffix
16-Lead "Power Slab" Dual-In-Line Plastic Package

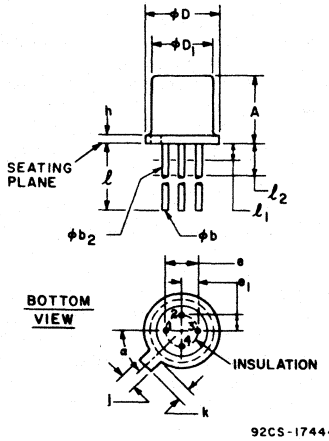


NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-32023

JEDEC TO-72 Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX	MIN	MAX	
A	0.170	0.210	4.32	5.33	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		4
e_1	0.050 T.P.		1.27 T.P.		4
h		0.030		0.762	
l	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
l	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
α	45° T.P.		45° T.P.		4, 6

Note 1 (Four leads) Maximum number leads omitted in this outline, "none" (0). The number and position of leads actually present are indicated in the product registration. Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads.

Note 2 (All leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and .500" (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond .500" (12.70 mm) from seating plane.

Note 3 Measured from maximum diameter of the product.

Note 4 Leads having maximum diameter .019" (.483 mm) measured in gaging plane .054" (1.37 mm) + .001" (.025 mm) - .000" (.000 mm) below the seating plane of the product shall be within .007" (.178 mm) of their true position relative to a maximum width tab.

Note 5 The product may be measured by direct methods or by gage.

Note 6 Tab centerline.

92CS-17444R1

Abstracts of Application Notes

AN-3193 ..... 9 pages
Application Considerations for the RCA-3N128 VHF MOS Field-Effect Transistor

This Note describes applications and vhf circuit considerations for a high-frequency n-channel MOS field-effect transistor, the RCA 3N128. Biasing requirements and basic circuit configurations are discussed, and selection of the optimum operating point and methods of automatic gain control are explained. The cross-modulation and intermodulation distortion characteristics of the 3N128 MOS transistor are compared to those of bipolar transistors, and procedures are given for the design of a practical vhf amplifier that uses the 3N128.

AN-3341 ..... 3 pages
VHF Mixer Design Using the RCA-3N128 MOS Transistor

The 3N128 is a vhf MOS field-effect transistor suitable for use throughout the vhf band (30 to 300 MHz) as an amplifier, mixer, or oscillator. This Note discusses some of the design criteria pertinent to the construction of MOS mixers, and presents an example of a complete vhf MOS converter.

AN-3452 ..... 7 pages
Chopper Circuits Using RCA MOS Field-Effect Transistors

Although electromechanical relays have long been used to convert low-level dc signals into ac signals or for multiplex purposes, relays are seriously limited with respect to life, speed, and size. Conventional (bipolar) transistors overcome the inherent limitations of relays, but introduce new problems of offset voltage and leakage currents. This Note describes the use of MOS field-effect transistors in solid-state chopper and multiplex designs that have the long life, fast speed, and small size of bipolar-transistor choppers, but that eliminate their inherent offset-voltage and leakage-current problems.

AN-3453 ..... 6 pages
An FM Tuner Using an RCA-40468 MOS-Transistor RF Amplifier

This Note describes an FM tuner that incorporates an MOS field-effect transistor as the rf amplifier, and shows how the MOS transistor is instrumental in minimizing the spurious responses normally found in FM receivers.

AN-3535 ..... 6 pages
An FM Tuner Using Single-Gate MOS Field-Effect Transistors as RF Amplifier and Mixer

Selection of the transistors for use in FM-tuner stages involves consideration of such device characteristics as spurious response, dynamic range, noise immunity, gain, and feedthrough capacitance. MOS field-effect transistors are especially suitable for use in FM rf-amplifier and mixer stages because of their inherent superiority for spurious-response rejection and signal-handling capability. This Note describes an FM tuner that uses an RCA-40468 MOS transistor as the rf amplifier and an RCA-40559 MOS transistor as the mixer.

AN-4018 ..... 5 pages
Design of Gate-Protected MOS Field-Effect Transistors

MOS (metal-oxide-semiconductor) field-effect transistors are in demand for rf-amplifier applications because their transfer characteristics make possible significantly better performance than that experienced with other solid-state devices. Unless equipped with gate protection, however, MOS transistors require careful handling to prevent static discharges from rupturing the dielectric material that separates the gate from the channel. This Note describes the design of dual-gate MOS field-effect transistors that use a built-in signal-limiting diode structure to provide an effective short circuit to static discharge and limit high potential buildup across the gate insulation.

AN-4125 ..... 7 pages
MOS/FET Biasing Techniques

Field-effect transistors are applied in rf amplifiers, and mixers, if and audio amplifiers, electrometer and memory circuits, attenuators, and switching circuits. The dual-gate MOS/FET appears to be particularly useful in rf stages because of low feedback capacitance, high transconductance, and superior cross modulation with automatic-gain-control capability. The rules for biasing FET's vary slightly depending on type. However, most possibilities are covered in this Note through examination of the biasing of a single-gate, a junction-gate, and a dual-gate transistor. Substrate biasing and biasing to compensate for temperature variations are also discussed.

AN-4431 ..... 8 pages
RF Applications of the Dual-Gate MOS/FET Up to 500 MHz

The dual-gate protected, metal-oxide silicon, field-effect transistor (MOS FET) is especially useful for high-frequency applications in rf amplifier circuits. The dual-gate feature permits the design of simple AGC circuitry requiring very low power. The integrated diodes protect the gates against damage due to static discharge that may develop during handling and usage. This Note describes the use of the RCA-3N200 dual-gate MOS FET in rf applications. The 3N200 has good power gain and a low noise factor at frequencies up to 500 MHz, offers especially good cross-modulation performance, and has a wide dynamic range; its low-feedback capacitance provides stable performance without neutralization.

AN-4590 ..... 16 pages
Using MOS/FET Integrated Circuits in Linear Circuit Applications

A brief review of MOS/FET IC device theory is given, and some linear circuit applications are surveyed. Theory discussed includes gate protection and electrical requirements. Applications include choppers, attenuators, constant-current sources, general-purpose amplifier circuits, and rf amplifiers, oscillators, and mixers.

ICAN-4072 ..... 8 pages
Applications of the RCA-CA3048 Integrated-Circuit Amplifier Array

The RCA-CA3048 integrated circuit, an array of four identical amplifiers, each with independent inputs and outputs, all on a single monolithic silicon chip, has an operating and storage temperature range of -25°C to +85°C. Each amplifier in the low-noise array has a typical open-loop gain of 58 dB and input impedance of 90,000 ohms. The gain-frequency response, stability, output swing versus supply voltage, and noise of the device are discussed. Circuit applications include Hartley and Colpitts Oscillators, astable multivibrators, a 4-channel linear mixer, a driver for a 600-ohm balanced line, and a gain-controlled amplifier.

ICAN-5015 ..... 15 pages
Application of the RCA-CA3008 and CA3010 Integrated-Circuit Operational Amplifiers

This Note describes the circuit arrangement, lists the performance characteristics, explains the major design considerations, and discusses typical applications of the CA3008 and CA3010 operational amplifiers. These amplifiers are silicon monolithic integrated circuits designed to operate from two symmetrical low- or medium-level dc power supplies (at supply voltages in the range from +3 volts to +6 volts).

Abstracts of Application Notes (Cont'd)

ICAN-5022 ..... 26 pages
Application of the RCA-CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers

The CA3004, CA3005, and CA3006 rf amplifiers are discussed. These silicon-epitaxial monolithic integrated circuits are designed to operate from low or medium levels of dc supply voltage, over a range of ambient temperatures from -55°C to +125°C, and at frequencies from dc to 100 MHz. They may be used with external tuned-circuit, transformer, or resistive load impedances to provide wide- or narrow-band amplification, mixing, limiting, product detection, frequency generation, and generation of pulse or digital waveforms.

ICAN-5030 ..... 11 pages
Application of the RCA-CA3000 Integrated-Circuit DC Amplifier

This Note describes the RCA-CA3000 dc amplifier, a stabilized and compensated differential amplifier that has push-pull outputs, high-impedance (0.1-megohm) inputs, and gain of approximately 30 dB at frequencies up to one MHz. Its useful frequency response can be increased to several tens of megahertz by the use of external resistors or coils. The CA3000 can be used as a single switch (with pedestal), a squelchable audio amplifier (with suppressed switching transient), a modulator, a mixer or a product detector. When suitable external components are added, it can also be used as an oscillator, a one-shot multivibrator, or a trigger with controllable hysteresis.

ICAN-5036 ..... 9 pages
Application of the RCA-CA3002 Integrated-Circuit IF Amplifier

The RCA-CA3002 integrated-circuit if amplifier described in this Note is a balanced differential amplifier that can be used with either a single-ended or a push-pull input and can provide either a direct-coupled or a capacitance-coupled single-ended output. Its applications include RC-coupled if amplifiers that use the internal silicon output-coupling capacitor, video amplifiers that use an external coupling capacitor, envelope detectors, product detectors, and various trigger circuits.

ICAN-5037 ..... 4 pages
Application of the RCA-CA3007 Integrated-Circuit Audio Amplifier

This Application Note describes the RCA-CA3007 audio driver, a balanced differential configuration with either a single-ended or a differential input and two push-pull emitter-follower outputs. The circuit features all-monolithic silicon epitaxial construction, and is intended for use as a direct-coupled driver in a class B audio amplifier which exhibits both gain and operating-point stability over the temperature range from -55 to +125°C.

ICAN-5038 ..... 8 pages
Application of the RCA-CA3001 Integrated-Circuit Video Amplifier

The CA3001 silicon monolithic integrated circuit is designed for use in intermediate-frequency or video amplifiers at frequencies up to 20 MHz and in Schmitt-trigger applications. This integrated circuit can be gated, and gain control can be applied. The CA3001 incorporates all-monolithic silicon epitaxial construction designed for operation at ambient temperatures from -55 to +125°C, balanced differential-amplifier configuration with low-impedance double-ended input, and a built-in temperature-compensating network for gain or dc operating-point stability over the temperature range from -55 to +125°C.

ICAN-5213 ..... 6 pages
Application of the RCA CA3015 and CA3016 Integrated-Circuit Operational Amplifiers

The integrated-circuit operational amplifiers CA3015 and CA3016 are identical in circuit configuration to the CA3008 and CA3010, but have an improved device breakdown voltage that permits operation from +12-volt supplies as well as from +6-volt or +3-volt supplies. This Note describes the operating characteristics of the CA3015 and CA3016 at +12 volts, and discusses applications that take advantage of the higher gain-bandwidth product and increased output signal swing obtained at the higher voltages: a 50-dB amplifier; a 10-dB, 42-MHz amplifier; a twin-T bandpass amplifier; and a voltage-follower.

ICAN-5269 ..... 7 pages
Integrated Circuits for FM Broadcast Receivers

This Note describes several approaches to FM receiver design using silicon monolithic integrated circuits. The tuner section is described first, and then the if-amplifier and detector sections. Performance characteristics are described where applicable. The FM receivers discussed are designed for use from a +9-volt supply. The key to design simplicity is the use of the RCA multifunction integrated circuits CA3005, CA3012, and CA3014. The CA3005 may be used as a cascode rf amplifier, a differential rf amplifier, a mixer-oscillator, and an if amplifier; the CA3012 and CA3014 perform if amplification, limiting, detection, and preamplification.

ICAN-5296 ..... 5 pages
Application of the RCA-CA3018 Integrated-Circuit Transistor Array

The CA3018 integrated circuit consists of four silicon epitaxial transistors produced by a monolithic process on a single chip mounted in a 12-lead TO-5 package. The four active devices, two isolated transistors plus two transistors with an emitter-base common connection, are especially suitable for applications in which closely matched device characteristics are required, or in which a number of active devices must be interconnected with non-integrable components such as tuned circuits, large-value resistors, variable resistors, and microfarad bypass capacitors. Such areas of application include if, rf (through 100 MHz), video, agc, audio, and dc amplifiers.

ICAN-5299 ..... 6 pages
Application of the RCA-CA3019 Integrated-Circuit Diode Array

The CA3019 integrated-circuit diode array provides four diodes internally connected in a diode-quad arrangement plus two individual diodes. Its applications include gating, mixing, modulating, and detecting circuits. Because all the diodes are fabricated simultaneously on a single silicon chip, they have nearly identical characteristics, and their parameters track each other with temperature variations. Consequently, the CA3019 is particularly useful in circuit configurations that require either a balanced diode bridge or identical diodes.

ICAN-5337 ..... 10 pages
Application of the RCA-CA3028A and CA3028B Integrated-Circuit RD Amplifiers in the HF and VHF Ranges

The CA3028A and CA3028B monolithic-silicon integrated circuits are single-stage differential amplifiers intended for service in communications systems operating at frequencies up to 100 MHz with single power supplies. This Note provides technical data and recommended circuits for use of the CA3028A and CA3028B in rf amplifiers, autodyne converters, if amplifiers, and limiters. The CA3028A and CA3028B are suitable for use in a wide range of applications in dc, audio, and pulse amplifier service; they have been used as sense amplifiers, preamplifiers for low-level transducers, and dc differential amplifiers.

Abstracts of Application Notes (Cont'd)

ICAN-5338 ..... 14 pages
Application of the RCA-CA3021, CA3022, and CA3023 Integrated-Circuit, Wideband Amplifiers

The CA3021, CA3022, and CA3023 integrated circuits are multipurpose high-gain amplifiers designed for use in video and AM or FM if stages in single-power-supply systems. Specifically, they can be used in video amplifiers operating at frequencies through 30 MHz. AM and FM if amplifiers, and buffer amplifiers in which an isolation capability greater than 60 dB at 1 MHz is desired.

ICAN-5380 ..... 7 pages
Integrated-Circuit Frequency-Modulation IF Amplifiers

The discussion in this Note shows that the simplest approach to the use of the CA3012 and CA3028 integrated circuits in FM if-amplifier strips is to replace each stage in present discrete-transistor if strips with a differential amplifier. This integrated-circuit approach requires a minimum of re-engineering because a cascade of individually tuned if stages is used. From a performance point of view, this approach results in better AM rejection than that obtained with discrete circuits because of the inherent limiting achieved with the differential-amplifier configuration.

ICAN-5766 ..... 8 pages
Application of the RCA-CA3020 and CA3020A Integrated-Circuit Multipurpose Wideband Power Amplifiers

The CA3020 and CA3020A integrated circuits are multipurpose, multifunction power amplifiers designed for use as power-output amplifiers and driver stages in portable and fixed communications equipment and in ac servo-control systems. The flexibility of these circuits and the high-frequency capabilities of the circuit components make these types suitable for a wide variety of applications such as broadband amplifiers, video emplifiers, and video line drivers. Voltage gains of 60 dB or more are available, with a 3-dB bandwidth of 8 MHz. Applications covered include audio, wideband, and driver amplifiers.

ICAN-5841 ..... 4 pages
Feedback-Type Volume-Control Circuits for RCA-CA3041 and CA3042 Integrated Circuits

This Note describes feedback-type volume controls for use with RCA-CA3041 and CA3042 integrated circuits in television receivers. In television sets using these integrated circuits, the volume control is often located remote from the amplifier. The long leads required in such a configuration sometimes pick up undesirable signals that, in turn, cause the system to exhibit hum and noise at low volume levels. The proposed feedback-type volume control reduces hum and noise pick-up by reducing the gain of the system rather than the signal level, and thus eliminates the cost of shielding the leads.

ICAN-6048 ..... 12 pages
Some Applications of a Programmable Power Switch/Amplifier

The CA3094 monolithic programmable power switch/amplifier IC consists of a high-gain preamplifier driving a power-output amplifier stage. It can deliver average power of 3 watts or peak power of 10 watts to an external load, and can be operated from either a single or dual power supply. This Note briefly describes the characteristics of the CA3094, and illustrates its use in applications such as class A instrumentations and power amplifiers, class A driver-amplifiers for complementary power transistors, wide-frequency-range power multivibrators, current- or voltage-controlled oscillators, comparators (threshold detectors), voltage regulators, analog timers (long time delays), alarm systems, motor-speed controllers, thyristor-firing circuits, battery-charge regulator circuits, and ground-fault-interrupter circuits.

ICAN-6077 ..... 12 pages
An IC Operational-Transconductance-Amplifier (OTA) with Power Capability

This Note defines the OTA and describes two circuits of this type, the CA3080 and the CA3094. The single, highly linear operational-transconductance-amplifier, the CA3080, because of its extremely linear transconductance characteristics with respect to amplifier bias current, has gained wide acceptance as a gain-control block. The CA3094 improved on the performance of the CA3080 through the addition of a pair of transistors; these transistors extended the current-carrying capability to 300 milliamperes, peak. The CA3094, is useful in an extremely broad range of circuits in consumer and industrial applications; this Note describes only a few of the many consumer applications.

ICAN-6157 ..... 12 pages
Applications of the CA3085-Series Monolithic IC Voltage Regulators

This Note describes the basic circuit of the CA3085-series devices and some typical applications that include a high-current regulator, constant-current regulators, a switching regulator, a negative-voltage regulator, a dual-tracking regulator, high-voltage regulators, and various methods of providing current limiting. A circuit in which the CA3085 is used as a general-purpose amplifier is also shown.

ICAN-6182 ..... 32 pages
Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3058, CA3059, and CA3079)

CA3058, CA3059, and CA3079 zero-voltage switches are monolithic integrated circuits designed primarily for use as trigger circuits for thyristors in many highly diverse ac power-control and power-switching applications. This Note discusses the operation and application of these circuits.

ICAN-6247 ..... 8 pages
Application of the CA3126Q Chroma-Processing IC Using Sample-and-Hold Circuit Techniques

This Note describes the CA3126Q monolithic integrated circuit intended for use in processing the chrominance signal in a color television receiver. In performing the functions of color subcarrier regeneration and chroma control, emphasis has been placed on utilizing all the information available in the signal so as to approach ultimate system performance capability, while at the same time substantially reducing the number of external components and adjustments.

ICAN-6257 ..... 8 pages
Application of the CA3089E FM-IF Subsystem

The CA3089E, is an FM-IF subsystem intended for use in FM receiver applications. In addition to the amplifier-limiter and quadrature detector sections, the CA3089E provides such auxiliary functions as mute, AFC output, tuning-meter output, and delayed rf-AGC. This Note briefly describes each circuit section and discusses practical aspects of designing with this device.

ICAN-6259 ..... 10 pages
Integrated-Circuit Stereo Decoder Using the CA3090AQ Stereo Multiplex Demodulator

The CA3090AQ integrated circuit provides features heretofore unavailable to the receiver designer. This device needs only a single tuning adjustment, which reduces to a minimum the manual effort during assembly; the phase-locked loop maintains performance under conditions of temperature variations, humidity, and aging. The compactness of the CA3090AQ and of the required external components, added to the other attributes, makes this stereo decoder a significant advancement in the state of the art of stereo decoder designs.

Abstracts of Application Notes (Cont'd)

ICAN-6302 ..... 9 pages
Description and Application of the RCA-CA3120E Integrated-Circuit TV-Signal Processor

The CA3120E is a 16-pin, dual-in-line monolithic-silicon integrated circuit that processes a video signal and provides the following outputs: non-inverted video output; noise-processed, inverted video output; dual-polarity, composite synchronization signals; and automatic gain-control signals (agc). The IC, which can be used in color or monochrome TV receivers, requires a single-polarity power supply (positive) and includes impulse-noise inversion and delay circuits that reduce the deleterious effects of impulse noise in the receiver agc and synchronization (sync) circuits. Standard agc strobing techniques are also used. The agc and impulse-noise thresholds are automatically set and require no controls. The if maximum-gain bias and the tuner agc delay may be adjusted for optimum TV-receiver performance; the time constant for the sync-separator input can also be optimized by the set designer.

ICAN-6303 ..... 16 pages
A Single IC for the Complete PIX-IF-System in TV Receivers

The CA3068 linear integrated circuit is a PIX-IF-sybsystem in a shielded, quad-formed, dual-in-line, 20-lead, plastic package. This package contains all the active devices and most of the passive elements necessary for a high performance, PIX-IF-system for a TV receiver. This Note describes the receiver functions performed by the CA3068, and its application to color and monochrome TV receivers.

ICAN-6668 ..... 16 pages
Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers

The CA3080 and CA3080A are similar in generic form to conventional operational amplifiers, but differ sufficiently to justify an explanation of their characteristics. This class of operational amplifier includes not only the usual differential input terminals, but an additional control terminal that enhances the device's flexibility. This Note describes the operation of the OTA and features various circuits using it. For example, communications and industrial applications, including modulators, multiplexers, sample-and-hold circuits, gain control circuits and micropower comparators, are shown and discussed. These circuits show the operation of the OTA in conjunction with CMOS devices as post-amplifiers.

ICAN-6728 ..... 8 pages
Application of the CA3134E Sound IF and Output Subsystems in Television Receivers

In the CA3134, the sound IF and audio output subsystems for color or black-and-white television receivers are combined in a single monolithic integrated circuit. The consolidation of these functions into an integrated circuit minimizes the number of components needed and reduces the area of the printed-circuit board necessary for this portion of a television receiver. This consolidation also permits a reduction in manufacturers' component inventories and simplifies field servicing. Circuit characteristics, functions, and applications are discussed.

ICAN-6732 ..... 8 pages
Measurement of Burst ("Popcorn") Noise in Linear Integrated Circuits

The advent in recent years of very high-gain operational amplifiers operating in the 1/f noise-frequency spectrum has placed emphasis on the need for very low-noise devices. This need is particularly true for operational amplifiers which have either low-offset characteristics and/or offset-null capability.

The traditional methods used to select very-low-noise devices for operational amplifiers involve the measurement of either spot or wideband (≈10 kHz) noise figures in the 1/f frequency range (10 Hz to 10 kHz) at various source resistances. This type of measurement, however, only provides an indication of the average noise power at the measurement frequency and does not reveal the burst ("popcorn") noise characteristics of the Device Under Test (DUT). This Note describes in detail a test that will detect burst noise.

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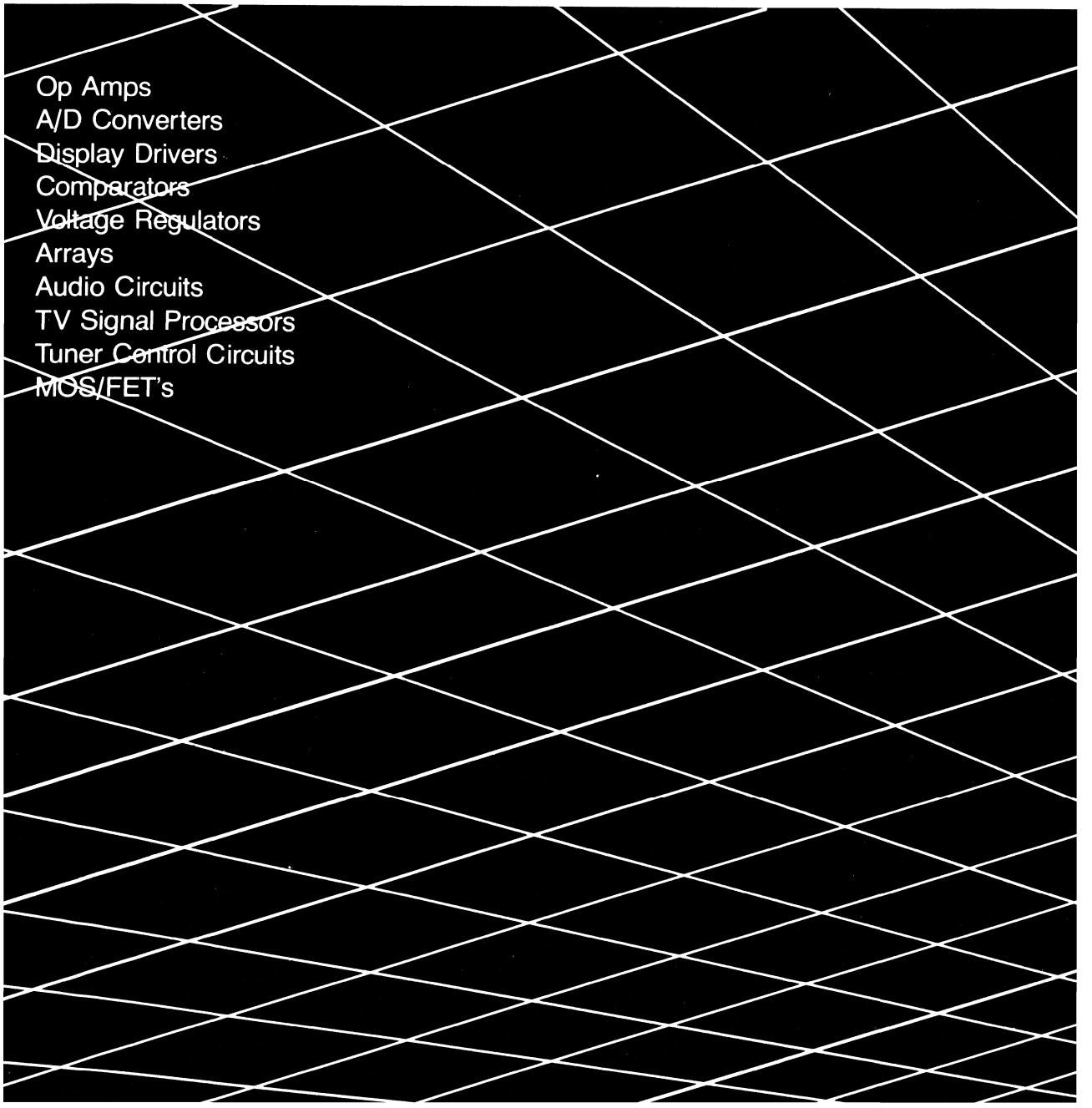
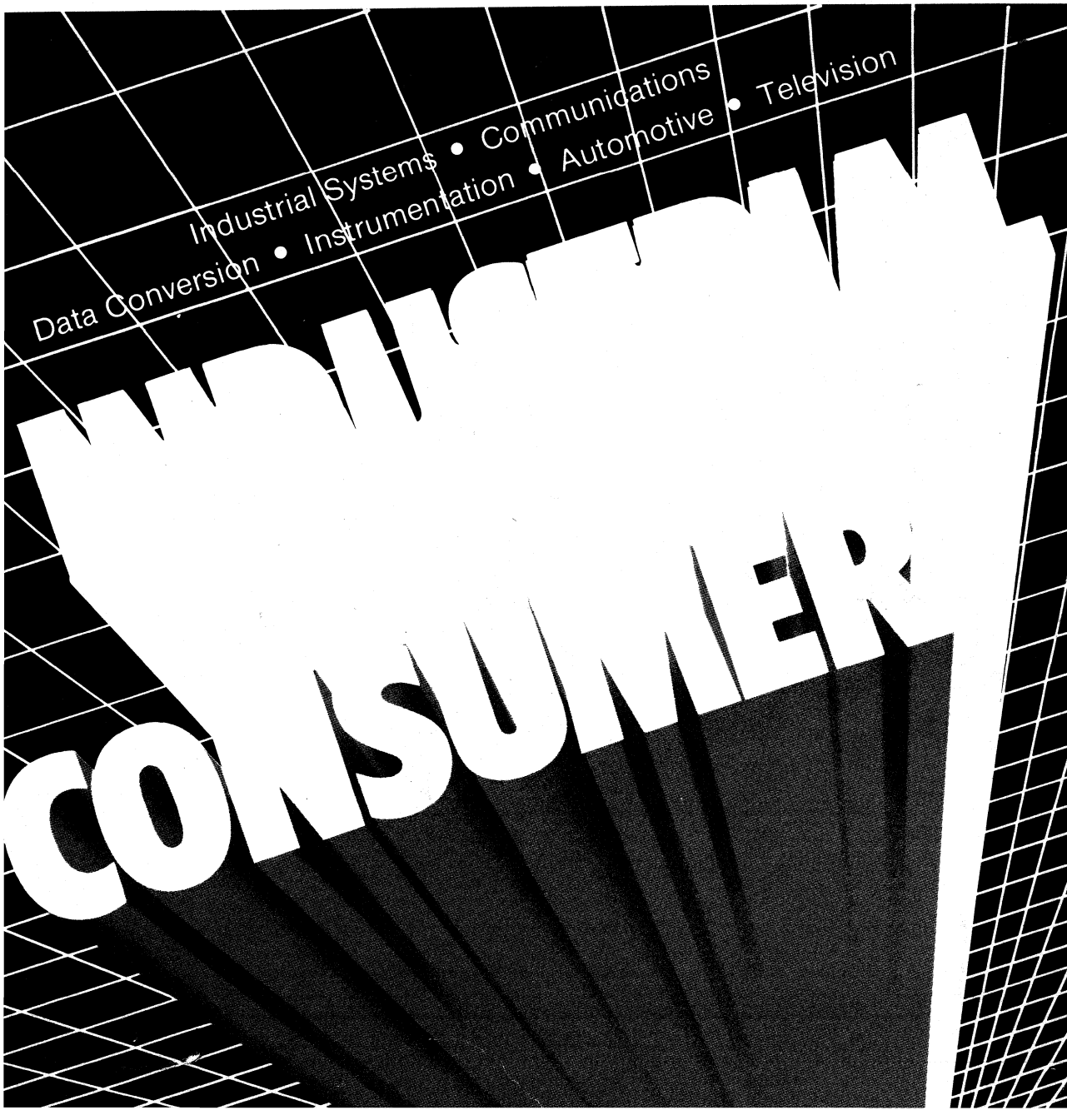


RCA Solid State

Linear Integrated Circuits
and MOS/FET's



RCA Linear Integrated Circuits
and MOS/FET's

This DATABOOK contains detailed technical information on the full line of linear integrated circuits and the low-power line of metal-oxide-semiconductor field-effect transistors (MOS/FET's) currently available from RCA Solid State Division. This broad spectrum of products includes many highly diverse types intended for a wide range of circuit functions in industrial and/or consumer applications.

The first section, a general over-all guide to available products, contains a complete index of types, photographs of the wide variety of package options, product classification and selection guides, recommended operating and handling procedures, a list of special terms and symbols, and a cross-reference listing that shows the recommended RCA replacement types for many popular industry devices. This general section is followed by technical data on individual types grouped into eleven broad product categories, including: Operational Amplifiers, Voltage Comparators, Data-Conversion Circuits, Arrays, Power Control Circuits, Differential Amplifiers, Special-Function Circuits, Audio Circuits, Radio Circuits, and MOS/FET's. The first page of each data section lists all the types included in the section grouped according to specific circuit functions together with a reference to the page that contains the technical data for each type.

The final section of the DATABOOK lists high-reliability types supplied for military, aerospace, and critical industrial applications and defines the screening levels to which each of them are supplied, shows dimensional outlines for all package types, and lists, together with a brief abstract, current RCA application notes on linear integrated circuits and MOS/FET's.

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General Guide to Linear Integrated Circuits

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CA201	T	S	—	—	—	—	786	28
CA224	E	—	—	—	—	—	796	104
CA239	E	—	—	—	—	—	795	301
CA239A	E	—	—	—	—	—	795	301
CA258	T	S	E	—	—	—	1019	93
CA258A	T	S	E	—	—	—	1019	93
CA301A	T	S	E	—	H	—	786	28
CA307	T	S	E	—	H	—	785	34
CA311	T	S	E	—	—	—	797	270
CA324	E	—	H	—	—	—	796	104
CA339	E	—	H	—	—	—	795	301
CA339A	E	—	—	—	—	—	795	301
CA358	T	S	E	H	—	—	1019	93
CA358A	T	S	E	—	—	—	1019	93
CA555	T	S	E	—	—	—	834	653
CA555C	T	S	E	—	H	—	834	653
CA723	T	E	—	—	—	—	788	520
CA723C	T	E	H	—	—	—	788	520
CA741	T	S	E	—	—	—	531	38
CA741C	T	S	E	—	H	—	531	38
CA747	T	E	—	—	—	—	531	38
CA747C	T	E	—	H	—	—	531	38
CA748	T	S	E	—	—	—	531	38
CA748C	T	S	E	—	H	—	531	38
CA1458	T	S	E	—	H	—	531	38
CA1524	E	—	—	—	—	H	1239	528
CA1558	T	S	E	—	—	—	531	38
CA1724	E	—	—	—	—	—	1228	393
CA1725	E	—	—	—	—	H	1228	393
CA2002	★	M	—	—	—	—	1156	660
CA2004	★	M	—	—	—	—	1105	665
CA2524	E	—	—	—	—	H	1239	528
CA2904	T	E	—	—	—	—	1019	93
CA3000	■	H	—	—	—	—	121	562
CA3001	■	H	—	—	—	—	122	569
CA3002	■	H	—	—	—	—	123	612
CA3004	■	H	—	—	—	—	124	575
CA3005	■	H	—	—	—	—	125	581
CA3006	■	—	—	—	—	—	125	581
CA3007	■	—	—	—	—	—	126	588
CA3008	‡‡	—	—	—	—	—	316	114
CA3008A	‡‡	—	—	—	—	—	316	121
CA3010	■	—	—	—	—	—	316	114
CA3010A	■	—	—	—	—	—	310	121
CA3015	■	—	H	—	—	—	316	114
CA3015A	■	—	—	—	—	—	310	121
CA3016	‡‡	—	—	—	—	—	316	114
CA3016A	‡‡	—	—	—	—	—	310	121
CA3018	■	—	H	—	—	—	338	396
CA3018A	■	—	—	—	—	—	338	396

Type Number	Package Suffix						Data Bulletin File No.	Page
CA3019	■	H	—	—	—	—	236	384
CA3020	■	H	—	—	—	—	339	500
CA3020A	■	—	—	—	—	—	339	500
CA3021	■	—	—	—	—	—	243	129
CA3022	■	—	—	—	—	—	243	129
CA3023	■	H	—	—	—	—	243	129
CA3026	■	H	—	—	—	—	338	354
CA3028A	■	S	—	—	H	—	382	593
CA3028B	■	S	—	—	—	—	382	593
CA3029	•	—	—	—	—	—	316	114
CA3029A	•	—	—	—	—	—	310	121
CA3030	•	—	—	—	—	—	316	114
CA3030A	•	—	—	—	—	—	310	121
CA3035	■	VI	H	—	—	—	274	362
CA3036	■	—	—	—	—	—	275	402
CA3037	†	—	—	—	—	—	316	114
CA3037A	†	—	—	—	—	—	310	121
CA3038	†	—	—	—	—	—	316	114
CA3038A	†	—	—	—	—	—	310	121
CA3039	■	—	H	—	—	—	343	386
CA3040	■	—	—	—	—	—	363	604
CA3045	†	F	—	H	—	—	341	404
CA3046	•	—	—	—	—	—	341	404
CA3048	•	H	—	—	—	—	377	365
CA3049	T	—	H	—	—	—	611	372
CA3050	†	—	—	—	—	—	361	410
CA3051	•	—	—	—	—	—	361	410
CA3052	•	—	—	—	—	—	387	377
CA3053	■	S	—	—	—	—	382	593
CA3054	•	—	H	—	—	—	388	354
CA3058	†	—	—	—	—	—	490	550
CA3059	•	H	—	—	—	—	490	550
CA3060	D	E	H	—	—	—	537	224
CA3060A	D	—	—	—	—	—	537	224
CA3060B	D	—	—	—	—	—	537	224
CA3075	Δ	H	—	—	—	—	429	670
CA3076	■	H	—	—	—	—	430	674
CA3078	T	S	E	H	—	—	535	237
CA3078A	T	S	E	H	—	—	535	237
CA3079	•	—	—	—	—	—	490	550
CA3080	■	E	S	H	—	—	475	245
CA3080A	■	E	S	—	—	—	475	245
CA3081	•	F	H	—	—	—	480	332
CA3082	•	F	H	—	—	—	480	332
CA3083	•	F	—	H	—	—	481	418
CA3084	•	—	H	—	—	—	482	422
CA3085	■	E	S	—	H	—	491	543
CA3085A	■	S	E	—	—	—	491	543
CA3085B	■	S	—	—	—	—	491	543
CA3086	•	F	—	—	—	—	483	427
CA3088	E	—	—	—	—	—	560	678
CA3089	E	—	—	—	—	—	561	682
CA3091	D	H	—	—	—	—	534	618
CA3093	E	H	—	—	—	—	533	432
CA3094	T	S	E	H	—	—	598	213
CA3094A	T	S	E	—	—	—	598	213
CA3094B	T	S	—	—	—	—	598	213
CA3096	E	H	—	—	—	—	595	438
CA3096A	E	—	—	—	—	—	595	438
CA3096C	E	—	—	—	—	—	595	438
CA3097	E	H	—	—	—	—	633	448

Index to Devices

Type Number	Package Suffix						Data Bulletin File No.	Page
CA3098	T	S	E	H	—	—	896	278
CA3099	E	H	—	—	—	—	620	285
CA3100	T	S	E	H	—	—	625	135
CA3102	E	H	—	—	—	—	611	372
CA3105	★	M	—	—	—	—	1382	46
CA3118	T	H	—	—	—	—	532	459
CA3118A	T	—	—	—	—	—	532	459
CA3123	E	—	—	—	—	—	631	688
CA3127	E	—	—	—	—	—	662	466
CA3128	Q	—	—	—	—	—	1161	471
CA3130	T	S	E	H	—	—	817	141
CA3130A	T	S	E	—	—	—	817	141
CA3130B	T	S	—	—	—	—	817	141
CA3138	E	H	—	—	—	—	1131	473
CA3138A	E	—	—	—	—	—	1131	473
CA3140	T	S	E	H	—	—	957	156
CA3140A	T	S	E	—	—	—	957	156
CA3140B	T	S	—	—	—	—	957	156
CA3141	E	—	—	—	—	—	906	390
CA3146	E	H	—	—	—	—	532	459
CA3146A	E	—	—	—	—	—	532	459
CA3152	E	—	—	—	—	—	1351	48
CA3160	T	S	E	H	—	—	976	176
CA3160A	T	S	E	—	—	—	976	176
CA3160B	T	S	—	—	—	—	976	176
CA3161	E	—	—	—	—	—	1079	335
CA3162	E	—	—	—	—	—	1080	308
CA3164	E	—	—	—	—	—	1139	647
CA3165	E	E1§	—	—	—	—	1278	494
CA3168	E	—	—	—	—	—	1140	339
CA3169	★	M	—	—	—	—	1277	508
CA3179	E	—	—	—	—	H	1176	630
CA3183	E	H	—	—	—	—	532	459
CA3183A	E	—	—	—	—	—	532	459
CA3189	E	—	—	—	—	—	1046	692
CA3193	T	S	E	H	—	—	1249	52
CA3193A	T	S	E	H	—	—	1249	52

Type Number	Package Suffix						Data Bulletin File No.	Page
CA3193B	T	S	E	H	—	—	1249	52
CA3199	E	—	—	—	—	—	1302	639
CA3207	E	H	—	—	—	—	1322	343
CA3208	E	H	—	—	—	—	1322	343
CA3209	E	—	—	—	—	—	1343	698
CA3211	E	—	—	—	—	—	1379	644
CA3219	E	—	—	—	—	—	1359	514
CA3227	E	—	—	—	—	—	1345	476
CA3228	E	—	—	—	—	—	1346	517
CA3240	E*	E1§	—	—	—	—	1050	193
CA3240A	E*	E1§	—	—	—	—	1050	193
CA3246	E	—	—	—	—	—	1345	476
CA3260	T	S	E	H	—	—	1266	208
CA3260A	T	S	E	H	—	—	1266	208
CA3260B	T	S	E	H	—	—	1266	208
CA3280	E	—	—	—	—	H	1174	260
CA3280A	E	—	—	—	—	H	1174	260
CA3290	T	S	E*	E1§	—	—	1049	291
CA3290A	T	S	E*	E1§	—	—	1049	291
CA3290B	T	S	—	—	—	—	1049	291
CA3300	D	H	—	—	—	—	1316	316
CA3308	D	—	—	—	—	—	1352	327
CA3401	E	—	H	—	—	—	630	110
CA3420	S	T	E	H	—	—	1320	63
CA3420A	S	T	E	H	—	—	1320	63
CA3420B	S	T	E	H	—	—	1320	63
CA3440	S	T	E	H	—	—	1318	254
CA3440A	S	T	E	H	—	—	1318	254
CA3440B	S	T	E	H	—	—	1318	254
CA3493	S	T	E	—	—	—	1290	68
CA3493A	S	T	E	—	—	—	1290	68
CA3493B	S	T	E	—	—	—	1290	68
CA3524	E	—	—	—	—	H	1239	528
CA3600	E	—	—	—	—	—	619	479
CA6078A	T	S	—	—	—	—	592	79
CA6741	T	S	—	—	—	—	592	79

■ No designated suffix letter for this type in TO-5 style package

‡‡ No designated suffix letter for this type of ceramic flat package

• No designated suffix letter for this type in dual-in-line plastic package

† No designated suffix letter for this type in dual-in-line ceramic package

Δ No designated suffix letter for this type in quad-in-line plastic package

* In 8-lead dual-in-line Mini-DIP package

§ In 14-lead dual-in-line plastic package

★ No designated suffix letter for this type in TO-220-style package with vertical-mount lead form.

Packages

RCA linear device packages are identified by letters as indicated in the following chart. When ordering a Linear device, it is important that the appropriate suffix letter(s) be affixed to the type number of the device.

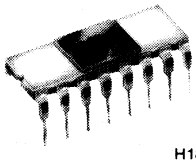
Package	Suffix Letter
Dual-In-Line Welded-Seal Ceramic Package	D
Dual-In-Line Plastic Package	E
Dual-In-Line Frit-Seal Ceramic Package	F
Chip	H
Dual-In-Line Plastic Package with "Power Slab"	P
Modified Dual-In-Line Plastic Package with "Power Slab"	EM
Modified Quad-In-Line Plastic Package	QM
Quad-In-Line Plastic Package	Q
TO-5 Style Package with Dual-In-Line Formed Leads (DIL-CAN)	S
TO-5 Style Package with Straight Leads	T
TO-220 Style Package with Horizontal-Mount Lead Form	M
TO-5 Style Package with Radial Formed Leads	V1
Staggered Quad-In-Line Plastic Package	W
Ceramic Flat Package	K

Notes:

1. Some types may have an additional "M" suffix following the package designation suffix, i.e., CA3134EM. The additional "M" suffix simply indicates that the device is a mechanical variant of the basic package type.

2. RCA linear integrated circuits are provided in chip form to allow customer design of special and complex circuits to suit individual needs. Linear chips are electrically identical to and offer the features of their counterparts, sealed in ceramic, TO-5, and plastic packages. The package-options charts shown with the functional diagrams for each generic type of RCA linear integrated circuit indicate those types for which chip versions are available.

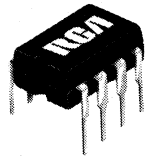
D Suffix
Dual-In-Line Welded-Seal Ceramic Package



H1844

14 and 16-lead versions

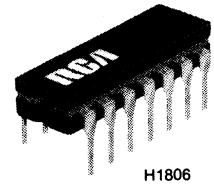
E Suffix
Dual-In-Line Plastic Package



H1817

8, 14, 16, 18, 22, 24 and 28-lead versions

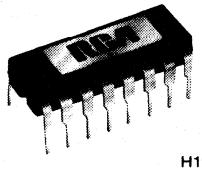
F Suffix
Dual-In-Line Frit-Seal Ceramic Package



H1806

14 and 16-lead versions

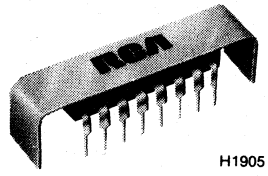
P Suffix
"Power Slab" Plastic Dual-In-Line Package



H1902

CA3136P only

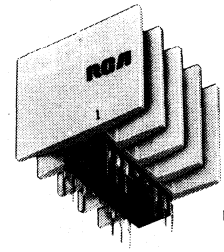
EM Suffix
Modified 16-lead Dual-In-Line Plastic Package with "Power Slab"



H1905

CA3134EM only

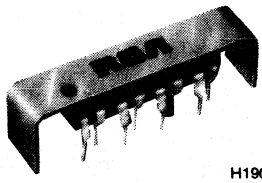
EM Suffix
Modified 16-lead Dual-In-Line Plastic Package with "Power Slab"



H1827

Packages (Cont'd)

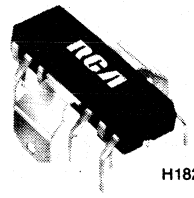
QM Suffix
Quad-In-Line Plastic Package (QUIP) with "Power Slab"



H1906

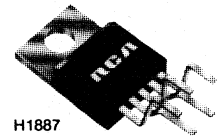
16-lead version

Q Suffix
Modified 16-lead QUIP



H1825

VERSA-V and VERSA-V1 TO-220 Style Plastic Package with Vertical-Mount Lead Form



H1887

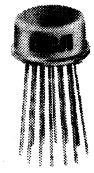
(Versions with horizontal-mount lead form are also available).

S Suffix
TO-5 Style Package with Dual-In-Line Formed Leads (DIL-CAN)

H1787

8-lead version

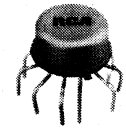
T Suffix
TO-5 Style Package with Straight Leads



H1463

8, 10, and 12-lead versions

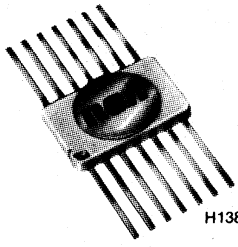
V1 Suffix
TO-5 Style Package with Radial Formed Leads



H1561

8, 10, and 12-lead versions

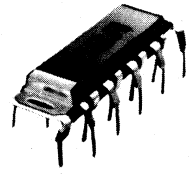
K Suffix
Ceramic Flat Package



H1383R1

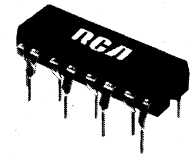
14-lead version

Shielded 20-lead Quad-In-Line Plastic Package



H1704

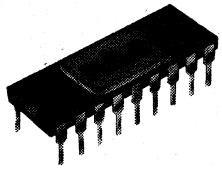
W Suffix
Staggered Quad-In-Line Plastic Package



H1885.

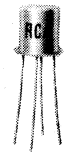
14 and 16-lead versions

D Suffix
18-lead Dual-In-Line Side-Brazed Ceramic Package



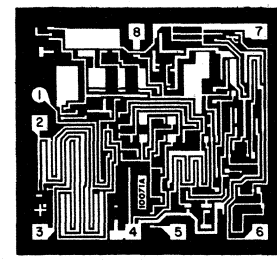
H1910

JEDEC TO-72



H1299

H Suffix
Chip



92CM-32235

Product Classification Chart

Industrial Circuits

OPERATIONAL AMPLIFIERS

General Purpose

Single Unit	Dual Unit
CA101	CA082*
CA201	CA083*
CA301A	CA158
CA307	CA258
CA741	CA358
CA748	CA747
CA3105	CA1458
CA3152*	CA1558
CA3193*	CA2904
CA3420*	Quad Unit
CA3493*	CA084*
CA6741•	CA124
	CA224
	CA324
	CA3401

General Purpose Wideband

Single Unit
CA080*
CA081*
CA3008
CA3010
CA3015
CA3016
CA3029
CA3030
CA3037
CA3038
CA3100*
CA3130*
CA3140*
CA3160*
Dual Unit
CA3240*
CA3260*

Variable

High Current
CA3094
Micropower
CA3060
CA3078
CA3080
CA3440*
CA6078A•
Dual Unit
CA3280

DIFFERENTIAL AMPLIFIERS

CA3000
CA3001
CA3004
CA3005
CA3006
CA3007
CA3026
CA3028
CA3040
CA3049
CA3050
CA3051
CA3053
CA3054
CA3102

ARRAYS

Amplifier/Diode

Amplifier
CA3026
CA3035
CA3048
CA3049
CA3052
CA3054
CA3060
CA3102
Diode
CA3019
CA3039
CA3141

Transistor

CA1724	CA3096
CA1725	CA3097
CA3018	CA3118
CA3036	CA3127
CA3045	CA3128
CA3046	CA3138
CA3050	CA3146
CA3051	CA3183
CA3081	CA3227
CA3082	CA3246
CA3083	▲CA3600
CA3084	
CA3086	
CA3093	

POWER CONTROL CIRCUITS

Voltage Regulators	Solenoid & Motor Drivers
CA723	CA3169
CA1524	CA3219
CA2524	
CA3085	Power Amplifiers
CA3524	CA3020
	CA3105
Zero-Voltage Switches	
CA3058	Automotive Ignition Switch
CA3059	CA3165
CA3079	
Programmable Schmitt Triggers	Universal Controller
CA3098	CA3228
CA3099	

DATA CONVERSION

A/D Converters	
CA3162	
CA3300	
CA3308	
Display Drivers	
CA3161	CA3081
CA3168	CA3082
CA3207*	
CA3208*	

VOLTAGE COMPARATORS

Single Unit
CA311
CA3098+
CA3099+
Dual Unit
CA3290*
Quad Unit
CA139
CA239
CA339

SPECIAL FUNCTION CIRCUITS

Timer	Automotive Circuits	Broadband (Video) Amplifiers
CA555	CA3105	CA080*
	CA3130*	CA081*
Four Quadrant Multiplier	CA3160*	CA082*
CA3091	CA3161	CA083*
	CA3165	CA084*
Single-Chip Detector Alarm	CA3168	CA3001
Systems	CA3169	CA3002
CA3164*	**CA3207***	CA3020
	CA3208*	CA3021
Prescalers	CA3219	CA3022
CA3179	CA3228	CA3023
CA3199	CA3260*	CA3040
CA3211	CA3290*	CA3071
		CA3100*
		CA3130*
		CA3140*
		CA3160*
		CA3240*
		CA3260*

MOS/FET's

Single Gate		Dual Gate		Dual Gate Protected	
3N128	3N153	3N140	40600	3N187	40673
3N138	3N154	3N141	40601	3N200	40819
3N139	40467A	3N159	40602	3N204	40820
3N142	40468A		40603	3N205	40821
3N143	40559A		40604	3N206	40822
3N152				3N211	40823
				3N212	40841
				3N213	

•Low-noise versions of CA741 and CA3078 *BiMOS types ▲CMOS types +Programmable

Product Classification Chart

Consumer Circuits

AUDIO CIRCUITS	RADIO CIRCUITS		MOS/FET's		
Drivers	AM/FM Com-	FM IF	Single Gate	Dual Gate	Dual Gate
CA3094	munications	Circuits	3N128	3N140	Protected
	Circuits	Gain Blocks	3N138	3N141	3N187
Power	CA3075	CA3076	3N139	3N159	3N200
Amplifiers	CA3076		3N142	40600	3N204
CA2002	CA3088	Subsystems	3N143	40601	3N205
CA2004	CA3089	CA3075	3N152	40602	3N206
	CA3123	CA3089	3N153	40603	3N211
Preamplifiers	CA3143	CA3189	3N154	40604	3N212
CA3036	CA3179	CA3209	40467A		3N213
CA3048	CA3189		40468A		40673
CA3052	CA3199		40559A		40819
	CA3209				40820
					40821
					40822
					40823
					40841

Operating and Handling Considerations

Solid state devices are being designed into an increasing variety of electronic equipment because of their high standards of reliability and performance. However, it is essential that equipment designers be mindful of good engineering practices in the use of these devices to achieve the desired performance.

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of linear integrated circuits and MOS field-effect transistors.

The ratings included in RCA data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

The design flexibility provided by integrated circuits and MOS/FET's makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of these devices provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

MOUNTING

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with gold or nickel plated Kovar leads.* It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress. The aluminum-foil-lined cardboard "sandwich pack" employed for static protection of the flat-pack also provides some additional protection against lead corrosion, and it is recommended that the devices be stored in this package until used.

When integrated circuits are welded onto printed circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

MOS FIELD-EFFECT TRANSISTORS

Insulated-Gate Metal Oxide-Semiconductor Field-Effect Transistors (MOS FETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in an MOS FET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applica-

* MIL-38510A, paragraph 3.5.6.1(a), lead material.

tions, with virtually no problems of damage due to electrostatic discharge.

In some MOS FETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOS FETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

*Trade Mark: Emerson and Cumming, Inc.

Operating and Handling Considerations

SOLID STATE CHIPS

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

Terms and Symbols

A	closed-loop voltage gain
A_{AF}	audio amplifier gain
A_{DIFF}	differential voltage gain
ACC	automatic chroma control
AFC	automatic frequency control
AFT	automatic fine tuning
AGC	automatic gain control
AMR	am rejection
A_{OL}	open-loop voltage gain
A_V	amplifier voltage gain
b_{fs}	small-signal, common-source, forward transfer susceptance (imaginary part of corresponding admittance; see y_{fs})
b_{is}	small-signal, common-source, input susceptance (imaginary part of corresponding admittance; see y_{is})
b_{os}	small-signal, common-source, output susceptance (imaginary part of corresponding admittance, see y_{os})
b_{rs}	small-signal, common-source, reverse transfer susceptance (imaginary part of corresponding admittance, see y_{rs})
BW	bandwidth (unity gain)
BW_{OL}	open-loop bandwidth
C_{BI}	base-to-substrate capacitance
C_{CB}	collector-to-base capacitance
C_{EB}	emitter-to-base capacitance
C_{EXT}	external capacitance
C_{FB}	feedback capacitance
C_I	input capacitance
C_{ios}	small-signal output capacitance
C_{is}	small-signal input capacitance
C_{iss}	small-signal, common-source short-circuit input capacitance
C_{I-O}	input-to-output capacitance; data in/out capacitance
CMMR	common-mode rejection ratio
C_O	output capacitance
C_{os}	feedthrough capacitance
C_{oss}	small-signal, common-source short-circuit output capacitance
C_{QP}	charge-pump capacitance
C_{rss}	small-signal, common-source short-circuit, reverse transfer capacitance
e_i	input sensitivity
E_N	I/F noise voltage
e_N	low-frequency noise voltage; equivalent short-circuit input noise voltage ($\mu V\sqrt{Hz}$)
$e_{N(total)}$	wideband noise voltage referenced to input
e_{O1}/e_{O2}	channel separation
E_{ON}	broadband output noise voltage
f_{CL}	clock input frequency
f_{max}	maximum operating frequency
f_p	charge-pump input-pulse frequency
f_t	unity-gain crossover frequency; gain-bandwidth product
f_ϕ	input-pulse frequency
G_p	power gain
G_m	forward transconductance (large-signal)
h_{FE}	static forward-current transfer ratio (beta)
h_{fe}	small-signal forward-current transfer ratio
I^+	dc supply current
I^-	dc supply current
I_A	amplifier supply current
I_{ABC}	amplifier bias current
I_{AGC}	AGC source current
I_B	base current
I_C	collector current
I_{CBO}	collector cutoff current
I_{CEO}	collector cutoff current
$I_{CE(OFF)}$	output leakage current
I_D	drain current
$I_{D(ON)}$	dc on-state drain current
I_{DARK}	dark current
I_{DF}	diode forward current
I_{DDO}	supply current for drain supply voltage (V_{DD})
I_{DS}	zero-gate (bias) drain current (dual-gate types)
I_{DSS}	zero-gate (bias) drain current (single-gate types)
I_F	forward current
I_G	channel (input) gate lead current
I_{GR}	channel (input) gate reverse current
I_{GS}	gate terminal current (single-gate types)
I_{G1S}	gate-No.1 terminal current dual-gate types
I_{G2S}	gate-No. 2 terminal current dual-gate types
I_{GSSF}	gate-to-source forward leakage current, all other terminals shorted to source (dual-gate types).
I_{G1SSF}	gate-No.1 source forward leakage current, all other terminals shorted to source (dual-gate types).
I_{G2SSF}	gate-No. 2-to-source forward leakage current, all other terminals shorted to source (dual-gate types).
I_{GSSR}	gate-to-source reverse leakage current, all other terminals shorted to source (single-gate types).
I_{G1SSR}	gate-No. 1-to-source reverse leakage current, all other terminals shorted to source (dual-gate types).
I_{G2SSR}	gate-No.2-to-source reverse leakage current, all other terminals shorted to source (dual-gate types).
I_{GT}	gate trigger current; gate terminal current
I_I	input current
I_{IB}	input bias current
I_{IBC}	internal bias current
I_{IO}	input offset current
αI_{IO}	average temperature coefficient of input offset current
$\Delta I_{IO}/\Delta T$	temperature coefficient of input offset current (drift)
I_{LIM}	short-circuit limiting current
I_{MTR}	current-mirror transfer ratio
I_N	I/F noise current
i_N	equivalent open-circuit noise current ($pA/\sqrt{Hz}$)
I_O	output current
$I_{O(DIFF)}$	differential output current (sink)
I_{OO}	output offset current
I_{OL}	output leakage current, low
I_{OM}	peak output current
$\lvert I_{OM}\rvert$	magnitude of peak output current
I_{OM}^+	maximum output current (source)
I_{OM}^-	maximum output current (sink)
I_p	photo current
I_{p-p}	peak-to-peak output current
I_Q	total quiescent current
I_{QPL}	charge-pump input current
I_R	dc reverse (leakage) current
I_{REFO}	supply current for reference supply voltage
I_{SSO}	strobe load current voltage (V_{SS})
I_{SXO}	supply current for supply voltage
I_{TH}	threshold current
I_{TOTAL}	total supply current
k_N	normalized factor ($k_N = k/k_r$)
MAG	maximum available power gain
MUG	maximum useable power gain (unneutralized)
NF	noise factor
P_O	power output
P_D	device dissipation
P_{SRR}	power supply rejection ratio
$r_{ds(off)}$	small-signal drain-to-source off-state resistance
$r_{ds(on)}$	static drain-to-source on-state resistance
R_{GS}	gate leakage-current resistance
R_O	output resistance
R_o	low-frequency output resistanc
r_o	small-signal output resistance
r_{oss}	small-signal, short-circuit, common-source output resistance
R_I	differential input resistance
r_i	small-signal input resistance
r_{iss}	small-signal, short-circuit, common-source input resistanc
R_i	low-frequency input resistance
R_{ON}	ON resistance; the ON-state resistance of an analog switch at specified input and load conditions.
ΔR_{ON}	ΔON resistance; the difference in ON-state resistance between any 2 analog switches at specified input and load conditions.
S/N	signal-to-noise ratio
SR	slew rate
T_A	ambient temperature
t_d	delay time
t_{DR}	differential recovery time
t_f	fall time
$t_{f\phi}$	input-pulse rise time
THD	total harmonic distortion
t_{off}	turn-off time
t_{on}	turn-on time
t_r	rise time
$t_{R\phi}$	input-pulse rise time
t_{rr}	reverse recovery time
t_S	setup time
t_{STG}	storage time
t_W	pulse width
V^+	DC positive supply voltage
V^-	DC negative supply voltage
V_{ABC}	amplifier bias voltage
V_{BB}	substrate voltage
V_{BE}	base-to-emitter voltage

Terms and Symbols

$V_{BE(sat)}$	base-to-emitter saturation voltage
$V_{(BR)CBO}$	collector-to-base breakdown voltage
$V_{(BR)CES}$	collector-to-emitter breakdown voltage
$V_{(BR)DI}$	dc breakdown voltage between diode and substrate
$V_{(BR)R}$	dc reverse breakdown voltage
$V_{(BR)EBO}$	emitter-to-base breakdown voltage
$V_{(BR)GSSF}$	dc gate-to-source forward breakdown voltage, all other terminals shorted to source (single-gate types)
$V_{(BR)G1SSF}$	dc gate-No.1-to-source forward breakdown voltage, all other terminals shorted to source (dual-gate types)
$V_{(BR)G2SSF}$	dc gate No.2-to-source forward breakdown voltage, all other terminals shorted to source (dual-gate types)
$V_{(BR)GSSR}$	dc gate-to-source reverse breakdown voltage, all other terminals shorted to source (single-gate types)
$V_{(BR)G2SSR}$	dc gate-No.2-to-source reverse breakdown voltage, all other terminals shorted to source (dual-gate types)
V_{CBO}	collector-to-base voltage
V_{CC}	drain supply voltage used as a second positive supply voltage. It is $\leqslant V_{DD}$ and referenced to V_{SS}
VCO	voltage controlled oscillator
V_{CEO}	collector-to-emitter voltage
$V_{CEO(sus)}$	collector-to-emitter sustaining voltage
V_{CIO}	collector-to-substrate voltage
V_{CP}	charge pump voltage
V_{DD}	drain supply voltage (the most positive supply voltage; always referenced to ground)
V_{DG}	drain-to-gate voltage (single-gate types)
V_{DG1}	drain-to-gate-No.1 voltage (dual-gate types)
V_{DG2}	drain-to-gate-No.2 voltage (single-gate types)
V_{DIO}	diode-to-substrate voltage
V_{DR}	diode reverse voltage
V_{DS}	drain-to-source voltage
V_{EE}	source voltage (the most negative supply voltage in a 3-supply voltage system)
V_F	dc forward voltage
$\Delta V_F/\Delta T$	temperature coefficient of forward voltage drop
V_{GH}	channel gate input voltage, high level
V_{GL}	channel gate input voltage, low level
V_{GS}	gate-to-source voltage
$V_{GS}(TH)$	gate-to-source threshold voltage
$V_{GS}(Off)$	gate-to-source cutoff voltage (single-gate types)
V_{G1S}	gate-No.1-to-source voltage (dual-gate type)
$V_{G1S}(Off)$	gate-No.1-to-source cutoff voltage (dual-gate types)
V_{G2S}	gate-No.2-to-source voltage (dual-gate types)
$V_{G2S}(off)$	gate-No.2-to-source cutoff voltage (dual-gate types)
V_I	input voltage
$V_{I(Lim)}$	input limiting voltage
V_{ICR}	common-mode input voltage range
V_{IL}	input-voltage, low level
V_{IH}	input-voltage, high level
V_{IO}	input offset voltage
$\lvert V_{IO}\rvert$	magnitude of input offset voltage
$\Delta V_{IO}/\Delta T$	temperature coefficient of magnitude of input offset voltage
$\Delta V_{IO}/\Delta T$	temperature coefficient of input offset voltage drift
$\Delta V_{IO}/\Delta V^+$	positive input-offset-voltage sensitivity
$\Delta V_{IO}/\Delta V^-$	negative input-offset-voltage sensitivity
αV_{IO}	average temperature coefficient of input-offset voltage
$V_{i(Lim)}$	input limiting voltage (knee)
V_{knee}	protective diode knee voltage (protected gate types)
V_N	output noise voltage
V_O	output voltage
$\Delta V_O/\Delta V^-$	dc supply voltage sensitivity
$\Delta V_O/\Delta V^+$	dc supply voltage sensitivity
$V_{O(rms)}$	open-loop output voltage swing
ΔV_O	output voltage temperature coefficient
$V_{Op\text{-}p}$	output voltage swing
$V_{O(af)}$	recovered af voltage
V_{OL}	output voltage, low level; the voltage level at an output when the input logic conditions have been set to establish logic LOW output.
V_{OO}	output offset voltage
V_{OH}	output voltage, high level; the voltage level at an output when the input logic conditions have been set to establish a logic HIGH output.
V_{OM}^+	maximum output voltage
V_{OM}^-	maximum output voltage
V_{QP}	charge pump voltage
V_{QPL}	charge pump input voltage, low level
V_{QPH}	charge-pump input voltage, high level
V_{REF}	reference voltage
V_{REG}	regulated supply voltage
V_{RR}	supply voltage rejection ratio
V_{TH}	input threshold voltage
V_Z	zener voltage
Y_{fs}	magnitude of small-signal, common-source, short-circuit forward transfer admittance (transadmittance)
Y_{is}	small-signal, common-source, short-circuit, input-admittance (conductance, real part of admittance; susceptance, imaginary part of admittance)
Y_{os}	small-signal, common-source, short-circuit, output admittance
$\lvert Y_{rs}\rvert$	magnitude of small-signal, common-source, short-circuit, reverse transadmittance
$<Y_{rs}$	phase angle of small-signal, common-source, short-circuit, reverse transadmittance
$(-)_{rs}$	angle of reverse transadmittance, common-source circuit
Z_1	input impedance
Z_O	output impedance
Z_Z	zener impedance
ϕ	phase angle
ϕ	phase margin
η	efficiency
ϕL	open-loop phase lag

Cross-Reference Directory for Linear Integrated Circuits

Industry Type	RCA Replacement Type
AD301AH	CA301AT,LM301AH
AD301AN	CA301AE,LM301AN
AD741H	CA741T,LM741H
AD741N	CA741E,LM741N
AD741CH	CA741CT,LM741CH
AD741CN	CA741CE,LM741CN
AD2020	CA3162E
AMLM301AH	CA301AT,LM301AH
AMLM301H	CA301T,LM301AH
AMLM307H	CA307T,LM307H
AMLM311H	CA311T,LM311H
AM723HC	CA723CT,LM723CH
AM723HM	CA723T,LM723H
AM741HC	CA741CT,LM741CH
AM741HM	CA741T,LM741H
AM747HC	CA747CT
AM747HM	CA747T
AM748HC	CA748CT, LM748CH
AM1458H	CA1458T,LM1458H
AM1558H	CA1558T,LM1558H
HA1-2630	CA3020
HA1-2650	LM1558A, CA1558E
HA1-2655	LM1458H, CA1458E
HA1-2720	CA6078
HA2-2311-5	CA311T,LM311H
HA2-2520	CA3100T
HA2-2650	CA1558T,LM1558H
HA2-2655	CA1458T,LM1458H
HA2-2720	CA3078E
ITT1352N	CA1352E
ITT3064C	CA3064T
ITT3064N	CA3064E
ITT3065N	CA3065E
LF156H	CA081T
LF356H	CA081CT
LF356J	CA081E
LM100	CA3085E
LM124N	CA124E
LM139J	CA139F
LM139AN	CA139AE
LM139AJ	CA139AF
LM139N	CA139E
LM158AH	CA158AT
LM158AN	CA158AE
LM158AT	CA158AT
LM158N	CA158E
LM158P	CA158E
LM158T	CA158T
LM201AN	CA201AE
LM201AP	CA201AE
LM201AV	CA201AE
LM201H	CA201T
LM201N	CA201E
LM201T	CA201T
LM224N	CA224E
LM239AD	CA239AF
LM239AF	CA239AF
LM239AJ	CA239AF
LM239AN	CA239AE
LM239D	CA239F
LM239F	CA239F
LM239J	CA239F
LM239N	CA239E
LM258AH	CA258AT
LM258AN	CA258AE
LM258AT	CA258AT
LM258H	CA258T
LM258L	CA258T
LM258N	CA258E
LM258P	CA258E
LM258T	CA258T
LM301AH	CA301AT,LM301AH
LM301AL	CA301AT,LM301AH
LM301AN	CA301AE,LM301AN
LM301AP	CA301AE,LM301AN
LM301AT	CA301AT,LM301AH
LM301AV	CA301AE,LM301AN
LM307H	CA307T,LM307H
LM307N	CA307E,LM307N
LM307T	CA307T,LM307H
LM311H	CA311T,LM311H
LM311L	CA311T,LM311H
LM311N	CA311E,LM311N
LM311P	CA311E,LM311N
LM311T	CA311T,LM311H
LM324N	CA324E,LM324N
LM339AJ	CA339AF
LM339AN	CA339AE,LM339AN
LM339D	CA339F
LM339F	CA339F
LM339J	CA339F
LM339N	CA339E,LM339N
LM358AH	CA358AT
LM358AN	CA358AE
LM358AT	CA358AT
LM358H	CA358T
LM358L	CA358T
LM358N	CA358E
LM358P	CA358E
LM358T	CA358T
LM393N	CA3290E
LM555CH	CA555CT,LM555CH
LM555CN	CA555CE,LM555CN
LM555H	CA555T
LM555N	CA555E,LM555N
LM723CH	CA723CT,LM723CH
LM723CN	CA723CE,LM723CN
LM723H	CA723T,LM723H
LM723N	CA723E,LM723N
LM741CH	CA741CT,LM741CH
LM741CN	CA741CE,LM741CN
LM741H	CA741T,LM741H
LM741N	CA741E,LM741N
LM746N	CA3072
LM747CH	CA747CT
LM747CN	CA747CE
LM747H	CA747T
LM748CH	CA748CT,LM748CH
LM748CN	CA748CE,LM748CN
LM748H	CA748T,LM748H
LM1310N	CA1310E
LM1391N	CA1391E
LM1394N	CA1394E
LM1458H	CA1458T,LM1458H
LM1458N	CA1458E,LM1458N
LM1558H	CA1558T,LM1558H
LM1558N	CA1558E
LM1800N	CA758E
LM1820N	CA3123E
LM1845N	CA3120E
LM2111N	CA2111AE
LM2901J	CA2901F
LM2901N	LM2901N
LM2902N	LM2902N
LM2904N	CA2904E,LM2904N
LM2904P	CA2904E,LM2904N
LM3011H	CA3011
LM3018H	CA3018
LM3018AH	CA3018A
LM3019H	CA3019
LM3026H	CA3026
LM3028AH	CA3028A
LM3028B	CA3028B
LM3039H	CA3039
LM3045D	CA3045,CA3045F
LM3046N	CA3046
LM3053H	CA3053
LM3054N	CA3054
LM3064H	CA3064
LM3064N	CA3064E
LM3065N	CA3065
LM3066N	CA3066
LM3067N	CA3067
LM3070N	CA3070
LM3071N	CA3071
LM3075N	CA3075
LM3086N	CA3086
LM3089N	CA3089E, CA3189E
LM3126N	CA3126E
LM3146AN	CA3146AE
LM3302J	LM3302F
LM3302	LM3302N
LM3401N	CA3401E
M5141T	CA741CT,LM741CH
MC1310P	CA1310E
MC1352P	CA1352E
MC1357P	CA2111AE
MC1357PQ	CA2111AQ
MC1358P	CA3065
MC1364G	CA3064T
MC1364P	CA3064E
MC1370P	CA3070
MC1371P	CA3071
MC1375P	CA3075
MC1389P	CA3089E, CA3189E
MC1391P	CA1391E
MC1394P	CA1394E
MC1398P	CA1398E
MC1455G	CA555CT,LM555CH
MC1455P1	CA555CE,LM555CN
MC1458G	CA1458T,LM1458H
MC1458P1	CA1458E,LM1458N
MC1458T	CA1458T,LM1458H
MC1555G	CA555T
MC1555P1	CA555CE,LM555CN
MC1558G	CA1558T,LM1558H
MC1558P1	CA1558E
MC1558T	CA1558T,LM1558H
MC1723CG	CA723CT,LM723CH
MC1723CP	CA723CE,LM723CN
MC1723G	CA723T,LM723H
MC1741CG	CA741CT,LM741CH
MC1741CP1	CA741CE, LM741CN
MC1741G	CA741T,LM741H

Cross-Reference Directory for Linear Integrated Circuits

Industry Type	RCA Replacement Type
MC1747CG	CA747CT
MC1747G	CA747T
MC1748CG	CA748CT,LM748CH
MC1748CP1	CA748CE,LM748CN
MC1748G	CA748T,LM748H
MC3346P	CA3046
MC3386P	CA3086
MC34001BP	CA081AE
MC34001P	CA081E
MC34002BP	CA082AE
MC34002P	CA082E
MC3401P	CA3401E
NE555P	CA555CE,LM555CN
NE555L	CA555CT,LM555CH
NE555T	CA555CT,LM555CH
NE555V	CA555CE,LM555CN
PM741J	CA741T,LM741H
PM741CJ	CA741CT,LM741CH
PM747K	CA747T
PM747CK	CA747CT
RC555NB	CA555CE,LM555CN
RC555T	CA555CT,LM555CH
RC723CN	LM723CN
RC723DB	CA723CE,LM723CN
RC723T	CA723CT,LM723CH
RC1458NB	CA1458E,LM1458N
RC1458T	CA1458T,LM1458T
RC3401DB	CA3401E
RC741DB	CA741CE,LM741CN
RC741NB	CA741CE,LM741CN
RC741T	CA741T,LM741H
RC747DB	CA747CE
RC747T	CA747T
RM555T	CA555T,LM555H
RM723T	CA723T, LM723H
RM741T	CA741T,LM741H
RM747T	CA747T
RM1558T	CA1558T, LM1558H
SE555L	CA555T
SE555N	CA555E
SE555P	CA555E
SE555T	CA555T
SFC2301A	CA301AT,LM301AH
SFC2301ADC	CA301AE,LM301AN
SFC2307	CA307T,LM307H
SFC2311	CA311T,LM311H
SFC2741C	CA741CT,LM741CH
SFC2741M	CA741T,LM741H
SFC2748DC	CA748CE,LM748CN
SFC2748C	CA748CT,LM748CH
SG301AN	CA301AE,LM301AN
SG301AT	CA301AT,LM301AH
SG307N	CA307E,LM307N
SG307T	CA307T,LM307H
SG311M	CA311E,LM311N
SG311T	CA311T,LM311H
SG723CN	CA723CE,LM723CN
SG723CT	CA723CT,LM723CH
SG723T	CA723T,LM723H
SG741CN	CA741CE,LM741CN
SG741CT	CA741CT,LM741CH
SG741T	CA741T,LM741H
SG747CN	CA747CE
SG747CT	CA747CT
SG747T	CA747T
SG748CN	CA748CE,LM748CN
SG748CT	CA748CT,LM748CH

Industry Type	RCA Replacement Type
SG748T	CA748T,LM748H
SG1458M	CA1458E,LM1458N
SG1458T	CA1458T,LM1458H
SG1558T	CA1558T
SG2524N	CA2524E
SG3018T	CA3018
SG3018AT	CA3018A
SG3058J	CA3058
SG3059J	CA3059
SG3079J	CA3079
SG3081N	CA3081
SG3081J	CA3081F
SG3082N	CA3082
SG3082J	CA3082F
SG3083J	CA3083F
SG3401N	CA3401E
SG3524N	CA3524E
SN76115N	CA1310E
SN76116N	CA758E
SN76242N	CA3070
SN76243AN	CA3071
SN76264N	CA3072
SN76267N	CA3067
SN76298N	CA1398E
SN76564N	CA3064
SN76565N	CA3064E
SN76635N	CA3123E
SN76650N	CA1352E
SN76666N	CA3065
SN76675N	CA3075
SN76676P	CA3076
SN76689N	CA3089E, CA3189E
SSS301AJ	CA301AT,LM301AH
SSS301AP	CA301AE,LM301AN
SSS741CJ	CA741CT,LM741CH
SSS1458J	CA1458T,LM1458H
SSS1558J	CA1558T,LM1558H
TDA2002V	CA2002
TDA2002H	CA2002M
TBB0747	CA747CT
TBB0748	CA748CT,LM748CH
TBB0748B	CA748CE,LM748CN
TBB1458B	CA1458E,LM1458N
TBC0747	CA747T
TCA270	CA270
TDA3081N	CA3081
TDA3082N	CA3082
TDA3083N	CA3083
TDA7607	CA7607E
TDA7611	CA7611E
TDB0723	CA723CT,LM723CH
TDB0723A	CA723CE,LM723CN
TDC0723	CA723T,LM723H
TL080ML	CA080T
TL080AML	CA080AT
TL080CL	CA080CT
TL080CP	CA080E
TL080ACP	CA080AE, CA080BE
TL081ML	CA081T
TL081AML	CA081AT
TL081CL	CA081CT
TL081CP	CA081E
TL081ACP	CA081AE
TL081BCP	CA081BE
TL082ML	CA082T
TL082	CA082CT

Industry Type	RCA Replacement Type
TL082CP	CA082E
TL082ACP	CA082AE
TL082BCP	CA082BE
TL083CN	CA083E
TL083ACN	CA083AE
TL084ACN	CA084AE
TL084CN	CA084E
TL084BCN	CA084BE
U5B7741312	CA741T,LM741H
U5B7741393	CA741CT,LM741CH
U5B7748312	CA748T,LM748H
U5B7748393	CA748CT,LM748CH
U5R7723312	CA723T,LM723H
U5R7723393	CA723CT
U6A7723393	CA723CE,LM723CN
U9T7741393	CA741CE,LM741CN
ULN2111A	CA2111AE
ULN2111N	CA2111AQ
ULN2114A	CA3072
ULN2124A	CA3070
ULN2125A	CA3120E
ULN2127A	CA3071
ULN2129A	CA3075
ULN2137A	CA3123E
ULN2165A	CA3065
ULN2210A	CA1310E
ULN2212B	CA3012
ULN2262A	CA3126Q
ULN2264A	CA3064
ULN2267A	CA3067
ULN2269A	CA3121E
ULN2289A	CA3089E, CA3189E
ULN2298A	CA1398E
ULX2244A	CA758E
μA301AH	CA301AT,LM301AH
μA307H	CA307T,LM307H
μA307T	CA307E,LM307N
μA301AT	CA301AE,LM301AN
μA311H	CA311T, LM311H
μA311T	CA311E,LM311N
μA555HC	CA555CT,LM555CH
μA555HM	CA555T
μA555TC	CA555CE,LM555CN
μA720PC	CA3123E
μA723CA	CA723CE,LM723CN
μA723CL	CA723CT,LM723CH
μA723CN	CA723CE,LM723CN
μA723HC	CA723CT,LM723CH
μA723HM	CA723T,LM723H
μA723MN	CA723E,LM723N
μA723ML	CA723T,LM723H
μA723PC	CA723CE,LM723CN
μA741CN	CA741CE,LM741CN
μA741CL	CA741CT,LM741CH
μA741CP	CA741CE,LM741CN
μA741CT	CA741CE,LM741CN
μA741HC	CA741CT,LM741CH
μA741HM	CA741T,LM741H
μA741ML	CA741T,LM741H
μA741MN	CA741E,LM741N
μA741MP	CA741E,LM741N
μA741PC	CA741CE,LM741CN
μA746PC	CA3072
μA747CA	CA747CE
μA747CL	CA747CT
μA747CN	CA747CE

Cross-Reference Directory for Linear Integrated Circuits

Industry Type	RCA Replacement Type
μA747HC	CA747CT
μA747HM	CA747T
μA747ML	CA747T
μA747MN	CA747E
μA747PC	CA747CE
μA747A	CA747E
μA748CL	CA748CT,LM748CH
μA748CN	CA748CE,LM748CN
μA748CP	CA748CE,LM748CN
μA748CT	CA748CT,LM748CH
μA748HC	CA748CT,LM748CH
μA748HM	CA748T,LM748H
μA748ML	CA748T,LM748H
μA748MN	CA748E,LM748N
μA748MP	CA748E,LM748N
μA748T	CA748E,LM748N
μA748TC	CA748CE,LM748CN
μA758PC	CA758E
μA780PC	CA3070
μA781PC	CA3071
μA787PC	CA3126Q
μA1391T	CA1391E
μA1394T	CA1394E
μA1458HC	CA1458T,LM1458H
μA1458TC	CA1458E,LM1458N
μA1558HM	CA1558T
μA3018HM	CA3018
μA3018AHM	CA3018A

Industry Type	RCA Replacement Type
μA3019HM	CA3019
μA3026HM	CA3026
μA3036HM	CA3036
μA3039HM	CA3039
μA3045DM	CA3045,CA3045F
μA3046DC	CA3046
μA3054PC	CA3054
μA3064HC	CA3064
μA3064PC	CA3064E
μA3065PC	CA3065
μA3066PC	CA3066
μA3075PC	CA3075
μA3086DC	CA3086F
μA3089E	CA3089E, CA3189E
μA3401P	CA3401E
μPC151A	CA741CT,LM741CH
μPC151C	CA741CE,LM741CN
μPC157A	CA301AT,LM301AH
μPC157C	CA301AE,LM301AN
μPC251A	CA747CT
μPC251C	CA747CE
μPC301AC	CA301AE,LM301AN
μPC311C	CA311E,LM311N
μPC324C	CA324E,LM324N
μPC339C	CA339E,LM339N
μPC741C	CA741CE,LM741CN
μPC1458C	CA1458E,LM1458N

LM Branded Linear IC's

RCA supplies the following Linear IC's branded with the industry standard "LM" Brand. Technical Data on LM Branded types is identical to the corresponding CA Branded types. See chart below.

Type	Equivalent CA Type	Data Bulletin File No.	Page
LM1458H	CA1458T	531	38
LM1458N	CA1458E	531	38
LM1558H	CA1558T	531	38
LM201H	CA201T	786	28
LM2901N	*		
LM2902N	*		
LM2904N	CA2904E	1019	38
LM301AH	CA301AT	786	28
LM301AN	CA301AE	786	28
LM307H	CA307T	785	34
LM307N	CA307E	785	34
LM311H	CA311T	797	270
LM311N	CA311E	797	270
LM324N	CA324E	796	104
LM3302N	*		
LM339AN	CA339AE	795	301

Type	Equivalent CA Type	Data Bulletin File No.	Page
LM339N	CA339E	795	301
LM358N	CA358E	1019	98
LM555CH	CA555CT	834	653
LM555CN	CA555CE	834	653
LM723CH	CA723CT	788	520
LM723CN	CA723CE	788	520
LM723H	CA723T	788	520
LM723N	CA723E	788	520
LM741CH	CA741CT	531	38
LM741CN	CA741CE	531	38
LM741H	CA741T	531	38
LM741N	CA741E	531	38
LM748CH	CA748CT	531	38
LM748CN	CA748CE	531	38
LM748H	CA748T	531	38
LM748N	CA748E	531	38

*No CA Branded part type conforms to industry standard data

The EVP option

For systems designers, the key to cost-effective device procurement is often found in determining the right level of reliability. How much reliability? At what cost?

For semiconductor manufacturer and user alike, the answer has always been the same. As much reliability as the application requires at the lowest practical cost.

The screening programs of RCA employ this philosophy to achieve Linear IC reliability goals in both standard product and military high-reliability product.

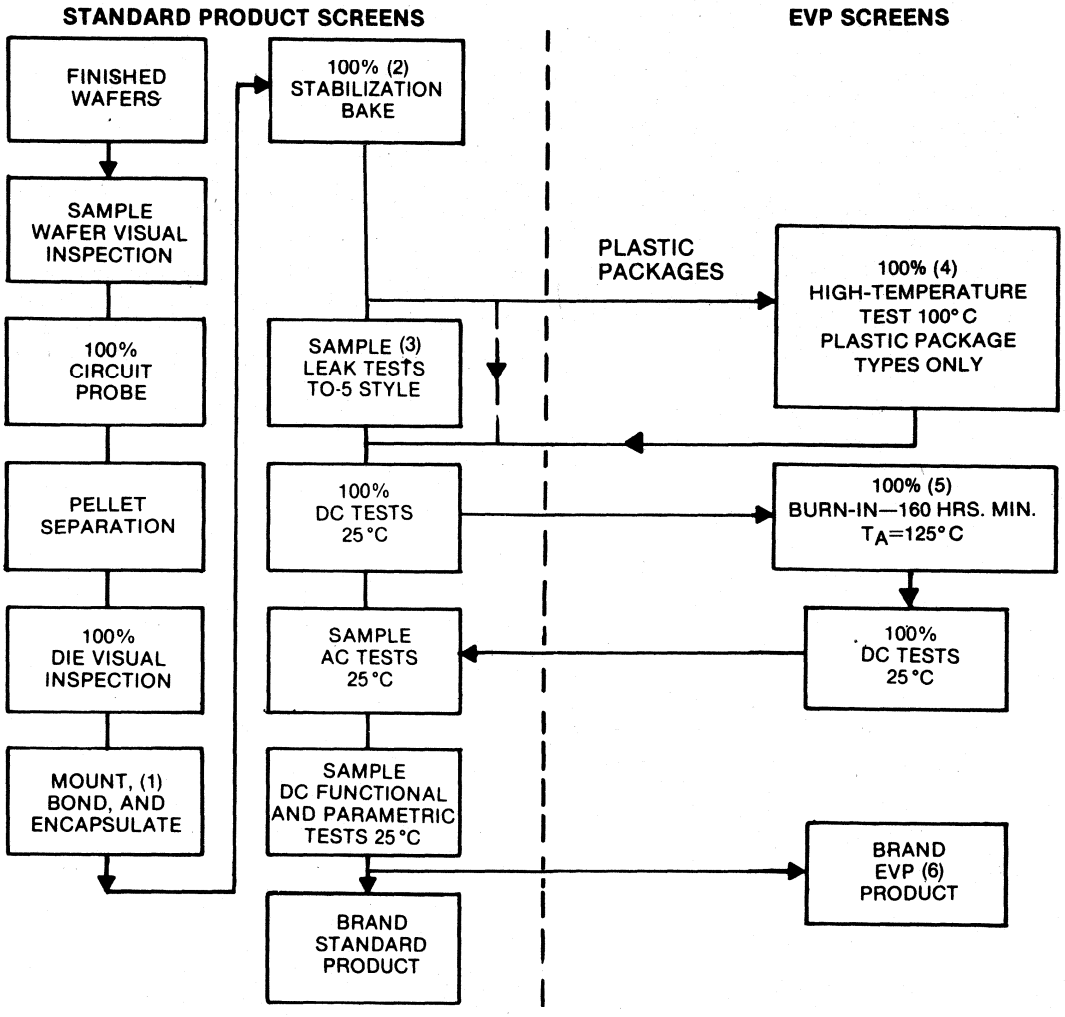
As both integrated circuits and their application become more complex, an increasing number of linear IC users find the cost-effective answer to reliability requirements in a new level of reliability screening. One which for the intended use, is more effective than standard product but does not involve the higher costs required to achieve military reliability levels.

This new cost-effective approach to enhanced commercial reliability is provided by the RCA Extra Value Program.

The Extra Value Program adds a burn-in and additional testing to the comprehensive real-time controls and test procedures carried out on standard plastic and TO-5-style product. The enhanced product of the Extra Value Program achieves AQL levels as shown in the chart below.

TEST	EVP PRODUCT
100% High-Temperature Continuity or Functional Test at 100 °C	Plastic-package types only
Sample Leak Test	TO-5-style package types only; Gross leak rate = $1x10^{-5}$ Atm.cc/sec. max.; Fine leak rate = $5x10^{-8}$ Atm.cc/sec. max.
100% Burn-In	160 Hrs. Min. at 125 °C per MIL-STD-883A Method 1015.1
AQL DC Parametric Tests	0.25% Max.
AQL DC Functional Tests	0.15% Max.
Marking	Standard Part No. with Blue Dot

PROCESS FLOW CHART



(1) Epoxy mount and cure; ultrasonic aluminum wire bond on TO-5-style or thermosonic gold-wire bond on plastic types; encapsulate in TO-5-style or plastic dual-in-line package.

(2) Stabilization bake 6 hours at 175 °C for plastic-package types, 16 hours at 200 °C for TO-5-style types.

(3) Gross leak rate of $1x10^{-5}$ Atm.cc/sec max. and fine leak rate of $5x10^{-8}$ Atm.cc/sec max.

(4) High-temperature (i.e., heat-pipe, hot-rail) test
   (a) automatic test for continuity on each terminal at 100 °C for array types.
   (b) continuity or functional gain test at 100 °C for op-amps, comparators, and voltage regulators.

(5) 100% dc test before and after burn-in per MIL-STD-883A Method 1015.1

(6) Brand EVP product surviving both Enhancement Screens with Standard Type Number plus blue dot.

The extra value of burn-in

Quality relates to the percentage of defective units at "time zero". It is a measure of devices dead-on-arrival (DOA). While the total absence of even a single defective unit in any lot of devices received from the semiconductor manufacturer may be the ideal goal, it is an impractical one.

Testing experience and a complete understanding of failure mechanisms tell us that every increment of improvement over the standard 0.65% AQL carries a price tag which becomes disproportionately high relative to the number of line rejects it will eliminate.

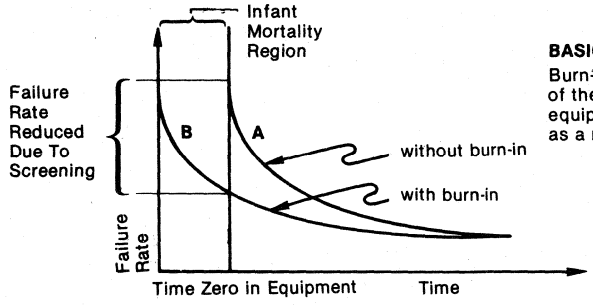
Application experience shows that the simple reduction of AQL does in no way guarantee an improvement in field-failure rates.

Reliability, in contrast to the zero-time aspects of quality, is a measure of the maintenance of quality through time in actual system environment.

Component burn-in is effective in screening out temperature- and time-dependent mechanisms that would normally escape detection under a 100% final electrical test.

Thus, the Extra Value Program offers greater cost effectiveness in achieving field reliability than any program which relies solely on reduced outgoing or incoming inspection levels.

The basic theory of burn-in and the type of improvement which can be expected through reduced device infant mortality is depicted in the chart below.



BASIC THEORY OF SCREENING

Burn-in and screening eliminate a major percentage of the infant mortality. Component life in equipment is translated from curve A to curve B as a result of burn-in

EVP SCREENING	ORDERING INFORMATION		
	Package Type	Standard Type No.	Extra Value Type No.
Burn-In Time — 160 Hrs. Min. Burn-In Temperature — 125 °C Hot Continuity Test Temperature — 100 °C	Plastic Dual-In-Line	CA741E	CA741EX
	TO-5 Style	CA3140T	CA3140TX

Operational Amplifiers
Technical Data

General Purpose

General Purpose Wideband

Variable

*BiMOS types
•Low-noise versions of CA741 and CA3078

Op Amp, Comparator, and OTA

Selection Chart ..... Pages 24 — 27

Op-Amp, Comparator, and OTA Selection Chart

Type #	Description	Basic Ratings			Input Characteristics @ 25°C				
		Compens. Internal External	V^+, V^- Max. V	I_S Max. nA	V_{IO} Max. mV	I_B Max. nA	I_{IO} Max. nA	V_{ICR} (Plus) V	V_{ICR} (Minus) V
CA080E	Single BiMOS Op-Amp with High Slew Rate	E	±18	2.8	15	.050	.030	10	10
CA080T-S		E	±18	2.8	6	.040	.020	12	12
CA080AE		E	±18	2.8	6	.040	.020	12	12
CA080AT-S		E	±18	2.8	3	.040	.020	12	12
CA080BE		E	±18	2.8	3	.030	.010	12	12
CA080CT-S		E	±18	2.8	15	.050	.030	10	10
CA081E	Single BiMOS Op-Amp with High Slew Rate	I, E	±18	2.8	15	.050	.030	10	10
CA081T-S		I, E	±18	2.8	6	.040	.020	12	12
CA081AE		I, E	±18	2.8	6	.040	.020	12	12
CA081AT-S		I, E	±18	2.8	3	.040	.020	12	12
CA081BE		I, E	±18	2.8	3	.030	.010	12	12
CA081CT-S		I, E	±18	2.8	15	.050	.030	10	10
CA082E	Dual BiMOS Op-Amp with High Slew Rate	I	±18	5.6	15	.050	.030	10	10
CA082T-S		I	±18	5.6	6	.040	.020	12	12
CA082AE		I	±18	5.6	6	.040	.020	12	12
CA082AT-S		I	±18	5.6	3	.040	.020	12	12
CA082BE		I	±18	5.6	3	.030	.010	12	12
CA082CT-S		I	±18	5.6	15	.050	.030	10	10
CA083E	Dual BiMOS Op-Amp with High Slew Rate	I	±18	5.6	15	.050	.030	10	10
CA083AE		I	±18	5.6	6	.040	.020	12	12
CA083BE		I	±18	5.6	3	.030	.010	12	12
CA084E	Quad BiMOS Op-Amp with High Slew Rate	I	±18	11.2	15	.050	.030	10	10
CA084AE		I	±18	11.2	6	.040	.020	12	12
CA084BE		I	±18	11.2	3	.030	.010	12	12
CA101	General Purpose Op-Amp	E	±22	3.0	5.0	500	200	12	12
CA124[11]	Quad Op-Amp	I	±16	8	5	150	30	V^+–1.5	0
CA139[11]	Quad Volt Comparator	NA	±18	8	5	100	25	V^+–1.5	0
CA139A[11]	Quad Volt-Comparator	NA	±18	8	2	100	25	V^+–1.5	0
CA158[11]	Dual Op-Amp-General Purpose	E	±16	3	5	150	30	V^+–1.5	0
CA158A[11]	Dual Op-Amp-General Purpose	E	±16	3	2	50	10	V^+–1.5	0
CA201	General Purpose Op-Amp	E	±22	3	7.5	1,500	500	12	12
CA224[11]	Quad Op Amp	I	±16	8	7	250	50	V^+–1.5	0
CA239[11]	Quad Volt Comparator	NA	±18	8	5	250	50	V^+–1.5	0
CA258[11]	Dual Op-Amp-General Purpose	E	±16	3	5	150	30	V^+–1.5	0
CA258A[11]	Dual Op-Amp-General Purpose	E	±16	3	3	80	15	V^+–1.5	0
CA301A	General Purpose Op-Amp	E	±18	3	7.5	250	50	12	12
CA307	General Purpose Op-Amp	I	±18	3	7.5	300	50	12	12
CA311	Single Volt Comparator	NA	±18	8	7.5	250	50	14	14
CA324[11]	Quad Op-Amp	I	±16	8	7	250	50	V^+–1.5	0
CA339[11]	Quad Voltage Comparator	NA	±18	8	5	250	50	V^+–1.5	0
CA339A[11]	Quad Voltage Comparator	NA	±18	8	2	250	50	V^+–1.5	0
CA358[11]	Dual Op-Amp General Purpose	E	±16	3	7	250	50	V^+–1.5	0
CA358A[11]	Dual Op-Amp General Purpose	E	±16	3	3	100	30	V^+–1.5	0
CA741	Single-General Purpose Op-Amp	I	±22	2.8	5	500	200	12	12
CA741C	Single-General Purpose Op-Amp	I	±18	2.8	6	500	200	12	12
CA747	Dual 741	I	±22	5.6	5	500	200	12	12
CA747C	Dual 741	I	±18	5.6	6	500	200	12	12
CA748	Single-General Purpose Op-Amp	E	±22	2.8	5	500	200	12	12
CA748C	Single-General Purpose Op-Amp	E	±18	2.8	6	500	200	12	12
CA1458	Dual 748	I	±18	5.6	6	500	200	12	12
CA1558	Dual 748	I	±22	5.6	5	500	200	12	12
CA3008	General Purpose Op-Amp	E	±8	9	5	12,000	5,000	.50	4
CA3008A	General Purpose Op-Amp	E	±8	9	2	4,000	1,500	.50	4
CA3010	General Purpose Op-Amp	E	±8	9	5	12,000	5,000	.50	4
CA3010A	General Purpose Op-Amp	E	±8	9	2	4,000	5,000	.50	4
CA3015	General Purpose Op-Amp	E	±16	21	5	24,000	5,000	.65	8
CA3016	General Purpose Op-Amp	E	±16	21	5	24,000	5,000	.65	8
CA3029	General Purpose Op-Amp	E	±8	9	5	12,000	5,000	.50	4
CA3029A	General Purpose Op-Amp	E	±8	9	2	4,000	1,500	.50	4
CA3030	General Purpose Op-Amp	E	±16	21	5	24,000	5,000	.65	8
CA3030A	General Purpose Op-Amp	E	±16	21	2	6,000	1,600	.65	8
CA3037	General Purpose Op-Amp	E	±8	9	5	12,000	5,000	.50	4
CA3037A	General Purpose Op-Amp	E	±16	9	2	4,000	1,500	.50	4
CA3038	General Purpose Op-Amp	E	±16	21	5	24,000	5,000	.65	8
CA3038A	General Purpose Op-Amp	E	±16	21	2	6,000	1,600	.65	8
CA3060D	OTA - Triple Amplifier and Array	E	±7	3.6	5	5,000	1,000	4.3	5
CA3060AD		E	±18	3.6	5	5,000	1,000	12	12
CA3060BD	I_{ABC} = 100 μA	E	±18	3.6	5	5,000	1,000	12	12
CA3060E	I_{ABC} = 100 μA	E	±18	3.6	5	5,000	1,000	12	12

Output Characteristics				AC Characteristics @ 25°C			Package Characteristics[4]		Page #
V_{OUT} +[5] Min. V	V_{OUT}−[5] Min. V	R_L for V_{OUT} OHMS	AOL[1] Min V/V	BW[2] Typ MHz	Slew Rate[2] Typ V/μs	Temp[3] Range IMC	Plastic Ceramic	TO5 Metal CAN	
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C	8E		
24 V_{pp}	24 V_{pp}	10K	50K	5	13	M		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	8E		83
24 V_{pp}	24 V_{pp}	10K	50K	5	13	M	8E		
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C	8E		
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	50K	5	13	M		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	8E		83
24 V_{pp}	24 V_{pp}	10K	50K	5	13	M		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	8E		
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C	8E		
24 V_{pp}	24 V_{pp}	10K	50K	5	13	M		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	8E		83
24 V_{pp}	24 V_{pp}	10K	50K	5	13	M		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	8E		
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C		8T, 8S	
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C	14E		
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	14E		83
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	14E		
24 V_{pp}	24 V_{pp}	10K	25K	5	13	C	14E		
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	14E		83
24 V_{pp}	24 V_{pp}	10K	50K	5	13	C	14E		
10	10	2K	50K	1.0	10 non comp	M	8E	8T, 8S	28
V^+−1.5V	0	2K	50K	1.0	.5	M	14E		104
V_{SAT} = .5V		5.1K	50K	t_r = 300 ns	t_f = 1.3 μs	M	14E		301
V_{SAT} = .5V		5.1K	50K	t_r = 300 ns	t_f = 1.3 μs	M	14E		
V^+−1.5V	0	2K	50K	1.0	.5	M	8E	8T, 8S	93
V^+−1.5V	0	2K	50K	1.0	.5	M	8E	8T, 8S	
+10	+10	2K	20K	1.0	10 non comp	C	8E	8T, 8S	28
V^+−1.5V	0	2K	25K	1.0	.5	I	14E		104
V_{SAT} = .5V		2K	50K	t_r = 300 ns	t_f = 1.3 μs	I	14E		301
V^+−1.5V	0	2K	50K	1.0	.5	I	8E	8T, 8S	93
V^+−1.5V	0	2K	50K	1.0	.5	I	8E	8T, 8S	
+10	−10	2K	25K	1.0	10 non comp	C	8E	8T, 8S	28
+10	−10	2K	25K	2	.5	C	8E	8T, 8S	34
V_{SAT} = 1.5V		5K	200K	Response time 200 ns		C	8E	8T, 8S	270
V^+−1.5V	0	2K	25K	1.0	.5	C	14E		104
V_{SAT} = .5V		2K	50K	t_r = 300 ns	t_f = 1.3 μs	C	14E		301
V_{SAT} = .5V		2K	50K	t_r = 300 ns	t_f = 1.3 μs	C	14E		
V^+−1.5V	0	2K	25K	1.0	.5	C	8E	8T, 8S	93
V^+−1.5V	0	2K	25K	1.0	.5	C	8E	8T, 8S	
10	−10	2K	50K	1.0	.5	M	8E	8T, 8S	38
10	−10	2K	20K	1.0	.5	C	8E	8T, 8S	
10	−10	2K	50K	1.0	.5	M	14E	10T	38
10	−10	2K	20K	1.0	.5	C	14E	10T	
10	−10	2K	50K	1.0	.5	M	8E	8T, 8S	38
10	−10	2K	20K	1.0	.5	C	8E	8T, 8S	
10	−10	2K	20K	1.0	.5	C	8E	8T, 8S	38
10	−10	2K	50K	1.0	.5	M	8E	8T, 8S	38
2	−2	2K	.7K	.20[10]	3	M	14K		114
2	−2	2K	.7K	.20[10]	3	M	14K		121
2	−2	2K	.7K	.20[10]	3	M		12T	114
2	−2	2K	.7K	.20[10]	3	M		12T	121
6	−6	2K	2K	.20[10]	3	M		12T	114
6	−6	2K	2K	.20[10]	3	M	14K		114
2	−2	2K	.7K	.20[10]	7	M	14E		114
2	−2	2K	.7K	.20[10]	7	C	14E		121
6	−6	2K	2K	.20[10]	3	C	14E		114
6	−6	2K	2K	.20[10]	3	C	14E		121
2	−2	2K	.7K	.20[10]	7	C	14D		114
2	−2	2K	.7K	.20[10]	7	M	14D		121
6	−6	2K	2K	.20[10]	3	M	14D		114
6	−6	2K	2K	.20[10]	3	M	14D		121
4.6	−5.8	∞	gm=30μmho	.110	8	M	16D		
12	−12	∞	gm=30μmho	.110	8	M	16D		224
12	−12	∞	gm=30μmho	.110	8	M	16D		
12	−12	∞	gm=30μmho	.110	8	I	16E		

Op-Amp, Comparator, and OTA Selection Chart

Type #	Description	Basic Ratings			Input Characteristics @ 25°C				
		Compens. Internal External	V^+, V^- Max. V	I_S Max. nA	V_{IO} Max. mV	I_B Max. nA	I_{IO} Max. nA	V_{ICR} (Plus) V	V_{ICR} (Minus) V
CA3078	Micropower Op Amp	E	±7	.130	4.5	170	32	5	5
CA3078A	Micropower Op-Amp	E	±18	.025	3.5	12	2.5	5	5
CA3080	High Slew Rate OTA	E	±18	1.2	5	5,000	600	12	12
CA3080A	High Slew Rate OTA	E	±18	1.2	2	5,000	600	12	12
CA3094	Programmable	E	±12	.4	5	5,000	2,000	12	14
CA3094A	Power Switch/Amplifier	E	±18	.4	5	5,000	2,000	12	14
CA3094B	(OTA)	E	±22	.4	5	5,000	2,000	12	14
CA3100	Wideband BiMOS Op-Amp	E, I	±18	10.5	5	2,000	400	12	12
CA3130[11]	BiMOS Op-Amp with	E	±8	15	15	.050	.030	10	0
CA3130A[11]	MOS Input and	E	±8	15	5	.030	.020	10	0
CA3130B[11]	MOS Output	E	±8	15	2	.020	.010	10	0
CA3140	BiMOS Op-Amp with	I	±18	6	15	.050	.030	11	15
CA3140A	MOS Input and	I	±18	6	5	.030	.020	12	15
CA3140B	Bipolar Output	I	±22	6	2	.020	.010	12	15
CA3160[11]	BiMOS Op-Amp with	I, E	±8	15	15	.050	.030	10	0
CA3160A[11]	MOS Input and	I, E	±8	15	5	.030	.020	10	0
CA3160B[11]	MOS Output	I, E	±8	15	2	.020	.010	10	0
CA3193[8]	Precision - 5μV/°C, Neg. Null	I	±18	3.5	.500	40	10	10	12
CA3193A[8]	Precision - 3μV/°C, Neg. Null	I	±18	3.5	.200	20	5	10	12
CA3193B[8]	Precision — 2 μV/°C Neg. Null	I	±22	3.5	.075	15	3	10	12
CA3240	Dual BiMOS Op-Amp	I	±18	12	15	.050	.030	11	15
CA3240A	With MOS Input and Bipolar Output	I	±18	12	5	.040	.020	12	15
CA3260[11]	Dual BiMOS Op Amp	I	±8	15.5	15	.050	.030	10	0
CA3260A[11]	With MOS Input	I	±8	15.5	5	.030	.020	10	0
CA3260B[11]	and MOS Output	I	±8	15.5	2	.020	.010	10	0
CA3280[12]	Dual OTA	E	±18	4.8	3.0	5,000	700	13	13
CA3280A[12]	Dual OTA	E	±18	4.8	0.5	5,000	700	13	13
CA3290	Dual BiMOS	NA	±18	3	20	.050	.030	V^+–3.8V	V^-
CA3290A	Comparator with	NA	±18	3	10	.040	.025	V^+–3.8V	V^-
CA3290B	MOS Input & Bipolar Output	NA	±22	3	6	.030	.020	V^+–3.8V	V^-
CA3401	Quad Single Supply Op-Amp (Norton)	I	±18	14	NA	300	NA	NA	NA
CA3420	Low-Supply Voltage	I	±11	.550	10	.003	.0020	NS	NS
CA3420A	Low Current BiMOS	I	±11	.550	5	.003	.0020	.2	1.0
CA3420B	Op-Amp (±1V Operation)	I	±11	.550	2	.001	.0007	.2	1.0
CA3420	Low-Supply Voltage	I	±11	.700	10	.003	.0020	8.5	10
CA3420A	Low-Current BiMOS	I	±11	.700	5	.003	.0020	9.0	10
CA3420B	Op-Amp (±10V Operation)	I	±11	.700	2	.001	.0007	9.0	10
CA3440[7]	Nano Power	I	±12.5	.017	10	.050	.030	3.5	5.0
CA3440A[7]	BiMOS Op-Amps	I	±12.5	.017	5	.040	.020	3.5	5.0
CA3440B[7]		I	±12.5	.017	2	.030	.010	3.5	5.0
CA3493[8]	Precision - 5μV/°C - Pos. Null	I	±18	3.5	.500	40	10	10	12
CA3493A[8]	Precision - 3 μV°C - Pos. Null	I	±18	3.5	.200	20	5	10	12
CA3493B[8]	Precision - 2 μV/°C - Pos. Null	I	±22	3.5	.075	15	3	10	12
CA6078A[9, 10]	Low Burst Noise Micropower Op-Amp	E	±18	.025	3.5	12	3.5	14	14
CA6741[9]	Low Burst Noise General Purpose Op-Amp	I	±22	2.8	5.0	500	200	12	12

NOTES:

1. A_{OL} value is for a load resistor as specified in the output characteristics chart. If the load is different it will be displayed under the A_{OL} value.
   For OTA's the A_{OL} value is replaced by gm.
2. Slew rate values on externally compensated amplifiers will differ with compensation.
   For comparator circuits the slew rate and BW values are replaced by response times.
3. Temperature range's are defined as:
   C = 0°C to 70°C
   I = 40°C to 85°C
   M = –55°C to 125°C
4. Package suffix's are defined as:
   T = TO-5
   E = Plastic
   K = Ceramic Flat Pak
   D = Ceramic — Dual in Line
   S = TO-5 formed for 8 or 12 Lead Plastic
5. Output characteristics are defined for load resistors as defined in the chart. If there are characteristics for two load resistors they will be displayed by a slanted line.
6. CA3100 AC Characteristics:
   Slew rate characteristics in the chart is for C_c = 10 pf Av = 1, V_o = 10 V (pulse)
   For C_c = 0pf, A_V = 10, SR = 70 V/μs typ., 50 V/μs min.

Output Characteristics				AC Characteristics @ 25°C			Package Characteristics[4]		Page #
V_{OUT} +[5] Min. V	V_{OUT}−[5] Min. V	R_L for V_{OUT} OHMS	AOL[1] Min V/V	BW[2] Typ MHz	Slew Rate[2] Typ V/μs	Temp[3] Range IMC	Plastic Ceramic	TO5 Metal CAN	
5.1	−5.1	10K	25K	.002	1.5	C	8E	8T, 8S	237
5.1	−5.1	10K	40K	.0003	0.5	M	8E	8T, 8S	
12	12	∞	gm = 9.6 μmho	2	50	C	8E	8T, 8S	245
12	12	∞	gm = 9.6 μmho	2	50	M	8E	8T, 8S	
14.95	14.2	2K	20K	30	50	M	8E	8T, 8S	213
14.95	14.2	2K	20K	30	50	M	8E	8T, 8S	
14.95	14.2	2K	20K	30	50	M	8E	8T, 8S	
9	−9	2K	630	38	25[6]	M	8E	8T, 8S	135
14.99/12	.001	∞/2K	50K	15/C_c= 0	30/C_c = 0	M	8E	8T, 8S	141
14.99/12	.001	∞/2K	50K	15/C_c = 0	30/C_c = 0	M	8E	8T, 8S	
14.99/12	.001	∞/2K	100K	15/C_c = 0	30/C_c = 0	M	8E	8T, 8S	
12	−14	2K	20K	4.5	9	M	8E	8T, 8S	156
12	−14	2K	20K	4.5	9	M	8E	8T, 8S	
12	−14	2K	50K	4.5	9	M	8E	8T, 8S	
14.99/12	.001	∞/2K	50K	4	10	M	8E	8T, 8S	176
14.99/12	.001	∞/2K	50K	4	10	M	8E	8T, 8S	
14.99/12	.001	∞/2K	100K	4	10	M	8E	8T, 8S	
13	−13	2K	100K	1.2	.25	C	8E	8T, 8S	52
13	−13	2K	316K	1.2	.25	I	8E	8T, 8S	
13	−13	2K	1000K	1.2	.25	M	8E	8T, 8S	
12	−14	2K	20K	4.5	9	M	8E, 14E1	8T, 8S	193
12	−14	2K	20K	4.5	9	M	8E, 14E1	8T, 8S	
14.99/11	.001	∞/2K	50K	4	10	M	8E	8T, 8S	208
14.99/11	.001	∞/2K	50K	4	10	M	8E	8T, 8S	
14.99/11	.001	∞/2K	100M	4	10	M	8E	8T, 8S	
12	−12	∞	50K/∞	9	125	M	16E		260
12.5	−13.3	∞	50K/∞	9	125	M	16E		
V_{SAT} = .4V		(4mA)	25K	t_r = 1.2 μs	t_f = 200 ns	M	8E, 14E1	8T, 8S	291
V_{SAT} = .4V		(4mA)	25K	t_r = 1.2 μs	t_f = 200 ns	M	8E, 14E1	8T, 8S	
V_{SAT} = .4V		(4mA)	50K	t_r = 1.2 μs	t_f = 200 ns	M	8E, 14E1	8T, 8S	
13.5	.10	10K	1K	5	.6	M	14E		110
.90	−.85	∞	10K/10KΩ	.5	.5	M	8E	8T, 8S	63
.90	−.85	∞	20K/10KΩ	.5	.5	M	8E	8T, 8S	
.90	−.95	∞	20K/10KΩ	.5	.5	M	8E	8T, 8S	
9.7	−9.7	∞	10K/10KΩ	.5	.5	M	8E	8T, 8S	63
9.7	−9.7	∞	20K/10KΩ	.5	.5	M	8E	8T, 8S	
9.7	−9.7	∞	20K/10KΩ	.5	.5	M	8E	8T, 8S	
3	−3	10K	10K	.063	.03	M	8E	8T, 8S	254
3	−3	10K	10K	.063	.03	M	8E	8T, 8S	
3	−3	10K	32K	.063	.03	M	8E	8T, 8S	
13	−13	2K	100K	1.2	.25	C	8E	8T, 8S	68
13	−13	2K	316K	1.2	.25	I	8E	8T, 8S	
13	−13	2K	1000K	1.2	.25	M	8E	8T, 8S	
13.7	−13.7	10K	40K	.0003	1.5	M		8T, 8S	79
12	−12	2K	50K	1.0	.50	M		8T, 8S	79

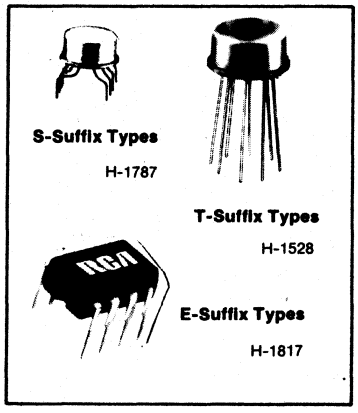
NOTES (cont'd):

7. For CA3440 series R_{SET} = 10 MΩ.
8. CA3493 is equivalent to CA3193 with the exception of nulling & pin out. CA3493 is pos nulling with pinout equivalent μA725. CA3193 has CA741 pinout.
   Temp COEFF = $\Delta V_{IO}/\Delta T$

	Typ	Max	
CA3193/CA3493	1.0	5	μV/° C
CA3193A/CA3493A	1.0	3	μV/° C
CA3193B/CA3493B	.60	2	μV/° C

9. CA6078T and CA6741T are for applications where low noise (burst + I/f) is a prime requirement.
10. −3 db BW
11. Characteristics shown are for single supply operation.
12. CA3280 characteristics @ I_{ABC} = 500 μA except V_{IO}, I_B, I_{IO} which are at I_{ABC} = 1 mA.

CA101, CA201, CA301A Types



Operational Amplifiers

For Commercial, Industrial, and Military Applications

Features:

- *Short-circuit protection and latch-free operation*
- *Unity-gain phase compensation with a single 30-pF capacitor*
- *Replacement for industry types 101, 201, 301A*
- *CA301A Slew Rate (Summing ampl.) 10 V/μs*

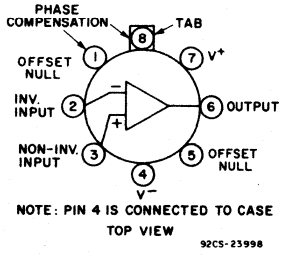
The RCA-CA101, CA201, and CA301A are general-purpose, high-gain operational amplifiers for use in military, industrial, and commerical applications.

These types, which are externally phase compensated, permit a choice of operation for optimum high-frequency performance at a selected gain; unity-gain compensation can be obtained with a single 30-pF capacitor.

All types are available in 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads ("DIL-CAN", S suffix). The CA301A is also available in the 8-lead dual-in-line plastic package ("MINI-DIP"), E suffix), and in chip form (H suffix).

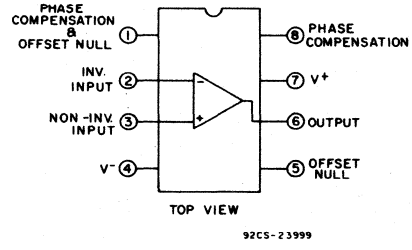
Applications:

- *Long-interval integrator*
- *Timers*
- *Sample-and-hold circuits*
- *Summing amplifiers*
- *Multivibrators*
- *Comparators*
- *Instrumentation*
- *AC/DC converters*
- *Inverting amplifiers*
- *Sine- & square-wave generators*
- *Capacitance multipliers & simulated inductors*



a — TO-5 Style package for all types

T-Suffix
S-Suffix



b — Plastic package for CA301A

E-Suffix

Fig. 1 - Functional diagrams.

Maximum Ratings, *Absolute Maximum Values at T_A = 25° C:*

DC SUPPLY VOLTAGE (Between V+ and V⁻ Terminals):
- CA101, CA201 ..... 44 V
- CA301A ..... 36 V

DC INPUT VOLTAGE ..... ±15 V
(For supply voltages less than ±15 V, the Input Voltage rating is equal to the DC Supply Voltage)
DIFFERENTIAL INPUT VOLTAGE ..... ±30 V
OUTPUT SHORT-CIRCUIT DURATION ..... Indefinite*
DEVICE DISSIPATION:
- UP TO T_A = 75° C ..... 500 mW
- Above T_A = 75° C Derate linearly at ..... 6.67 mW/° C

AMBIENT TEMPERATURE RANGE:
- Operating —
  - CA101 ..... -55 to +125° C
  - CA201, CA301A ..... 0 to +70° C
- Storage (All types) ..... -65 to +150° C

LEAD TEMPERATURE (During Soldering):
- At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265° C

* At $T_A \leq 70°$ C and $T_C \leq 125°$ C (CA101); $T_A \leq 55°$ C and $T_C \leq 70°$ C (CA201, CA301A).

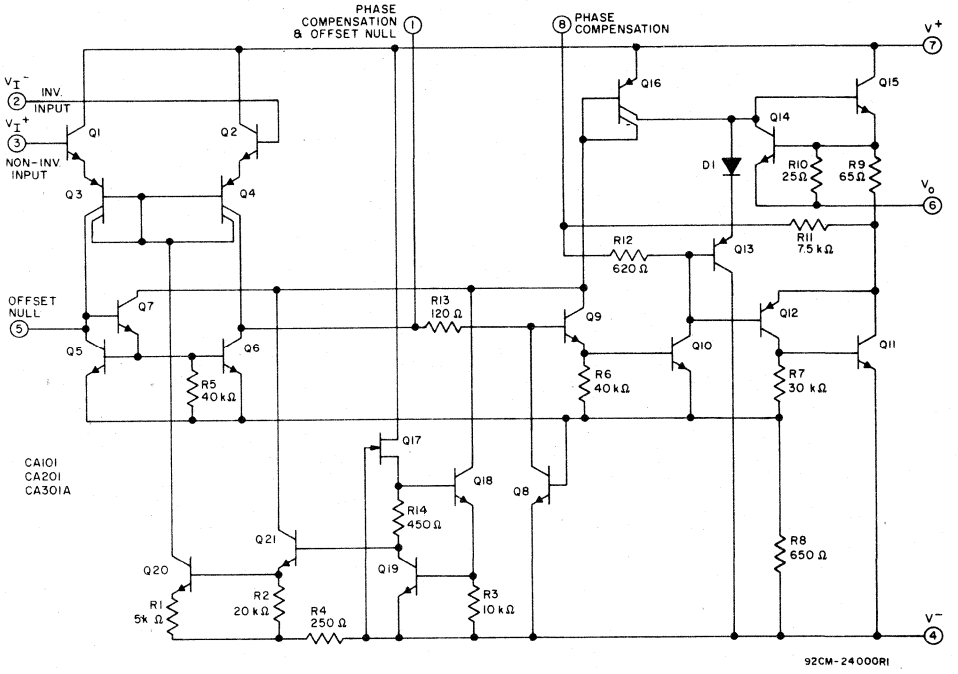


Fig. 2 - Schematic diagram.

CA101, CA201, CA301A Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	TEST CONDITIONS Δ	LIMITS									UNITS
	Supply Voltage (V±) = 5 to 15 V	CA101			CA201			CA301A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage V_{IO}	T_A=25°C $R_S \leq 10k\Omega$	—	1	5	—	2	7.5	—	—	—	mV
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	—	2	7.5	
	$R_S \leq 10k\Omega$	—	—	6	—	—	10	—	—	—	
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	—	—	10	
Average Temperature Coefficient of Input Offset Voltage αV_{IO}	$R_S \leq 10k\Omega$	—	6	—	—	10	—	—	—	—	μV/°C
	$R_S \leq 50\Omega$	—	3	—	—	6	—	—	—	—	
		—	—	—	—	—	—	—	6	30	
Average Temperature Coefficient of Input Offset Current αI_{IO}	-55°C to +25°C	—	—	—	—	—	—	—	—	—	nA/°C
	0°C to +25°C	—	—	—	—	—	—	—	0.02	0.6	
	+25°C to +70°C	—	—	—	—	—	—	—	0.01	0.3	
	+25°C to +125°C	—	—	—	—	—	—	—	—	—	
Input Offset Current I_{IO}	T_A = 0°C	—	—	—	—	150	750	—	—	—	nA
	T_A = 25°C	—	40	200	—	100	500	—	3	50	
	T_A = 70°C	—	—	—	—	50	400	—	—	—	
	T_A = 125°C	—	10	200	—	—	—	—	—	—	
		—	—	—	—	—	—	—	—	70	
	T_A = -55°C	—	100	500	—	—	—	—	—	—	
Input Bias Current I_{IB}	T_A = -55°C	—	0.28	1.5	—	—	—	—	—	—	μA
	T_A = 0°C	—	—	—	—	0.32	2	—	—	—	
	T_A = 25°C	—	0.12	0.5	—	0.25	1.5	—	0.07	0.25	
		—	—	—	—	—	—	—	—	0.3	
Supply Current $I_\pm$	T_A=25°C $V_\pm$=15V	—	—	—	—	—	—	—	1.8	3	mA
	$V_\pm$=20V	—	1.8	3	—	1.8	3	—	—	—	
	T_A=125°C $V_\pm$=20V	—	1.2	2.5	—	—	—	—	—	—	
Open-Loop Differential Voltage Gain A_{OL}	T_A=25°C $V_\pm$=15V V_O=±10V $R_L \geq 2k\Omega$	50	160	—	20	150	—	25	160	—	V/mW
	$V_\pm$=15V V_O=±10V $R_L \geq 2k\Omega$	25	—	—	15	—	—	15	—	—	
Input Resistance R_I	T_A=25°C	0.3	0.8	—	0.1	0.4	—	0.5	2	—	MΩ
Output Voltage Swing V_{OPP}	$V_\pm$=15V R_L=10kΩ	±12	±14	—	±12	±14	—	±12	±14	—	V
	$V_\pm$=15V R_L=2kΩ	±10	±13	—	±10	±13	—	±10	±13	—	
Common-Mode Input-Voltage Range V_{ICR}	$V_\pm$=15V	±12	—	—	±12	—	—	±12	—	—	V
	$V_\pm$=20V	—	—	—	—	—	—	—	—	—	
Common-Mode Rejection Ratio CMRR	$R_S \leq 10k\Omega$	70	90	—	65	90	—	—	—	—	dB
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	70	90	—	
Supply-Voltage Rejection Ratio PSRR	$R_S \leq 10k\Omega$	70	90	—	70	90	—	—	—	—	dB
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	70	90	—	

Δ Characteristics applicable over operating temperature range (T_A) as shown below, unless otherwise specified:
CA101: -55 to +125°C; CA201, CA301A: 0 to 70°C

TYPICAL STATIC CHARACTERISTICS

TYPE CA101

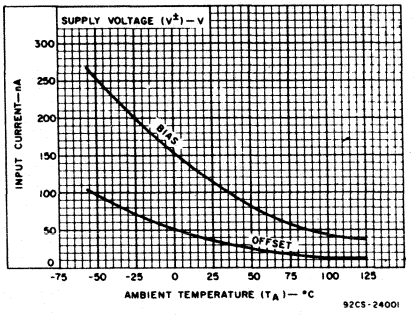


Fig. 3 - Input current (I_{IO}, I_{IB}) vs. temperature.

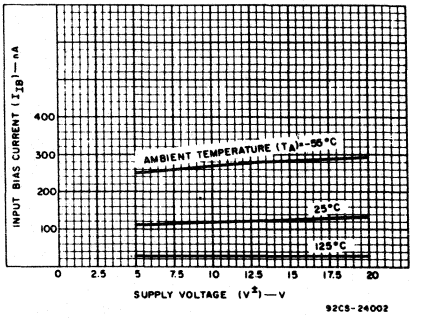


Fig. 4 - Input bias current vs. supply voltage.

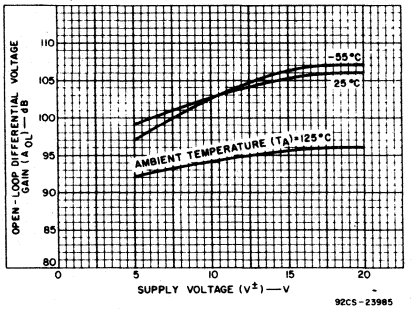


Fig. 5 - Voltage gain vs. supply voltage.

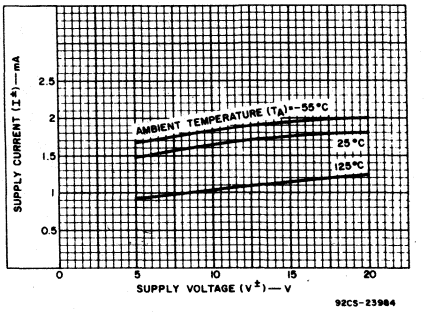


Fig. 6 - Supply characteristics.

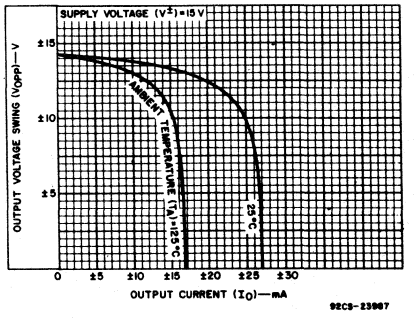


Fig. 7 - Output characteristics.

TYPE CA201

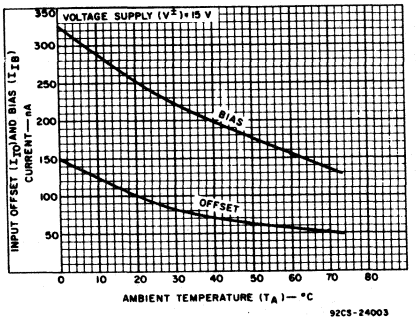


Fig. 8 - Input current (I_{IO}, I_{IB}) vs. temperature.

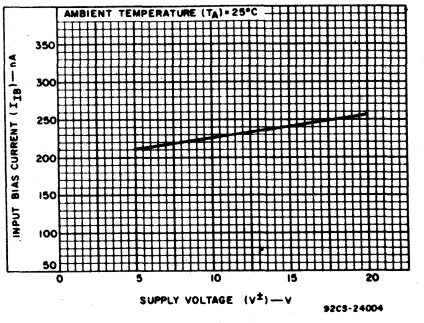


Fig. 9 - Input bias current (I_{IB}) vs. supply voltage.

CA101, CA201, CA301A Types

TYPICAL STATIC CHARACTERISTICS (Cont'd)

TYPE CA201

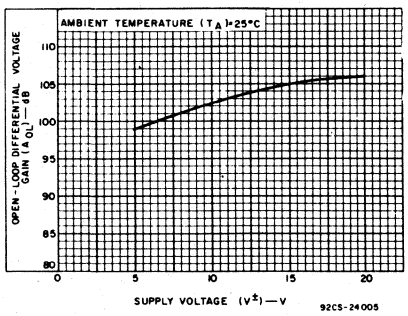


Fig. 10 - Voltage gain vs. supply voltage.

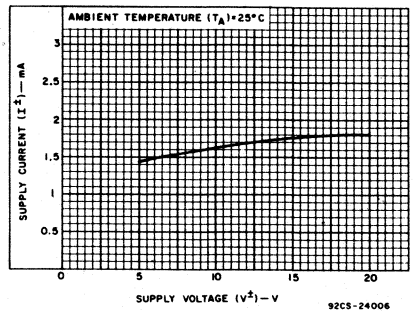


Fig. 11 - Supply characteristics.

TYPE CA301A

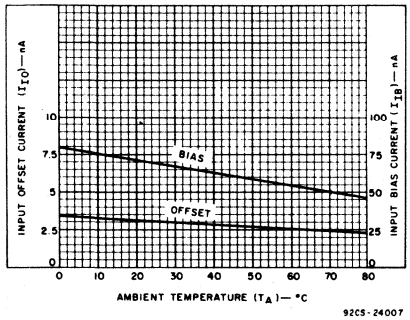


Fig. 12 - Input current (I_{IO}, I_{IB}) vs. temperature.

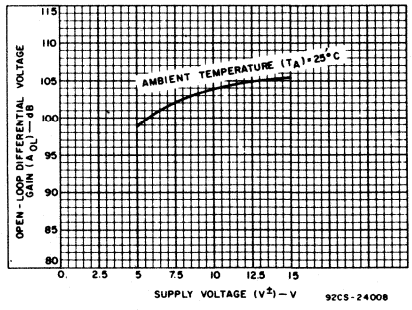


Fig. 13 - Voltage gain vs. supply voltage.

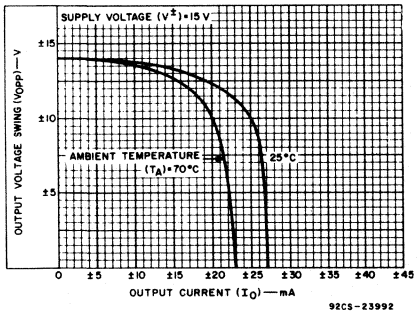


Fig. 14 - Output characteristics.

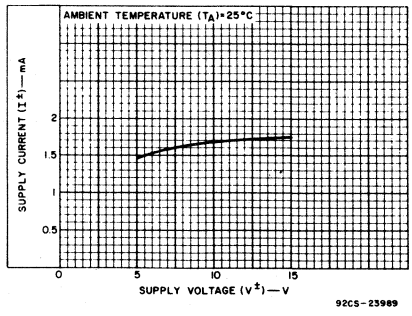


Fig. 15 - Supply characteristics.

TYPICAL DYNAMIC CHARACTERISTICS
TYPES CA101, CA201, CA301A

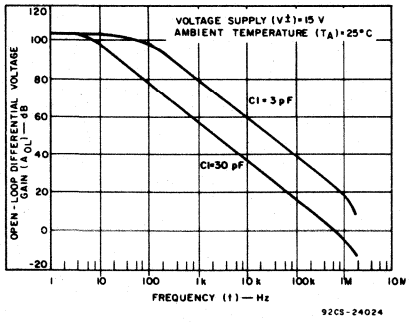


Fig. 16 - Voltage gain vs. frequency.

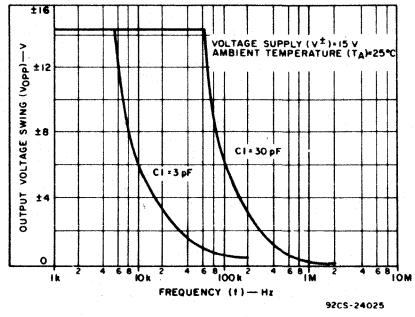


Fig. 17 - Output voltage swing vs. frequency.

TYPICAL DYNAMIC CHARACTERISTICS (Cont'd) FOR TYPES CA101, CA201 AND CA301A

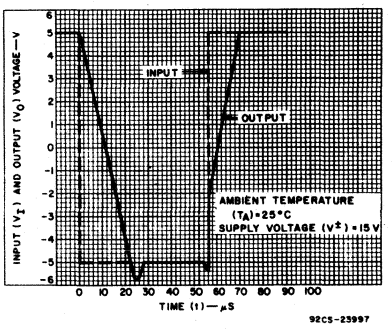


Fig. 18 - Voltage follower pulse response.

TYPE CA301A

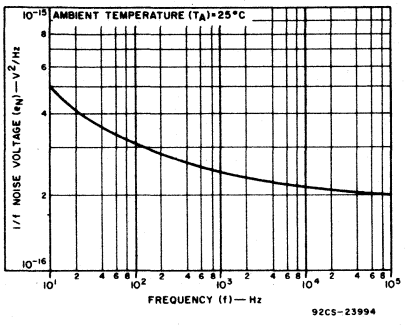


Fig. 19 - 1/f noise voltage vs. frequency.

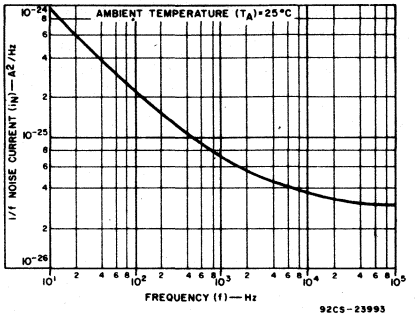
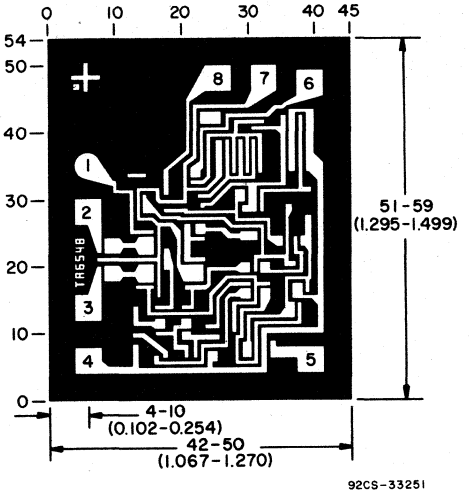


Fig. 20 - 1/f noise current vs. frequency.



Dimensions and pad layout for CA301H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

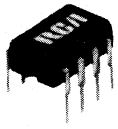
CA307

S-Suffix Types
(DIL-CAN)

H-1787

T-Suffix Types
(TO-5 Style)

H-1528



G-Suffix Types
E-Suffix Types
(Mini-DIP)

H-1817

Operational Amplifier

For Military, Industrial, and Commerical Applications

Applications:

- *Long-interval integrators*
- *Timers*
- *Sample-and-hold circuits*
- *Summing amplifiers*
- *Multivibrators*

The RCA CA307 is a general-purpose operational amplifier intended for use in military, industrial, and commerical applications. A 30-pF on-chip capacitor provides internal frequency compensation.

The CA307 is available in 8-lead TO-5 style packages with standard leads (T suffix), with dual-in-line formed leads ("DIL-CAN", S suffix), in the 8-lead dual-in-line plastic package ("MINI-DIP", E suffix), and in chip form (H suffix).

The CA307 is a direct replacement for industry type 307 in packages with similiar terminal arrangements.

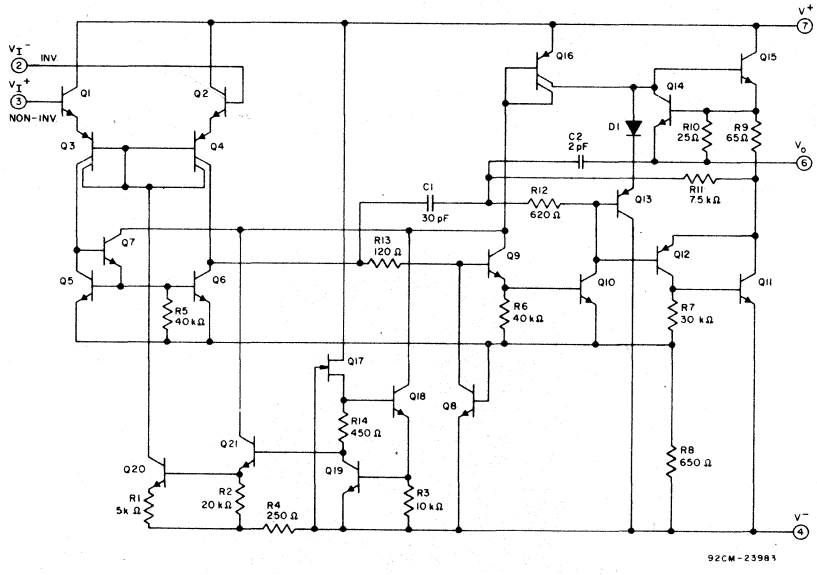


Fig. 1 - Schematic diagram of CA307.

Maximum Ratings, *Absolute Maximum Values at T_A = 25° C:*

DC SUPPLY VOLTAGE (Between V+ and V⁻ Terminals):
CA307 ..... 36 V
DC INPUT VOLTAGE ..... ±15 V
(For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage)
DIFFERENTIAL INPUT VOLTAGE ..... ±30 V
OUTPUT SHORT-CIRCUIT DURATION* ..... Indefinite
DEVICE DISSIPATION UP TO T_A = 70° C ..... 500 mW
Above T_A = 70° C Derate linearly at ..... 6.67 mW/° C
AMBIENT TEMPERATURE RANGE:
Operating ..... 0° C to +70° C†
Storage ..... -65° C to +150° C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265° C

*For type CA307 continuous short circuit is allowed for Case Temperature to +70° C and ambient temperature to +55° C.
†Types CA307 E, S, and T can be operated over the temperature range of -55 to +125° C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70° C.

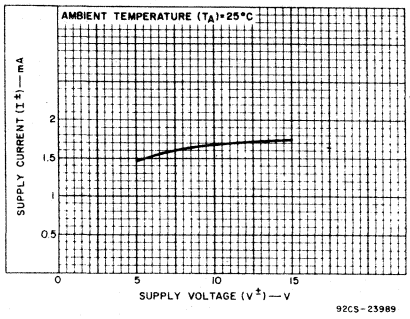


Fig. 2 - Supply current vs. supply voltage.

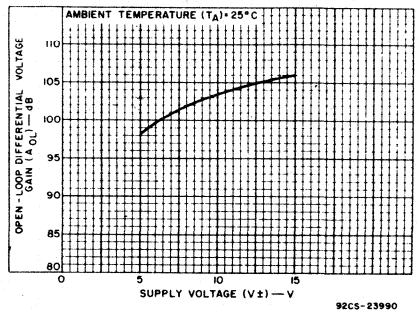


Fig. 3 - Open-loop differential voltage gain vs. supply voltage.

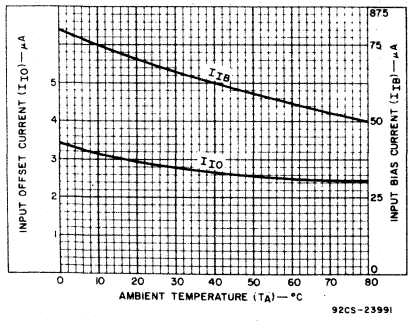


Fig. 4 - Input offset and input bias current vs. ambient temperature.

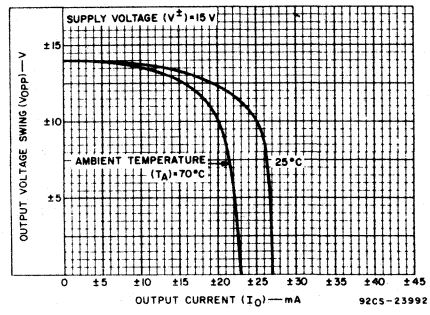


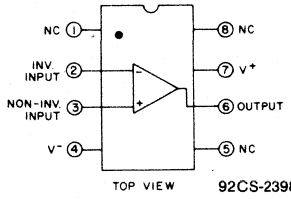
Fig. 5 - Output voltage swing vs. output current.

CA307

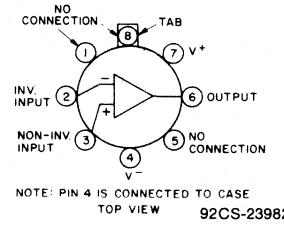
ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS△	LIMITS			UNITS
		Supply Voltage (V±) = 5 V to 15 V	CA307			
			Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	T_A = 25° C, $R_S \leq$ 50 kΩ	—	2	7.5	mV
		$R_S \leq$ 50 kΩ	—	—	10	
Average Temperature Coefficient of Input Offset Voltage	αV_{IO}		—	6	30	μV/° C
Input Offset Current	I_{IO}		—	—	70	nA
		T_A = 25° C	—	3	50	
Average Temperature Coefficient of Input Offset Current	αI_{IO}	+25 to 70° C	—	0.01	0.3	nA/° C
		0 to +25° C	—	0.02	0.6	
Input Bias Current	I_{IB}		—	—	300	nA
		T_A = 25° C	—	70	250	
Supply Current	I±	T_A = +125° C, V± = 20 V	—	—	—	mA
		T_A = 25° C, V± = 15 V	—	1.8	3	
Open-Loop Differential Voltage Gain	A_{OL}	V± = 15 V, V_O = ±10V, $R_L \geq$ 2kΩ	15	—	—	V/mV
		V±=15V, V_O=±10 V, R_L≥2kΩ,T_A=25° C	25	160	—	
Input Resistance	R_I	T_A = 25° C	0.5	2	—	MΩ
Output Voltage Swing	V_{OPP}	V± = 15 V, R_L = 10 kΩ	±12	±14	—	V
		V± = 15 V, R_L = 2 kΩ	±10	±13	—	
Input Voltage Range	V_{ICR}	V± = 15 V	±12	—	—	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq$ 50 kΩ	70	90	—	dB
Supply-Voltage Rejection Ratio	PSRR	$R_S \leq$ 50 kΩ	70	96	—	dB

△Characteristics applicable over operating temperature range T_A = 0 to 70° C unless otherwise specified.



FUNCTIONAL DIAGRAM FOR PLASTIC PACKAGE



FUNCTIONAL DIAGRAM FOR TO-5 STYLE PACKAGES

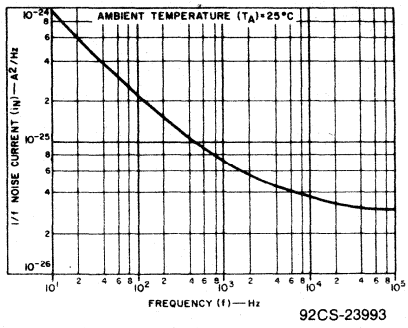


Fig. 6 - 1/f noise current vs. frequency.

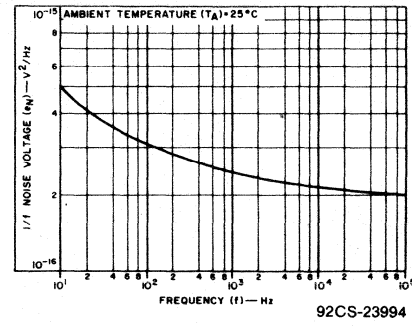


Fig. 7 - 1/f noise voltage vs. frequency.

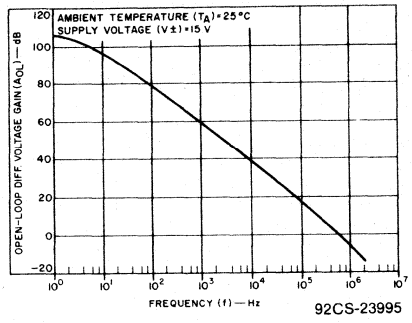


Fig. 8 - Open-loop differential voltage gain vs. frequency.

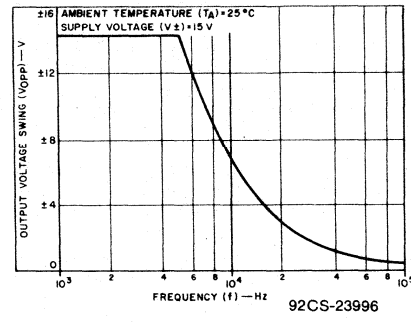


Fig. 9 - Output voltage swing vs. frequency.

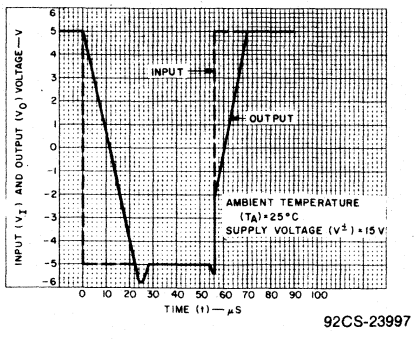
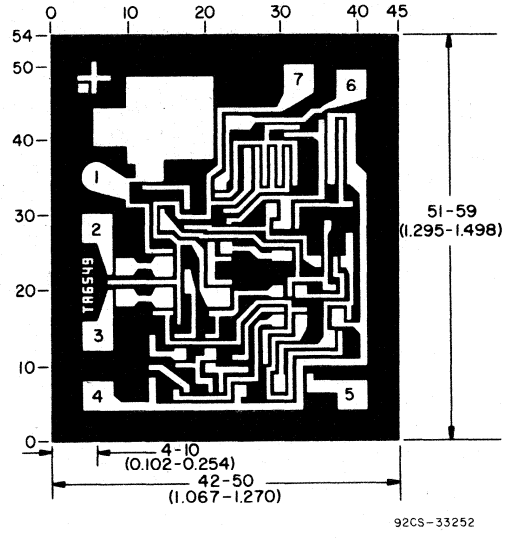


Fig. 10 - Input and output voltage vs. time.

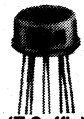


Dimensions and pad layout for CA307H.

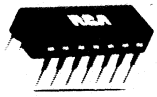
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA741, CA747, CA748, CA1458, CA1558 Types

(E Suffix)
8-LEAD DIP
(MINI-DIP)
H-1817



(T Suffix)
8-LEAD
TO-5
H-1528



(E Suffix)
14-LEAD DIP
H-1517

(S Suffix)
8-LEAD
TO-5
(DIL-CAN)
H-1787

Operational Amplifiers

High-Gain Single and Dual Operational Amplifiers
For Military, Industrial and Commerical Applications

Features:

- *Input bias current (all types):*
  500 nA max.
- *Input offset current (all types):*
  200 nA max.

Applications:

- *Comparator*
- *DC amplifier*
- *Integrator or differentiator*
- *Multivibrator*
- *Narrow-band or band-pass filter*
- *Summing amplifier*

The RCA-CA1458, CA1558 (dual types); CA741C, CA741 (single-types); CA747C, CA747 (dual types); and CA748C, CA748 (single types) are general-purpose, high-gain operational amplifiers for use in military, industrial, and commercial applications.

These monolithic silicon integrated-circuit devices provide output short-circuit protection and latch-free operation. These types also feature wide common-mode and differential-mode signal ranges and have low-offset voltage nulling capability when used with an appropriately valued potentiometer. A 5-megohm potentiometer is used for offset nulling types CA748C, CA748 (See Fig. 10); a 10-kilohm potentiometer is used for offset nulling types CA741C, CA741, CA747CE, CA747E (See Fig. 9); and types CA1458, CA1558, CA747CT, have no specific terminals for offset nulling. Each type consists of a differential-input amplifier that effectively drives a gain and level-shifting stage having a complementary emitter-follower output.

This operational amplifier line also offers the circuit designer the option of operation with internal or external phase compensation.

Types CA748C and CA748, which are externally phase compensated (terminals 1 and 8) permit a choice of operation for improved bandwidth and slew-rate capabilities. Unity gain with external phase compensation can be obtained with a single 30-pF capacitor. All the other types are internally phase-compensated.

RCA's manufacturing process make it possible to produce IC operational amplifiers with low-burst ("popcorn") noise characteristics. Type CA6741, a low-noise version of the CA741, gives limit specifications for burst noise in the data bulletin, File No. 530. Contact your RCA Sales Representative for information pertinent to other operational amplifier types that meet low-burst noise specifications.

RCA Type No.	No. of Ampl.	Phase Comp.	Offset Voltage Null	Min. A_{OL}	Max. V_{IO} (mV)	Operating-Temperature Range (°C)
CA1458	dual	int.	no	20k	6	0 to +70▲
CA1558	dual	int.	no	50k	5	−55 to +125
CA741C	single	int.	yes	20k	6	0 to +70▲
CA741	single	int.	yes	50k	5	−55 to +125
CA747C	dual	int.	yes*	20k	6	0 to +70▲
CA747	dual	int.	yes*	50k	5	−55 to +125
CA748C	single	ext.	yes	20k	6	0 to +70▲
CA748	single	ext.	yes	50k	5	−55 to +125

*In the 14-lead dual-in-line plastic package only.

▲All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

CA741, CA747, CA748, CA1458, CA1558 Types

ORDERING INFORMATION

When ordering any of these types, it is important that the appropriate suffix letter for the package required be affixed to the type number. For example: If a CA1458 in a straight-lead TO-5 style package is desired, order CA1458T.

TYPE NO.	PACKAGE TYPE AND SUFFIX LETTER							FIG. NO.
	TO-5 STYLE			PLASTIC		CHIP	BEAM-LEAD	
	8L	10L	DIL-CAN	8L	14L			
CA1458	T		S	E		H		1d, 1h
CA1558	T		S	E				1d, 1h
CA741C	T		S	E		H		1a, 1e
CA741	T		S	E			L	1a, 1e
CA747C		T			E	H		1b, 1f
CA747		T			E			1b, 1f
CA748C	T		S	E		H		1c, 1g
CA748	T		S	E				1c, 1g

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^\circ C$:

DC Supply Voltage (between V^+ and V^- terminals):
- CA741C, CA747C▲, CA748C, CA1458▲ . . . . . 36 V
- CA741, CA747▲, CA748, CA1558▲ . . . . . 44 V

Differential Input Voltage . . . . . ±30 V
DC Input Voltage* . . . . . ±15 V
Output Short-Circuit Duration . . . . . Indefinite
Device Dissipation:
- Up to 70°C (CA741C, CA748C) . . . . . 500 mW
- Up to 75°C (CA741, CA748) . . . . . 500 mW
- Up to 30°C (CA747) . . . . . 800 mW
- Up to 25°C (CA747C) . . . . . 800 mW
- Up to 30°C (CA1558) . . . . . 680 mW
- Up to 25°C (CA1458) . . . . . 680 mW

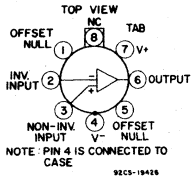
For Temperatures Indicated Above . . . . . Derate linearly 6.67 mW/°C
Voltage between Offset Null and V^- (CA741C, CA741, CA747CE) . . . . . ±0.5 V
Ambient Temperature Range:
- Operating – CA741, CA747E, CA748, CA1558 . . . . . −55 to +125 °C
- CA741C, CA747C, CA748C, CA1458 . . . . . 0 to +70 °C†
- Storage . . . . . −65 to +150 °C

Lead Temperature (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . 265 °C

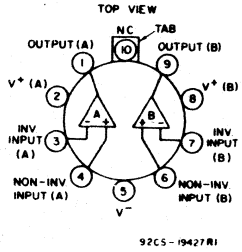
* If Supply Voltage is less than ± 15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

▲ Voltage values apply for each of the dual operational amplifiers.

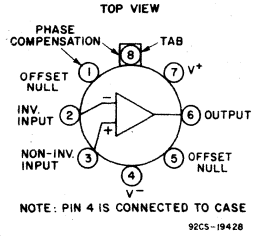
† All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.



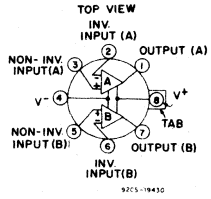
1a.–CA741CS,CA741CT,CA741S, & CA741T with internal phase compensation.



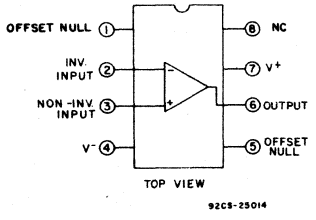
1b.–CA747CT and CA747T with internal phase compensation.



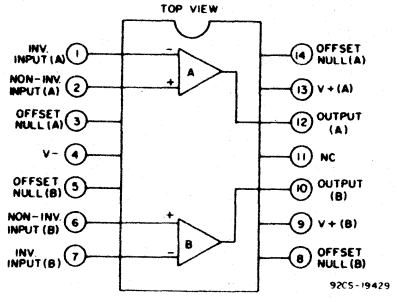
1c.–CA748CS, CA748CT,CA748S, and CA748T with external phase compensation.



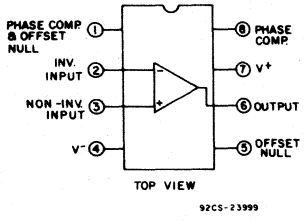
1d.–CA1458S,CA1458T,CA1558S, and CA1558T and internal phase compensation.



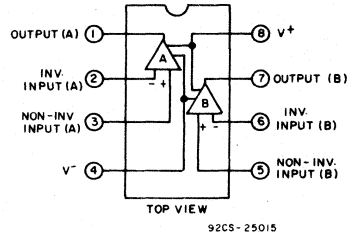
1e.–CA741C and CA741E with internal phase compensation.



1f.–CA747CE and CA747E with internal phase compensation.



1g.–CA748CE and CA748E with external phase compensation.



1h.–CA1458E and CA1558E with internal phase compensation.

Fig. 1 – Functional diagrams.

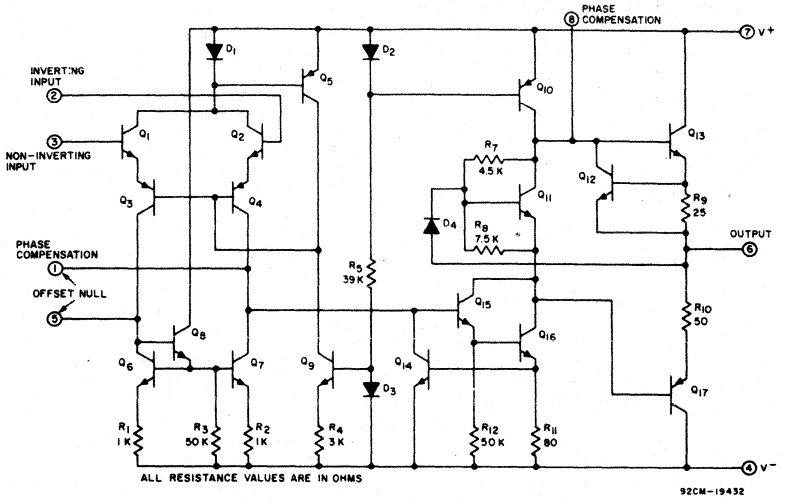


Fig.2—Schematic diagram of operational amplifier with external phase compensation for CA748C and CA748.

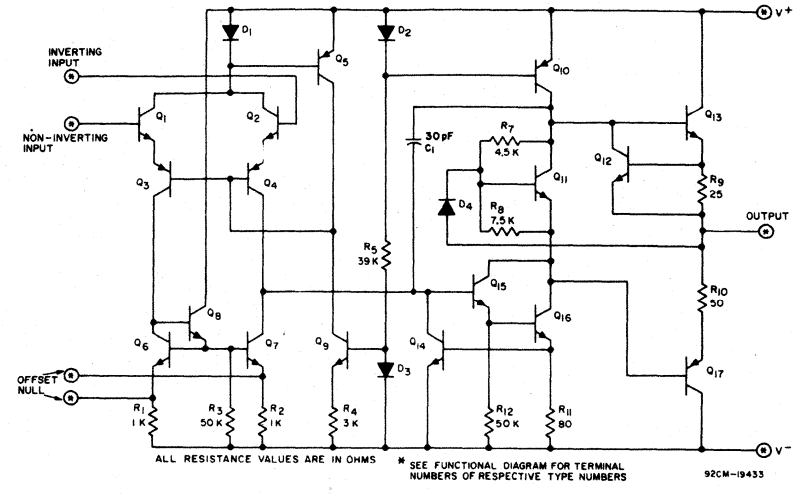


Fig.3—Schematic diagram of operational amplifiers with internal phase compensation for CA741C, CA741, and for each amplifier of the CA747C, CA747, CA1458, and CA1558.

CA741, CA747, CA748, CA1458, CA1558 Types

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	TEST CONDITIONS V± = ±15 V •	TYP. VALUES ALL TYPES	UNITS
Input Capacitance, C_I		1.4	pF
Offset Voltage Adjustment Range		±15	mV
Output Resistance, R_O		75	Ω
Output Short-Circuit Current		25	mA
Transient Response: Rise Time, t_r	Unity gain, V_I = 20 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF	0.3	μs
Transient Response: Overshoot		5	%
Slew Rate, SR: Closed-loop	$R_L \geq$ 2 kΩ	0.5	V/μs
Slew Rate, SR: Open-loop▲		40	

▲ Open-loop slew rate applies only for types CA748C and CA748.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, V^+ = 15 V, V^- = −15 V	Ambient Temperature, T_A	LIMITS CA741C CA747C* CA748C CA1458* Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S \leq$ 10 kΩ	25 °C	–	2	6	mV
		0 to 70 °C	–	–	7.5	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		0 to 70 °C	–	–	300	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		0 to 70 °C	–	–	800	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V_O = ±10 V	25 °C	20,000	200,000	–	
		0 to 70 °C	15,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		25 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq$ 10 kΩ	25 °C	70	90	–	dB
Supply-Voltage Rejection Ratio, PSRR	$R_S \leq$ 10 kΩ	25 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq$ 10 kΩ	25 °C	±12	±14	–	V
	$R_L \geq$ 2 kΩ	25 °C	±10	±13	–	
		0 to 70 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
Device Dissipation, P_D		25 °C	–	50	85	mW

* Values apply for each section of the dual amplifiers.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, $V^+ = 15$ V, $V^- = -15$ V	Ambient Temperature, T_A	LIMITS CA741 CA747* CA748 CA1558* Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S = \leq 10\,k\Omega$	25 °C	–	1	5	mV
		−55 to +125 °C	–	1	6	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		−55 °C	–	85	500	
		+125 °C	–	7	200	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		−55 °C	–	300	1500	
		+125 °C	–	30	500	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq 2\,k\Omega$ $V_O = \pm 10$ V	25 °C	50,000	200,000	–	
		−55 to +125 °C	25,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		−55 to +125 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq 10\,k\Omega$	−55 to +125 °C	70	90	–	dB
Supply Voltage Rejection Ratio, PSRR	$R_S \leq 10\,k\Omega$	−55 to +125 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq 10\,k\Omega$	−55 to +125 °C	±12	±14	–	V
	$R_L \geq 2\,k\Omega$	−55 to +125 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
		−55 °C	–	2	3.3	
		+125 °C	–	1.5	2.5	
Device Dissipation, P_D		25 °C	–	50	85	mW
		−55 °C	–	60	100	
		+125 °C	–	45	75	

* Values apply for each section of the dual amplifiers.

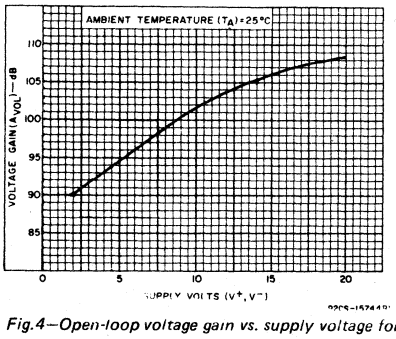


Fig.4—Open-loop voltage gain vs. supply voltage for all types except CA748 and CA748C.

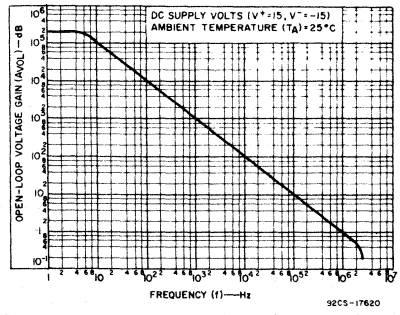


Fig.5—Open-loop voltage gain vs. frequency for all types except CA748 and CA748C.

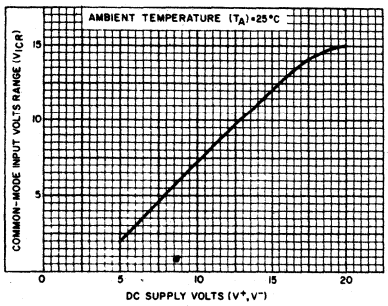


Fig.6—Common-mode input voltage range vs. supply voltage for all types.

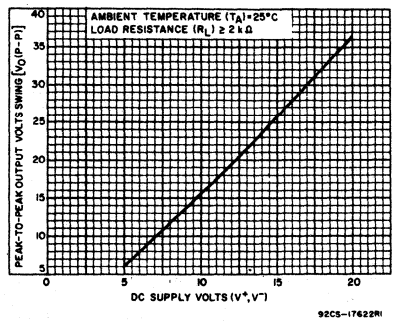


Fig.7—Peak-to-peak output voltage vs. supply voltage for all types except CA748 and CA748C.

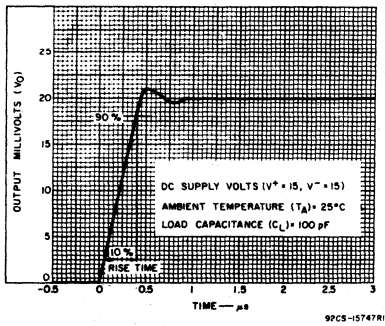


Fig.8—Output voltage vs. transient response time for CA741C and CA741.

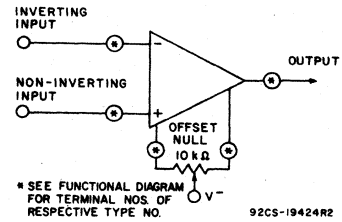


Fig.9—Voltage offset null circuit for CA741C, CA741, CA747CE, and CA747E.

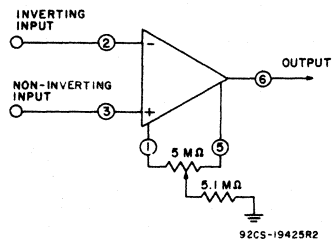


Fig.10—Voltage-offset null circuit for CA748C and CA748.

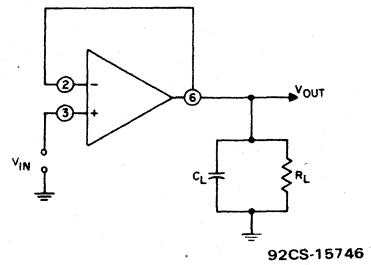


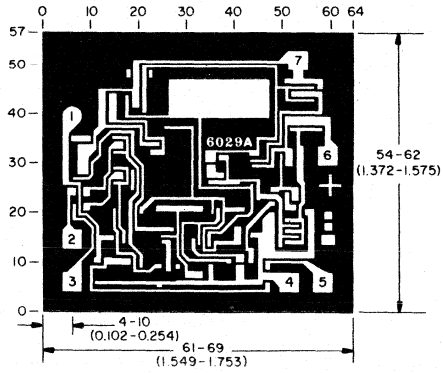
Fig.11—Transient response test circuit for all types.

CA741, CA747, CA748, CA1458, CA1558 Types

CHIP PHOTOS

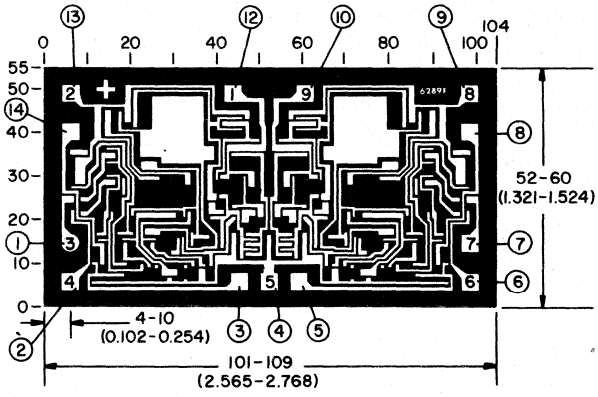
Dimensions and Pad Layouts

CA741CH



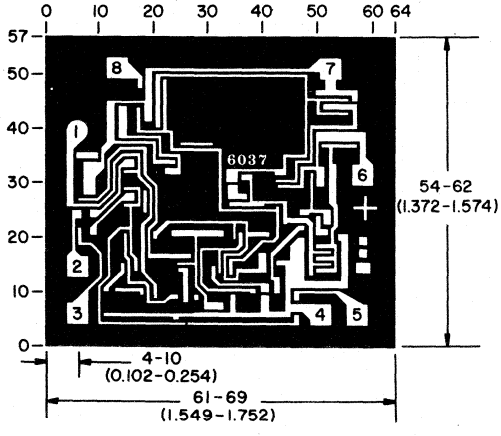
92CS-33259

CA747CH



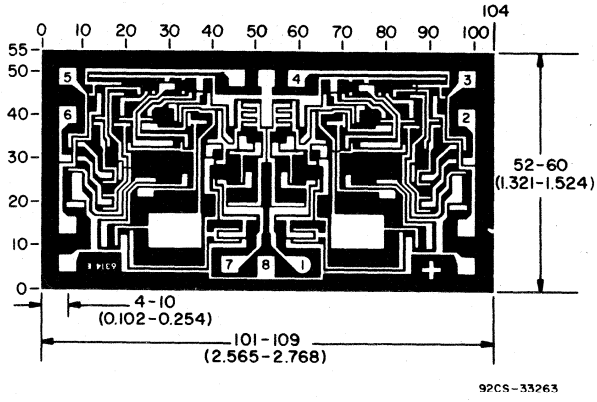
NOTE: NOS. IN PADS ARE FOR 10-LEAD TO-5
NOS. OUTSIDE OF CHIP ARE FOR 14-LEAD DIP

92CM-33260



92CS-33261

CA748CH

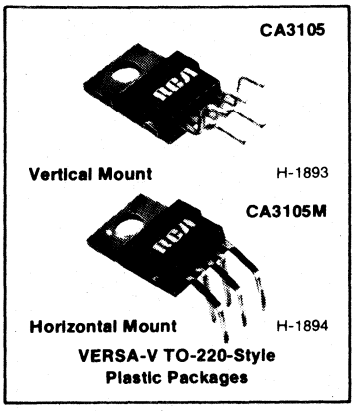


92CS-33263

CA1458H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3105, CA3105M



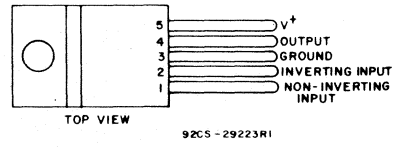
High-Power Operational Amplifier

Features

- *Output short circuit and thermal overload protection*
- *Load dump voltage surge protection*
- *Output current capability of up to 3.5 A*
- *Compensated for gains > 30*
- *VERSA-V power transistor package–requires no electrical insulation*

The RCA-CA3105 is a monolithic silicon operational amplifier designed for driving loads as low as 1.6 ohms. It provides a high output current capability (up to 3.5 A), and rapid settling time. It is ideal for use in ac or dc servo amplifiers, deflection yoke drivers, programmable power supplies, power multivibrators, power dump flashers, etc.

The CA3105 is supplied in a 5-lead plastic TO-220-style VERSA-V package. All leads (except terminal 3) are electrically insulated from the mounting flange, eliminating the need for insulating hardware. The VERSA-V package is available with two lead configurations. The CA3105 has a vertical mount lead form, and the CA3105M has a horizontal mount lead form.



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE	28 V
OPERATING SUPPLY VOLTAGE	18 V
OUTPUT PEAK CURRENT:	
REPETITIVE	3.5 A
NON-REPETITIVE	4.5 A
POWER DISSIPATION, P_D @ T_A=90°C	15 W
THERMAL RESISTANCE, JUNCTION-TO-CASE	4°C/W
AMBIENT-TEMPERATURE RANGE:	
OPERATING	0 to +125°C
STORAGE	−40 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 12 s max.	260°C

ELECTRICAL CHARACTERISTICS @ T_A = 25° C, V_S = +10 V Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}		—	1.3	5.0	mV
Input Bias Current, I_B	$T_A \leq T_{MAX}$	24	30	35	nA
Input Offset Current, I_{IO}	V_{CM} = 0	—	2.6	7	nA
Voltage Gain, A_{OL}		76	80	84	dB
Output Voltage Swing, V_O	A_V = +1 R_L = 100 Ω	±8	±8.5	±8.8	V
	R_L=50 KΩ	±8	±8.7	±9	V
Common Mode Rejection Ratio, CMRR		64	65	67	dB
Power Supply Rejection Ratio, PSRR		53	55	60	dB
Quiescent Supply Current, I_S		65	85	100	mA
Input Capacitance, C_{in}	f = 1 MHz	—	5	—	pF
Slew Rate, SR	R_L = 100 Ω, A_V = +1	—	5	—	V/μs
Gain Bandwidth Product	A_{VL} = 0 dB, R_L = 100 Ω C_L = 100 pF, V_{IN} = 20, f = 1 kHz	—	5	—	MHz

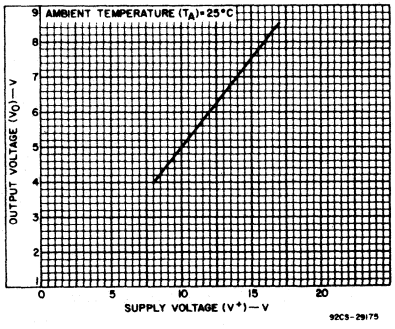


Fig. 1 - Typical quiescent output voltage as a function of supply voltage.

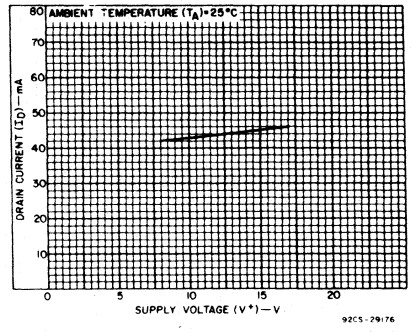


Fig. 2 - Typical quiescent drain current as a function of supply voltage.

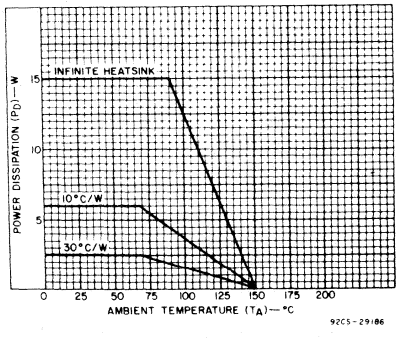


Fig. 3 - Maximum allowable power dissipation as a function of ambient temperature.

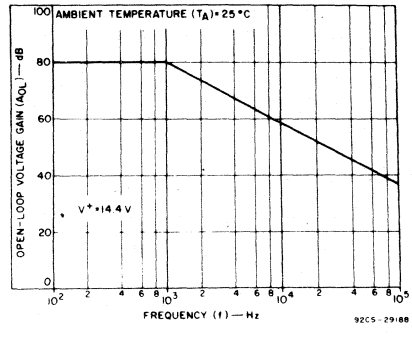
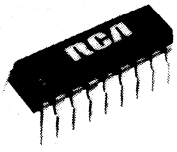


Fig. 4 - Open-loop voltage gain as a function of frequency.

CA3152E



H-1899

E-SUFFIX
18-Lead Dual-In-Line
Plastic Package

BiMOS Input Op-Amp, Frequency Band-Select Switch, and Quad Comparator

For Television Tuning Interfacing

Features:

- *Input op-amp: high impedance PMOS input transistors and internal reference bias*
- *Low input bias current and internal diode protection at op-amp inputs*
- *High op-amp output voltage swing (0.7-28.0 V dc) with 3-mA source or sink capability*
- *Three op-amp output voltage logic-controlled clamp levels*
- *Logic-controlled bandswitching with four separate outputs*
- *Two bandswitch output current sinks*
- *Two bandswitch current-limited output current sources*
- *Internally referenced quad comparator*
- *Low drive current input requirement*
- *Low output leakage*
- *High output current sink capability*
- *Bipolar and PMOS processes on a single chip*

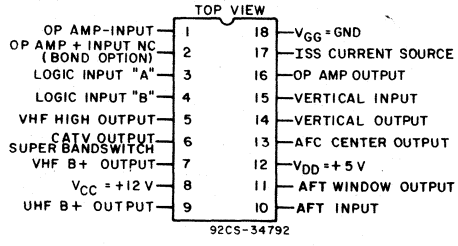
The RCA CA3152E* linear integrated circuit has three major sections for interfacing television tuning systems: an input op-amp, a band-select switch, and an internally referenced quad-comparator.

The op-amp output voltage has a wide dynamic range with a 3-mA source or sink capability and can be clamped to three discrete levels in response to logic inputs. The op-amp also has internal bias reference and phase compensation. High impedance PMOS input transistors are protected by input limiting diode clippers.

The band-select switch has two logic inputs controlling four outputs: VHF B+, VHF HIGH, SUPERBAND CATV, AND UHF B+. The VHF B+ and UHF B+ outputs are current sources which are short-circuit protected by current limiting. VHF HIGH and SUPERBAND CATV outputs are current sinks with low off-state leakage.

The quad comparator features internal reference bias, low output leakage, and 6-mA current sinking capability. The outputs of two of the comparators are internally connected to form a window comparator.

The CA3152E is supplied in an 18-lead dual-in-line plastic package.



TERMINAL ASSIGNMENT

*Formerly RCA Dev. Type No. TA10702

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_A=25° C)

SUPPLY CURRENT (I_{SS})	20 mA
SUPPLY VOLTAGE (V_{CC}) (PIN 8)	+18 V dc
SUPPLY VOLTAGE (V_{DD}) (PIN 12)	+8 V dc
DEVICE DISSIPATION PER PACKAGE (P_D):	
UP TO 55° C	750 mW
ABOVE 55° C (Derate Linearly)	7.9 mW/° C
AMBIENT TEMPERATURE RANGE:	
OPERATING (T_A)	0 to +70 °C
STORAGE (T_{stg})	−55 to +150 °C

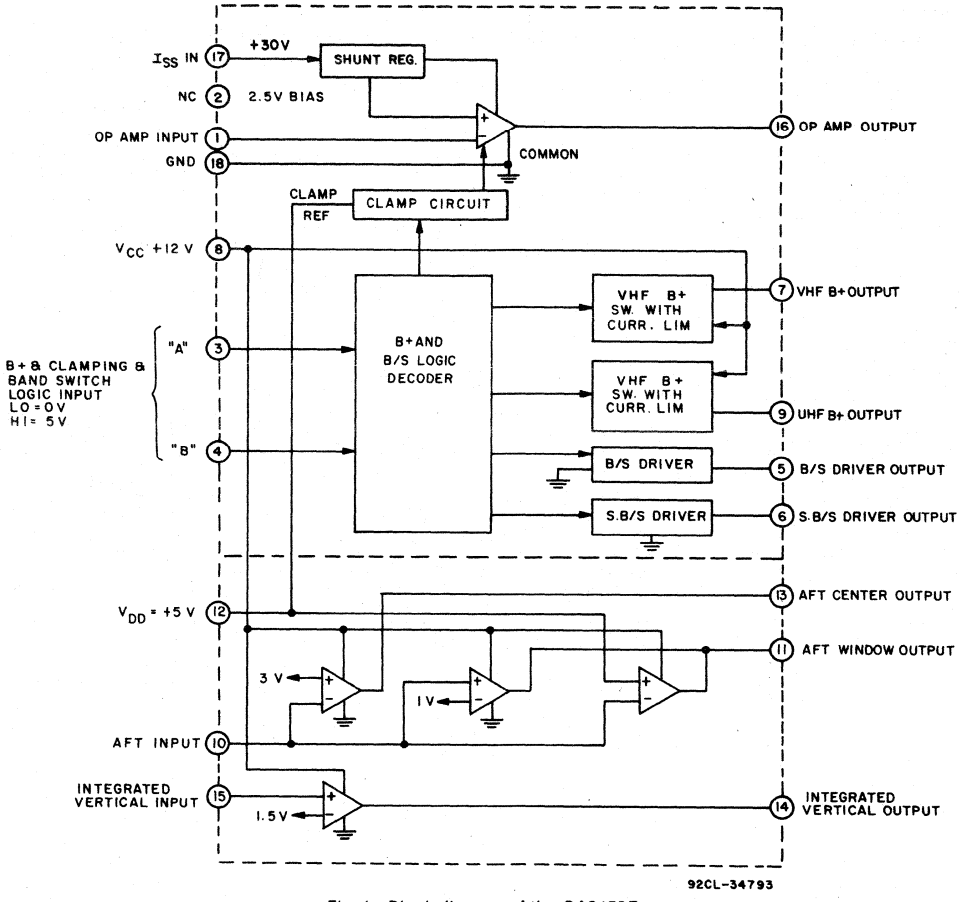


Fig. 1 - Block diagram of the CA3152E.

LOGIC TABLE FOR BANDSWITCH AND OP-AMP OUTPUTS

Inputs				Outputs					
Op-Amp Pin 1	V_A Pin 3	V_B Pin 4	BAND	VHF B+ Source Pin 7	UHF B+ Source Pin 9	VHF High Sink Pin 5	Super Bandswitch CATV Sink Pin 6	Pin 16 Voltage Min.	Pin 16 Voltage Max.
1	0	0	Low VHF	ON	OFF	OFF	OFF	0.7 V	1.1 V
1	0	1	High VHF Midband CATV	ON	OFF	ON	OFF	1.6 V	2.1 V
1	1	0	Superband CATV	ON	OFF	ON	ON	4.9 V	5.75 V
1	1	1	UHF	OFF	ON	ON	OFF	0.7 V	1.1 V
0	0	0		ON	OFF	OFF	OFF	28 V	34 V
0	0	1		ON	OFF	ON	OFF	28 V	34 V
0	1	0		ON	OFF	ON	ON	28 V	34 V
0	1	1		OFF	ON	ON	OFF	28 V	34 V

Logic 1=5 V
Logic 0=0 V

CA3152E

COMMON SECTION

ELECTRICAL CHARACTERISTICS @ T_A=25°C; I_{SS}=9 mA, V_{DD}=+5 V dc, V_{CC}=+12 V dc

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		Min.	Max.	
I_{CC} Supply Current, I_8	All Outputs Open	0.1	2	mA
I_{DD} Supply Current, I_{12}	All Outputs Open	0.1	1.5	mA
Tuning Voltage Supply Regulator, V_{17}	I_{SS}=9 mA	29	35	V dc
V_{17} Regulation, ΔV_{17}	V_1=V_{17} @ I_{SS}=6 mA, V_2=V_{17} @ I_{SS}=12 mA, ΔV_{17}=$\lvert V_1-V_2 \rvert$	0	0.8	V dc

OP-AMP SECTION

ELECTRICAL CHARACTERISTICS @ T_A=25°C; I_{SS}=9 mA, V_{DD}=+5 V dc, V_{CC}=+12 V dc
V_H=2.4 V Min., V_L=0.8 V Max., V_A=Pin 3, V_B=Pin 4

CHARACTERISTIC	V_A	V_B	TEST CONDITIONS	LIMITS		UNITS
				Min.	Max.	
Bias Voltage, V_1 Bias	V_L	V_L	Pin 1 through 10 KΩ to Pin 16	2.35	2.65	V dc
Bias Current, I_1 Bias	V_L	V_L	Pin 1 to Ground	—	100	pA
Output Source Current, I_{16} Source	V_L	V_L	V_1=0 V, V_{16}=17.5 V dc	−3	—	mA
Output Sink Current, I_{16} Sink	V_L	V_L	V_1=5 V dc, V_{16}=17.5 V dc	3	—	mA
Open Loop Voltage Gain, V_{16} A_{OL}	V_L	V_L	I_{SS}=10 mA, R_L=10 KΩ, V_1=2.5 V dc, V_{16}=17.5 V dc	1	—	V/mV
High Clamp Output Voltage, V_{16} HCL	V_L	V_L	V_1=0 V dc	28	34	V dc
Low Clamp Output Voltage, V_{16} CL1	V_L	V_L	V_1=5 V dc	0.7	1.1	V dc
Low Clamp Output Voltage, V_{16} CL2	V_L	V_H	V_1=5 V dc	1.6	2.1	V dc
Low Clamp Output Voltage, V_{16} CL3	V_H	V_L	V_1=5 V dc	4.9	5.75	V dc

BANDSWITCH SECTION

ELECTRICAL CHARACTERISTICS @ T_A=25°C; I_{SS}=9 mA, V_{DD}=+5 V dc, V_{CC}=+12 V dc
V_H=2.4 V Min., V_L=0.8 V Max., V_A=Pin 3, V_B=Pin 4, V_I=5 V

CHARACTERISTIC	V_A	V_B	TEST CONDITIONS	LIMITS		UNITS
				Min.	Max.	
Pin 7 ON (VHF ON)	V_H	V_L	I_7=−15 mA	11.3	—	V dc
Pin 9 ON (UHF ON)	V_H	V_H	I_9=−15 mA	11.3	—	V dc
Pin 7 OFF (VHF OFF)	V_H	V_H	I_7=1 mA	—	1.5	V dc
Pin 9 OFF (UHF OFF)	V_H	V_L	I_9=1 mA	—	1.5	V dc
VHF Short Circuit Current, I_7 SC	V_L	V_L	—	20	45	mA
UHF Short Circuit Current, I_9 SC	V_H	V_H	—	20	45	mA
V5 Saturation Voltage, V_5 SAT	V_H	V_L	I_5=2.5 mA	—	0.5	V dc
V6 Saturation Voltage, V_6 SAT	V_H	V_L	I_6=2.5 mA	—	0.5	V dc
Bandswitch Leakage Current, I_5 L	V_L	V_L	V_5=15 V dc	−0.2	1	μA
Superbandswitch Leakage Current, I_6 L	V_L	V_L	V_6=15 V dc	−0.2	1	μA
Logic Input Low Input Current, I_3 L	—	—	V_A=0 V dc, V_B=5 V dc	0	−30	μA
Logic Input Low Input Current, I_4 L	—	—	V_A=5 V dc, V_B=0 V dc	0	−30	μA
Logic Input High Input Current, I_3 H	—	—	V_A=5 V dc, V_B=0 V dc	—	1	μA
Logic Input High Input Current, I_4 H	—	—	V_A=0 V dc, V_B=5 V dc	—	1	μA

DC COMPARATOR SECTION
ELECTRICAL CHARACTERISTICS @ T_A=25° C; I_{SS}=9 mA, V_{DD}=+5 V dc, V_{CC}=+12 V dc

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		Min.	Max.	
Input Bias Current, I_{10} BIAS L	V_{10}=0 V dc	—	−750	nA
Input Bias Current, I_{10} BIAS H	V_{10}=6 V dc	+1	−0.450	mA
Input Bias Current, I_{15} BIAS L	V_{15}=0 V dc	0	−250	nA
Input Bias Current, I_{15} BIAS H	V_{15}=6 V dc	+1	−0.160	mA
Output Sink Current, I_{11} Sink	V_{10}=0 V dc, V_{11}=1.5 V dc	6	—	mA
Output Sink Current, I_{11} Sink	V_{10}=6 V dc, V_{11}=1.5 V dc	6	—	mA
Output Saturation Voltage, V_{11} SAT1	V_{10}=0 V dc, I_{11} SINK=4 mA	100	700	mV
Output Saturation Voltage, V_{11} SAT2	V_{10}=6 V dc, I_{11} SINK=4 mA	100	700	mV
Output Leakage Current, I_{11} LEAKAGE	V_{10}=2.25 V dc, V_{11}=12 V dc	−0.2	1.0	μA
Output Sink Current, I_{13} SINK	V_{10}=6 V dc, V_{13}=1.5 V dc	6	—	mA
Output Saturation Voltage, V_{13} SAT	V_{10}=6 V dc, I_{13} SINK=4 mA	100	700	mV
Output Leakage Current, I_{13} LEAKAGE	V_{10}=2.25 V dc, V_{13}=12 V dc	−0.2	1.0	μA
Output Sink Current, I_{14} SINK	V_{15}=0 V dc, V_{14}=1.5 V dc	6	—	mA
Output Saturation Voltage, V_{14} SAT	V_{15}=0 V dc, I_{14} SINK=4 mA	100	700	mV
Output Leakage Current, I_{14} LEAKAGE	V_{15}=2.25 V dc, V_{14}=12 V dc	−0.2	1.0	μA
AFT Center Reference Voltage, V_{13} REF	(See Fig. 2)	2.8	3.2	V dc
AFT Window Reference Voltage Low, V_{11} REF LOW	(See Fig. 2)	0.8	1.2	V dc
AFT Window Reference Voltage High, V_{11} REF HIGH	(See Fig. 2)	4.95	5.05	V dc
Vertical Output Reference, V_{14} REF	(See Fig. 2)	1.3	1.7	V dc

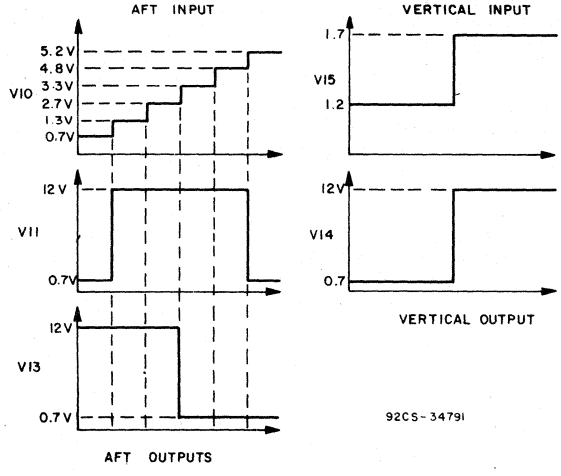
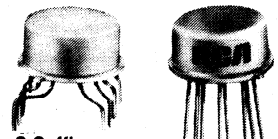


Fig. 2 - Quad comparator action.

CA3193, CA3193A, CA3193B Types



S Suffix
8-LEAD TO-5
with Dual-In-Line
Formed Leads
"DIL-CAN"
H-1787

T Suffix
8-LEAD TO-5
H-1528

E Suffix
8-LEAD Dual-
In-Line Plastic
Package "Mini-DIP"
H-1817

BiMOS Precision Operational Amplifier

FEATURES:

- *Low V_{IO}: 75 μV max. (CA3193B)*
  200 μV max. (CA3193A)
  500 μV max. (CA3193)
- *Low $\Delta V_{IO}/\Delta T$: 2 μV/° C max. (CA3193B)*
  3 μV/° C max. (CA3193A)
  5 μV/° C max. (CA3193)
- *Low I_{IO} and I_I*
- *Low $\Delta I_{IO}/\Delta T$: 50 pA/° C max. (CA3193B)*
  150 pA/° C max. (CA3193)
- *Low $\Delta I_I/\Delta T$: 0.5 nA/° C max. (CA3193B)*
  3.7 nA/° C max. (CA3193)
- *Extremely high gain:*
  120 dB min. (CA3193B)
  110 dB min. (CA3193A)
  100 dB min. (CA3193)
- *Low VIO vs. time*
- *High CMRR and PSRR*
- *Internally compensated: 1.2-MHz gain-bandwidth product*
- *Low input noise: 0.1 Hz to 10 Hz*
  Noise voltage: 0.36 μVp-p typ.
  Noise current: 12 pAp-p typ.

APPLICATIONS

- *Thermocouple preamplifiers*
- *Strain-gauge bridge amplifiers*
- *Summing amplifiers*
- *Differential amplifiers*
- *Bilateral current sources*
- *Log amplifiers*
- *Differential voltmeters*
- *Precision voltage references*
- *Active filters*
- *Buffers*
- *Integrators*
- *Sample-and-hold circuits*
- *Low frequency filters*

The CA3193B, CA3193A and CA3193 are ultra-stable, precision-instrumentation, operational amplifiers that employ both PMOS and bipolar transistors on a single monolithic chip. The CA3193-series amplifiers are internally phase-compensated and provide a gain-bandwidth product of 1.2 MHz. They are pin-compatible with the industry 741 series and many other IC op amps, and may be used as replacements for 741-series types in most applications.

The CA3193 series can also be used as functional replacements for op-amp types 725, 108A, OP-5, OP-7, LM11 and LM714 in many applications where nulling is not employed. Because of their low offset voltage and low offset voltage-versus-temperature coefficient, the CA3193-series amplifiers have a wider range of applications than most op amps and are particularly well suited for use as thermocouple amplifiers, high-gain filters, buffers, strain-gauge bridge amplifiers and precision voltage references.

The three types in the CA3193 series are functionally identical. The CA3193B, however, operates from supply voltages of ±3.5 V to ± 22 V and has an operating temperature range of -55° C to +125° C. The CA3193 and CA3193A operate from supply voltages of ± 3.5 V to ± 18 V and have operating temperature ranges of -25° C to +85° C and 0° C to +70° C, respectively.

The CA3193-series types are supplied in standard 8-lead TO-5-style (T suffix), 8-lead dual-in-line formed lead TO-5-style (DIL-CAN—S suffix) and 8-lead dual-in-line plastic (Mini-DIP—E suffix) packages.

Circuit Description
The block diagram of the CA3193 amplifier, Fig. 2, shows the voltage gain and supply current for each of its four amplifier stages. Simplified and complete schematic diagrams of the CA3193 amplifier are shown in Figs. 3 and 4, respectively.

Absolute-Maximum Ratings, *Absolute-Maximum Values at $T_A = 25°C$*

	CA3193	CA3193A	CA3193B	
DC Supply Voltage	±18	±18	±22	V
Differential-Mode Input Voltage	±5	±5	±5	V
Common-Mode DC Input Voltage	(V+ −4), V−	(V+ −4), V−	(V+ −4), V−	V
Input Terminal Current	1	1	1	mA
Device Dissipation				
Without Heat Sink				
Up to 55 °C	630	630	630	mW
Above 55 °C	Derate Linearly 6.67			mW/°C
Temperature Range	0 to 70	−25 to 85	−55 to 125	°C
Output Short-Circuit Duration*	Indefinite	Indefinite	Indefinite	
Lead Temperature (During Soldering) at distance of 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	±265	±265	±265	°C

*Short circuit may be applied to ground or to either supply.

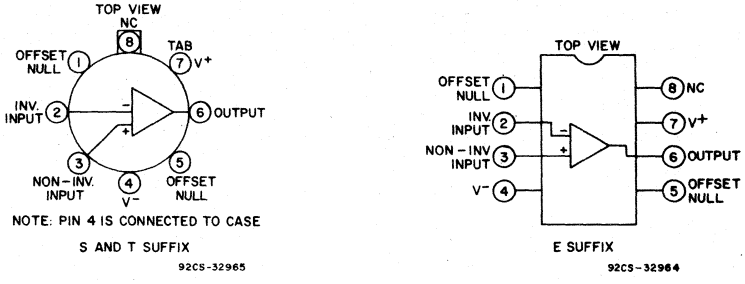


Fig. 1 — Functional diagram of CA3193 series.

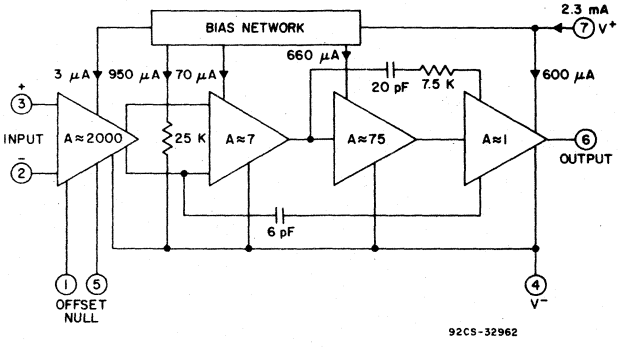


Fig. 2 — Block diagram of CA3193 series.

Circuit Description (cont'd)

A quad of physically cross-connected n-p-n transistors comprise the input-stage differential pair (Q1,Q2 in Figs. 3 and 4); this arrangement contributes to the low input offset-voltage characteristics of the amplifier. The ultra-high gain provided in the first stage ensures that subsequent stages cannot significantly influence the overall offset-voltage characteristics of the amplifier. High load impedances for the input-stage differential pair (Q1,Q2) are provided by the cascode-connected p-n-p transistors Q3,Q5 and Q4,Q6, thereby contributing to the high gain developed in the stage.

The second stage of the amplifier consists of a differential amplifier employing PMOS/FETs (Q7,Q8 in Figs. 3 and 4) with

CA3193, CA3193A, CA3193B Types

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 15$ V and $V^- = 15$ V unless otherwise specified.

CHARACTERISTIC	LIMITS									UNITS
	CA3193B			CA3193A			CA3193			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	40	75	—	140	200	—	300	500	μV
V_{IO} @ Max.Temp.	—	—	275	—	—	380	—	—	725	μV
Input Offset Voltage Temp.Coefficient, $\Delta V_{IO}/\Delta T$ (Over specified temperature range for each device)	—	0.60	2	—	1	3	—	1	5	μV/°C
Input Offset Current, I_{IO}	—	1	3	—	3	5	—	5	10	nA
$\|I_{IO}\|$ @ Max.Temp.	—	—	8	—	—	11	—	—	17	nA
Input Offset Current Temp. Coefficient, $\Delta I_{IO}/\Delta T$ (Over specified temperature range for each device)	—	0.01	0.05	—	0.03	0.10	—	0.04	0.15	nA/°C
Input Bias Current, I_I	—	6	15	—	10	20	—	20	40	nA
$\|I_B\|$ @ Max.Temp.	—	—	60	—	—	83	—	—	207	nA
Input Bias Current Temp. Coefficient, $\Delta I_I/\Delta T$	—	0.08	0.50	—	0.10	1.18	—	0.15	3.70	nA/°C
Input Noise Voltage, e_n p-p (0.1 to 10 Hz)	—	0.36	0.60	—	0.36	—	—	0.36	—	μV p-p
Input Noise Voltage Density, e_n										
$f_O = 10$ Hz	—	25	50	—	25	—	—	25	—	
$f_O = 100$ Hz	—	25	45	—	25	—	—	25	—	
$f_O = 1000$ Hz	—	24	45	—	24	—	—	24	—	nV/$\sqrt{\text{Hz}}$
$f_O = 10$ kHz	—	24	45	—	24	—	—	24	—	
$f_O = 100$ kHz	—	22	40	—	22	—	—	22	—	
Input Noise Current, i_n p-p (0.1 to 10 Hz)	—	12	20	—	12	20	—	12	20	pA p-p
Input Noise Current Density, i_n										
$f_O = 10$ Hz	—	0.83	2.30	—	0.83	—	—	0.83	—	
$f_O = 100$ Hz	—	0.80	1.20	—	0.80	—	—	0.80	—	
$f_O = 1000$ Hz	—	0.75	1.00	—	0.75	—	—	0.75	—	pA/$\sqrt{\text{Hz}}$
$f_O = 10$ kHz	—	0.72	0.80	—	0.72	—	—	0.72	—	
$f_O = 100$ kHz	—	0.60	0.80	—	0.60	—	—	0.60	—	

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V+ = 15$ V and $V- = 15$ V (Cont'd) unless otherwise specified.

CHARACTERISTIC	LIMITS									UNITS
	CA3193B			CA3193A			CA3193			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Common-Mode Input Voltage Range, V_{ICR}	−12	−13.5 to 11.5	10	−12	−13.5 to 11.5	10	−12	−13.5 to 11.5	10	V
Common-Mode Rejection Ratio, ($V_{CM} = V_{ICR}$)	120	130	—	110	115	—	100	110	—	dB
		0.316	1		1.78	3.16		3.16	10	μV/V
Power Supply Rejection Ratio, PSRR, $\Delta V_{IO}/\Delta V\pm$	110	130	—	100	130	—	100	130	—	dB
		0.316	3.16		0.316	10		0.316	10	μV/V
Maximum Output Voltage Swing ($R_L \geq 2$ KΩ)	±13.0	±13.5	—	±13.0	±13.5	—	±13.0	±13.5	—	V
Large-Signal Voltage Gain ($V_O = \pm 10$)										
$R_L \geq 1$ KΩ	—	115	—	—	—	—	—	—	—	
$R_L \geq 2$ KΩ	120	125	—	110	115	—	100	110	—	dB
$R_L \geq 10$ KΩ	—	130	—	—	125	—	—	115	—	
Short-Circuit Output Current to the Opposite Rail, $I_{OM}+$, $I_{OM}-$	−25	±7	25	−25	±7	25	−25	±7	25	mA
Slew Rate, SR ($R_L \geq 2$ KΩ; Unity Gain Voltage Follower)	—	0.25	—	—	0.25	—	—	0.25	—	V/μs
Gain-Bandwidth Product, f_t $A_{OL} = 0$ dB $R_L = 2$ kΩ $C_L = 100$ pF $V_{IN} = 20$ f = 1 kHz	—	1.20	—	—	1.20	—	—	1.20	—	MHz
Small-Signal Transient Response, t_r (V_{IN} = 20 mV p-p, f = 1 kHz	—	0.29	—	—	0.29	—	—	0.29	—	μs
Supply Current, $R_L = \infty$ $V+ = 15$, $V- = -15$	—	2.3	3.5	—	2.3	3.5	—	2.3	3.5	mA
Temperature Range	−55	—	125	−25	—	85	0	—	70	°C

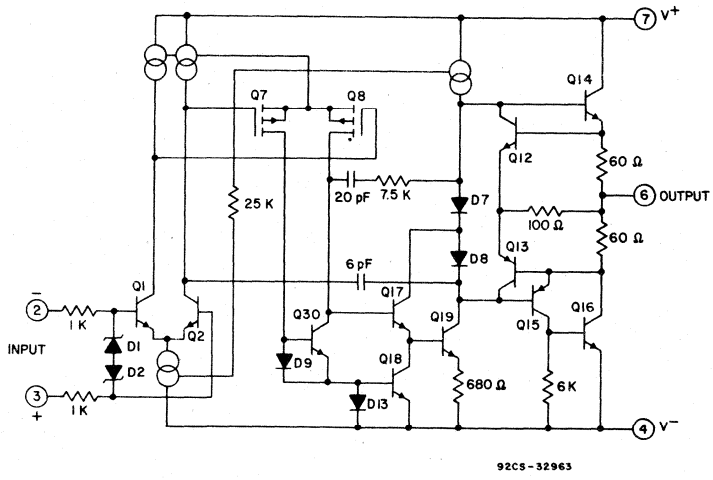


Fig. 3 — CA3193 simplified schematic diagram.

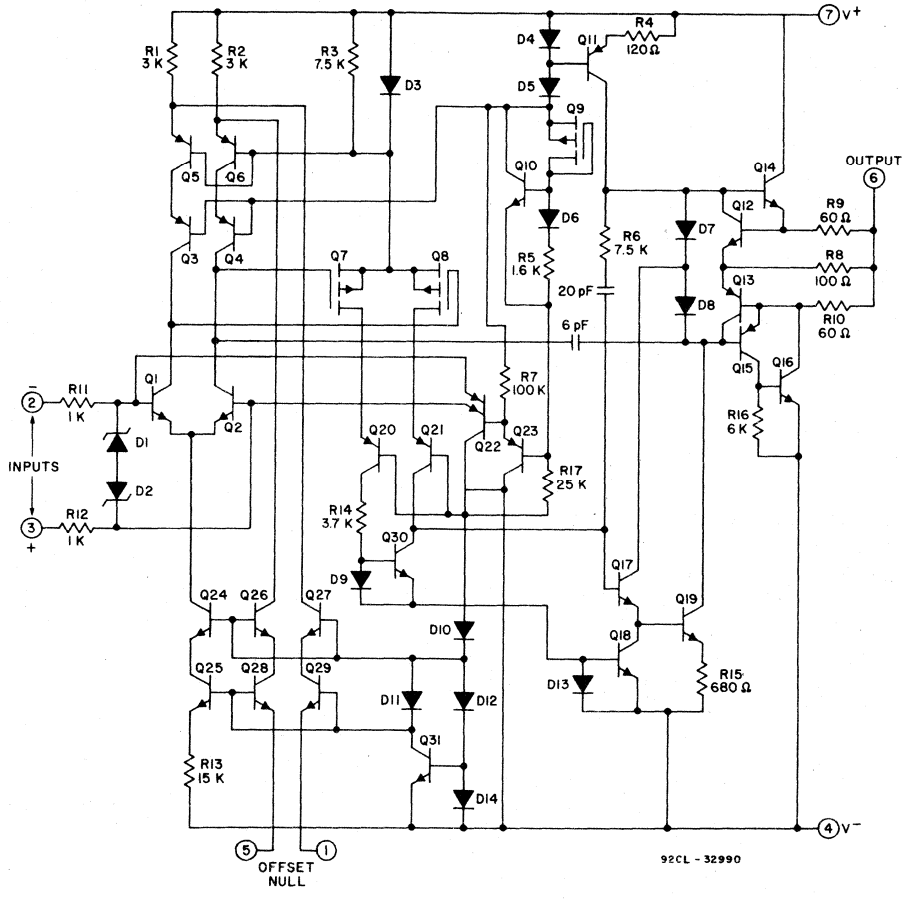


Fig. 4 — Schematic diagram of CA3193 series.

Circuit Description (cont'd)

appropriate drain loading. Since Q7 and Q8 are MOS/FETs, their loading on the first stage is quite low, thereby making an additional contribution to the high gain developed in the first stage. The second stage is also configured to convert its differential signal to a single-ended output signal by means of current mirror D9,Q30 (Figs. 3 and 4) to drive subsequent gain stage.

The third stage of the amplifier consists of Darlington-connected n-p-n transistors (Q17,Q19 in Figs. 3 and 4), driving the quasi-complementary Class AB output stage (Q14 and Q15,Q16 in Figs. 3 and 4). Output-stage short-circuit protection is activated by voltage drops developed across the 60-ohm resistors adjacent to the output terminal (R9 and R10, Fig. 4). When the voltage drop developed across either of these resistors reaches a potential equal to 1 V_{be}, the respective protective transistor (Q12 or Q13) is activated and shunts the base drive from the bases of the output stage transistors (Q14 and Q15,Q16).

Internal frequency compensation for the CA3193 amplifier is provided by two internal networks, a 6-pF capacitor connected between the input-stage transistor collectors and the node between the third and output stages and a second network, consisting of a 20-pF capacitor in series with a 7.5-KΩ resistor connected between the input and output nodes of the third stage.

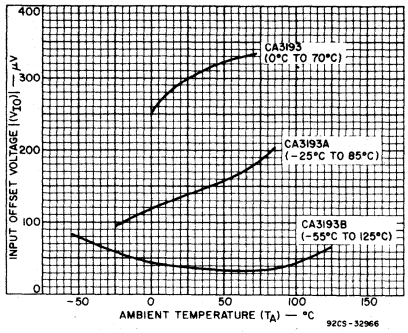


Fig. 5 — Typical input offset-voltage temperature characteristic for CA3193 series.

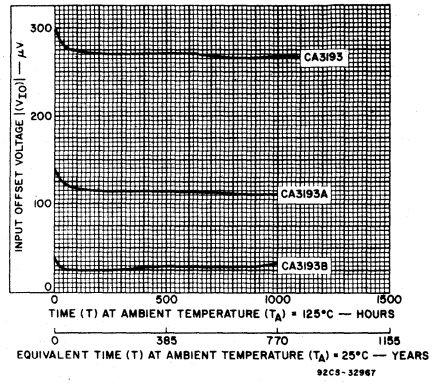


Fig. 6 — Input offset voltage vs. time.

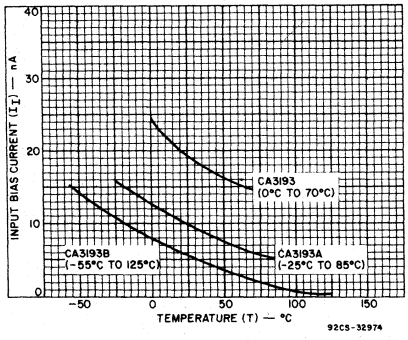


Fig. 7 — Typical input bias current vs. temperature

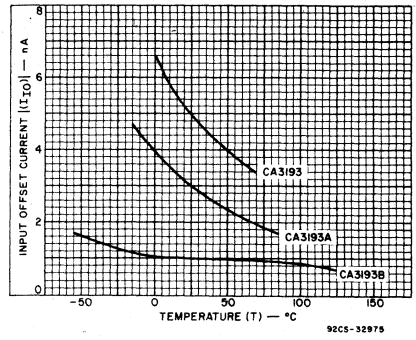


Fig. 8 — Typical input offset current vs. temperature.

CA3193, CA3193A, CA3193B Types

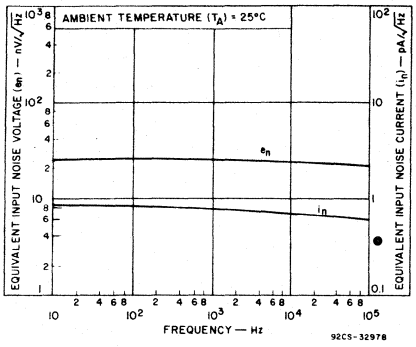


Fig. 9 — Input noise voltage and current density vs. frequency.

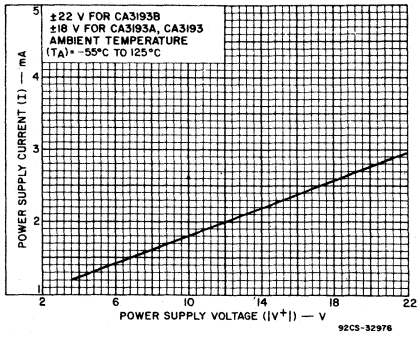


Fig. 10 — Power supply voltage (V+, V−) vs. supply current.

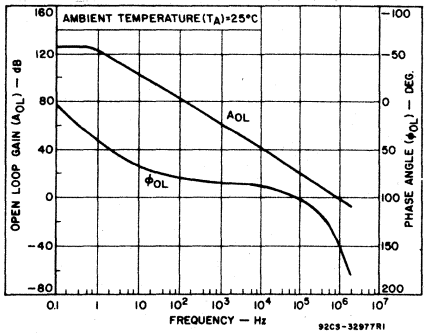


Fig. 11 — Open-loop gain and phase-shift response for CA3193B.

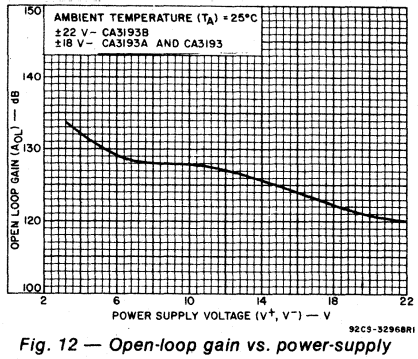


Fig. 12 — Open-loop gain vs. power-supply voltage.

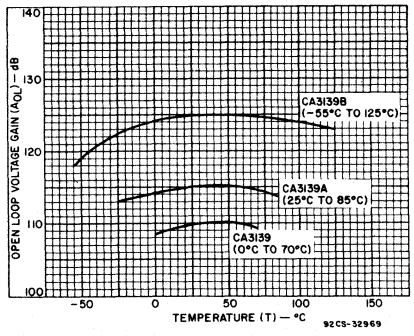
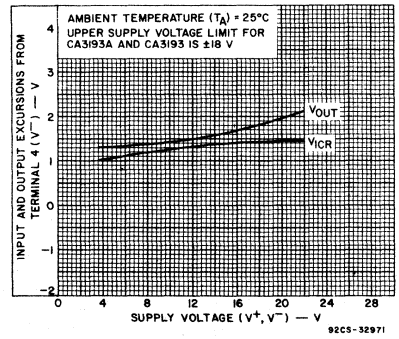


Fig. 13 — Open-loop gain vs. temperature for CA3193 series.



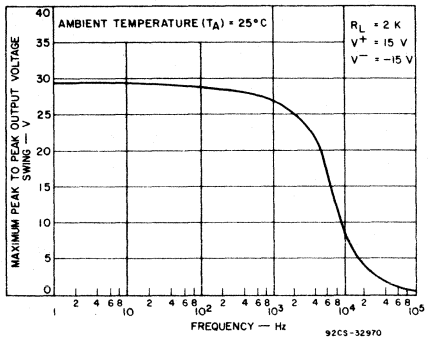


Fig. 14 — Maximum undistorted output voltage vs. frequency.

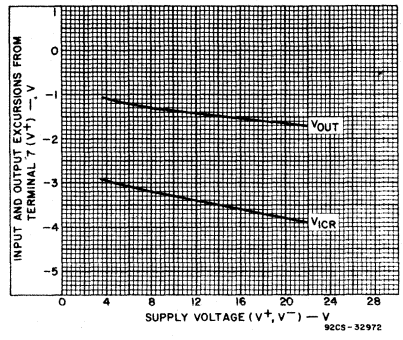


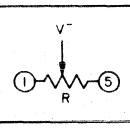
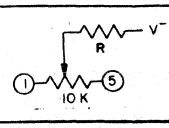
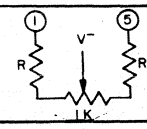
Fig. 15 — Output-voltage-swing capability and common-mode input-voltage vs. supply voltage.

Offset Voltage Nulling

The input offset voltage can be nulled to zero by any of the three methods shown in the table below. A 10K potentiometer between terminals 1 and 5, with its wiper returned to V⁻, will provide a gross nulling for all types. For finer nulling, either of the other two circuits shown below may be used, thus providing simpler improved resolution for all types.

CAUTION: The CA3193 amplifiers will be damaged if they are plugged into op-amp circuits employing nulling with respect to the V+ supply bus.

Offset Voltage Nulling

Offset Nulling Circuits			
Type	**Resistor R Value**	**Resistor R Value**	**Resistor R Value**
CA3193B CA3193A CA3193	10K 10K 10K	100K 50K 20K	20K 10K 5K
	Gross Offset Adjustment	Finer Offset Adjustments	

Test Circuits

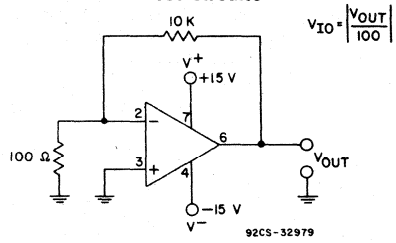
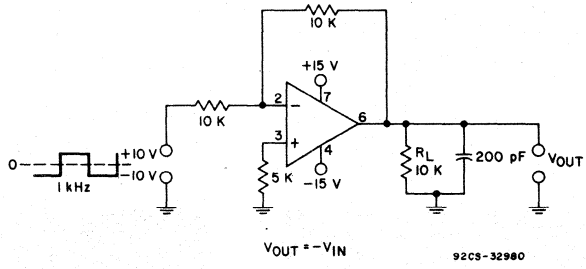
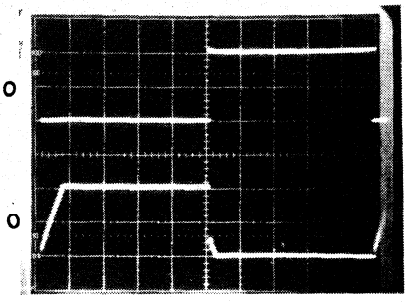


Fig. 16 - Input offset voltage test circuit.



a



TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT.: $\frac{10\,V}{DIV}$ $V^+ = 15\,V$ $V^- = -15\,V$

HOR.: $\frac{.1\,ms}{DIV}$ $R_L = 10\,K$

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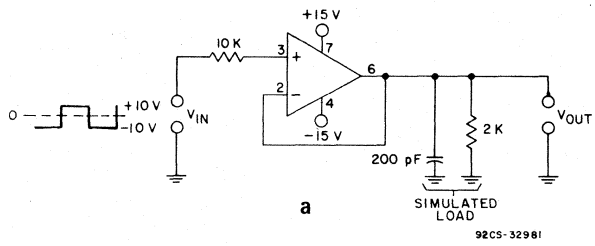
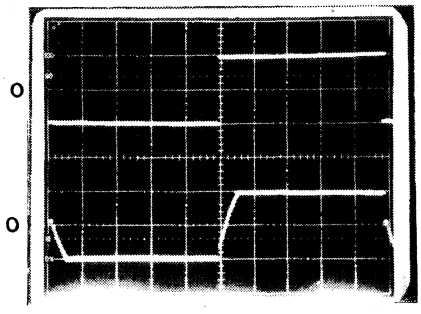
b

Fig. 17 - Inverting amplifier (a) test circuit (b) response to 1-kHz, 20-V p-p square wave.





TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT: 10 V / DIV

HOR : .1 ms / DIV

V+ = 15 V

V⁻ = 15 V

R_L = 2K

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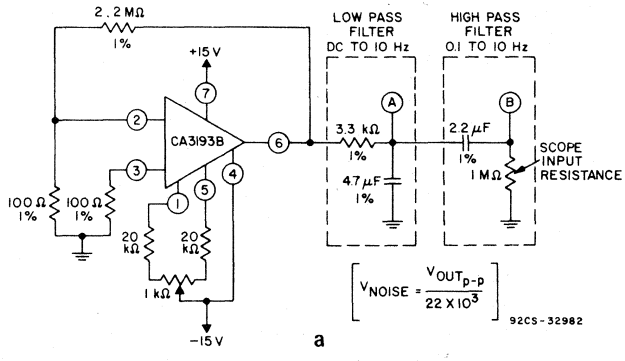
Fig. 18 - Voltage follower (a) test circuit (b) response to 20-V p-p, 1-kHz square-wave input.



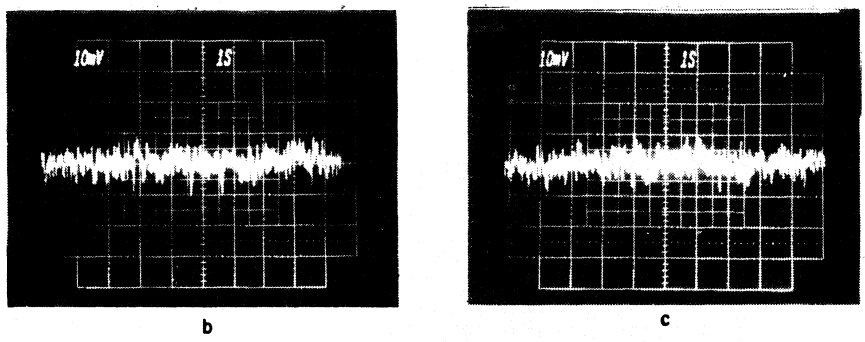
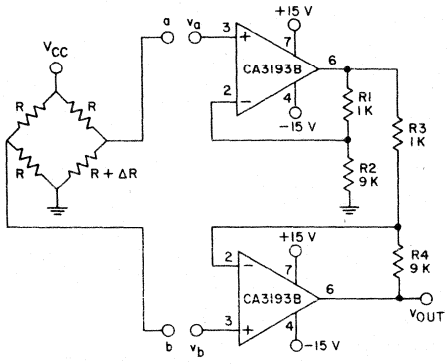


Fig. 19 - Low frequency noise (a) test circuit—0.1 to 10 Hz (b) output A waveform—0 to 10 Hz noise (c) output B waveform—0 to 10 Hz noise.

Application Circuits



$$V_{OUT} = -V_a\left(\frac{R2}{R1}+1\right)\frac{R4}{R3} + V_b\left(\frac{R4}{R3}+1\right)$$

FOR IDEAL RESISTORS WITH $\frac{R1}{R2} = \frac{R3}{R4}$

$$V_{OUT} = V_b - V_a\left(\frac{R4}{R3}+1\right)$$

$$A = \frac{V_{OUT}}{V_b - V_a} = \left(\frac{R4}{R3}+1\right)$$

FOR VALUES ABOVE $V_{OUT} = (V_b - V_a)(10)$

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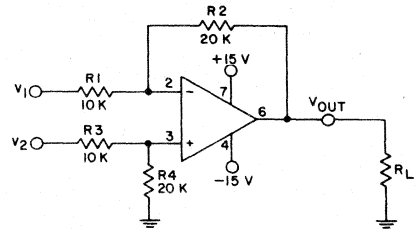
Fig. 20 - Typical two-op amp bridge-type differential amplifier.



$$V_{OUT} = V_2\left(\frac{R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right) - V_1\left(\frac{R2}{R1}\right)$$

IF R4 = R2, R3 = R1 AND $\frac{R2}{R1} = \frac{R4}{R3}$

THEN $V_{OUT} = (V_2 - V_1)\left(\frac{R2}{R1}\right)$

FOR VALUES ABOVE $V_{OUT} = 2(V_2 - V_1)$

IF A_V IS TO BE MADE 1 AND IF R1 = R3 = R4 = R WITH R2 = 0.999 R (0.1% MISMATCH IN R2)

THEN $V_{OCM} = 0.0005\ V_{IN}$ OR CMRR = 66 dB
THUS, THE CMRR OF THIS CIRCUIT IS LIMITED BY THE MATCHING OR MISMATCHING OF THIS NETWORK RATHER THAN THE AMPLIFIER.

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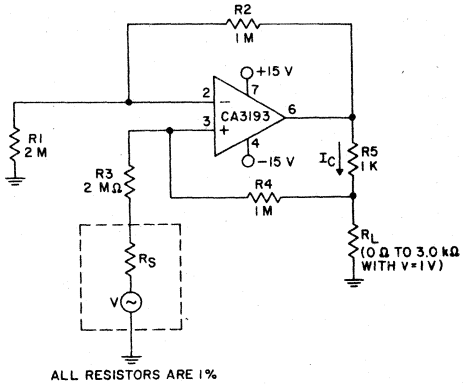
Fig. 21 - Differential amplifier (simple subtractor) using CA3193B.



ALL RESISTORS ARE 1%

IF R1 = R3 AND R2 ≈ R4 + R5 THEN

I_L IS INDEPENDENT OF VARIATIONS IN R_L FOR R_L VALUES OF 0 Ω TO 3 kΩ WITH V = 1 V

$$I_L = \frac{V}{R3\,R5} = \frac{V}{(2\,M)(1K)} = \frac{V}{2\,K} = 500\ \mu A$$

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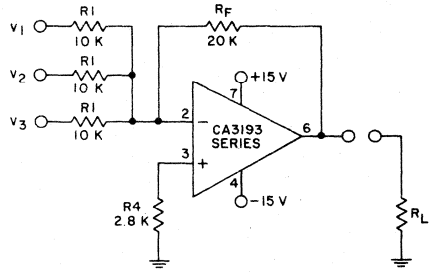
Fig. 22 - Using CA3193B as a bilateral current source.



$$V_{OUT} = -\left(\frac{R_F}{R1}V_1 + \frac{R_F}{R1}V_2 + \frac{R_F}{R1}V_3\right)$$

$$V_{OUT} = -(2V_1 + 2V_2 + 2V_3)$$

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Fig. 23 - Typical summing amplifier application.

CA3193, CA3193A, CA3193B Types

The CA3193B is an excellent choice for use with thermocouples. In Fig. 24, the CA3193B amplifies the signal generated 500 times. The three 22-megohm resistors will provide full-scale output if the thermocouple opens.

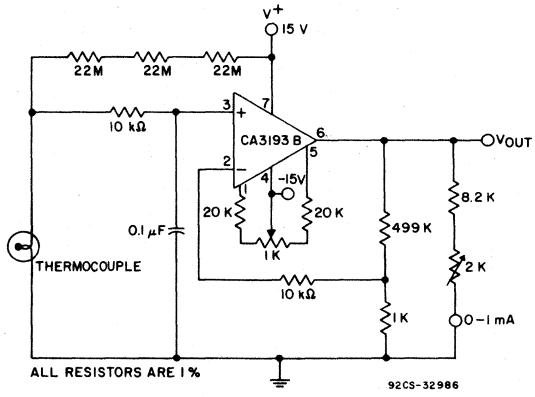
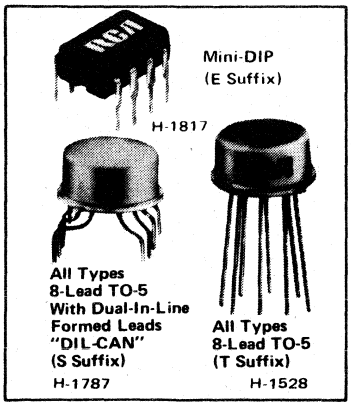


Fig. 24 - The CA3193B used in a thermocouple circuit.



Low-Supply Voltage, Low-Input Current BiMOS OP-AMPS

Features:

- *2 V Supply at 300 μA Supply Current*
- *1 pA (typ) Input Current (Essentially Constant to 85° C)*
- *Rail-to-Rail Output Swing (Drive ±2 mA into 1 KΩ Load)*
- *Pin Compatible with 741 Op-Amp*
- *Low Cost 8-Lead Minidip, TO-5*

Applications:

- *pH Probe Amplifiers*
- *Picoammeters*
- *Electrometer (High Z) instruments*
- *Portable Equipment*
- *Inaccessible Field Equipment*
- *Battery Dependent Equipment (Medical and Military)*

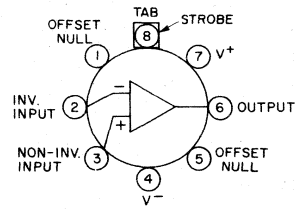
The RCA-CA3420B, CA3420A, and CA3420• are integrated-circuit operational amplifiers that combine PMOS transistors and BiPolar transistors on a single monolithic chip. The CA3420B, CA3420A, and CA3420 BIMOS operational amplifiers feature gate-protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 1 pA). The internal bootstrapping network features a unique guard-banding technique for reducing the doubling of leakage current for every 10° C increase in temperature. The CA3420 series operates at total supply voltages from 2 to 20 volts either single or dual supply. These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Additionally, they have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.45 volt below the negative supply terminal, an important attribute for single-supply application. The output stage uses a feedback OTA type amplifier that can swing essentially from rail-to-rail. The output driving current of 1.5 mA MIN is provided by using non-linear current mirrors.

The CA3420-series has the same 8-lead pin-out used for the industry standard 741. They are supplied in the standard 8-lead TO-5 style package (S suffix, and T suffix); in the standard 8-lead dual-in-line plastic package (Minidip - E suffix), and are also available in chip form (H suffix).

• **Formerly Dev. Type No. TA10841**

TERMINAL ASSIGNMENTS

TOP VIEW

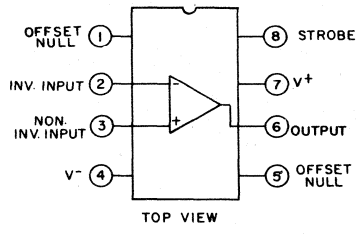


NOTE: PIN 4 IS CONNECTED TO CASE

92CS-33997

S AND T SUFFIXES

TOP VIEW



TOP VIEW

92CS-29086

E SUFFIX

CA3420, CA3420A, CA3420B

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25° C):

DC Supply Voltage
(Between V^+ and V^- Terminals) ..... 22 V
Differntial-Mode
Input Voltage ..... ±15 V
Common-Mode DC
Input Voltage ..... (V^+ + 8 V) to (V^- -0.5 V)
Input-Terminal Current ..... 1 mA
Device Dissipation:
Without Heat Sink —
Up to 55° C ..... 630 mW
Above 55° C ..... Derate linearly 6.67 mW/° C
With Heat Sink -
Up to 110° C ..... 630 mW
Above 110° C ..... Derate linearly 16.7 mW° C

Temperature Range:
Operating (All Types) ..... -55 to +125° C
Storage (All Types) ..... -65 to +150° C
Output Short-Circuit
Duration* ..... Indefinite
Lead Temperature
(During Soldering):
At Distance 1/16 ± 1/32 Inch
(1.59 ± 0.79 mm) from case
For 10 seconds max. ..... +265° C

*Short circuit may be applied to ground or to either supply.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

Characteristic		Test Conditions V+ = +10V; V- = -10V TA = 25° C		CA3420B (T,S)	CA3420A (T,S,E)	CA3420 (T,S,E)	Units
Input Resistance	R_I			150	150	150	TΩ
Input Capacitance	C_I			4.9	4.9	4.9	pF
Output Resistance	R_O			300	300	300	Ω
Equivalent Input Noise Voltage	e_n	f = 1 KHz	R_S 100 Ω	62	62	62	nV/ Hz
		f = 10 KHz		38	38	38	
Short-Circuit Current Source Source IOM+				2.6	2.6	2.6	mA
To Opposite Supply Sink IOM-				2.4	2.4	2.4	mA
Gain-Bandwidth Product	f_T			0.5	0.5	0.5	MHz
Slew Rate	SR			0.5	0.5	0.5	V/μs
Transient Response Rise Time tr		R_L = 2 K Ω		0.7	0.7	0.7	μs
Overshoot		C_L = 100 pF		15	15	15	%
Current from Terminal 8 To V-	I_{8+}			20	20	20	μA
Current from Terminal 8 To V+	I_{8-}			2	2	2	mA

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V+ = 1V, V- = -1V, TA = 25°C unless otherwise specified

Characteristic	Limits									Units
	CA3420B			CA3420A			CA3420			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $\|V_{IO}\|$	—	0.8	2	—	2	5	—	5	10	mV
Input Offset Current $\|I_{IO}\|$ *	—	0.01	4.0	—	0.01	4	—	0.01	4	pA
Input Current $\|I_I\|$ *	—	0.02	5	—	0.02	5	—	1	5	pA
Large-Signal Voltage Gain	20K	100K	—	20K	100K	—	10K	100K	—	V/V
AOL (R_L = 10 KΩ)	86	100	—	86	100	—	80	100	—	dB
Common-Mode	—	320	560	—	560	1000		560	1800	μV/V
Rejection Ratio CMRR	65	70	—	60	65	—	55	65	—	dB
Common-Mode Input VICR +	+0.2	+0.5	—	+0.2	+0.5	—	+0.2	+0.5	—	V
Voltage Range VICR -	-1	-1.3	—	-1	-1.3	—		-1.3	—	V
Power Supply Rejection	—	20	180	—	32	320	—	100	1000	μV/V
Ratio PSRR ΔVIO/ΔV	75	94	—	70	90	—	60	80	—	dB
Max Output Voltage VOM +	+0.90	+0.95	—	+0.90	+0.95	—	+0.90	+0.95	—	V
RL = 00 VOM -	-0.85	-0.91	—	-0.85	-0.91	—	-0.85	-0.91	—	V
Supply Current I+	—	350	650	—	350	650	—	350	650	μA
Device Dissipation P_D	—	0.7	1.1	—	0.7	1.1	—	0.7	1.1	mW
Input Offset Voltage Temp. Drift ΔVIO/ΔT	—	4	—	—	4	—	—	4	—	μV/°C

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V+ = 10V, V- = -10V, TA = 25°C unless otherwise specified

Characteristic	Limits									Units
	CA3420B			CA3420A			CA3420			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $\|V_{IO}\|$	—	0.8	2	—	2	5	—	5	10	mV
Input Offset Current $\|I_{IO}\|$ *	—	0.03	4	—	0.03	4	—	0.03	4	pA
Input Current $\|I_I\|$ *	—	0.05	5	—	0.05	5	—	0.05	5	pA
Large-Signal Voltage Gain	20K	100K	—	20K	100K	—	10K	100K	—	V/V
AQL (R_L = 10K Ω)	86	100	—	86	100	—	80	100	—	dB
Common-Mode	—	32	100	—	100	320	—	100	320	μV/V
Rejection Ratio CMRR	80	90	—	70	80	—	70	80	—	dB
Common-Mode Input VICR +	+9.0	+9.3	—	+9.0	+9.3	—	+8.5	+9.3	—	V
Voltage Range VICR -	-10	-10.3	—	-10	-10.3	—	-10	-10.3	—	V
Power Supply Rejection	—	20	180	—	32	320	—	32	320	μV/V
Ratio PSRR ΔVIO/ΔV	75	94	—	70	90	—	70	90	—	dB
Max Output Voltage VOM +	+9.7	+9.9	—	+9.7	+9.9	—	+9.7	+9.9	—	V
RL = 00 VOM -	-9.7	-9.85	—	-9.7	-9.85	—	-9.7	-9.85	—	V
Supply Current I+	—	450	1000	—	450	1000	—	450	1000	μA
Device Dissipation P_D	—	9	14	—	9	14	—	9	14	mW
Input Offset Voltage Temp. Drift ΔVIO/ΔT	—	4	—	—	4	—	—	4	—	μV/°C

* The maximum limit represents the levels obtainable on high speed automatic test equipment. Typical values are obtained under laboratory conditions.

CA3420, CA3420A, CA3420B

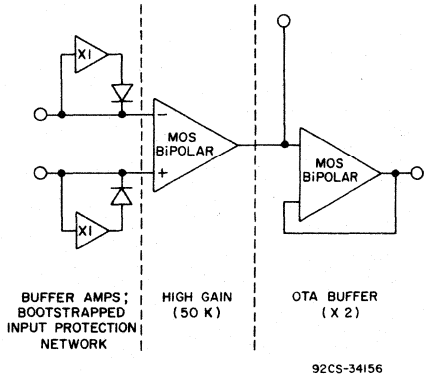


Fig. 1 - Functional diagram for CA3420.

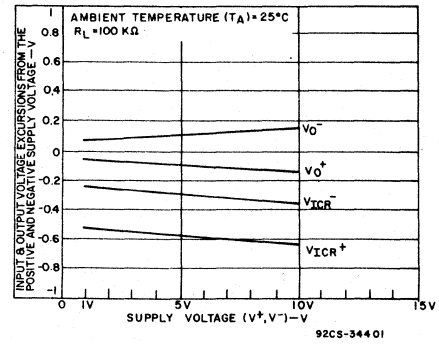


Fig. 2 - Output-voltage-swing and common-mode input-voltage range versus supply voltage.

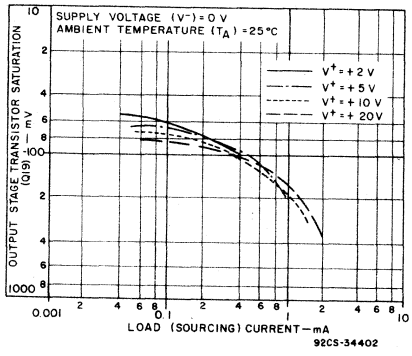


Fig. 3 - Output voltage versus load sourcing current.

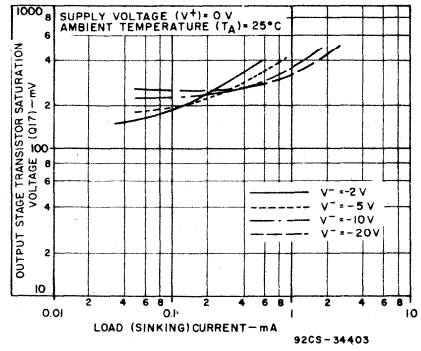


Fig. 4 - Output voltage versus load sinking current.

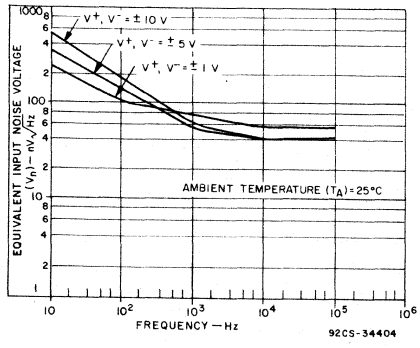


Fig. 5 - Input noise voltage versus frequency.

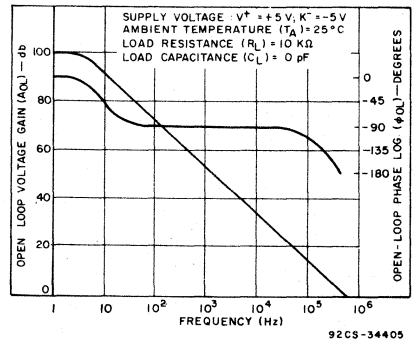


Fig. 6 - Open-loop gain and phase-shift response.

Application Circuits

Picoameter Circuit

The exceptionally low input current (typically 0.2 pA) makes the CA3420 highly suited for use in a picoameter circuit. With only a single 10K megohm resistor, this circuit covers the range from ±1.5 pA. Higher current ranges are possible with suitable switching techniques and current scaling resistors. Input transient protection is provided by the 1-megohm resistor in series with the input. Higher current ranges require that this resistor be reduced. The 10-megohm resistor connected to pin 2 of the CA3420 decouples the potentially high input capacitance often associated with lower current circuits and reduces the tendency for the circuit to oscillate under these conditions.

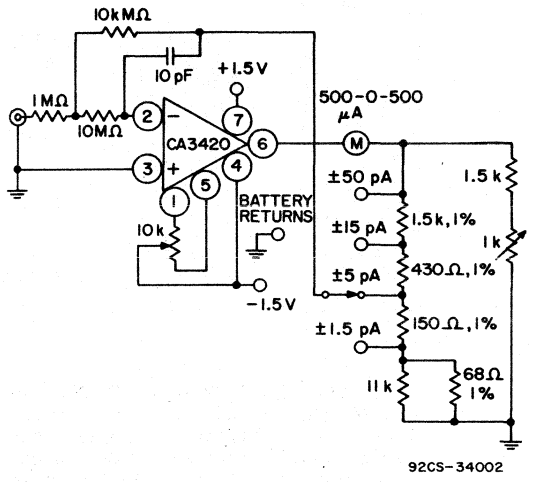


Fig. 7 - Picoameter circuit.

High-Input-Resistance Voltmeter

Advantage is taken of the high input impedance of the CA3420 in a high-input-resistance dc voltmeter. Only two 1.5 V "AA" type penlite batteries power this exceedingly high-input resistance (>1,000,000-megohms) dc voltmeter. Full-scale deflection is ±500 mV, ±150 mV, and ±15 mV. Higher voltage ranges are easily added with external input voltage attenuator networks.

The meter is placed in series with the gain network, thus eliminating the meter temperature coefficient error term.

Supply current in the standby position with the meter undeflected is 300 μA. At full-scale deflection this current rises to 800 μA. Carbon-zinc battery life should be in excess of 1,000 hours.

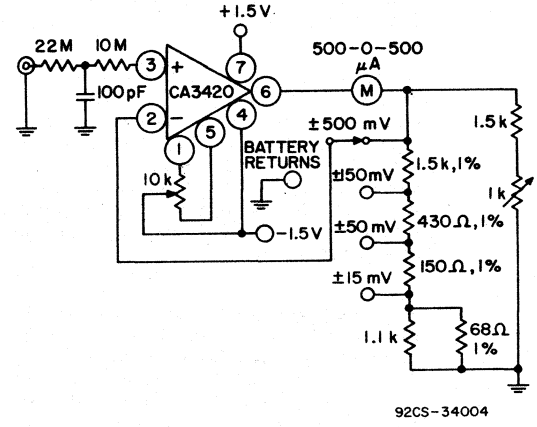
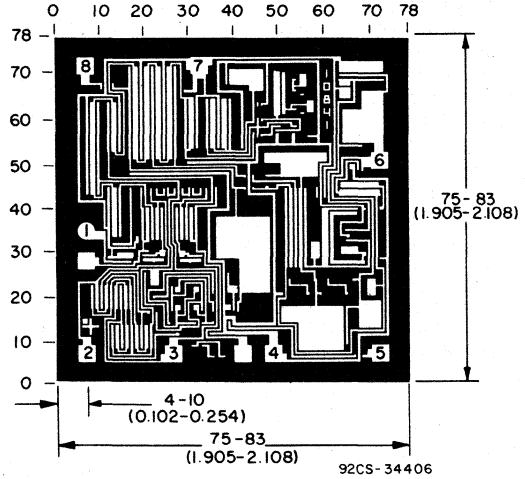


Fig. 8 - High input resistance voltmeter.

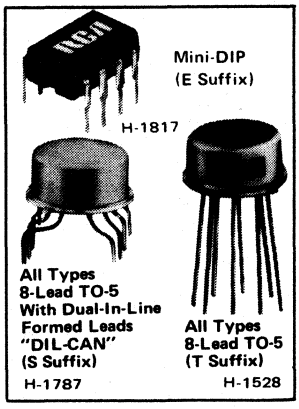


The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CA3420H.

CA3493, CA3493A, CA3493B



BiMOS Precision Operational Amplifier

Features

- *Low V_{IO}: 75 μV max. (CA3493B)*
  200 μV max. (CA3493A)
  500 μV max. (CA3493)
- *Low $\Delta V_{IO}/\Delta T$: 2 μV/°C max. (CA3493B)*
  3 μV/°C max. (CA3493A)
  5 μV/°C max. (CA3493)
- *Low I_{IO} and I_I*
- *Low $\Delta I_{IO}/\Delta T$: 50 pA/°C max. (CA3493B)*
  150 pA/°C max. (CA3493)
- *Low $\Delta I_I/\Delta T$: 0.5 nA/°C max. (CA3493B)*
  3.7 nA/°C max. (CA3493)
- *Extremely high gain:*
  120 dB min. (CA3493B)
  110 dB min. (CA3493A)
  100 dB min. (CA3493)
- *Low V_{IO} vs. time*
- *High CMRR and PSRR*
- *Internally compensated: 1.2-MHz gain-bandwidth product*
- *Low input noise: 0.1 Hz to 10 Hz*
  Noise voltage: 0.36 μV_{p-p} typ.
  Noise current: 12 pA_{p-p} typ.

Applications

- *Thermocouple preamplifiers*
- *Strain-gauge bridge amplifiers*
- *Summing amplifiers*
- *Differential amplifiers*
- *Bilateral current sources*
- *Log amplifiers*
- *Differential voltmeters*
- *Precision voltage references*
- *Active filters*
- *Buffers*
- *Integrators*
- *Sample-and-hold circuits*
- *Low frequency filters*

The CA3493B, CA3493A and CA3493 are ultra-stable, precision-instrumentation, operational amplifiers that employ both PMOS and bipolar transistors on a single monolithic chip. The CA3493-series amplifiers are internally phase-compensated and provide a gain-bandwidth product of 1.2 MHz. They are pin-compatible with many industrial types such as 725, 108A, OP-5, OP-7, LM11 and LM714 where positive nulling is employed.

Because of their low offset voltage and low offset voltage-versus-temperature coefficient, the CA3493-series amplifiers have a wider range of applications than most op amps and are particularly well suited for use as thermocouple amplifiers, high-gain filters, buffers, strain-gauge bridge amplifiers and precision voltage references.

The three types in the CA3493 series are functionally identical. The CA3493B, however, operates from supply voltages of ±3.5 V to ±22 V and has an operating temperature range of −55 °C to +125 °C. The CA3493 and CA3493A operate from supply voltages of ±3.5 V to ±18 V and have operating temperature ranges of −25 °C to +85 °C and 0 °C to +70 °C, respectively.

The CA3493-series types are supplied in standard 8-lead TO-5-style (T suffix), 8-lead dual-in-line formed lead TO-5-style (DIL-CAN—S suffix) and 8-lead dual-in-line plastic (Mini-DIP—E suffix) packages.

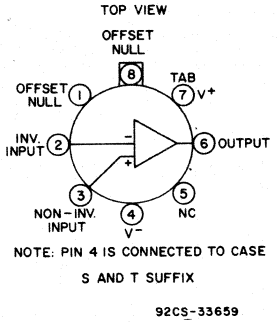
Circuit Description

The block diagram of the CA3493 amplifier, Fig. 2, shows the voltage gain and supply current for each of its four amplifier stages. Simplified and complete schematic diagrams of the CA3493 amplifier are shown in Figs. 3 and 4, respectively.

Absolute-Maximum Ratings, *Absolute-Maximum Values at $T_A = 25°C$*

	CA3493B	CA3493A	CA3493	
DC Supply Voltage	±22	±18	±18	V
Differential-Mode Input Voltage	±5	±5	±5	V
Common-Mode DC Input Voltage	(V+ −4), V−	(V+ −4), V−	(V+ −4), V−	V
Input Terminal Current	1	1	1	mA
Device Dissipation				
Without Heat Sink				
Up to 55°C	630	630	630	mW
Above 55°C		Derate Linearly 6.67		mW/°C
Temperature Range	−55 to 125	−25 to 85	0 to 70	°C
Output Short-Circuit Duration*	Indefinite	Indefinite	Indefinite	
Lead Temperature (During Soldering) at distance of 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	±265	±265	±265	°C

*Short circuit may be applied to ground or to either supply.



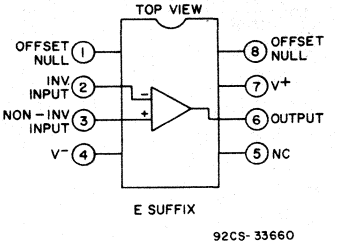


Fig. 1 - Functional diagram of CA3493 series.

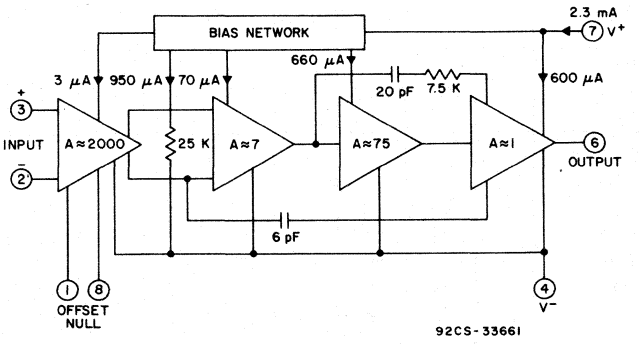


Fig. 2 - Block diagram of CA3493 series.

Circuit Description (cont'd)

A quad of physically cross-connected n-p-n transistors comprise the input-stage differential pair (Q1,Q2 in Figs. 3 and 4); this arrangement contributes to the low input offset-voltage characteristics of the amplifier. The ultra-high gain provided in the first stage ensures that subsequent stages cannot significantly influence the overall offset-voltage characteristics of the amplifier. High load impedances for the input-stage differential pair (Q1,Q2) are provided by the cascode-connected p-n-p transistors Q3,Q5 and Q4,Q6, thereby contributing to the high gain developed in the stage.

The second stage of the amplifier consists of a differential amplifier employing PMOS/FETs (Q7,Q8 in Figs. 3 and 4) with

CA3493, CA3493A, CA3493B

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 15$ V and $V^- = 15$ V unless otherwise specified.

CHARACTERISTIC	LIMITS									UNITS
	CA3493B			CA3493A			CA3493			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	40	75	—	140	200	—	300	500	μV
V_{IO} @ Max.Temp.	—	—	275	—	—	380	—	—	725	μV
Input Offset Voltage Temp.Coefficient, $\Delta V_{IO}/\Delta T$ (Over specified temperature range for each device)	—	0.60	2	—	1	3	—	1	5	μV/°C
Input Offset Current, I_{IO}	—	1	3	—	3	5	—	5	10	nA
$\|I_{IO}\|$ @ Max.Temp.	—	—	8	—	—	11	—	—	17	nA
Input Offset Current Temp. Coefficient, $\Delta I_{IO}/\Delta T$ (Over specified temperature range for each device)	—	0.01	0.05	—	0.03	0.10	—	0.04	0.15	nA/°C
Input Bias Current, I_I	—	6	15	—	10	20	—	20	40	nA
$\|I_B\|$ @ Max.Temp.	—	—	60	—	—	83	—	—	207	nA
Input Bias Current Temp. Coefficient, $\Delta I_I/\Delta T$	—	0.08	0.50	—	0.10	1.18	—	0.15	3.70	nA/°C
Input Noise Voltage, $e_{n\ p\text{-}p}$ (0.1 to 10 Hz)	—	0.36	0.60	—	0.36	—	—	0.36	—	μV p-p
Input Noise Voltage Density, e_n										
$f_O = 10$ Hz	—	25	50	—	25	—	—	25	—	
$f_O = 100$ Hz	—	25	45	—	25	—	—	25	—	
$f_O = 1000$ Hz	—	24	45	—	24	—	—	24	—	nV/
$f_O = 10$ kHz	—	24	45	—	24	—	—	24	—	$\sqrt{Hz}$
$f_O = 100$ kHz	—	22	40	—	22	—	—	22	—	
Input Noise Current, $i_{n\ p\text{-}p}$ (0.1 to 10 Hz)	—	12	20	—	12	20	—	12	20	pA p-p
Input Noise Current Density, i_n										
$f_O = 10$ Hz	—	0.83	2.30	—	0.83	—	—	0.83	—	
$f_O = 100$ Hz	—	0.80	1.20	—	0.80	—	—	0.80	—	
$f_O = 1000$ Hz	—	0.75	1.00	—	0.75	—	—	0.75	—	pA/
$f_O = 10$ kHz	—	0.72	0.80	—	0.72	—	—	0.72	—	$\sqrt{Hz}$
$f_O = 100$ kHz	—	0.60	0.80	—	0.60	—	—	0.60	—	

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 15$ V and $V^- = 15$ V (Cont'd) unless otherwise specified.

CHARACTERISTIC	LIMITS									UNITS
	CA3493B			CA3493A			CA3493			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Common-Mode Input Voltage Range, V_{ICR}	−12	−13.5 to 11.5	10	−12	−13.5 to 11.5	10	−12	−13.5 to 11.5	10	V
Common-Mode Rejection Ratio, ($V_{CM} = V_{ICR}$)	120	130	—	110	115	—	100	110	—	dB
		0.316	1		1.78	3.16		3.16	10	μV/V
Power Supply Rejection Ratio, PSRR, $\Delta V_{IO}/\Delta V \pm$	110	130	—	100	130	—	100	130	—	dB
		0.316	3.16		0.316	10		0.316	10	μV/V
Maximum Output Voltage Swing ($R_L \geq 2$ KΩ)	±13.0	±13.5	—	±13.0	±13.5	—	±13.0	±13.5	—	V
Large-Signal Voltage Gain ($V_O = \pm 10$)										
$R_L \geq 1$ KΩ	—	115	—	—	—	—	—	—	—	
$R_L \geq 2$ KΩ	120	125	—	110	115	—	100	110	—	dB
$R_L \geq 10$ KΩ	—	130	—	—	125	—	—	115	—	
Short-Circuit Output Current to the Opposite Rail, I_{OM}^+, I_{OM}^-	−25	±7	25	−25	±7	25	−25	±7	25	mA
Slew Rate, SR ($R_L \geq 2$ KΩ; Unity Gain Voltage Follower)	—	0.25	—	—	0.25	—	—	0.25	—	V/μs
Gain-Bandwidth Product, f_t $A_{OL} = 0$ dB $R_L = 2$ kΩ $C_L = 100$ pF $V_{IN} = 20$ f = 1 kHz	—	1.20	—	—	1.20	—	—	1.20	—	MHz
Small-Signal Transient Response, t_r ($V_{IN} = 20$ mV p-p, f = 1 kHz	—	0.29	—	—	0.29	—	—	0.29	—	μs
Supply Current, $R_L = \infty$ $V^+ = 15$, $V^- = -15$	—	2.3	3.5	—	2.3	3.5	—	2.3	3.5	mA
Temperature Range	−55	—	125	−25	—	85	0	—	70	°C

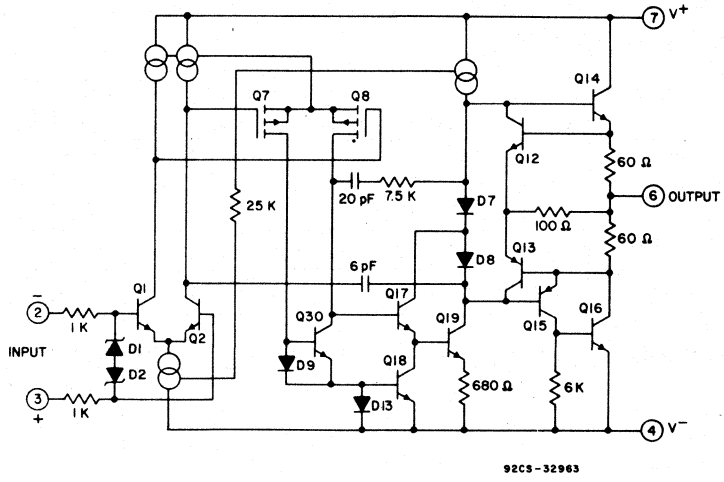


Fig. 3 - CA3493 simplified schematic diagram.

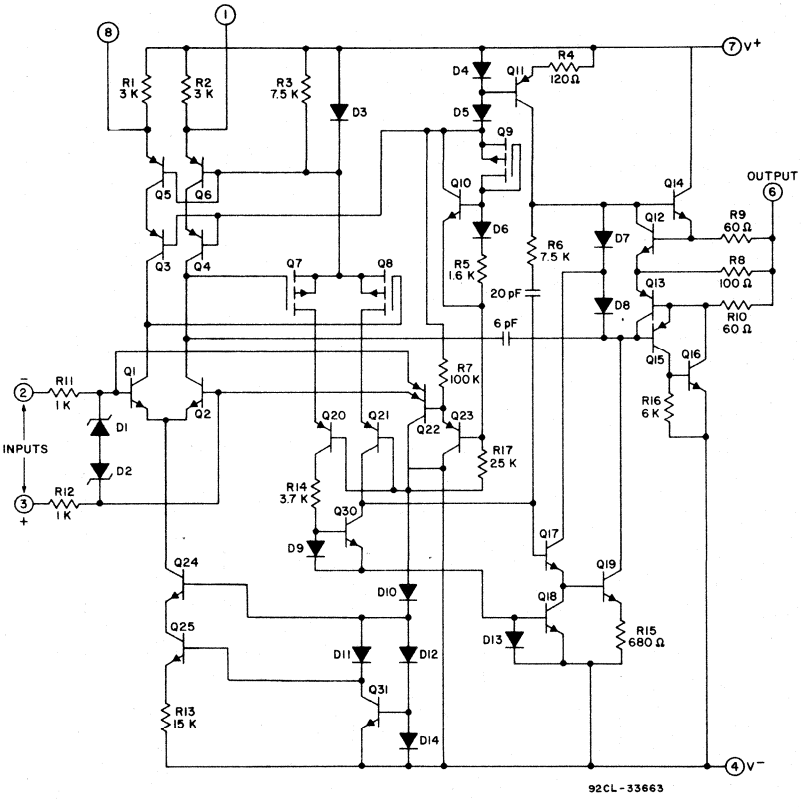


Fig. 4 - Schematic diagram of CA3493 series.

Circuit Description (cont'd)

appropriate drain loading. Since Q7 and Q8 are MOS/FETs, their loading on the first stage is quite low, thereby making an additional contribution to the high gain developed in the first stage. The second stage is also configured to convert its differential signal to a single-ended output signal by means of current mirror D9,Q30 (Figs. 3 and 4) to drive subsequent gain stage.

The third stage of the amplifier consists of Darlington-connected n-p-n transistors (Q17,Q19 in Figs. 3 and 4), driving the quasi-complementary Class AB output stage (Q14 and Q15,Q16 in Figs. 3 and 4). Output-stage short-circuit protection is activated by voltage drops developed across the 60-ohm resistors adjacent to the output terminal (R9 and R10, Fig. 4). When the voltage drop developed across either of these resistors reaches a potential equal to 1 V_{be}, the respective protective transistor (Q12 or Q13) is activated and shunts the base drive from the bases of the output stage transistors (Q14 and Q15,Q16).

Internal frequency compensation for the CA3493 amplifier is provided by two internal networks, a 6-pF capacitor connected between the input-stage transistor collectors and the node between the third and output stages and a second network, consisting of a 20-pF capacitor in series with a 7.5-KΩ resistor connected between the input and output nodes of the third stage.

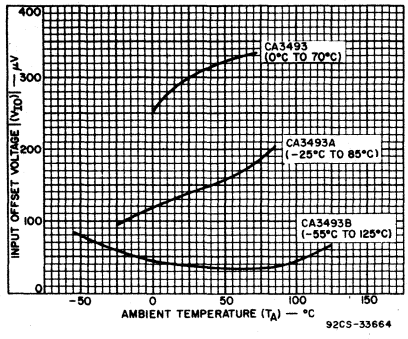


Fig. 5 — Typical input offset-voltage temperature characteristic for CA3493 series.

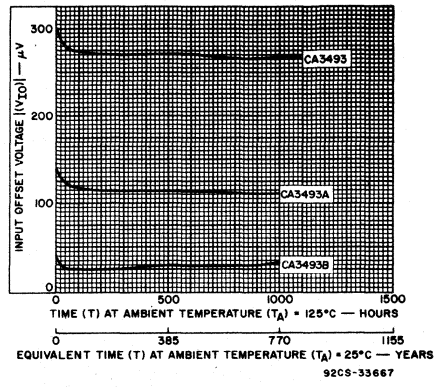


Fig. 6 — Input offset voltage vs. time.

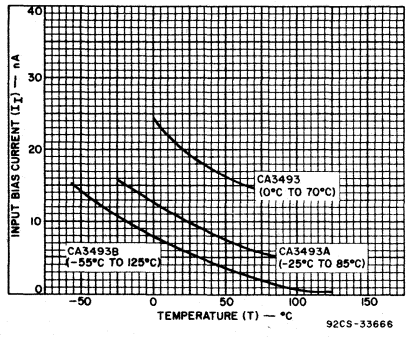


Fig. 7 — Typical input bias current vs. temperature

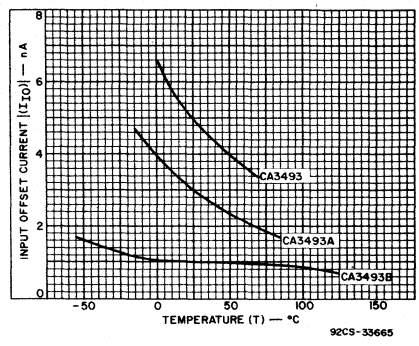


Fig. 8 — Typical input offset current vs. temperature.

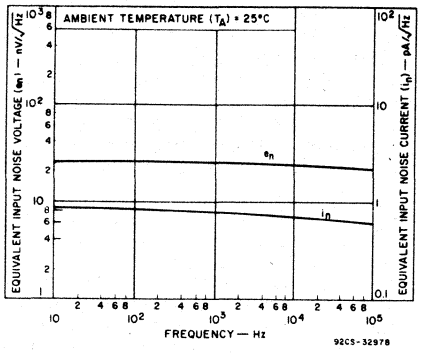


Fig. 9 — Input noise voltage and current density vs. frequency.

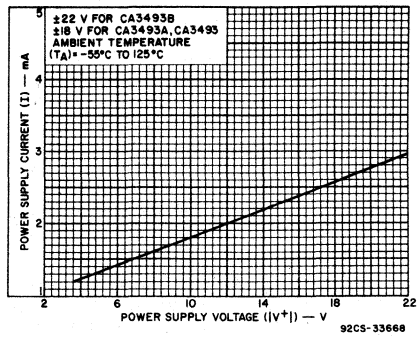


Fig. 10 — Power supply voltage (V+, V−) vs. supply current.

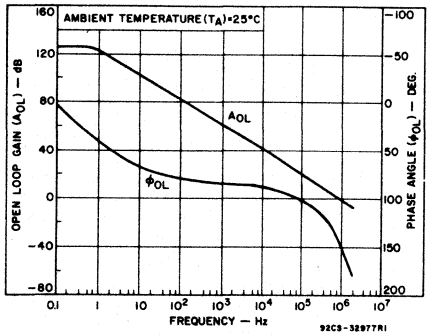


Fig. 11 — Open-loop gain and phase-shift response for CA3493B.

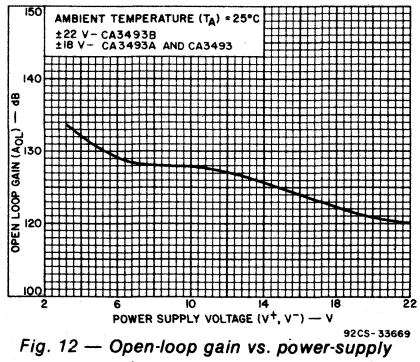


Fig. 12 — Open-loop gain vs. power-supply voltage.

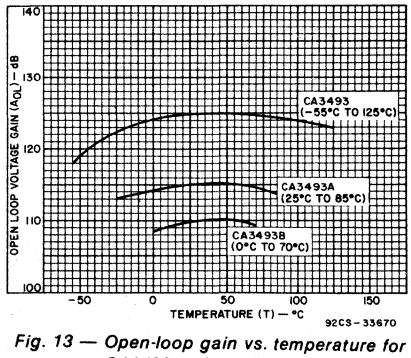


Fig. 13 — Open-loop gain vs. temperature for CA3493 series.

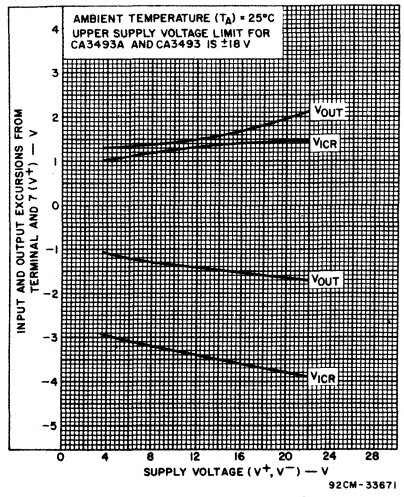


Fig. 15 — Output-voltage-swing capability and common-mode input-voltage vs. supply voltage.

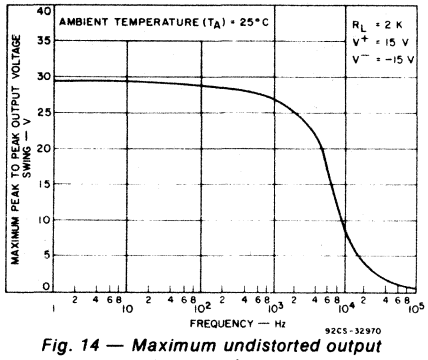


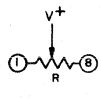
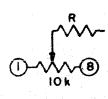
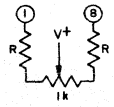
Fig. 14 — Maximum undistorted output voltage vs. frequency.

Offset Voltage Nulling

The input offset voltage can be nulled to zero by any of the three methods shown in the table below. A 10K potentiometer between terminals 1 and 8, with its wiper returned to V^+, will provide a gross nulling for all types. For finer nulling, either of the other two circuits shown below may be used, thus providing simpler improved resolution for all types.

CAUTION: The CA3493 amplifiers will be damaged if they are plugged into op-amp circuits employing nulling with respect to the V^- supply bus.

Offset Voltage Nulling

Offset Nulling Circuits			
Type	**Resistor R Value**	**Resistor R Value**	**Resistor R Value**
CA3493B CA3493A CA3493	10K 10K 10K	100K 50K 20K	20K 10K 5K
	Gross Offset Adjustment	Finer Offset Adjustments	

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Test Circuits

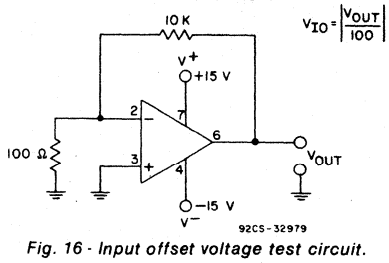
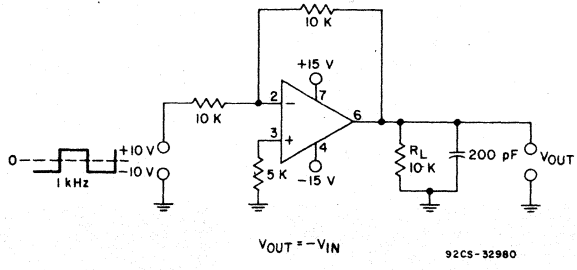
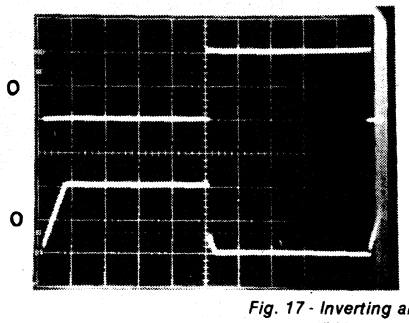


Fig. 16 - Input offset voltage test circuit.



a



TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT. : $\frac{10V}{DIV}$ $V^+ = 15V$ $V^- = -15V$

HOR. : $\frac{.1ms}{DIV}$ $R_L = 10K$

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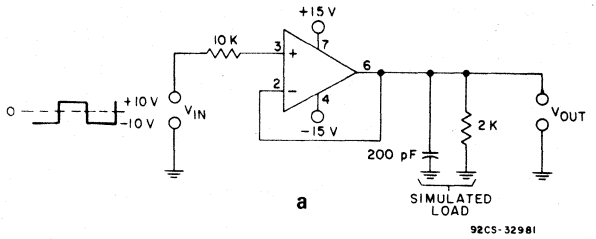
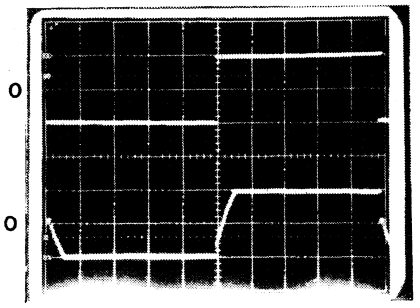
b

Fig. 17 - Inverting amplifier (a) test circuit (b) response to 1-kHz, 20-V p-p square wave.





TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT: $\frac{10\ V}{DIV}$

HOR : $\frac{.1\ ms}{DIV}$

$V^+ = 15\ V$

$V^- = 15\ V$

$R_L = 2K$

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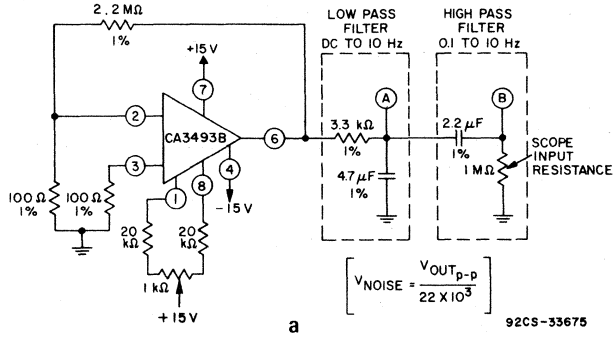
Fig. 18 - Voltage follower (a) test circuit (b) response to 20-V p-p, 1-kHz square-wave input.



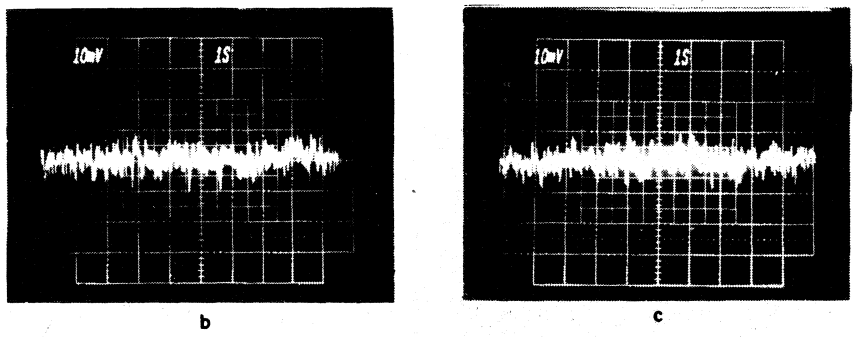
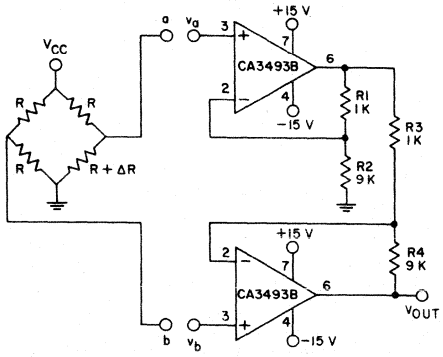


Fig. 19 - Low frequency noise (a) test circuit—0.1 to 10 Hz (b) output A waveform—0 to 10 Hz noise (c) output B waveform—0 to 10 Hz noise.

Application Circuits



$$V_{OUT} = -V_a\left(\frac{R2}{R1}+1\right)\frac{R4}{R3} + V_b\left(\frac{R4}{R3}+1\right)$$

FOR IDEAL RESISTORS WITH $\frac{R1}{R2} = \frac{R3}{R4}$

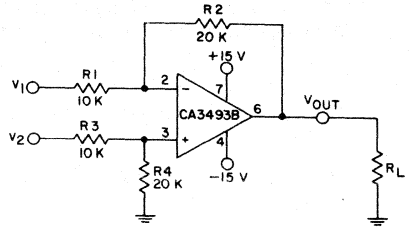
$$V_{OUT} = V_b - V_a\left(\frac{R4}{R3}+1\right)$$

$$A = \frac{V_{OUT}}{V_b - V_a} = \left(\frac{R4}{R3}+1\right)$$

FOR VALUES ABOVE $V_{OUT} = (V_b - V_a)(10)$

92CS-33676

Fig. 20 - Typical two-op amp bridge-type differential amplifier.



$$V_{OUT} = V_2\left(\frac{R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right) - V_1\left(\frac{R2}{R1}\right)$$

IF R4 = R2, R3 = R1 AND $\frac{R2}{R1} = \frac{R4}{R3}$

THEN $V_{OUT} = (V_2 - V_1)\left(\frac{R2}{R1}\right)$

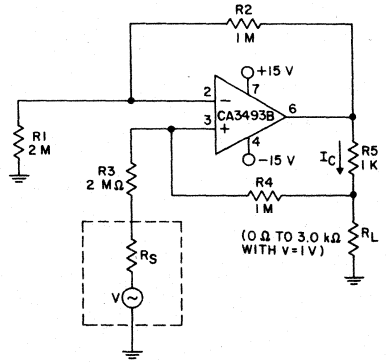
FOR VALUES ABOVE $V_{OUT} = 2(V_2 - V_1)$

IF A_V IS TO BE MADE 1 AND IF R1 = R3 = R4 = R
WITH R2 = 0.999 R (0.1% MISMATCH IN R2)

THEN V_{OCM} = 0.0005 V_{IN} OR CMRR = 66 dB
THUS, THE CMRR OF THIS CIRCUIT IS LIMITED BY THE MATCHING OR MISMATCHING OF THIS NETWORK RATHER THAN THE AMPLIFIER.

92CS-33677

Fig. 21 - Differential amplifier (simple subtractor) using CA3493B.



ALL RESISTORS ARE 1%

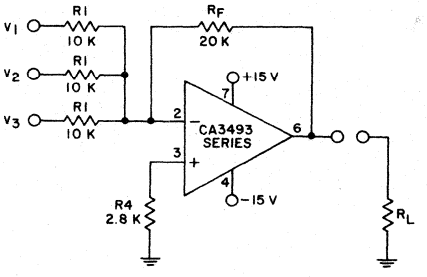
IF R1 = R3 AND R2 ≈ R4 + R5 THEN

I_L IS INDEPENDENT OF VARIATIONS IN R_L
FOR R_L VALUES OF 0 Ω TO 3 kΩ WITH V = 1 V

$$I_L = \frac{V}{R3}\frac{R4}{R5} = \frac{V}{(2\,M)(1K)} = \frac{V}{2\,K} = 500\ \mu A$$

92CS-33678

Fig. 22 - Using CA3493B as a bilateral current source.



$$V_{OUT} = -\left(\frac{R_F}{R1}V_1 + \frac{R_F}{R1}V_2 + \frac{R_F}{R1}V_3\right)$$

$$V_{OUT} = -(2V_1 + 2V_2 + 2V_3)$$

92CS-33679

Fig. 23 - Typical summing amplifier application.

CA3493, CA3493A, CA3493B

The CA3493B is an excellent choice for use with thermocouples. In Fig. 24, the CA3493B amplifies the signal generated 500 times. The three 22-megohm resistors will provide full-scale output if the thermocouple opens.

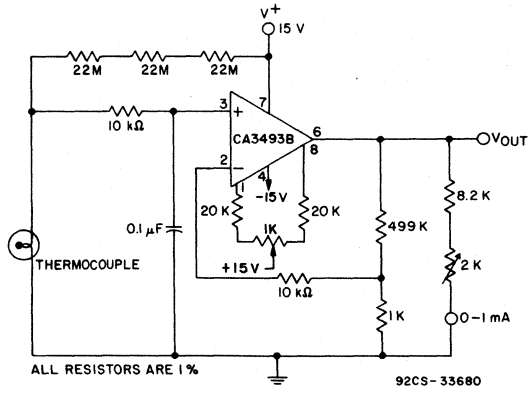
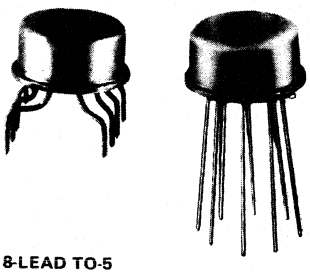


Fig. 24 - The CA3493B used in a thermocouple circuit.



8-LEAD TO-5 with Dual-In-Line Formed Leads H-1787

8-LEAD TO-5 H-1528

Operational Amplifiers

CA6078AT – Micropower Type
CA6741T – General-Purpose Type

For Applications where Low Noise (Burst + 1/f) is a Prime Requirement

Virtually free from "popcorn" (burst) noise: device rejected if any noise burst exceeds 20 μV (peak), referred to input over a 30-second time period.

RCA CA6078AT and CA6741T* are low-noise linear IC operational amplifiers that are virtually free of "popcorn" (burst) noise.

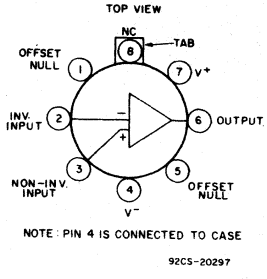
These low-noise versions of the CA3078AT and CA3741T are a result of improved processing developments and rigid burst-noise inspection criteria. A highly selective test circuit (See Fig. 2) assures that each type meets the rigid low-noise standards shown in the data section. This low-burst-noise property also assures excellent performance throughout the 1/f noise spectrum.

In addition the CA6078AT and CA6741T offer the same features incorporated in the CA3078AT and CA3741T respectively, including output short-circuit protection, latch-free operation, wide common-mode and differential-mode signal ranges, and low-offset nulling capability.

For detailed data, characteristics curves, schematic diagram, dimensional outline, and test circuits, refer to the Operational Amplifier Data Bulletins File No. 531 and 535. In addition, for details of considerations in burst-noise measurements, refer to Application Note, ICAN-6732, "Measurement of Burst ("Popcorn") Noise in Linear IC's".

The CA6078AT and CA6741T utilize the hermetically sealed 8-lead TO-5 type package. The CA6078AT and the CA6741T can also be supplied on request with dual-in-line formed leads. These types are identified as the CA6078AS and CA6741S. This formed-lead configuration conforms to that of the 8-lead dual-in-line (Mini–Dip) package. For terminal arrangements, see page 4.

*Formerly Dev. No. TA5807X and TA6029 respectively.



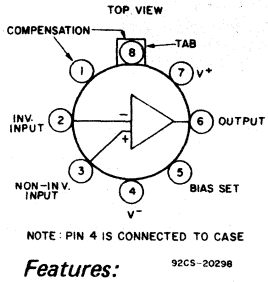
CA6741T

Applications:

- **Low-noise AC amplifier**
- **Narrow-band or band-pass filter**
- **Integrator or differentiator**
- **DC amplifier**
- **Summing amplifier**

Features:

- **Internal phase compensation**
- **Input bias current: 500 nA max.**
- **Input offset current: 200 nA max.**
- **Open-loop voltage gain: 50,000 (94 dB) min.**
- **Input offset voltage: 5 mV max.**



CA6078AT

Applications:

- **Portable electronics**
- **Medical electronics**
- **DC amplifier**
- **Narrow-band or band-pass filter**
- **Integrator or differentiator**
- **Instrumentation**
- **Telemetry**
- **Summing amplifier**

Features:

- **Open-loop voltage gain: 40,000 (92 dB) min.**
- **Input offset voltage:3.5 mV max.**
- **Operates with low total supply voltage: 1.5 V min. (± 0.75 V)**
- **Low quiescent operating current: adjustable for application optimization**
- **Input bias current: adjustable to below 1 nA**

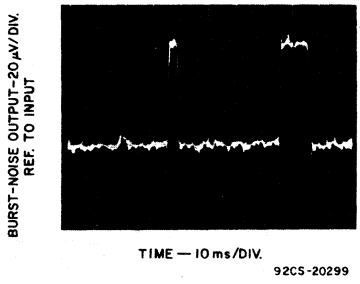
CA6078, CA6741

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

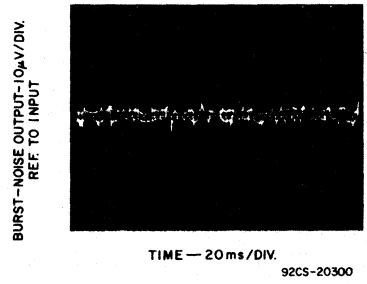
	CA6741T	CA6078AT
DC Supply Voltage (between V^+ and V^- terminals)	44 V	36 V
Differential-Mode Input Voltage	±30 V	±6 V
Common-Mode DC Input Voltage▲	±15 V	V^+ to V^-
Device Dissipation:		
Up to 75°C (CA6741T), Up to 125° (CA6078AT)	500 mW	250 mW
Above 75°C	Derate linearly 5 mW/°C	–
Temperature Range:		
Operating	−55 to +125 °C	−55 to +125 °C
Storage	−65 to +150 °C	−65 to +150 °C
Output Short-Circuit Duration●	No limitation	No limitation
Lead Temperature (During soldering):		
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm)		
from case for 10 seconds max.	300 °C	300 °C

▲If Supply Voltage is less than ±15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

●Short circuit may be applied to ground or to either supply.



a. Typ. device with high-burst-noise characteristic.



b. Typ. device controlled for burst noise.

Fig.1—Typ. waveforms of type with high burst noise and type controlled for burst noise.

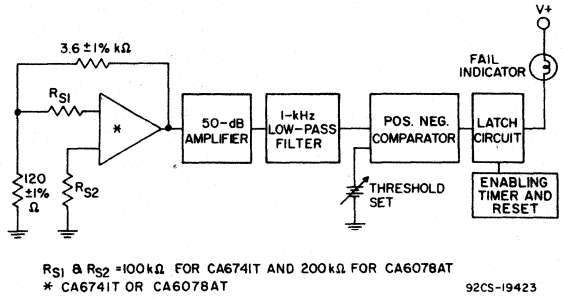


Fig.2—Block diagram of burst-noise "popcorn" test equipment.

ELECTRICAL CHARACTERISTICS – CA6078AT, *For Equipment Design.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Supply Volts: $V^+ = 6$, $V^- = -6$ $T_A = 25^oC$, $I_Q = 20\ \mu A$	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz $R_{S1} = R_{S2} = 200\ k\Omega$	Device is rejected if the total noise voltage (burst + $1/f$), referred to input, exceeds 20 μV peak, during a 30-sec. test period.			
Principal Characteristics (For detailed Electrical Characteristics refer to CA3078AT Data Bulletin, File No. 535.)						
Input Offset Voltage	V_{IO}	$R_S \leq 10\ k\Omega$	–	0.7	3.5	mV
Input Offset Current	I_{IO}		–	0.5	2.5	nA
Input Bias Current	I_{IB}		–	7	12	nA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 10\ k\Omega$	40,000	100,000	–	
		$V_O = \pm 4V$	92	100	–	dB
Common-Mode Input Voltage Range	V_{ICR}	$V^+ = V^- = 15$ V	±14	–	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\Omega$	80	115	–	dB
Output Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10\ \Omega$	±13.7	±14.1	–	V
		$R_L \geq 2\ k\Omega$	–	±14	–	
Supply Current	I_Q		–	20	25	μA

ELECTRICAL CHARACTERISTICS – CA6741T, *For Equipment Design.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Supply Volts; $V^+ = 15$, $V^- = -15$ $T_A = 25^oC$	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz $R_{S1} = R_{S2} = 100\ k\Omega$	Device is rejected if the total noise voltage (burst + $1/f$), referred to input, exceeds 20 μV peak, during a 30-sec. test period.			
Principal Characteristics (For detailed Electrical Characteristics refer to CA3741T Data Bulletin, File No. 531.)						
Input Offset Voltage	V_{IO}	$R_S \leq 10\ k\Omega$	–	1	5	mV
Input Offset Current	I_{IO}		–	20	200	nA
Input Bias Current	I_{IB}		–	80	500	nA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 2\ k\Omega$	50,000	200,000	–	
		$V_O = \pm 10$ V	94	106	–	dB
Common-Mode Input Voltage Range	V_{ICR}		±12	±13	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\Omega$	70	90	–	dB
Output Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10\ k\Omega$	±12	±14	–	V
		$R_L \geq 2\ k\Omega$	±10	±13		
Supply Current	I_Q		–	1.7	2.8	mA

CA6078, CA6741

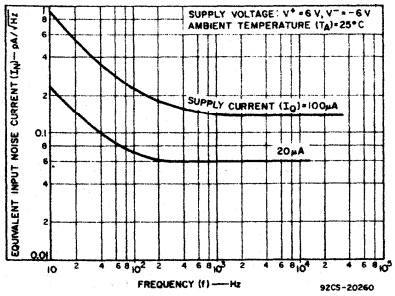


Fig.3—I_N vs. Frequency for CA6078AT.

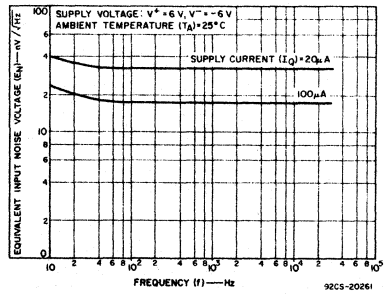


Fig.4—E_N vs. Frequency for CA6078AT.

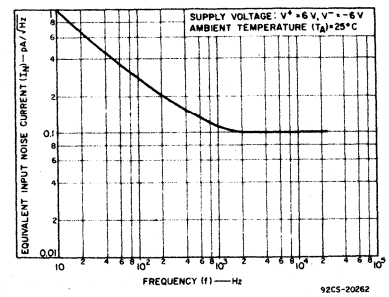


Fig.5—I_N vs. Frequency for CA6741T.

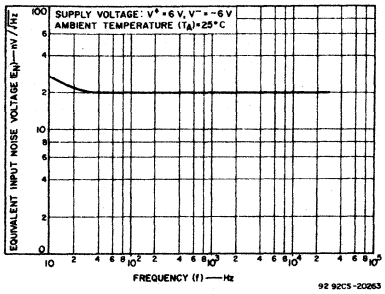


Fig.6—E_N vs. Frequency for CA6741T.

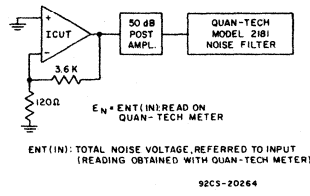


Fig.7—Test block diagram for E_N.

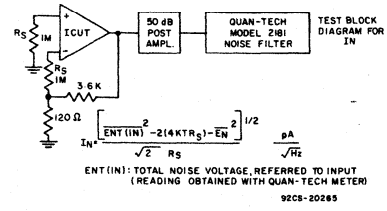
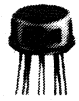
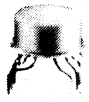


Fig.8—Test block diagram for I_N.


(E Suffix)
8-LEAD
(MINI-DIP)
H-1517


(T Suffix)
8-LEAD
TO-5 H-1528


(E Suffix)
14-LEAD DIP
H-1817


(S Suffix)
8-LEAD
TO-5
(DIL-CAN)
H-1787

BiMOS Operational Amplifiers

With MOS/FET Input, Composite Bipolar/MOS Output

Single Amplifier: CA080, CA081
Dual Amplifier: CA082, CA083
Quad Amplifier: CA084

Features:

- *Very low input bias and offset currents*
- *Input impedance typically 1.5 x 10^{12} Ω*
- *Low input offset voltage*
- *Wide common-mode input voltage range*
- *Low power consumption*
- *Fast slew rate*
- *Unity-gain bandwidth = 5 MHz (typ.)*
- *Wide output voltage swing*
- *Low distortion*
- *Continuous short circuit protection*
- *Direct replacement for industry type TL080 series in most applications*

The RCA-CA080, CA081, CA082, CA083, and CA084 BiMOS operational amplifiers combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOS/FET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range. The bipolar and MOS output transistors allow a wide output voltage swing and provide a high output current capability.

Package Selection Chart

Type No.	Package Type & Suffix			
	8L TO-5	DIL-CAN	Mini-DIP	14L DIP
CA080	T	S	E	
CA080A	T	S	E	
CA080B			E	
CA080C	T	S		
CA081	T	S	E	
CA081A	T	S	E	
CA081B			E	
CA081C	T	S		
CA082	T	S	E	
CA082A	T	S	E	
CA082B			E	
CA082C	T	S		
CA083				E
CA083A				E
CA083B				E
CA084				E
CA084A				E
CA084B				E

Applications:

- *Inverters*
- *High-Q notch filters*
- *IC preamplifiers*
- *Unity Gain Absolute Value Amplifiers*
- *Sample and hold amplifiers*
- *Active filters*

The CA080 is externally phase-compensated, and the CA081, CA082, CA083, and CA084 are internally phase-compensated. All types except the CA082 have provisions for external offset nulling.

The CA080, CA081, CA082, CA083, and CA084 are available in chip form (H Suffix).

Operating Temperature Ranges:

-55 to +125° C	0 to +70° C
CA080T, CA080S	CA080CT, CA080CS
CA080AT, CA080AS	CA080BE
CA081T, CA081S	CA081CT, CA081CS
CA081AT, CA081AS	CA081BE
CA082T, CA082S	CA082CT, CA082CS
CA082AT, CA082AS	CA082BE
	CA083BE, CA083AE
	CA083BE
	CA084, CA084AE
	CA084BE

CA080, CA081, CA082, CA083, CA084 Series

MAXIMUM RATINGS, *Absolute Maximum Values:*

DC SUPPLY VOLTAGE V± ..... ±18 V
DIFFERENTIAL INPUT VOLTAGE ..... ±16 V
INPUT VOLTAGE RANGE ..... ± 15 V
INPUT CURRENT ..... 1 mA
OUTPUT SHORT-CIRCUIT DURATION ..... UNLIMITED*
POWER DISSIPATION, PD:
At TA = 25°C:
E Suffix ..... 625 mW
T Suffix ..... 680 mW
Derating Factors:
Mini-DIP ..... Derate linearly at 6.67 mW/°C above 56°C
14-Lead DIP ..... Derate linearly at 6.67 mW/°C above 56°C
TO-5 ..... Derate linearly at 6.67 mW/°C above 56°C
AMBIENT TEMPERATURE RANGE:
CT, CS, E, Suffixes ..... 0 to +70°C
T, S, Suffixes ..... -55 to +125°C
STORAGE TEMPERATURE RANGE, ALL TYPES ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

* The output may be shorted to ground or either supply if the maximum temperature and dissipation ratings are observed.

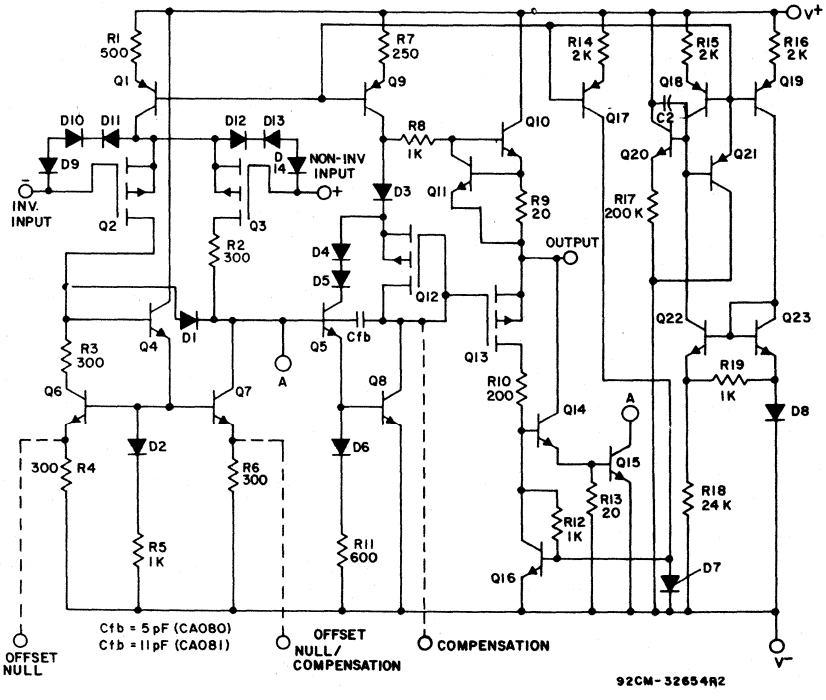
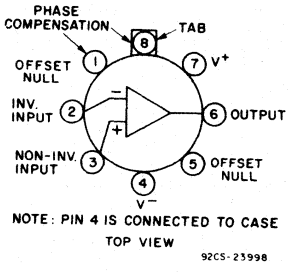


Fig. 1 - Schematic diagram of the CA080, CA081, CA082, CA083, and CA084.

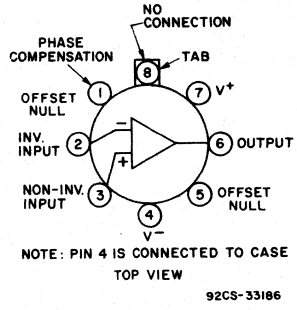
CA080, CA081, CA082, CA083, CA084 Series

Texas Instruments-to-RCA Package Suffix Cross Reference Chart

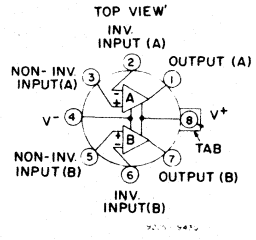
Texas Instruments		RCA	
Suffix	**Description**	**Suffix**	**Description**
ACJG	Ceramic DIL	AS	DILCAN TO-5
ACL	TO-5	AT	TO-5
ACN	Plastic DIL	AE	Plastic DIL
ACP	Plastic DIL	AE	Plastic DIL
CJG	Ceramic DIL	CS	DILCAN TO-5
CL	TO-5	CT	TO-5
CN	Plastic DIL	E	Plastic DIL
CP	Plastic DIL	E	Plastic DIL
IJG	Ceramic DIL	S	DILCAN TO-5
IL	TO-5	T	TO-5
IP	Plastic DIL	E	DILCAN TO-5
MJG	Ceramic DIL	S	DILCAN TO-5
ML	TO-5	T	TO-5
AML	TO-5	AT	TO-5
BCP	Plastic DIL	BE	Plastic DIL



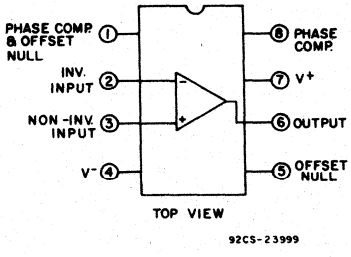
CA080
T, S Suffixes



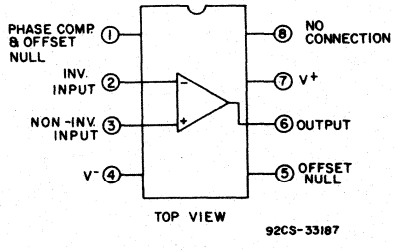
CA081
T, S Suffixes



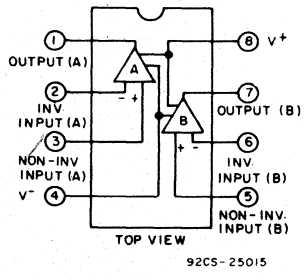
CA082
T, S Suffixes



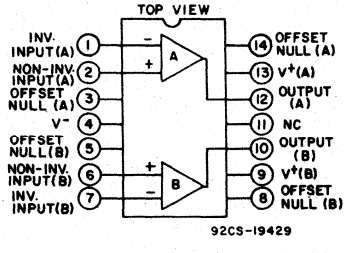
CA080
E Suffix



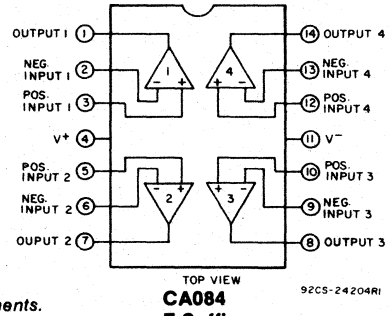
CA081
E Suffix



CA082
E Suffix



CA083
E Suffix



CA084
E Suffix

Fig. 2 - Terminal assignments.

CA080, CA081, CA082, CA083, CA084 Series

TYPICAL OPERATING CHARACTERISTICS at $V\pm = 15$ V, $T_A = 25°C$

CHARACTERISTIC	TEST CONDITIONS	VALUE	UNITS
Slew Rate at Unity Gain, SR	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, A_{VD} = 1	13	V/μs
Rise Time, t_r	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, A_{VD} = 1	0.1	μs
Overshoot Factor		10	%
Equivalent Input Noise Voltage, e_n	R_S = 100 Ω, f = 1 kHz	40	nV/√Hz

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ and $T_A = -55$ to $+125°C$ for types supplied in TO-5 style packages (T, S Suffixes). $V^+ = \pm 15$ V

This does not include CA080C, CA081C, or CA082C. These types are supplied in TO-5 packages, but they are specified over the range of 0 to 70°C, and their limits are the same as those for the CA080, CA081, CA082, and CA083 in plastic packages over the range 0 to 70°C.

CHARACTERISTIC	TEST CONDITIONS	−55 to +125°C	+25°C	LIMITS: CA080T, S CA081T, S CA082T, S Min.	Typ.	Max.	LIMITS: CA080AT, S CA081AT, S CA082AT, S Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	R_S = 50Ω	X		—	3	6	—	2	3	mV
			X	—	—	9	—	—	5	
Temperature Coefficient of Input Offset Voltage, $\propto V_{IO}$	R_S = 50 Ω		X	—	10	—	—	10	—	μV/°C
Input Offset Current, I_{IO}		X		—	5	20	—	5	20	pA
			X	—	—	4	—	—	2	nA
Input Current		X		—	15	40	—	15	40	pA
			X	—	—	10	—	—	5	nA
Common-Mode Input Voltage Range, V_{ICR}		X		±12	—	—	±12	—	—	V
Maximum Output Voltage Swing, V_{OP-P}	R_L = 10 kΩ	X		24	27	—	24	27	—	V
	$R_L \geq 10$ kΩ		X	24	—	—	24	—	—	
	$R_L \geq 2$ kΩ		X	20	24	—	20	24	—	
Large-Signal Differential Voltage Gain, A_{VD}	$R_L \geq 2$ kΩ, $V_O = \pm 10$V	X		50	200	—	50	200	—	V/mV
			X	25	—	—	25	—	—	
Unity-Gain Bandwidth		X		—	5	—	—	5	—	MHz
Input Resistance, R_I		X		—	1.5	—	—	1.5	—	TΩ
Common-Mode Rejection Ratio, CMRR	$R_S \leq 10$ kΩ	X		80	86	—	80	86	—	dB
Power Supply Rejection Ratio, PSRR ($\Delta V^+ / \pm \Delta V_{IO}$)	$R_S \leq 10$ kΩ	X		80	86	—	80	86	—	dB
Supply Current, I^+ (per amp., CA082, CA083)	No load, No Signal	X		—	1.4	2.8	—	1.4	2.8	mA
Channel Separation, V_{O1}/V_{O2} (between amps., CA082, CA083)	A_{VD} = 100	X		—	120	—	—	120	—	dB

ELECTRICAL CHARACTERISTICS at T_A = 25°C, T_A = 0 to +70°C for types supplied in plastic dual-in-line packages (E Suffix). V^+ = ±15 V

CHARACTERISTIC	TEST CONDITIONS	0 to 70°C	+25°C	LIMITS CA080BE CA081BE CA082BE CA083BE CA084BE Min.	Typ.	Max.	LIMITS CA080AE CA081AE CA082AE CA083AE CA084AE Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	R_S = 50Ω	X		—	2	3	—	3	6	mV
			X	—	—	5	—	—	7.5	
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 50 Ω		X	—	10	—	—	10	—	μV/°C
Input Offset Current, I_{IO}		X		—	5	10	—	5	20	pA
			X	—	—	0.4	—	—	0.6	nA
Input Current		X		—	15	30	—	15	40	pA
			X	—	—	0.7	—	—	1	nA
Common-Mode Input Voltage Range, V_{ICR}		X		±12	—	—	±12	—	—	V
Maximum Output Voltage Swing, V_{OP-P}	R_L = 10 kΩ	X		24	27	—	24	27	—	V
	R_L ≥ 10 kΩ		X	24	—	—	24	—	—	
	R_L ≥ 2 kΩ		X	20	24	—	20	24	—	
Large-Signal Differential Voltage Gain, A_{VD}	R_L ≥ 2 kΩ,	X		50	200	—	50	200	—	V/mV
	V_O = ±10V		X	—	—	—	—	—	—	
Unity-Gain Bandwidth		X		—	5	—	—	5	—	MHz
Input Resistance, R_I		X		—	1.5	—	—	1.5	—	TΩ
Common-Mode Rejection Ratio, CMRR	R_S ≤ 10 kΩ	X		80	86	—	80	86	—	dB
Power Supply Rejection Ratio, PSRR ($\Delta V^+/\pm\Delta V_{IO}$)	R_S ≤ 10 kΩ	X		80	86	—	80	86	—	dB
Supply Current, I^+ (per amp., CA082, CA083, CA084)	No load, No Signal	X		—	1.4	2.8	—	1.4	2.8	mA
Channel Separation, V_{O1}/V_{O2} (between amps.,CA082, CA083)	A_{VD} = 100	X		—	120	—	—	120	—	dB

CA080, CA081, CA082, CA083, CA084 Series

ELECTRICAL CHARACTERISTICS at T_A = 25°C, T_A = 0 to 70°C for types supplied in plastic dual-in-line packages (E Suffix). V^+ = ±15 V

The limits for the CA080C, CA081C, and CA082C in TO-5 packages are the same as those for the types in this chart.

CHARACTERISTIC	TEST CONDITIONS	0 to 70°C	+25°C	LIMITS CA080E, T CA081E, T CA082E, T CA083E CA084E Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	R_S = 50Ω	X		—	5	15	mV
			X	—	—	20	
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 50 Ω		X	—	10	—	μV/°C
Input Offset Current, I_{IO}		X		—	5	30	pA
			X	—	—	1	nA
Input Current		X		—	15	50	pA
			X	—	—	2	nA
Common-Mode Input Voltage Range, V_{ICR}		X		±10	—	—	V
Maximum Output Voltage Swing, V_{OP-P}	R_L = 10 kΩ	X		24	27	—	V
	$R_L \geq$ 10 kΩ		X	24	—	—	
	$R_L \geq$ 2 kΩ		X	20	24	—	
Large-Signal Differential Voltage Gain, A_{VD}	$R_L \geq$ 2 kΩ, V_O = ±10V	X		25	200	—	V/mV
			X	—	—	—	
Unity-Gain Bandwidth		X		—	5	—	MHz
Input Resistance, R_I		X		—	1.5	—	TΩ
Common-Mode Rejection Ratio, CMRR	$R_S \leq$ 10 kΩ	X		70	76	—	dB
Power Supply Rejection Ratio, PSRR ($\Delta V^+ / \pm \Delta V_{IO}$)	$R_S \leq$ 10 kΩ	X		70	76	—	dB
Supply Current, I^+ (per amp., CA082, CA083)	No load, No Signal	X		—	1.4	2.8	mA
Channel Separation, V_{O1}/V_{O2} (between amps., CA082, CA083)	A_{VD} = 100	X		—	120	—	dB

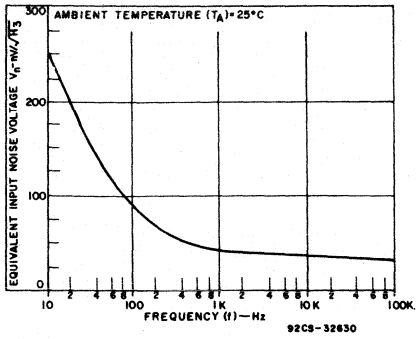


Fig. 3 - Noise voltage as a function of frequency.

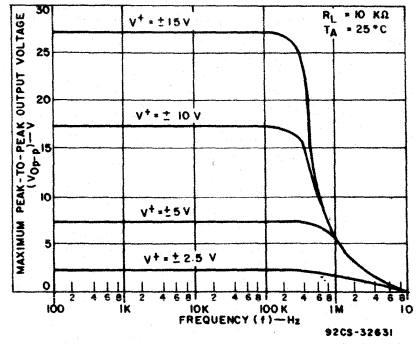


Fig. 4 - Output voltage as a function of frequency.

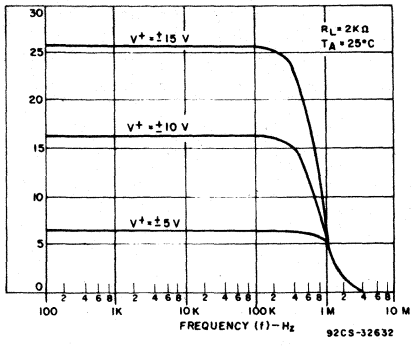


Fig. 5 - Output voltage as a function of frequency.

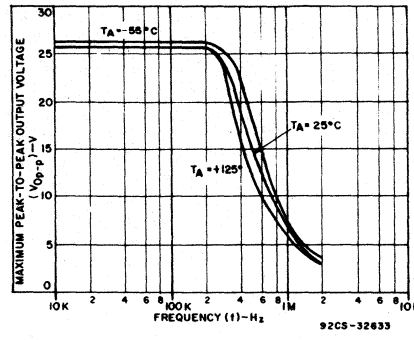


Fig. 6 - Output voltage as a function of frequency.

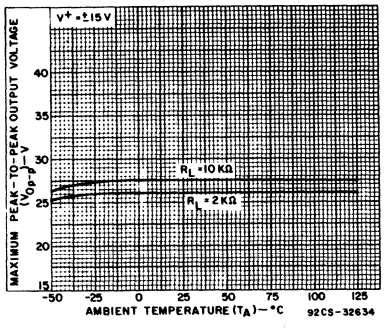


Fig. 7 - Output voltage as a function of ambient temperature.

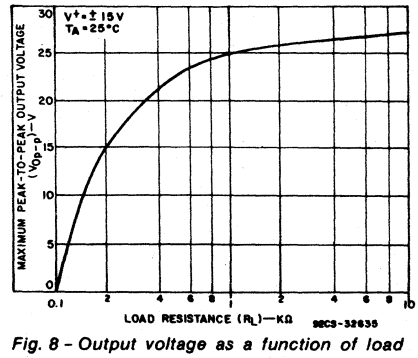


Fig. 8 - Output voltage as a function of load resistance.

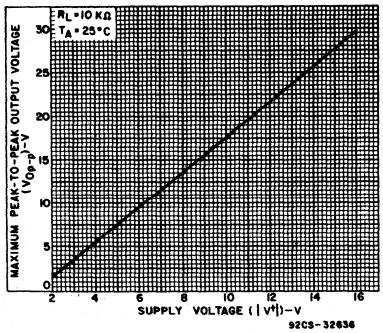


Fig. 9 - Output voltage as a function of supply voltage.

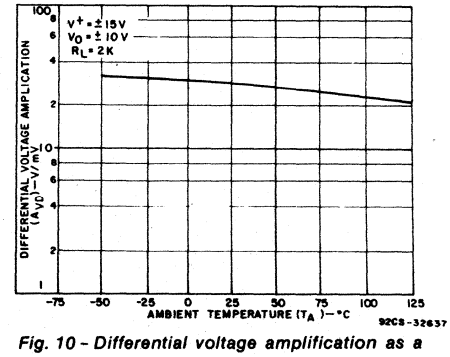


Fig. 10 - Differential voltage amplification as a function of ambient temperature.

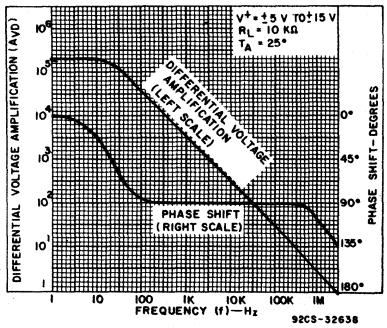


Fig. 11 - Differential voltage amplification as a function of frequency.

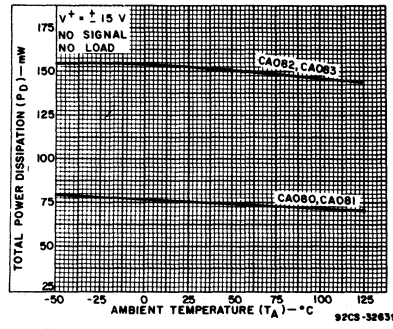


Fig. 12 - Total power dissipation as a function of ambient temperature.

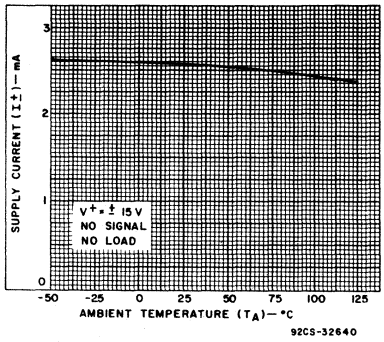


Fig. 13 - Supply current as a function of ambient temperature.

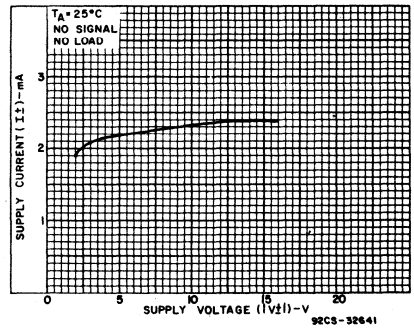


Fig. 14 - Supply current as a function of supply voltage.

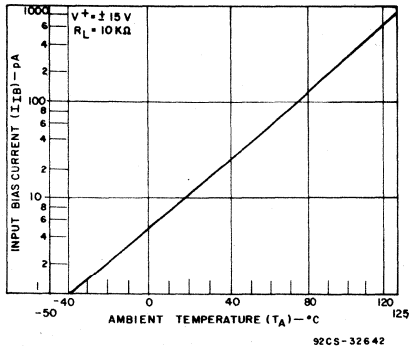


Fig. 15 - Input bias current as a function of ambient temperature.

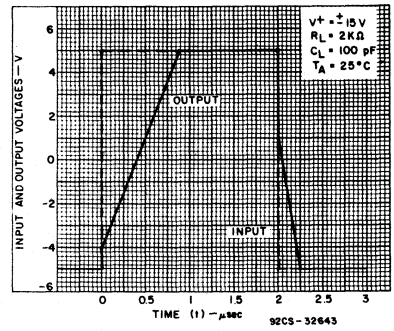


Fig. 16 - Voltage follower large-signal pulse response.

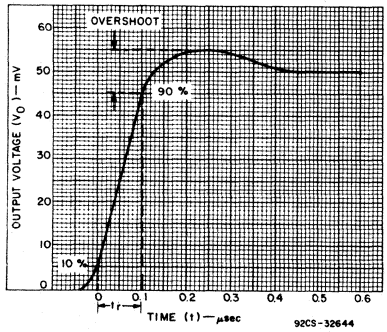


Fig. 17 - Output voltage as a function of elapsed time.

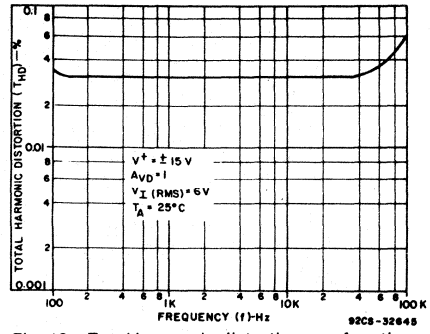


Fig. 18 - Total harmonic distortion as a function of frequency.

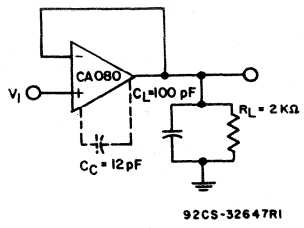


Fig. 19 - Unity-gain amplifier.

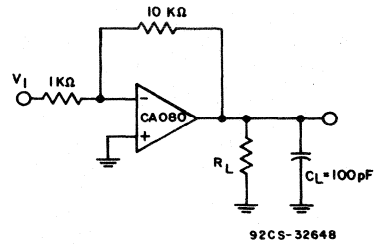


Fig. 20 - 10X inverting amplifier.

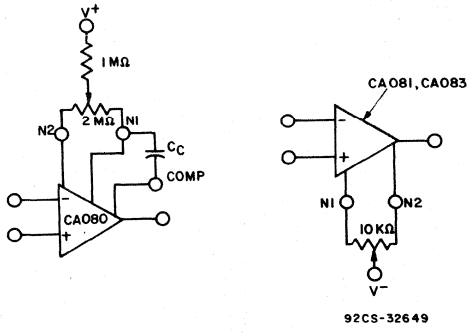


Fig. 21 - Input-offset voltage null circuits.

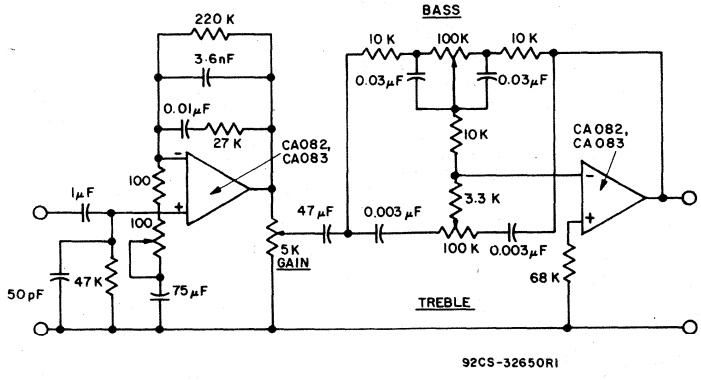


Fig. 22 - IC preamplifier.

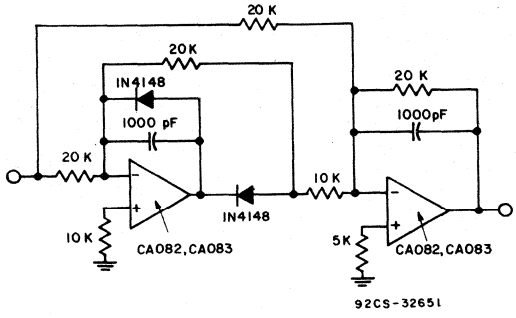


Fig. 23 - Unity-gain absolute-value amplifier.

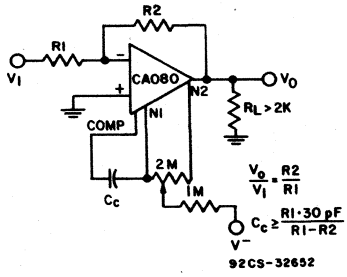


Fig. 24 - Inverting amplifier with single-pole compensation and offset adjustment.

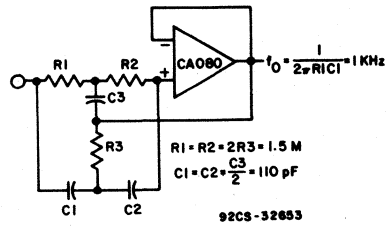


Fig. 25 - High Q notch filter.

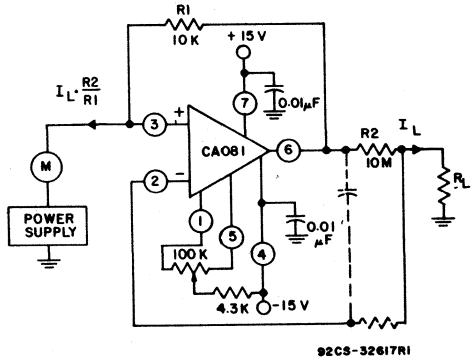


Fig. 26 - Basic current amplifier for low-current measurement systems.

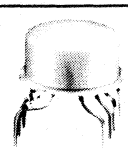
CURRENT AMPLIFIER

The low input-terminal current needed to drive the CA081 makes it ideal for use in current-amplifier applications such as the one shown in Fig.26. In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R2/R1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100 nA, with values shown, the load current presented to the supply will be 100 μA; a much easier current to measure in many systems.

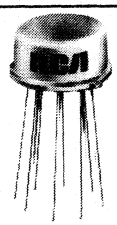
Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output-load capacitance and the potential oscillation in this situation. Essentially, the necessary high-frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types



S-Suffix Types
(DIL-CAN)
H-1787



T-Suffix Types
(TO-5 Style)
H-1528

E-Suffix Types
(Mini-DIP)
H-1817

Dual Operational Amplifiers

For Commerical, Industrial, and Military Applications

Features:

- *Internal frequency compensation for unity gain*
- *High dc voltage gain - 100 dB typ.*
- *Wide bandwidth at unity gain - 1 MHz typ.*
- *Wide power supply range:*
  Single supply 3 to 30 V
  Dual supplies ± 1.5 to ± 15 V
- *Low supply current - 1.5 mA typ.*
- *Low input bias current*
- *Low input offset voltage and current*
- *Input common-mode voltage range includes ground*
- *Differental input voltage range equal to V+ range*
- *Large output voltage swing - 0 to V+ -1.5 V*

The RCA-CA158, CA158A, CA258, CA258A, CA358, CA358A and CA2904 types consist of two independent, high gain, internally frequency compensated operational amplifiers which are designed specifically to operate from a single power supply over a wide range of voltages. They may also be operated from split power supplies. The supply current is basically independent of the supply voltage over the recommended voltage range.

These devices are particularly useful in interface circuits with digital systems and can be operated from the single common 5 Vdc power supply. They are also intended for transducer amplifiers, dc gain blocks and many other conventional op amp circuits which can benefit from the single power supply capability.

The CA158, CA158A, CA258, CA258A, CA358, CA358A, and CA2904 types are supplied in 8-lead dual-in-line plastic packages (MINI-DIP, E suffix), 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads (DIL-CAN, S suffix). The CA358 is also supplied in chip form (H suffix).

The CA158, CA158A, CA258, CA258A, CA358, CA358A, and CA2904 types are an equivalent to or a replacement for the industry types 158, 158A, 258, 258A, 358, 358A, and CA2904.

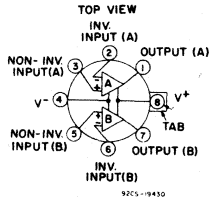


Fig. 1 - Functional diagram for CA158, CA258, and CA358 S- and T-suffix types.

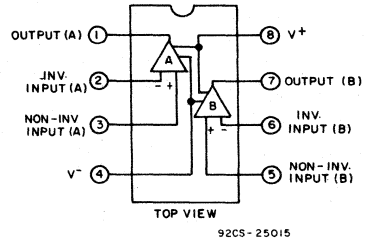


Fig. 2 - Functional diagram for CA158, CA258, CA358, and CA2904 E-suffix types.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

SUPPLY VOLTAGE, V^+:	
CA2904	26 V or ± 13 V
Other Types	32 V or ± 16 V
DIFFERENTIAL INPUT VOLTAGE:	
All Types	± 32 V
INPUT VOLTAGE	−0.3 V to V^+ V
INPUT CURRENT ($V_I < -0.3$ V) +	50 mA
OUTPUT SHORT CIRCUIT TO GROUND ($V^+ \leq 15$ V)*	Continuous
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	630 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to + 125°C
Storage	−65 to + 150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+ 300 °C

+ This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V dc.

* The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

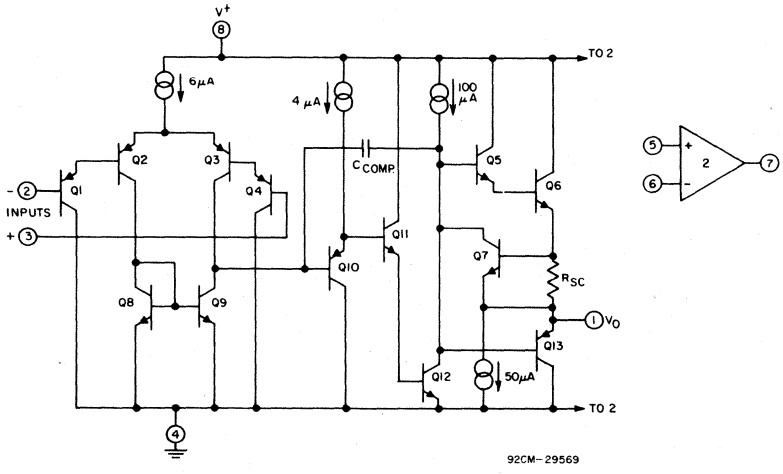


Fig.3 – Schematic diagram – one of two operational amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply For Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA158A (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
T_A = 25°C					
Input Offset Voltage, V_{IO}	Note 3	–	1	2	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	2	10	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	20	50	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
T_A = –55 to +125°C					
Input Offset Voltage, V_{IO}	Note 3	–	–	4	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	15	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	30	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	200	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	100	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA258A (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
T_A = 25°C					
Input Offset Voltage, V_{IO}	Note 3	–	1	3	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	2	15	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	40	80	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
T_A = –25 to +85°C					
Input Offset Voltage, V_{IO}	Note 3	–	–	4	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_s = 0	–	7	15	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	30	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	200	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	100	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA358A (E. T. S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	3	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	100	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	25	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	65	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = 0 to +70°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	5	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	20	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	75	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	300	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	200	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of thedevice. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA158 (E, T, S) CA258 (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
T_A = 25°C					
Input Offset Voltage, V_{IO}	Note 3	–	2	5	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	3	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	150	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
T_A = –55 to + 125°C (CA158); T_A = –25 to +85°C (CA258)					
Input Offset Voltage, V_{IO}	Note 3	–	–	7	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	100	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	300	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA358 (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	25	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	65	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = 0 to +70°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	9	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	150	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	500	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ \geq$ 15 V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA2904E			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
T_A = 25°C					
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	R_L = 10 kΩ .	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	—	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	50	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	50	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
T_A = -40 to +85°C					
Input Offset Voltage, V_{IO}	Note 3	–	–	10	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	45	200	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	500	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of thedevice. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

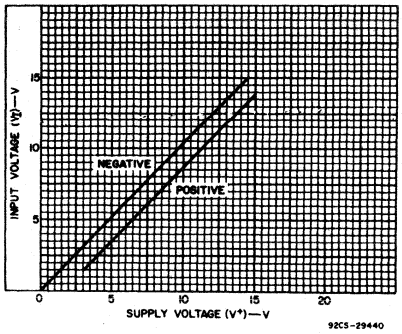


Fig.4 – Input voltage range as a function of supply voltage.

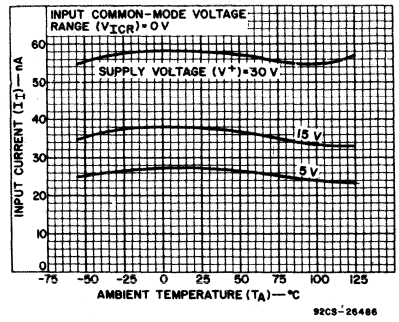


Fig.5 – Input current as a function of ambient temperature.

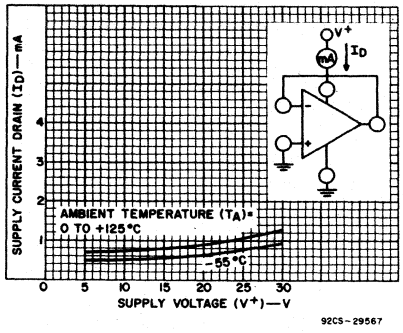


Fig.6 – Supply current drain as a function of supply voltage.

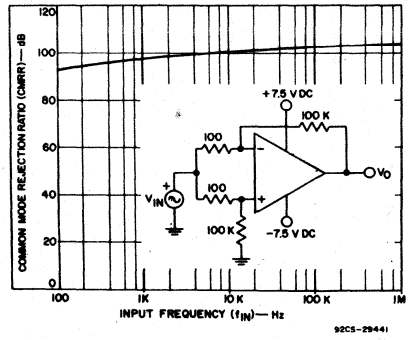


Fig.7 – Common mode rejection ratio as a function of input frequency.

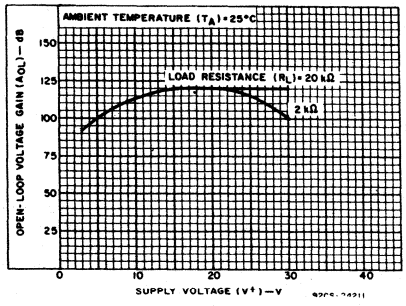


Fig.8 – Voltage gain as a function of supply voltage.

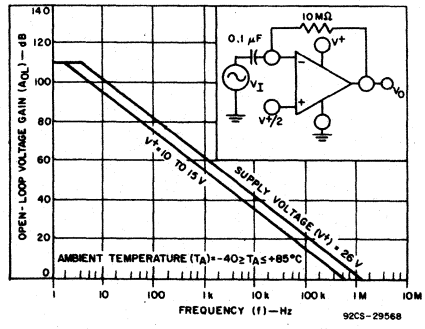


Fig.9 – Open-loop frequency response.

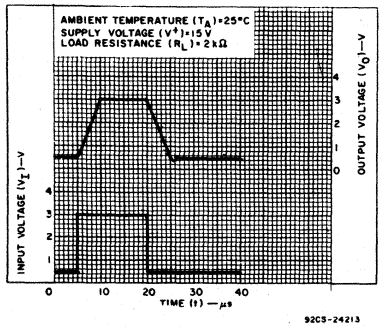


Fig.10 – Voltage follower pulse response.

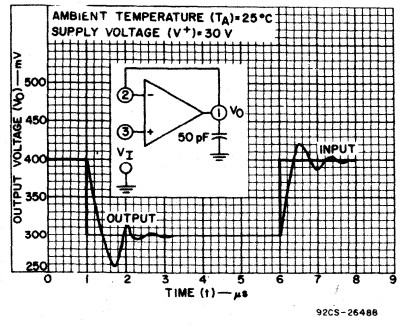


Fig.11 – Voltage follower pulse response (small signal).

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

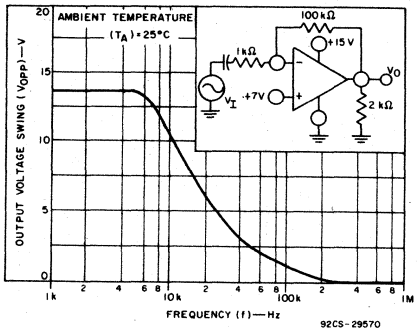


Fig.12 – Large-signal frequency response.

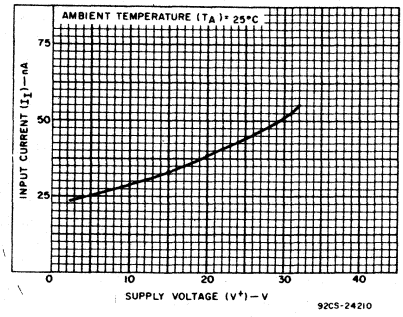


Fig.13 – Input current as a function of supply voltage.

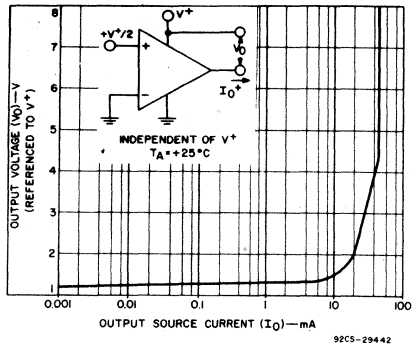


Fig.14 – Output source current characteristics.

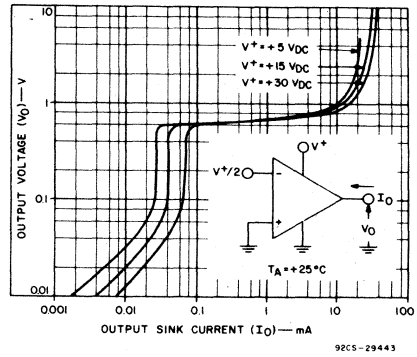


Fig.15 – Output sink current characteristics.

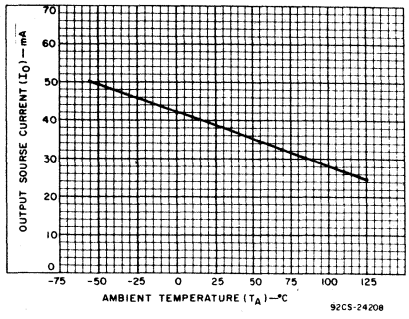


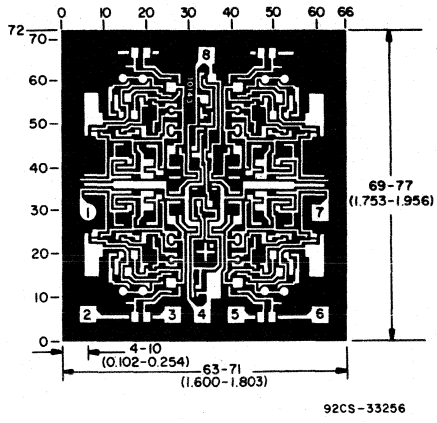
Fig.16 – Output current as a function of ambient temperature.

ORDERING INFORMATION

These packages are identified by Suffix Letters indicated in the chart shown below. When ordering these devices, it is important that the appropriate suffix letter be affixed to the type number of the device required.

PACKAGE	SUFFIX LETTERS	TYPES
8-Lead Dual-In-Line Plastic with	E	CA158, A CA258, A CA358, A CA2904
8-Lead TO-5 Style with Standard Leads	T	CA158, A CA258, A CA358, A
8-Lead TO-5 Style with Dual-In-Line Formed Leads	S	

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

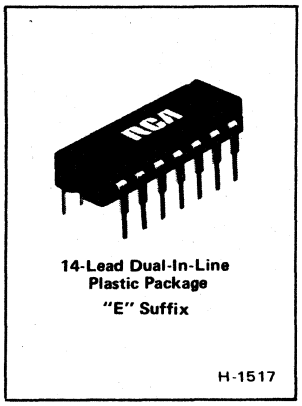


Dimensions and pad layout for CA358H..

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA124, CA224, CA324 Types



14-Lead Dual-In-Line Plastic Package "E" Suffix

H-1517

Quad Operational Amplifiers

For Commercial, Industrial, and Military Applications

Features:

- Operation from single or dual supplies
- Unity-gain bandwidth . . . . . 1 MHz (typ.)
- DC voltage gain . . . . . 100 dB (typ.)
- Input bias current . . . . . 45 nA (typ.)
- Input offset voltage . . . . . 2 mV (typ.)
- Input offset current . . . . . 5 nA (typ.) for CA224, CA324
  . . . . . 3 nA (typ.) for CA124
- Replacement for industry types 124, 224, 324

The RCA-CA124, -CA224, and -CA324 consist of four independent, high-gain operational amplifiers on a single monolithic substrate. An on-chip capacitor in each of the amplifiers provides frequency compensation for unity gain. These devices are designed specifically to operate from either single or dual supplies, and the differential voltage range is equal to the power-supply voltage. Low power drain and an input common-mode voltage range of from 0 V to $V^+ - 1.5$ V (single-supply operation) make the CA124, CA224, and CA324 suitable for battery operation.

Applications

- Summing amplifiers
- Multivibrators
- Oscillators
- Transducer amplifiers
- DC gain blocks

The CA124, CA224, and CA324 are supplied in a 14-lead dual-in-line plastic package (E suffix). The CA324 is also available in chip form (H suffix).

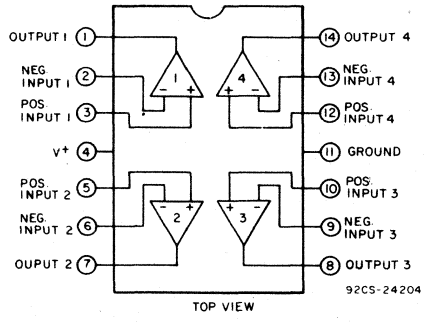


Fig. 1 – Functional diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

SUPPLY VOLTAGE	32 V or ±16 V
DIFFERENTIAL INPUT VOLTAGE	±32 V
INPUT VOLTAGE	−0.3 V to +32 V
INPUT CURRENT ($V_I < -0.3$ V)†	50 mA
OUTPUT SHORT CIRCUIT TO GROUND ($V^+ \leq 15$ V)*	Continuous
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

*The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device.

†This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V dc.

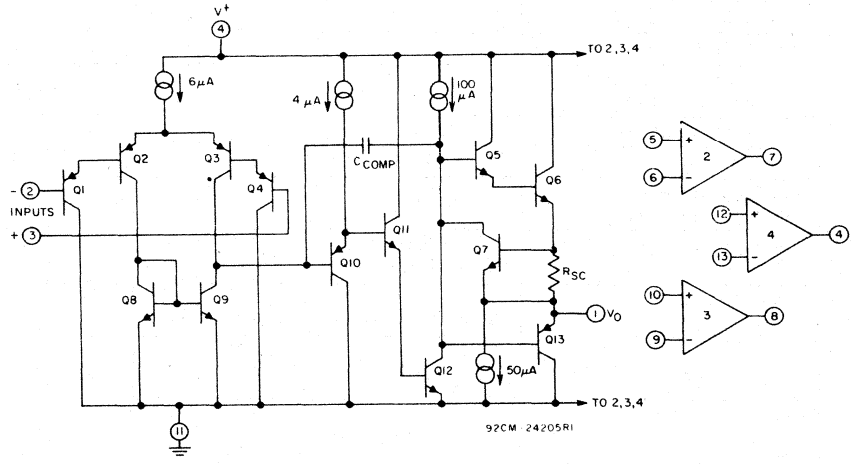


Fig. 2—Schematic diagram—one of four operational amplifiers.

CA124, CA224, CA324 Types

ELECTRICAL CHARACTERISTICS (Values Apply For Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	CA124 LIMITS			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	5	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+–1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+=30 V	0	–	V^+–1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	3	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	150	nA
Output Current (Source), I_O	V_I^+=+1 V, V_I^-=0 V, V^+=15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+=0 V, V_I^-=1 V, V^+=15 V	10	20	–	mA
	V_I^+=0 V, V_I^-=1 V, V_O=200 mV	12	50	–	μA
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	94	100	–	dB
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f=1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = –55 to +125°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	7	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	100	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	–	300	nA
Supply Current, I^+	$R_L = \infty$ On All Ampl.	–	0.8	2	mA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V	0	–	V^+–2	V
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	88	–	–	dB
Output Voltage Swing: High-Level, V_{OH}	R_L=2 kΩ, V^+=30 V	26	–	–	V
	R_L=10 kΩ	27	28	–	
Low-Level, V_{OL}	R_L=10 kΩ	–	5	20	mV
Output Current: Source, I_O	V_I^+=1 V_{DC}, V_I^-=0, V^+=15 V	10	20	–	mA
Sink, I_O	V_I^-=1 V_{DC}, V_I^+=0, V^+=15 V	5	8	–	mA
Differential Input Voltage	Note 2	–	–	V^+	V

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go to +32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

ELECTRICAL CHARACTERISTICS (Values apply for each operational amplifier)

CHARACTERISTIC	TEST CONDITIONS	CA224, CA324 LIMITS			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+–1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+= 30 V	0	–	V^+–1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	V_I^+=+1 V, V_I^-=0 V, V^+=15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+=0 V, V_I^-=1 V, V^+=15 V	10	20	–	mA
	V_I^+=0 V, V_I^-=1 V, V_O=200 mV	12	50	–	μA
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	88	100	–	dB
Common-Mode Rejection Ratio, CMRR	DC	65	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = –40 to +85°C (CA224), T_A = 0 to 70°C (CA324)				
Input Offset Voltage, V_{IO}	Note 3	–	–	9	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_s = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	150	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	–	500	nA
Supply Current, I^+	R_L =∞ On All Ampl.	–	0.8	2	mA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V	0	–	V^+–2	V
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	83	–	–	dB
Output Voltage Swing: High-Level, V_{OH}	R_L = 2 kΩ, V^+ = 30 V	26	–	–	V
	R_L = 10 kΩ	27	28	–	
Low-Level, V_{OL}	R_L = 10 kΩ	–	5	20	mV
Output Current: Source, I_O	V_I^+=1 V_{DC}, V_I^-=0, V^+=15 V	10	20	–	mA
Sink, I_O	V_I^-=1 V_{DC}, V_I^+=0, V^+=15 V	5	8	–	mA
Differential Input Voltage	Note 2	–	–	V^+	V

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go to +32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

CA124, CA224, CA324 Types

TYPICAL CHARACTERISTICS CURVES

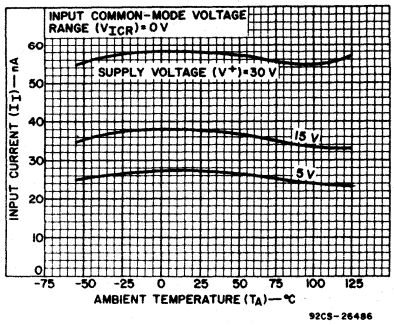


Fig. 3—Input current vs. ambient temperature.

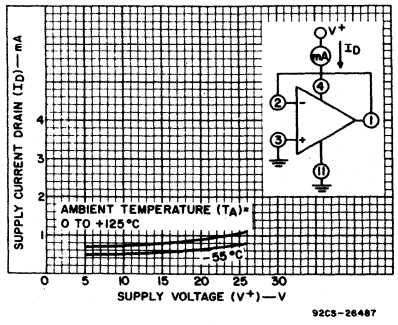


Fig. 4—Supply current drain vs. supply voltage.

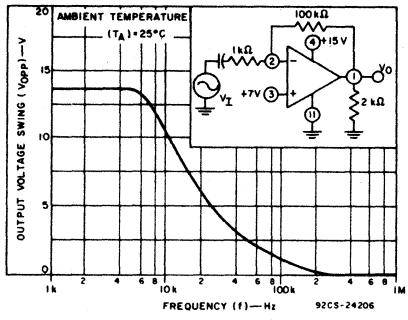


Fig. 5—Large-signal frequency response.

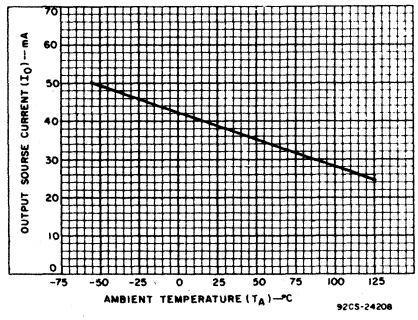


Fig. 6—Output current vs. ambient temperature.

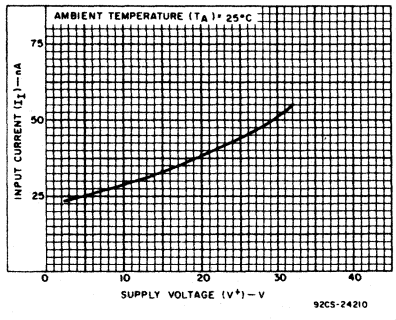


Fig. 7—Input current vs. supply voltage.

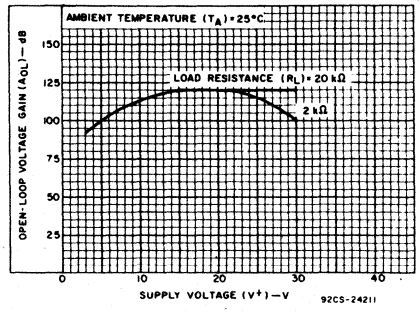


Fig. 8—Voltage gain vs. supply voltage.

TYPICAL CHARACTERISTICS CURVES (CONT'D)

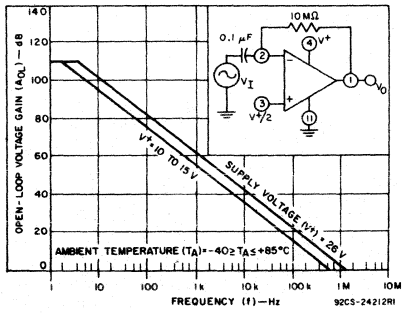


Fig. 9—Open-loop frequency response.

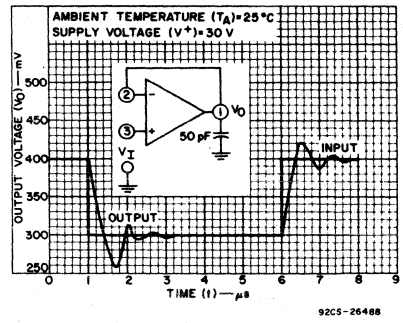


Fig. 10—Voltage follower pulse response (small signal).

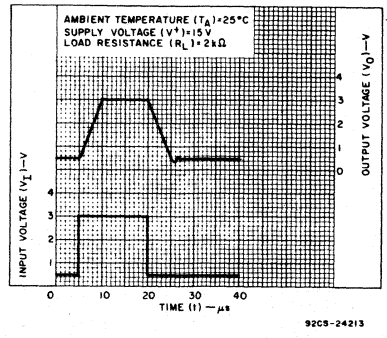
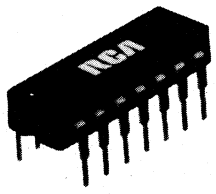


Fig. 11—Voltage follower pulse response.

CA3401E



14-Lead Dual-In-Line
Plastic Package
(E-Suffix Type)

H-1517

Quad Single-Supply Operational Amplifier

For Automotive Electronics and Industrial Control Systems

"E" Suffix Types — Standard Dual-In-Line Plastic Package

Features:
- *Single-supply operation - +5 V to +18 Vdc*
- *Internally compensated*
- *Wide unity-gain bandwidth - 5 MHz typ.*
- *Low input bias current - 50 nA typ.*
- *High open-loop gain - 2000 V/V typ.*

Applications:
- *Automotive*
- *Constant-Current Sources*
- *Multivibrators*
- *Sample and Hold*
- *Square-Wave Generator*
- *Oscillators*
- *Tachometers*
- *Active Filters*
- *Multi-Channel Amplifiers*
- *Summing Amplifiers*

The RCA-3401 is a high-gain monolithic quad operational amplifier designed specifically for applications using a single positive power supply. No external compensation is necessary. Closed-loop stability in each of the four independent amplifiers is maintained by a 3-pF on-chip capacitor. The CA3401 is ideally suited for applications in industrial control systems, automotive electronics, and general purpose amplifiers, e.g. oscillators, tachometers, active filters, and multichannel amplifiers.

The CA3401 is supplied in a 14-lead dual-in-line plastic package (E suffix), and is also available in chip form (H suffix). It is a direct replacement for the Motorola MC3401P, and is pin-compatible with the Motorola MC3301P and the National Semi-conductor LM3900N. The CA3401 can be operated over the temperature range of -55 to +125°C, although the limit values of certain specified electrical characteristics apply only over the range of 0 to +75°C.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DC SUPPLY VOLTAGE	+18 V
INPUT SIGNAL CURRENT	5 mA
DEVICE DISSIPATION:	
Up to T_A = 25°C	625 mW
Above T_A = 25°C	Derate lineary 5 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	-55 to + 125°C
Storage	-65 to + 150°C
LEAD TEMPERATURE (During soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	300°C

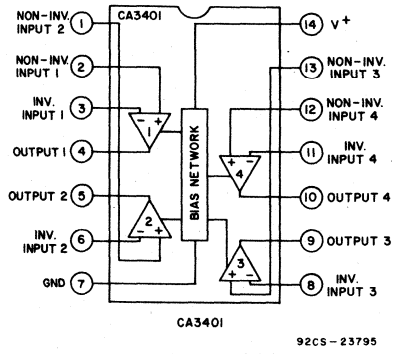


Fig. 1 - Block diagram of CA3401.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V^+ = 15 V (Unless Indicated Otherwise)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
STATIC					
Output Voltage:					
High, V_{OH}		13.5	14.2	–	V
Low, V_{OL}		–	0.03	0.1	
Max. Undistorted Output Swing, V_{OP-P}	0°C<T_A<75°C	10	13.5	–	
Output Current:					
Source, I_{SOURCE}		5	10	–	mA
Sink, I_{SINK}		0.5	1	–	
Total Quiescent Current: I_Q					
Noninverting inputs open		–	6.9	10	mA
Noninverting inputs grounded		–	7.8	14	
Input Bias Current, I_{IB}	R_L = ∞ T_A = 25°C	–	50	300	nA
	R_L = ∞ 0°C ≤T_A≤75°C	–	–	500	
DYNAMIC					
Open-Loop Voltage Gain, A_{OL}	T_A = 25°C	1000	2000	–	V/V
	0°C≤T_A≤75°C	800	–	–	
Input Resistance, R_I		0.1	1	–	MΩ
Slew Rate, SR	C_L = 100 pF, R_L = 5 kΩ	–	0.6	–	V/μs
Unity Gain Gandwidth, BW		–	5	–	MHz
Phase Margin, ϕ		–	70	–	Degrees
Power Supply Rejection	f = 100 Hz	–	55	–	dB
Channel Separation, e_{01}/e_{02}	f = 1 kHz	–	65	–	dB

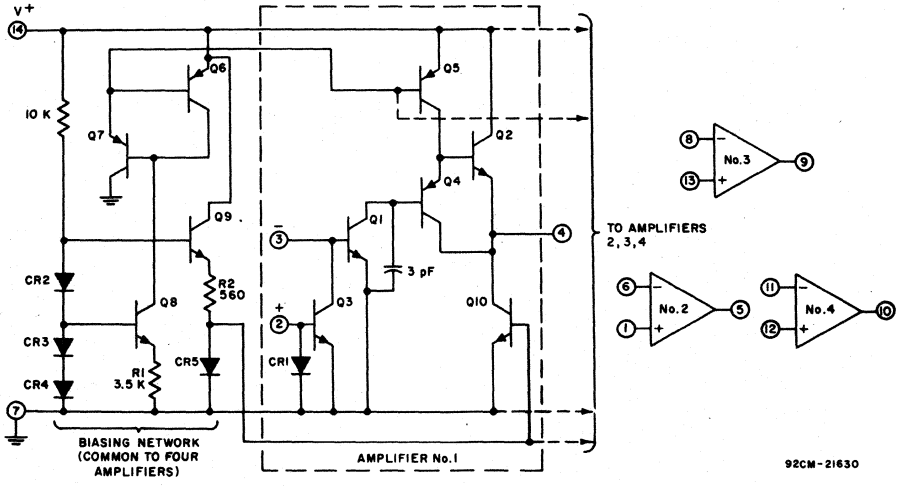


Fig.2 – Schematic diagram of CA3401.

CA3401E

TEST CIRCUITS

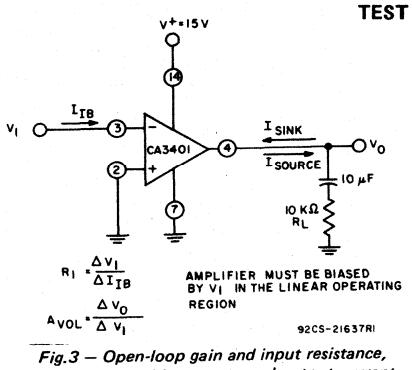


Fig.3 – Open-loop gain and input resistance, input bias current and output current test circuit.

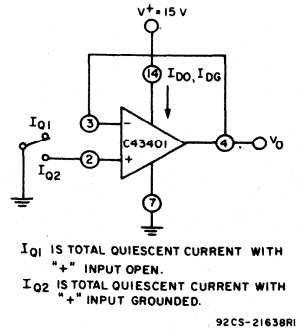


Fig.4 – Quiescent power supply current test circuit.

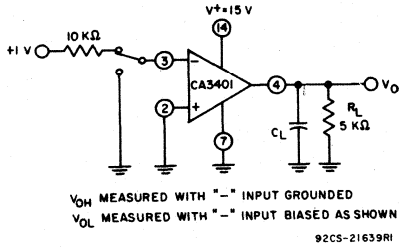


Fig.5 – Output voltage swing test circuit.

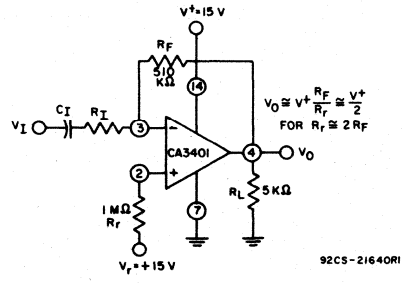


Fig.6 – Peak-to-peak output voltage test circuit.

TYPICAL CHARACTERISTIC CURVES

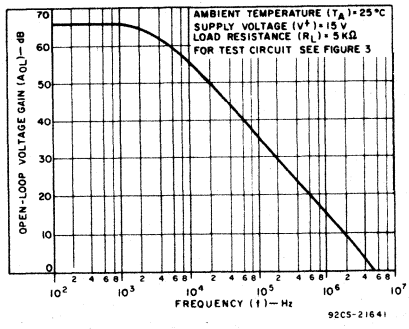


Fig.7 – Open-loop voltage gain vs. frequency.

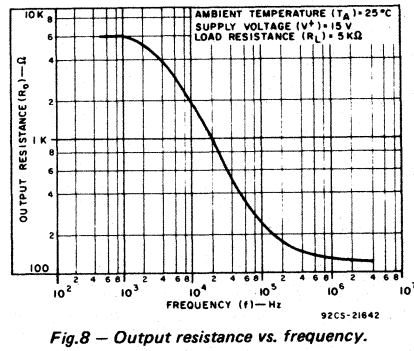


Fig.8 – Output resistance vs. frequency.

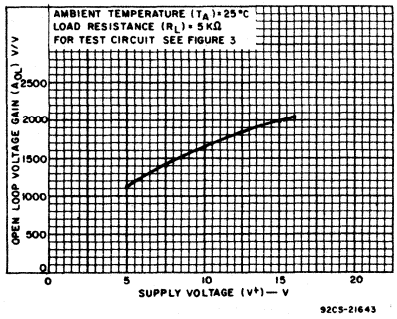


Fig.9 – Open-loop voltage gain vs. supply voltage.

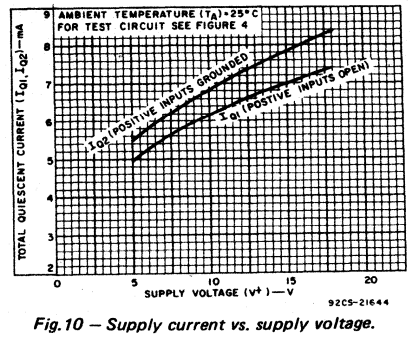


Fig.10 – Supply current vs. supply voltage.

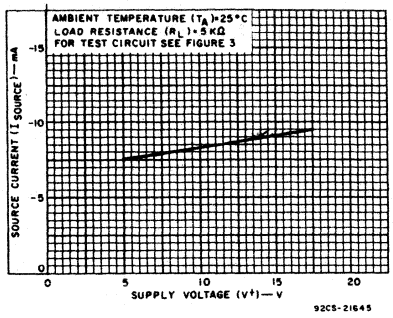


Fig. 11 – Source current vs. supply voltage.

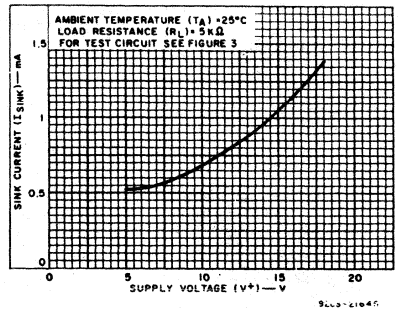
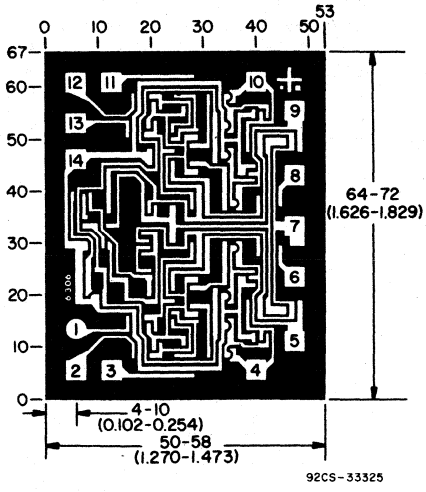


Fig. 12 – Sink current vs. supply voltage.

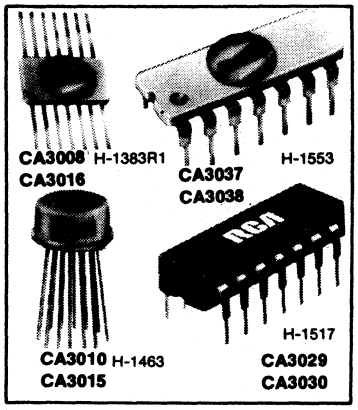


Dimensions and pad layout for CA3401H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038



Operational Amplifiers

Features:

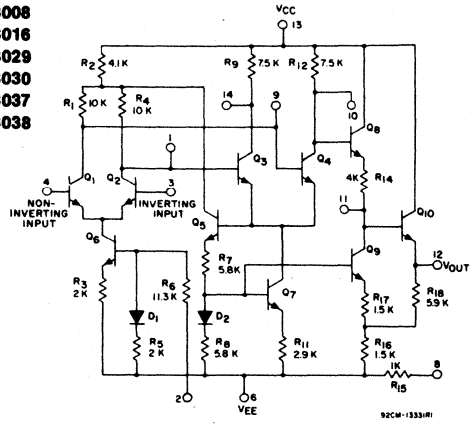
- *All types are electrically identical within their voltage groups*
- *For use in telemetry, data-processing, instrumentation, and communication equipment*
- *Built-in temperature stability from −55°C to +125°C for flat pack, TO-5 style, and ceramic dual-in-line packages; 0°C to +70°C for plastic dual-in-line packages*

6-Volt Types	12-Volt Types	Package
CA3008	CA3016	14-Lead Flat Pack
CA3010	CA3015	12-Lead TO-5 Style
CA3029	CA3030	14-Lead Plastic Dual-In-Line (TO-116)
CA3037	CA3038	14-Lead Ceramic Dual-In-Line (TO-116)

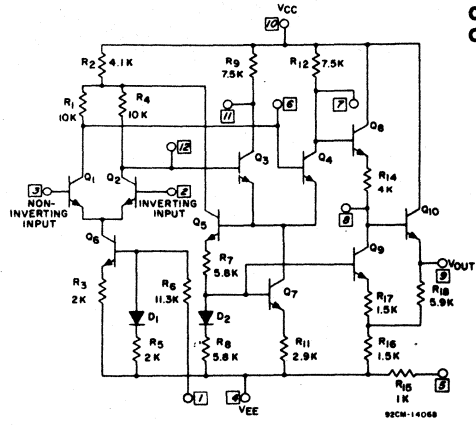
Applications:

- *Narrow-band and band-pass amplifier*
- *Operational functions*
- *Feedback amplifier*
- *DC and video amplifier*
- *Multivibrator*
- *Oscillator*
- *Comparator*
- *Servo driver*
- *Scaling adder*
- *Balanced modulator-driver*

CA3008
CA3016
CA3029
CA3030
CA3037
CA3038



CA3010
CA3015



Schematic diagrams.

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010	CA3008 CA3029 CA3037	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010	CA3008 CA3029 CA3037	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 (CA3008, CA3029, CA3037) 4 & 9 (CA3010)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.6, CA3008, CA3029, CA3037 No.4, CA3010 (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015	CA3016 CA3030 CA3038	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015	CA3016 CA3030 CA3038	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 (CA3016, CA3030, CA3038) 4 & 9 (CA3015)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.6, CA3016, CA3030, CA3038 No.4, CA3015 (Substrate) DO NOT GROUND				

	CA3008 CA3016 CA3037 CA3010 CA3015 CA3038	CA3029 CA3030
OPERATING TEMPERATURE RANGE	-55°C to +125°C	0°C to +70°C
STORAGE TEMPERATURE RANGE	-65°C to +200°C	-25°C to +85°C

	CA3016 CA3030 CA3015 CA3038	CA3008 CA3029 CA3010 CA3037
MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V	-4 V to +1 V
MAXIMUM DEVICE DISSIPATION	600 mW	300 mW

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 (CA3008, CA3016, CA3029, CA3030, CA3037, CA3038) Terminal No.5 (CA3010, CA3015) Not Connected Unless Otherwise Specified	Test Circuit	CA3008 CA3010 CA3029 CA3037			CA3016 CA3015 CA3030 CA3038			Units	Typical Characteristic Curves
			Fig.	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	1.08 -	5 -	- -	- 1.37	- 5	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.54 -	5 -	- -	- 1.07	- 5	μA	2
Input Bias Current	I_I	= +6V = -6V = +12V = -12V	5	- -	5.3 -	12 -	- -	- 9.6	- 24	μA	3
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_T	= +6 V = -6 V = +12V = -12V	4	- -	30 -	- -	- -	- 175	- -	mW	none
		[5] shorted to [9] V_{CC} = +6V, V_{EE} = -6V		-	102	-	-	-	-		
		8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	500	-		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Common-Mode Rejection Ratio	CMR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	4 -	6.75 -	- -	- 12	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	10 -	14 -	- -	- 5	- 7.8	- -	kΩ	13
Output Impedance	Z_{OUT}	= +6V = -6V = +12V = -12V	15	- -	200 -	- -	- -	- 92	- -	Ω	16
Common-Mode Input-Voltage Range	V_{CMR}	= +6V = -6V = +12V = -12V	11	- -	+0.5 -4 -	- -	- -	- +0.65 -8	- -	V	none

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038; Italic Numbers in Square Boxes are for CA3010, CA3015

INPUT OFFSET VOLTAGE AND CURRENT

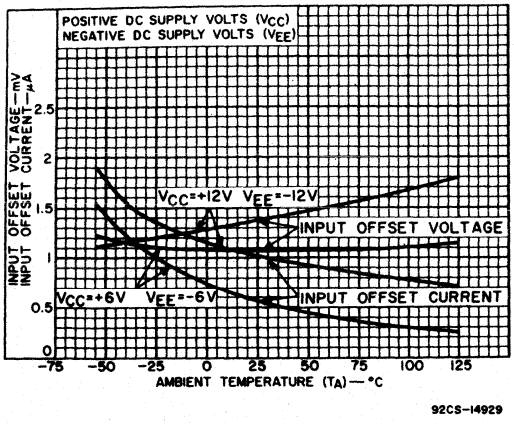


Fig.2

INPUT BIAS CURRENT

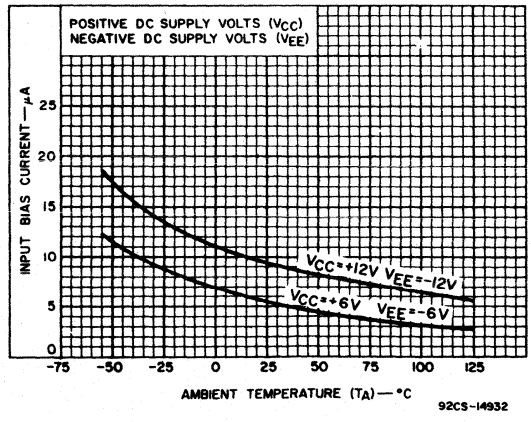


Fig.3

INPUT OFFSET VOLTAGE, INPUT OFFSET VOLTAGE SENSITIVITY, AND DEVICE DISSIPATION TEST CIRCUIT

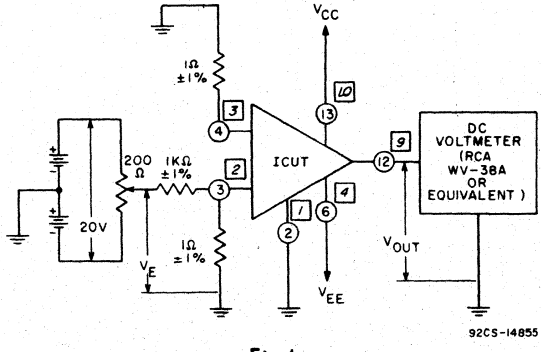


Fig.4

INPUT OFFSET CURRENT AND INPUT BIAS CURRENT TEST CIRCUIT

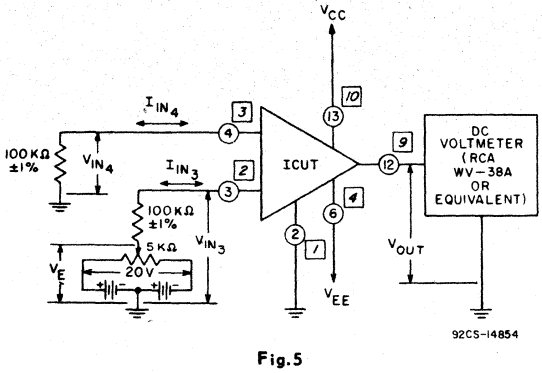


Fig.5

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the diference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\ (\text{Step 2}) - V_{OUT}\ (\text{Step 3})}{2\ \text{volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$

I_C = Direct Current into Terminal (13) or [10]

I_E = Direct Current out of Terminal (6) or [4]

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN_4}.
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN_4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038; Italic Numbers in Square Boxes are for CA3010, CA3015

OPEN-LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3008, CA3010, CA3015, CA3016, CA3037, CA3038

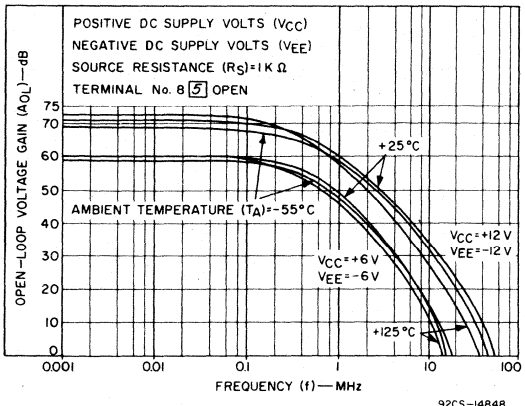


Fig.6

OPEN-LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3029 AND CA3030

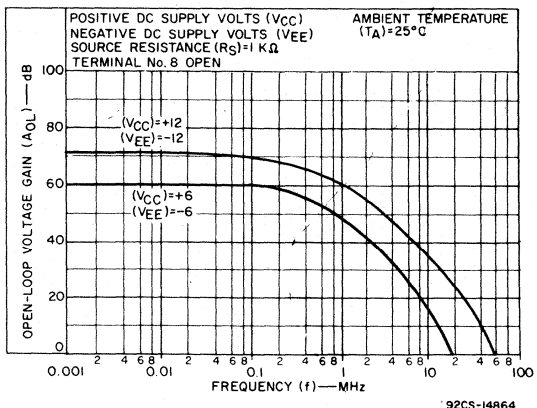
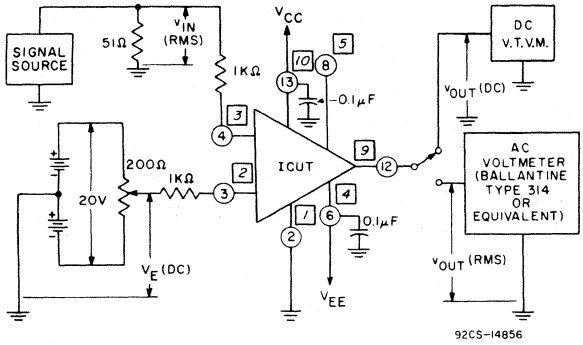


Fig.7

OPEN-LOOP DIFFERENTIAL VOLTAGE GAIN, MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE, AND OPEN-LOOP BANDWIDTH AT -3 dB POINT TEST CIRCUIT



Procedure:

1. Adjust V_E for V_{OUT} = ±0.1 V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at f = 1 kHz.

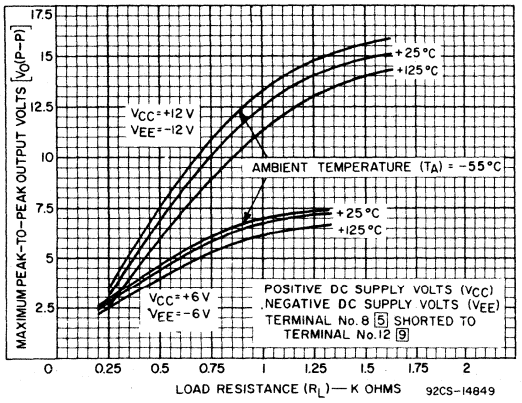
$$A_{OL} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

3. Measure Maximum Peak-to-Peak Output Voltage at f = 1 kHz.
4. Measure Open-Loop Bandwidth at -3 dB Point.

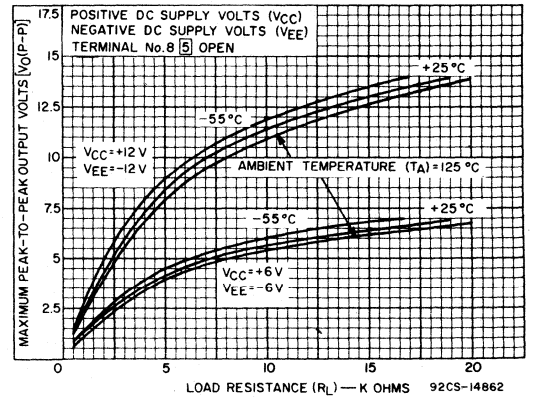
Reference Level = A_{OL} at 1 kHz.

Fig.8

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3008, CA3010, CA3015, CA3016, CA3037, CA3038



(a)



(b)

Fig.9

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038; Italic Numbers in Square Boxes are for CA3010, CA3015

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3029 AND CA3030

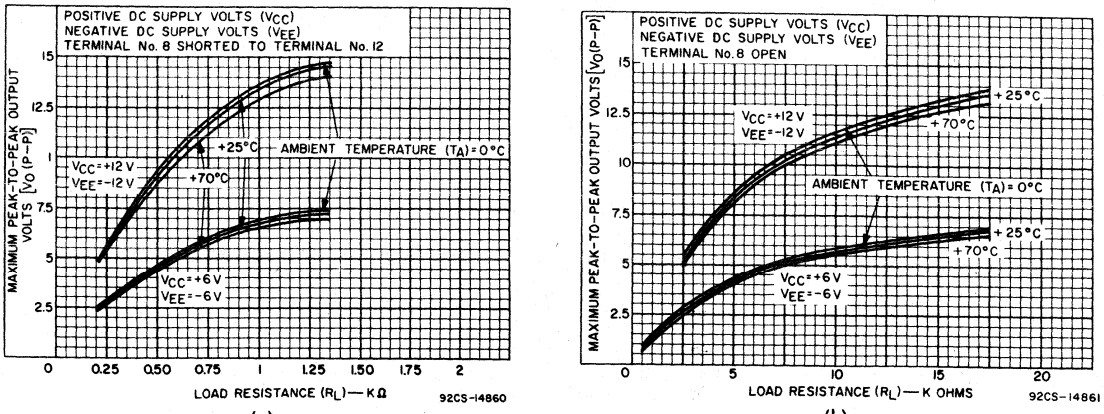
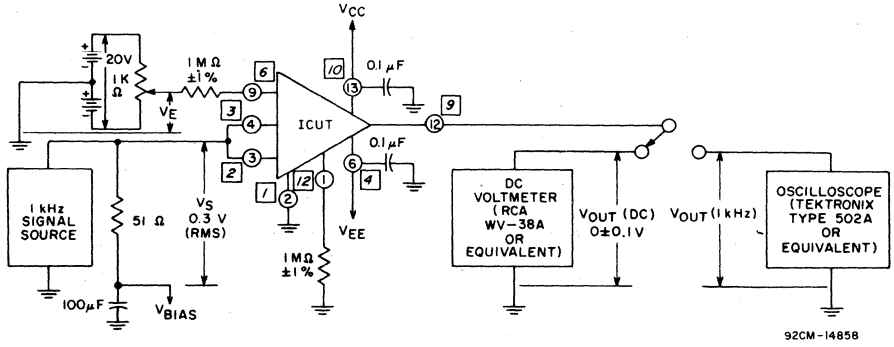


Fig.10

COMMON-MODE REJECTION RATIO AND COMMON-MODE INPUT-VOLTAGE-RANGE TEST CIRCUIT



Procedures:

Common-Mode Rejection Ratio:

1. Set V_{BIAS} = 0. Adjust V_E for V_{OUT}(DC) = 0 ± 0.1 V.
2. Apply 1-kHz sinusodial input signal and adjust for V_S = 0.3 V (RMS).
3. Measure and record the RMS value of V_{OUT}. An oscilloscope is used for this measurement so that the output signal may be visually separated.from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT}/V_S$$

$$A_{CM} \text{ in dB} = -20 \log_{10} V_S/V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$CMR \text{ in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB}.$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

Fig.11

COMMON-MODE REJECTION RATIO vs. FREQUENCY

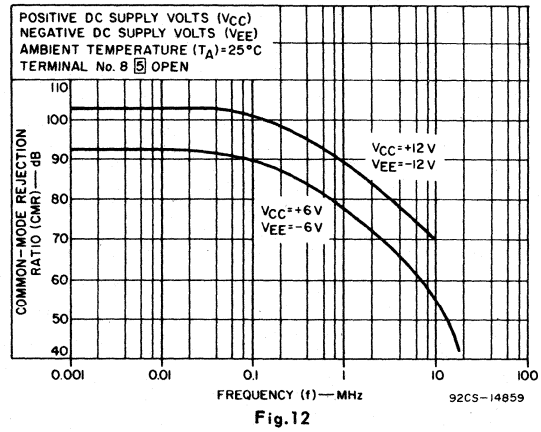


Fig.12

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038; Italic Numbers in Square Boxes are for CA3010, CA3015

SINGLE-ENDED INPUT IMPEDANCE vs. TEMPERATURE

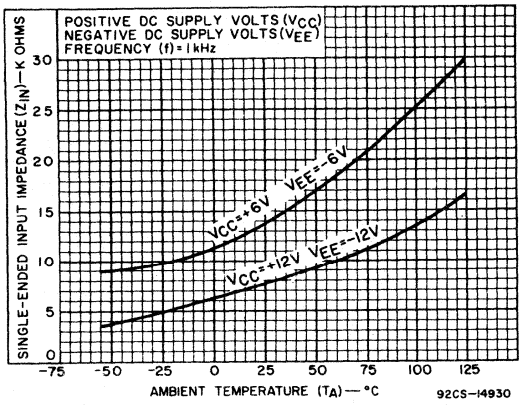


Fig.13

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

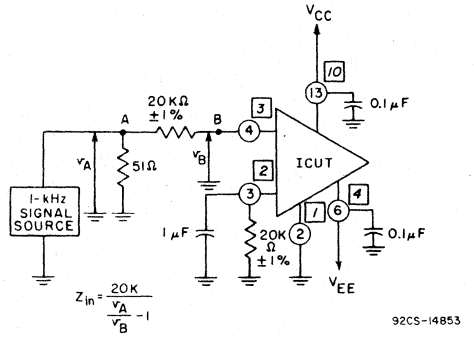


Fig.14

OUTPUT IMPEDANCE TEST CIRCUIT

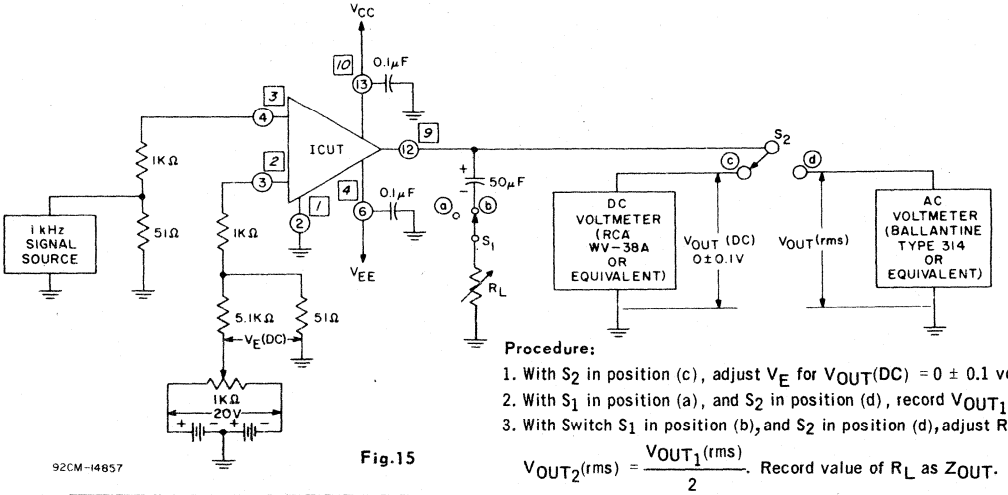
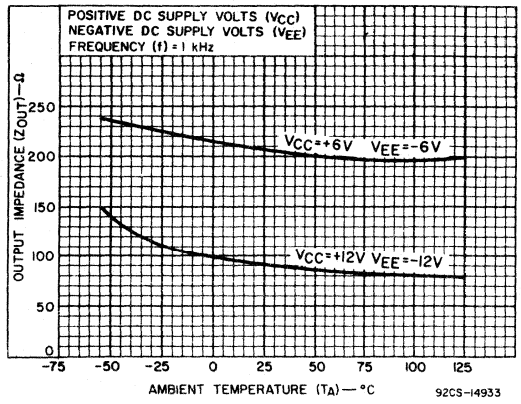


Fig.15

Procedure:

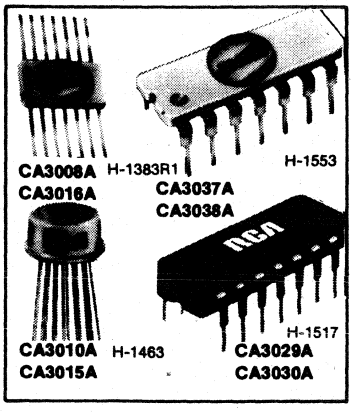
1. With S_2 in position (c), adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ volt.
2. With S_1 in position (a), and S_2 in position (d), record $V_{OUT_1}(rms)$.
3. With Switch S_1 in position (b), and S_2 in position (d), adjust R_L until $V_{OUT_2}(rms) = \frac{V_{OUT_1}(rms)}{2}$. Record value of R_L as Z_{OUT}.



OUTPUT IMPEDANCE vs. TEMPERATURE

Fig.16

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A



Operational Amplifiers

Features:

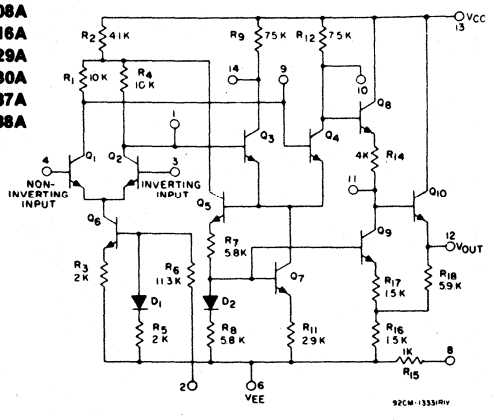
- *These new types have all the desirable features and characteristics of their prototypes plus lower noise figures and improved input characteristics for offset voltage, offset current, bias current, and impedance*
- *All types are electrically identical within their voltage groups*
- *For use in telemetry, data-processing, instrumentation, and communication equipment*
- *Built-in temperature stability from −55°C to +125°C for flat pack, TO-5 style, and ceramic dual-in-line packages; 0°C to +70°C for plastic dual-in-line packages*

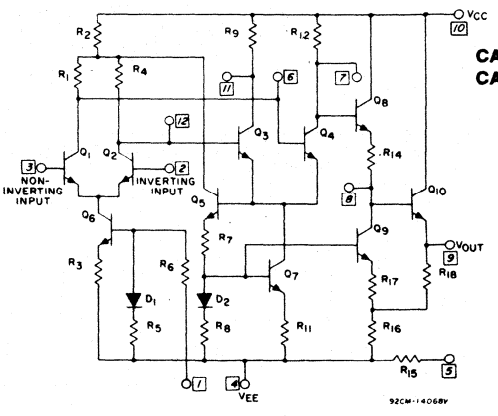
6-Volt Types	12-Volt Types	Package
CA3008A	CA3016A	14-Lead Flat Pack
CA3010A	CA3015A	12-Lead TO-5 Style
CA3029A	CA3030A	14-Lead Plastic Dual-In-Line (TO-116)
CA3037A	CA3038A	14-Lead Ceramic Dual-In-Line (TO-116)

Applications:

- *Narrow-band and band-pass amplifier*
- *Operational functions*
- *Feedback amplifier*
- *DC and video amplifier*
- *Multivibrator*
- *Oscillator*
- *Comparator*
- *Servo driver*
- *Scaling adder*
- *Balanced modulator-driver*

CA3008A
CA3016A
CA3029A
CA3030A
CA3037A
CA3038A





Schematic diagrams.

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010A	CA3008A CA3029A CA3037A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010A	CA3008A CA3029A CA3037A	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
-	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 (CA3008A, CA3029A, CA3037A) 4 & 9 (CA3010A)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.6, CA3008A, CA3029A, CA3037A No.4, CA3010A (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015A	CA3016A CA3030A CA3038A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015A	CA3016A CA3030A CA3038A	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
-	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 (CA3016A, CA3030A, CA3038A) 4 & 9 (CA3015A)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.6, CA3016A, CA3030A, CA3038A No.4, CA3015A (Substrate) DO NOT GROUND				

	CA3008A CA3010A CA3016A CA3015A CA3037A CA3038A	CA3029A CA3030A
OPERATING TEMPERATURE RANGE	-55°C to +125°C	0°C to +70°C
STORAGE TEMPERATURE RANGE	-65°C to +200°C	-25°C to +85°C

	CA3016A CA3015A CA3030A CA3038A	CA3008A CA3029A
MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V	-4 V to +1 V
MAXIMUM DEVICE DISSIPATION	600 mW	300 mW

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 (CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A), Terminal No.5 (CA3010A, CA3015A) Not Connected Unless Otherwise Specified	Test Circuit Fig.	CA3008A CA3010A CA3029A CA3037A Min.	Typ.	Max.	CA3016A CA3015A CA3030A CA3038A Min.	Typ.	Max.	Units	Typical Characteristic Curves Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	0.9 -	2 -	- -	- 1	- 2	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.3 -	1.5 -	- -	- 0.5	- 1.6	μA	2
Input Bias Current	I_I	= +6V = -6V = +12V = -12V	5	- -	2.5 -	4 -	- -	- 4.7	- 6	μA	3
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_T	= +6 V = -6 V = +12V = -12V	4	- -	40 -	- -	- -	- 175	- -	mW	none
		[5] shorted to [9] V_{CC} = +6V, V_{EE} = -6V		-	102	-	-	-	-		
		8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	500	-		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Slew Rate	SR	V_{CC} = +6V V_{EE} = -6V R_S = 1 kΩ = +12V = -12V	none	- -	3 -	- -	- -	- 7	- -	V/μs	none
Common-Mode Rejection Ratio	CMR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	- -	6.75 -	- -	- -	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	15 -	20 -	- -	- 7.5	- 10	- -	kΩ	13
Output Impedance	Z_{OUT}	= 6V = -6V = +12V = -12V	15	- -	160 -	- -	- -	- 85	- -	Ω	16
Common-Mode Input-Voltage Range	V_{CMR}	= +6V = -6V = +12V = -12V	11	- -	+0.5 -4 -	- -	- -	- +0.65 -8	- -	V	none
Noise Figure	NF	V_{CC} = +3V, V_{EE} = -3V R_S = 1 kΩ = +6V = -6V = +9V = -9V = +12V = -12V	18	- - - -	6.3 8.3 - -	9 12 - -	- - - -	6.3 8.3 10 11	9 12 14 16	dB	17

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A; Italic Numbers in Square Boxes are for CA3010A, CA3015A

INPUT OFFSET VOLTAGE AND CURRENT

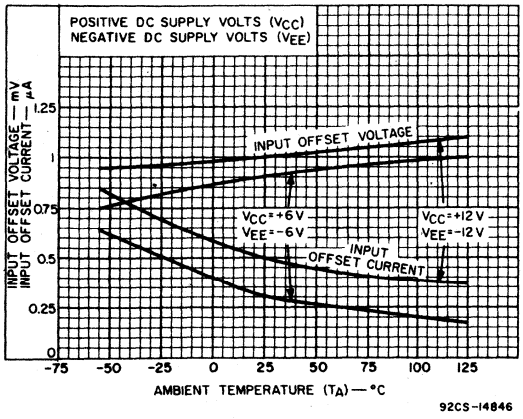


Fig.2

INPUT BIAS CURRENT

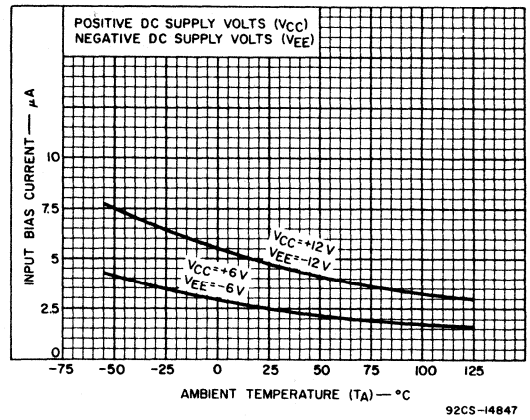


Fig.3

INPUT OFFSET VOLTAGE, INPUT OFFSET VOLTAGE SENSITIVITY, AND DEVICE DISSIPATION TEST CIRCUIT

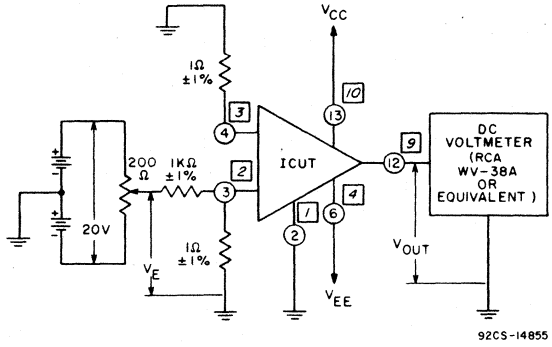


Fig.4

INPUT OFFSET CURRENT AND INPUT BIAS CURRENT TEST CIRCUIT

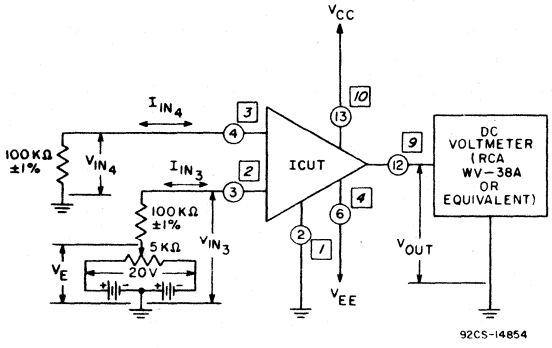


Fig.5

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the diference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\ (\text{Step 2}) - V_{OUT}\ (\text{Step 3})}{2\ \text{volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$

I_C = Direct Current into Terminal 13 or *10*

I_E = Direct Current out of Terminal 6 or *4*

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN4}
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A; Italic Numbers in Square Boxes are for CA3010A, CA3015A

OPEN LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3008A, CA3010A, CA3015A, CA3016A, CA3037A, CA3038A

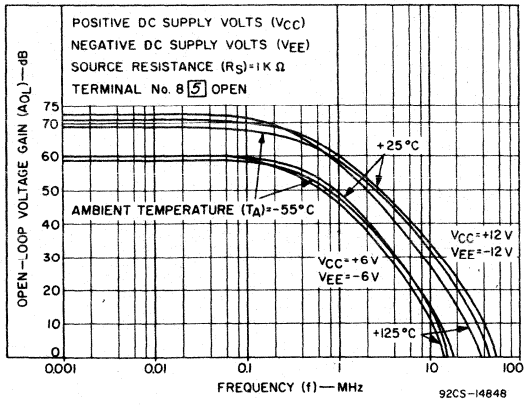


Fig.6

OPEN LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3029A AND CA3030A.

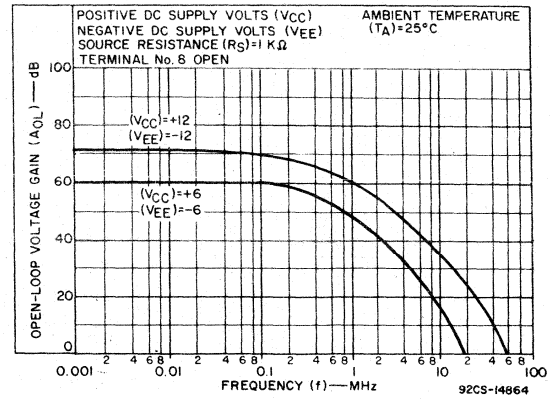
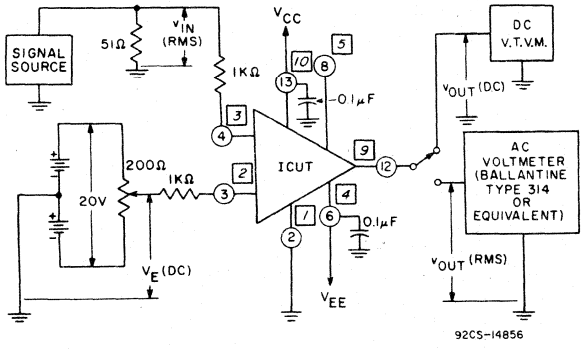


Fig.7

OPEN-LOOP DIFFERENTIAL VOLTAGE GAIN, MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE, AND OPEN-LOOP BANDWIDTH AT -3 POINT TEST CIRCUIT



Procedure:

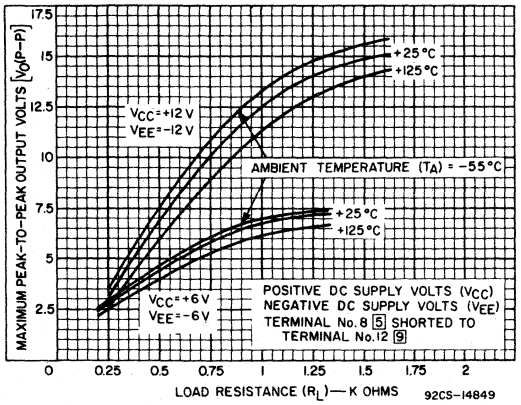
1. Adjust V_E for V_{OUT} = ±0.1 V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at f = 1 kHz

$$A_{OL} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

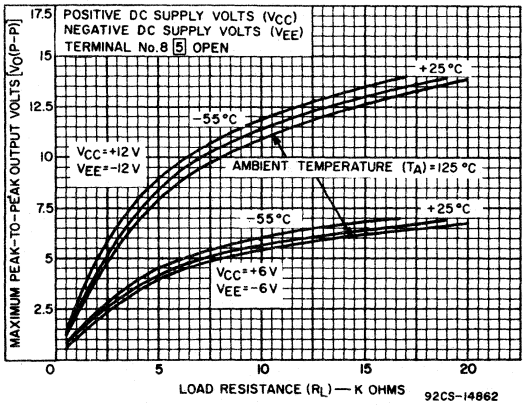
3. Measure Maximum Peak-to-Peak Output Voltage at f = 1 kHz
4. Measure Open-Loop Bandwidth at -3 dB Point
   Reference Level = A_{OL} at 1 kHz

Fig.8

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3008A, CA3010A, CA3015A, CA3016A, CA3037A, CA3038A



(a)



(b)

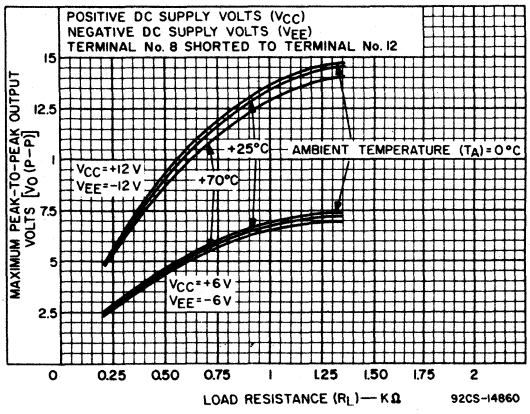
Fig.9

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

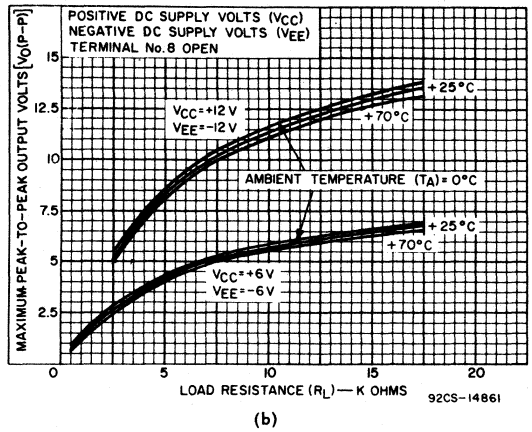
TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A; Italic Numbers in Square Boxes are for CA3010A, CA3015A

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3029A AND CA3030A



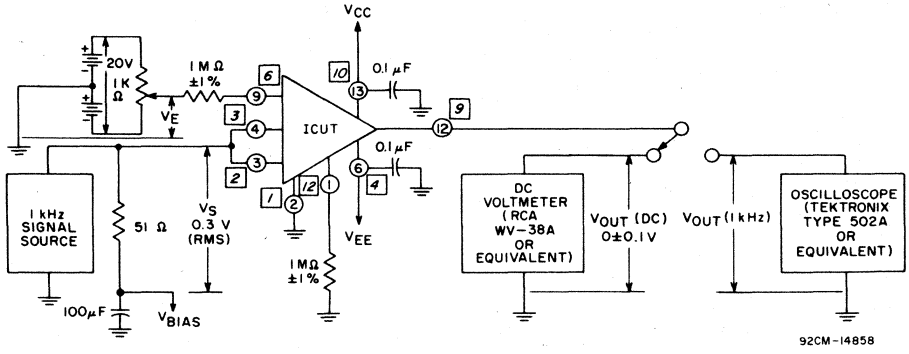
(a)



(b)

Fig.10

COMMON-MODE REJECTION RATIO AND COMMON-MODE INPUT-VOLTAGE-RANGE TEST CIRCUIT



Procedures:

Common-Mode Rejection Ratio:

1. Set V_{BIAS} = 0. Adjust V_E for V_{OUT}(DC) = 0 ± 0.1 V.
2. Apply 1-kHz sinusodial input signal and adjust for V_S = 0.3 V (RMS).
3. Measure and record the RMS value of V_{OUT}. An oscilloscope is used for this measurement so that the output signal may be visually separated.from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT}/V_S$$

$$A_{CM} \text{ in dB} = -20 \log_{10} V_S/V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$CMR \text{ in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB}.$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

Fig.11

COMMON-MODE REJECTION RATIO vs. FREQUENCY

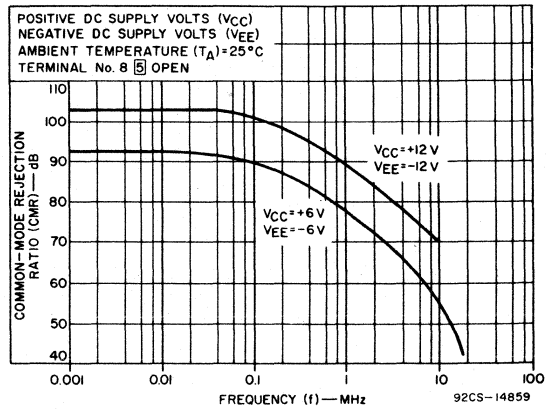


Fig.12

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A; Italic Numbers in Square Boxes are for CA3010A, CA3015A

SINGLE-ENDED INPUT IMPEDANCE vs. TEMPERATURE

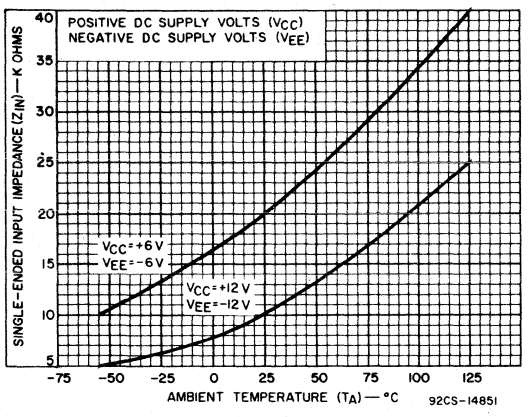


Fig.13

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

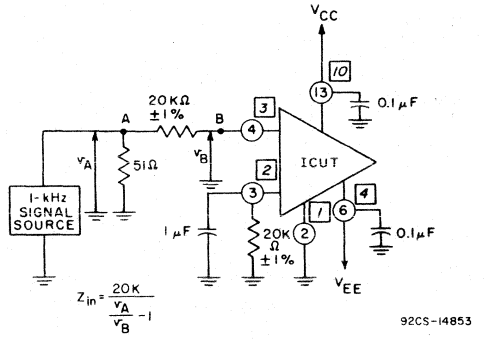


Fig.14

OUTPUT IMPEDANCE TEST CIRCUIT

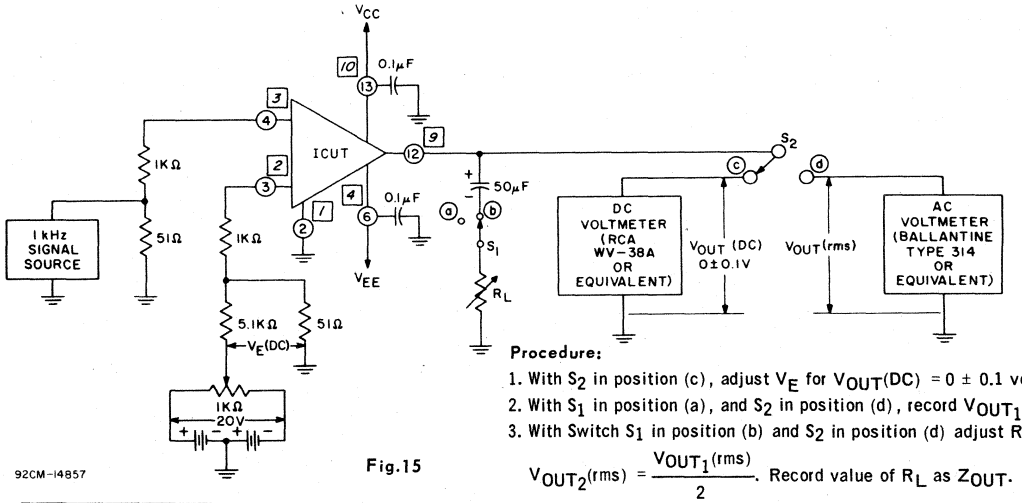
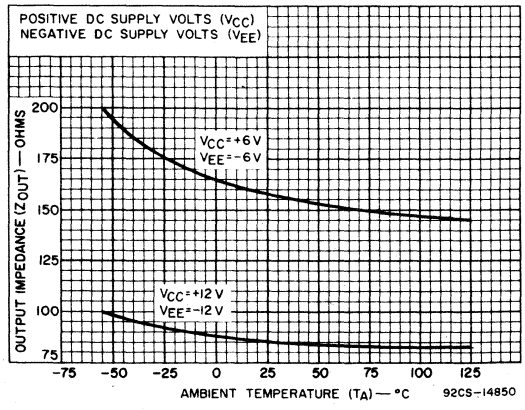


Fig.15

Procedure:

1. With S_2 in position (c), adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ volt.
2. With S_1 in position (a), and S_2 in position (d), record $V_{OUT_1}(rms)$.
3. With Switch S_1 in position (b) and S_2 in position (d) adjust R_L until $V_{OUT_2}(rms) = \frac{V_{OUT_1}(rms)}{2}$. Record value of R_L as Z_{OUT}.



OUTPUT IMPEDANCE vs. TEMPERATURE

Fig.16

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

NOISE FIGURE vs. FREQUENCY

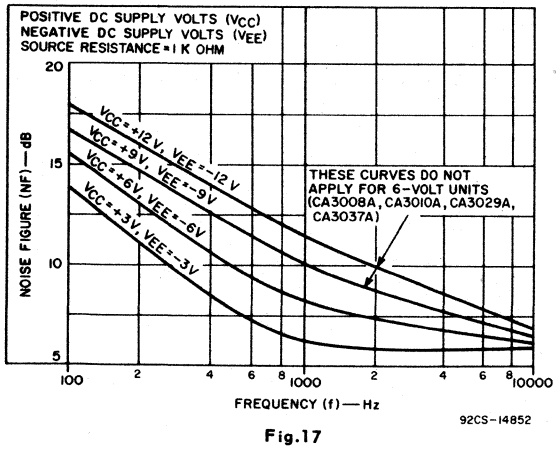


Fig.17

NOISE FIGURE TEST CIRCUIT

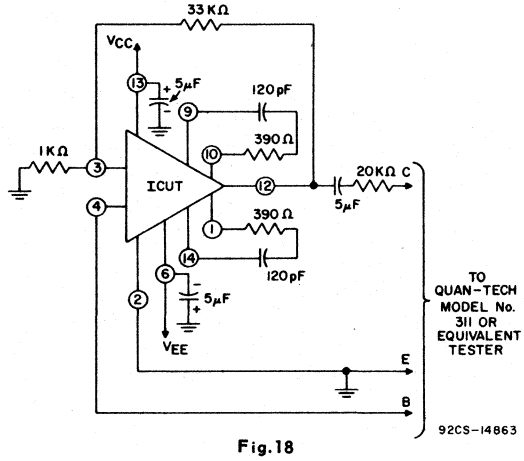


Fig.18

12-Lead TO-5

H-1463

Low-Power Wideband Amplifiers

Features:

- *Lower DC Power Drain:*
  P_T { *CA3021 = 4 mW typ.*; *CA3022 = 12.5 mW typ.*; *CA3023 = 35 mW tp.* } *at V_{CC} = 6 V*
- *Excellent frequency response:*
  -3dB BW { *CA3021 = 2.4 MHz typ.*; *CA3022 = 7.5 MHz typ.*; *CA3023 = 16 MHz typ.* }
- *High Voltage Gain:*
  A { *CA3021 = 56 dB typ. at 0.5 MHz*; *CA3022 = 57 dB typ. at 2.5 MHz*; *CA3023 = 53 dB typ. at 5 MHz* }
- *Wide AGC Range: 33 dB typ.*
- *Only one power supply (4.5 to 12 V) required*
- *Hermetically sealed 12-lead TO-5-style package*
- *Operation from −55° C to +125° C*

Applications:

- *Gain-controlled linear amplifiers*
- *AM/FM IF amplifiers*
- *Video amplifiers*
- *Limiters*

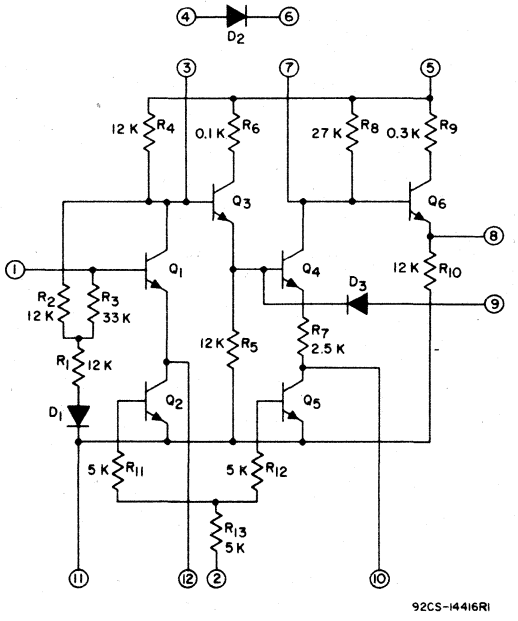


Fig. 1 - Schematic diagram for CA3021, CA3022, and CA3023.

CA3021, CA3022, CA3023

ABSOLUTE-MAXIMUM RATINGS:

OPERATING-TEMPERATURE RANGE	-55°C to +125°C	
STORAGE-TEMPERATURE RANGE	-65°C to +150°C	
LEAD TEMPERATURE (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C	
DEVICE DISSIPATION, P_T	120 max.	mW
INPUT-SIGNAL VOLTAGE	-3, +3 max.	V
DC VOLTAGES AND CURRENTS	See Table Below	

	VOLTAGE OR CURRENT LIMITS		CIRCUIT CONDITIONS	
TERMINAL	NEGATIVE	POSITIVE	TERMINAL	CONDITIONS
1	-3V	+3V	1	Connected to Voltage Source through 100Ω Resistor
			5	+12V
			10, 11, 12	Ground
2	-3V	+12V	5	+12V
			10, 11, 12	Ground
3	0V	+12V	5	+12V
			10, 11, 12	Ground
4	-12V	+12V	6, 11	Ground
	10 max. mA			
5	0V	+18V	10, 11, 12	Ground
6	-12V	+12V	5, 11	Ground
	10 max. mA			

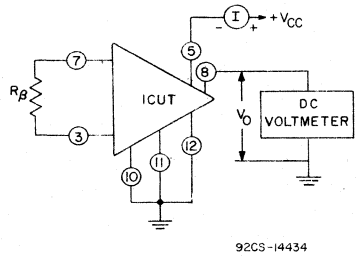
	VOLTAGE OR CURRENT LIMITS		CIRCUIT CONDITIONS	
TERMINAL	NEGATIVE	POSITIVE	TERMINAL	CONDITIONS
7	0V	+12V	5	+12V
			10, 11, 12	Ground
8	20 max. mA		5	+12V
			10, 11, 12	Ground
9	-0.5V	+3V	5	+12V
			10, 11, 12	Ground
10	0V	+4V	2,5	+12V
			11	Ground
11	-6V	+12V	2	Ground
			5	+12V
12	0V	+4V	2,5	+12V
			11	Ground

ELECTRICAL CHARACTERISTICS, at $T_A = 25^oC$, $V_{CC} = +6V$, unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS										
		TEST SETUP AND PROCEDURE	FEEDBACK RESISTANCE (R_β) BETWEEN TERMINALS 3 AND 7	FREQUENCY f	CA3021 (TA5219)			CA3022 (TA5236)			CA3023 (TA5218)			UNITS	TYPICAL CHARACTERISTIC CURVE
		Fig.	Ω	MHz	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units	Fig.
Device Dissipation	P_T	2	∞	-	1	4	8	–	–	–	–	–	–	mW	3a,d
			∞	–	–	–	–	5	12.5	24	–	–	–	mW	3b,d
			∞	–	–	–	–	–	–	–	24	35	48	mW	3c,d
Quiescent Output Voltage	V_O	2	39k	–	–	2.2	–	–	–	–	–	–	–	V	–
			10k	–	–	–	–	–	1.9	–	–	–	–	V	
			4.7k	–	–	–	–	–	–	–	–	1.3	–	V	
AGC Source Current	I_{AGC}	4	V_{AGC} =+6V		–	0.8	–	–	0.8	–	–	0.8	–	mA	–
Voltage Gain	A	5	560k	0.5	50	56	–	–	–	–	–	–	–	dB	6a
			39k	0.8	40	46	–	–	–	–	–	–	–	dB	6a,d
			39k	2.5	–	–	–	50	57	–	–	–	–	dB	6b
			10k	3	–	–	–	40	44	–	–	–	–	dB	6b,d
			18k	5	–	–	–	–	–	–	50	53	–	dB	6c
			4.7k	10	–	–	–	–	–	–	40	44	–	dB	6c,d
Bandwidth at -3 dB Point	BW	5	39k	–	0.8	2.4	–	–	–	–	–	–	–	MHz	6a
			10k	–	–	–	–	3	7.5	–	–	–	–	MHz	6b
			4.7k	–	–	–	–	–	–	–	10	16	–	MHz	6c
Input-Impedance Components: Input Resistance	R_{IN}	7	39k	1	–	4000	–	–	–	–	–	–	–	Ω	–
			10k	5	–	–	–	–	1300	–	–	–	–	Ω	
			4.7k	10	–	–	–	–	–	–	–	300	–	Ω	
Input-Impedance Components: Input Capacitance	C_{IN}	7	39k	1	–	11	–	–	–	–	–	–	–	pF	–
			10k	5	–	–	–	–	18	–	–	–	–	pF	
			4.7k	10	–	–	–	–	–	–	–	13	–	pF	
Output Resistance	R_{OUT}	8	39k	1	–	300	–	–	–	–	–	–	–	Ω	–
			10k	5	–	–	–	–	120	–	–	–	–	Ω	
			4.7k	10	–	–	–	–	–	–	–	100	–	Ω	
Noise Figure	NF	9	39k	1	–	4.2	8.5	–	–	–	–	–	–	dB	–
			10k	1	–	–	–	–	4.4	8.5	–	–	–	dB	
			4.7k	1	–	–	–	–	–	–	–	6.5	8.5	dB	
AGC Range	AGC	10	–	1	–	33	–	–	–	–	–	–	–	dB	–
			–	5	–	–	–	–	33	–	–	–	–	dB	
			–	10	–	–	–	–	–	–	–	33	–	dB	
Maximum Output Voltage (RMS Value)	v_{out}	5	39k	1	–	0.6	–	–	–	–	–	–	–	V(rms)	–
			10k	5	–	–	–	–	0.7	–	–	–	–	V(rms)	
			4.7k	10	–	–	–	–	–	–	–	0.5	–	V(rms)	

CA3021, CA3022, CA3023

TEST SETUP FOR MEASUREMENT OF DEVICE DISSIPATION AND QUIESCENT OUTPUT VOLTAGE



$P_T = V_{CC}(I)$

Fig.2

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3022

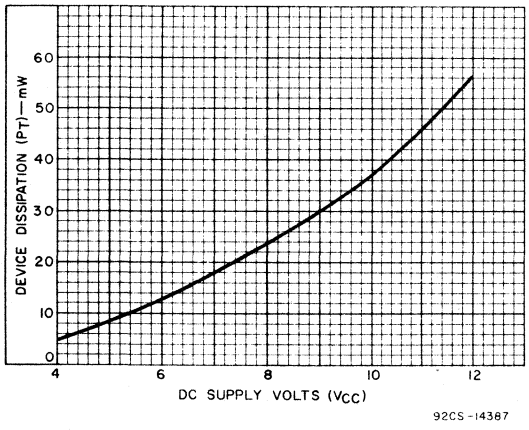


Fig.3(b)

DEVICE DISSIPATION VS TEMPERATURE FOR CA3021, CA3022, AND CA3023

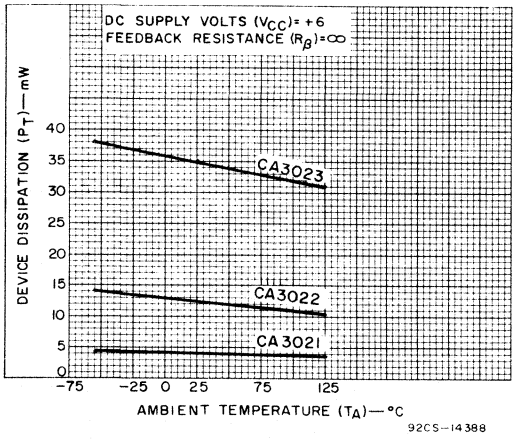


Fig.3(d)

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3021

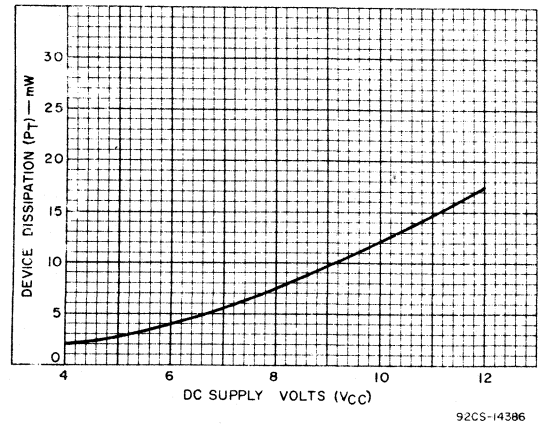


Fig.3(a)

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3023

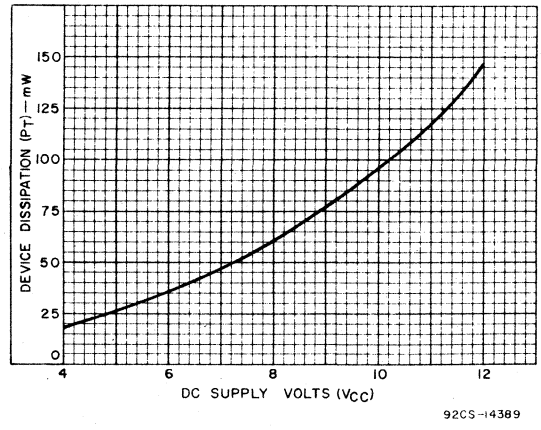
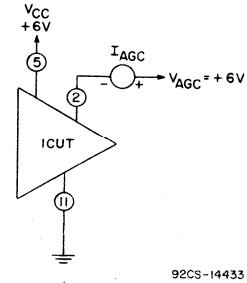


Fig.3(c)

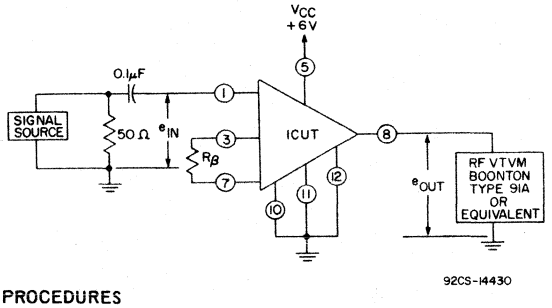
TEST SETUP FOR MEASUREMENT OF AGC SOURCE CURRENT



I_{AGC} IS THE CURRENT FLOWING INTO TERMINAL 2.

Fig.4

TEST SETUP FOR MEASUREMENTS OF VOLTAGE-GAIN, -3dB BANDWIDTH, AND MAXIMUM OUTPUT VOLTAGE



PROCEDURES

Voltage Gain:

(a) Set e_{in} = 0.5 mVat frequency specified, read e_{out} Voltage Gain

(A) = $20 \log_{10} \frac{e_{out}}{e_{in}}$

Bandwidth:

(a) Set e_{out} to a convenient reference voltage at f = 100 kHz and record corresponding value of e_{in}.

(b) Increase the frequency, keeping e_{in} constant until e_{out} drops 3-dB. Record Bandwidth.

Fig.5

VOLTAGE GAIN VS FREQUENCY FOR CA3021

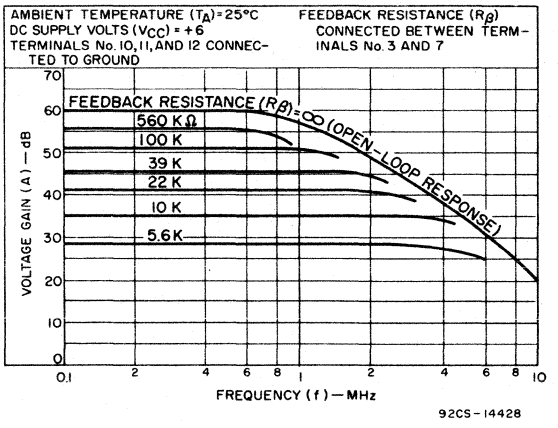


Fig.6(a)

VOLTAGE GAIN VS FREQUENCY FOR CA3022

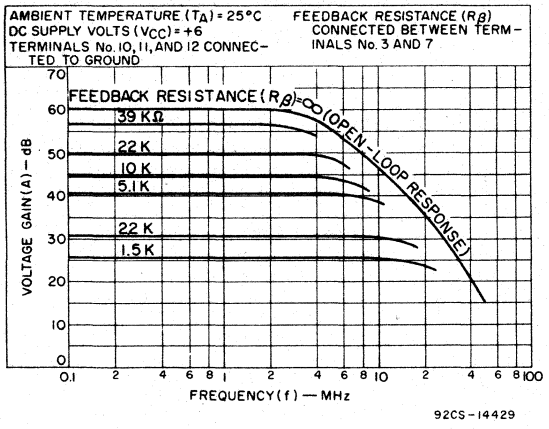


Fig.6(b)

VOLTAGE GAIN VS FREQUENCY FOR CA3023

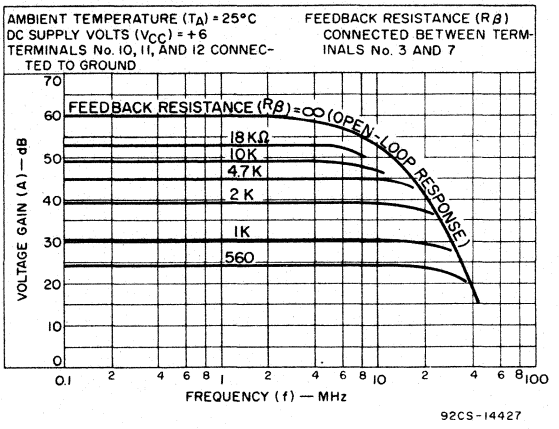


Fig.6(c)

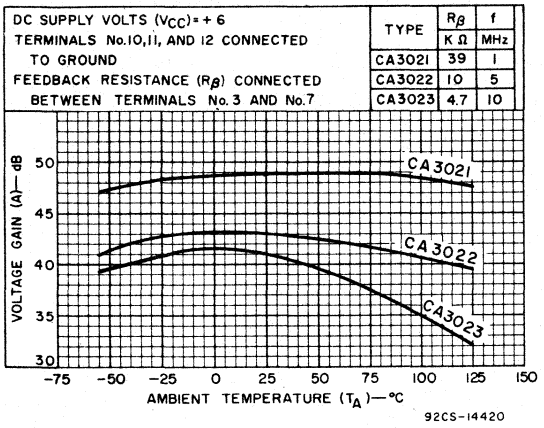
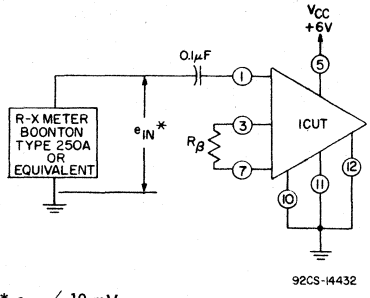


Fig.6(d)

VOLTAGE GAIN VS TEMPERATURE FOR CA3021, CA3022, AND CA3023

CA3021, CA3022, CA3023

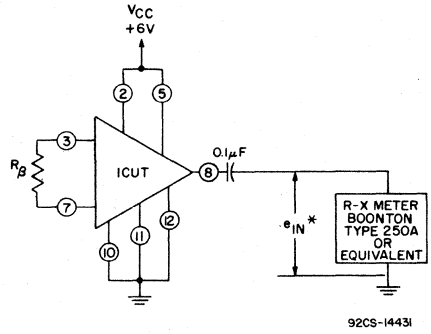
TEST SETUP FOR MEASUREMENT OF INPUT-IMPEDANCE COMPONENTS



* $e_{in} \leq 10$ mV

Fig.7

TEST SETUP FOR MEASUREMENT OF OUTPUT RESISTANCE

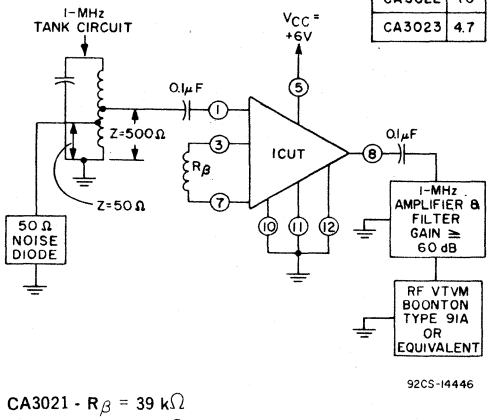


* $e_{in} \leq 10$ mV

Fig.8

TEST SETUP FOR MEASUREMENT OF NOISE FIGURE

ICUT	Rβ KΩ
CA3021	39
CA3022	10
CA3023	4.7

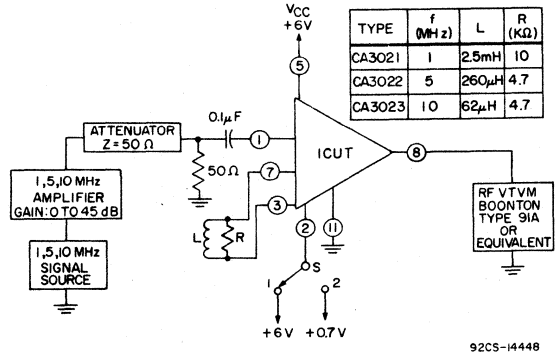


CA3021 - R_β = 39 kΩ
CA3022 - R_β = 10 kΩ
CA3023 - R_β = 4.7 kΩ

Fig.9

TEST SETUP FOR MEASUREMENT OF AGC RANGE

TYPE	f (MHz)	L	R (KΩ)
CA3021	1	2.5mH	10
CA3022	5	260μH	4.7
CA3023	10	62μH	4.7



$$\text{AGC RANGE} = 20 \log_{10} \frac{\text{A WITH S IN POSITION 1}}{\text{A WITH S IN POSITION 2}}$$

(A = VOLTAGE GAIN)

	f MHz
CA3021	1
CA3022	5
CA3023	10

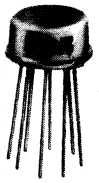
Fig. 10

CA3100 Types

Wideband Operational Amplifier

Mini-DIP
(E Suffix)
1-1817

8-Lead TO-5
With Dual-In-Line
Formed Leads
"DIL-CAN"
(S Suffix)
H-1787



8-Lead TO-5
(T Suffix)
H-1528

Features:

- *High open-loop gain at video frequencies - 42 dB typ. at 1 MHz*
- *High unity-gain crossover frequency (f_T) - 38 MHz typ.*
- *Wide power bandwidth - V_O = 18 Vp-p typ. at 1.2 MHz*
- *High slew rate - 70 V/μs [typ.] in 20 dB amplifier*
  25 V/μs [typ.] in unity-gain amplifier
- *Fast settling time - 0.6 μs typ.*
- *High output current - ±15 mA min.*
- *LM118, 748/LM101 pin compatibility*
- *Single capacitor compensation*
- *Offset null terminals*

Applications:

- *Video amplifiers*
- *Fast peak detectors*
- *Meter-driver amplifiers*
- *High-frequency feedback amplifiers*
- *Video pre-drivers*
- *Oscillators*
- *Multivibrators*
- *Voltage-controlled oscillator*
- *Fast comparators*

RCA-CA3100S, CA3100T is a large-signal wideband, high-speed operational amplifier which has a unity gain crossover frequency (f_T) of approximately 38 MHz and an open-loop, 3 dB corner frequency of approximately 110 kHz. It can operate at a total supply voltage of from 14 to 36 volts (±7 to ±18 volts when using split supplies) and can provide at least 18 Vp-p and 30 mA p-p at the output when operating from ±15 volt supplies. The CA3100 can be compensated with a single external capacitor and has dc offset adjust terminals for those applications requiring offset null. (See Fig. 15).

The CA3100 circuit contains both bipolar and P-MOS transistors on a single monolithic chip.

The CA3100 is supplied in either the standard 8-lead TO-5 package ("T" suffix), or in the 8-lead TO-5 dual-in-line formed-lead "DIL'CAN" package ("S" suffix).

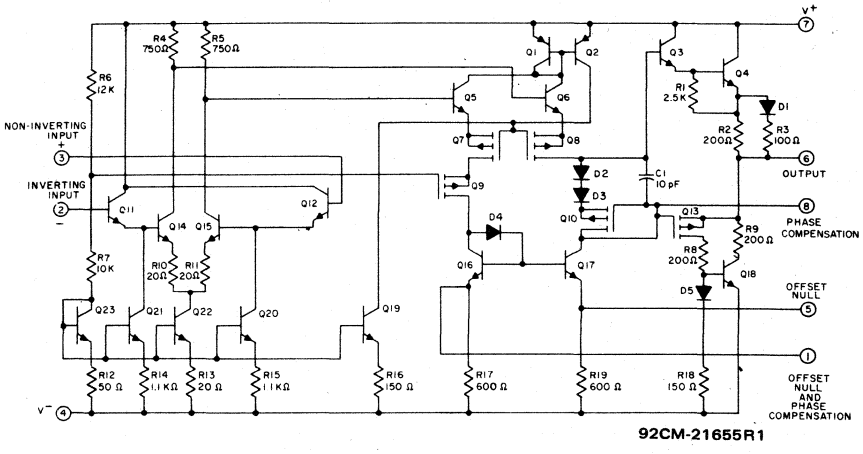


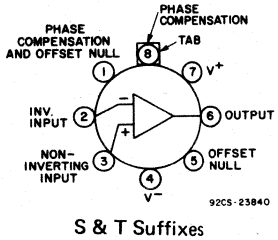
Fig. 1 — Schematic diagram for CA3100.

CA3100 Types

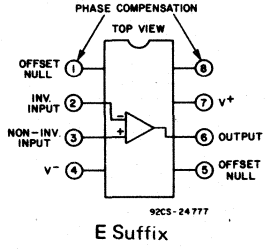
ELECTRICAL CHARACTERISTICS, *At T_A = 25°C:*

CHARACTERISTICS	TEST CONDITIONS SUPPLY VOLTAGE (V^+,V^-)=15 V UNLESS OTHERWISE SPECIFIED	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
STATIC					
Input Offset Voltage, V_{IO}	V_O = 0 ± 0.1 V	–	±1	±5	mV
Input Bias Current, I_{IB}	V_O = 0 ± 1 V	–	0.7	2	μA
Input Offset Current, I_{IO}	V_O = 0 ± 1 V	–	±0.05	±0.4	μA
Low-Frequency Open-Loop Voltage Gain, A_{OL}●	V_O = ± 1 V Peak, F = 1 kHz	56	61	–	dB
Common-Mode Input Voltage Range, V_{ICR}	CMRR ≥ 76 dB	±12	+14 −13	–	V
Common-Mode Rejection Ratio, CMRR	V_I Common Mode = ± 12 V	76	90	–	dB
Maximum Output Voltage: Positive, V_{OM}^+	Differential Input Voltage = 0 ± 0.1 V, R_L = 2 KΩ	+9	+11	–	V
Maximum Output Voltage: Negative, V_{OM}^-	Differential Input Voltage = 0 ± 0.1 V, R_L = 2 KΩ	−9	−11	–	V
Maximum Output Current: Positive, I_{OM}^+	Differential Input Voltage = 0 ± 0.1 V, R_L = 250 Ω	+15	+30	–	mA
Maximum Output Current: Negative, I_{OM}^-	Differential Input Voltage = 0 ± 0.1 V, R_L = 250 Ω	−15	−30	–	mA
Supply Current, I^+	V_O = 0 ± 0.1 V, R_L ≥ 10 KΩ	–	8.5	10.5	mA
Power-Supply Rejection Ratio, PSRR	ΔV^+ = ± 1 V, ΔV^- = ± 1 V	60	70	–	dB
DYNAMIC					
Unity-Gain Crossover Frequency, f_T	C_C = 0, V_O = 0.3 V (P-P)	–	38	–	MHz
1-MHz Open-Loop Voltage Gain, A_{OL}	f = 1 MHz, C_C = 0, V_O = 10 V (P-P)	36	42	–	dB
Slew Rate, SR: 20-dB Amplifier	A_V = 10, C_C = 0, V_I = 1 V (Pulse)	50	70	–	V/μs
Slew Rate, SR: Follower Mode	A_V = 1, C_C = 10 pF, V_I = 10 V (Pulse)	–	25	–	V/μs
Power Bandwidth, PBW▲: 20-dB Amplifier	A_V = 10, C_C = 0, V_O = 18 V (P-P)	0.8	1.2	–	MHz
Power Bandwidth, PBW▲: Follower Mode	A_V = 1, C_C = 10 pF, V_O = 18 V (P-P)	–	0.4	–	MHz
Open-Loop Differential Input Impedance, Z_I	F = 1 MHz	–	30	–	KΩ
Open-Loop Output Impedance, Z_O	F = 1 MHz	–	110	–	Ω
Wideband Noise Voltage Referred to Input, e_N(Total)	BW = 1 MHz, R_S = 1 KΩ	–	8	–	μV_{RMS}
Settling Time, t_s To Within ± 50 mV of 9 V Output Swing	R_L = 2 KΩ, C_L = 20 pF	–	0.6	–	μs

▲ Power Bandwidth = $\frac{\text{Slew Rate}}{\pi V_O \text{ (P-P)}}$ ● Low-frequency dynamic characteristic



S & T Suffixes



E Suffix

TERMINAL ASSIGNMENTS

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Supply Voltage (between V+ and V⁻ terminals)	36	V
Differential Input Voltage	±12	V
Input Voltage to Ground*	±15	V
Offset Terminal to V⁻ Terminal Voltage	±0.5	V
Output Current	50	mA•
Device Dissipation:		
Up to T_A = 55°C	630	mW
Above T_A = 55°C	6.67	mW/°C
Ambient Temperature Range:		
Operating:		
E Type	−40 to +85	°C
S and T Types	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

* If the supply voltage is less than ±15 volts, the maximum input voltage to ground is equal to the supply voltage.

• CA3100S, CA3100T does not contain circuitry to protect against short circuits in the output.

TYPICAL CHARACTERISTIC CURVES

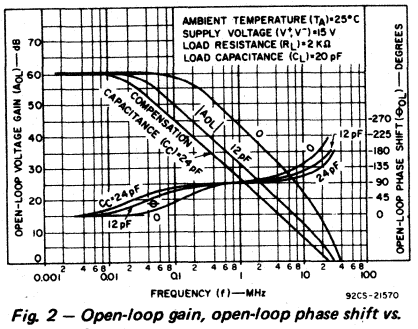


Fig. 2 – Open-loop gain, open-loop phase shift vs. frequency.

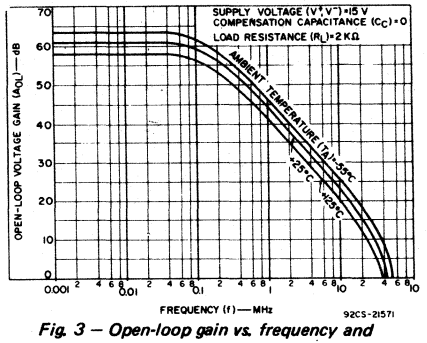


Fig. 3 – Open-loop gain vs. frequency and temperature.

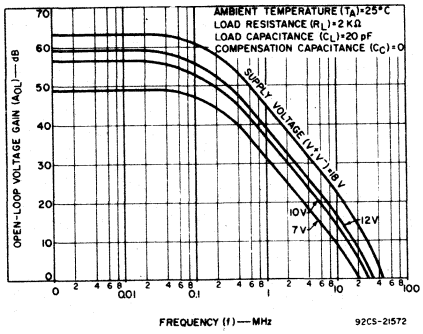


Fig. 4 – Open-loop gain vs. frequency and supply voltage.

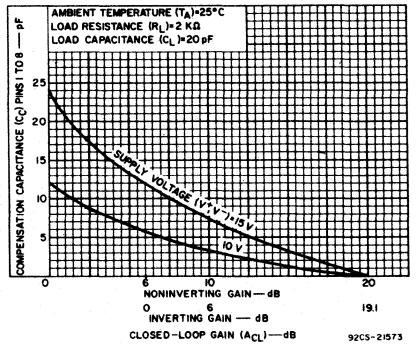


Fig. 5 – Required compensation capacitance vs. closed-loop gain.

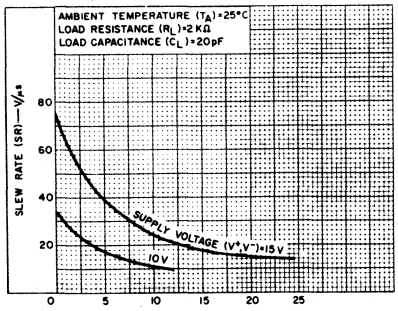


Fig. 6 – Slew rate vs. compensation capacitance.

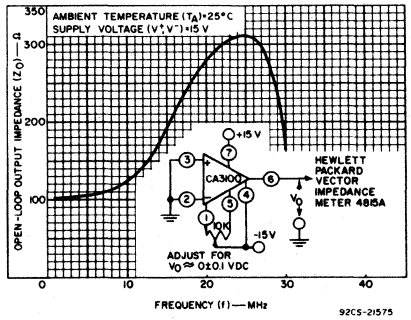


Fig. 7 – Typical open-loop output impedance vs. frequency.

TYPICAL CHARACTERISTIC CURVES (Cont'd)

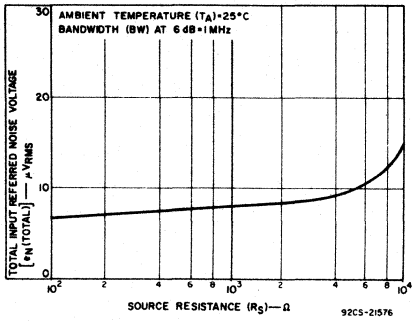


Fig. 8 – Wideband input noise voltage vs. source resistance.

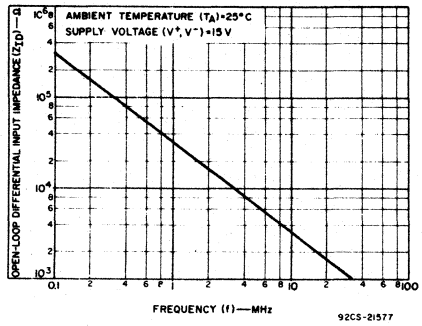


Fig. 9 – Typical open-loop differential input impedance vs. frequency.

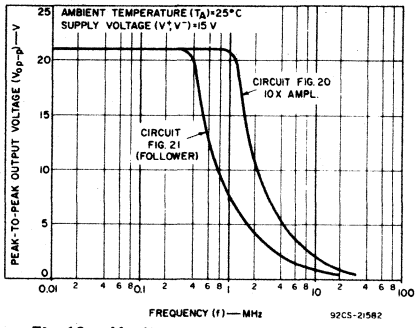


Fig. 10 – Maximum output voltage swing vs. frequency.

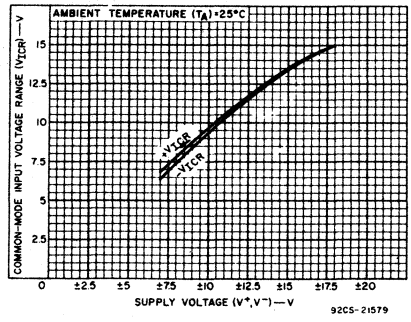


Fig. 11 – Common-mode input voltage range vs. supply voltage.

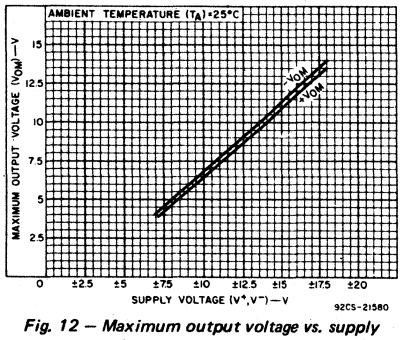


Fig. 12 – Maximum output voltage vs. supply voltage.

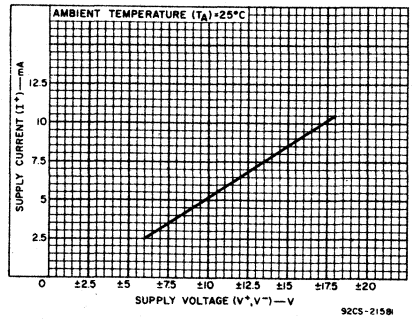


Fig. 13 – Supply current vs. supply voltage.

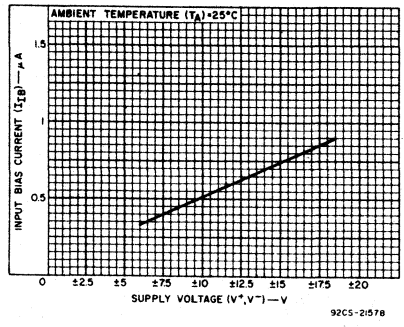


Fig. 14 – Input bias current vs. supply voltage.

TEST CIRCUITS

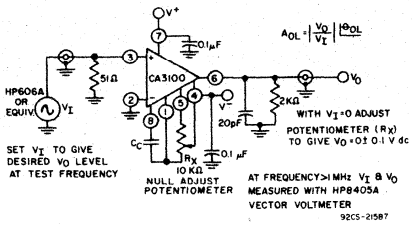


Fig. 15 – Open-loop voltage gain test circuit.

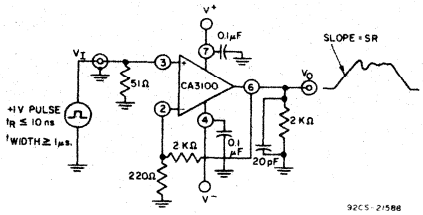


Fig. 16 – Slew rate in 10X amplifier test circuit.

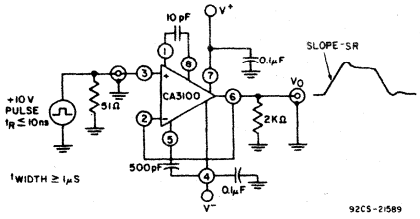


Fig. 17 – Follower slew rate test circuit.

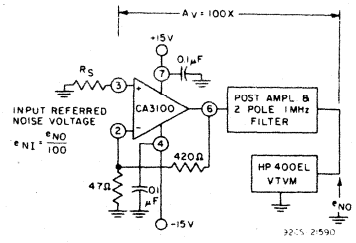


Fig. 18 – Wideband input noise voltage test circuit.

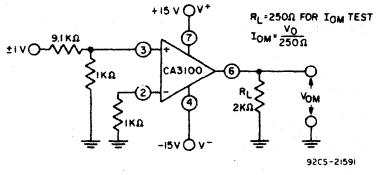


Fig. 19 – Output voltage swing (V_{OM}), output current swing (I_{OM}) test circuit.

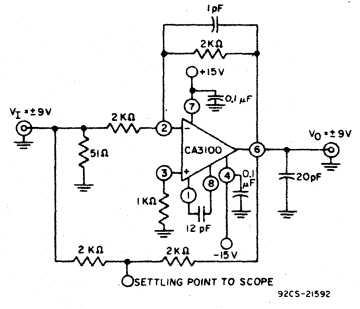


Fig. 20 – Settling time test circuit.

TYPICAL APPLICATIONS

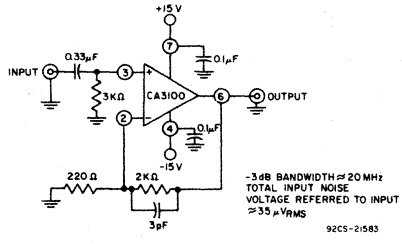


Fig. 21 – 20 dB video amplifier.

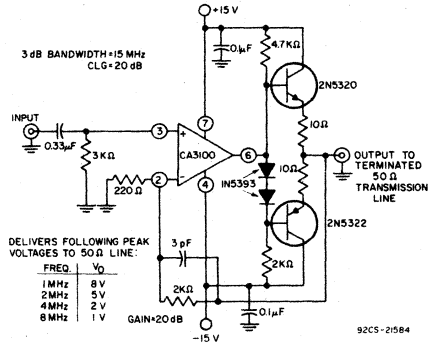


Fig. 22 – 20 dB video line driver.

TYPICAL APPLICATIONS (Cont'd)

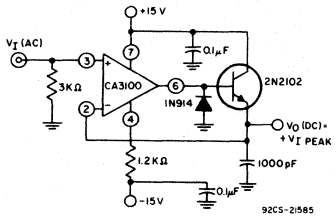


Fig. 23 – Fast positive peak detector.

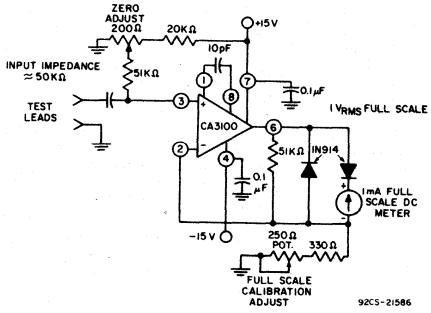
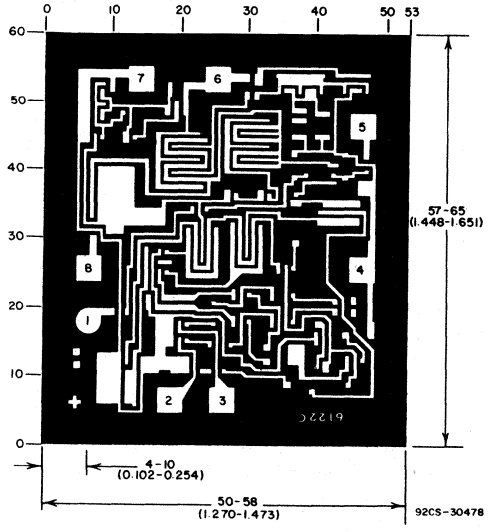


Fig. 24 – 1 MHz meter-driver amplifier.

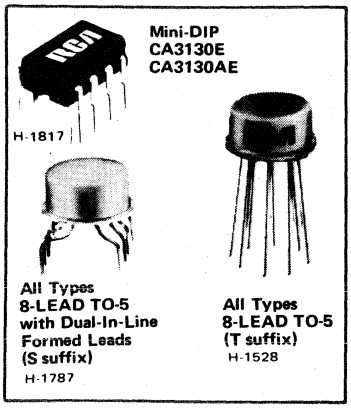
Chip Dimensions and Pad Layout



CA3100H Chip

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



BiMOS Operational Amplifiers

With MOS/FET Input/ COS/MOS Output

FEATURES:

- *MOS/FET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 × 10^{12}Ω) typ.
  very low II = 5 pA typ. at 15-V operation
  2 pA typ. at 5-V operation
- *Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *COS/MOS output stage permits signal swing to either (or both) supply rails*

} *Ideal for single-supply applications*

RCA-CA3130T, CA3130E, CA3130S, CA-3130AT, CA 3130AS, CA3130AE, CA3130BT, and CA3130BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3130 Series is supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA3130 is available in chip form (H suffix). The CA3130 and CA3130A are also available in the Mini-DIP 8-lead dual-in-line plastic package (E suffix). All types operate over the full military-temperature range of -55°C to +125°C. The CA3130B is intended for applications requiring premium-grade specifications. The CA3130A offers superior input characteristics over those of the CA3130.

- *Low V_{IO}: 2 mV max. (CA3130B)*
- *Wide BW: 15 MHz typ. (unity-gain crossover)*
- *High SR: 10 V/μs typ. (unity-gain follower)*
- *High output current (I_O): 20 mA typ.*
- *High A_{OL}: 320,000 (110 dB) typ.*
- *Compensation with single external capacitor*

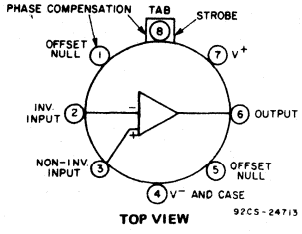
APPLICATIONS:

- *Ground-referenced single-supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *High-input-impedance comparators (ideal interface with digital COS/MOS)*
- *High-input-impedance wideband amplifiers*
- *Voltage followers (e.g., follower for single-supply D/A converter)*
- *Voltage regulators (permits control of output voltage down to zero volts)*
- *Peak detectors*
- *Single-supply full-wave precision rectifiers*
- *Photo-diode sensor amplifiers*

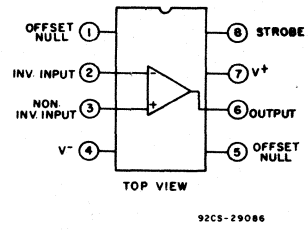
CA3130, CA3130A, CA3130B

ELECTRICAL CHARACTERISTICS at T_A=25°C, V^+=15 V, V^- = 0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS									Units
	CA3130B (T,S)			CA3130A (T,S,E)			CA3130 (T,S,E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.8	2	–	2	5	–	8	15	mV
Input Offset Current, $\|I_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	–	5	20	–	5	30	–	5	50	pA
Large-Signal Voltage Gain, A_{OL}	100 k	320 k	–	50 k	320 k	–	50 k	320 k	–	V/V
V_O=10 V_{p-p}, R_L=2 kΩ	100	110	–	94	110	–	94	110	–	dB
Common-Mode Rejection Ratio, CMRR	86	100	–	80	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR}	0	−0.5 to 12	10	0	−0.5 to 12	10	0	−0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	–	32	100	–	32	150	–	32	320	μV/V
Maximum Output Voltage:										
At R_L=2 kΩ V_{OM}^+	12	13.3	–	12	13.3	–	12	13.3	–	V
V_{OM}^-	–	0.002	0.01	–	0.002	0.01	–	0.002	0.01	
At R_L=∞ V_{OM}^+	14.99	15	–	14.99	15	–	14.99	15	–	
V_{OM}^-	–	0	0.01	–	0	0.01	–	0	0.01	
Maximum Output Current: I_{OM}^+ (Source) @ V_O = 0 V	12	22	45	12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O = 15 V	12	20	45	12	20	45	12	20	45	
Supply Current, I^+: V_O=7.5 V, R_L=∞	–	10	15	–	10	15	–	10	15	mA
V_O = 0 V, R_L = ∞	–	2	3	–	2	3	–	2	3	
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$*	–	5	–	–	10	–	–	10	–	μV/°C



S and T Suffixes



E Suffix

Fig.1 – Functional diagrams for the CA3130 series.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS ($V^+ = +7.5$ V, $V^- = -7.5$ V, $T_A = 25^oC$ (Unless Otherwise Specified))	CA3130B (T,S)	CA3130A (T,S,E)	CA3130 (T,S,E)	UNITS
Input Offset Voltage Adjustment Range	10 kΩ across Terms. 4 and 5 or 4 and 1	±22	±22	±22	mV
Input Resistance, R_I		1.5	1.5	1.5	TΩ
Input Capacitance, C_I	f = 1 MHz	4.3	4.3	4.3	pF
Equivalent Input Noise Voltage, e_n	BW = 0.2 MHz, R_S = 1 MΩ*	23	23	23	μV
Unity Gain Crossover Frequency, f_T	$C_C = 0$	15	15	15	MHz
	C_C = 47 pF	4	4	4	
Slew Rate, SR: Open Loop	$C_C = 0$	30	30	30	V/μs
Closed Loop	C_C = 56 pF	10	10	10	
Transient Response: Rise Time, t_r	C_C = 56 pF, C_L = 25 pF, R_L = 2 kΩ (Voltage Follower)	0.09	0.09	0.09	μs
Overshoot		10	10	10	%
Settling Time (4 V_{p-p} Input to <0.1%)		1.2	1.2	1.2	μs

* Although a 1-MΩ source is used for this test, the equivalent input noise remains constant for values of R_S up to 10 MΩ.

CHARACTERISTIC	TEST CONDITIONS ($V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$ (Unless Otherwise Specified))	CA3130B (T,S)	CA3130A (T,S,E)	CA3130 (T,S,E)	UNITS
Input Offset Voltage, V_{IO}		1	2	8	mV
Input Offset Current, I_{IO}		0.1	0.1	0.1	pA
Input Current, I_I		2	2	2	pA
Common-Mode Rejection Ratio, CMRR		100	90	80	dB
Large-Signal Voltage Gain, A_{OL}	V_O = 4 V_{p-p}, R_L = 5 kΩ	100 k	100 k	100 k	V/V
		100	100	100	dB
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.8	0 to 2.8	0 to 2.8	V
Supply Current, I^+	V_O = 5 V, $R_L = \infty$	300	300	300	μA
	V_O = 2.5 V, $R_L = \infty$	500	500	500	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	200	μV/V

CA3130, CA3130A, CA3130B

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC
INPUT VOLTAGE... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK −
UP TO 55°C ..... 630 mW
ABOVE 55°C .... Derate linearly 6.67 mW/°C
WITH HEAT SINK −
UP TO 90°C ..... 1 W
ABOVE 90°C ... Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:
OPERATING (all types) ..... −55 to + 125°C
STORAGE (all types) ..... −65 to + 150°C
OUTPUT SHORT-CIRCUIT
DURATION* ..... INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH
(1.59 ± 0.79 mm) FROM CASE
FOR 10 SECONDS MAX. ..... +265°C

*Short circuit may be applied to ground or to either supply.

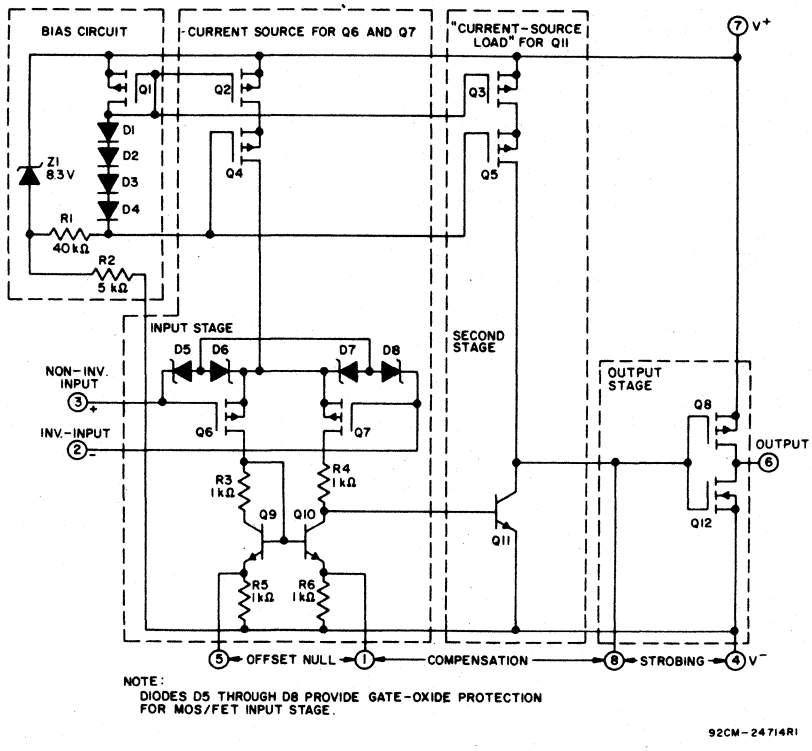


Fig. 2 – Schematic diagram of the CA3130 Series.

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3130 Series COS/MOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive COS/MOS digital circuits in comparator applications).

Input Stages—The circuit of the CA3130 is shown in Fig. 2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

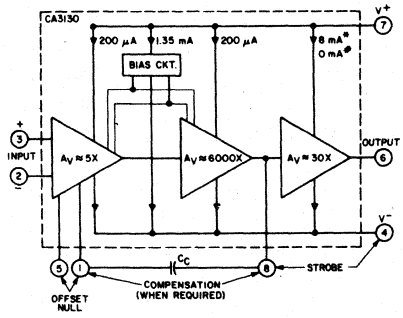
Second-Stage—Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit—At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes nonconductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage, Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage—The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are nonlinear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

†For general information on the characteristics of COS/MOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "COS/MOS Transistor Array".



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15 V
* WITH INPUT TERMINALS BIASED SO THAT TERM. 6 POTENTIAL IS +7.5 V ABOVE TERM. 4.
* WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.

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Fig. 3 – Block diagram of the CA3130 Series.

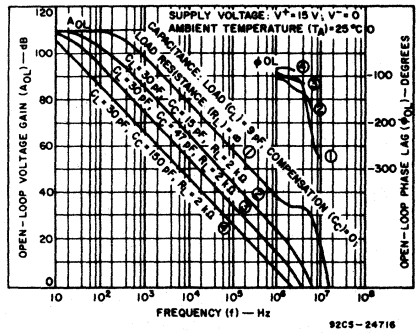

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Fig. 4 – Open-loop voltage gain and phase shift vs. frequency for various values of C_L, C_C, and R_L.

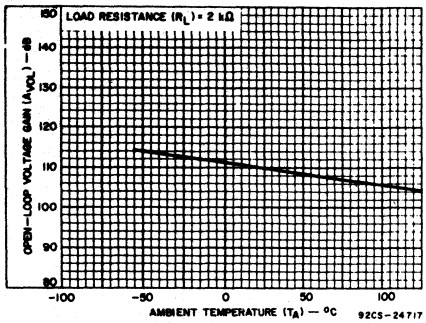


Fig. 5 – Open-loop gain vs. temperature.

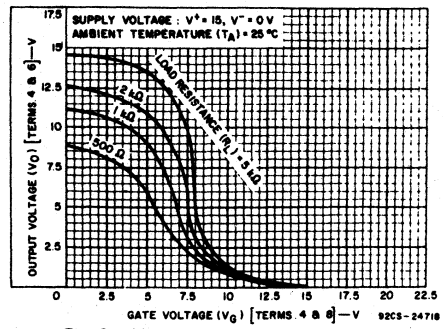


Fig. 6 – Voltage transfer characteristics of COS/MOS output stage.

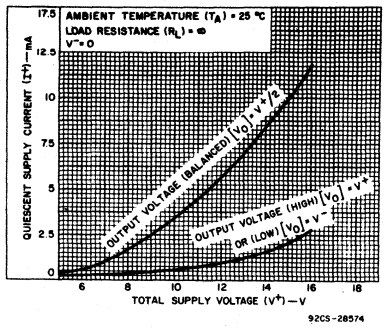


Fig. 7 – Quiescent supply current vs. supply voltage.

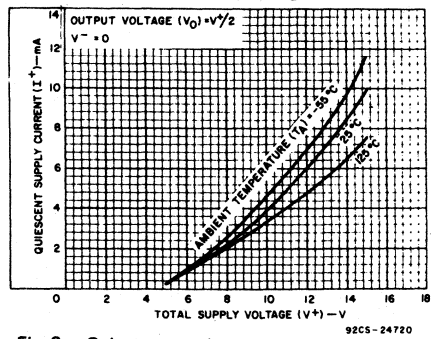


Fig. 8 – Quiescent supply current vs. supply voltage at several temperatures.

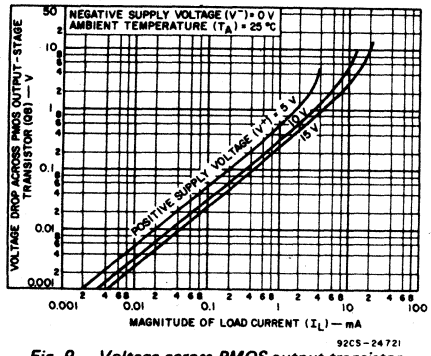


Fig. 9 – Voltage across PMOS output transistor (Q8) vs. load current.

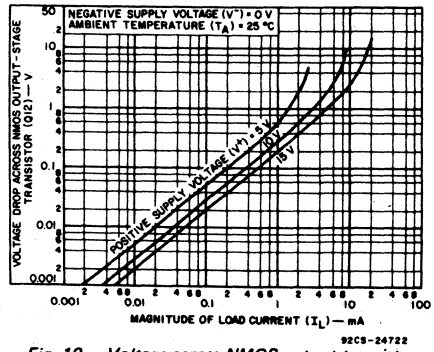


Fig. 10 – Voltage across NMOS output transistor (Q12) vs. load current.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3130 Series Op-Amps is typically 5 pA at T_A=25°C when terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig.11 contains data showing the variation of input current as a function of common-mode input voltage at T_A = 25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied

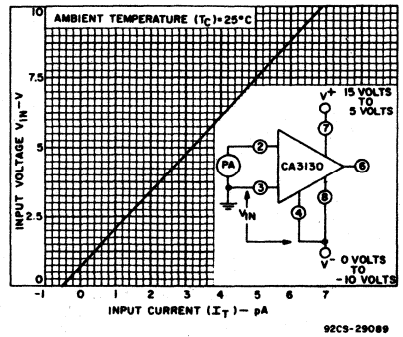


Fig.11 – Input current vs. common-mode voltage.

voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3130 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig.12 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

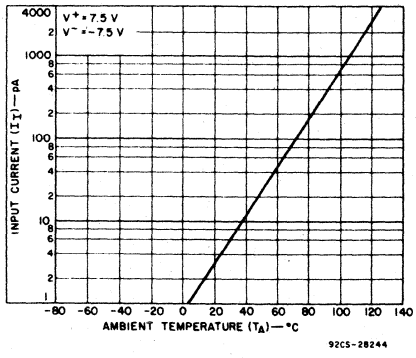


Fig.12 – Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terms. 2 and 3. Fig.13 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices (TO-5 package) during life testing. At lower temperatures (TO-5 and plastic), for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

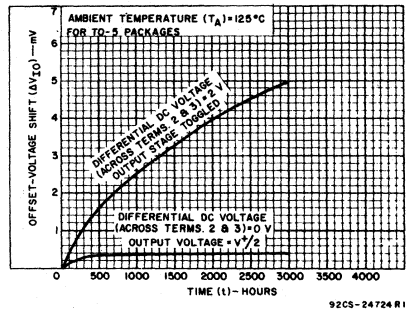


Fig.13 – Typical incremental offset-voltage shift vs. operating life.

Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 14a and 14b show the CA3130 connected for both dual- and single-supply operation.

Dual-supply operation: When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e.,

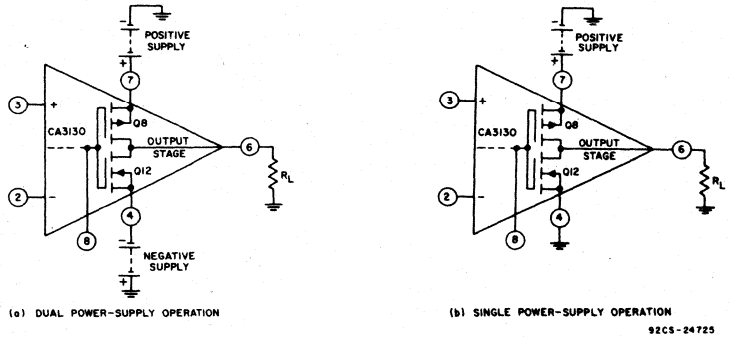


Fig.14 – CA3130 output stage in dual and single power-supply operation.

the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 14a shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L=\infty$, by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Fig.14b. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is a $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply-voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 23 μV when the test-circuit amplifier of Fig. 15 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

TYPICAL APPLICATIONS

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Fig. 16 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Fig. 17, together with related waveforms. This follower circuit is

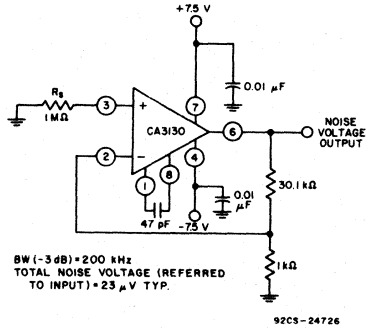
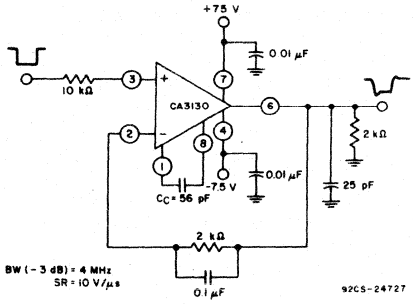
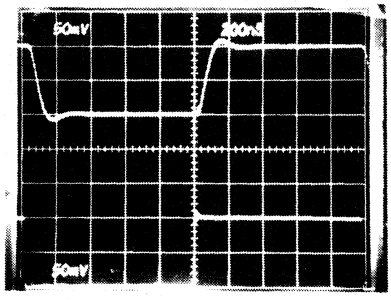
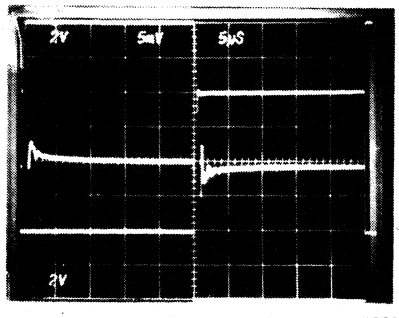


Fig.15 – Test-circuit amplifier (30-dB gain) used for wideband noise measurements.





Top Trace: Output
Bottom Trace: Input
(a) Small-signal response (50 mV/div. and 200 ns/div.)



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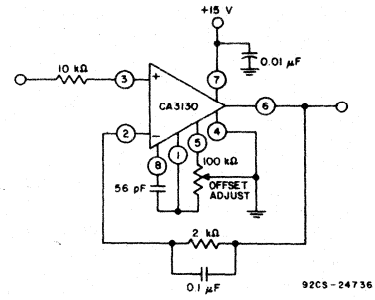
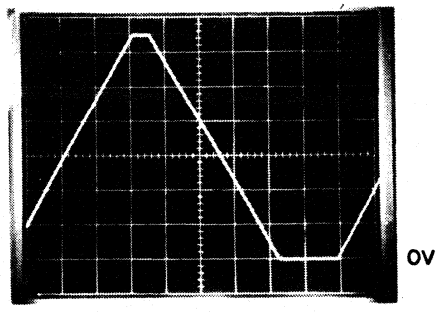
Top Trace: Output signal (2 V/div. and 5 μs/div.)
Center Trace: Difference signal (5 mV/div. and 5 μs/div.)
Bottom Trace: Input signal (2 V/div. and 5 μs/div.)
(b) Input-output difference signal showing settling time (Measurement made with Tektronix 7A13 differential amplifier)

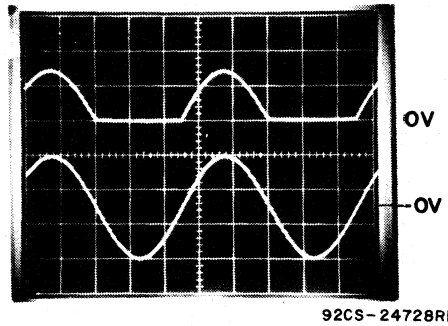
Fig. 16 – Split-supply voltage follower with associated waveforms.

linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 17a, with input-signal ramping. The waveforms in Fig. 17b show that the follower does not lose its input-to-output phase-sense, even though the input is





(a) Output-waveform with input-signal ramping (2 V/div. and 500 μs/div.)



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Top Trace: Output (5 V/div. and 200 μs/div.)
Bottom Trace: Input (5 V/div. and 200 μs/div.)
(b) Output-waveform with ground-reference sine-wave input

Fig. 17 – Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig. 9 in ICAN-6080).

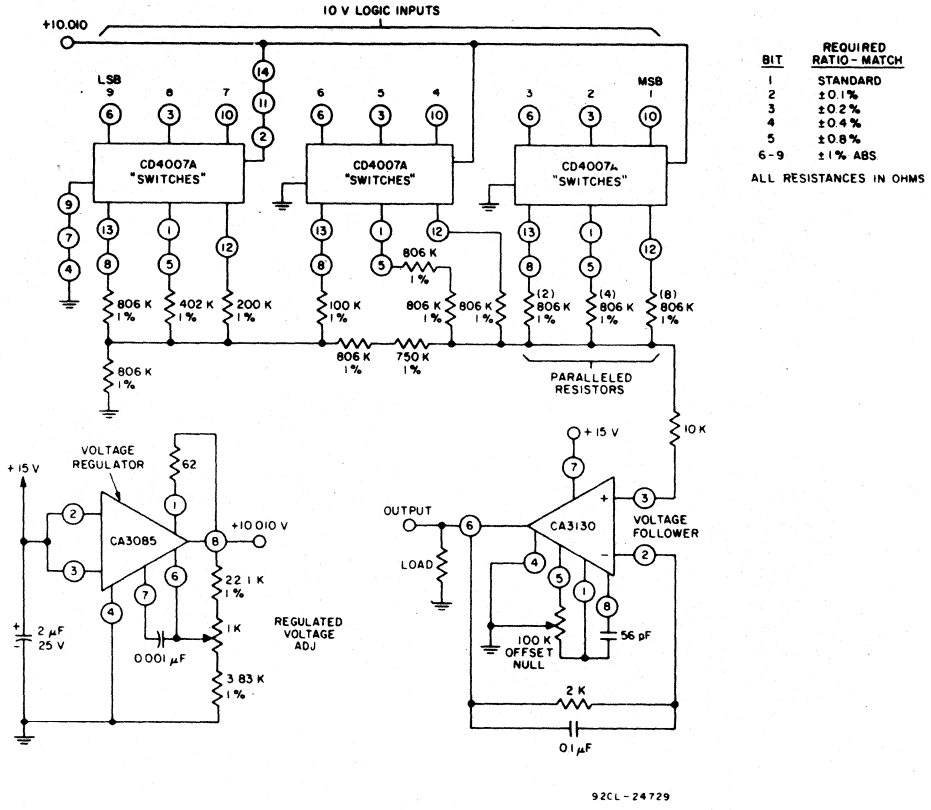
being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 17b also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.

9-Bit COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig.18 This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with COS/MOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig.18.

of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with varia-



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS

ALL RESISTANCES IN OHMS

Fig.18 – 9-bit DAC using COS/MOS digital switches and CA3130.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly

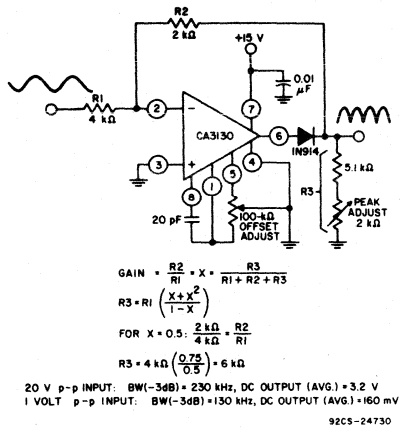
tions of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

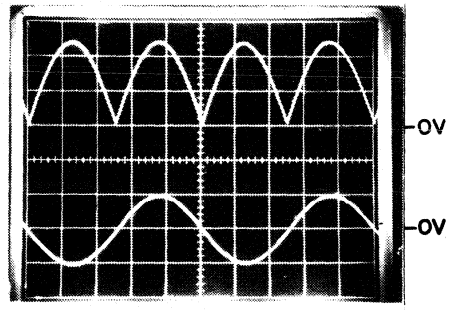
Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

The absolute-value circuit using the CA3130 is shown in Fig. 19. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a

*"Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC", Application Note ICAN-6080.

negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to −R2/R1. When the equality of the two equations shown in Fig. 19 is satisfied, the full-wave output is symmetrical.





Top Trace: Output signal (2 V/div.)
Bottom Trace: Input signal (10 V/div.)
Time base on both traces: 0.2 ms/div.

Fig. 19 — Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.

Peak Detectors

Peak-detector circuits are easily implemented with the CA3130, as illustrated in Fig. 20 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in an active "pull-down" mode so that the intrinsic capacitance can be discharged more expeditiously.

Error-Amplifier in Regulated-Power Supplies

The CA3130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero. Fig. 21 shows the schematic diagram of a 40-mA power supply capable of providing regulated output voltage by continuous adjustment over the range from 0 to 13 volts. Q3 and Q4 in IC2 (a CA3086 transistor-array IC) function as zeners to provide supply-voltage for the CA3130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier. Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q5 in IC3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R2.

Fig. 22 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous ad-

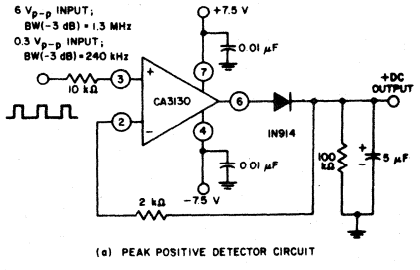


Fig. 20 — Peak-detector circuits.

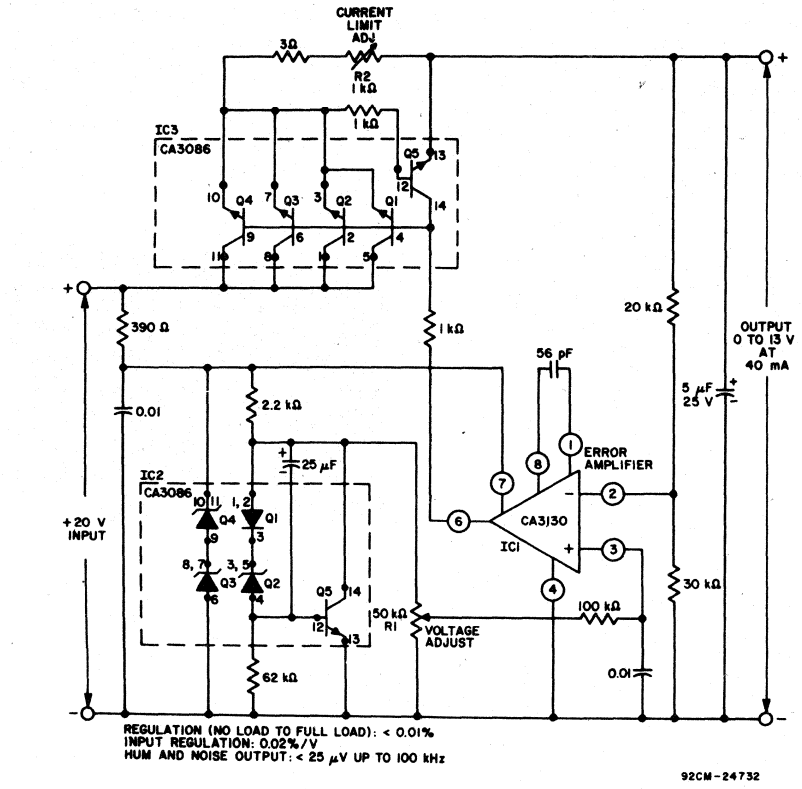


Fig.21 – Voltage regulator circuit (0 to 13 V at 40 ma).

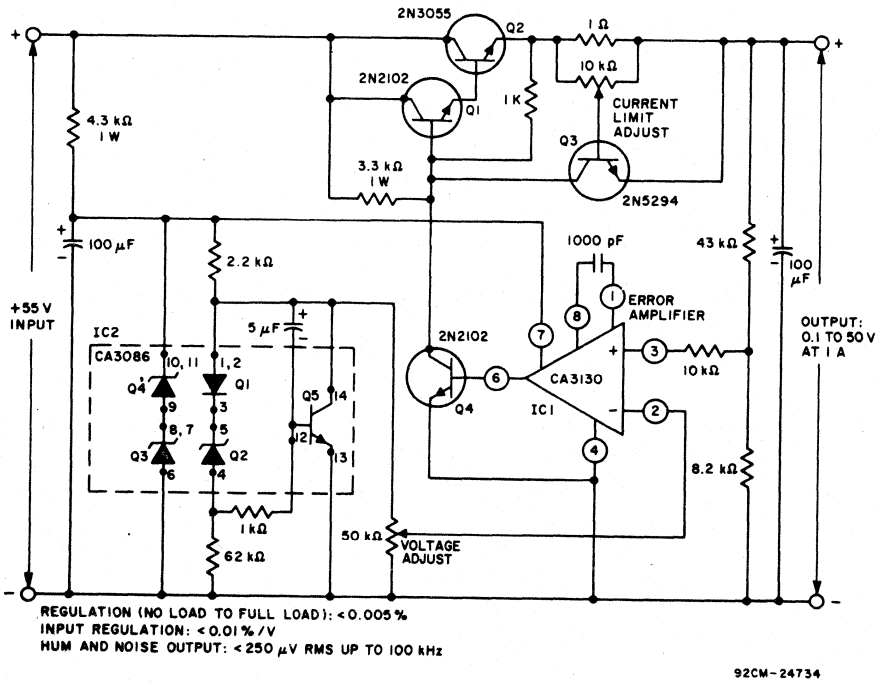


Fig.22 – Voltage regulator circuit (0.1 to 50 V at 1 A).

justment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Fig. 23. Resistors R1 and R2 are used to bias the CA3130 to the mid-point of the supply-voltage and R3 is the feedback resistor. The pulse repetition rate is selected by positioning S1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

Function Generator

Fig. 24 contains a schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)*, IC1, operated as a voltage-controlled current-source. The output, I_O, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA3130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

*See File No. 475 and ICAN-6668.

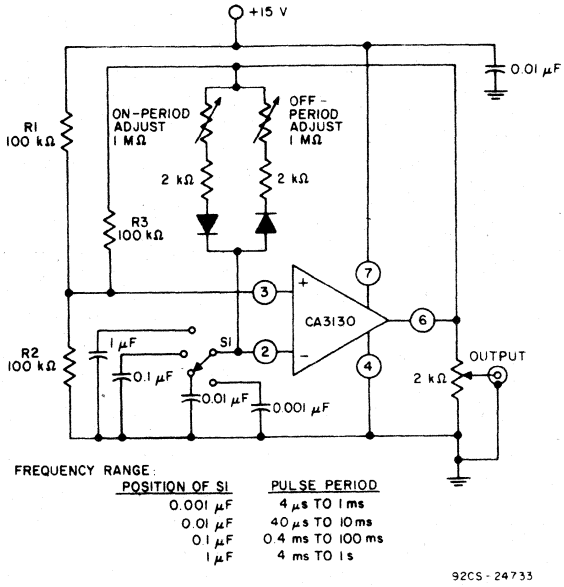


Fig.23 — Pulse generator (astable multivibrator) with provisions for independent control of "ON" and "OFF" periods.

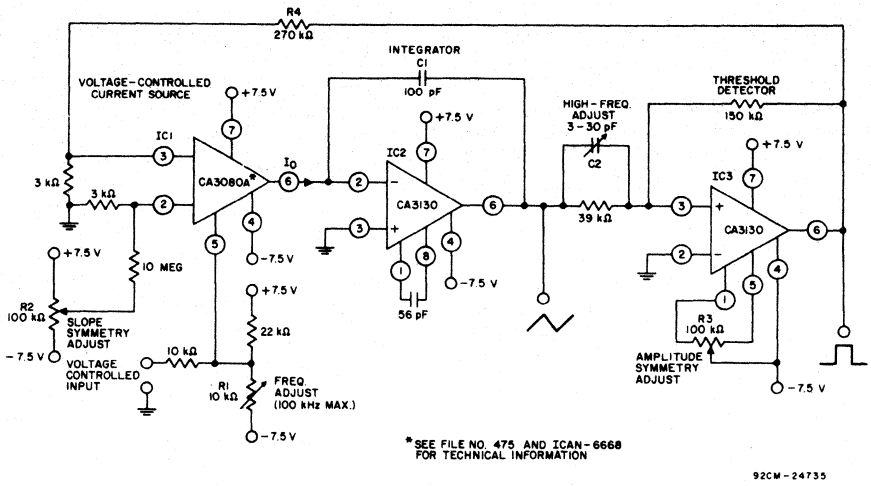


Fig. 24 — Function generator (frequency can be varied 1,000,000/1 with a single control).

Operation with Output-Stage Power-Booster

The current-sourcing and -sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 25, three COS/MOS transistor-pairs in a single CA3600E* IC array are shown parallel connected with the output stage in the CA3130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA3130 output stage by about 2.5X.

The amplifier circuit in Fig. 25 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (−3 dB) is 50 kHz.

*See File No. 619 for technical information.

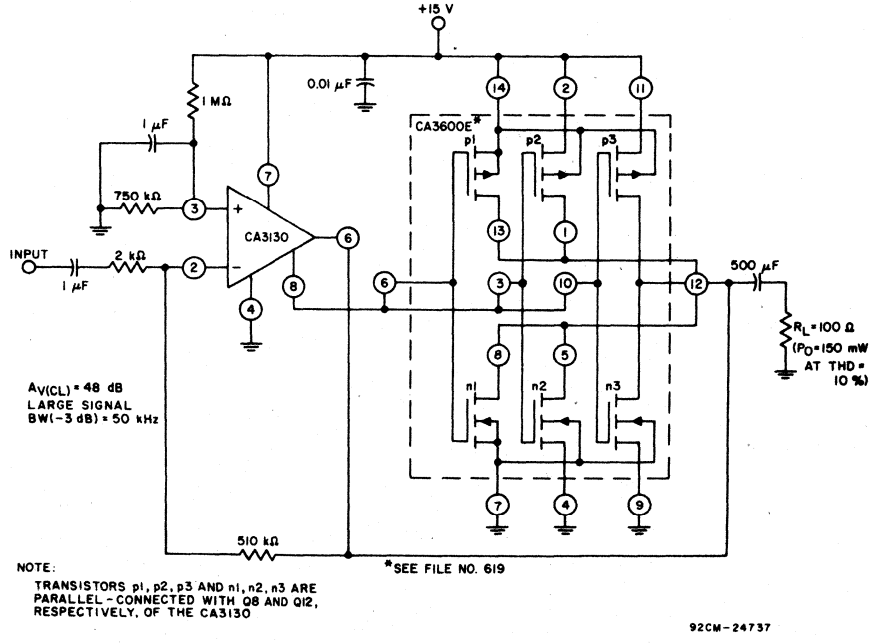
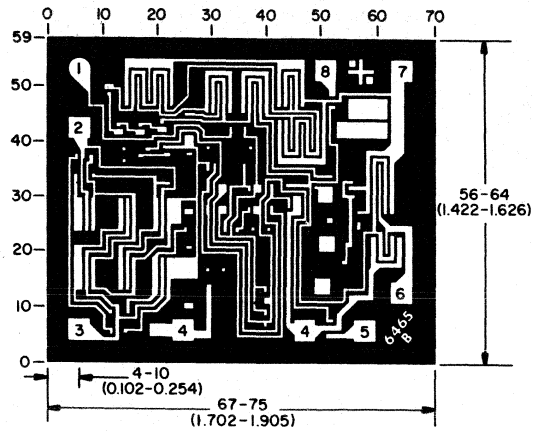


Fig. 25 — COS/MOS transistor array (CA3600E) connected as power-booster in the output stage of the CA3130.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and Pad Layout for CA3130H.

CA3140, CA3140A, CA3140B Types

BiMOS Operational Amplifiers

With MOS/FET Input/Bipolar Output

FEATURES:

- *MOS/FET Input Stage*
  - *(a) Very high input impedance (Z_{IN}) — 1.5 TΩ typ.*
  - *(b) Very low input current (I_I) — 10 pA typ. at ± 15 V*
  - *(c) Low input-offset voltage (V_{IO}) — to 2 mV max.*
  - *(d) Wide common-mode input-voltage range (V_{ICR})— can be swung 0.5 volt below negative supply-voltage rail*
  - *(e) Output swing complements input common-mode range*
  - *(f) Rugged input stage — bipolar diode protected*
- *Directly replaces industry type 741 in most applications*
- *Includes numerous industry operational amplifier categories such as general-purpose, FET input, wideband (high slew rate)*
- *Operation from 4-to-44 volts Single or Dual supplies*
- *Internally compensated*
- *Characterized for ± 15-volt operation and for TTL supply systems with operation down to 4 volts*
- *Wide bandwidth — 4.5 MHz unity gain at ± 15 V or 30 V; 3.7 MHz at 5 V*
- *High voltage-follower slew rate — 9 V/μs*
- *Fast setting time — 1.4 μs typ. to 10 mV with a 10-V_{p-p} signal*
- *Output swings to within 0.2 volt of negative supply*
- *Strobable output stage*

APPLICATIONS:

- *Ground-referenced single-supply amplifiers in automobile and portable instrumentation*
- *Sample and hold amplifiers*
- *Long-duration timers/multivibrators (microseconds—minutes—hours)*
- *Photocurrent instrumentation*
- *Peak detectors* ■ *Active filters*
- *Comparators*
- *Interface in 5 V TTL systems & other low-supply voltage systems*
- *All standard operational amplifier applications*
- *Function generators* ■ *Tone controls*
- *Power supplies* ■ *Portable instruments*
- *Intrusion alarm systems*

The CA3140B, CA3140A, and CA3140 are integrated-circuit operational amplifiers that combine the advantages of high-voltage PMOS transistors with high-voltage bipolar transistors on a single monolithic chip. Because of this unique combination of technologies, this device can now provide designers, for the first time, with the special performance features of the CA3130 COS/MOS operational amplifiers and the versatility of the 741 series of industry-standard operational amplifiers.

The CA3140, CA3140A, and CA3140 BiMOS operational amplifiers feature gate-protected MOS/FET (PMOS) transistors in the input circuit to provide very-high-input impedance, very-low-input current, and high-speed performance. The CA3140B operates at supply voltages from 4 to 44 volts; the CA3140A and CA3140 from 4 to 36 volts (either single or dual supply). These operational amplifiers are internally phase-compensated to achieve stable operation in unity-gain follower operation, and, additionally, have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset-voltage nulling. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load-terminal short-circuiting to either supply-rail or to ground.

The CA3140 Series has the same 8-lead terminal pin-out used for the "741" and other industry-standard operational amplifiers. They are supplied in either the standard 8-lead TO-5 style package (T suffix), or in the 8-lead dual-in-line formed-lead TO-5 style package "DIL-CAN" (S suffix). The CA3140 is available in chip form (H suffix). The CA3140A and CA3140 are also available in an 8-lead dual-in-line

plastic package (Mini-DIP-E suffix). The CA3140B is intended for operation at supply voltages ranging from 4 to 44 volts, for applications requiring premium-grade specifications. The CA3140A and CA3140 are for operation at supply voltages up to 36 volts (±18 volts). All types can be operated safely over the temperature range from -55°C to +125°C.

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS $V^+ = +15$ V, $V^- = -15$ V, $T_A = 25°C$	CA3140B (T,S)	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage Adjustment Resistor		Typ. Value of Resistor Between Term. 4 and 5 or 4 and 1 to Adjust Max. V_{IO}	43	18	4.7	kΩ
Input Resistance	R_I		1.5	1.5	1.5	TΩ
Input Capacitance	C_I		4	4	4	pF
Output Resistance	R_O		60	60	60	Ω
Equivalent Wideband Input Noise Voltage (See Fig. 39)	e_n	BW = 140 kHz, R_S = 1 MΩ	48	48	48	μV
Equivalent Input Noise Voltage (See Fig.10)	e_n	f = 1 kHz, R_S = 100 Ω	40	40	40	$nV/\sqrt{Hz}$
		f = 10 kHz, R_S = 100 Ω	12	12	12	$nV/\sqrt{Hz}$
Short-Circuit Current to Opposite Supply Source	I_{OM^+}		40	40	40	mA
Sink	I_{OM^-}		18	18	18	mA
Gain-Bandwidth Product, (See Figs. 5 &18)	f_T		4.5	4.5	4.5	MHz
Slew Rate, (See Fig.6)	SR		9	9	9	V/μs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low			220	220	220	μA
Transient Response: Rise Time	t_r	R_L = 2 kΩ, C_L = 100 pF	0.08	0.08	0.08	μs
Overshoot (See Fig. 37)	t_r	R_L = 2 kΩ, C_L = 100 pF	10	10	10	%
Settling Time at 10 V_{p-p}, (See Fig.17)	1 mV / 10 mV t_s	R_L = 2 kΩ, C_L = 100 pF, Voltage Follower	4.5	4.5	4.5	μs
	1 mV / 10 mV t_s	R_L = 2 kΩ, C_L = 100 pF, Voltage Follower	1.4	1.4	1.4	μs

CA3140, CA3140A, CA3140B Types

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At $V^+ = 15$ V, $V^- = 15$ V, $T_A = 25^oC$ Unless Otherwise Specified

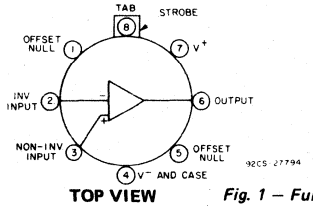
CHARACTERISTIC	LIMITS									UNITS
	CA3140B			CA3140A			CA3140			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	–	0.8	2	–	2	5	–	5	15	mV
Input Offset Current, $\|I_{IO}\|$	–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I	–	10	30	–	10	40	–	10	50	pA
Large-Signal Voltage Gain, A_{OL}● (See Figs. 4,18)	50 k	100 k	–	20 k	100 k	–	20 k	100 k	–	V/V
	94	100	–	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR (See Fig.9)	–	20	50	–	32	320	–	32	320	μV/V
	86	94	–	70	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR} (See Fig.20)	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	11	V
Power-Supply Rejection Ratio, PSRR $\Delta V_{IO}/\Delta V$ (See Fig.11)	–	32	100	–	100	150	–	100	150	μV/V
	80	90	–	76	80	–	76	80	–	dB
Max. Output Voltage■ V_{OM}^+ (See Figs.13,20) V_{OM}^-	+12	13	–	+12	13	–	+12	13	–	V
	−14	−14.4	–	−14	−14.4	–	−14	−14.4	–	
Supply Current, I^+ (See Fig.7)	–	4	6	–	4	6	–	4	6	mA
Device Dissipation, P_D	–	120	180	–	120	180	–	120	180	mW
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$	–	5	–	–	6	–	–	8	–	μV/°C
Max. Output Voltage,★ V_{OM}^+ V_{OM}^-	+19	+19.5	–	–	–	–	–	–	–	V
	−21	−21.4	–	–	–	–	–	–	–	
Large-Signal Voltage Gain, A_{OL}♦★	20 k	50 k	–	–	–	–	–	–	–	V/V
	86	94	–	–	–	–	–	–	–	dB

● At $V_O = 26V_{p\text{-}p}$, +12V, −14V and $R_L = 2\ k\Omega$.

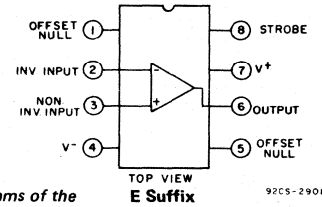
■ At $R_L = 2\ k\Omega$.

♦ At $V_O = +19$ V, −21 V, and $R_L = 2\ k\Omega$.

★ At $V^+ = 22$ V, $V^- = 22$ V.



TOP VIEW
S and T Suffixes



E Suffix

Fig. 1 – Functional diagrams of the CA3140 series.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3140, CA3140A	CA3140B
DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V	44 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±8 V	±8 V
COMMON-MODE DC INPUT VOLTAGE	(V^+ +8 V) to (V^- −0.5 V)	
INPUT-TERMINAL CURRENT	1 mA	
DEVICE DISSIPATION:		
WITHOUT HEAT SINK —		
UP TO 55°C	630 mW	
ABOVE 55°C	Derate linearly 6.67 mW/°C	
WITH HEAT SINK —		
Up to 55°C	1 W	
Above 55°C	Derate linearly 16.7 mW/°C	
TEMPERATURE RANGE:		
OPERATING (ALL TYPES)	−55 to + 125°C	
STORAGE (ALL TYPES)	−65 to +150°C	
OUTPUT SHORT-CIRCUIT DURATION*	INDEFINITE	
LEAD TEMPERATURE (DURING SOLDERING):		
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	+265°C	

* Short circuit may be applied to ground or to either supply.

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE

At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25°C$

CHARACTERISTIC		CA3140B (T,S)	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage	$\lvert V_{IO}\rvert$	0.8	2	5	mV
Input Offset Current	$\lvert I_{IO}\rvert$	0.1	0.1	0.1	pA
Input Current	I_I	2	2	2	pA
Input Resistance		1	1	1	TΩ
Large-Signal Voltage Gain (See Figs.4,18)	A_{OL}	100 k	100 k	100 k	V/V
		100	100	100	dB
Common-Mode Rejection Ratio,	CMRR	20	32	32	μV/V
		94	90	90	dB
Common-Mode Input-Voltage Range (See Fig.20)	V_{ICR}	−0.5	−0.5	−0.5	V
		2.6	2.6	2.6	
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$	32	100	100	μV/V
		90	80	80	dB
Maximum Output Voltage (See Figs.13,20)	V_{OM}^+	3	3	3	V
	V_{OM}^-	0.13	0.13	0.13	
Maximum Output Current: Source	I_{OM}^+	10	10	10	mA
Sink	I_{OM}^-	1	1	1	
Slew Rate (See Fig.6)		7	7	7	V/μs
Gain-Bandwidth Product (See Fig.5)	f_T	3.7	3.7	3.7	MHz
Supply Current (See Fig.7)	I^+	1.6	1.6	1.6	mA
Device Dissipation	P_D	8	8	8	mW
Sink Current from Term. 8 to Term. 4 to Swing Output Low		200	200	200	μA

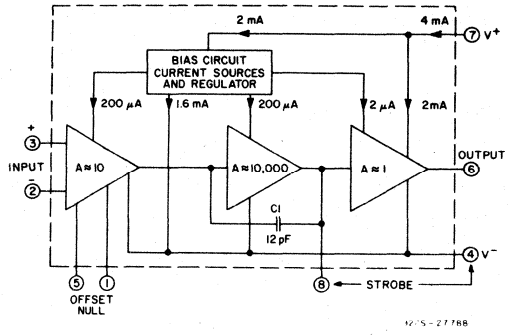


Fig.2 – Block diagram of CA3140 series.

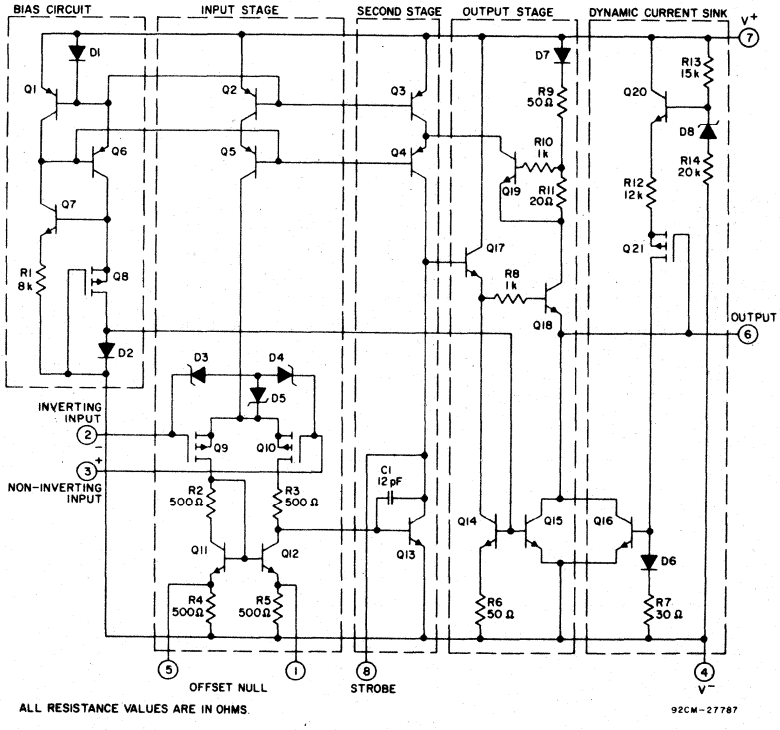


Fig.3 – Schematic diagram of CA3140 series.

CIRCUIT DESCRIPTION

Fig.2 is a block diagram of the CA3140 Series PMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant-current flow circuits in the first and second stages. The CA3140 includes an on-chip phase-compensating capacitor that is sufficient for the unity gain voltage-follower configuration.

Input Stages – The schematic circuit diagram of the CA3140 is shown in Fig.3. It consists of a differential-input stage using PMOS field-effect transistors (Q9, Q10) working into a mirror pair of bipolar transistors (Q11, Q12) functioning as load resistors together with resistors R2 through R5. The mirror-pair transistors also function as a differen-

tial-to-single-ended converter to provide base-current drive to the second-stage bipolar transistor (Q13). Offset nulling, when desired, can be effected with a 10-kΩ potentiometer connected across terminals 1 and 5 and with its slider arm connected to terminal 4. Cascode-connected bipolar transistors Q2, Q5 are the constant-current source for the input stage. The base-biasing circuit for the constant-current source is described subsequently. The small diodes D3, D4, D5 provide gate-oxide protection against high-voltage transients, e.g., static electricity.

Second Stage — Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q13 and its cascode-connected load resistance provided by bipolar transistors Q3, Q4. On-chip phase compensation, sufficient for a majority of the applications is provided by C1. Additional Miller-Effect compensation (roll-off) can be accomplished, when desired, by simply connecting a small capacitor between terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (terminal 4) by mechanical or electrical means, the output terminal 6 swings low, i.e., approximately to terminal 4 potential.

Output Stage — The CA3140 Series circuits employ a broadband output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q17, Q18) is established by transistors (Q14, Q15) whose base-currents are "mirrored" to current flowing through diode D2 in the bias circuit section. When the CA3140 is operating such that output terminal 6 is sourcing current, transistor Q18 functions as an emitter-follower to source current from the V+ bus (terminal 7), via D7, R9, and R11. Under these conditions, the collector potential of Q13 is sufficiently high to permit the necessary flow of base current to emitter follower Q17 which, in turn, drives Q18.

When the CA3140 is operating such that output terminal 6 is sinking current to the V− bus, transistor Q16 is the current-sinking element. Transistor Q16 is mirror-connected to D6, R7, with current fed by way of Q21, R12, and Q20. Transistor Q20, in turn, is biased by current-flow through R13, zener D8, and R14. The dynamic current-sink is controlled by voltage-level sensing. For purposes of explanation, it is assumed that output terminal 6 is quiescently established at the potential mid-point between the V+ and V− supply rails. When output-current sinking-mode operation is required, the collector potential of transistor Q13 is driven below its quiescent level, thereby causing Q17, Q18 to decrease the output voltage at terminal 6. Thus, the gate terminal of PMOS transistor Q21 is displaced toward the V− bus, thereby reducing the channel resistance of Q21. As a consequence, there is an incremental increase in current flow through Q20, R12, Q21, D6, R7, and the base of Q16. As a result, Q16 sinks current from terminal 6 in direct response to the incremental change in output voltage caused by Q18. This sink current flows regardless of load; any excess current is internally supplied by the emitter-follower Q18. Short-circuit protection of the output circuit is provided by Q19, which is driven into conduction by the high voltage drop developed across R11 under output short-circuit conditions. Under these conditions, the collector of Q19 diverts current from Q4 so as to reduce the base-current drive from Q17, thereby limiting current flow in Q18 to the short-circuited load terminal.

Bias Circuit — Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R1. The function of the bias circuit is to establish and maintain constant-current flow through D1, Q6, Q8 and D2. D1 is a diode-connected transistor mirror-connected in parallel with the base-emitter junctions of Q1, Q2, and Q3. D1 may be considered as a current-sampling diode that senses the emitter current of Q6 and automatically adjusts the base current of Q6 (via Q1) to maintain a constant current through Q6, Q8, D2. The base-currents in Q2, Q3 are also determined by constant-current flow D1. Furthermore, current in diode-connected transistor D2 establishes the currents in transistors Q14 and Q15.

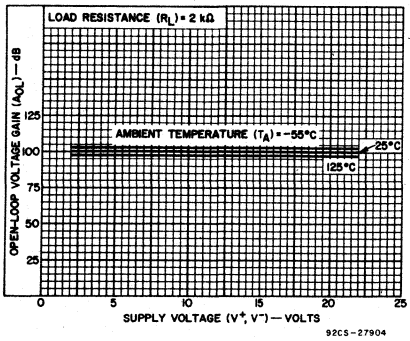


Fig.4 — Open-loop voltage gain vs supply voltage and temperature.

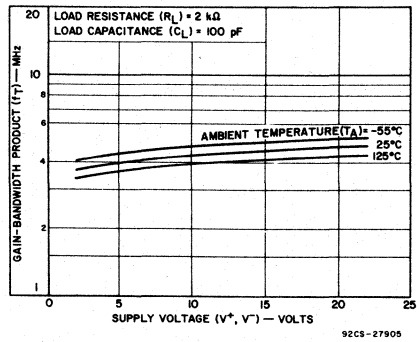


Fig.5 — Gain-bandwidth product vs supply voltage and temperature.

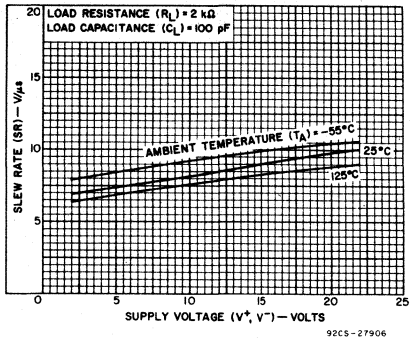


Fig.6 — Slew rate vs supply voltage andtemperature.

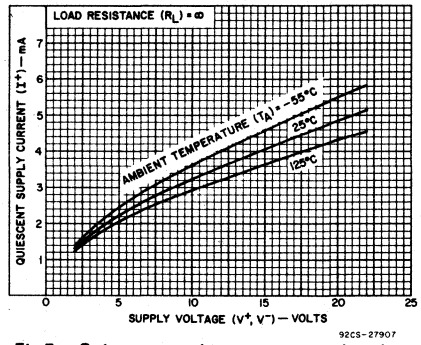


Fig.7 — Quiescent supply current vs supply voltage and temperature.

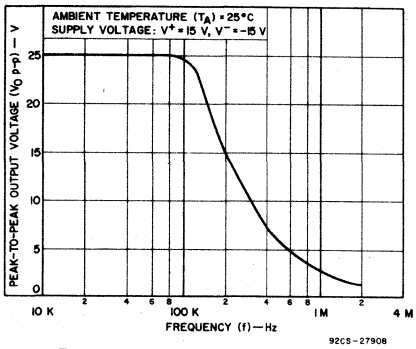


Fig.8 — Maximum output voltage swing vs frequency.

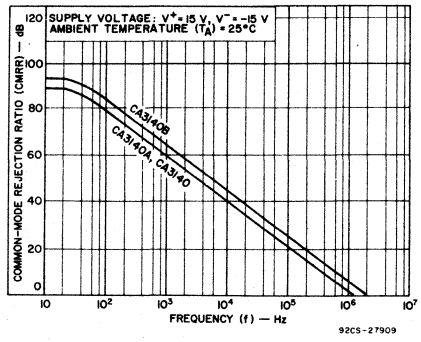


Fig.9 — Common-mode rejection ratio vs frequency.

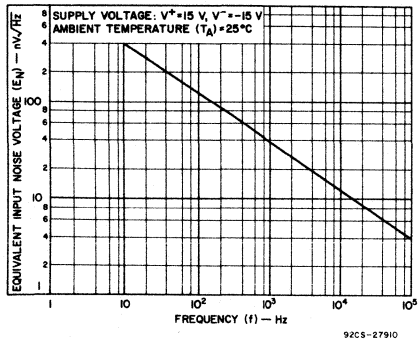


Fig.10 — Equivalent input noise voltage vs frequency.

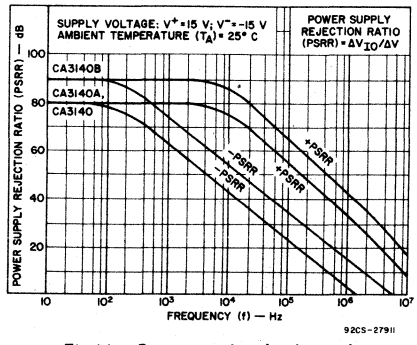


Fig.11 — Power supply rejection ratio vs frequency.

APPLICATIONS CONSIDERATIONS

Wide dynamic range of input and output characteristics with the most desirable high input-impedance characteristic is achieved in the CA3140 by the use of an unique design based upon the PMOS-Bipolar process. Input-common-mode voltage range and output-swing capabilities are complementary, allowing operation with the single supply down to four volts.

The wide dynamic range of these parameters also means that this device is suitable for many single-supply applications, such as, for example, where one input is driven below the potential of terminal 4 and the phase sense of the output signal must be maintained — a most important consideration in comparator applications.

OUTPUT CIRCUIT CONSIDERATIONS

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2-volt zener diode connected to terminal 8 as shown in Fig.12. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the CA3140. These voltages are independent of the operating supply voltage.

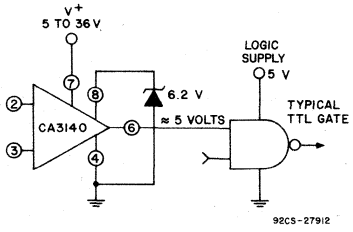


Fig.12 — Zener clamping diode connected to terminals 8 and 4 to limit CA3140 output swing to TTL levels.

Fig.13 shows output current-sinking capabilities of the CA3140 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

Fig.16 show some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

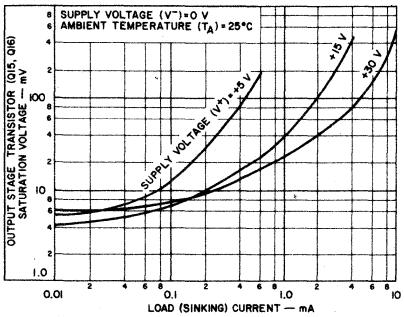


Fig.13 — Voltage across output transistors Q15 and Q16 vs load current.

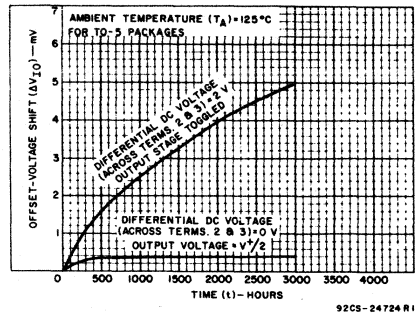


Fig.14 — Typical incremental offset-voltage shift vs operating life.

OFFSET-VOLTAGE NULLING

The input-offset voltage can be nulled by connecting a 10-kΩ potentiometer between terminals 1 and 5 and returning its wiper arm to terminal 4, see Fig.15a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig.15b, to optimize its utilization range are given in the table "Typical Electrical Characteristics" shown in this bulletin.

An alternate system is shown in Fig.15c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

LOW-VOLTAGE OPERATION

Operation at total supply voltages as low as 4 volts is possible with the CA3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low-voltage limitation occurs when the upper extreme of the input common-mode voltage range extends down to the voltage at terminal 4. This limit is reached at a total

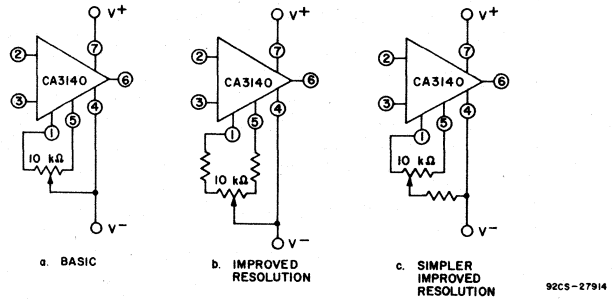
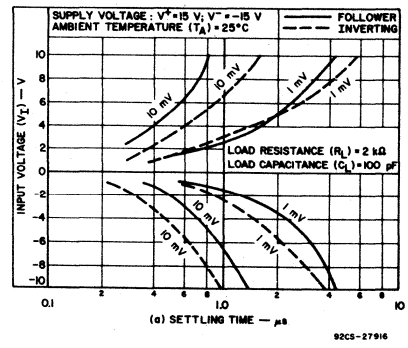


Fig.15 – Three offset-voltage nulling methods.

supply voltage just below 4 volts. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Fig.20 shows these characteristics and shows that with 2-volt dual supplies, the lower extreme of the input common-mode voltage range is below ground potential.



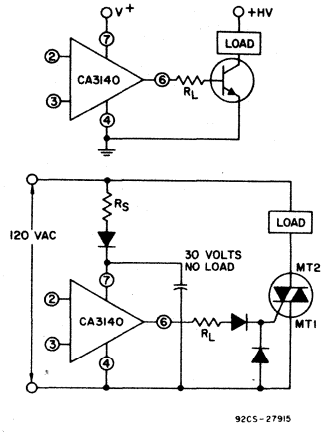
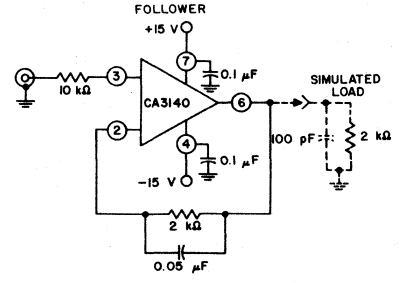


Fig.16 – Methods of utilizing the $V_{CE(sat)}$ sinking-current capability of the CA3140 series.



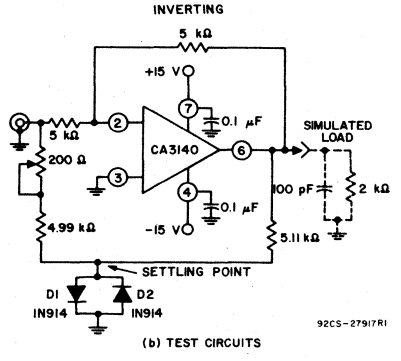


Fig.17 – Input voltage vs settling time.

BANDWIDTH AND SLEW RATE

For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between terminals 1 and 8 can reduce the open-loop −3 dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Fig.17 shows the typical settling time required to reach 1 mV or 10 mV of the final value for various levels of large signal inputs for the voltage-follower and inverting unity-gain amplifiers. The exceptionally fast setting time characteristics are largely due to the high combination of high gain and wide bandwidth of the CA3140; as shown in Fig. 18.

INPUT CIRCUIT CONSIDERATIONS

As mentioned previously, the amplifier inputs can be driven below the terminal 4 potential, but a series current-limiting re-

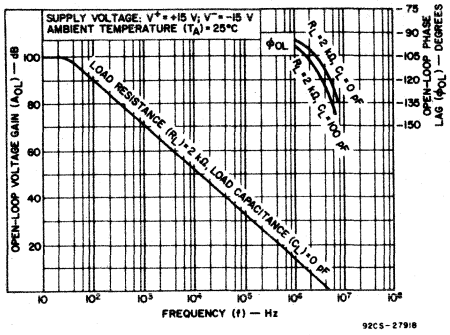


Fig.18 — Open-loop voltage gain and phase lag vs frequency.

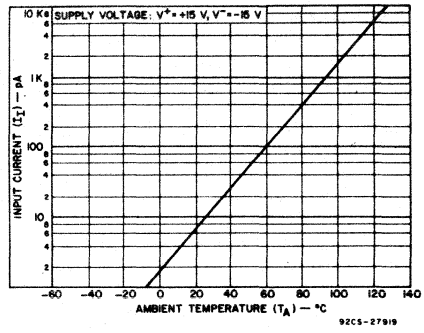


Fig.19 — Input current vs ambient temperature.

sistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3140 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig.19 shows typical input-terminal current versus ambient temperature for the CA3140.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Fig.14 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of 125°C (for TO-5); at lower temperatures (TO-5 and plastic), for example, at 85°C, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetircal, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar a transistor input stage.

SUPER SWEEP FUNCTION GENERATOR

A function generator having a wide tuning range is shown in Fig.21. The 1,000,000/1

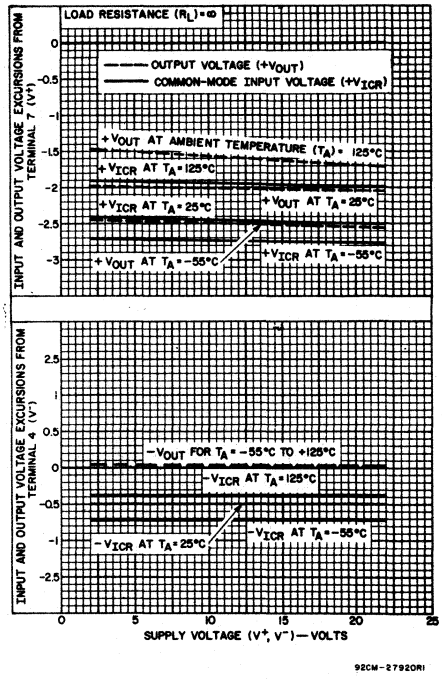


Fig.20 — Output-voltage-swing capability and common-mode input-voltage range vs supply voltage and temperature.

adjustment range is accomplished by a single variable potentiometer or by an auxiliary sweeping signal. The CA3140 functions as a non-inverting read-out amplifier of the triangular signal developed across the integrating capacitor network connected to the output of the CA3080A current source.

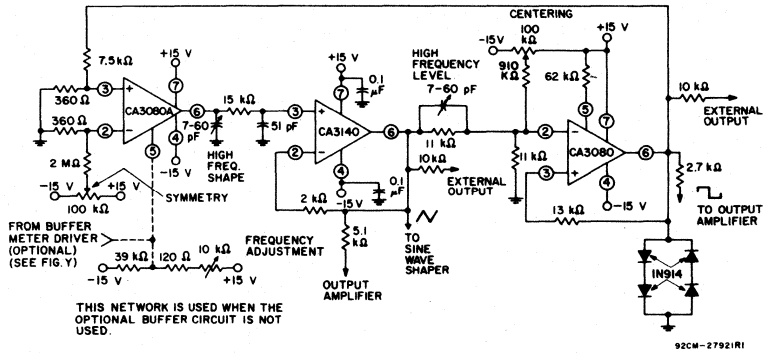
Buffered triangular output signals are then applied to a second CA3080 functioning as a high-speed hysteresis switch. Output from the switch is returned directly back to the

input of the CA3080A current source, thereby, completing the positive feedback loop.

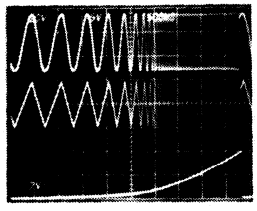
The triangular output level is determined by the four 1N914 level-limiting diodes of the second CA3080 and the resistor-divider network connected to terminal No.2 (input) of the CA3080. These diodes establish the input trip level to this switching stage and, therefore, indirectly determine the amplitude of the output triangle.

Compensation for propagation delays around the entire loop is provided by one adjustment on the input of the CA3080. This adjustment, which provides for a constant generator amplitude output, is most easily made while the generator is sweeping. High-frequency ramp linearity is adjusted by the single 7-to-60 pF capacitor in the output of the CA3080A.

It must be emphasized that only the CA-3080A is characterized for maximum output linearity in the current-generator function.



(a) Circuit



TOP TRACE: OUTPUT AT JUNCTION OF 2.7 Ω AND 51 Ω RESISTORS 5 V/DIV AND 500 ms/DIV
CENTER TRACE: EXTERNAL OUTPUT OF TRIANGULAR FUNCTION GENERATOR 2 V/DIV AND 500 ms/DIV
BOTTOM TRACE: OUTPUT OF "LOG" GENERATOR 10 V/DIV AND 500 ms/DIV

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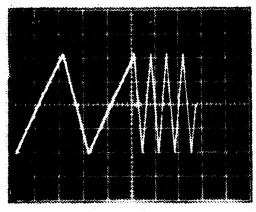
(b1) Function generator sweeping



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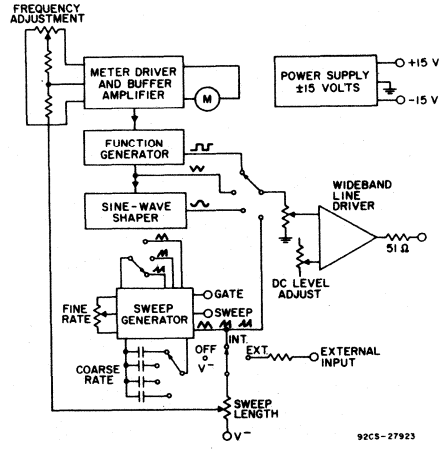
(b2) Function generator with fixed frequencies



(c) Interconnections

1V/DIV and 1 sec/DIV

Three tone test signals, highest frequency ⩾ 0.5 MHz. Note the slight assymmetry at the three-second/cycle signal. This assymmetry is due to slightly different positive and negative integration from the CA3080A and from the pc board and component leakages at the 100-pA level.

Fig.21 – Function generator.

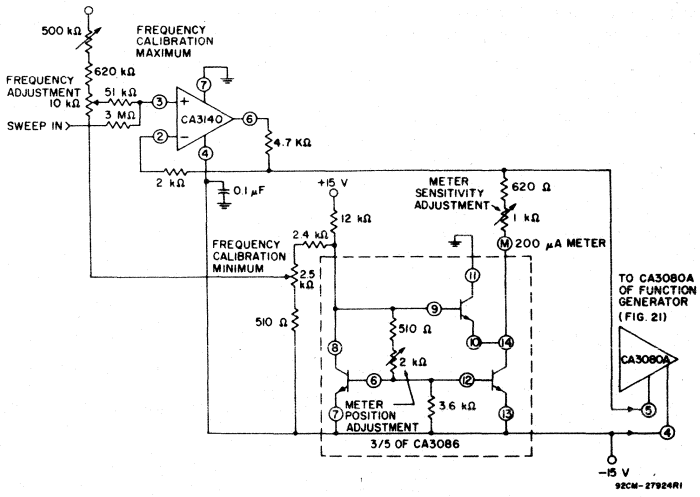


Fig. 22 – Meter driver and buffer amplifier.

METER DRIVER AND BUFFER AMPLIFIER

Fig. 22 shows the CA3140 connected as a meter driver and buffer amplifier. Low driving impedance is required of the CA-3080A current source to assure smooth operation of the Frequency Adjustment Control. This low-driving impedance requirement is easily met by using a CA3140 connected as a voltage follower. Moreover, a meter may be placed across the input to the CA3080A to give a logarithmic analog indication of the function generators frequency.

Analog frequency readout is readily accomplished by the means described above because the output current of the CA3080A varies approximately one decade for each 60-mV change in the applied voltage, V_{ABC} (voltage between terminals 5 and 4 of the CA3080A of the function generator). Therefore, six decades represent 360-mV change in V_{ABC}.

Now, only the reference voltage must be established to set the lower limit on the meter. The three remaining transistors from the CA3086 Array used in the sweep generator are used for this reference voltage. In addition, this reference generator arrangement tends to track ambient temperature variations, and thus compensates for the effects of the normal negative temperature coefficient of the CA3080A V_{ABC} terminal voltage.

Another output voltage from the reference generator is used to insure temperature tracking of the lower end of the Frequency Adjustment Potentiometer. A large series resistance simulates a current source, assuring similar temperature coefficients at both ends of the Frequency Adjustment Control.

To calibrate this circuit, set the Frequency Adjustment Potentiometer at its low end. Then adjust the Minimum Frequency Calibration Control for the lowest frequency. To establish the upper frequency limit, set the Frequency Adjustment Potentiometer to its upper end and then adjust the Maximum Frequency Calibration Control for the maximum frequency. Because there is interaction among these controls, repetition of the adjustment procedure may be necesary.

Two adjustments are used for the meter. The meter sensitivity control sets the meter-scale width of each decade, while the meter position control adjusts the pointer on the scale with negligible effect on the sensitivity adjustment. Thus, the meter sensitivity adjustment control calibrates the meter so that it deflects 1/6 of full scale for each decade change in frequency.

SINE-WAVE SHAPER

The circuit shown in Fig. 23 uses a CA3140 as a voltage follower in combination with diodes from the CA3019 Array to convert the triangular signal from the function generator to a sine-wave output signal having typically less than 2% THD. The basic zero-crossing slope is established by the 10-kΩ potentiometer connected between terminals 2 and 6 of the CA3140 and the 9.1-kΩ resistor and 10-kΩ potentiometer from terminal 2 to ground. Two break points are established by diodes D_1 through D_4. Positive feedback via D_5 and D_6 establishes the zero slope at the maximum and minimum levels of the sine wave. This technique is necessary because the voltage-follower configuration approaches unity gain rather than the zero gain required to shape the sine wave at the two extremes.

CA3140, CA3140A, CA3140B Types

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine-wave generator. The initial slope is adjusted with the potentiometer R_1, followed by an adjustment of R_2. The final slope is established by adjusting R_3, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessarv

SWEEPING GENERATOR

Fig. 24 shows a sweeping generator. Three CA3140's are used in this circuit. One CA3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third CA3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

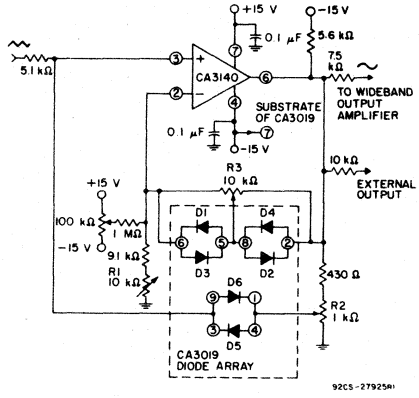


Fig. 23 – Sine-wave shaper.

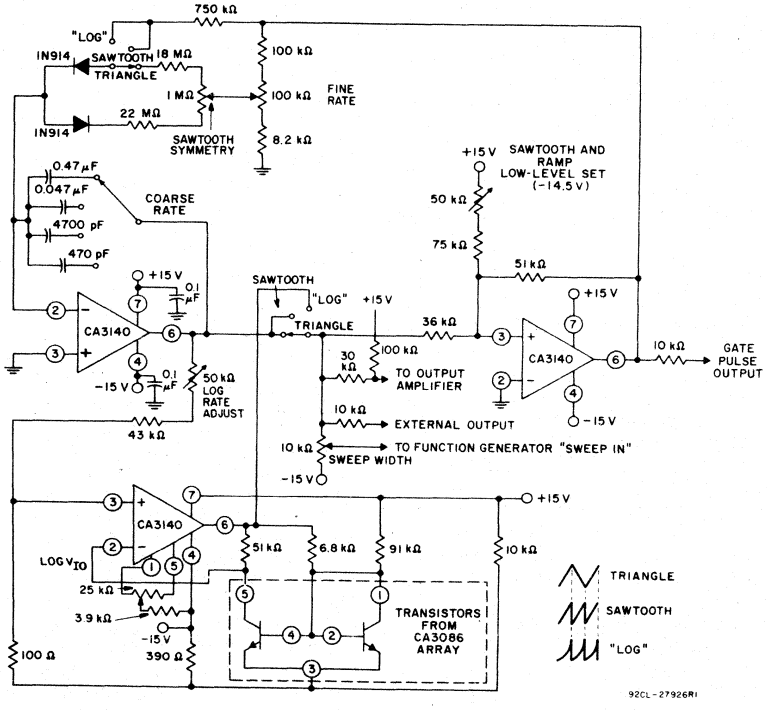


Fig. 24 – Sweeping generator.

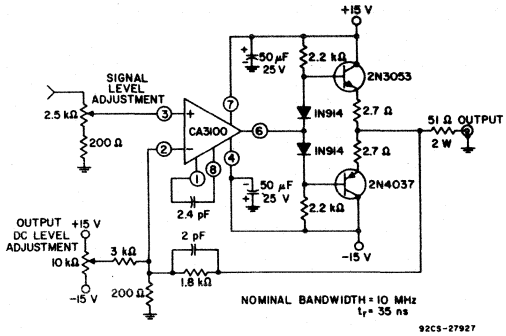


Fig. 25 – Wideband output amplifier.

WIDEBAND OUTPUT AMPLIFIER

Fig. 25 shows a high-slew-rate, wideband amplifier suitable for use as a 50-ohm transmission-line driver. This circuit, when used in conjunction with the function generator and sine-wave shaper circuits shown in Figs. 21 and 23 provides 18 volts peak-to-peak output open-circuited, or 9 volts peak-to-peak output when terminated in 50 ohms. The slew rate required of this amplifier is 28 volts/μs (18 volts peak-to-peak x π x 0.5 MHz).

POWER SUPPLIES

High input-impedance, common-mode capability down to the negative supply and high output-drive current capability are key factors in the design of wide-range output-voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0 to 24 volts.

Unlike many regulator systems using comparators having a bipolar transistor-input stage, a high-impedance reference-voltage divider from a single supply can be used in connection with the CA3140 (see Fig. 26).

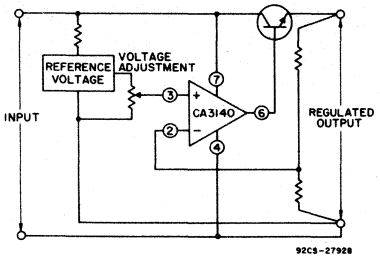


Fig. 26 – Basic single-supply voltage regulator showing voltage-follower configuration.

Essentially, the regulators, shown in Figs. 27 and 28, are connected as non-inverting power operational amplifiers with a gain of 3.2. An 8-volt reference input yields a maximum output voltage slightly greater than 25 volts. As a voltage follower, when the reference input goes to 0 volts the output will be 0 volts. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high I_{CBO} levels will also prevent the output voltage from reaching zero because there is a finite voltage drop (V_{CE}sat) across the output of the CA3140 (see Fig.13). This saturation voltage level may indeed set the lowest voltage obtainable.

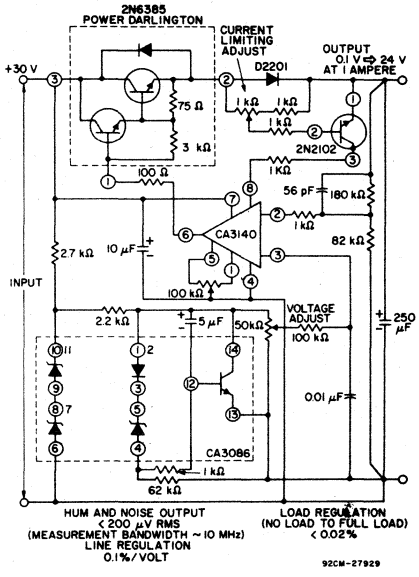


Fig. 27 – Regulated power supply.

The high impedance presented by terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the CA3140 in the event of unusual input or output transients on the supply-rail.

Figs. 27 and 28, show circuits in which a D2201 high-speed diode is used for the current sensor. This diode was chosen for its slightly higher forward-voltage drop characteristic thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1 ampere at 1 volt forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small-signal reference amplifier in the proximity of the current-sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode. In spite of those limitations, the current limiting point can easily be adjusted over the range from 10 mA to 1 ampere with a single adjustment potentiometer. If the temperature stability of the current-limiting system is a serious consideration, the more usual current-sampling resistor-type of circuitry should be employed.

A power Darlington transistor (in a heat sink TO-3 case), is used as the series-pass element for the conventional current-limiting system, Fig. 27, because high-power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat-sink VERSAWATT transistor is used as the series-pass element in the foldback current system, Fig.28, since dissipation levels will only approach 10 watts. In this system, the D2201 diode is used for current sampling. Foldback is provided by the 3 kΩ and 100 kΩ divider network connected to the base of the current-sensing transistor.

Both regulators, Figs. 27 and 28, provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200 μV as read with a meter having a 10-MHz bandwidth.

Fig.31 (a) shows the turn ON and turn OFF characteristics of both regulators. The slow turn-on rise is due to the slow rate of rise of the reference voltage. Fig. 29 (b) shows the transient response of the regulator with the switching of a 20-Ω load at 20 volts output.

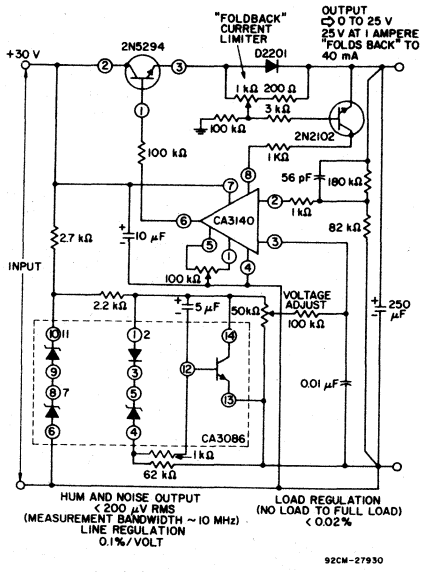
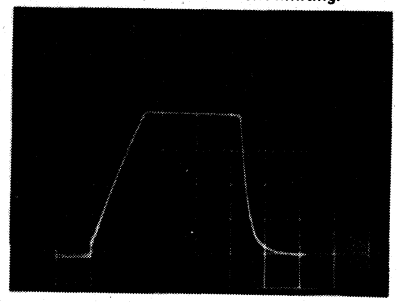
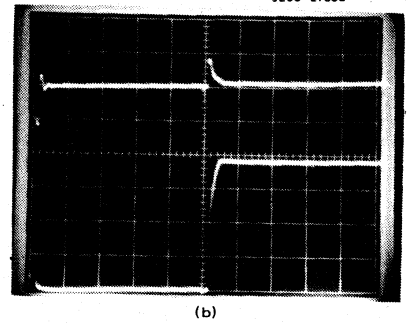


Fig. 28 – Regulated power supply with "foldback" current limiting.



(a)

SUPPLY TURN-ON AND TURN-OFF CHARACTERISTICS
(5 VOLTS / DIV. AND 1 s/DIV.)
92CS-27882



(b)

TRANSIENT RESPONSE
TOP TRACE : OUTPUT VOLTAGE
(200 mV/DIV AND 5 μs/DIV)
BOTTOM TRACE : COLLECTOR OF LOAD SWITCHING TRANSISTOR,
LOAD = 1 AMPERE
(5 VOLTS/DIV AND 5 μs/DIV)
92CS-27881

Fig. 29 – Waveforms of dynamic characteristics of power supply currents shown in Figs. 29 and 30.

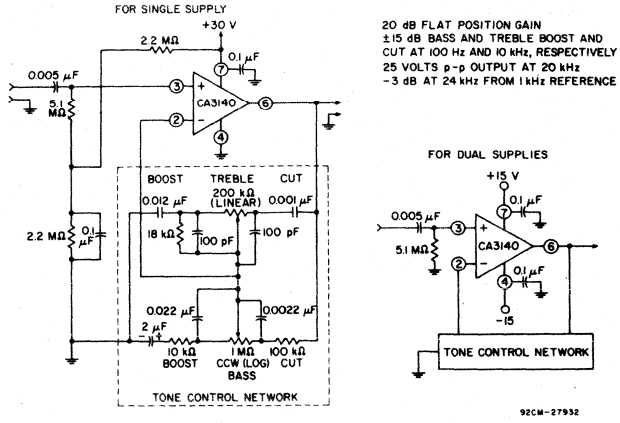


Fig. 30 – Tone control circuit using CA3130 series (20-dB midband gain).

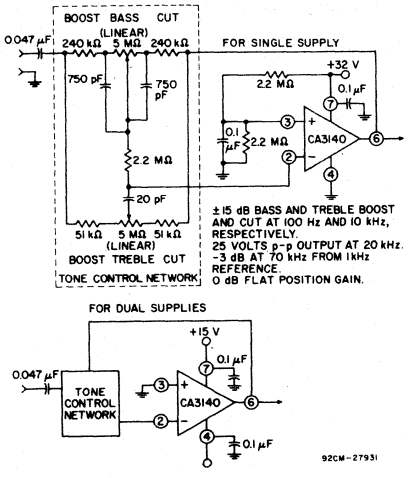


Fig. 31 – Baxandall tone control circuit using CA3140 series.

TONE CONTROL CIRCUITS

High-slew-rate, wide-bandwidth, high-output voltage capability and high input impedance are all characteristics required of tone-control amplifiers. Two tone control circuits that exploit these characteristics of the CA3140 are shown in Figs. 30 and 31.

The first circuit, shown in Fig. 31, is the Baxandall tone-control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the CA3140 makes possible the use of low-cost, low-value, small-size capacitors, as well as reduced load of the driving stage.

Bass treble boost and cut are ± 15 dB at 100 Hz and 10 kHz, respectively. Full peak-to-peak output is available up to at least 20 kHz due to the high slew rate of the CA3140. The amplifier gain is –3 dB down from its "flat" position at 70 kHz.

Fig. 30 shows another tone-control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20-dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from terminal No.3 to ground. A detailed analysis of this circuit is given in "An IC Operational Transconductance Amplifier (OTA) With Power Capability" by L, Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No.3, August, 1972.

WIEN BRIDGE OSCILLATOR

Another application of the CA3140 that makes excellent use of its high input-impedance, high-slew-rate, and high-voltage qualities is the Wien Bridge sine-wave oscillator. A basic Wien Bridge oscillator is shown in Fig. 32. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency equation reduces to the familiar $f = 1/2\pi RC$ and the gain required for oscillation, A_{OSC} is equal to 3. Note that if C_2 is increased by a factor of four and R_2 is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus per-

mitting a potentially higher operating frequency closer to the gain-bandwidth product of the CA3140.

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, R_S, is commonly replaced with some variable resistance element. Thus, through some control means, the value of R_S is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance is made to increase as the output amplitude is increased are a few of the elements often utilized.

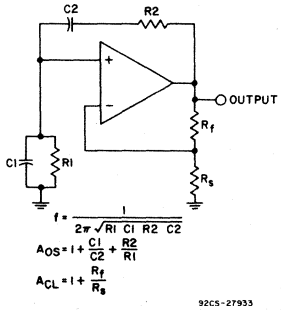


Fig. 32 – Basic Wien bridge oscillator circuit using an operational amplifier.

Fig. 33 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor (R_f of Fig. 32). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1-μF polycarbonate capacitors and 22 MΩ for the frequency determining network, the operating frequency is 0.007 Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of 180 kHz will reach a slew rate of approximately 9 volts/μs when its amplitude is 16 volts peak-to-peak.

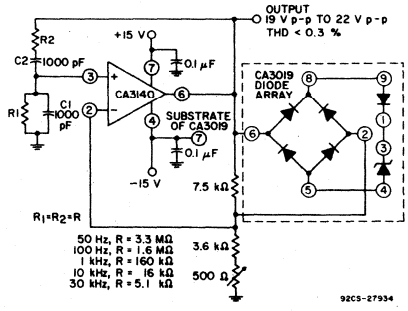


Fig. 33 – Wien bridge oscillator circuit using CA3140 series.

SIMPLE SAMPLE-AND-HOLD SYSTEM

Fig. 34 shows a very simple sample-and-hold system using the CA3140 as the readout amplifier for the storage capacitor. The CA3080A serves as both input buffer amplifier and low feed-through transmission switch.* System offset nulling is accomplished with the CA3140 via its offset nulling terminals. A typical simulated load of 2 kΩ and 30 pF is shown in the schematic.

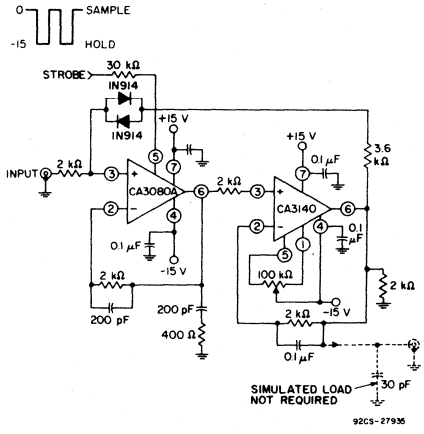
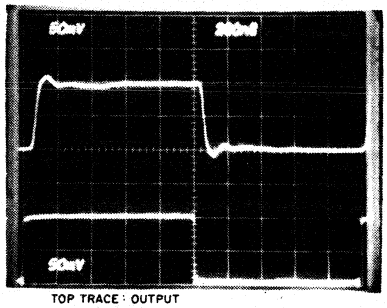


Fig. 34 – Sample- and hold circuit.

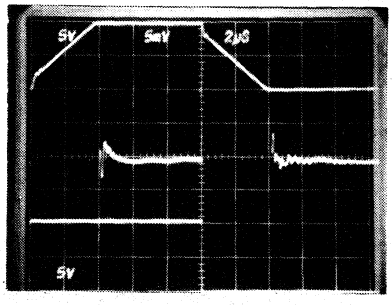
In this circuit, the storage compensation capacitance (C_1) is only 200 pF. Larger value capacitors provide longer "hold" periods but with slower slew rates. The slew rate $\frac{dv}{dt} = \frac{i}{c} = 0.5$ mA/200 pF = 2.5 V/μs.

* ICAN-6668 "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

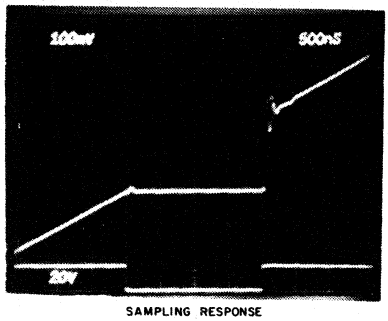
Pulse "droop" during the hold interval is 170 pA/200 pF which is = 0.85 μV/μs; (i.e., 170 pA/200 pF). In this case, 170 pA represents the typical leakage current of the CA3080A when strobed off. If C_1 were increased to 2000 pF, the "hold-droop" rate will decrease to 0.085 μV/μs, but the slew rate would decrease to 0.25 V/μs. The parallel diode network connected between terminal 3 of the CA3080A and terminal 6 of the CA3140 prevents large input-signal feed-through across the input terminals of the CA3080A to the 200 pF storage capacitor when the CA3080A is strobed off. Fig. 35 shows dynamic characteristic waveforms of this sample-and-hold system.



TOP TRACE: OUTPUT
(50 mV/DIV. AND 200 ns/DIV.)
BOTTOM TRACE: INPUT
(50 mV/DIV. AND 200 ns/DIV.)
92CS-27883



LARGE-SIGNAL RESPONSE AND SETTLING TIME
TOP TRACE: OUTPUT SIGNAL
(5 V/DIV. AND 2 μs/DIV.)
BOTTOM TRACE: INPUT SIGNAL
(5 V/DIV. AND 2 μs/DIV.)
CENTER TRACE: DIFFERENCE OF INPUT AND OUTPUT SIGNALS THROUGH TEKTRONIX AMPLIFIER 7A13
(5 mV/DIV. AND 2 μs/DIV.) 92CS-27884



SAMPLING RESPONSE
TOP TRACE: SYSTEM OUTPUT
(100 mV/DIV. AND 500 ns/DIV.)
BOTTOM TRACE: SAMPLING SIGNAL
(20 V/DIV. AND 500 ns/DIV.)
92CS-27885

Fig. 35 – Sample- and hold system dynamic characteristics waveforms.

CURRENT AMPLIFIER

The low input-terminal current needed to drive the CA3140 makes it ideal for use in current-amplifier applications such as the one shown in Fig. 36.● In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R2/R1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100 nA, with values shown, the load current presented to the supply will be 100 μA; a much easier current to measure in many systems.

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output-load capacitance and the potential oscillation in this situation. Essentially, the necessary high-frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

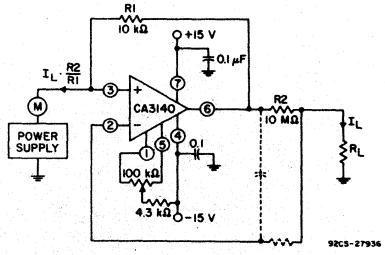


Fig. 36 – Basic current amplifier for low-current measurement systems.

Fig. 37 shows a single-supply, absolute-value, ideal full-wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No.6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3140 functions as a normal inverting amplifier with a gain equal to −R2/R1. When the equality of the two equations shown in Fig. 37 is satisfied, the full-wave output is symmetrical.

● "Operational Amplifiers Design and Applications", J. G. Graeme, McGraw-Hill Book Company, page 308 – "Negative Immittance Converter Circuits".

CA3140, CA3140A, CA3140B Types

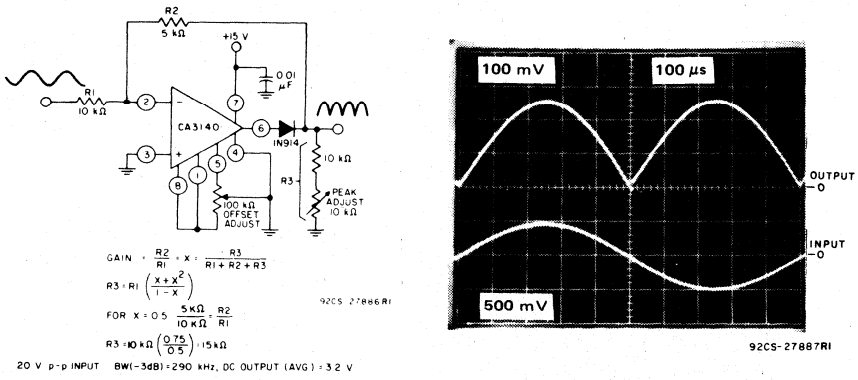


Fig. 37 – Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.

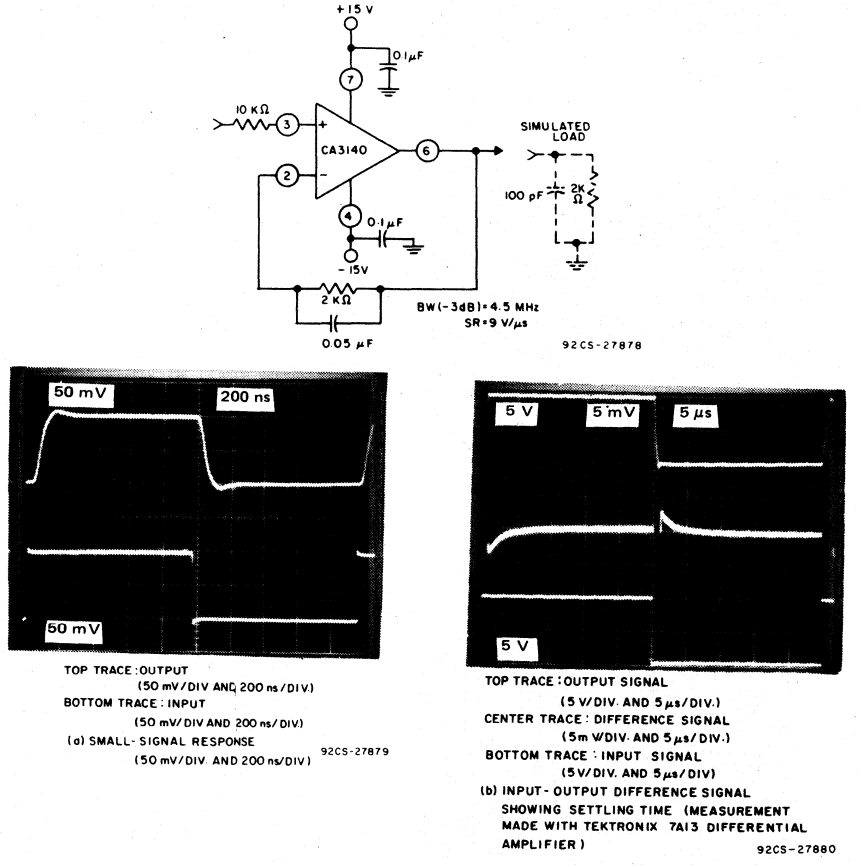


Fig. 38 – Split-supply voltage-follower test circuit and associated waveforms.

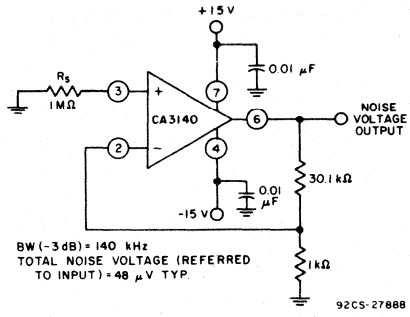
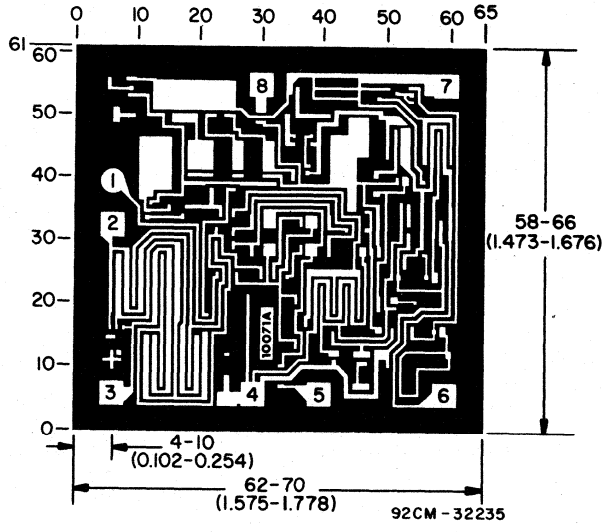


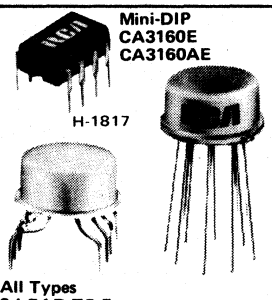
Fig. 39 – Test circuit amplifier (30-dB gain) used for wideband noise measurement.



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3160, CA3160A, CA3160B Types



BiMOS Operational Amplifiers

With MOS/FET Input, COS/MOS Output

FEATURES:

- *Similar to CA3130 but has internal compensation*
- *MOS/FET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 × 10^{12}Ω) typ.
  very low I_I = 5 pA typ. at 15-V operation
  2 pA typ. at 5-V operation
- *Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *COS/MOS output stage permits signal swing to either (or both) supply rails*

} *Ideal for single-supply applications*

The RCA-CA3160T, CA3160S, CA3160E; CA3160AT, CA3160AS, CA3160AE; and CA3160BT, CA3160BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip. The CA3160 series circuits are frequency-compensated versions of the popular CA3130 series.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3160 Series circuits operate at supply voltages ranging from 5 to 16 volts, or +2.5 to +8 volts when using split supplies, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3160 series is supplied in standard 8-lead TO-5 style packages (T suffix) and 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" packages (S suffix). The CA3160 is available in chip form (H suffix).

- *Low V_{IO}: 2 mV max. (CA3160B)*
- *Wide BW: 4 MHz typ. (unity-gain crossover)*
- *High SR: 10 V/μs typ. (unity-gain follower)*
- *High output current (I_O): 20 mA typ.*
- *High A_{OL}: 320,000 (110 dB) typ.*
- *Internal phase compensation for unity gain (With terminal access for supplementary external phase compensation network if desired)*

APPLICATIONS:

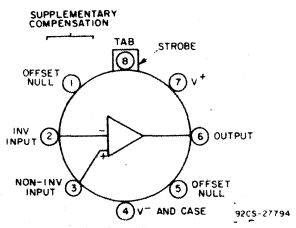
- *Ground-referenced single-supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *Ideal interface with digital COS/MOS*
- *High-input-impedance wideband amplifiers*
- *Voltage followers (e.g., follower for single-supply D/A converter)*
- *Wien-Bridge oscillators*
- *Voltage-controlled oscillators*
- *Photo-diode sensor amplifiers*

The CA3160A and CA3160 are also available in the 8-lead dual-in-line plastic package (Mini-DIP-E suffix). All types operate over the full military-temperature range of -55° C to +125° C. The CA3160B is intended for applications requiring premium-grade specifications. The CA3160A offers superior input characteristics over those of the CA3160.

CA3160, CA3160A, CA3160B Types

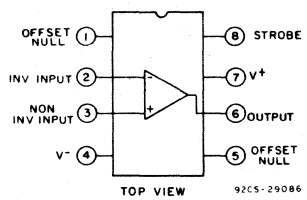
ELECTRICAL CHARACTERISTICS at T_A=25°C, V^+=15 V, V^- = 0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS									Units
	CA3160B (T, S)			CA3160A (T, S, E)			CA3160 (T, S, E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.8	2	–	2	5	–	6	15	mV
Input Offset Current, $\|I_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	–	5	20	–	5	30	–	5	50	pA
Large-Signal Voltage Gain, A_{OL}	100 k	320 k	–	50 k	320 k	–	50 k	320 k	–	V/V
V_O=10 V_{p-p}, R_L=2 kΩ	100	110	–	94	110	–	94	110	–	dB
Common-Mode Rejection Ratio, CMRR	86	100	–	80	95	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR}	0	−0.5 to 12	10	0	−0.5 to 12	10	0	−0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	–	32	100	–	32	150	–	32	320	μV/V
Maximum Output Voltage:										
At R_L=2 kΩ V_{OM}^+	12	13.3	–	12	13.3	–	12	13.3	–	V
At R_L=2 kΩ V_{OM}^-	–	0.002	0.01	–	0.002	0.01	–	0.002	0.01	V
At R_L=∞ V_{OM}^+	14.99	15	–	14.99	15	–	14.99	15	–	V
At R_L=∞ V_{OM}^-	–	0	0.01	–	0	0.01	–	0	0.01	V
Maximum Output Current: I_{OM}^+ (Source) @ V_O = 0 V	12	22	45	12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O = 15 V	12	20	45	12	20	45	12	20	45	mA
Supply Current, I^+: V_O=7.5 V, R_L=∞	–	10	15	–	10	15	–	10	15	mA
V_O = 0 V, R_L = ∞	–	2	3	–	2	3	–	2	3	mA
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$*	–	5	–	–	6	–	–	8	–	μV/°C



TOP VIEW

S and T Suffixes



E Suffix

CA3160 Series devices have an on-chip frequency-compensation network. Supplementary phase-compensation or frequency roll-off (if desired) can be connected externally between terminals 1 and 8.

Fig. 1 – Functional diagrams of the CA3160 Series.

CA3160, CA3160A, CA3160B Types

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS		CA3160B (T, S)	CA3160A (T, S, E)	CA3160 (T, S, E)	UNITS
	$V^+ = +7.5$ V, $V^- = -7.5$ V, $T_A = 25^oC$ (Unless Otherwise Specified)					
Input Offset Voltage Adjustment Range	10 kΩ across Terms. 4 and 5 or 4 and 1		±22	±22	±22	mV
Input Resistance, R_I			1.5	1.5	1.5	TΩ
Input Capacitance, C_I	f = 1 MHz		4.3	4.3	4.3	pF
Equivalent Input Noise Voltage, e_n	BW= 0.2 MHz	R_S=1 MΩ	40	40	40	μV
		R_S=10MΩ	50	50	50	
Equivalent Input Noise Voltage, e_n	R_S= 100 Ω	1 kHz	72	72	72	$nV\sqrt{Hz}$
		10 kHz	30	30	30	
Unity Gain Crossover Frequency, f_T			4	4	4	MHz
Slew Rate, SR:			10	10	10	V/μs
Transient Response: Rise Time, t_r	C_L = 25 pF, R_L = 2 kΩ (Voltage Follower)		0.09	0.09	0.09	μs
Overshoot			10	10	10	%
Settling Time (4 V_{p-p} Input to <0.1%)			1.8	1.8	1.8	μs

CHARACTERISTIC	TEST CONDITIONS	CA3160B (T, S)	CA3160A (T, S, E)	CA3160 (T, S, E)	UNITS
	$V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$ (Unless Otherwise Specified)				
Input Offset Voltage, V_{IO}		1	2	6	mV
Input Offset Current, I_{IO}		0.1	0.1	0.1	pA
Input Current, I_I		2	2	2	pA
Common-Mode Rejection Ratio, CMRR		100	90	80	dB
Large-Signal Voltage Gain, A_{OL}	$V_O = 4\ V_{p-p}$, R_L = 5 kΩ	100 k	100 k	100 k	V/V
		100	100	100	dB
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.8	0 to 2.8	0 to 2.8	V
Supply Current, I^+	V_O = 5 V, $R_L = \infty$	300	300	300	μA
	V_O = 2.5 V, $R_L = \infty$	500	500	500	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	200	μV/V

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC
INPUT VOLTAGE... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK −
UP TO 55°C ..... 630 mW
ABOVE 55°C .... Derate linearly 6.67 mW/°C
WITH HEAT SINK −
UP TO 90°C ..... 1 W
ABOVE 90°C ... Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:
OPERATING (All Types).... −55 to +125°C
STORAGE (All Types) ..... −65 to +150°C
OUTPUT SHORT-CIRCUIT
DURATION* ..... INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH
(1.59 ± 0.79 MM) FROM CASE
FOR 10 SECONDS MAX. ..... +265°C

*Short circuit may be applied to ground or to either supply.

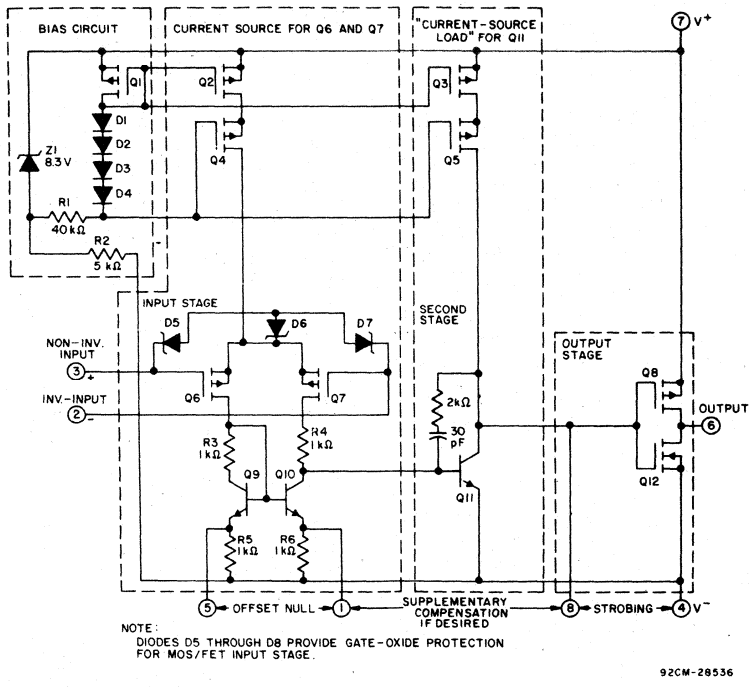


Fig.2 – Schematic diagram of the CA3160 Series.

CIRCUIT DESCRIPTION

Fig.3 is a block diagram of the CA3160 series COS/MOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3160 series circuits are ideal for single-supply operation. Three class A amplifier stages, having the individual gain capability and current consumption shown in Fig.3, provide the total gain of the CA3160. A biasing circuit provides two potentials for common use in the first and second stages. Terminals 8 and 1 can be used to supplement the internal phase compensation network if additional phase compensation or frequency roll-off is desired. Terminals 8 and 4 can also be used to strobe the output stage into a low quiescent current state. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply-rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive COS/MOS digital circuits in comparator applications).

CA3160, CA3160A, CA3160B Types

Input Stages – The circuit of the CA3160 is shown in Fig.2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4, are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D7 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

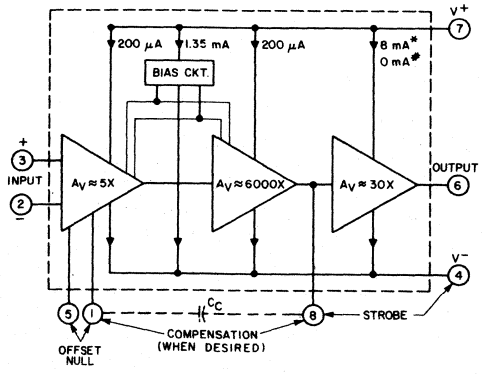
Second-Stage – Most of the voltage gain in the CA3160 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is described later. Miller Effect compensation (roll off) is accomplished by means of the 30-pF capacitor and 2-kΩ resistor connected between the base and collector of transistor Q11. These internal components provide sufficient compensation for unity gain operation in most applications. However, additional compensation, if desired, may be used between Terminals 1 and 8.

Bias-Source Circuit – At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Terminal 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage – The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig.6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

† For general information on the characteristics of COS/MOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "COS/MOS Transistor Array".



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15 V
* WITH INPUT TERMINALS BIASED SO THAT TERM. 6 POTENTIAL IS +7.5 V ABOVE TERM. 4.
* WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.

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Fig. 3 – Block diagram of the CA3160 Series.

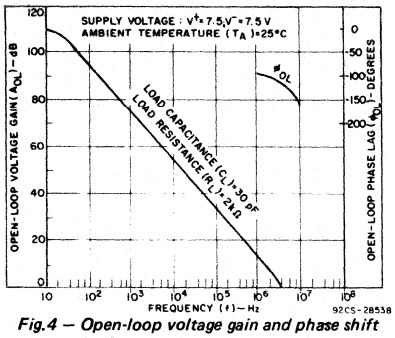


Fig.4 – Open-loop voltage gain and phase shift vs. frequency.

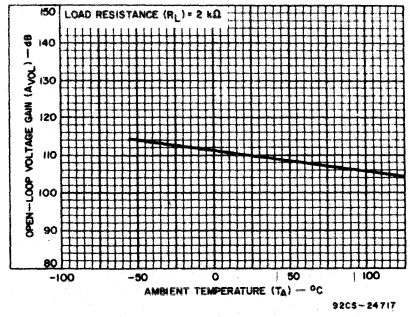


Fig.5 – Open-loop gain vs. temperature.

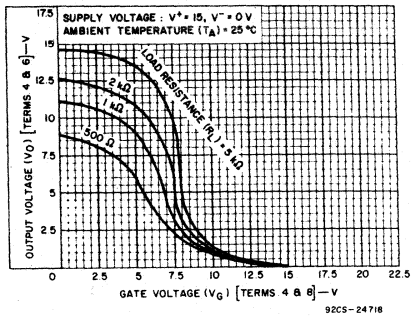


Fig.6 – Voltage transfer characteristics of COS/MOS output stage.

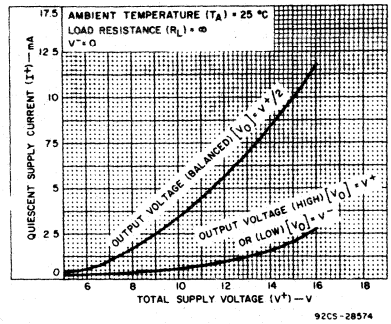


Fig.7 – Quiescent supply current vs. supply voltage.

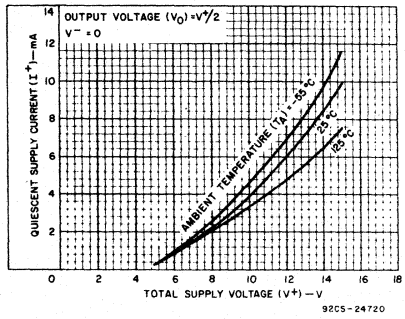


Fig.8 – Quiescent supply current vs. supply voltage at several temperatures.

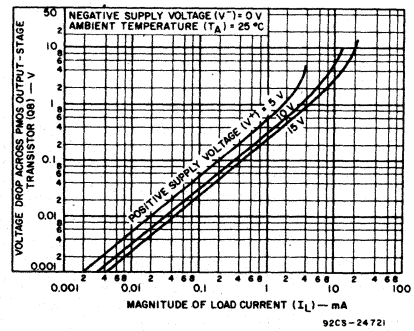


Fig.9 – Voltage across PMOS output transistor (Q8) vs. load current.

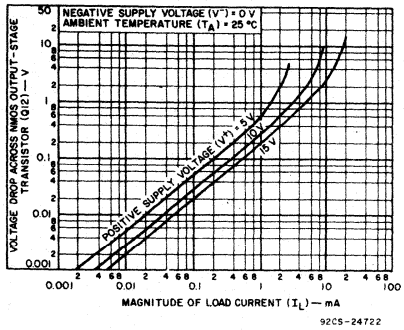


Fig.10 – Voltage across NMOS output transistor (Q12) vs. load current.

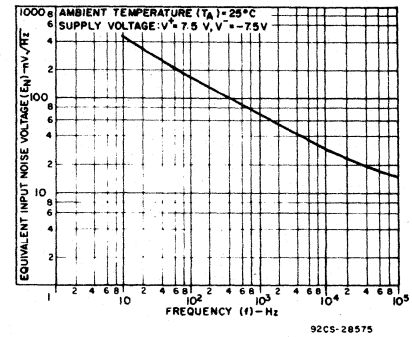


Fig.11 – Equivalent noise voltage vs. frequency.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3160 Series Op-Amps is typically 5 pA at T_A=25°C when Terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig. 12 contains

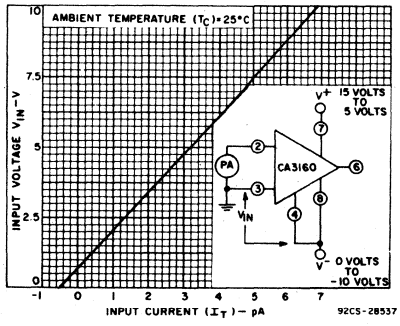


Fig. 12 – Input current vs. common-mode voltage.

data showing the variation of input current as a function of common-mode input voltage at T_A=25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3160 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Input-Current Variation with Temperature

The input current of the CA3160 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig. 13 provides data on the typical variation of input bias current as a function of temperature in the CA3160.

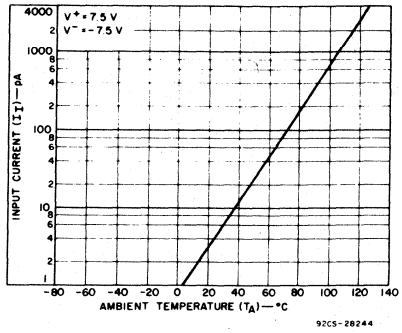


Fig. 13 – Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3160. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3160 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terminals 2 and 3. Fig. 14 shows typical data pertinent to shifts in offset voltage encountered with CA3160 devices in TO-5 packages during life testing. At lower temperatures (TO-5 and plastic) for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those en-

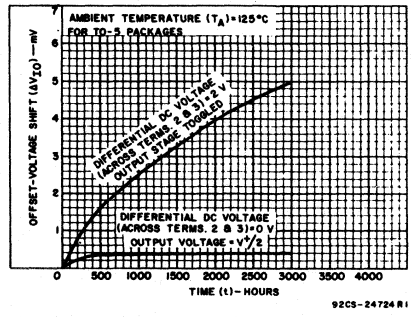
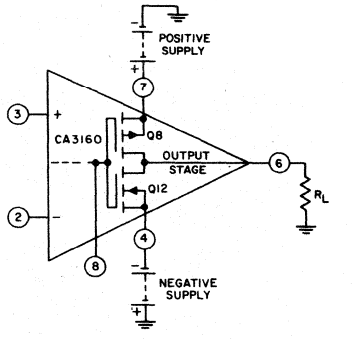


Fig. 14 – Typical incremental offset-voltage shift vs. operating life.

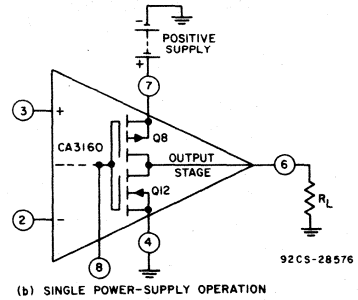
countered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output state is "toggled", e.g., as in comparator applications.

Power-Supply Considerations

Because the CA3160 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 15(a) and 15(b) show the CA3160 connected for both dual- and single-supply operation.



(a) DUAL POWER-SUPPLY OPERATION



(b) SINGLE POWER-SUPPLY OPERATION

Fig. 15 – CA3160 output stage in dual and single power-supply operation.

Dual-supply operation: When the output voltage at Terminal 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3160 operated under these conditions.

Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3160, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 15(a) shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L=\infty$, by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Terminal 6 and ground in the circuit of Fig. 15(b). Let it further be assumed again that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is a $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3160 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 40 μV when the test-circuit amplifier of Fig.16 is operated at a total supply voltage of 15 volts. This value of

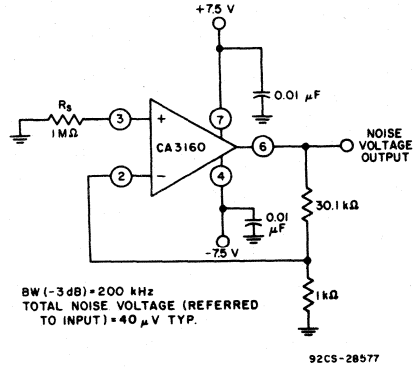
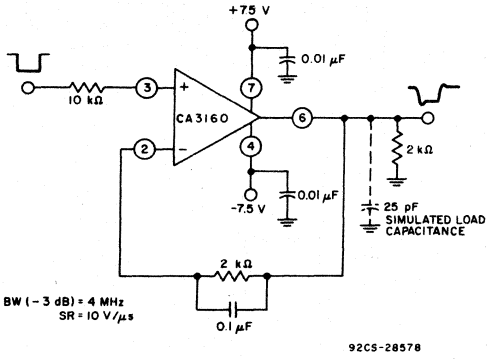
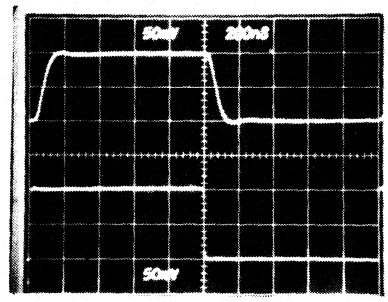


Fig. 16 – Test-circuit amplifier (30-dB gain) used for wideband noise measurements.

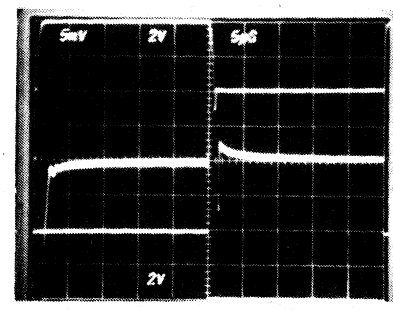
total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.



(a)



(b) *Small Signal Response*
Top Trace: Output
Bottom Trace: Input



(c) *Input-Output Difference Signal Showing Settling Time*
Top Trace: Output Signal
Center Trace: Difference Signal 5 mV/div
Bottom Trace: Input Signal

Fig. 17 – Split-supply voltage follower with associated waveforms.

TYPICAL APPLICATIONS

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3160, are particularly suited to service as voltage followers. Fig.17 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3160 in a split-supply configuration.

A voltage follower, operated from a single-supply, is shown in Fig.18 together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig.18b with input-signal ramping. The waveforms in Fig.18c show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig.18c also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3160 in a single-supply voltage-follower application.

9-Bit COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig.19. This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3160 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with COS/MOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig.19.

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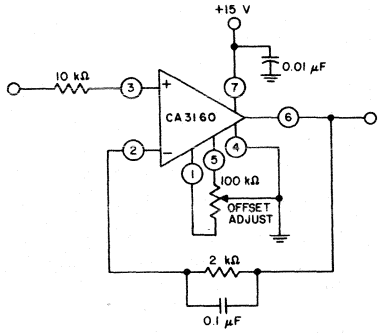
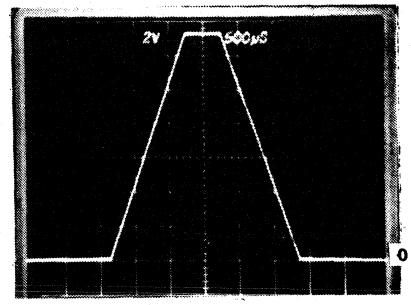
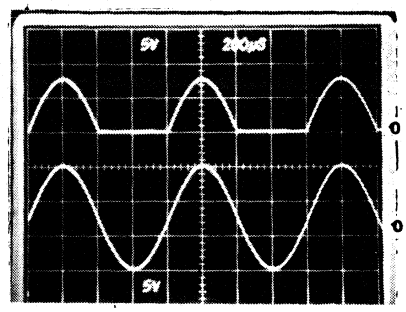
* "Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC", Application Note ICAN-6080.



(a)



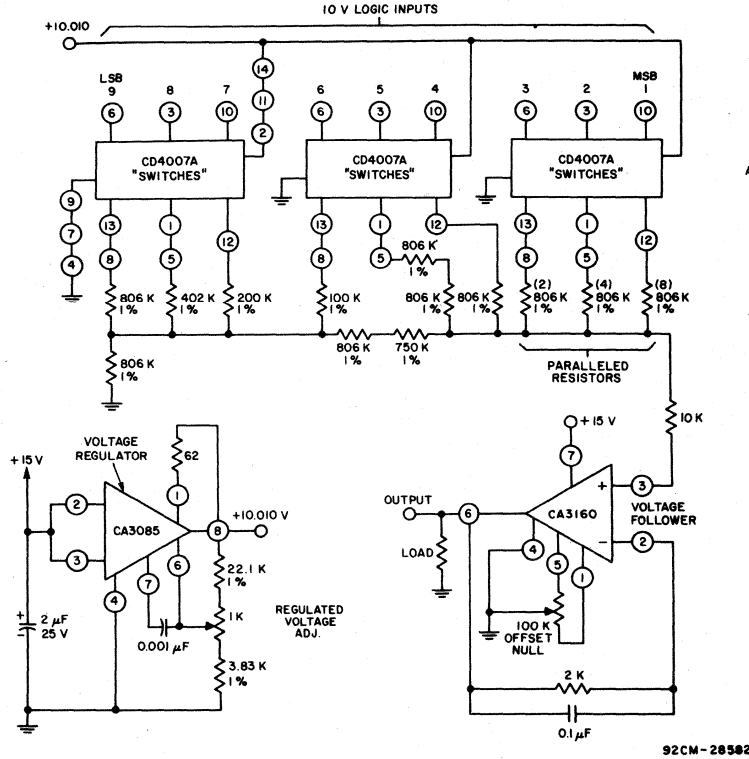
(b) Output signal with input-signal ramping.



92CS-28581R1

(c) Output-Waveform with Ground-Reference Sine-Wave Input
Top Trace: Output
Bottom Trace: Input

Fig.18 – Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig.9 in ICAN-6080.)



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS.

ALL RESISTANCES IN OHMS

Fig.19 – 9-bit DAC using COS/MOS digital switches and CA3160.

The circuit uses an R/2R voltage-ladder network, with the output-potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3160 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

Error-Amplifier in Regulated Power Supplies

The CA3160 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero.

The circuit shown in Fig.20 uses a CA3160 as an error amplifier in a continuously adjustable 1-ampere power supply. One of the key features of this circuit is its ability to regulate down to the vicinity of zero volts with only one dc power supply input.

An RC network, connected between the base of the output drive transistor and the input voltage, prevents "turn-on overshoot", a condition typical of many operational-amplifier regulator circuits. As the amplifier becomes operational, this RC network ceases to have any influence on the regulator performance.

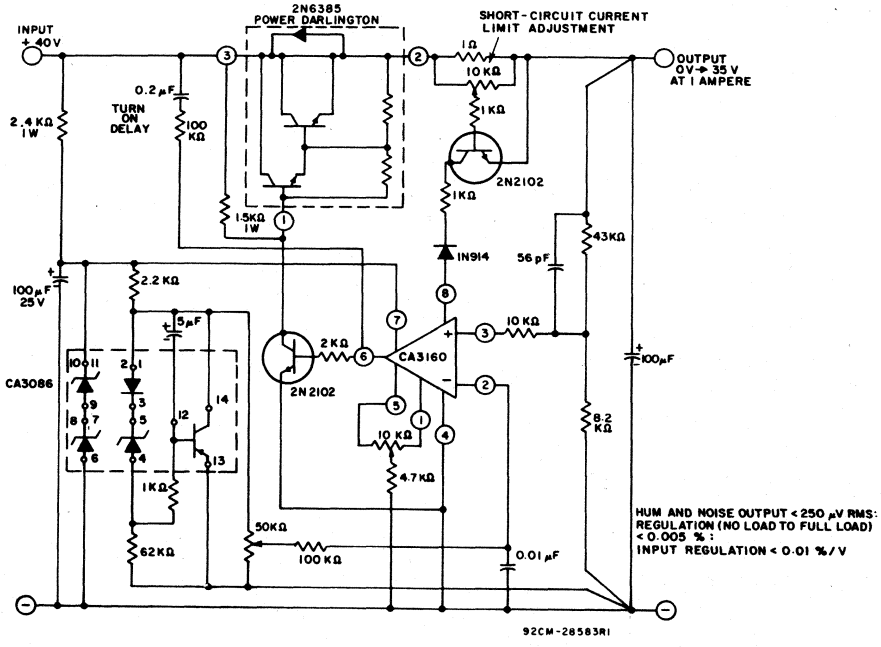


Fig.20 – Voltage regulator circuit (0.1 to 35 V at 1 A).

Precision Voltage-Controlled Oscillator

The circuit diagram of a precision voltage-controlled oscillator is shown in Fig.21. The oscillator operates with a tracking error in the order of 0.02 percent and a temperature coefficient of 0.01%/°C. A multivibrator (A_1) generates pulses of constant amplitude (V) and width (T_2). Since the output (terminal 6) of A_1 (a CA3130) can swing within about 10 millivolts of either supply-rail, the output pulse amplitude (V) is essentially equal to V+. The average output voltage ($E_{avg} = V\ T_2/T_1$) is applied to the non-inverting input terminal of comparator A_2 via an integrating network R_3, C_2. Comparator A_2 operates to establish circuit conditions such that $E_{avg} = V1$. This circuit condition is accomplished by feeding an output signal from terminal 6 of A_2 through R_4, D_4 to the inverting terminal (terminal 2) of A_1, thereby adjusting the multivibrator interval, T_3.

Voltmeter With High Input Resistance

The voltmeter circuit shown in Fig.22 illustrates an application in which a number of the CA3160 characteristics are exploited. Range-switch SW1 is ganged between input and output circuitry to permit selection of the proper output voltage for feedback to Terminal 2 via 10 KΩ current-limiting resistor. The circuit is powered by a single 8.4-volt mercury battery. With zero input signal, the circuit consumes somewhat less than 500 microamperes plus the meter current required to indicate a given voltage. Thus, at full-scale input, the total supply current rises to slightly more than 1500 microamperes.

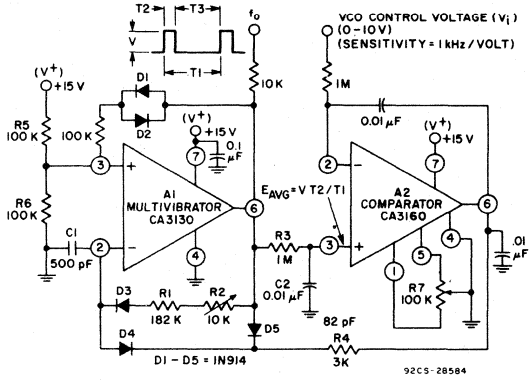


Fig.21 – Voltage-controlled oscillator.

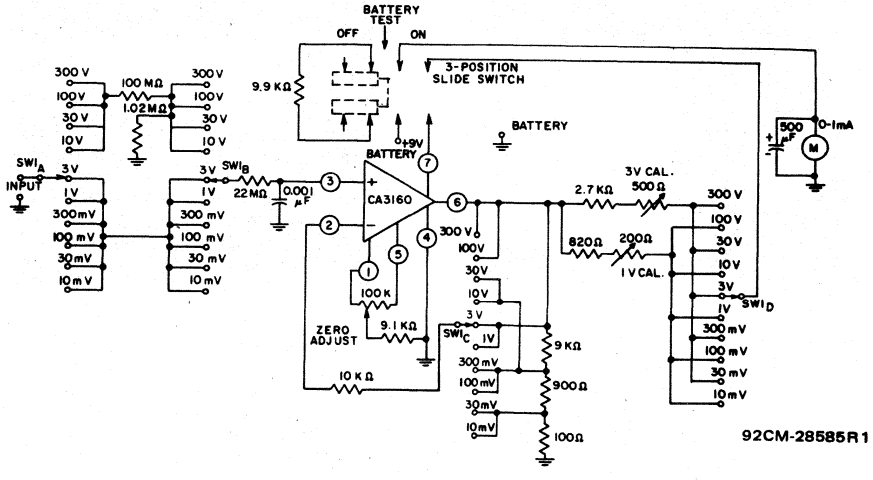


Fig.22 – High-input-resistance DC voltmeter.

CA3160, CA3160A, CA3160B Types

Function Generator

A function generator having a wide tuning range is shown in Fig.23. The adjustment range, in excess of 1,000,000/1, is accomplished by a single potentiometer. Three operational amplifiers are utilized: a CA3160 as a voltage follower, a CA3080 as a high-speed comparator, and a second CA3080A as a programmable current source. Three variable capacitors C1, C2, and C3 shape the triangular signal between 500 kHz and 1 MHz. Capacitors C4, C5, and the trimmer potentiometer in series with C5 maintain essentially constant (±10%) amplitude up to 1 MHz.

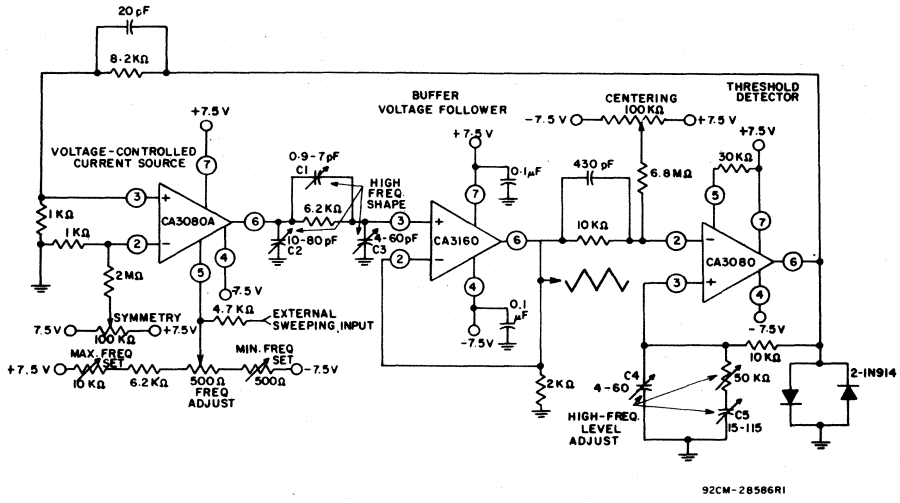
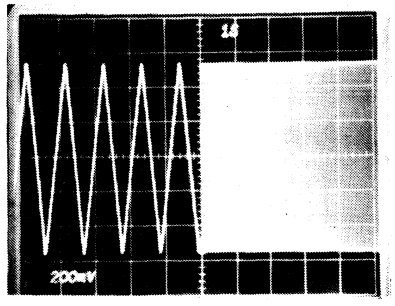
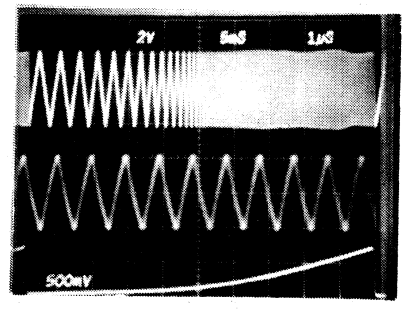


Fig.23(a) – 1,000,000/1 single-control function generator – 1 MHz to 1 Hz.



(b) – Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.

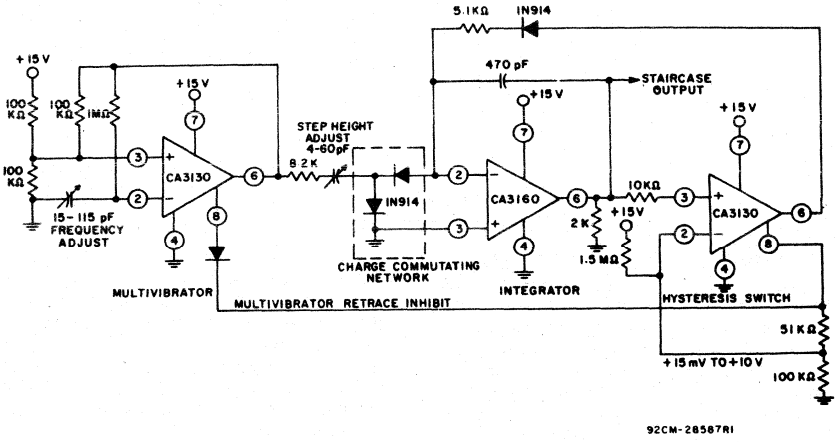


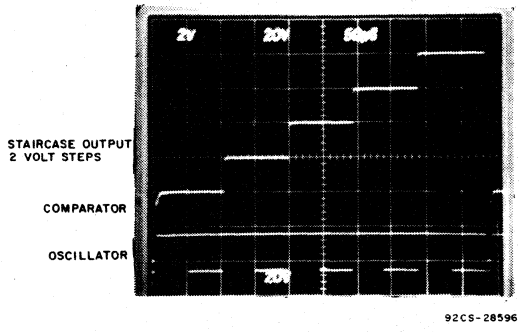
92CS-28588

(c) – Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

Staircase Generator

Fig.24 shows a staircase generator circuit utilizing three COS/MOS operational amplifiers. Two CA3130's are used; one as a multivibrator, the other as a hysteresis switch. The third amplifier, a CA3160, is used as a linear staircase generator.





(b) – Staircase Generator Waveform
Top Trace: Staircase Output
2 Volt Steps
Center Trace: Comparator
Bottom Trace: Oscillator

Picoammeter Circuit

Fig. 25 is a current-to-voltage converter configuration utilizing a CA3160 and CA3140 to provide a picoampere meter for ±3 pA full-scale meter deflection. By placing Terminals 2 and 4 of the CA3160 at ground potential, the CA3160 input is operated in the "guarded mode". Under this operating condition, even slight leakage resistance present between Terminals 3 and 2 or between Terminals 3 and 4 would result in zero voltage across this leakage resistance, thus substantially reducing the leakage current.

If the CA3160 is operated with the same voltage on input Terminals 3 and 2 as on Terminal 4, a further reduction in the input current to the less than one picoampere level can be achieved as shown in Fig. 12.

To further enhance the stability of this circuit, the CA3160 can be operated with its output (Terminal 6) near ground, thus markedly reducing the dissipation by reducing the supply current to the device.

The CA3140 stage serves as a X100 gain stage to provide the required plus and minus output swing for the meter and feedback network. A 100-to-1 voltage divider network consisting of a 9.9-KΩ resistor in series with a 100-ohm resistor sets the voltage at the 10-KMΩ resistor (in series with Terminal 3) to ±30 mV full-scale deflection. This 30-mV signal results from ±3 volts appearing at the top of the voltage divider network which also drives the meter circuitry.

By utilizing a switching technique in the meter circuit and in the 9.9 KΩ and 100-ohm network similar to that used in voltmeter circuit shown in Fig. 22, a current range of 3 pA to 1 nA full scale can be handled with the single 10-KMΩ resistor.

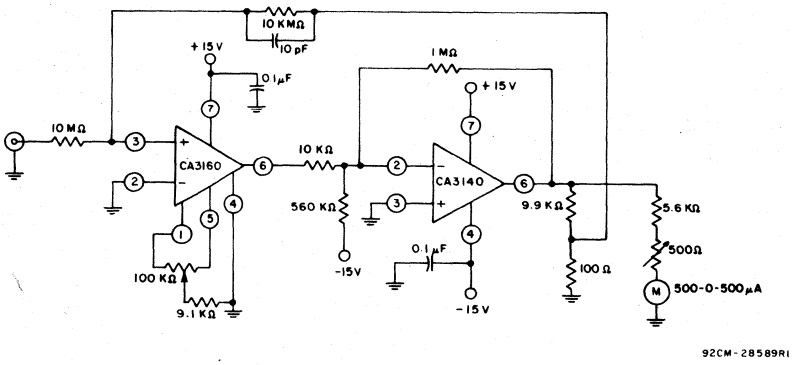


Fig.25 – Current-to-voltage converter to provide a picoammeter with ± 3 pA full-scale deflection.

Single-Supply Sample-and-Hold System

Fig. 26 shows a single-supply sample-and-hold system using a CA3160 to provide a high input impedance and an input-voltage range of 0 to 10 volts. The output from the input buffer integrator network is coupled to a CA3080A. The CA3080A functions as a strobeable current source for the CA3140 output integrator and storage capacitor. The CA3140 was chosen because of its low output impedance and constant gain-bandwidth product. Pulse "droop" during the hold interval can be reduced to zero by adjusting the 100-KΩ bias-voltage potentiometer on the positive input of the CA3140. This zero adjustment sets the CA3080A output voltage at its zero current position. In this sample-and-hold circuit it is essential that the amplifier bias current be reduced to zero to minimize output signal current during the hold mode. Even with 320 mV at the amplifier bias circuit terminal (5) at least ± 100 pA of output current will be available.

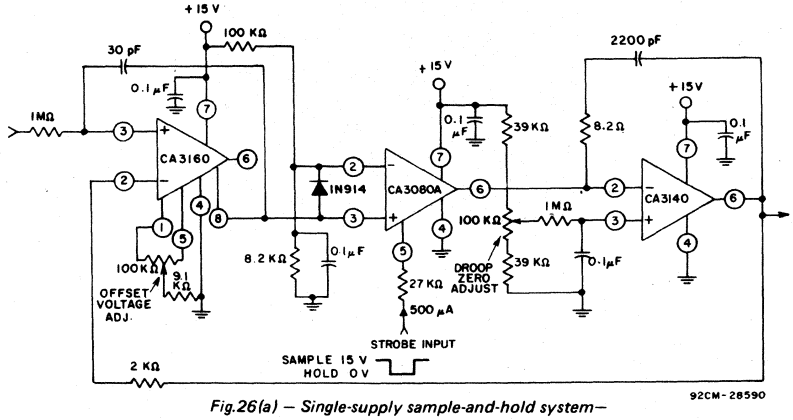
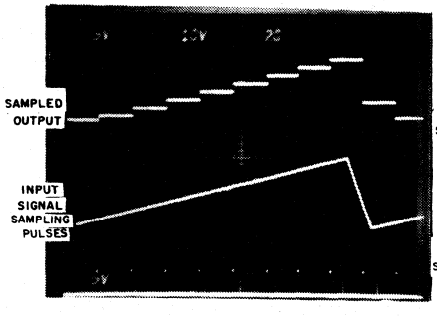
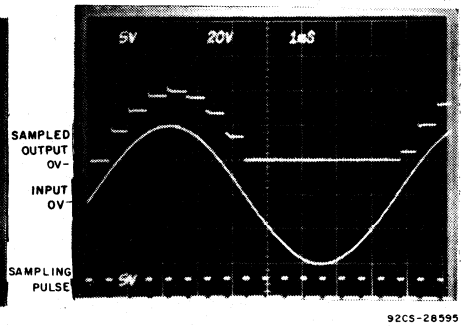


Fig.26(a) – Single-supply sample-and-hold system– input 0-to-10 volts.



(b) – Sample-and-hold waveform.
Top Trace: Sampled Output
Center Trace: Input Signal
Bottom Trace: Sampling Pulses



(c) – Sample-and-hold waveform.
Top Trace: Sampled Output
Center Trace: Input
Bottom Trace: Sampling Pulse

Wien Bridge Oscillator

A simple, single-supply Wien Bridge oscillator using a CA3160 is shown in Fig. 27. A pair of parallel-connected 1N914 diodes comprise the gain-setting network which standardizes the output voltage at approximately 1.1 volts. The 500-ohm potentiometer is adjusted so that the oscillator will always start and the oscillation will be maintained. Increasing the amplitude of the voltage may lower the threshold level for starting and for sustaining the oscillation, but will introduce more distortion.

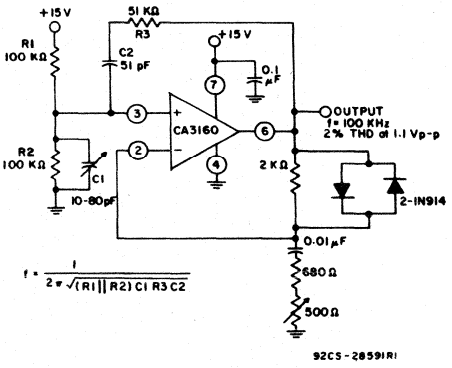


Fig.27 – Single-supply Wien Bridge oscillator.

Operation with Output-Stage Power-Booster

The current sourcing and sinking capability of the CA3160 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig.28, three COS/MOS transistor-pairs in a single CA3600 IC array are shown parallel-connected with the output stage in the CA3160. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA3160 output stage by about 2.5X.

The amplifier circuit in Fig. 28 employs feedback to establish a closed-loop gain of 20 dB. The typical large-signal-bandwidth (−3 dB) is 190 kHz.

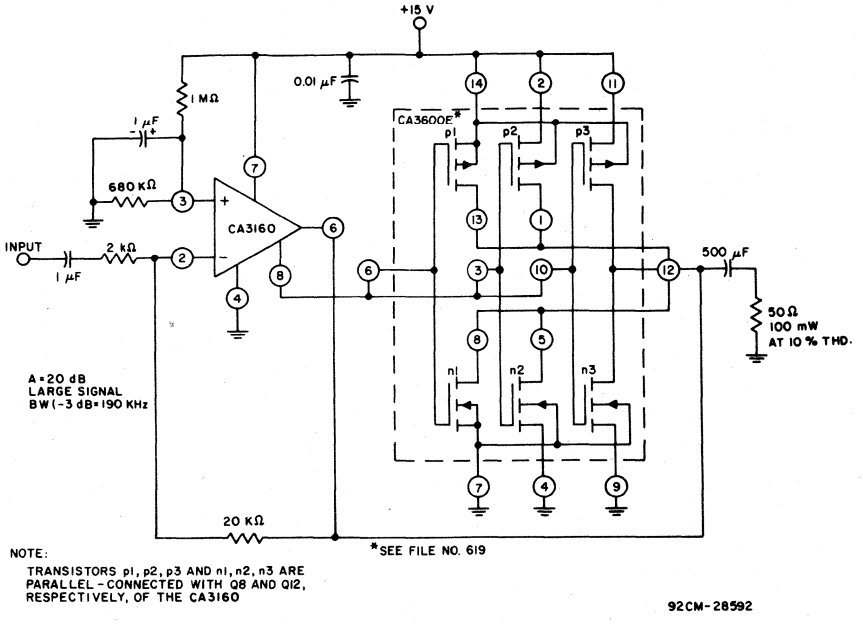
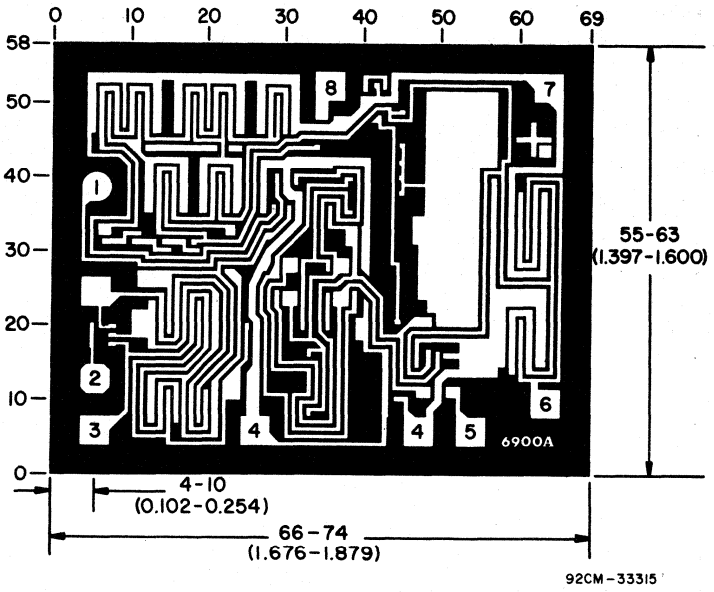


Fig.28 – COS/MOS transistor array (CA3600E) connected as power booster in the output stage of the CA3160.

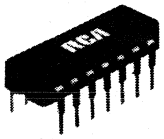
CA3160, CA3160A, CA3160B Types



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photograph and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips the cleavage angles are 57^{o} instead of 90^{o} with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.


Mini-DIP
(E Suffix)
H-1817


14-Lead DIP
(E1 Suffix)
H-1517

Dual BiMOS Operational Amplifiers

With MOS/FET Input, Bipolar Output

Features:

- *Dual version of CA3140*
- *Internally compensated*
- *MOS/FET input stage*
  - (a) *Very high input impedance (Z_{IN}) - 1.5 TΩ typ.*
  - (b) *Very low input current (I_I) - 10 pA typ. at ± 15 V*
  - (c) *Wide common-mode input-voltage range (V_{ICR}) - can be swung 0.5 volt below negative supply-voltage rail*
  - (d) *Rugged input stage - bipolar diode protected*
- *Directly replaces industry types 747 and 1458 in most applications*
- *Operation from 4-to-36 volts single or dual supplies*
- *Characterized for ± 15-volt operation and for TTL supply systems with operation down to 4 volts*
- *Wide bandwidth - 4.5 MHz unity gain at ± 15 V or 30 V*
- *High voltage-follower slew rate - 9/Vμs*
- *Output swings to within 0.5 volt of negative supply at $V^+ = 5$ V, $V^- = 0$*

Applications:

- *Ground-referenced single-supply amplifiers in automobile and portable instrumentation*
- *Sample and hold amplifiers*
- *Long-duration timers/multivibrators (microseconds - minutes - hours)*
- *Photocurrent instrumentation*
- *Active filters*
- *Intrusion alarm systems*
- *Comparators*
- *Instrumentation amplifiers*
- *Function generators*
- *Power supplies*

The RCA-CA3240A and CA3240 are dual versions of the popular CA3140-series integrated circuit operational amplifiers. They combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOS/FET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range (typically to 0.5 V below the negative supply rail). The bipolar output transistors allow a wide output voltage swing and provide a high output current capability.

The CA3240A and CA3240 are supplied in the 8-lead dual-in-line plastic package (Mini-DIP, E suffix), and in the 14-lead dual-in-line plastic package (E1 suffix). They are pin-compatible with the industry standard 747 and 1458 operational amplifiers in similar packages. The CA3240A and CA3240 have an operating-temperature range of −40 to +85° C. The offset null feature is available only when these types are supplied in the 14-lead dual-in-line plastic package (E1 suffix). The CA3240 is also available in chip form (H suffix).

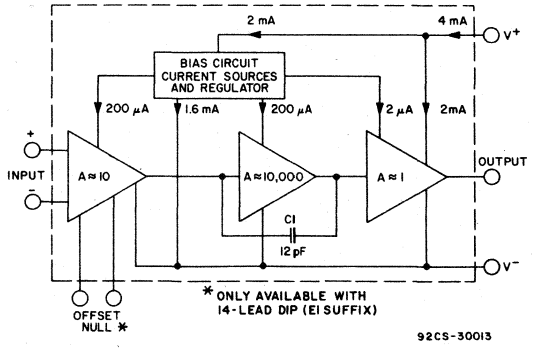


Fig. 1 — Block diagram of one-half CA3240 series.

CA3240, CA3240A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V
OPERATING VOLTAGE RANGE	4 to 36 V or ±2 to ±18 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±8 V
COMMON-MODE DC INPUT VOLTAGE	(V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT	1 mA
DEVICE DISSIPATION:	
UP TO 55°C	630 mW
ABOVE 55°C	Derate linearly 6.67 mW/°C
TEMPERATURE RANGE:	
OPERATING	−40 to +85°C
STORAGE	−65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION●	UNLIMITED
LEAD TEMPERATURE (DURING SOLDERING):	
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	+265°C

● Short circuit may be applied to ground or to either supply. Temperatures and/or supply voltages must be limited to keep dissipation within maximum rating.

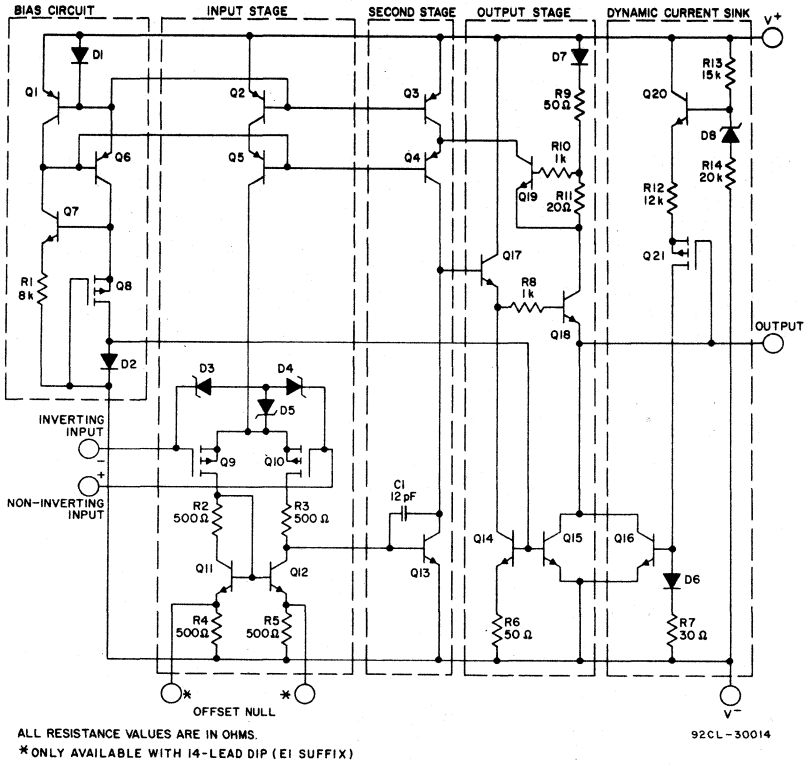


Fig. 2 – Schematic diagram of one-half CA3240 series.

Circuit Description

The schematic diagram of one amplifier section of the CA3240 is shown in Fig. 2. It consists of a differential amplifier stage using PMOS transistors Q9 and Q10 with gate-to-source protection against static discharge damage provided by zener diodes D3, D4, and D5. Constant current bias is applied to the differential amplifier from transistors Q2 and Q5 connected as a constant-current source. This assures a high common-mode rejection ratio. The output of the differential amplifier is coupled to the base of gain stage transistor Q13 by means of an n-p-n current mirror that supplies the required differential-to-single-ended conversion. Provision for offset null for types in the 14-lead plastic package (E1 suffix) is provided through the use of this current mirror.

The gain stage transistor Q13 has a high-impedance active load (Q3 and Q4) to provide maximum open-loop gain. The collector of Q13 directly drives the base of the compound emitter-follower output stage. Pull-down for the output stage is provided by two independent circuits: (1) constant-current-connected transistors Q14 and Q15 and (2) dynamic current-sink transistor Q16 and its associated circuitry. *The level of pull-down current is constant at about 1 mA for Q15 and varies from 0 to 18 mA for Q16 depending on the magnitude of the voltage between the output terminal and V^+.* The dynamic current sink becomes active whenever the output terminal is more negative than V^+ by about 15 V. When this condition exists, transistors Q21 and Q16 are turned on causing Q16 to sink current from the output terminal to V^-. This current always flows when the output is in the linear region, either from the load resistor or from the emitter of Q18 if no load resistor is present. The purpose of this dynamic sink is to permit the output to go within 0.2 V (V_{CE}(sat)) of V^- with a 2-kΩ load to ground. *When the load is returned to V^+, it may be necessary to supplement the 1 mA of current from Q15 in order to turn on the dynamic current sink (Q16).* This may be accomplished by placing a resistor (approx. 2 kΩ) between the output and V^-.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At V^+ = 15 V, V^- = 15 V, T_A = 25°C Unless Otherwise Specified

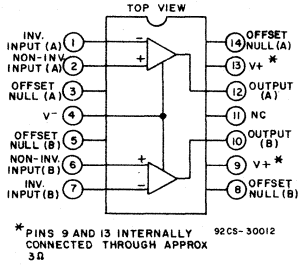
CHARACTERISTIC	LIMITS						UNITS
	CA3240A			CA3240			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	–	2	5	–	5	15	mV
Input Offset Current, $\|I_{IO}\|$	–	0.5	20	–	0.5	30	pA
Input Current, I_I	–	10	40	–	10	50	pA
Large-Signal Voltage Gain, A_{OL}●	20 k	100 k	–	20 k	100 k	–	V/V
(See Figs. 4, 19)	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR	–	32	320	–	32	320	μV/V
(See Fig. 9)	70	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR} (See Fig. 16)	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	11	V
Power-Supply Rejection Ratio, $\frac{\Delta V_{IO}}{\Delta V}$ PSRR	–	100	150	–	100	150	μV/V
(See Fig. 11)	76	80	–	76	80	–	dB
Maximum Output Voltage,■ V_{OM}^+	+12	13	–	+12	13	–	V
(See Figs. 22, 16) V_{OM}^-	−14	−14.4	–	−14	−14.4	–	
Maximum Output Voltage,† V_{OM}^-	0.4	0.13	–	0.4	0.13	–	V
Supply Current, I^+ (See Fig. 7) For Both Amps.	–	8	12	–	8	12	mA
Total Device Dissipation, P_D	–	240	360	–	240	360	mW

● At V_O = 26 V_{p-p}, +12 V, −14 V and R_L = 2 kΩ.
■ At R_L = 2 kΩ.
† At V^+ = 5 V, V^- = GND, I_{Sink} = 200 μA.

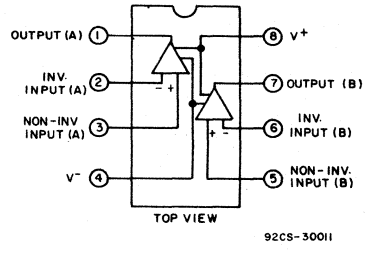
CA3240, CA3240A Types

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS $V^+ = +15$ V, $V^- = -15$ V, $T_A = 25^oC$	TYPICAL VALUES CA3240A	TYPICAL VALUES CA3240	UNITS
Input Offset Voltage Adjustment Resistor (E1 Package Only)		Typ. Value of Resistor Between Terms. 4 and 3(5) or Between 4 and 14(8) to Adjust Max. V_{IO}	18	4.7	kΩ
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I		4	4	pF
Output Resistance	R_O		60	60	Ω
Equivalent Wideband Input Noise Voltage (See Fig. 21)	e_n	BW=140 kHz, R_S = 1 MΩ	48	48	μV
Equivalent Input Noise Voltage (See Fig. 10)	e_n	f= 1 kHz, R_S=	40	40	nV/√Hz
		f=10 kHz, 100 Ω	12	12	
Short-Circuit Current to Opposite Supply Source	I_{OM}^+		40	40	mA
Sink	I_{OM}^-		11	11	
Gain-Bandwidth Product (See Figs. 5 and 19)	f_T		4.5	4.5	MHz
Slew Rate (See Fig. 6)	SR		9	9	V/μs
Transient Response: Rise Time	t_r	R_L=2 kΩ	0.08	0.08	μs
Overshoot (See Fig. 20)		C_L=100 pF	10	10	%
Settling Time at 10 V_{p-p}, (See Fig. 17) 1 mV	t_s	R_L=2 kΩ, C_L=100 pF, Voltage Follower	4.5	4.5	μs
10 mV			1.4	1.4	
Crosstalk		f = 1 kHz	120	120	dB



E1 Suffix
Pin compatible with the industry-standard 747



E Suffix
Pin compatible with the industry-standard 1458

Fig. 3 — Functional diagrams.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V^+ = 15 V, V^- = 15 V, T_A = −40 to +85°C Unless Otherwise Specified

CHARACTERISTIC		TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage,	$\lvert V_{IO}\rvert$	3	10	mV
Input Offset Current,♦	$\lvert I_{IO}\rvert$	32	32	pA
Input Current,♦	I_I	640	640	pA
Large-Signal Voltage Gain, (See Figs. 4, 19)	A_{OL}●	63 k	63 k	V/V
		96	96	dB
Common-Mode Rejection Ratio, (See Fig. 9)	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range, (See Fig. 16)	V_{ICR}	−15 to +12.3	−15 to +12.3	V
Power-Supply Rejection Ratio, (See Fig. 11)	$\Delta V_{IO}/\Delta V$ PSRR	150	150	μV/V
		76	76	dB
Maximum Output Voltage,■ (See Figs. 16, 22)	V_{OM}^+	12.4	12.4	V
	V_{OM}^-	−14.2	−14.2	
Supply Current, (See Fig. 7) For Both Amps.	I^+	8.4	8.4	mA
Total Device Dissipation,	P_D	252	252	mW
Temperature Coefficient of Input Offset Voltage,	$\Delta V_{IO}/\Delta T$	15	15	μV/°C

● At V_O = 26 $V_{p\text{-}p}$, +12 V, −14 V and R_L = 2 kΩ.

■ At R_L = 2 kΩ.

♦ At T_A = 85°C

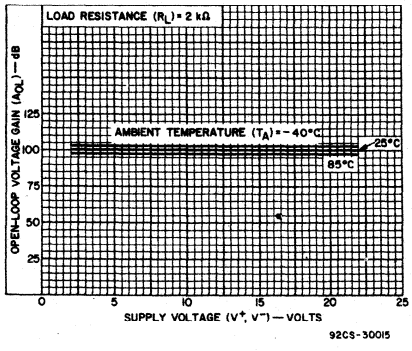


Fig. 4 — Open-loop voltage gain as a function of supply voltage and temperature.

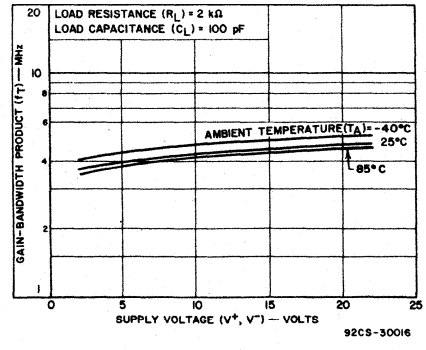


Fig. 5 — Gain-bandwidth product as a function of supply voltage and temperature.

CA3240, CA3240A Types

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE
At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25°C$

CHARACTERISTIC		TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage,	$\|V_{IO}\|$	2	5	mV
Input Offset Current,	$\|I_{IO}\|$	0.1	0.1	pA
Input Current,	I_I	2	2	pA
Input Resistance		1	1	TΩ
Large-Signal Voltage Gain, (See Figs. 4, 19)	A_{OL}	100 k	100 k	V/V
		100	100	dB
Common-Mode Rejection Ratio,	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range, (See Fig. 22)	V_{ICR}	−0.5	−0.5	V
		2.6	2.6	
Power-Supply Rejection Ratio,	PSRR	31.6	31.6	μV/V
		90	90	dB
Maximum Output Voltage, (See Figs. 16,22)	V_{OM}^+	3	3	V
	V_{OM}^-	0.3	0.3	
Maximum Output Current: Source,	I_{OM}^+	20	20	mA
Sink	I_{OM}^-	1	1	
Slew Rate (See Fig. 6)		7	7	V/μs
Gain-Bandwidth Product, (See Fig. 5)	f_T	4.5	4.5	MHz
Supply Current, (See Fig. 7)	I^+	4	4	mA
Device Dissipation,	P_D	20	20	mW

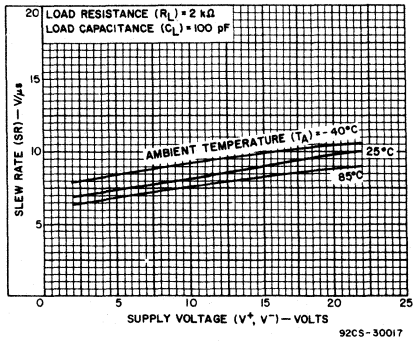


Fig. 6 — Slew rate as a function of supply voltage and temperature.

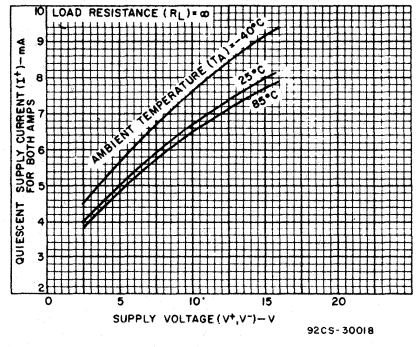


Fig. 7 — Quiescent supply current as a function of supply voltage and temperature.

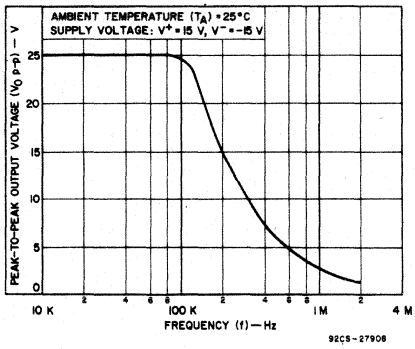


Fig. 8 — Maximum output voltage swing as a function of frequency.

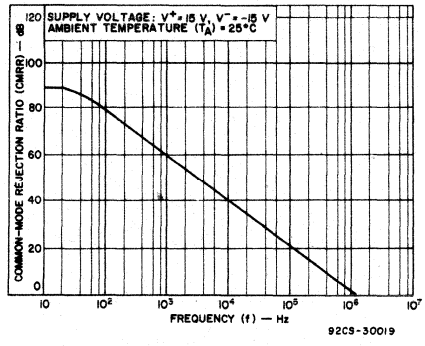


Fig. 9 — Common-mode rejection ratio as a function of frequency.

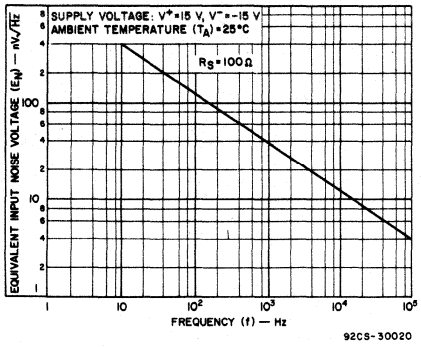


Fig. 10 — Equivalent input noise voltage as a function of frequency.

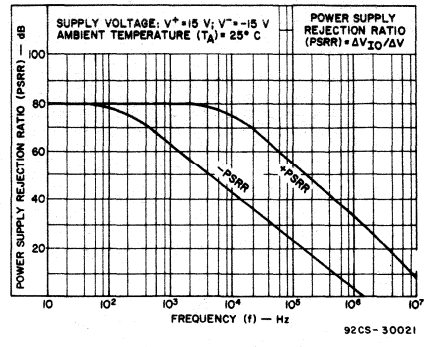


Fig. 11 — Power supply rejection ratio as a function of frequency.

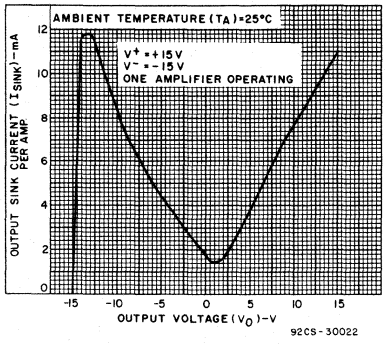


Fig. 12 — Output sink current as a function of output voltage.

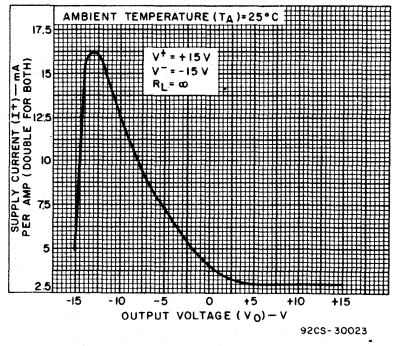


Fig. 13 — Supply current as a function of output voltage.

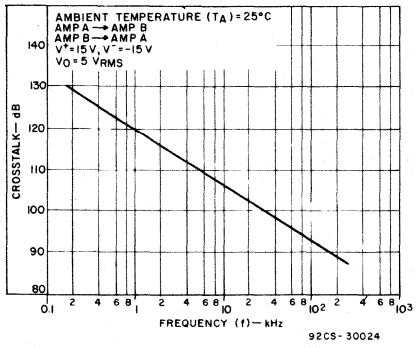


Fig. 14 — Crosstalk as a function of frequency.

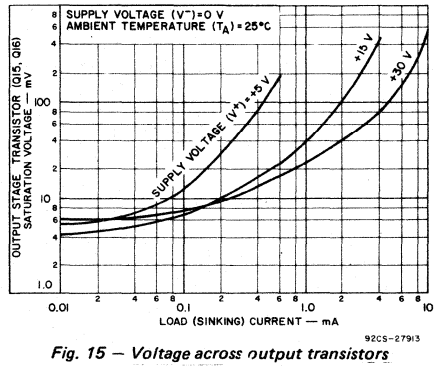


Fig. 15 — Voltage across output transistors Q15 and Q16 as a function of load current.

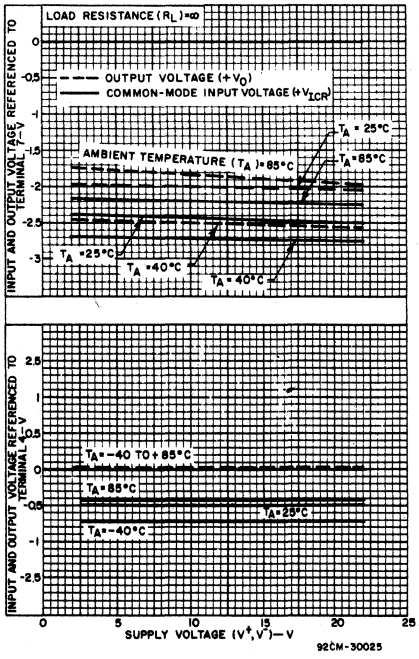


Fig. 16 — Output-voltage-swing capability and common-mode input-voltage range as a function of supply voltage and temperature.

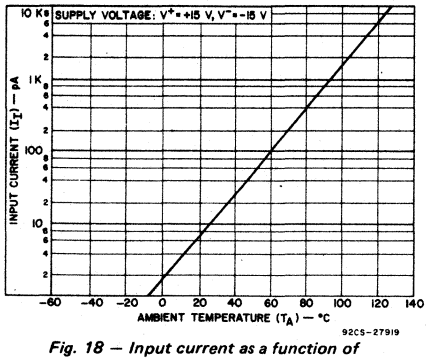
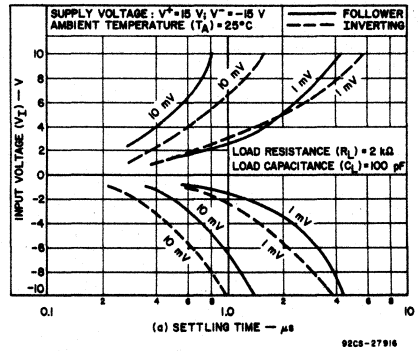


Fig. 18 — Input current as a function of ambient temperature.



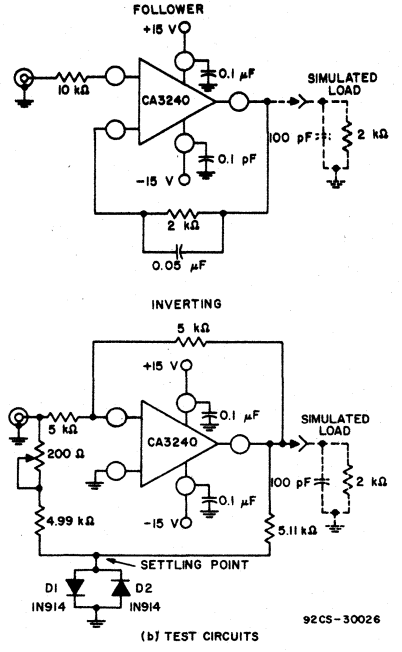


Fig. 17 — Input voltage as a function of settling time.

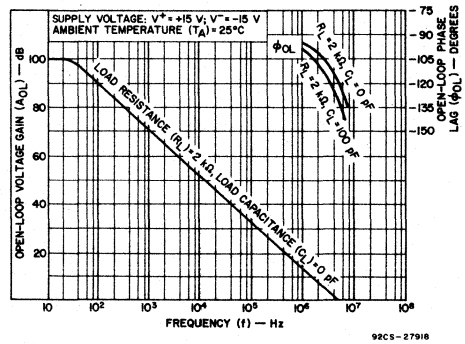
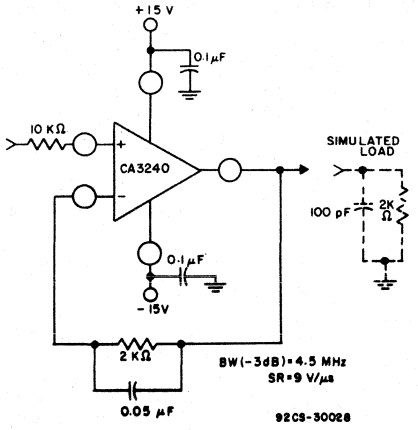
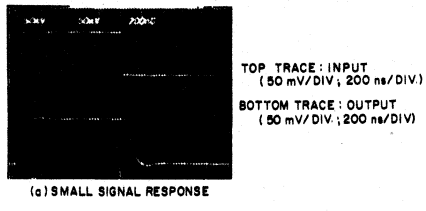


Fig. 19 — Open-loop voltage gain and phase lag as a function of frequency.





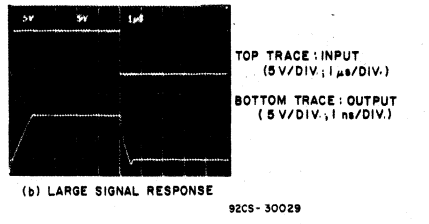


Fig. 20 – Split-supply voltage-follower test circuit and associated waveforms.

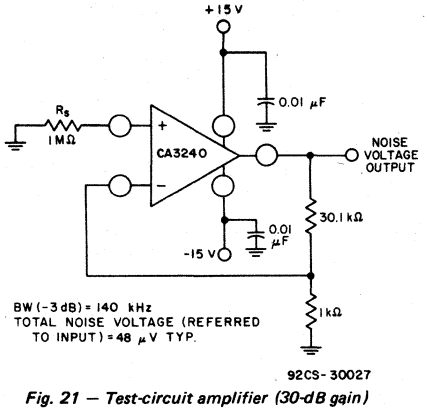


Fig. 21 – Test-circuit amplifier (30-dB gain) used for wideband noise measurement.

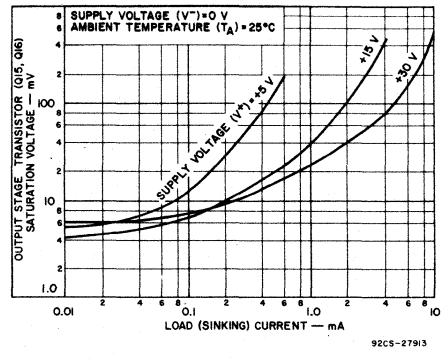


Fig. 22 – Voltage across output transistors Q15 and Q16 as a function of load current.

APPLICATIONS CONSIDERATIONS

Output Circuit Considerations

Fig. 22 shows output current-sinking capabilities of the CA3240 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

Fig. 23 shows some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

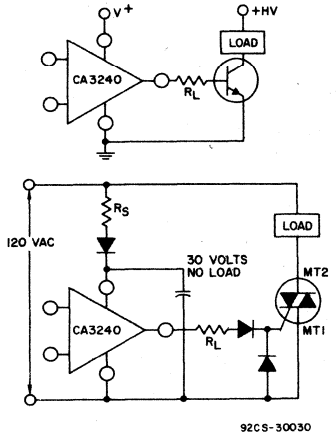


Fig. 23 – Methods of utilizing the $V_{CE}(sat)$ sinking-current capability of the CA3240 series.

Input Circuit Considerations

As indicated by the typical VICR, this device will accept inputs as low as 0.5 V below V^-. However, a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3240 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig. 24 shows typical input-terminal current versus ambient temperature for the CA3240.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

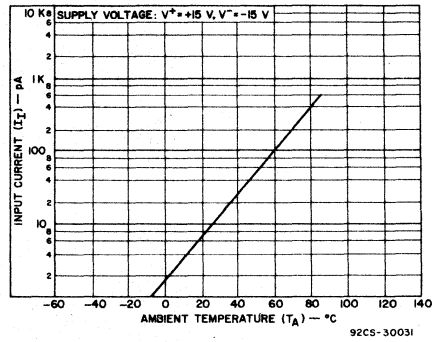


Fig. 24 – Input current as a function of ambient temperature.

Offset-Voltage Nulling

The input-offset voltage of the CA3240AE1 and CA3240E1 can be nulled by connecting a 10-kΩ potentiometer between Terminals 3 and 14 or 5 and 8 and returning its wiper arm to Terminal 4, see Fig. 25a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig. 25b, to optimize its utilization range are given in the table "Electrical Characteristics For Design Guidance" shown in this bulletin.

An alternate system is shown in Fig. 25c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

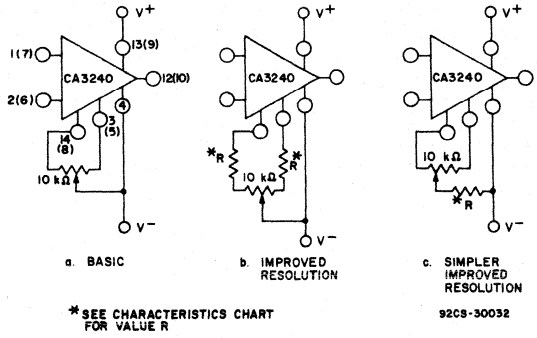


Fig. 25 – Three offset-voltage nulling methods. (CA3240AE1, CA3240E1 only.)

TYPICAL APPLICATIONS

On/Off Touch Switch

The on/off touch switch shown in Fig. 26 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the "on" plate is touched, current flows between the two halves of the grid causing a positive shift in the output voltage (Term. 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing triac driver. When a positive pulse occurs at Terminal 7 of the CA3240E, the triac is turned on and held on by the CA3059 and its associated positive feedback circuitry (51-kΩ resistor and 36-kΩ/42-kΩ voltage divider). When the positive pulse occurs at Terminal 1 (CA3240E), the triac is turned off and held off in a similar manner. Note that power for the CA3240E is supplied by the CA3059 internal power supply.

The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while allowing sufficiently high circuit impedance to provide protection against electrical shock.

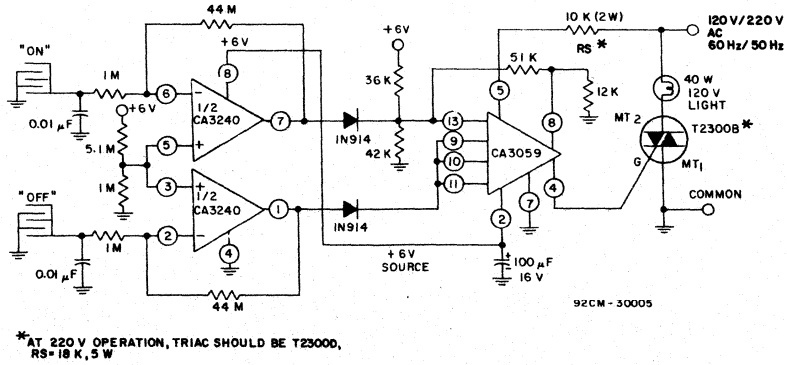


Fig. 26 – On/off touch switch.

CA3240, CA3240A Types

Dual Level Detector (window comparator)

Fig. 27 illustrates a simple dual liquid level detector using the CA3240E as the sensing amplifier. This circuit operates on the principle that most liquids contain enough ions in solution to sustain a small amount of current flow between two electrodes submersed in the liquid. The current, induced by an 0.5-V potential applied between two halves of a PC board grid, is converted to a voltage level by the CA3240E in a circuit similar to that of the on/off touch switch shown in Fig. 26. The changes in voltage for both the upper and lower level sensors are processed by the CA3140 to activate an LED whenever the liquid level is above the upper sensor or below the lower sensor.

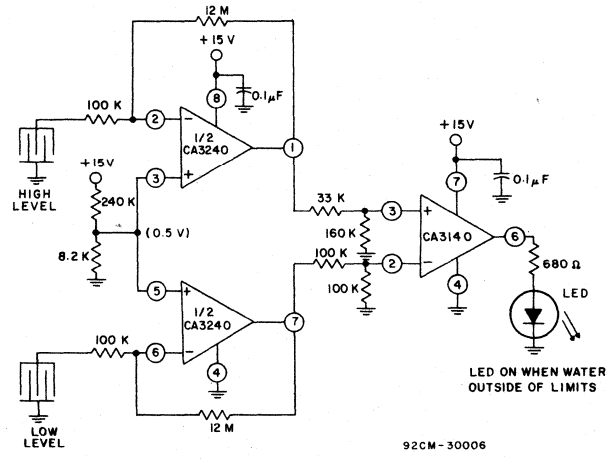


Fig. 27 – Dual level detector.

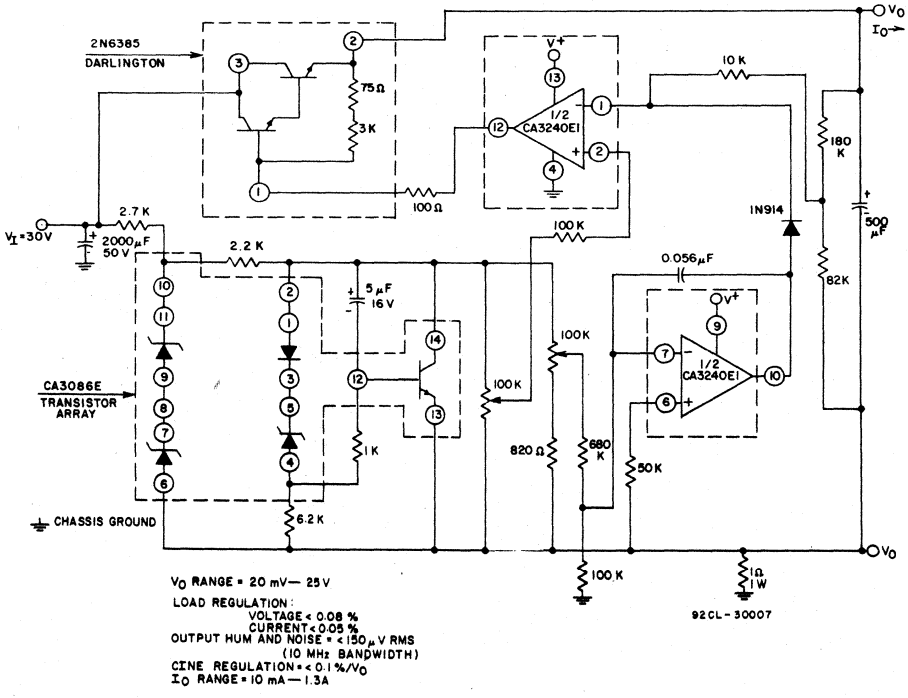


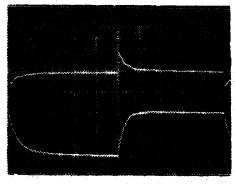
Fig. 28 – Constant-voltage/constant-current power supply.

Constant-Voltage/Constant-Current Power Supply

The constant-voltage/constant-current power supply shown in Fig. 28 uses the CA3240E as a voltage-error and current-sensing amplifier. The CA3240E is ideal for this application because its input common-mode voltage-range includes ground, allowing the supply to adjust from 20 mV to 25 V without requiring an additional negative input voltage. Also, the ground reference capability of the CA-3240E allows it to sense the voltage across the 1-Ω current-sensing resistor in the negative output lead of the power supply. The CA3086 transistor array functions as a reference for both constant-voltage and constant-current limiting. The 2N6385 power Darlington is used as the pass element and may be required to dissipate as much as 40 W. Fig. 29 shows the transient response of the supply during a 100-mA to 1-A load transition.

Precision Differential Amplifier

Fig. 30 shows the CA3240E in the classical precision differential amplifier circuit. The CA3240E is ideally suited for biomedical applications because of its extremely high input impedance. To insure patient safety, an extremely high electrode series resistance is required to limit any current that might result in patient discomfort in the event of a fault condition. In this case, 10-MΩ resistors have been used to limit the current to less than 2 μA without affecting the performance of the circuit. Fig. 31 shows a typical electrocardiogram waveform obtained with this circuit.



TRANSIENT RESPONSE

TOP TRACE : OUTPUT VOLTAGE
(500 mV/cm AND 5 μs/cm)
BOTTOM TRACE : COLLECTOR OF LOAD
SWITCHING TRANSISTOR
LOAD = 100 mA TO 1A
(5 V/cm AND 5 μs/cm)

92CS-30034

Fig. 29 – Transient response.

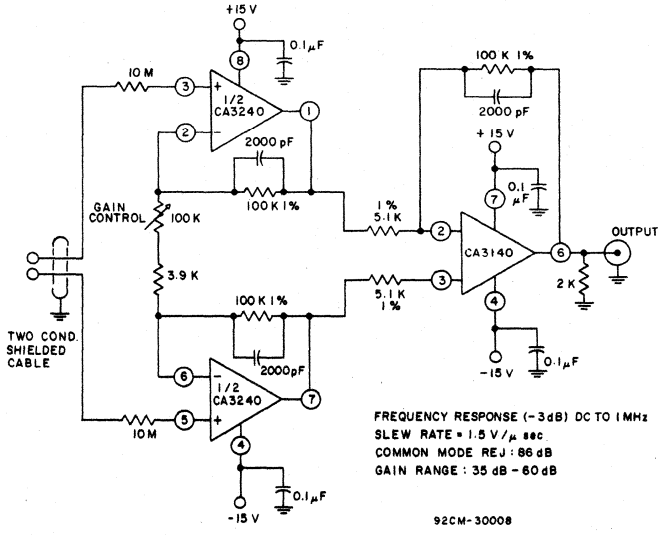
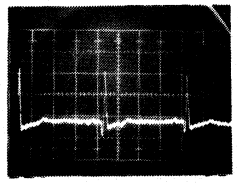


Fig. 30 – Precision differential amplifier.



TYPICAL ELECTROCARDIOGRAM WAVEFORM

VERTICAL : 1.0 mV/DIV.
(AMPLIFIER GAIN = 100 X)
(SCOPE SENSITIVITY = 0.1V/DIV.
HORIZONTAL : > 0.2 SEC/DIV (UNCAL)

92CS-30033

Fig. 31 – Typical electrocardiogram waveform.

Differential Light Detector

In the circuit shown in Fig. 32, the CA3240E converts the current from two photo diodes to voltage, and applies 1 V of reverse bias to the diodes. The voltages from the CA3240E outputs are subtracted in the second stage (CA3140) so that only the difference is amplified. In this manner, the circuit can be used over a wide range of ambient light conditions without circuit component adjustment. Also, when used with a light source, the circuit will not be sensitive to changes in light level as the source ages.

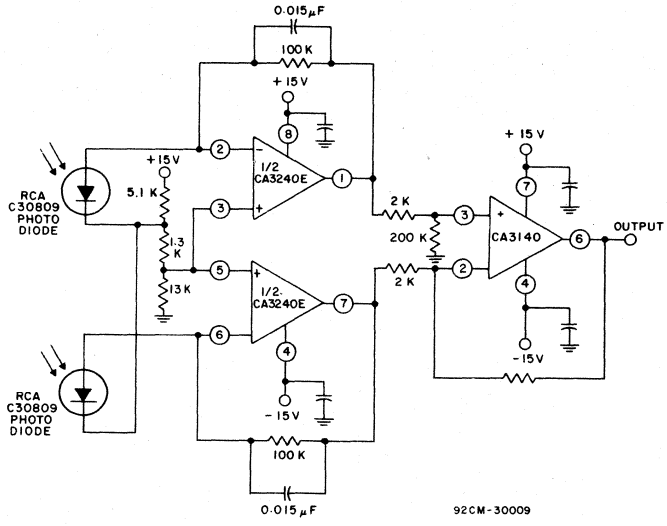
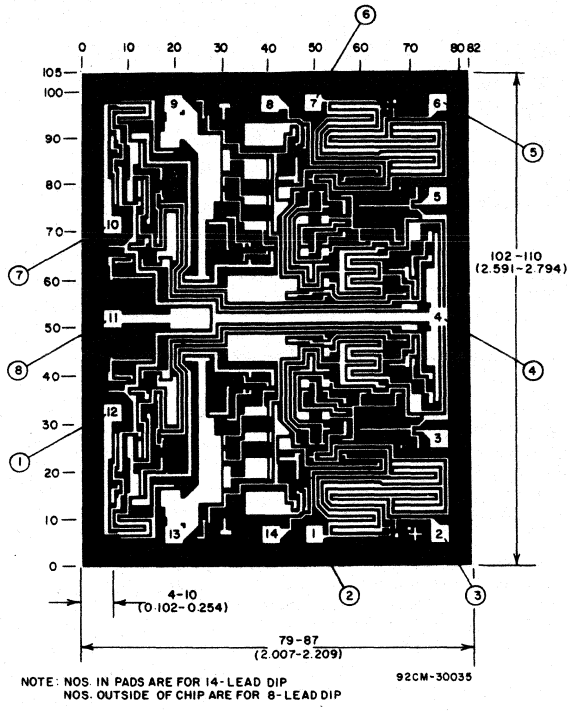


Fig. 32 – Differential light detector.

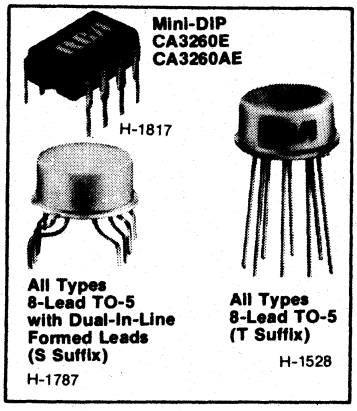
CA3240H Dimensions and Pad Layout



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57^{o} instead of 90^{o} with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3260, CA3260A, CA3260B Types



BiMOS Operational Amplifiers

With MOS/FET Input, COS/MOS Output

FEATURES:

- *Dual version of the CA3160*
- *MOS/FET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 × 10^{12}Ω) typ.
  very low II = 5 pA typ. at 15-V operation
  = 2 pA typ. at 5-V operation
- *Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *COS/MOS output stage permits signal swing to either (or both) supply rails*

} *Ideal for single-supply applications*

- *Low V_{IO}: 2 mV max. (CA3260B)*
  Wide BW: 4 MHz typ. (unity-gain crossover)
  High SR: 10 V/μs typ. (unity-gain follower)
  High output current (I_O): 20 mA typ.
- *High A_{OL}: 320,000 (110 dB) typ.*
- *Internal phase compensation for unity gain.*
- *Same pin-out as CA1458, CA1558*

APPLICATIONS:

- *Ground-referenced single-supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *Ideal interface with digital COS/MOS*
- *High-input-impedance wideband amplifiers*
- *Voltage followers*
  (e.g., follower for single-supply D/A converter)
- *Voltage regulators*
  (permits control of output voltage down to zero volts)
- *Wien-Bridge oscillators*
- *Voltage-controlled oscillators*
- *Photo-diode sensor amplifiers*

The RCA-CA3260T, CA3260S, CA3260E; CA3260AT, CA3260AS, CA3260AE; and CA3260BT, CA3260BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip. The CA3260 series circuits are dual versions of the popular CA3160 series.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3260-series circuits operate at supply voltages ranging from 4 to 16 volts, or ±2 to ±8 volts when using split supplies.

The CA3260 series is supplied in standard 8-lead TO-5-style packages (T suffix) and 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" packages (S suffix). The CA3260 is available in chip form (H suffix).

The CA3260A and CA3260 are also available in the 8-lead dual-in-line plastic package (Mini-DIP E suffix). All types operate over the full military-temperature range of -55° C to +125° C. The CA3260B is intended for applications requiring premium-grade specifications. The CA3260A offers superior input characteristics over those of the CA3260.

ELECTRICAL CHARACTERISTICS for Each Amplifier at T_A=25°C, V^+=15 V, V^-=0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS									UNITS
	CA3260B (T,S)			CA3260A (T,S,E)			CA3260 (T,S,E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\lvert V_{IO} \rvert$, $V^{\pm}$=±7.5 V	—	0.8	2	—	2	5	—	6	15	mV
Input Offset Current, $\lvert I_{IO} \rvert$, $V^{\pm}$=±7.5 V	—	0.5	10	—	0.5	20	—	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	—	5	20	—	5	30	—	5	50	pA
Large-Signal Voltage Gain, A_{OL}	100 k	320 k	—	50 k	320 k	—	50 k	320 k	—	V/V
V_O=10 V_{p-p}, R_L=10 kΩ	100	110	—	94	110	—	94	110	—	dB
Common-Mode Rejection Ratio, CMRR	86	100	—	80	95	—	70	90	—	dB
Common-Mode Input Voltage Range, V_{ICR}	0	0.5 to 12	10	0	0.5 to 12	10	0	0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	—	32	100	—	32	150	—	32	320	μV/V
Maximum Output Voltage:										
At R_L=10 kΩ V_{OM}^+	11	13.3	—	11	13.3	—	11	13.3	—	V
At R_L=10 kΩ V_{OM}^-	—	0.002	0.01	—	0.002	0.01	—	0.002	0.01	V
At R_L=∞ V_{OM}^+	14.99	15	—	14.99	15	—	14.99	15	—	V
At R_L=∞ V_{OM}^-	—	0	0.01	—	0	0.01	—	0	0.01	V
Maximum Output Current, I_{OM}^+ (Source) @ V_O=7.5 V	12	22	45	12	22	45	12	22	45	mA
I_{OM} (Sink) @ V_O=7.5 V	12	20	45	12	20	45	12	20	45	mA
Total Supply Current, I^+ R_L=∞										
V_O(Ampli.A)=V_O (Ampli.B)=7.5 V	—	9	15.5	—	9	15.5	—	9	15.5	mA
V_O (Ampli.A)=V_O (Ampli.B)=0 V	—	1.2	3	—	1.2	3	—	1.2	3	mA
V_O (Ampli.A)=0 V V_O(Ampli.B)=7.5 V	—	5	8.5	—	5	8.5	—	5	8.5	mA
Input Offset Voltage Temp.Drift, $\Delta V_{IO}/\Delta T$	—	5	—	—	6	—	—	8	—	μV/°C
Crosstalk f=1 kHz	—	120	—	—	120	—	—	120	—	dB

CA3260, CA3260A, CA3260B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals)..... 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE..... ±8 V
COMMON-MODE DC
INPUT VOLTAGE..... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK —
UP TO 55°C..... 630 mW
ABOVE 55°C ... Derate linearly 6.67 mW/°C
WITH HEAT SINK —
UP TO 90°C..... 1 W
ABOVE 90°C ... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING (All Types) ..... −55 to +125°C
STORAGE (All Types) ..... −65 to +150°C
OUTPUT SHORT-CIRCUIT
DURATION*..... INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
At distance 1/16 ± 1/32 in.
(1.59 ± 0.79 mm) from case
for 10 s max. ..... +265°C

*Short circuit may be applied to ground or to either supply.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS	CA3260 (T, S)	CA3260 (T, S, E)	CA3260 (T, S, E)	UNITS
V^+=+7.5 V, V^-=−7.5 V, T_A=25°C (Unless Otherwise Specified)					
Input Resistance, R_I		1.5	1.5	1.5	TΩ
Input Capacitance, C_I	f=1 MHz	4.3	4.3	4.3	pF
Unity Gain Crossover Frequency, f_T		4	4	4	MHz
Slew Rate, SR		10	10	10	V/μs
Transient Response: Rise Time, t_r	C_L=25 pF, R_L=2 kΩ (Voltage Follower)	0.09	0.09	0.09	μs
Overshoot		10	10	10	%
Settling Time (4 V_{p-p} Input to < 0.1%)		1.8	1.8	1.8	μs
V^+=5 V, V^-=0 V, T_A=25°C (Unless Otherwise Specified)					
Input Offset Voltage, V_{IO}		1	2	6	mV
Input Offset Current, I_{IO}		0.1	0.1	0.1	pA
Input Current, I_I		2	2	2	pA
Common-Mode Rejection Ratio, CMRR		80	70	60	dB
Large-Signal Voltage Gain, A_{OL}	V_O=4 V_{p-p}, R_L=20 kΩ	100 k 100	100 k 100	100 k 100	V/V dB
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.5	0 to 2.5	0 to 2.5	V
Supply Current, I^+	V_O=5 V, R_L=∞	1	1	1	mA
	V_O=2.5 V, R_L=∞	1.2	1.2	1.2	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	200	μV/V

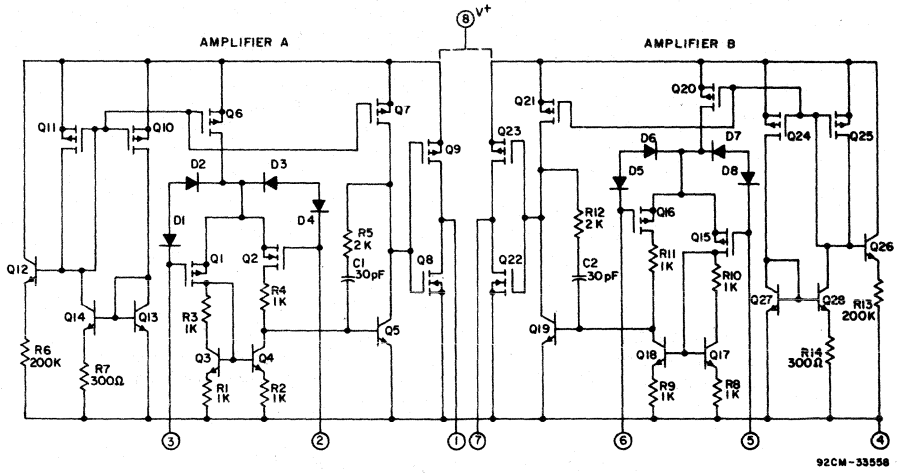
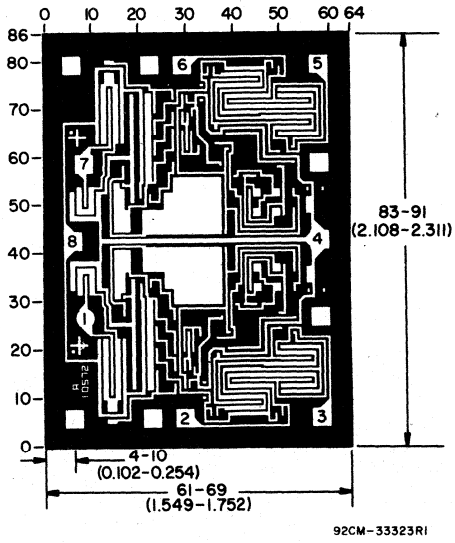


Fig. 1 - Schematic diagram of CA3260 series.

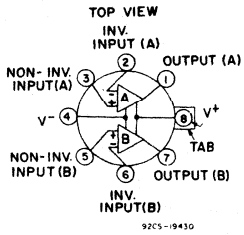


Dimensions and pad layout for CA3260H.

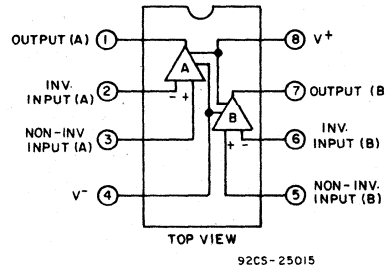
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3260, CA3260A, CA3260B Types



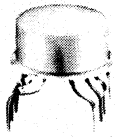
S and T Suffixes
Pin compatible with the industry-standard 1458



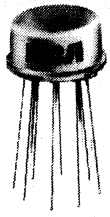
E Suffix
Pin compatible with the industry-standard 1458

Fig. 2 - Functional diagrams for the CA3260 Series.

CA3094, CA3094A, CA3094B Types



S-Suffix Types
8-LEAD TO-5
with Dual-In-Line
Formed Leads
"DIL-CAN"
H-1787



T-Suffix Types
8-LEAD TO-5
H-1528

H-1817

CA3094E
8-LEAD DUAL
IN-LINE PLASTIC
PACKAGE
"MINI-DIP"

Programmable Power Switch/Amplifier

For Control & General-Purpose Applications

CA3094T,S,E:	For Operation Up to 24 Volts
CA3094AT,S,E:	For Operation Up to 36 Volts
CA3094BT,S:	For Operation Up to 44 Volts

Features:

- *Designed for single or dual power supply*
- *Programmable: strobing, gating, squelching, AGC capabilities*
- *Can deliver 3 watts (avg.) or 10 W (peak) to external load (in switching mode)*
- *High-power, single-ended class A amplifier will deliver power output of 0.6 watt [1.6 W device dissipation]*
- *Total harmonic distortion [THD] @ 0.6 W in class A operation - 1.4% typ.*
- *High current-handling capability - 100 mA (avg.), 300 mA (peak)*
- *Sensitivity controlled by varying bias current*
- *Output: "sink" or "drive" capability*

Applications:

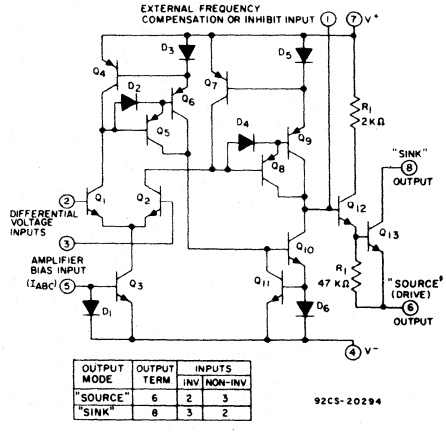
- *Error-signal detector: temperature control with thermistor sensor; speed control for shunt wound dc motor*
- *Over-current, over-voltage, over-temperature protectors*
- *Dual-tracking power supply with RCA-CA3085*
- *Wide-frequency-range oscillator*
- *Analog timer*
- *Level detector*
- *Alarm systems*
- *Voltage follower*
- *Ramp-voltage generator*
- *High-power comparator*
- *Ground-fault interrupter [GFI] circuits*

The CA3094 is a differential-input power-control switch/amplifier with auxiliary circuit features for ease of programmability. For example, an error or unbalance signal can be amplified by the CA3094 to provide an on-off signal or proportional-control output signal up to 100 mA. This signal is sufficient to directly drive high-current thyristors, relays, dc loads, or power transitors. The CA3094 has the generic characteristics of the RCA-CA3080 operational amplifier directly coupled to an integral Darlington power transistor capable of sinking or driving currents up to 100 mA.

The gain of the differential input stage is proportional to the amplifier bias current (I_{ABC}), permitting programmable variation of the integrated circuit sensitivity with either digital and/or analog programming signals. For example, at an I_{ABC} of 100 μA, a one-millivolt change at the input will change the output from 0 to 100 mA (typical).

The CA3094 is intended for operation up to 24 volts and is especially useful for timing circuits, in automotive equipment, and in other applications where operation up to 24 volts is a primary design requirement (see Figs. 28, 29 and 30 in Applications Section). The CA3094A and CA3094B are like the CA3094 but are intended for operation up to 36 and 44 volts, respectively (single or dual supply).

These types are available in 8-lead TO-5 style packages with standard leads ("T" suffix) and with dual-in-line formed leads "DIL-CAN" ("S" suffix). Type CA3094 is also available in an 8-lead dual-in-line plastic package "MINI-DIP" ("E" suffix), and in chip form ("H" suffix).



OUTPUT MODE	OUTPUT TERM	INPUTS	
		INV	NON-INV
"SOURCE"	6	2	3
"SINK"	8	3	2

Fig. 1 — Schematic diagram of CA3094.

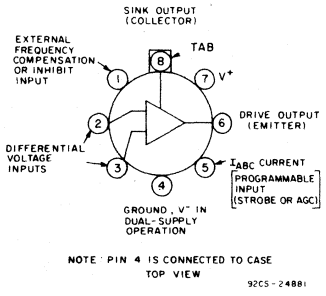
CA3094, CA3094A, CA3094B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

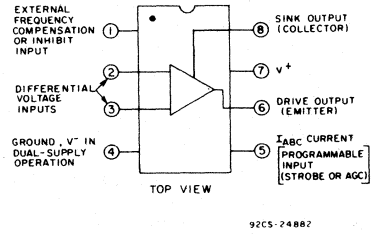
	CA3094	CA3094A	CA3094B	
DC SUPPLY VOLTAGE:				
Dual Supply	± 12 V	± 18 V	± 22 V	V
Single Supply	24 V	36 V	44 V	V
DC DIFFERENTIAL INPUT VOLTAGE (Terminals 2 and 3)	± 5*			V
DC COMMON-MODE INPUT VOLTAGE	Term. 4 ⩽ Term. 2 & 3 ⩽ Term. 7			
PEAK INPUT SIGNAL CURRENT (Terminals 2 and 3)	± 1			mA
PEAK AMPLIFIER BIAS CURRENT (Terminal 5)	2			mA
OUTPUT CURRENT:				
Peak	300			mA
Average	100			mA
DEVICE DISSIPATION:				
Up to T_A = 55°C:				
Without heat sink	630			mW
With heat sink	1.6			W
Above T_A = 55°C:				
Without heat sink derate linearly	6.67			mW/°C
With heat sink derate linearly	16.7			mW/°C
THERMAL RESISTANCE (Junction to Air)	140			°C/W
AMBIENT TEMPERATURE RANGE:				
Operating	−55 to +125			°C
Storage	−65 to +150			°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 300			°C

*Exceeding this voltage rating will not damage the device unless the peak input signal current (1 mA) is also exceeded.

FUNCTIONAL DIAGRAMS



TO-5 Style Package



Plastic Package

TYPICAL CHARACTERISTICS CURVES

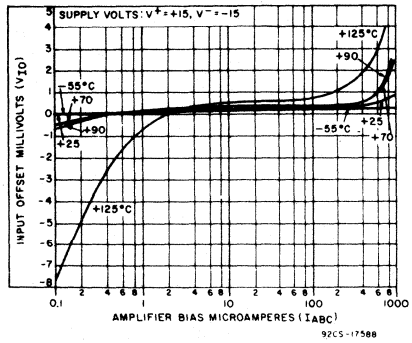


Fig.2 – Input offset voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

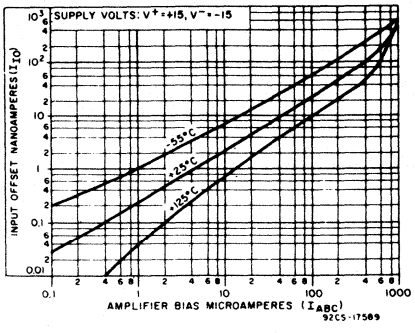


Fig.3 – Input offset current vs. amplifier bias current (I_{ABC}, terminal No.5).

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

CHARACTERISTIC	TEST CONDITIONS: Single Supply V^+ = 30 V, Dual Supply V^+ = 15 V, V^- = 15 V, I_{ABC} = 100 μA Unless Otherwise Specified	LIMITS: Min.	Typ.	Max.	UNITS
INPUT PARAMETERS					
Input Offset Voltage V_{IO}	T_A = 25°C	–	0.4	5	mV
	T_A = 0 to 70°C	–	–	7	mV
Input-Offset-Voltage Change $\lvert\Delta V_{IO}\rvert$	Change in V_{IO} Between I_{ABC} = 100 μA and I_{ABC} = 5 μA	–	1	8	mV
Input Offset Current I_{IO}	T_A = 25°C	–	0.02	0.2	μA
	T_A = 0 to 70°C	–	–	0.3	μA
Input Bias Current I_I	T_A = 25°C	–	0.2	0.50	μA
	T_A = 0 to 70°C	–	–	0.70	μA
Device Dissipation P_D	I_{out} = 0	8	10	12	mW
Common-Mode Rejection Ratio CMRR		70	110	–	dB
Common-Mode Input–Voltage Range V_{ICR}	V^+ = 30 V, High	27	28.8	–	V
	V^+ = 30 V, Low	1.0	0.5	–	V
	V^+ = 15 V	+12	+13.8	–	V
	V^- = 15 V	–14	–14.5	–	V
Unity Gain-Bandwidth	I_C = 7.5 mA, V_{CE} = 15 V, I_{ABC} = 500 μA	–	30	–	MHz
Open-Loop Bandwidth At –3 dB Point BW_{OL}	I_C = 7.5 mA, V_{CE} = 15 V, I_{ABC} = 500 μA	–	4	–	kHz
Total Harmonic Distortion (Class A Operation) THD	P_D = 220 mW	–	0.4	–	%
	P_D = 600 mW	–	1.4	–	
Amplifier Bias Voltage V_{ABC} (Terminal (No.5 to Terminal No.4)		–	0.68	–	V
Input Offset Voltage Temperature Coefficient $\Delta V_{IO}/\Delta T$		–	4	–	μV/°C
Power-Supply Rejection $\Delta V_{IO}/\Delta V$		–	15	150	μV/V
1/F Noise Voltage E_N	f = 10 Hz, I_{ABC} = 50 μA	–	18	–	$\eta V/\sqrt{Hz}$
1/F Noise Current I_N	f = 10 Hz, I_{ABC} = 50 μA	–	1.8	–	$pA/\sqrt{Hz}$
Differential Input Resistance R_I	I_{ABC} = 20 μA	0.50	1	–	MΩ
Differential Input Capacitance C_I	f = 1 MHz, V^+ = 30 V	–	2.6	–	pF

CA3094, CA3094A, CA3094B Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
	Single Supply V^+ = 30 V Dual Supply V^+ = 15 V, V^- = 15 V I_{ABC} = 100 μA Unless Otherwise Specified	Min.	Typ.	Max.	
OUTPUT PARAMETERS (Differential Input Voltage = 1V)					
Peak Output Voltage: (Terminal No. 6) With Q13 "ON" V^+_{OM} With Q13 "OFF" V_{OM}^-	V^+ = 30 V R_L = 2 kΩ to ground	 26 –	 27 0.01	 – 0.05	 V V
Peak Output Voltage: (Terminal No. 6) Positive V^+_{OM} Negative V_{OM}^-	V^+ = +15 V, V^- = -15 V R_L = 2 kΩ to −15 V	 +11 –	 +12 −14.99	0.5 – −14.95	 V V
Peak Output Voltage: (Terminal No. 8) With Q13 "ON" V^+_{OM} With Q13 "OFF" V_{OM}^-	V^+ = 30 V R_L = 2 kΩ to 30 V	 29.95 –	 29.99 0.040	 – –	 V V
Peak Output Voltage: (Terminal No. 8) Positive V^+_{OM} Negative V_{OM}^-	V^+ = 15 V, V^- = − 15 V R_L = 2 kΩ to + 15 V	 +14.95 –	 +14.99 14.96	 – –	 V V
Collector-to-Emitter Saturation Voltage (Terminal No. 8) $V_{CE(sat)}$	V^+ = 30 V I_C = 50 mA Terminal No.6 grounded	–	0.17	0.80	V
Output Leakage Current (Terminal No. 6 to Terminal No. 4)	V^+ = 30 V	–	2	10	μA
Composite Small-Signal Current Transfer Ratio (Beta) (Q_{12} and Q_{13}) h_{fe}	V^+ = 30 V V_{CE} = 5 V I_C = 50 mA	16,000	100,000	–	
Output Capacitance: Terminal No. 6 Terminal No. 8 C_O	f = 1 MHz All Remaining Terminals Tied to Terminal No. 4	 – –	 5.5 17	 – –	 pF pF
TRANSFER PARAMETERS					
Voltage Gain A	V^+ = 30 V I_{ABC} = 100 μA ΔV_{out} = 20 V R_L = 2 kΩ	20,000 86	100,000 100	– –	V/V dB
Forward Transconductance To Terminal No. 1 g_m		1650	2200	2750	μmhos
Slew Rate: Open Loop: Positive Slope Negative Slope	 I_{ABC} = 500 μA R_L = 2 kΩ	 – –	 500 50	 – –	 V/μs V/μs
Unity Gain (Non-Inverting, Compensated)	I_{ABC} = 500 μA R_L = 2 kΩ	–	0.7	–	V/μs

TYPICAL CHARACTERISTICS CURVES (Cont'd)

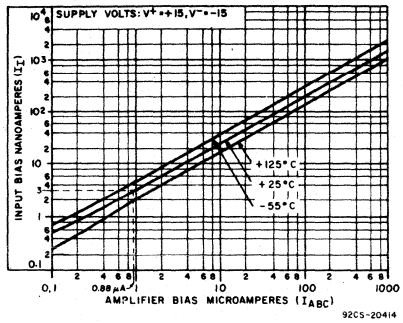


Fig.4 – Input bias current vs. amplifier bias current (I_{ABC}, terminal No.5).

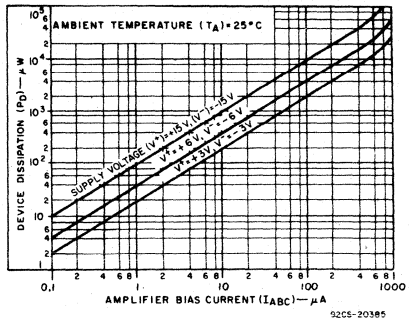


Fig.5 – Device dissipation vs. amplifier bias current (I_{ABC}, terminal No.5).

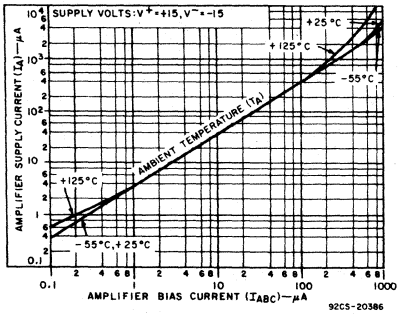


Fig.6 – Amplifier supply current vs. amplifier bias current (I_{ABC}, terminal No.5).

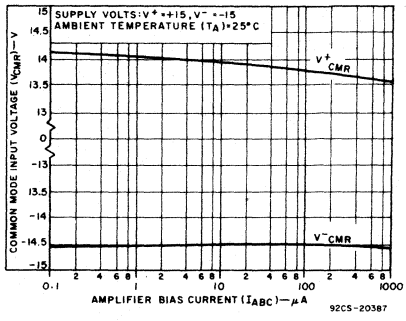


Fig.7 – Common mode input voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

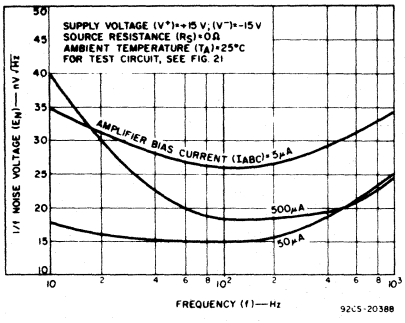


Fig.8 – 1/F Noise voltage vs. frequency.

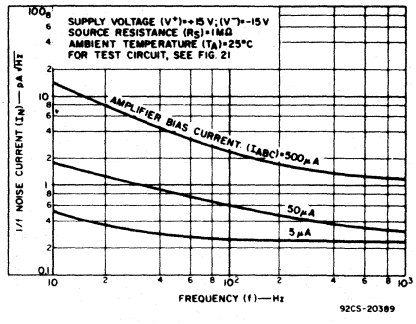


Fig.9 – 1/F Noise current vs. frequency.

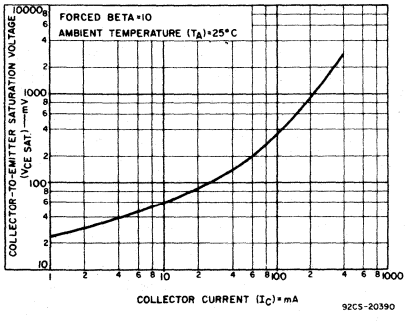


Fig.10 – Collector-emitter saturation voltage vs. collector current of output transistor Q_{13}.

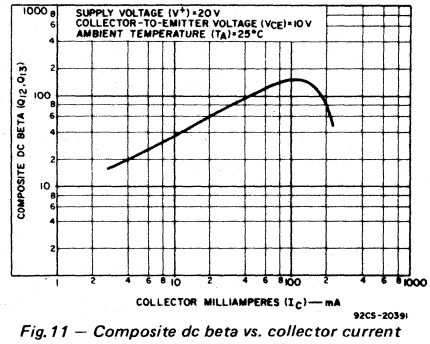


Fig.11 – Composite dc beta vs. collector current of Darlington-connected output transistors (Q_{12}, Q_{13}).

CA3094, CA3094A, CA3094B Types

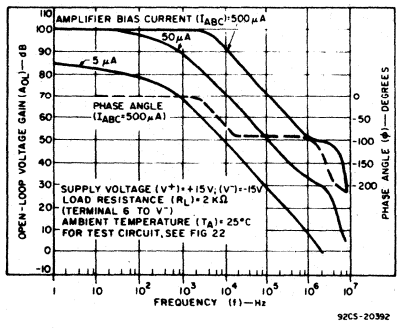


Fig. 12 – Open-loop voltage gain vs. frequency.

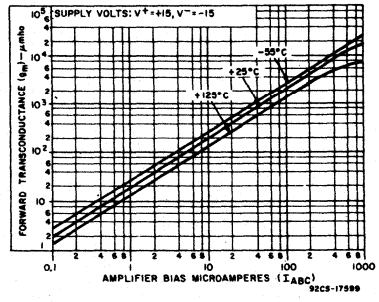


Fig. 13 – Forward transconductance vs amplifier bias current.

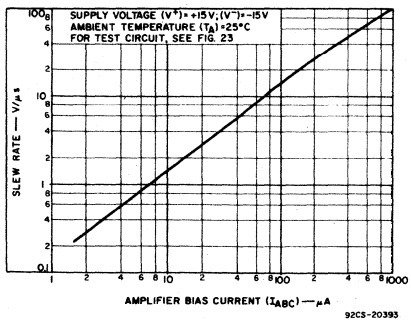


Fig. 14 – Slew rate vs amplifier bias current.

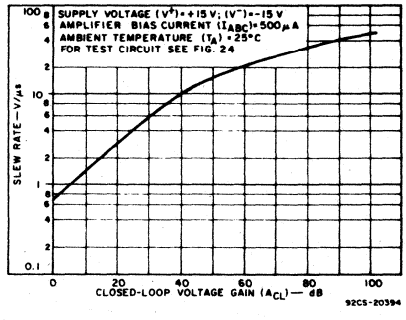


Fig. 15 – Slew rate vs closed-loop voltage gain.

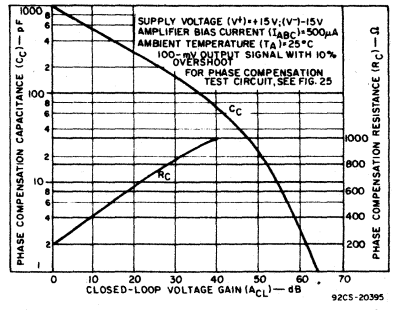


Fig. 16 – Phase compensation capacitance and resistance vs closed-loop voltage gain.

OPERATING CONSIDERATIONS

The "Sink" Output (terminal No.8) and the "Drive" Output (terminal No.6) of the CA3094 are not inherently current (or power) limited. Therefore, if a load is connected between terminal No.6 and terminal No.4 (V^- or ground), it is important to connect a current-limiting resistor between terminal 8 and terminal No.7 (V^+) to protect transistor Q_{13} under shorted load conditions. Similarly, if a load is connected between terminal No.8 and terminal No.7, the current-limiting resistor should be connected between terminal No.6 and terminal No.4 or ground. In circuit applications where the emitter of the output transistor is not connected to the most negative potential in the system, it is recommended that a 100-ohm current-limiting resistor be inserted between terminal No.7 and the V^+ supply.

TEST CIRCUITS

I/F Noise Measurement Circuit

When using the CA3094, A, or B audio amplifier circuits, it is frequently necessary to consider the noise performance of the device. Noise measurements are made in the circuit shown in Fig.21. This circuit is a 30-dB, non-inverting amplifier with emitter-follower output and phase compensation from terminal No.2 to ground. Source resistors (Rs) are set to 0.Ω or 1 MΩ for E noise and I noise measurements, respectively. These measurements are made at frequencies of 10, Hz, 100 Hz, and 1 kHz with a 1-Hz measurement bandwidth. Typical values for 1/f noise at 10 Hz and 50 μA I_{ABC} are E_n = 18 nV/$\sqrt{Hz}$ and I_N = 1.8 pA/$\sqrt{Hz}$.

TEST CIRCUITS

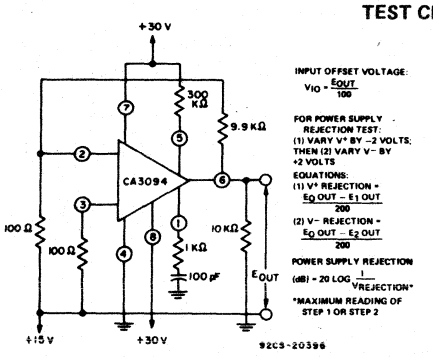


Fig. 17 – Input offset voltage and power-supply rejection test circuit.

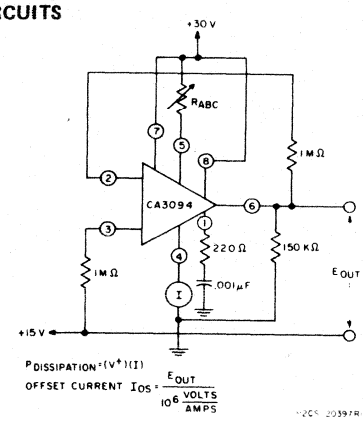


Fig. 18 – Input offset current test circuit.

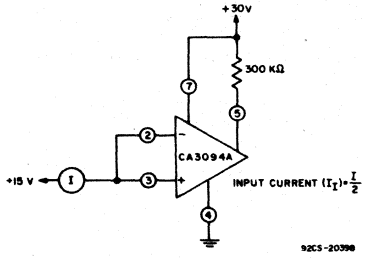


Fig. 19 – Input bias current test circuit.

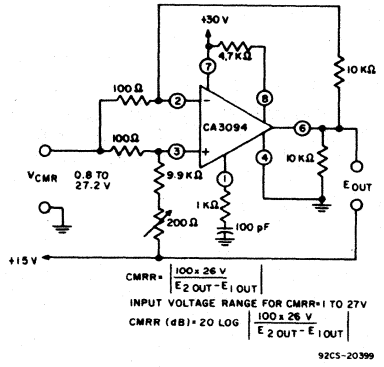


Fig. 20 – Common-mode range and rejection ratio test circuit.

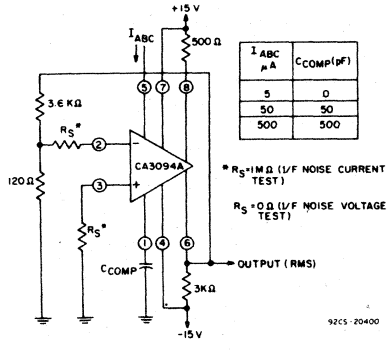


Fig. 21 – 1/F noise test circuit.

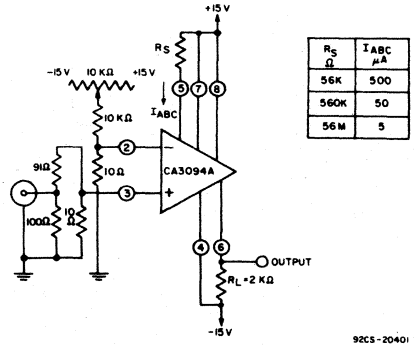


Fig. 22 – Open-loop gain vs frequency test circuit.

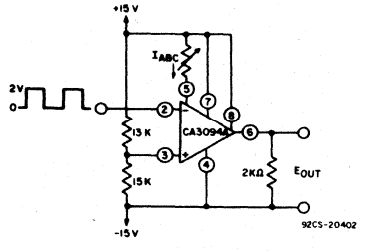


Fig. 23 – Open-loop slew rate vs I_{ABC} test circuit.

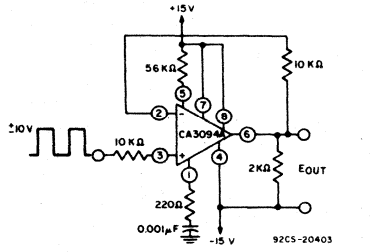
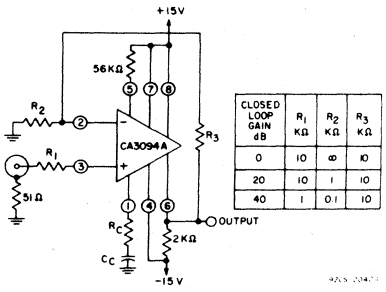


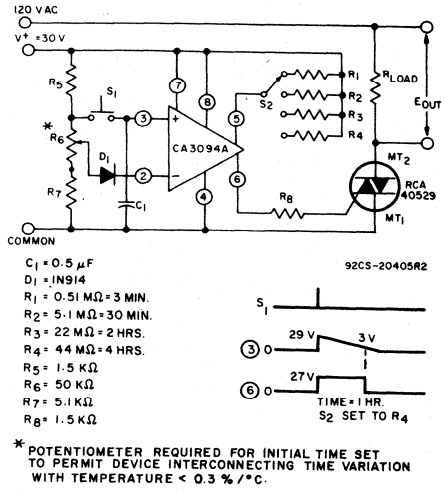
Fig. 24 – Slew rate vs. non-inverting unity gain test circuit.

TEST CIRCUITS (Cont'd)



CLOSED LOOP GAIN dB	R1 KΩ	R2 KΩ	R3 KΩ
0	10	∞	10
20	10	1	10
40	1	0.1	10

Fig.25 – Phase compensation test circuit.



* POTENTIOMETER REQUIRED FOR INITIAL TIME SET TO PERMIT DEVICE INTERCONNECTING TIME VARIATION WITH TEMPERATURE < 0.3 %/°C.

Fig.26 – Presettable analog timer.

TYPICAL APPLICATIONS

For Additional Application Information, refer to Application Note ICAN-6048 "Some Applications of a Programmable Power/ Switch Amplifier IC".

Design Considerations

The selection of the optimum amplifier bias current (I_{ABC}) depends on –

1. The Desired Sensitivity – the higher the I_{ABC}, the higher the sensitivity – i.e., a greater-drive current capability at the output for a specific voltage change at the input.
2. Required Input Resistance – the lower the I_{ABC}, the higher the input resistance.

If the desired sensitivity and requred input resistance are not known and are to be experimentally determined, or the anticipated equipment design is sufficiently flexible to tolerate a wide range of these parameters, it is recommended that the equipment designer begin his calculations with an I_{ABC} of 100 μA, since the CA3094 is characterized at this value of amplifier bias current.

The CA3094 is extremely versatile and can be used in a wide variety of applications.

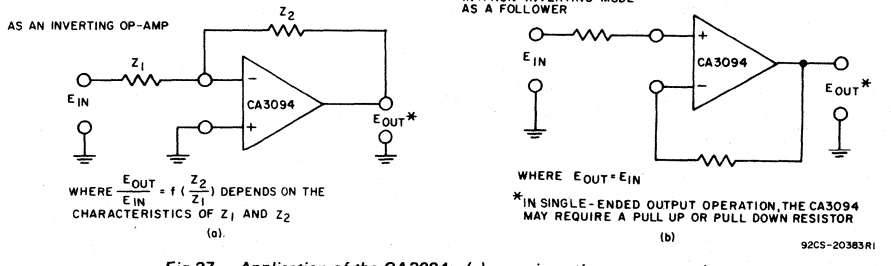
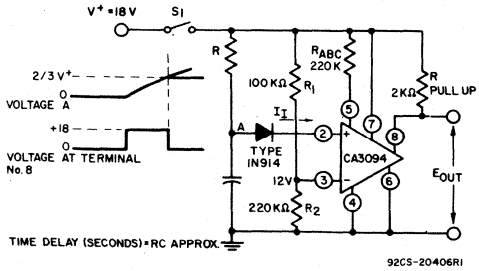


Fig.27 – Application of the CA3094: (a) as an inverting op-amp, and (b) in a non-inverting mode, as a follower.



Problem: To calculate the maximum value of R required to switch a 100-mA output current comparator

Given: $I_{ABC} = 5\ \mu A$, $R_{ABC} = 3.6\ M\Omega \approx \frac{18\ V}{5\ \mu A}$

$I_I = 500$ nA @ $I_{ABC} = 100\ \mu A$ (from Fig.4)

$I_I = 5\ \mu A$ can be determined by drawing a line on Fig.4 through $I_{ABC} = 100\ \mu A$ and $I_B = 500$ nA parallel to the typical $T_A = 25^oC$ curve.

Then: $I_I = 33$ nA @ $I_{ABC} = 5\ \mu A$

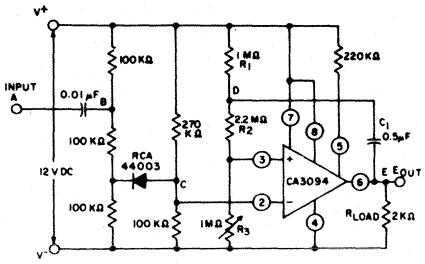
$$R_{max} = \frac{18-12\ volts}{33nA} = 180\ M\Omega\ @\ T_A = 25^oC$$

$$R_{max} = 180\ M\Omega \times 2/3^* = 120\ M\Omega\ @\ T_A = -55^oC$$

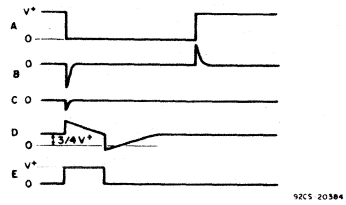
* Ratio of I_I at $T_A = +25^oC$ to I_I at $T_A = -55^oC$ for any given value of I_{ABC}.

Fig.28 – RC timer.

TYPICAL APPLICATIONS (Cont'd)



On a negative-going transient at input (A), a negative pulse at C will turn "on" the CA3094, and the output (E) will go from a low to a high level.



At the end of the time constant determined by C_1, R_1, R_2, R_3, the CA3094 will return to the "off" state and the output will be pulled low by R_{LOAD}. This condition will be independent of the interval when input A returns to a high level.

Fig.29 – RC timer triggered by external negative pulse.

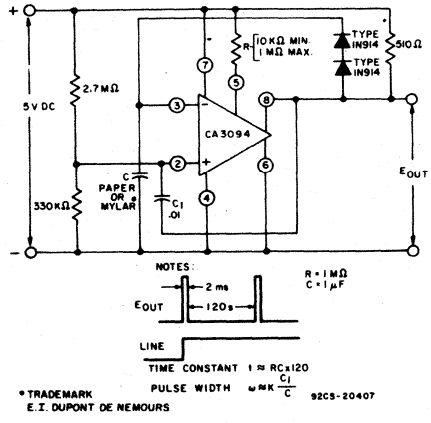


Fig.30 – Free-running pulse generator.

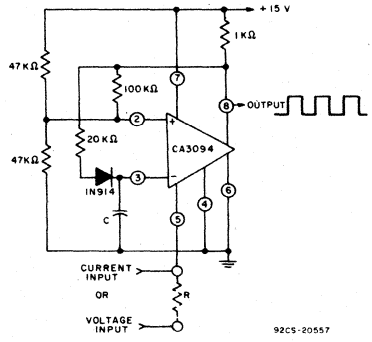


Fig.31 – Current or voltage-controlled oscillator.

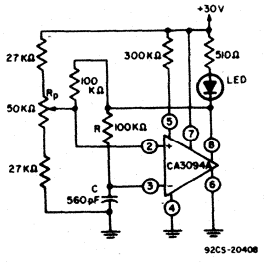


Fig.32 – Single-supply astable multivibrator.

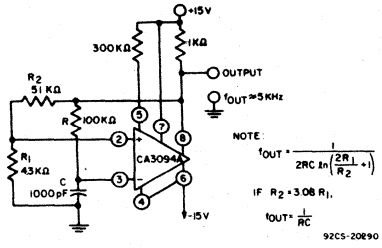
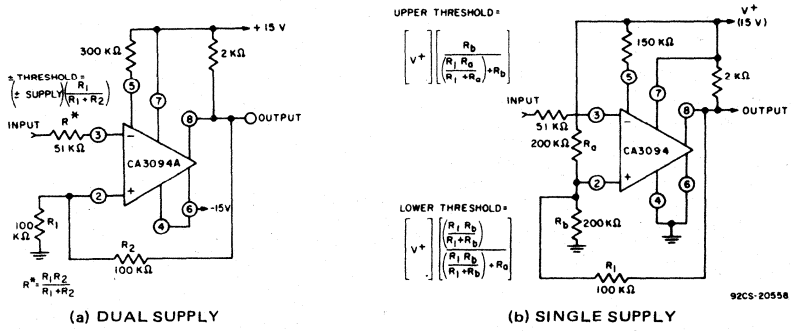


Fig.33 – Dual-supply astable multivibrator.

TYPICAL APPLICATIONS (Cont'd)



(a) DUAL SUPPLY (b) SINGLE SUPPLY

Fig.34 – Comparators (threshold detectors) –dual- and single-supply types.

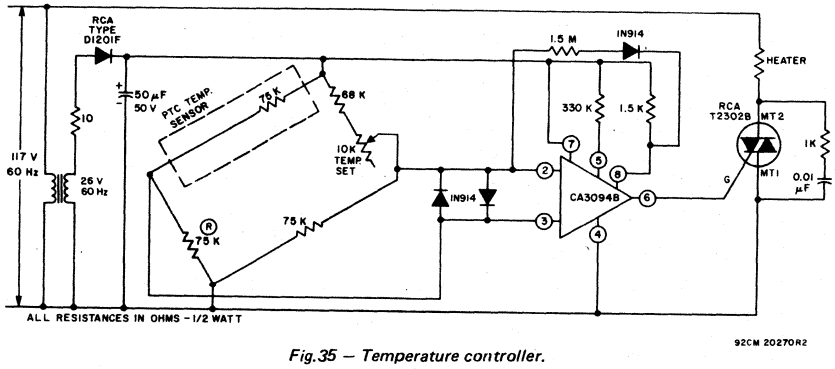


Fig.35 – Temperature controller.

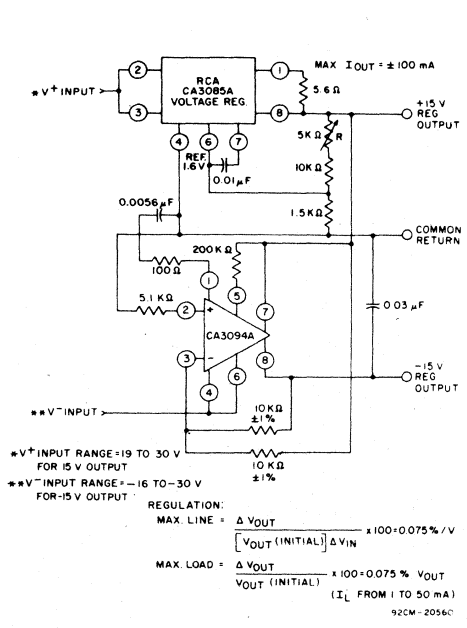


Fig.36 – Dual-voltage tracking regulator.

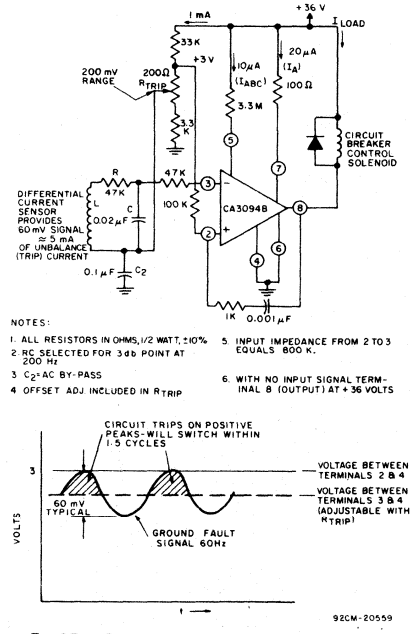
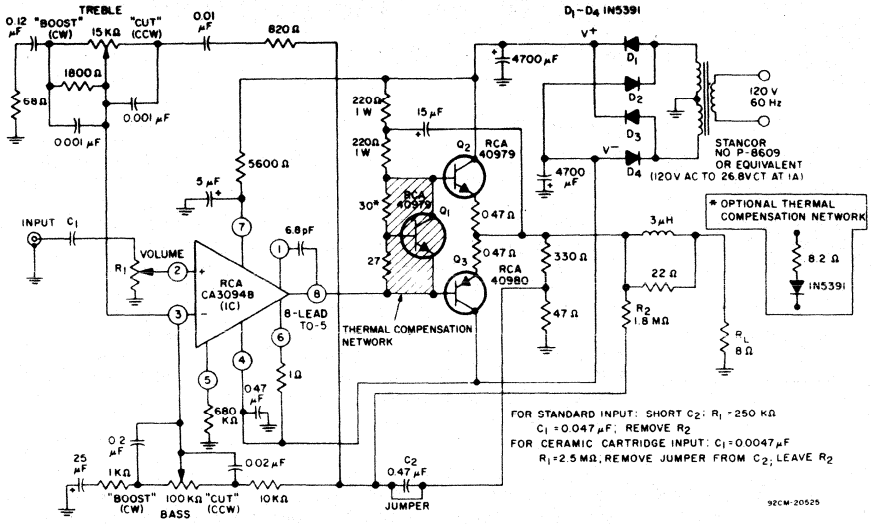


Fig.37 – Ground fault interrupter (GFI) and waveform pertinent to ground fault detector.

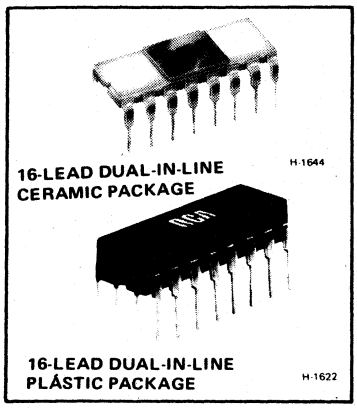


TYPICAL PERFORMANCE DATA
For 12-W Audio Amplifier Circuit

Power Output (8Ω load, Tone Control set at "Flat")		
Music (at 5% THD, regulated supply)	15	W
Continuous (at 0.2% IMD, 60 Hz & 2 kHz mixed in a 4:1 ratio, unregulated supply) See Fig. 8 In ICAN-6048	12	W
Total Harmonic Distoration		
At 1 W, unregulated supply	0.05	%
At 12 W, unregulated supply	0.57	%
Voltage Gain	40	dB
Hum and Noise (Below continuous Power Output)	83	dB
Input Resistance	250	kΩ
Tone Control Range	See Fig. 9 In ICAN-6048	

Fig.38 — 12-watt amplifier circuit featuring true complementary-symmetry output stage with CA3094 in driver stage.

CA3060, CA3060A Types



Operational Transconductance Amplifier Arrays

Features:

- *Low power consumption - as low as 100 μW per amplifier*
- *Independent biasing for each amplifier*
- *High forward transconductance*
- *Programmable range of input characteristics*
- *Low input bias and input offset current*
- *High input and output impedance*
- *No effect on device under output short-circuit conditions*
- *Zener diode bias regulator*

Applications:

- *For low power conventional operational amplifier applications*
- *Active filters*
- *Comparators*
- *Gyrators*
- *Mixers*
- *Modulators*
- *Multiplexers*
- *Multipliers*
- *Strobing and gating functions*
- *Sample and hold functions*

RCA-CA3060AD, CA3060BD, CA3060D, and CA3060E, monolithic integrated circuits, are arrays of three independent Operational Transconductance Amplifiers. This type of amplifier is a new circuit concept that has the generic characteristics of an operational voltage amplifier with the exception that the forward gain characteristic is best described by transconductance rather than voltage gain (open-loop voltage gain is the product of the transconductance and the load resistance, $g_m R_L$). When operated into a suitable load resistor and with provisions for feedback, these amplifiers are well suited for a wide variety of operational-amplifier and related applications. In addition, the extremely high output impedance makes these types particularly well suited for service in active filters.

The three amplifiers in the CA3060 family are identical push-pull Class A types which can be independently biased to achieve a wide range of characteristics for specific application. The electrical characteristics of each amplifier are a function of the amplifier bias current (I_{ABC}). This feature offers the system designer maximum flexibility with regard to output current capability, power consumption, slew rate, input resistance, input bias current, and input offset current. The linear variation of the parameters with respect to bias and the ability to maintain a constant dc level between input and output of each amplifier also makes the CA3060 suitable for a variety of non-linear applications such as mixers, multipliers, and modulators.

In addition; the types in the CA3060 family incorporate a unique Zener diode regulator system that permits current regulation below supply voltages normally associated with such systems.

Generic applications of the OTA are described in ICAN-6668, Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers.

The CA3060AD, CA3060BD, nd CA3060D are supplied in a hermetic 16-lead dual-in-line ceramic package which can be operated over the full military temperature range, −55° C to +125° C. The CA3060E is supplied in a 16-lead dual-in-line plastic package and is operational from −40° C to +85° C.

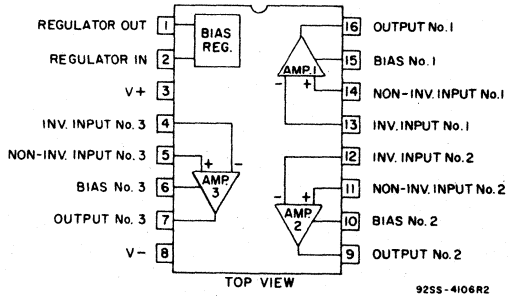


Fig. 1 — Functional block diagram for each type in the CA3060 family.

MAXIMUM RATINGS, *Absolute Maximum Values at T_A = 25°C*

DC Supply Voltage (between V^+ and V^- terminals):
CA3060AD, CA3060BD, CA3060E ..... 36V (±18V)
CA3060D ..... 14 V (±7V)

Differential Input Voltage (each amplifier):
CA3060AD, CA3060BD, CA3060E ..... ±5V
CA3060D ..... ±5V

DC Input Voltage ..... V^+ to V^-

Input Signal Current (each amplifier of each type): ..... ±1 mA

Amplifier Bias Current (each amplifier of each type) ..... 2 mA

Bias Regulator Input Current ..... -5 mA

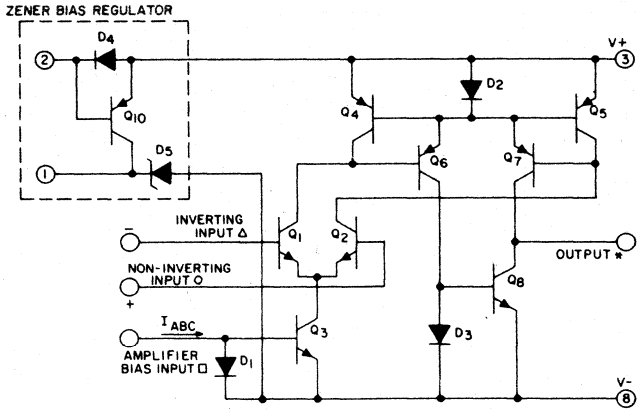
Output Short-Circuit Duration* ..... No limitation

Device Dissipation:
Total Package of each type up to T_A = 75°C ..... 490 mW
Above T_A = 75°C ..... Derate linearly 6.67 mW/°C

Temperature Range:
Operating –
CA3060AD, CA3060BD, CA3060D ..... -55 to +125°C
CA3060E ..... -40 to +85°C
Storage –
CA3060AD, CA3060BD, CA3060D,
CA3060E ..... -65 to +150°C

Lead Temperature (During Soldering):
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm)
from case for 10s max ..... +300°C

*Short circuit may be applied to ground or to either supply.



Δ INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 13, 12 AND 4, RESPECTIVELY
O NON-INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS TERMINAL Nos. 14, 11, AND 5, RESPECTIVELY
* OUTPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 16, 9, AND 7, RESPECTIVELY
□ AMPLIFIER BIAS CURRENT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 15, 10, AND 6, RESPECTIVELY

NOTE: A complete schematic diagram of the OTA is shown on Page 6. 92CS-15860RI

Fig.2—Simplified schematic diagram showing bias regulator and one operational transconductance amplifier for each type of the CA3060 family.

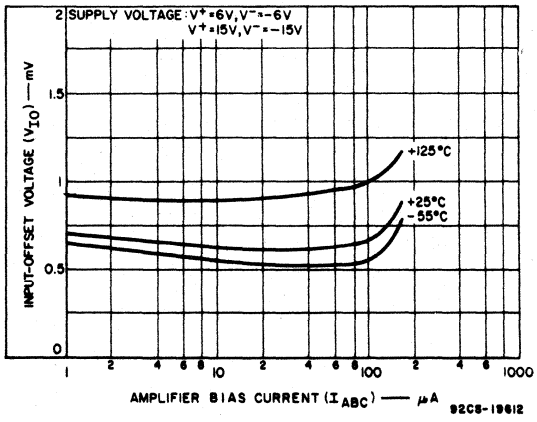


Fig.3—Input offset voltage vs. amplifier bias current.

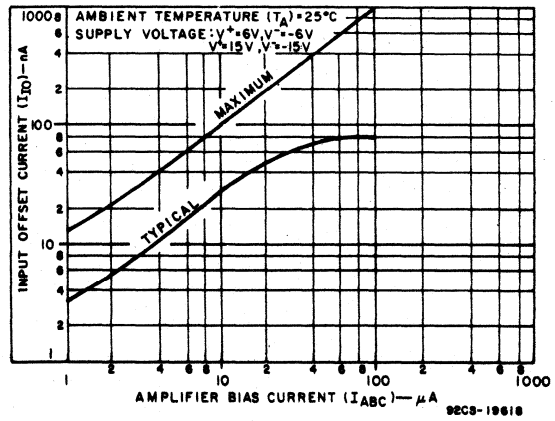


Fig.4—Input offset current vs. amplifier bias current.

CA3060, CA3060A Types

ELECTRICAL CHARACTERISTICS (CA3060D)

For each amplifier at T_A = 25°C, V^+ = 6 V, V^- = -6 V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVES Fig.	LIMITS — Amplifier Bias Current I_{ABC} = 1 μA MIN.	TYP.	MAX.	I_{ABC} = 10 μA MIN.	TYP.	MAX.	I_{ABC} = 100 μA MIN.	TYP.	MAX.	UNITS
STATIC CHARACTERISTICS												
Input Offset Voltage	V_{IO}	3	–	1	5	–	1	5	–	1	5	mV
Input Offset Current	I_{IO}	4	–	3	14	–	30	100	–	250	1000	nA
Input Bias Current	I_{IB}	5a, b	–	33	70	–	300	550	–	2500	5000	nA
Peak Output Current	I_{OM}	6a, b	1.3	2.3	–	15	26	–	150	240	–	μA
Peak Output Voltage: Positive	V_{OM^+}	7	4.6	5	–	4.5	4.8	–	4.5	4.7	–	V
Peak Output Voltage: Negative	V_{OM^-}	7	5.8	5.95	–	5.8	5.95	–	5.7	5.9	–	V
Amplifier Supply Current (each amplifier)	I_A	8a, b	–	8.5	14	–	85	120	–	850	1200	μA
Power Consumption (each amplifier)	P	–	–	0.10	0.17	–	1	1.45	–	10	14.5	mW
Input Offset-Voltage Sensitivity■: Positive	$\Delta V_{IO}/\Delta V^+$	–	–	1.5	120	–	2	120	–	2	120	μV/V
Input Offset-Voltage Sensitivity■: Negative	$\Delta V_{IO}/\Delta V^-$	–	–	20	120	–	20	120	–	30	120	μV/V
Amplifier Bias Voltage*	V_{ABC}	9	–	0.54	–	–	0.60	–	–	0.66	–	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)												
Forward Transconductance (large signal)	g_{21}	10a, b	0.3	1.55	–	3	18	–	30	102	–	mmho
Common-Mode Rejection Ratio	CMRR	–	70	110	–	70	110	–	70	90	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–	4.4 to -5.1 min. 4.7 to -5.3 typ.			4.3 to -5 min. 4.6 to -5.2 typ.			4.3 to -5 min. 4.6 to -5.2 typ.			V
Slew Rate (Test ckt., Fig. 13	SR		–	0.1	–	–	1	–	–	8	–	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	–	20	–	–	45	–	–	110	–	kHz
Input Impedance Components: Resistance	R_I	12	800	1600	–	90	170	–	10	20	–	kΩ
Input Impedance Components: Capacitance at 1 MHz	C_I	–	–	2.7	–	–	2.7	–	–	2.7	–	pF
Output Impedance Components: Resistance	R_O	14	–	200	–	–	20	–	–	2	–	MΩ
Output Impedance Components: Capacitance at 1 MHz	C_O	–	–	4.5	–	–	4.5	–	–	4.5	–	pF
ZENER BIAS REGULATOR CHARACTERISTICS (at T_A = 25°C, I_Z = 0.1 mA)						MIN.	TYP.	MAX.				
Voltage	V_Z	15	Temp. Coeff. = 3 mV/°C			6.2	6.7	7.9				V
Impedance	Z_Z	–					200	300				Ω

* Temperature-Coefficient; -2.2 mV/°C (at V_{ABC} = 0.54 V, I_{ABC} = 1 μA; -2.1 mV/°C (at V_{ABC} = 0.060 V, I_{ABC} = 10 μA); -1.9 mV/°C (at V_{ABC} = 0.66 V, I_{ABC} = 100 μA)

■ Conditions for Input Offset Voltage and Supply Sensitivity:

(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test —

V^+ is reduced to 5 volts for V^+ sensitivity

V^- is reduced to -5 volts for V^- sensitivity

(b) V^+ sensitivity in μV/V = $\frac{\text{Voffset - Voffset for +5 V and -6 V supplies}}{\text{1 volt}}$

V^- sensitivity in μV/V = $\frac{\text{Voffset - Voffset for -5 V and +6 V supplies}}{\text{1 volt}}$

ELECTRICAL CHARACTERISTICS (CA3060AD, CA3060BD, CA3060E)

For each amplifier at T_A = 25°C, V^+ = 15 V, V^- = -15 V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVE Fig.	LIMITS Amplifier Bias Current I_{ABC} = 1 μA MIN.	TYP.	MAX.	I_{ABC} = 10 μA MIN.	TYP.	MAX.	I_{ABC} = 100 μA MIN.	TYP.	MAX.	UNITS
			CA3060BD						CA3060AD CA3060BD CA3060E			
STATIC CHARACTERISTICS												
Input Offset Voltage	V_{IO}	3	–	1	5	–	1	5	–	1	5	mV
Input Offset Current	I_{IO}	4	–	3	14	–	30	100	–	250	1000	nA
Input Bias Current	I_{IB}	5a,b	–	33	70	–	300	550	–	2500	5000	nA
Peak Output Current	I_{OM}	6a,b	1.3	2.3		15	26	–	150	240	–	μA
Peak Output Voltage: Positive	V_{OM^+}	7	12	13.6	–	12	13.6	–	12	13.6	–	V
Negative	V_{OM^-}		12	14.7	–	12	14.7	–	12	14.7	–	
Amplifier Supply Current (each amplifier)	I_A	8a,b	–	8.5	14	–	85	120	–	850	1200	μA
Power Consumption (each amplifier)	P_T	–	–	0.26	0.42	–	2.6	3.6	–	26	36	mW
Input Offset-Voltage Sensitivity■: Positive	$\Delta V_{IO}/\Delta V^+$	--	–	1.5	150	–	2	150	–	2	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	20	150	–	20	150	–	30	150	
Amplifier Bias Voltage*	V_{ABC}	9	–	0.54	–	–	0.60	–	–	0.66	–	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)												
Forward Transconductance (large signal)	g_{21}	10a,b	0.3	1.55	–	3	18	–	30	102	–	mmho
Common-Mode Rejection Ratio	CMRR	–	70	110	–	70	110	–	70	90	–	dB
Common-Mode Input Voltage Range	V_{ICR}	–	+12 to -12 min. +13 to -14 typ.			+12 to -12 min. +13 to -14 typ.			+12 to -12 min. +13 to -14 typ.			V
Slew Rate (Test ckt., Fig. 13)	SR	–	–	0.1	–	–	1	–	–	8	–	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	-	20	–	–	45	–	–	110	–	kHz
Input Impedance Components: Resistance	R_I	12	800	1600	–	90	170	–	10	20	–	kΩ
Capacitance at 1 MHz	C_I	–	–	2.7	–	–	2.7	–	–	2.7	–	pF
Output Impedance Components: Resistance	R_O	14	–	200	–	–	20	–	–	2	–	MΩ
Capacitance at 1 MHz	C_O	–	–	4.5	–	–	4.5	–	–	4.5	–	pF
ZENER BIAS REGULATOR CHARACTERISTICS (at T_A=25°C, I_Z = 0.1 mA)						MIN.	TYP.	MAX.				
Voltage	V_Z	15	Temp. Coeff. = 3 mV/°C			6.2	6.7	7.9				V
Impedance	Z_Z	–					200	300				Ω

* Temperature Coefficient; -2.2 mV/°C (at V_{ABC} = 0.54 V, I_{ABC} = 1 μA; -2.1 mV/°C (at V_{ABC} = 0.060 V, I_{ABC} = 10 μA); -1.9 mV/°C (at V_{ABC} = 0.66 V, I_{ABC} = 100 μA)

■ Conditions for Input Offset Voltage and Supply Sensitivity:

(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test ---

V^+ is reduced to 13 volts for V^+ sensitivity

V^- is reduced to −13 volts for V^- sensitivity

(b) V^+ sensitivity in μV/V = $\frac{\text{Voffset - Voffset for +13 V and −15 V supplies}}{\text{1 volt}}$

V^- sensitivity in μV/V = $\frac{\text{Voffset - Voffset for −13 V and +15 V supplies}}{\text{1 volt}}$

CA3060, CA3060A Types

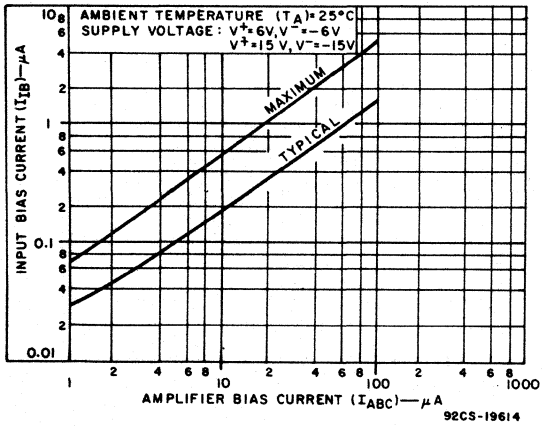


Fig.5a—Input bias current vs. amplifier bias current

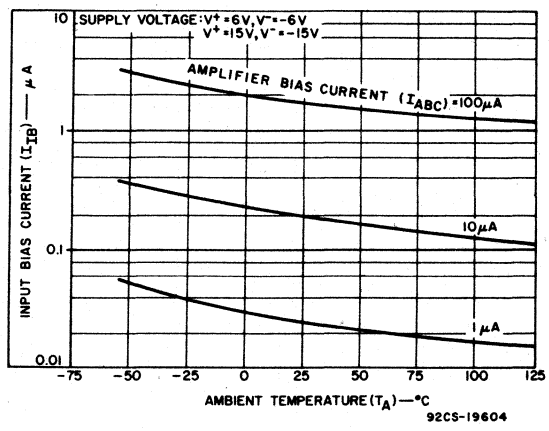


Fig.5b—Input bias current vs. ambient temperature.

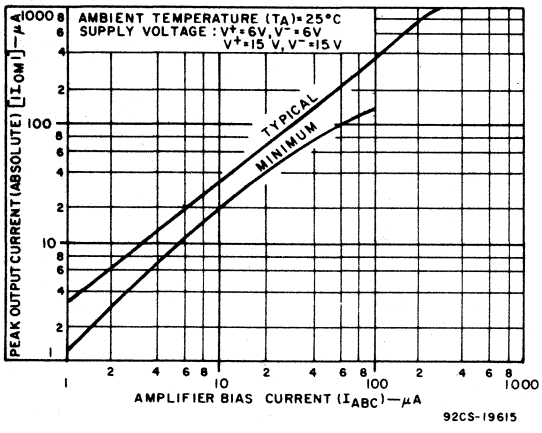


Fig.6a—Peak output current vs. amplifier bias current.

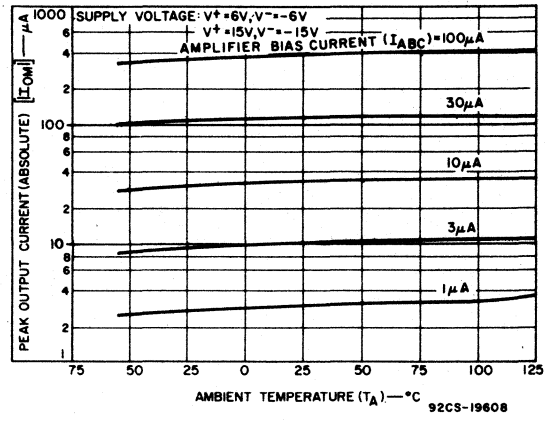


Fig.6b—Peak output current vs. ambient temperature.

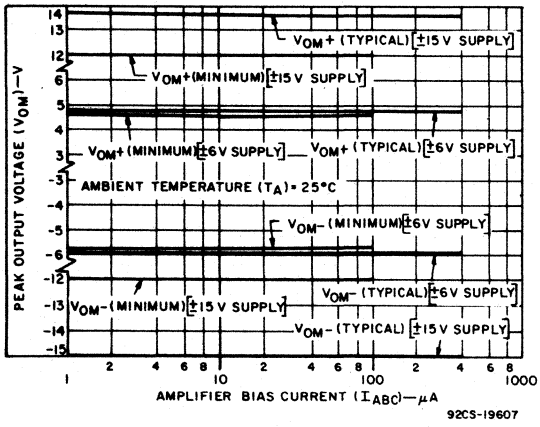


Fig.7—Peak output voltage vs. amplifier bias current.

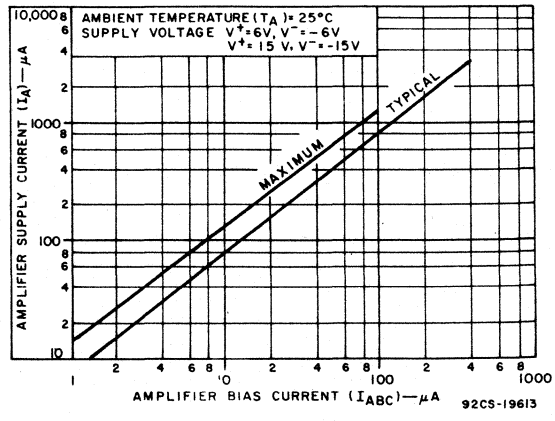


Fig.8a—Amplifier supply current (each amplifier) vs. amplifier bias current.

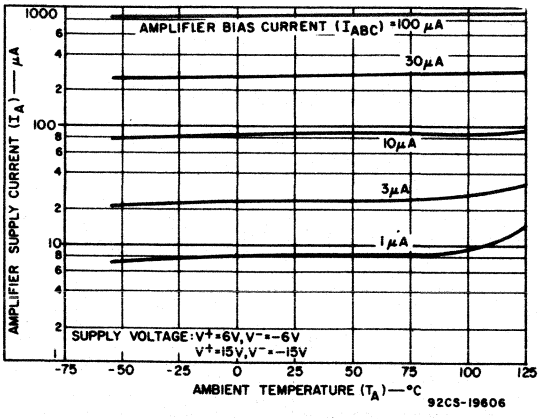


Fig.8b—Amplifier supply current (each amplifier) vs. ambient temperature.

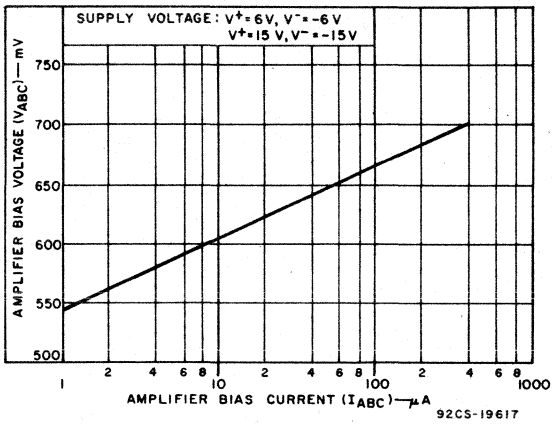


Fig.9—Amplifier bias voltage vs. amplifier bias current.

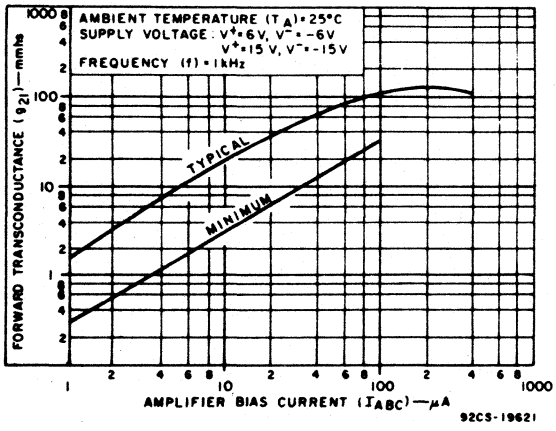


Fig.10a—Forward transconductance vs. amplifier bias current.

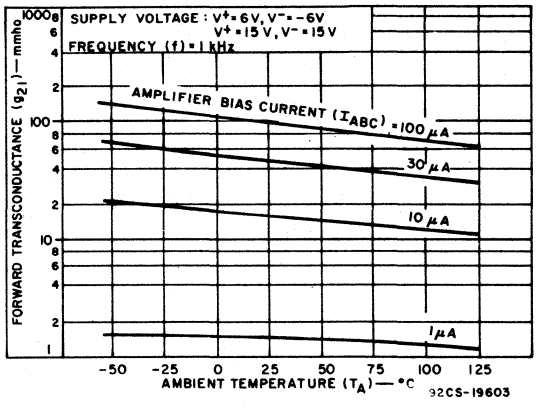


Fig.10b—Forward transconductance vs. ambient temperature.

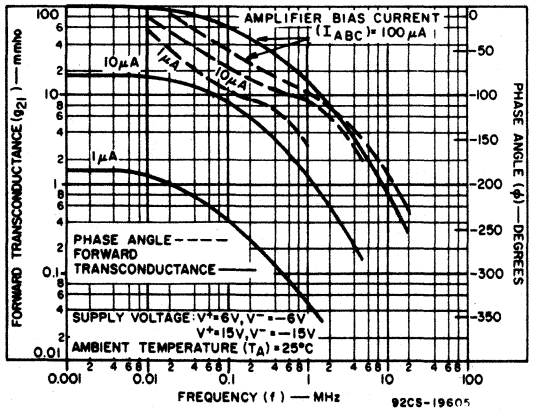


Fig.11—Forward transconductance vs. frequency.

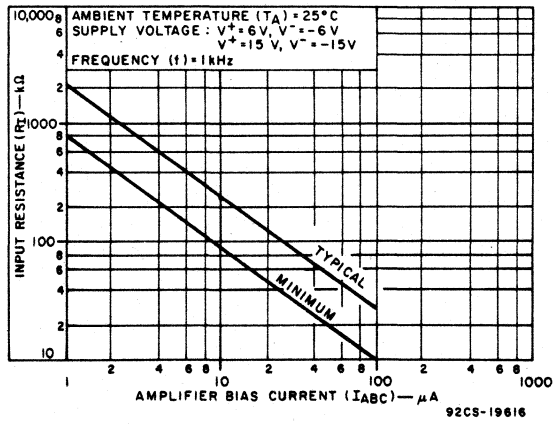
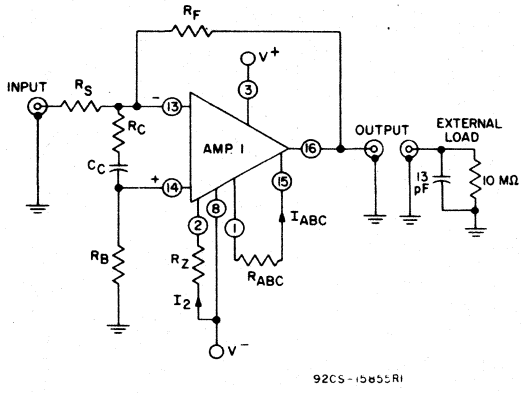


Fig.12—Input resistance vs. amplifier bias current.



V_Z is measured between terminals 1 and 8.

V_{ABC} is measured between terminals 15 and 8.

$$R_Z = \frac{[(V^+)-(V^-)-0.7]}{I_2}, \quad R_{ABC} = \frac{V_Z - V_{ABC}}{I_{ABC}}$$

Supply Voltage: for both ±6 V and ±15 V.

TYPICAL SLEW RATE TEST CIRCUIT PARAMETERS

I_{ABC}	SLEW RATE	I_2	R_{ABC}	R_S	R_F	R_B	R_C	C_C
μA	V/μs	μA	ohms					μF
100	8	200	62 k	100k	100k	51k	100	0.02
10	1	200	620k	1M	1M	510k	1k	0.005
1	0.1	2	6.2M	10M	10M	5.1M	∞	0

Fig. 13—Slew rate test circuit for amplifier No. 1 of CA3060.

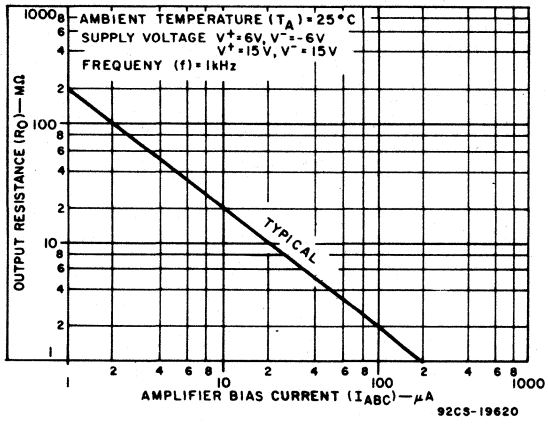


Fig. 14—Output resistance vs. amplifier bias current.

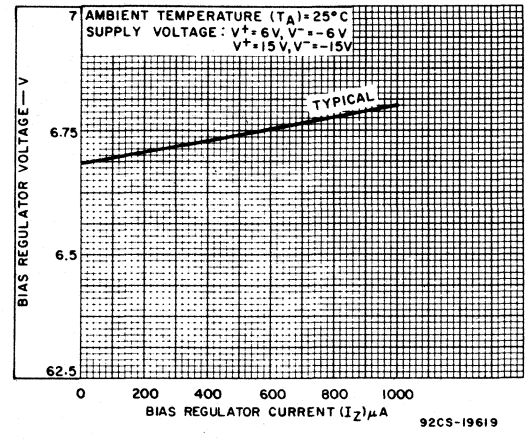


Fig. 15—Bias regulator voltage vs. bias regulator current.

OPERATING CONSIDERATIONS

The CA3060 consists of three operational amplifiers similar in form and application to conventional operational amplifiers but sufficiently different from the standard operational amplifier (op-amp) to justify some explanation of their characteristics. The amplifiers incorporated in the CA3060 are best described by the term Operational Transconductance Amplifier (OTA). The characteristics of an ideal OTA are similar to those of an ideal op-amp except that the OTA has an extremely high output impedance. Because of this inherent characteristic the output signal is best defined in terms of current which is proportional to the difference between the voltages of the two input terminals. Thus, the transfer characteristic is best described in terms of transconductance rather than voltage gain. Other than the difference given above, the characteristics tabulated on pages 3 and 4 of this data bulletin are similar to those of any typical op-amp.

The OTA circuitry incorporated in the CA3060 (See Fig. 16) provides the equipment designer with a wider variety of circuit arrangements than does the standard op-amp; because as the curves in the data bulletin indicate, the user may select the optimum circuit conditions for a specific application simply by varying the bias conditions of each amplifier. If low power consumption, low bias, and low offset current, or high input impedance are primary design requirements, then low current operating conditions may be selected. On the other hand, if operation into a moderate load impedance is the primary consideration, then higher levels of bias may be used.

Bias Considerations for Op-Amp Applications

The operational transconductance amplifiers allow the circuit designer to select and control the operating conditions of the circuit merely by the adjustment of the input bias current I_{ABC}. This enables the designer to have complete control over transconductance, peak output current and total power consumption independent of supply voltage.

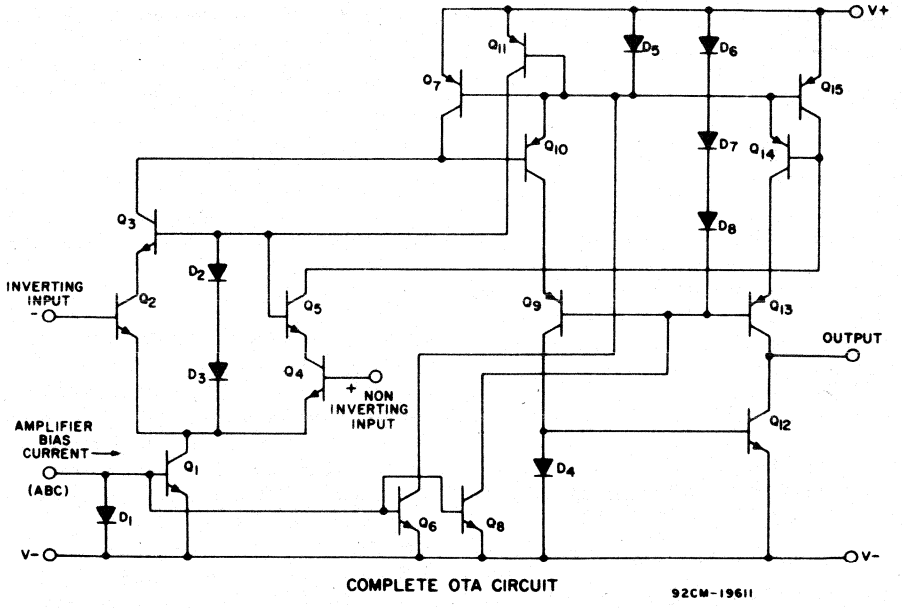


Fig. 16—Complete schematic diagram showing bias regulator and one of the three operational transconductance amplifiers.

In addition, the high output impedance makes these amplifiers ideal for applications where current summing is involved.

The design of a typical operational amplifier circuit (See Fig. 17) would proceed as follows:

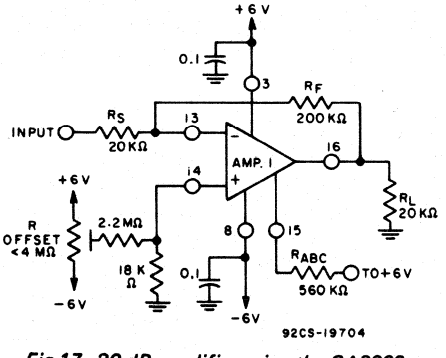


Fig. 17—20-dB amplifier using the CA3060.

Circuit Requirements
Closed loop voltage gain = 10 (20 dB)
Offset voltage adjustable to zero
Current drain as low as possible
Supply voltage = ±6 V
Maximum input voltage = ±50 mV
Input resistance = 20 kΩ
Load resistance = 20 kΩ
Device: CA3060

Calculation

1. Required transconductance g_{21}.
   Assume that the open loop gain A_{OL} must be at least ten times the closed loop gain. Therefore, the forward transconductance required is given by

$$g_{21} = A_{OL}/R_L$$

$$= 100/18\ k\Omega$$

$$\cong 5.5\ mmho$$

(R_L = 20 kΩ in parallel with 200 kΩ

$\cong$ 18 kΩ)

2. Selection of suitable amplifier bias current.
   The amplifier bias current is selected from the minimum value curve of transconductance (Fig. 10a) to assure that the amplifier will provide sufficient gain. For the required g_{21} of 5.5 mmho an amplifier bias current I_{ABC} of 20 μA is suitable.

3. Determination of Output Swing Capability.
   For a loop gain of 10 the output swing is ±0.5 V and the peak load current 25 μA. However, the amplifier must also supply the necessary current through the feedback resistor and for R_S = 20 kΩ than R_F = 200 kΩ if A_{OL} = 10. Therefore, the feedback loading = 0.5/200 kΩ = 2.5 μA.

   The total amplifier current output requirements are, therefore, ±27.5 μA. Referring to the data given in Fig. 6a we see that for an amplifier bias current of 20 μA the amplifier output current is ±40 μA. This is obviously adequate and it is not necessary to change the amplifier bias current I_{ABC}.

4. Calculation of bias resistance.
   For minimum supply current drain the amplifier bias current I_{ABC} should be fed directly from the supplies and not from the bias regulator. The value of the resistor R_{ABC} may be directly calculated using Ohm's law.

$$R_{ABC} = \frac{V_{SUP} - V_{ABC}}{I_{ABC}}$$

$$R_{ABC} = \frac{12 - 0.63}{20 \times 10^{-6}}$$

$$= 568.5\ k\Omega \text{ or } \cong 560\ k\Omega$$

5. Calculation of offset adjustment circuit.
   In order to reduce the loading effect of the offset adjustment circuit on the power supply, the offset control should be arranged to provide the necessary offset current. The source resistance of the non-inverting input is made equal to the source resistance of the inverting input.

i.e. $\frac{20 \times 200 \times 10^6 \text{ ohms}}{220 \times 10^3} \cong 18\ k\Omega$

Because the maximum offset voltage is 5 mV and an additional increment due to the offset current (Fig. 4) flowing through the source resistance

(i.e. $200 \times 10^{-9} \times 18 \times 10^3$ volts), therefore,

the Offset Voltage Range = 5 mV + 3.6 mV = ±8.6 mV

The current necessary to provide this offset is

$$\frac{8.6 \times 10^{-3}}{18 \times 10^3} \text{ or } 0.48\ \mu A$$

With a supply voltage of ±6 V, this current can be provided by a 10 MΩ resistor. However, the stability of such a resistor is often questionable and a more realistic value of 2.2 MΩ was used in the final circuit.

OTHER CONSIDERATIONS

Capacitance Effects

The CA3060 is designed to operate at such low power levels that high impedance circuits must be employed. In designing such circuits, particularly feedback amplifiers, stray circuit capacitance must always be considered because of its adverse effect on frequency response and stability. For example a 10-kΩ load with a stray capacitance of 15 pF has a time constant of 1 MHz. Fig. 18 illustrates how a 10-kΩ 15-pF load modifies the frequency characteristic.

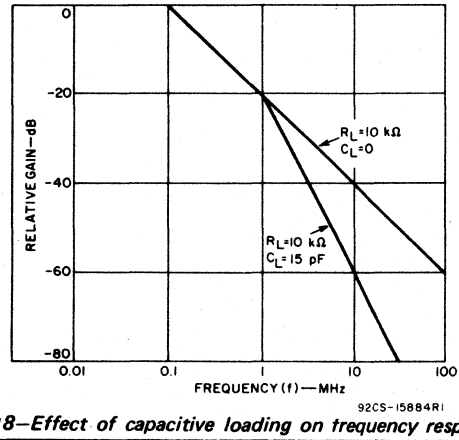


Fig. 18—Effect of capacitive loading on frequency response.

Capacitive loading also has an effect on slew rate; because the peak output current is established by the amplifier bias current, I_{ABC} (see Fig. 6a), the maximum slew rate is limited to the maximum rate at which the capacitance can be charged by the I_{OM}. Therefore,

$$SR = dV/dt = I_{OM}/C_L$$

where C_L is the total load capacitance including strays. This relationship is shown graphically in Fig. 19. When measuring slew rate for this data bulletin, care was taken to keep the total capacitive loading to 13 pF.

Phase Compensation

In many applications phase compensation will not be required for the amplifiers of the CA3060. When needed, compensation may easily be accomplished by a simple RC network at the input of the amplifier as shown in Fig. 13. The values given in Fig. 13 provide stable operation for the critical unity gain condition, assuming that capacitive loading on the output is 13 pF or less. Input phase compensation is recommended in order to maintain the highest possible slew rate.

In applications such as integrators, two OTAs may be cascaded to improve current gain. Compensation is best accomplished in this case with a shunt capacitor at the output of the first amplifier. The high gain following compensation assures a high slew rate.

APPLICATIONS

Having determined the operating points of the CA3060 amplifiers, they can now function in the same manner as conventional op-amps, and thus, are well suited for most op-amp applications, including inverting and non-inverting amplifiers, integrators, differentiators, summing amplifiers etc.

TRI-LEVEL COMPARATOR

Tri-level comparator circuits are an ideal application for the CA3060 since it contains the requisite three amplifiers. A tri-level comparator has three adjustable limits. If either the upper or lower limit is exceeded, the appropriate output is activated until the input signal returns to a selected intermediate limit. Tri-level comparators are particularly suited to many industrial control applications.

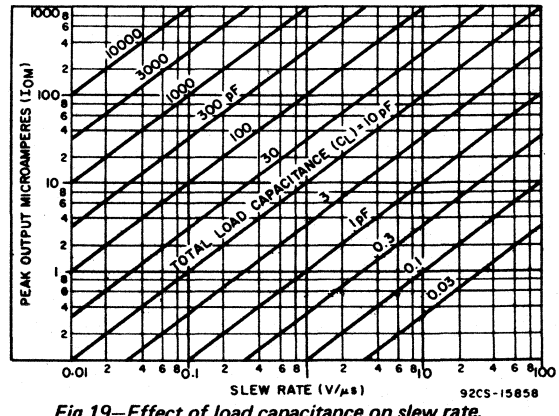


Fig. 19—Effect of load capacitance on slew rate.

Circuit Description

Fig. 20 shows the block diagram of a tri-level comparator using the CA3060. Two of the three amplifiers are used to compare the input signal with the upper-limit and lower-limit reference voltages. The third amplifier is used to compare the input signal with a selected value of intermediate-limit reference voltage. By appropriate selection or resistance ratios this intermediate-limit may be set to any voltage between the upper-limit and lower-limit values. The output of the upper-limit and lower-limit comparator sets the corresponding upper or lower-limit flip-flop. The activated flip-flop retains its state until the third comparator (intermediate-limit) in the CA3060 initiates a reset function, thereby indicating that the signal voltage has returned to the intermediate-limit selected. The flip-flops employ two CA3086 transistor-array IC's, with circuitry to provide separate "SET" and "POSITIVE OUTPUT" terminals.

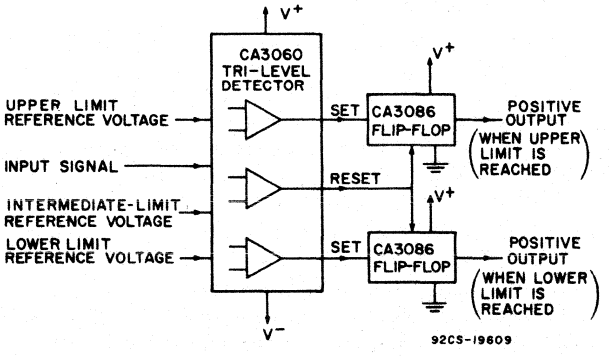


Fig.20—Functional block diagram of a tri-level comparator.

The circuit diagram of a tri-level comparator appears in Fig. 21. Power is provided for the CA3060 via terminals 3 and 8 by ±6-volt supplies and the built-in regulator provides amplifier-bias-current (I_{ABC}) to the three amplifiers via terminal 1. Lower-limit and upper-limit reference voltages are selected by appropriate adjustment of potentiometers R1 and R2, respectively. When resistors R3 and R4 are equal in value (as shown), the intermediate-limit reference voltage is automatically established at a value midway between the lower-limit and upper-limit values. Appropriate variation of resistors R3 and R4 permits selection of other values of intermediate-limit voltages. Input signal (E_S) is applied to the three comparators via terminals 5, 12, and 14. The "SET" output lines trigger the appropriate flip-flop whenever the input signal reaches a limit value. When the input signal returns to an intermediate-value, the common flip-flop "RESET" line is energized. The loads in the circuits, shown in Fig. 21 are 5-V, 25-mA lamps.

Active Filters — Using the CA3060 as a Gyrator

The high output impedance of the OTAs makes the CA3060 ideally suited for use as a gyrator in active filter applications. Fig. 22 shows two OTAs of the CA3060 connected as a gyrator in an active filter circuit. The OTAs in this circuit can make a 3-μF capacitor function as a floating 10-kilohenry inductor across Terminals A and B. The measured Q of 13 (at a frequency of 1 Hz) of this inductor compares favorably with a calculated Q of 16. The 20-kilohm to 2-megohm attenuators in this circuit extend the dynamic range of the OTA by a factor of 100. The 100-kilohm potentiometer, across V+ and V-, tunes the inductor by varying the g_{21} of the OTAs, thereby changing the gyration resistance.

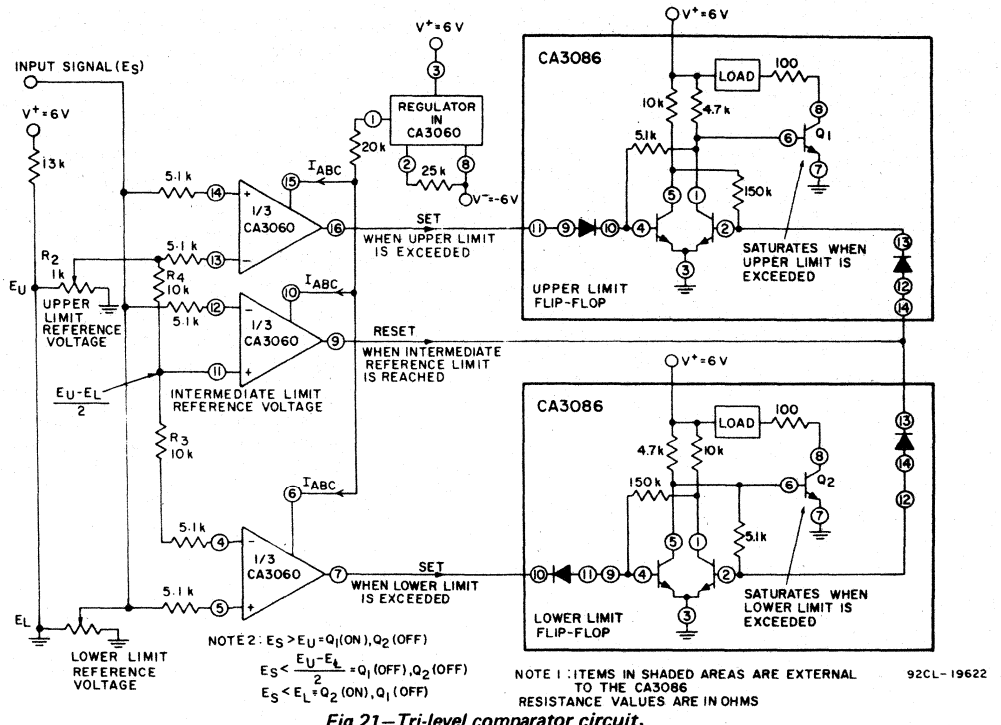


Fig.21—Tri-level comparator circuit.

CA3060, CA3060A Types

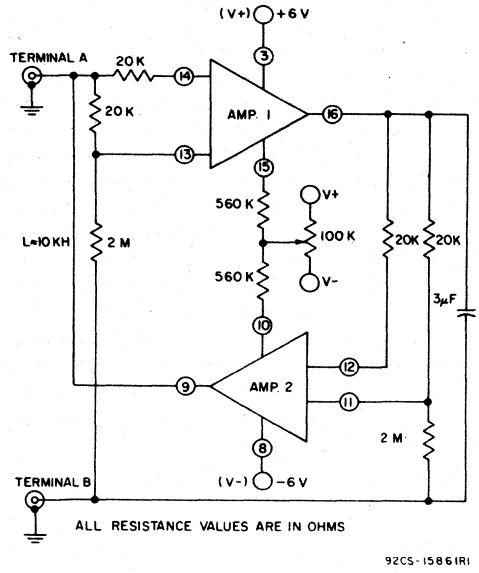


Fig.22—Two operational transconductance amplifiers of the CA3060 connected as a gyrator in an active filter circuit.

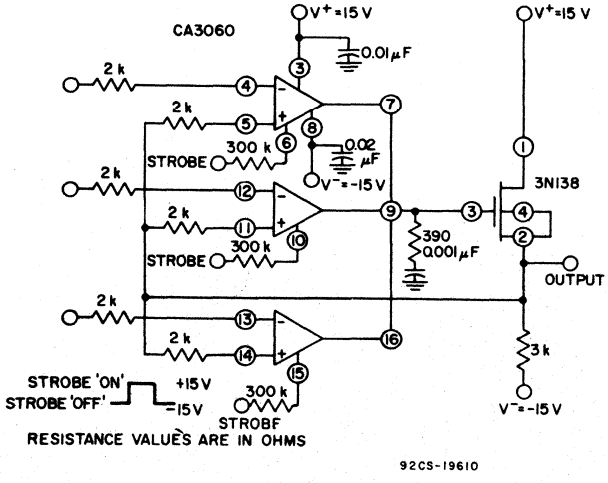


Fig.23—Three-channel multiplexer.

THREE CHANNEL MULTIPLEXER

Fig. 23 shows a schematic of a three channel multiplexer using a single CA3060 and a 3N138 MOS/FET as a buffer and power amplifier.

When the CA3060 is connected as a high-input impedance voltage follower, and strobe "ON," each amplifier is activated and the output swings to the level of the input of that amplifier. The cascade arrangement of each CA3060 amplifier with the MOS/FET provides an open loop voltage gain in excess of 100 dB, thus assuring excellent accuracy in the voltage follower mode with 100% feedback.

Operation at ±6 volts is also possible with several minor changes. First, the resistance in series with amplifier bias current (I_{ABC}) terminal of each amplifier should be decreased to maintain 100 μA of strobe—"ON" current at this lower supply voltage. Second, the drain resistance for the MOS/FET should be decreased to maintain the same value of source current. The low cost dual-gate protected MOS/FET, RCA-40841, may be used when operating at the low supply voltage.

The phase compensation network consists of a single 390Ω resistor and a 1000-pF capacitor, located at the interface of the CA3060 output and the MOS/FET gate. The bandwidth of the system is 1.5 MHz and the slew rate is 0.3 volts/μsec. The system slew rate is directly proportional to the value of the phase compensation capacitor. Thus, with higher gain settings where lower values of phase compensation capacitors are possible, the slew rate is proportionally increased.

NON LINEAR APPLICATIONS

AM Modulator (Two-Quadrant Multiplier)

Fig. 24 shows Amplifier No. 3 of the CA3060 used in an AM modulator or 2-quadrant multiplier circuit. When modulation is applied to the amplifier bias input, Terminal B, and the carrier frequency to the differential input, Terminal A, the waveform, shown in Fig. 24, is obtained. Fig. 24 is a result of adjusting the input offset control to balance the circuit so that no modulation can occur at the output without a carrier input. The linearity of the modulator is indicated by the solid trace of the superimposed modulating frequency. The maximum depth of modulation is determined by the ratio of the peak input modulating voltage to $V_{\bar{}}$.

The two-quadrant multiplier characteristic of this modulator is easily seen if modulation and carrier are reversed as shown in Fig. 24. The polarity of the output must follow that of the differential input; therefore, the output is positive only during, the positive half cycle of the modulation and negative only in the second half cycle. Note, that both the input and output signals are referenced to ground. The output signal is zero when either the differential input or I_{ABC} are zero.

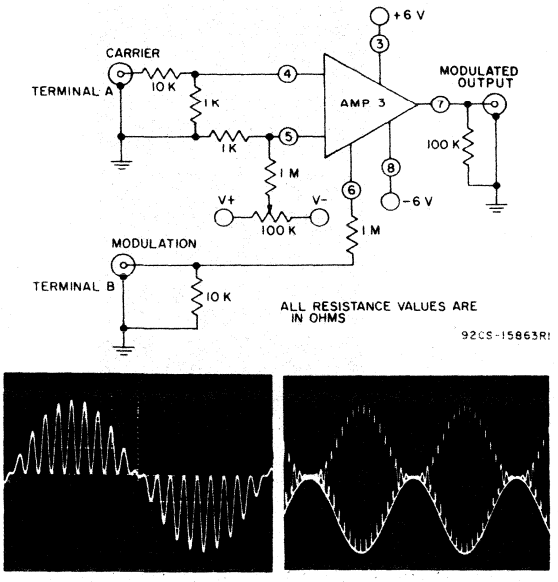


Fig.24—Two-quadrant multiplier circuit using the CA3060 with associated waveforms.

Four-Quadrant Multiplier

The CA3060 is also useful as a four-quadrant multiplier. A block diagram of such a multiplier, utilizing Amplifier Nos. 1, 2, and 3, is shown in Fig. 25 and a typical circuit is shown in Fig. 26. The multiplier consists of a single CA3060 and, as in the two-quadrant multiplier, exhibits no level shift between input and output. In Fig. 25, Amplifier No. 1 is connected as an inverting amplifier for the X-input signal. The output current of Amplifier No. 1 is calculated as follows:

$$I_O(1) = [-V_X]\ [g_{21}(1)] \qquad \text{(Eq.3)}$$

Ampl. No. 2 is a non-inverting amplifier so that

$$I_O(2) = [+V_X]\ [g_{21}(2)] \qquad \text{(Eq. 4)}$$

Because the amplifier output impedances are high, the load current is the sum of the two output currents, for an output voltage

$$V_O = V_X R_L\ [g_{21}(2) - g_{21}(1)] \qquad \text{(Eq. 5)}$$

The transconductance is approximately proportional to the amplifier bias current; therefore, by varying the bias current the g_{21} is also controlled. Amplifier No. 2 bias current is proportional to the Y-input signal and is expressed as

$$I_{ABC(2)} \approx \frac{(V\text{-}) + V_Y}{R_1} \qquad \text{(Eq. 6)}$$

Hence,

$$g_{21}(2) \approx k\ [\ (V\text{-}) + V_Y\ ]. \qquad \text{(Eq. 7)}$$

Bias for Amplifier No. 1 is derived from the output of Amplifier No. 3 which is connected as a unity-gain inverting amplifier. $I_{ABC(1)}$, therefore, varies inversely with V_Y. And by the same reasoning as above

$$g_{21}(1) \approx k\ [(V\text{-}) - V_Y]. \qquad \text{(Eq. 8)}$$

Combining equation 5, 7, and 8 yields:

$$V_O \approx V_X \cdot k \cdot R_L \left|[(V\text{-}) + V_Y] - [(V\text{-}) - V_Y]\right| \quad \text{or}$$

$$V_O \approx 2\,k\,R_L\,V_X\,V_Y$$

Fig. 26 shows the actual circuit including all the adjustments associated with differential input and an adjustment for equalizing the gains of Amplifiers No. 1 and No. 2. Adjustment of the circuit is quite simple. With both the X and Y voltages at zero, connect Terminal 10 to Terminal 8. This procedure disables Amplifier No. 2 and permits adjusting the offset voltage of Amplifier No. 1 to zero by means of the 100-kΩ potentiometer. Next, remove the short between Terminals 10 and 8 and connect Terminal 15 to Terminal 8. This step disables Amplifier No. 1 and permits Amplifier No. 2 to be zeroed with the other potentiometer. With AC signals on both the X and Y input, R3 and R11 are adjusted for symmetrical output signals. Fig. 27 shows the output waveform with the multiplier adjusted. The voltage waveform in Fig. 27a shows suppressed carrier modulation of 1-kHz carrier with a triangular wave.

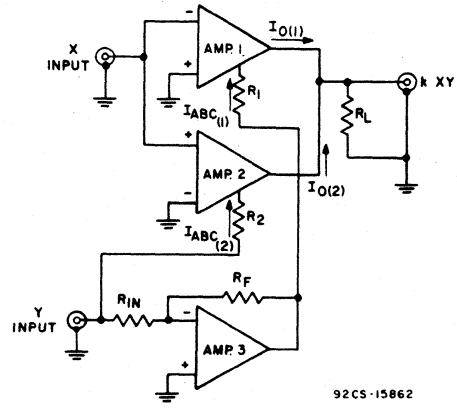


Fig.25—Four-quadrant multiplier using the CA3060.

Figures 27b and 27c, respectively, show the squaring of a triangular wave and a sine wave. Notice that in both cases the outputs are always positive and return to zero after each cycle.

CA3060, CA3060A Types

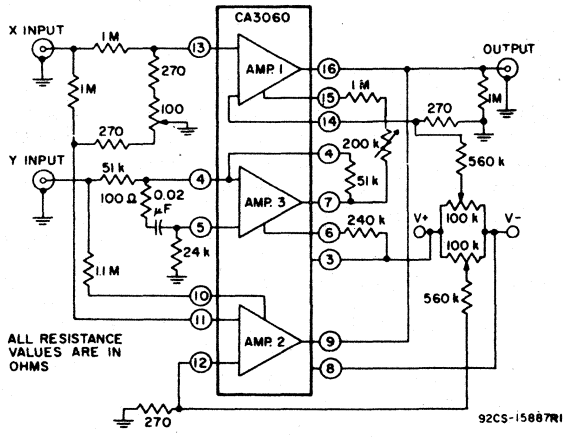


Fig.26—Typical four-quadrant multiplier circuit.

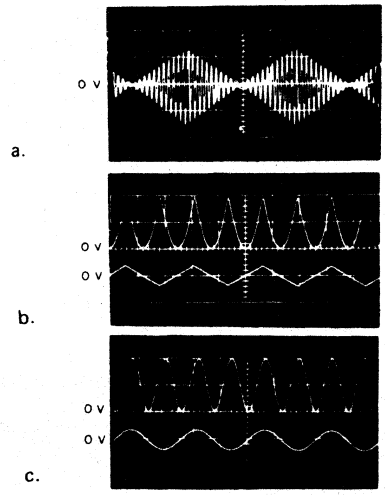
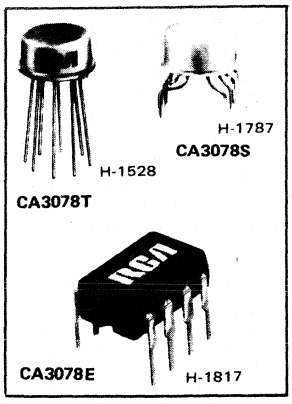


Fig.27—Voltage waveforms of four-quadrant multiplier circuit.



Micropower Operational Amplifier

Features:

- Low standby power: as low as 700 nW
- Wide supply voltage range: ±0.75 to ±15 V
- High peak output current: 6.5 mA min.
- Adjustable quiescent current
- Output short-circuit protection

Applications:

- Portable electronics
- Medical electronics
- Instrumentation
- Telemetry
- Intrusion alarms

The RCA-CA3078 and CA3078A are high-gain monolithic operational amplifiers which can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The CA3078 and CA3078A provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5-volt battery is a practical reality with these devices.

The CA3078A is a preminum device having a supply voltage range of $V^{\pm}$ = 0.75 to $V^{\pm}$ = 15 V and an operating temperature range of −25°C to +125°C. The CA3078 has the same lower supply voltage limit but the upper limit is V^{+} = +6 V and V^{-} = −6 V. The operating temperature range is from 0°C to +70°C.

The CA3078 and CA3078A are supplied in the standard 8-lead TO-5 package ("T" suffix), the 8-lead dual-in-line formed-lead "DIL-CAN" package ("S" suffix), or the 8-lead dual-in-line plastic "MINI-DIP" package ("E" suffix).

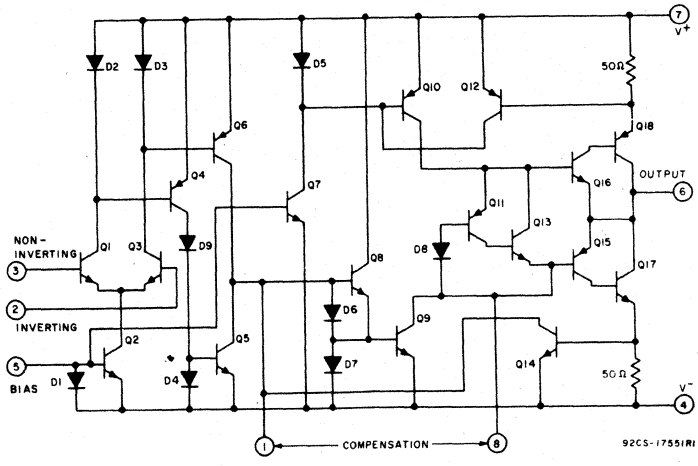


Fig. 1 – Schematic diagram of the CA3078 and CA3078A.

CA3078, CA3078A Types

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25°C$*

	CA3078A	CA3078
DC Supply Voltage (between V^+ and V^- terminal	36 V	14 V
Differential Input Voltage	±6 V	±6 V
DC Input Voltage	V^+ to V^-	V^+ to V^-
Input Signal Current	0.1 mA	0.1 mA
Output Short-Circuit Duration*	No Limitation	No Limitation
Device Dissipation	150 mW (up to 125°C)	500 mW (up to 70°C)
Temperature Range:		
Operating	−55 to +125°C	0 to +70°C
Storage	−65 to +150°C	−65 to +150°C
Lead Temperature (During Soldering):		
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10s max.	+300°C	+300°C

* Short circuit may be applied to ground or to either supply.

ELECTRICAL CHARACTERISTICS For Equipment Design

CHARACTERISTICS SYMBOLS	TEST CONDITIONS			CA3078A LIMITS					CA3078 LIMITS					UNITS
				R_{SET} = 5.1 MΩ, I_Q = 20 μA					R_{SET} = 1 MΩ, I_Q = 100 μA					
				T_A = 25°C			T_A = −55 to 125°C		T_A = 25°C			T_A = 0 to 70°C		
	V^+ & V^- V	R_S kΩ	R_L kΩ	MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
V_{IO}	6	≤10	–	–	0.70	3.5	–	4.5	–	1.3	4.5	–	5	mV
V_{IO}		–	–	–	0.50	2.5	–	5.0	–	6	32	–	40	nA
I_{IB}		–	–	–	7	12	–	50	–	60	170	–	200	nA
A_{OL}		–	≥10	92	100	–	90	–	88	92	–	86	–	dB
I_Q		–	–	–	20	25	–	45	–	100	130	–	150	μA
P_D		–	–	–	240	300	–	540	–	1200	1560	–	1800	μW
V_{OM}		–	≥10	±5.1	±5.3	–	±5	–	±5.1	±5.3	–	±5	–	V
V_{ICR}		≤10	–	–	−5.5 to +5.8	–	−5 to +5	–	–	−5.5 to +5.8	–	−5 to +5	–	V
CMRR		≤10	–	80	115	–	–	–	80	110	–	–	–	dB
I_{OM}^+ or I_{OM}^-		–	–	–	12	–	6.5	30	–	12	–	6.5	30	mA
$\Delta V_{IO}/\Delta V^+$		≤10		76	105	–	–	–	76	93	–	–	–	μV/V
$\Delta V_{IO}/\Delta V^-$			–	76	105	–	–	–	76	93	–	–	–	
				R_{SET} = 13 MΩ, I_Q = 20 μA										
V_{IO}	15	≤10	–	–	1.4	3.5	–	4.5	–	–	–	–	–	mV
A_{OL}		–	≥10	92	100	–	88	–	–	–	–	–	–	dB
I_Q		–	–	–	20	30	–	50	–	–	–	–	–	μA
P_D		–	–	–	600	750	–	1350	–	–	–	–	–	μW
V_{OM}		–	≥10	±13.7	±14.1	–	±13.5	–	–	–	–	–	–	V
CMRR		≤10	–	80	106	–	–	–	–	–	–	–	–	dB
I_{IB}		–	–	–	7	14	–	55	–	–	–	–	–	nA
I_{IO}		–	–	–	0.50	2.7	–	5.5	–	–	–	–	–	nA

ELECTRICAL CHARACTERISTICS, *at $T_A = 25°C$*

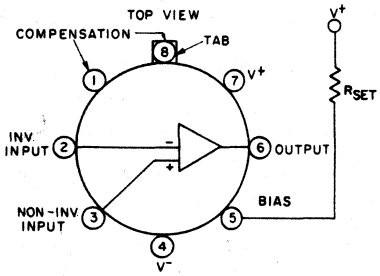
Typical Values Intended Only for Design Guidance

CHARACTERISTICS SYMBOLS	TYPICAL VALUES				UNITS
	CA3078A		CA3078		
	$V^+ = +1.3$ V, $V^- = -1.3$ V $R_{SET} = 2$ MΩ $I_Q = 10$ μA	$V^+ = +0.75$ V, $V^- = -0.75$ V $R_{SET} = 10$ MΩ $I_Q = 1$ μA	$V^+ = +1.3$ V, $V^- = -1.3$ V $R_{SET} = 2$ MΩ $I_Q = 10$ μA	$V^+ = +0.75$ V, $V^- = -0.75$ V $R_{SET} = 10$ MΩ $I_Q = 1$ μA	
V_{IO}	0.7	0.9	1.3	1.5	mV
I_{IO}	0.3	0.054	1.7	0.5	nA
I_{IB}	3.7	0.45	9	1.3	nA
A_{OL}	84	65	80	60	dB
I_Q	10	1	10	1	μA
P_D	26	1.5	26	1.5	μW
V_{OPP}	1.4	0.3	1.4	0.3	V
V_{ICR}	−0.8 to +1.1	−0.2 to +0.5	−0.8 to +1.1	−0.2 to +0.5	V
CMRR	100	90	100	90	dB
$I_{OM}^{\pm}$	12	0.5	12	0.5	mA
$\Delta V_{IO}/\Delta V^{\pm}$	20	50	20	50	μV/V

Typical Values Intended Only for Design Guidance *at $T_A = 25°C$ and $V^+ = +6$ V, $V^- = -6$ V*

CHARACTERISTICS SYMBOLS	TEST CONDITIONS	CA3078A		CA3078	UNITS
		$R_{SET} = 5.1$ MΩ $I_Q = 20$ μA	$R_{SET} = 1$ MΩ $I_Q = 100$ μA	$R_{SET} = 1$ MΩ $I_Q = 100$ μA	
$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10$ kΩ	5	6	6	μV/°C
$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10$ kΩ	6.3	70	70	pA/°C
BW_{OL}	3dB pt.	0.3	2	2	kHz
SR	See Figs. 20, 21	0.027	0.04	0.04	V/μs
		0.5	1.5	1.5	
–	10% to 90% Rise Time	3	2.5	2.5	μs
R_I		7.4	1.7	0.87	MΩ
R_O		1	0.8	0.8	kΩ
e_N (10 Hz)	$R_S = 0$	40	–	25	nV/$\sqrt{Hz}$
i_N (10 Hz)	$R_S = 1$ MΩ	0.25	–	1	pA/$\sqrt{Hz}$

CA3078, CA3078A Types



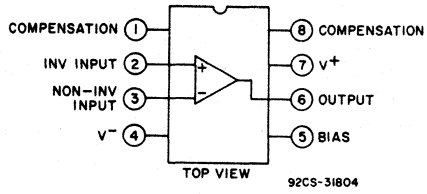


Fig. 2 – Functional diagrams.

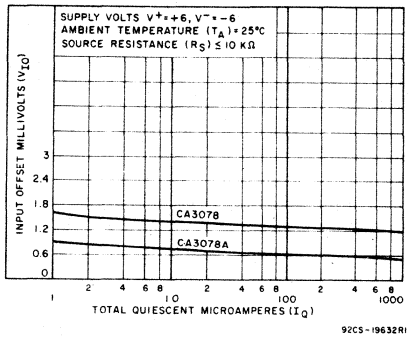


Fig. 3 – Input offset voltage vs. total quiescent current.

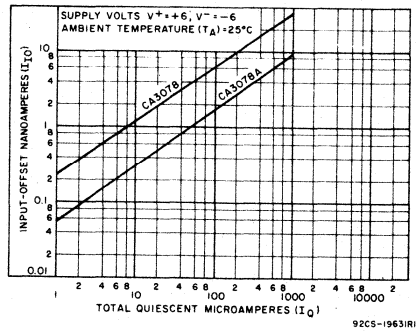


Fig. 4 – Input offset current vs. total quiescent current.

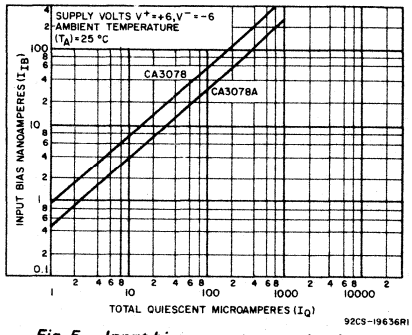


Fig. 5 – Input bias current vs. total quiescent current.

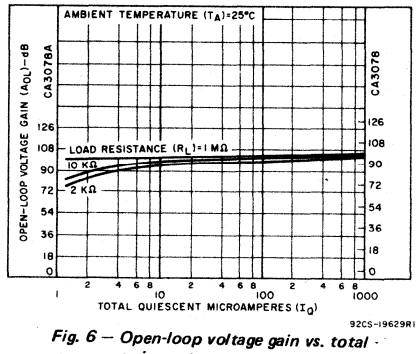


Fig. 6 – Open-loop voltage gain vs. total quiescent current.

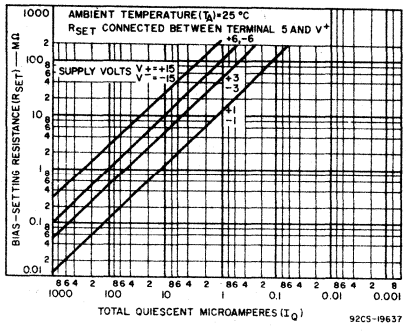


Fig. 7 – Bias-setting resistance vs. total quiescent current.

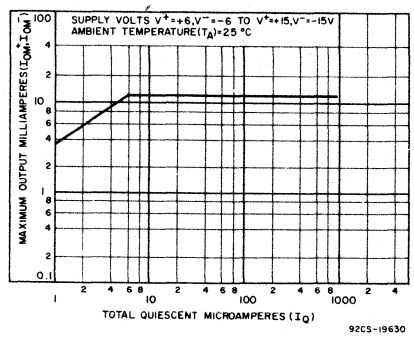


Fig. 8 – Maximum output current vs. total quiescent current.

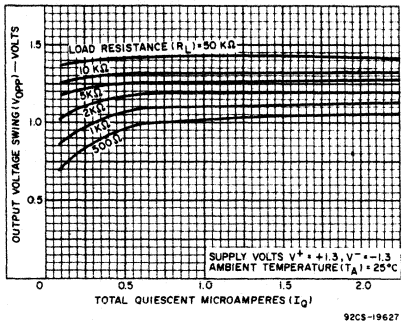


Fig. 9 — Output voltage swing vs. total quiescent current.

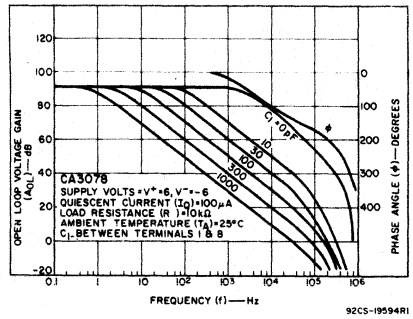


Fig. 10 — Open-loop voltage gain vs. frequency for I_Q = 100 μA — CA3078.

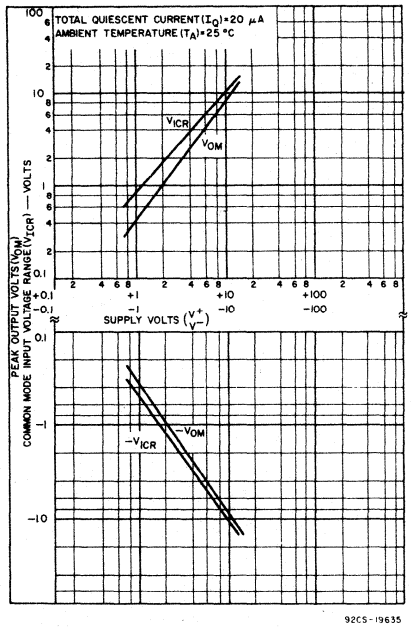


Fig. 11 — Output and common-mode voltage vs. supply voltage.

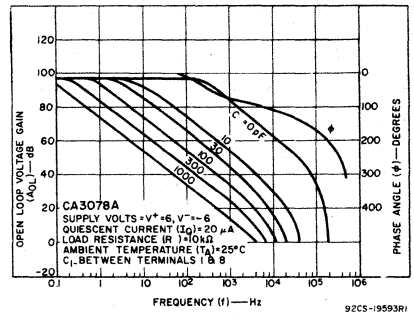


Fig. 12 — Open-loop voltage gain vs. frequency for I_Q = 20 μA — CA3078.

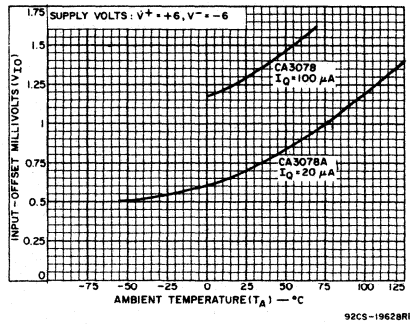


Fig. 13 — Input offset voltage vs. temperature.

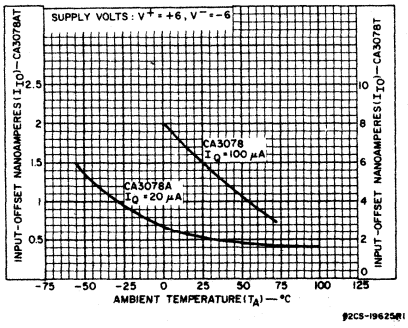


Fig. 14 — Input offset current vs. temperature.

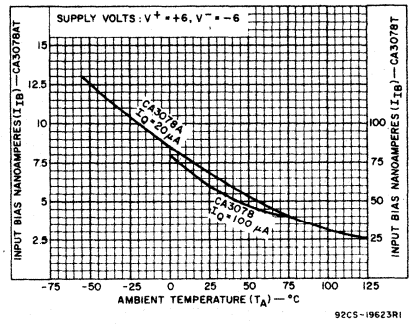


Fig. 15 — Input bias current vs. temperature.

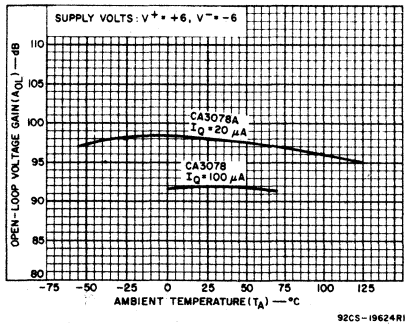


Fig. 16 – Open-loop voltage gain vs. temperature.

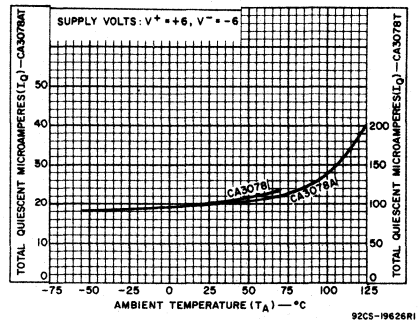


Fig. 17 – Total quiescent current vs. temperature.

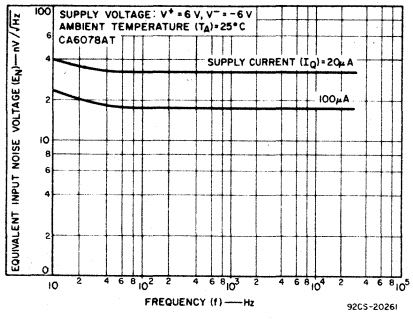


Fig. 18 – Quivalent input noise voltage vs. frequency.

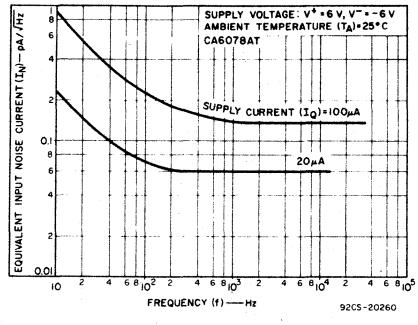


Fig. 19 – Equivalent input noise current vs. frequency.

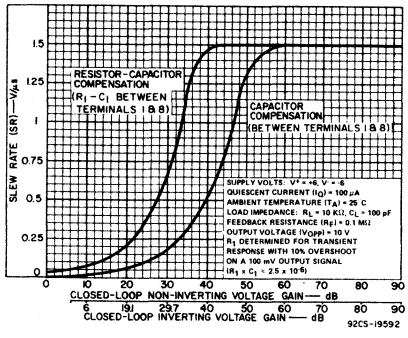


Fig. 20 – Slew rate vs. closed-loop gain for I_Q = 100 μA – CA3078.

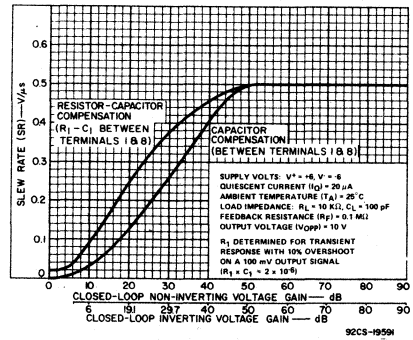


Fig. 21 – Slew rate vs. closed-loop gain for I_Q = 20 μA – CA3078.

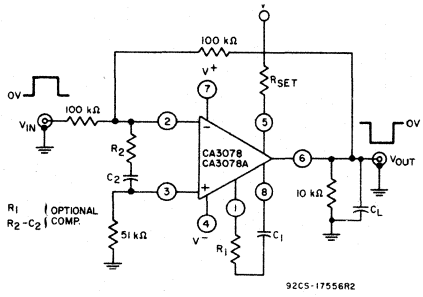


Fig. 22 – Transient response and slew-rate, unity gain (inverting) test circuit.

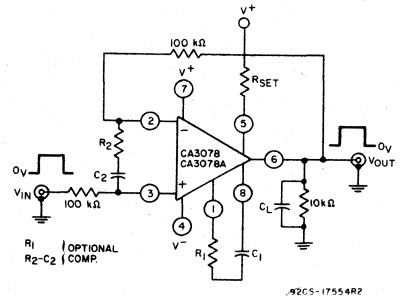


Fig. 23 – Slew-rate, unity gain (non-inverting) test circuit.

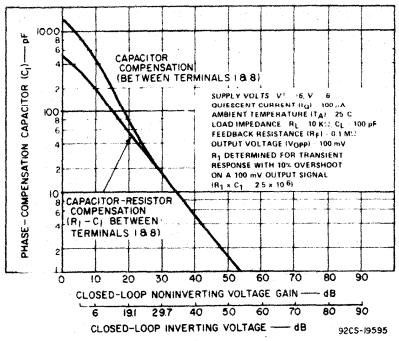


Fig. 24 – Phase compensation capacitance vs. closed-loop gain – CA3078.

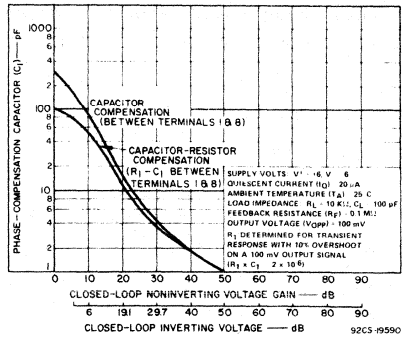


Fig. 25 – Phase compensation capacitance vs. closed-loop gain – CA3078A.

Table I – Unity-gain slew rate vs. compensation – CA3078 and CA3078A

SUPPLY VOLTS: $V^+ = 6$, $V^- = -6$	**TRANSIENT RESPONSE: 10% OVERSHOOT FOR AN OUTPUT VOLTAGE OF 100 mV**
OUTPUT VOLTAGE (V_O) = ±5 V	**AMBIENT TEMPERATURE (T_A) = 25°C**
LOAD RESISTANCE (R_L) = 10 kΩ	

COMPENSATION TECHNIQUE	UNITY GAIN (INVERTING) Fig. 22					UNITY GAIN (NON-INVERTING) Fig. 23				
	R1	C1	R2	C2	SLEW RATE	R1	C1	R2	C2	SLEW RATE
CA3078 – I_Q = 100 μA	kΩ	pF	kΩ	μF	V/μs	kΩ	pF	kΩ	μF	V/μs
Single Capacitor	0	750	∞	0	0.0085	0	1500	∞	0	0.0095
Resistor & Capacitor	3.5	350	∞	0	0.04	5.3	500	∞	0	0.024
Input	∞	0	0.25	0.306	0.67	∞	0	0.311	0.45	0.67
CA3078A – I_Q = 20 μA										
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor & Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	0.4

OPERATING CONSIDERATIONS

Compensation Techniques

The CA3078A and CA3078 can be phase-compensated with one or two external components depending upon the closed-loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from terminal 1 to terminal 8. Values of the resistor and capacitor required for compensation as a function of closed loop gain are shown in Figs. 24 and 25. These curves represent the compensation necessary at quiescent currents of 100 μA and 20 μA, respectively, for a transient response with 10% overshoot. Figs. 20 and 21 show the slew rates that can be obtained with the two different compensation techniques. Higher speeds can be achieved with input compensation, but this increases noise output. Compensation can also be accomplished with a single capacitor connected from terminal 1 to terminal 8, with speed being sacrificed for simplicity. Table I gives an indication of slew rates that can be obtained with various compensation techques at quiescent currents of 100 μA and 20 μA.

Single Supply Operation

The CA3078A and CA3078 can operate from a single supply with a minimum total supply voltage of 1.5 volts. Figs. 27 and 28 show the CA3078A or CA3078 in inverting the non-inverting 20-dB amplifier configurations utilizing a 1.5-volt type "AA" cell for a supply. The total power consumption for

either circuit is approximately 675 nanowatts. The output voltage swing in this configuration is 300 mV p-p with a 20 kΩ load.

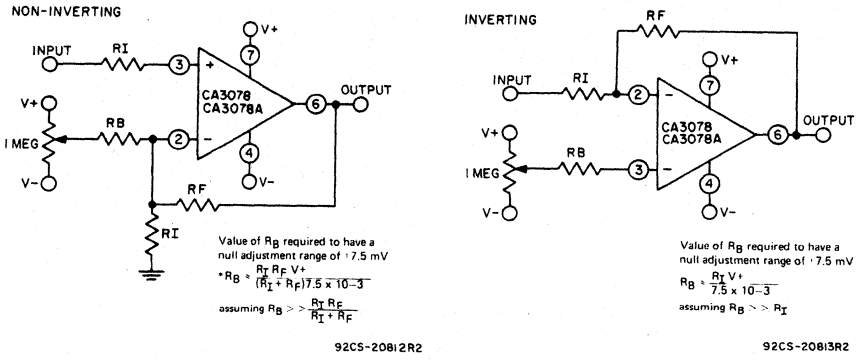


Fig. 26 – Offset voltage null circuits.

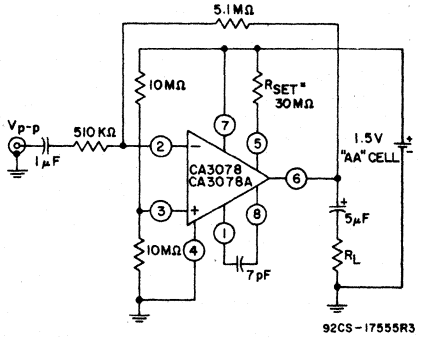


Fig. 27 – Inverting 20-dB amplifier circuit.

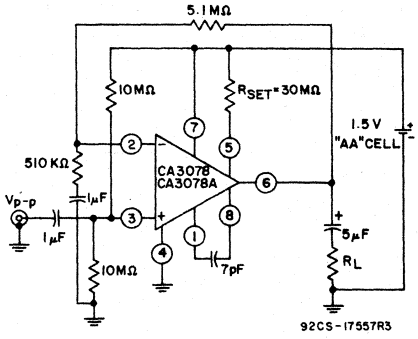
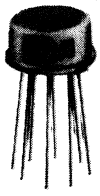
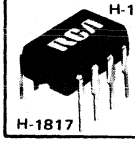


Fig. 28 – Non inverting 20-dB amplifier circuit.

CA3080S
CA3080AS
8-LEAD TO-5
with Dual-In-Line
Formed Leads
"DIL-CAN"
H-1787



CA3080
CA3080A
8-LEAD TO-5
H-1528



H-1817

CA3080E
CA3080AE
8-LEAD Dual-
In-Line Plastic
Package
"MINI-DIP"

Operational Transconductance Amplifiers (OTA's)

Gatable-Gain Blocks

Features:

- Slew rate (unity gain, compensated): 50 V/μs
- Adjustable power consumption: 10μW to 30 mW
- Flexible supply voltage range: ± 2 V to ± 15 V
- Fully adjustable gain: 0 to $g_m R_L$ limit
- Tight g_m spread: CA3080 (2:1), CA3080A (1.6:1)
- Extended g_m linearity: 3 decades

The RCA-CA3080 and CA3080A types are Gatable-Gain Blocks which utilize the unique operational-transconductance-amplifier (OTA) concept described in Application Note ICAN-6668, "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

The CA3080 and CA3080A types have differential input and a single-ended, push-pull, class A output. In addition, these types have an amplifier bias input which may be used either for gating or for linear gain control. These types also have a high output impedance and their transconductance (g_m) is directly proportional to the amplifier bias current (I_{ABC}).

The CA3080 and CA3080A types are notable for their excellent slew rate (50 V/μs), which makes them especially useful for multiplex and fast unity-gain voltage followers. These types are especially applicable for multiplex applications because power is consumed only when the devices are in the "ON" channel state.

The CA3080A is rated for operation over the full military-temperature range (−55 to +125°C) and its characteristics are specifically controlled for applications such as sample-hold, gain-control, multiplex, etc. Operational transconductance amplifiers are also useful in programmable power-switch applications, e.g., as described in Application Note ICAN-6048, "Some Applications of a Programmable Power Switch/Amplifier" (CA3094, CA3094A, CA3094B).

These types are supplied in the 8-lead TO-5-style package (CA3080, CA3080A), and in the 8-lead TO-5-style package with dual-in-line formed leads ("DIL-CAN", CA3080S, CA3080AS). The CA3080 is also supplied in the 8-lead dual-in-line plastic ("MINI-DIP") package (CA3080E, CA3080AE), and in chip form (CA3080H).

Applications:

- **Sample and hold**
- **Multiplex**
- **Voltage follower**
- **Multiplier**
- **Comparator**

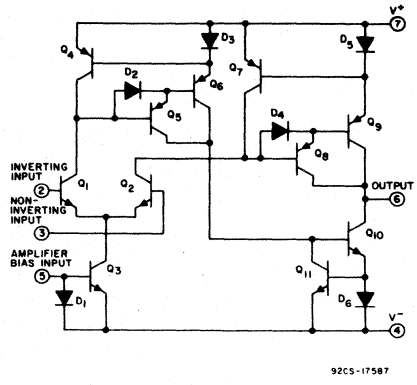


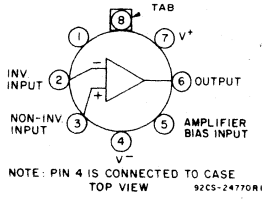
Fig.1 – Schematic diagram for CA3080 and CA3080A.

CA3080, CA3080A Types

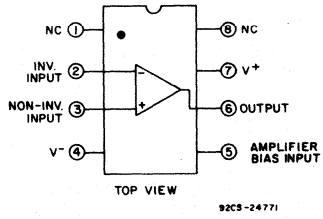
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (Between V^+ and V^- terminals)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE	V^+ to V^-
INPUT SIGNAL CURRENT	1 mA
AMPLIFIER BIAS CURRENT	2 mA
OUTPUT SHORT-CIRCUIT DURATION*	Indefinite
DEVICE DISSIPATION	125 mW
TEMPERATURE RANGE:	
Operating	
CA3080, CA3080E, CA3080S	0 to + 70 °C
CA3080A, CA3080AE, CA3080AS	−55 to + 125 °C
Storage	−65 to + 150 °C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 265 °C

* Short circuit may be applied to ground or to either supply.



TO-5 Style Package



Plastic Package (E Suffix)

Fig.2 – Functional diagrams.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS FOR THE CA3080 AND CA3080A

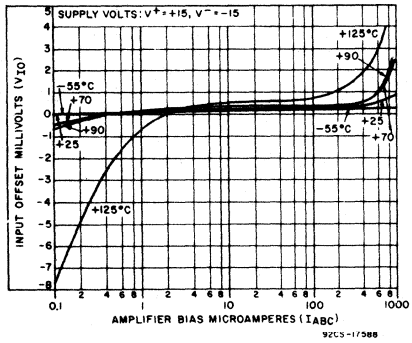


Fig.3 – Input offset voltage as a function of amplifier bias current.

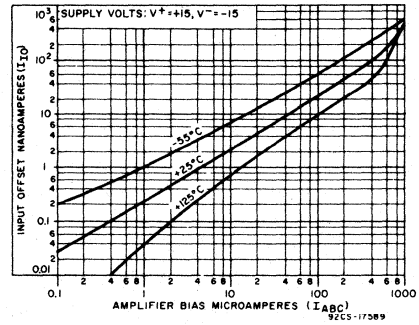


Fig.4 – Input offset current as a function of amplifier bias current.

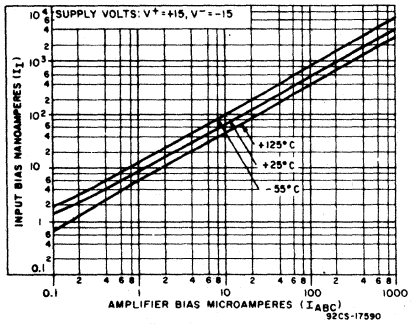


Fig.5 – Input bias current as a function of amplifier bias current.

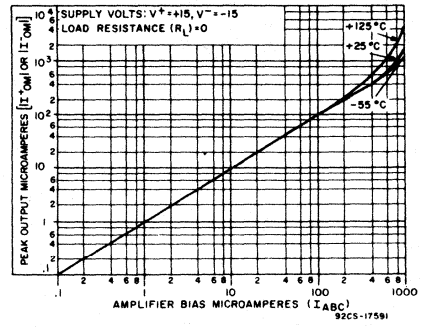


Fig.6 – Peak output current as a function of amplifier bias current.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS: $V^+ = 15$ V, $V^- = -15$ V, $I_{ABC} = 500\ \mu A$, $T_A = 25^oC$ (unless indicated otherwise)	CA3080, CA3080E, CA3080S LIMITS			UNITS
			Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}		–	0.4	5	mV
		$T_A = 0$ to 70^oC	–	–	6	
Input Offset Current	I_{IO}		–	0.12	0.6	μA
Input Bias Current	I_I		–	2	5	μA
		$T_A = 0$ to 70^oC	–	–	7	
Forward Transconductance (large signal)	g_m		6700	9600	13000	μmho
		$T_A = 0$ to 70^oC	5400	–	–	
Peak Output Current	$\lvert I_{OM} \rvert$	$R_L = 0$	350	500	650	μA
		$R_L = 0$, $T_A = 0$ to 70^oC	300	–	–	
Peak Output Voltage:						
Positive	V^+_{OM}	$R_L = \infty$	12	13.5	–	V
Negative	V^-_{OM}		−12	−14.4	–	
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity:						
Positive	$\Delta V_{IO}/\Delta V^+$		–	–	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	–	150	
Common-Mode Rejection Ratio	CMRR		80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}		12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I		10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

			CA3080, CA3080E, CA3080S	
Input Offset Voltage	V_{IO}	$I_{ABC} = 5\ \mu A$	0.3	mV
Input Offset Voltage Change	$\lvert \Delta V_{IO} \rvert$	$I_{ABC} = 500\ \mu A$ to $I_{ABC} = 5\ \mu A$	0.2	mV
Peak Output Current	I_{OM}	$I_{ABC} = 5\ \mu A$	5	μA
Peak Output Voltage:				
Positive	V^+_{OM}	$I_{ABC} = 5\ \mu A$	13.8	V
Negative	V^-_{OM}		−14.5	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	0.08	nA
		$I_{ABC} = 0$, $V_{TP} = 36$ V	0.3	
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4$ V	0.008	nA
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate:				
Maximum (uncompensated)	SR		75	V/μs
Unity Gain (compensated)			50	
Open-Loop Bandwidth	BW_{OL}		2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	f = 1 MHz	0.024	pF
Propagation Delay	t_{PHL}, t_{PLH}	$I_{ABC} = 500\ \mu A$	45	ns

CA3080, CA3080A Types

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS: $V^+ = 15$ V, $V^- = -15$ V, $I_{ABC} = 500\ \mu A$, $T_A = 25^oC$ (unless indicated otherwise)	CA3080A, CA3080AE, CA3080AS LIMITS Min.	Typ.	Max.	UNITS
Input Offset Voltage	V_{IO}	$I_{ABC} = 5\ \mu A$	–	0.3	2	mV
			–	0.4	2	
		$T_A = -55$ to $+125^oC$	–	–	5	
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	$I_{ABC} = 500\ \mu A$ to $I_{ABC} = 5\ \mu A$	–	0.1	3	mV
Input Offset Current	I_{IO}		–	0.12	0.6	μA
Input Bias Current	I_I		–	2	5	μA
		$T_A = -55$ to $+125^oC$	–	–	8	
Forward Transconductance (large signal)	g_m		7700	9600	12000	μmho
		$T_A = -55$ to $+125^oC$	4000	–	–	
Peak Output Current	$\lvert I_{OM}\rvert$	$I_{ABC} = 5\ \mu A$, $R_L = 0$	3	5	7	μA
		$R_L = 0$	350	500	650	
		$R_L = 0$, $T_A = -55$ to $+125^oC$	300	–	–	
Peak Output Voltage:						V
Positive	V^+_{OM}	$I_{ABC} = 5\ \mu A$	12	13.8	–	
Negative	V^-_{OM}	$R_L = \infty$	−12	−14.5	–	
Positive	V^+_{OM}	$R_L = \infty$	12	13.5	–	
Negative	V^-_{OM}		−12	−14.4	–	
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity:						$\mu V/V$
Positive	$\lvert\Delta V_{IO}/\Delta V^+\rvert$		–	–	150	
Negative	$\lvert\Delta V_{IO}/\Delta V^-\rvert$		–	–	150	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	–	0.08	5	nA
		$I_{ABC} = 0$, $V_{TP} = 36$ V	–	0.3	5	
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4$ V	–	0.008	5	nA
Common-Mode Rejection Ratio	CMRR		80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}		12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I		10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

			CA3080A, CA3080AE, CA3080AS	
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate:				V/μs
Maximum (uncompensated)	SR		75	
Unity Gain (compensated)			50	
Open-Loop Bandwidth	BW_{OL}	–	2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		.15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	f = 1 MHz	0.024	pF
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	$I_{ABC} = 100\ \mu A$, $T_A = -55$ to $+125^oC$	3	$\mu V/^oC$
Propagation Delay	t_{PHL}, t_{PLH}	$I_{ABC} = 500\ \mu A$	45	ns

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

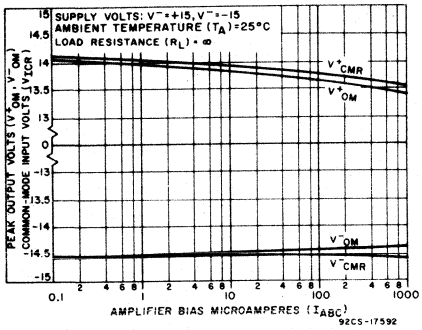


Fig.7 – Peak output voltage as a function of amplifier bias current.

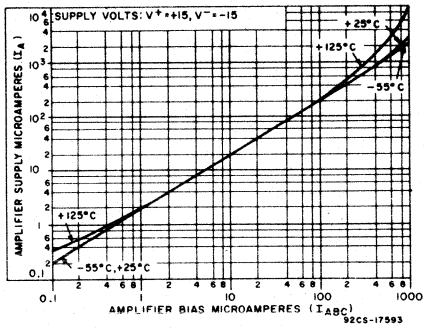


Fig.8 – Amplifier supply current as a function of amplifier bias current.

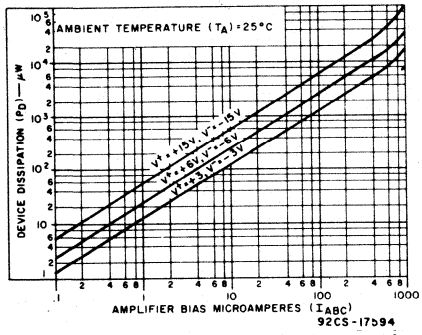


Fig.9 – Total power dissipation as a function of amplifier bias current.

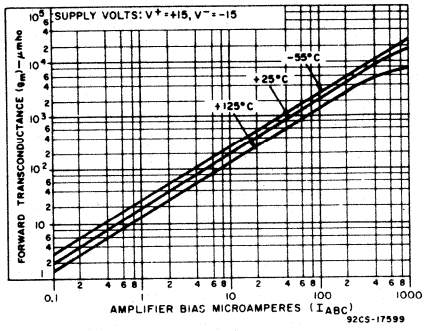


Fig.10 – Transconductance as a function of amplifier bias current.

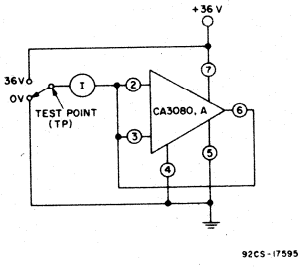


Fig.11 – Leakage current test circuit.

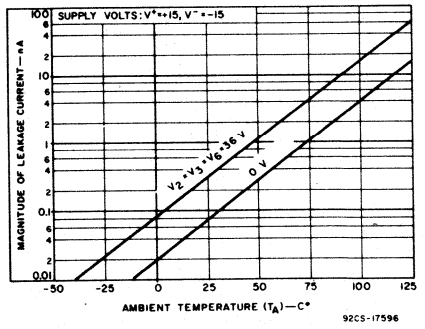


Fig.12 – Leakage current as a function of temperature.

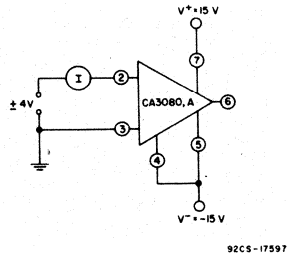


Fig.13 – Differential input current test circuit.

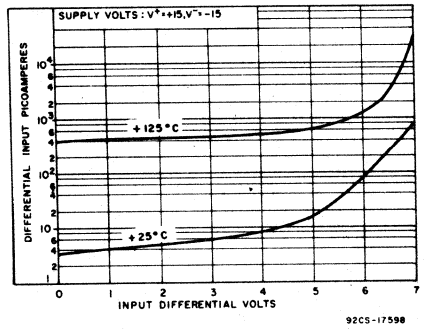


Fig.14 – Input current as a function of input differential voltage.

CA3080, CA3080A Types

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

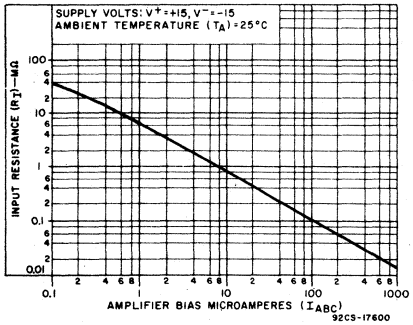


Fig. 15 – Input resistance as a function of amplifier bias current.

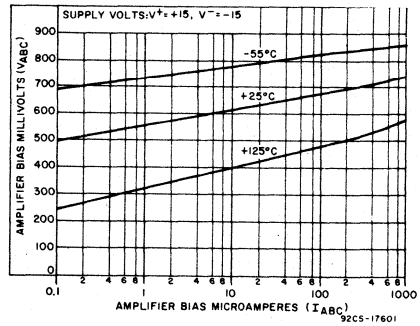


Fig. 16 – Amplifier bias voltage as a function of amplifier bias current.

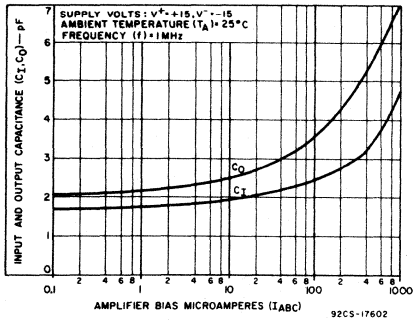


Fig. 17 – Input and output capacitance as a function of amplifier bias current.

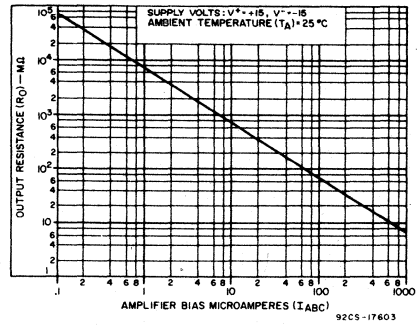


Fig. 18 – Output resistance as a function of amplifier bias current.

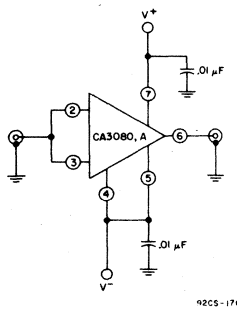


Fig. 19 – Input-to-output capacitance test circuit.

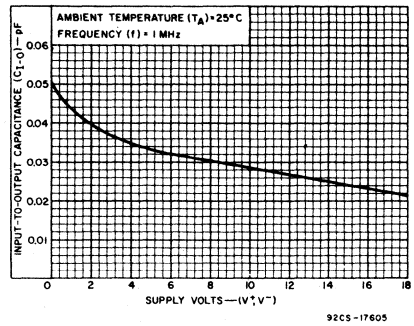
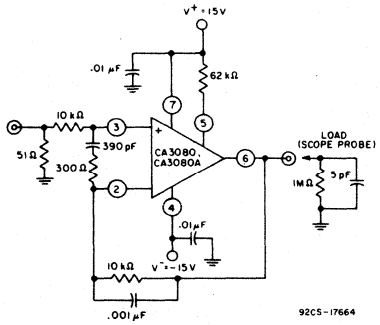


Fig. 20 – Input-to-output capacitance as a function of supply voltage.

APPLICATIONS



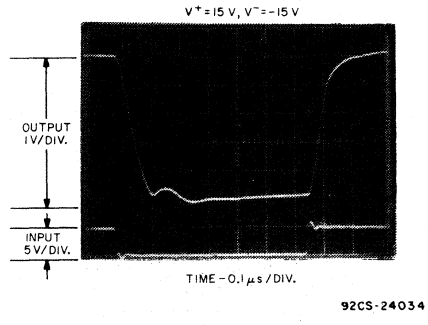


Fig. 21 – Schematic diagram of the CA3080 and CA3080A in a unity-gain voltage follower configuration and associated waveform.

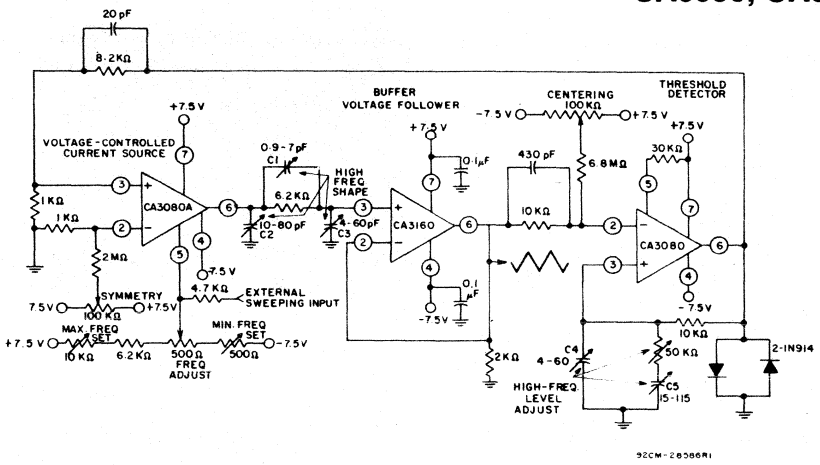
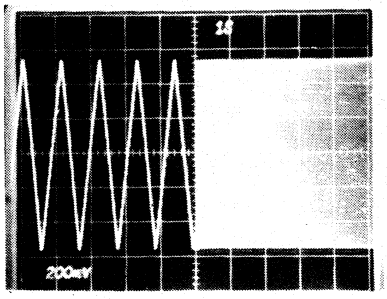
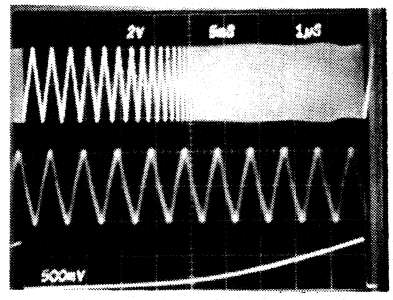


Fig.22 – 1,000,000/1 single-control function generator – 1 MHz to 1 Hz.



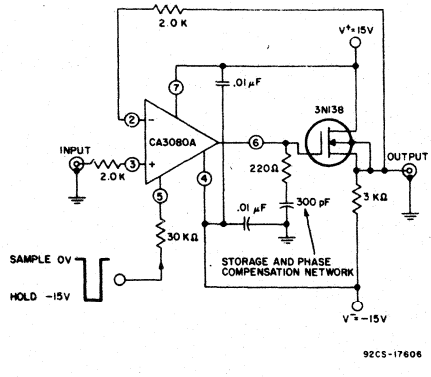
(a) – Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.



92CS-28588

(b) – Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

Fig.23 – Function generator dynamic characteristics waveforms.



SLEW RATE(IN SAMPLE MODE)=1.3 V/μs
ACQUISITION TIME*=3μs

* TIME REQUIRED FOR OUTPUT TO SETTLE WITHIN ±3mV OF A 4-VOLT STEP

Fig.24 – Schematic diagram of the CA3080A in a sample-hold configuration.

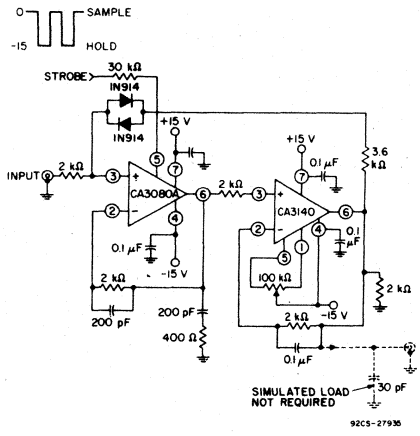
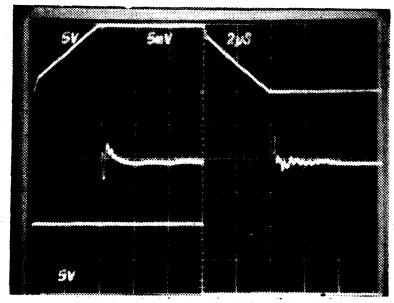


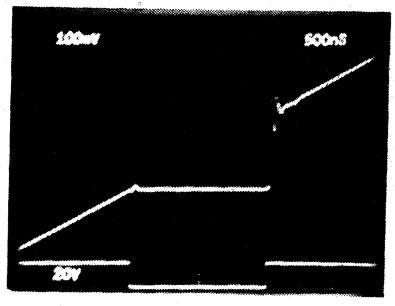
Fig.25 – Sample- and hold circuit.



LARGE-SIGNAL RESPONSE AND SETTLING TIME
TOP TRACE: OUTPUT SIGNAL (5 V/DIV. AND 2 μs/DIV.)
BOTTOM TRACE: INPUT SIGNAL (5 V/DIV. AND 2 μs/DIV.)
CENTER TRACE: DIFFERENCE OF INPUT AND OUTPUT SIGNALS THROUGH TEKTRONIX AMPLIFIER 7A13 (5 mV/DIV. AND 2 μs/DIV.)

92CS-27684

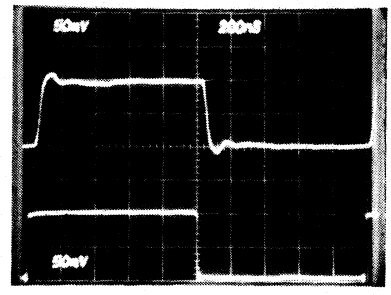
Fig.26 – Large-signal response and settling time for circuit shown in Fig.25.



SAMPLING RESPONSE
TOP TRACE: SYSTEM OUTPUT (100 mV/DIV. AND 500 ns/DIV.)
BOTTOM TRACE: SAMPLING SIGNAL (20 V/DIV. AND 500 ns/DIV.)

92CS-27885

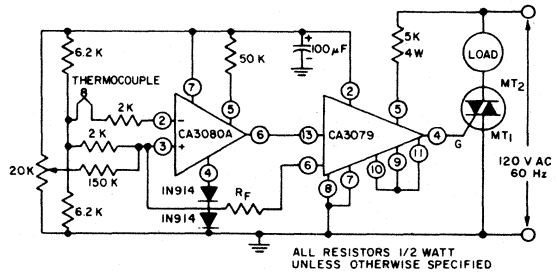
Fig.27 – Sampling response for circuit shown in Fig. 25.



TOP TRACE: OUTPUT (50 mV/DIV. AND 200 ns/DIV.)
BOTTOM TRACE: INPUT (50 mV/DIV. AND 200 ns/DIV.)

92CS-27883

Fig.28 – Input and output response for circuit shown in Fig. 25.



92CS-22619R1

Fig.29 – Thermocouple temperature control with CA3079 zero voltage switch as the output amplifier.

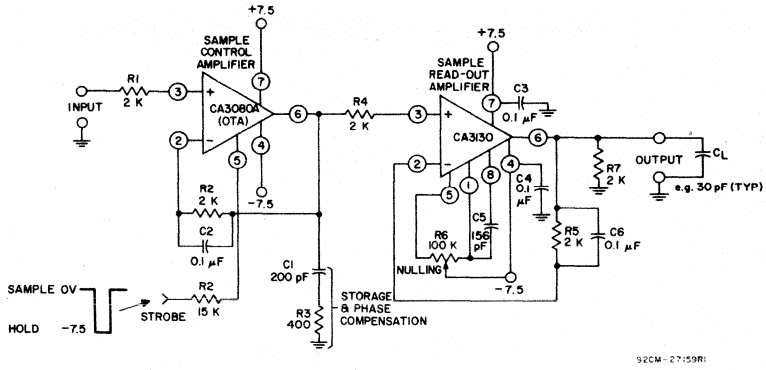
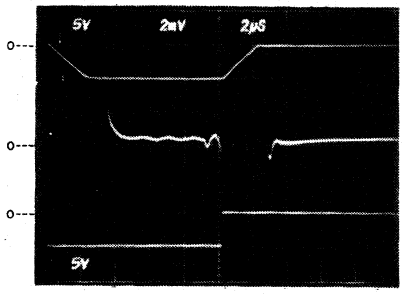
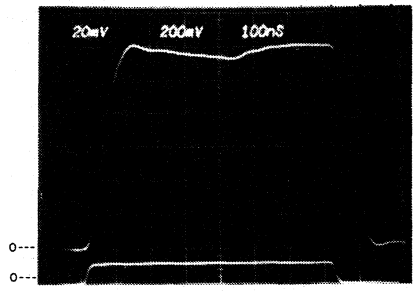


Fig.30 – Schematic diagram of the CA3080A in a sample-hold circuit with BiMos output amplifier.



TOP TRACE: OUTPUT—5 V/DIV. & 2 μs/DIV.
CENTER TRACE: DIFFERENTIAL COMPARISON OF INPUT & OUTPUT—2 mV/DIV. & 2 μs/DIV.
BOTTOM TRACE: INPUT—5 V/DIV. & 2 μs/DIV.
92CS-27161

Fig.31 – Large-signal response for circuit shown in Fig. 30.



TOP TRACE: OUTPUT—20 mV/DIV. & 100 ns/DIV.
BOTTOM TRACE: INPUT—200 mV/DIV. & 100 ns/DIV.
92CS-27160

Fig.32 – Small-signal response for circuit shown in Fig. 30.

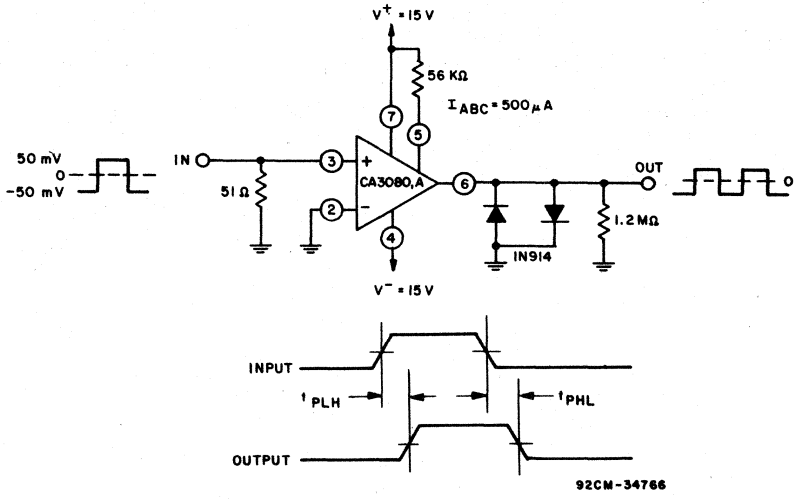
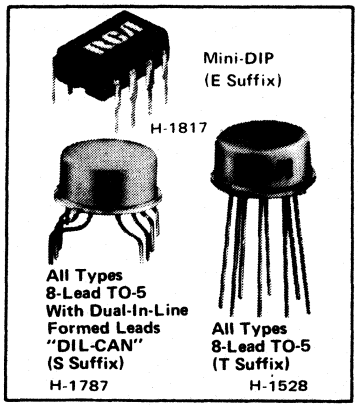


Fig. 33 - Propagation delay test circuit and associated waveforms.

CA3440, CA3440A, CA3440B



Nanopower BiMOS Op Amp

Features:

- *300-nW (typ.) standby power at $V^+ = 5$ V*
- *Supply current, BW, slew rate programmable using external resistor*
- *10-pA (typ.) input current*
- *4.0 to 15-V supply*
- *Output drives typical bipolar-type loads*
- *Low-cost 8-lead Mini-DIP, TO-5*

The RCA-CA3440B, CA3440A, and CA3440* are integrated circuit operational amplifiers that combine the advantages of MOS and bipolar transistors on a single monolithic chip.

The CA3440-series BiMOS Op Amp features gate-protected PMOS transistors in the input circuit to provide very-high-input impedance and very-low-input current (10 pA). These devices operate at total supply voltages from 4 to 15 volts and can be operated over the temperature range from −55°C to +125°C. Their virtues are programmability and very low standby power consumption (300 nW). These operational amplifiers are internally phase-compensated to achieve stable operation in the unity-gain follower configuration. Terminals are also provided for use in applications requiring input offset-voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.5 volts below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses MOS complementary source-follower form which permits moderate load driving capability (10 KΩ) at very low total standby currents (50 nA).

The CA3440-series has the same 8-lead terminal pin-out used for "741" and other industry-standard op amps with two exceptions: terminals one and five must be connected to the negative supply or to a potentiometer if nulling is required. Terminal 8 must be programmed through an external resistor returned to the negative supply.

These devices are supplied in either the standard 8-lead TO-5 style package (T suffix), 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" package (S suffix), or in the 8-lead dual-in-line plastic package "Mini-DIP" (E suffix). They are also available in chip form (H suffix).

* Formerly Dev. Type No. TA10590.

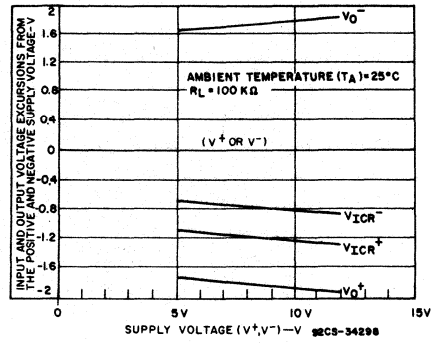


Fig. 1 - Output-voltage-swing and common-mode input-voltage range versus supply voltage.

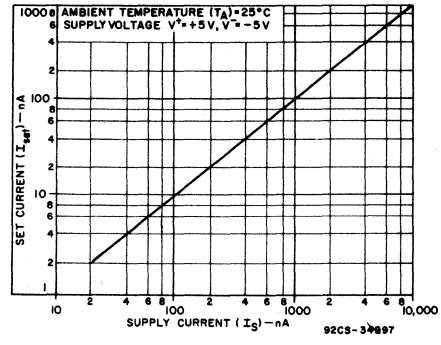


Fig. 2 - Set current versus supply current.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE
(BETWEEN V^+ AND V^- TERMINALS) ..... 25 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±9 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK —
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate linearly 6.67 mW/°C
WITH HEAT SINK —
AT 125°C ..... 418 mW
BELOW 125°C ..... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING ..... −55 to +125°C
STORAGE ..... −65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 IN. (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX. ..... +265°C

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS V^+=+5 V; V^-=-5 V R_{SET}=10 MΩ; T_A=25°C		CA3440B (T,S)	CA3440A	CA3440	UNITS
Input Resistance, R_I			2	2	2	TΩ
Input Capacitance, C_T			3.5	3.5	3.5	pF
Ouput Resistance, R_O			450	450	450	Ω
Equivalent Input Noise Voltage, e_n	f= 1 kHz	R_S=100 Ω	110	110	110	$nV/\sqrt{Hz}$
	f=10 kHz	R_S=100 Ω	110	110	110	$nV/\sqrt{Hz}$
Short-Circuit Current Source IOM^+			15	15	15	mA
To Opposite Supply Sink IOM^-			4.5	4.5	4.5	mA
Gain-Bandwidth Product, f_T			63	63	63	kHz
Slew Rate, SR			0.03	0.03	0.03	V/μs
Transient Response Rise Time, t_r	R_L= 10 kΩ		5.6	5.6	5.6	μs
Overshoot	C_L=100 pF		10	10	10	%

CA3440, CA3440A, CA3440B

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V^+ = +5 V, V^- = -5 V, T_A = 25°C Unless Otherwise Specified, R_{SET}=10 MΩ

CHARACTERISTIC	LIMITS									UNITS
	CA3440B			CA3440A			CA3440			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	0.8	2	—	2	5	—	5	10	mV
Input Offset Current, $\|I_{IO}\|$	—	2.5	10	—	2.5	20	—	2.5	30	pA
Input Current, $\|I_I\|$	—	10	30	—	10	40	—	10	50	pA
Large-Signal Voltage Gain, AOL	32K	100K	—	10K	100K	—	10K	100K	—	V/V
(R_L=10 KΩ)	90	100	—	80	100	—	80	100	—	dB
Common-Mode	—	32	180	—	100	320	—	100	320	μV/V
Rejection Ratio, CMRR	75	90	—	70	80	—	70	80	—	dB
Common-Mode Input Voltage Range, $\overline{VICR}^+$	+3.5	+3.7	—	+3.5	+3.7	—	+3.5	+3.7	—	V
$\overline{VICR}^-$	−5.0	−5.3	—	−5.0	−5.3	—	−5.0	−5.3	—	V
Power Supply Rejection Ratio, $\Delta VIO/\Delta V$	—	20	180	—	32	320	—	32	320	μV/V
PSRR	75	94	—	70	90	—	70	90	—	dB
Maximum Output Voltage, V_{OM}^+	+3	+3.2	—	+3	+3.2	—	+3	+3.2	—	V
V_{OM}^-	−3	−3.2	—	−3	−3.2	—	−3	−3.2	—	V
Supply Current, I^+	—	10	17	—	10	17	—	10	17	μA
Device Dissipation, P_D	—	100	170	—	100	170	—	100	170	μW
Input Offset Voltage Temperature Drift, $\Delta VIO/\Delta T$	—	4	—	—	4	—	—	4	—	μV/°C

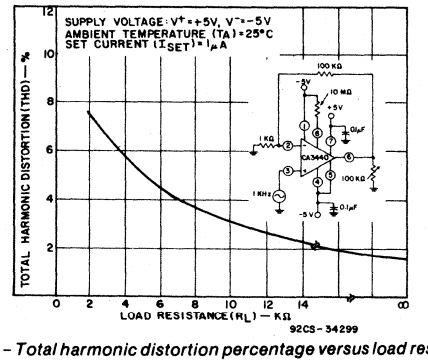


Fig. 3 - Total harmonic distortion percentage versus load resistance.

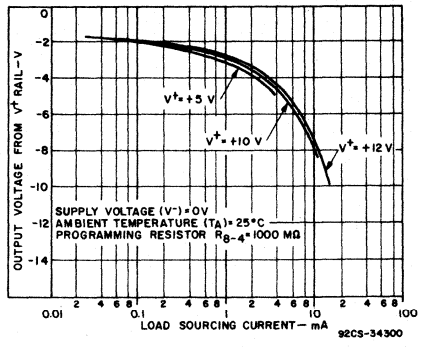


Fig. 4 - Output voltage versus sourcing load current.

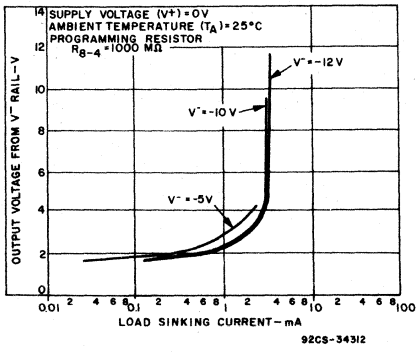


Fig. 5 - Output voltage versus sinking load current.

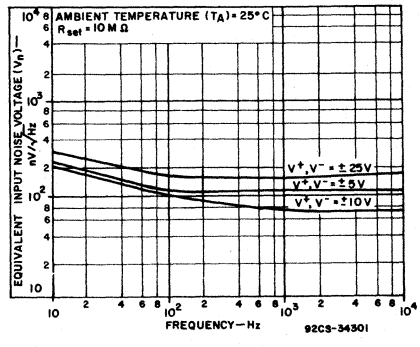


Fig. 6 - Input noise voltage versus frequency.

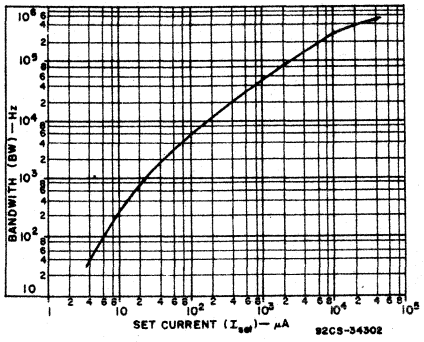


Fig. 7 - Bandwidth versus set current.

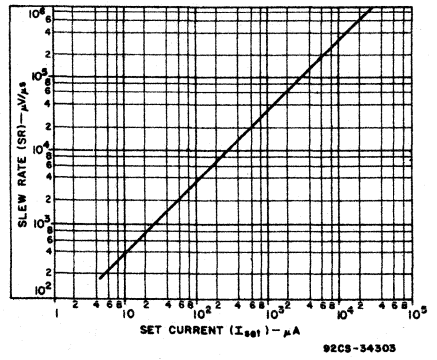


Fig. 8 - Slew rate versus set current.

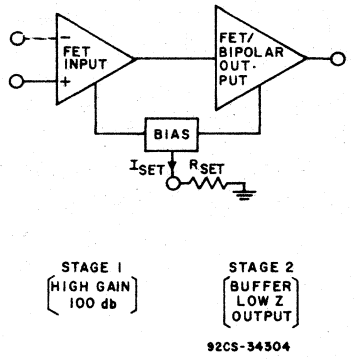


Fig. 9 - Nanopower op amp (supply current programmable using R_{SET}) 1-pA typical input bias current, 4.0 to 15-volt supply.

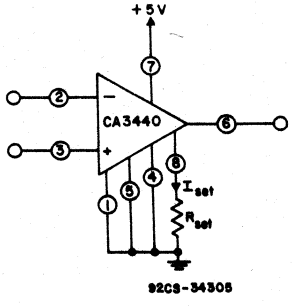


Fig. 10 - Nanopower op amp (usable standby power versus programming resistor R_{SET}).

As R_{SET} is increased, I_{SET} and the standby power decrease while the BW/SR also decreases.

Operating at a +5 V single supply, the CA3440 exhibits the following characteristics:

R_{SET}	Standby Power	BW	SR
1 MΩ	250 μW	164 kHz	0.17 V/μs
10 MΩ	25 μW	27 kHz	0.017 V/μs
100 MΩ	2.5 μW	2.6 kHz	.0017 V/μs
1000 MΩ	250 nW	78 Hz	0.00017 V/μs

The CA3440 is pin-compatible with the 741 except that pins 1 and 5 (typical negative nulling pins) must be connected either directly to pin 4 or to a negative nulling potentiometer. In addition, pin 8, the I_{SET} terminal, must be returned to either ground or −V via R_{SET}.

CA3440, CA3440A, CA3440B

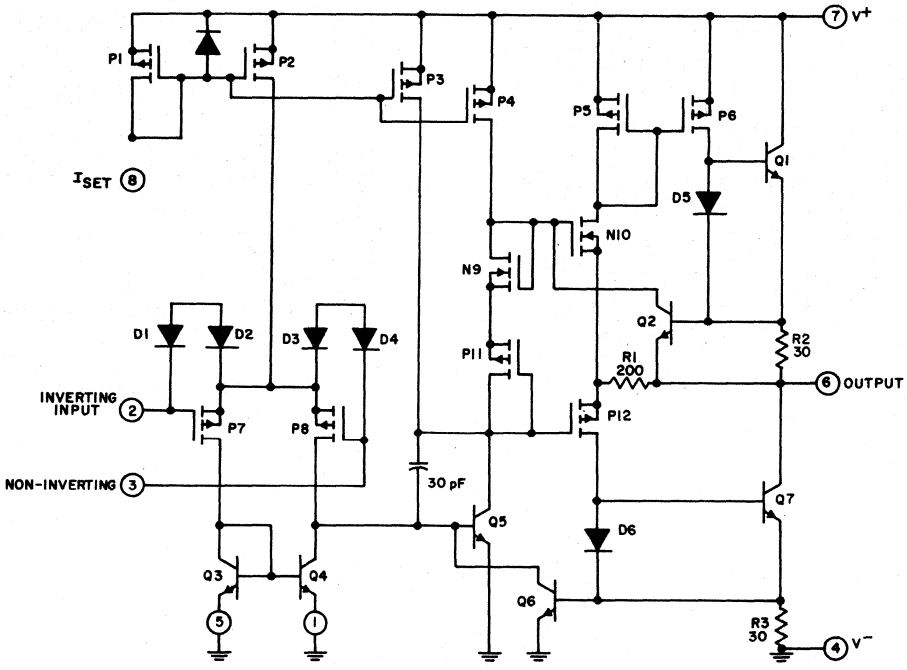


Fig. 11 - Schematic diagram for CA3440. 92CM-34308

APPLICATIONS CIRCUITS

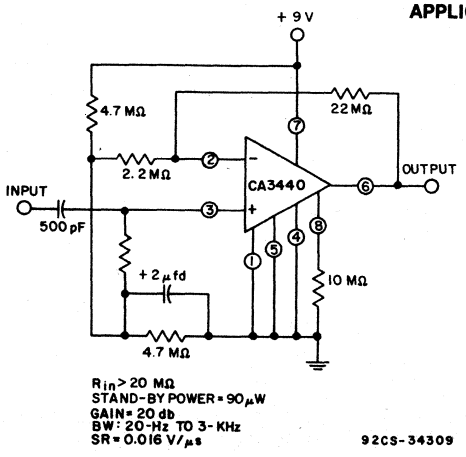


Fig. 12 - High-input impedance amplifier.

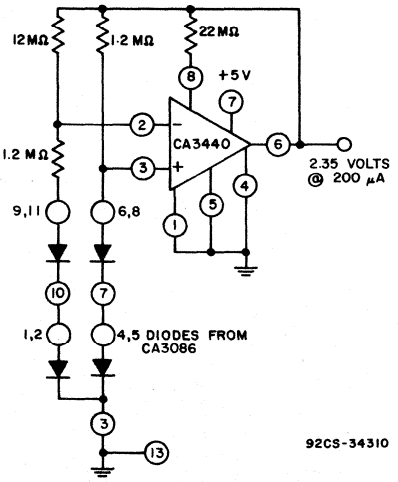
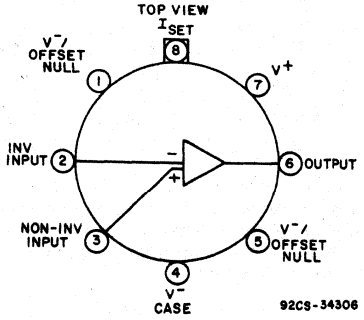
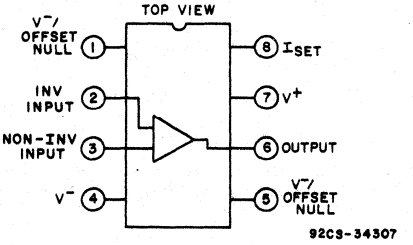


Fig. 13 - Micropower bandgap reference.

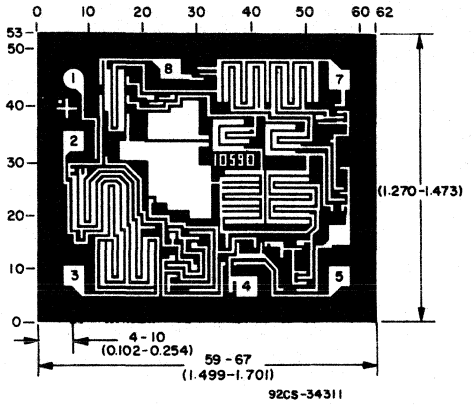


S and T Suffixes



E Suffix

Functional diagrams for CA3440 series.

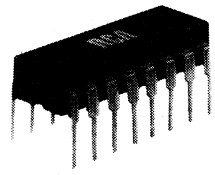


Dimensions and pad layout for CA3440H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3280, CA3280A



16-Lead Dual-In-Line Plastic Package

H-1622

Dual Variable Operational Amplifiers

Features:

- **Low initial input-offset voltage: 500 μV max. (CA3280A)**
- **Low offset-voltage change versus I_{ABC}: $<$ 500 μV typ. for all types**
- **Low offset-voltage drift: 5 μV/C max. (CA3280A)**
- **Excellent matching of the two amplifiers for all characteristics**
- **Internal current-driven linearizing diodes reduce the external input current to an offset component**
- **Differential amplifier emitters brought out for use in emitter-coupled dual-differential amplifier applications**
- **Low noise: 8 nV/$\sqrt{\text{Hz}}$ @ 1 kHz typ.**
- **Low distortion: 0.4% THD typ.**
- **Two modes of gain control**

The RCA-CA3280 and CA3280A types types consist of two variable operational amplifiers that are designed to substantially reduce the initial input offset voltage and the offset-voltage variation with respect to changes in programming current. This design results in reduced "AGC thump," an objectionable characteristic of many AGC systems. Interdigitation, or crosscoupling, of critical portions of the circuit reduces the amplifier dependence upon thermal and processing variables.

The CA3280 has all the generic characteristics of an operational voltage amplifier

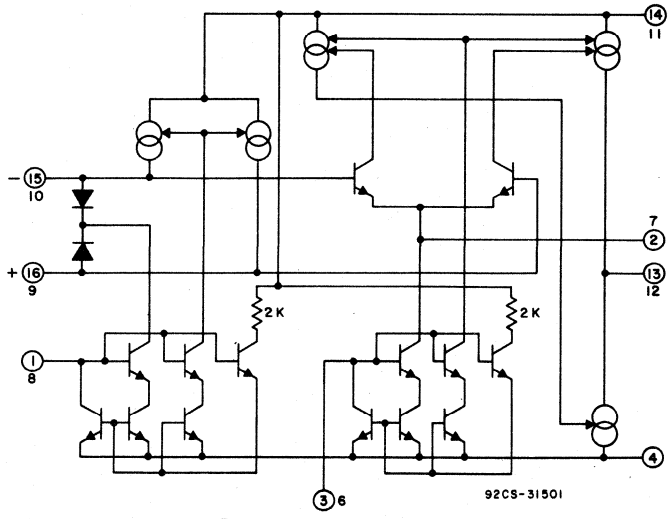


Fig. 1 — Functional diagram of 1/2 CA3280.

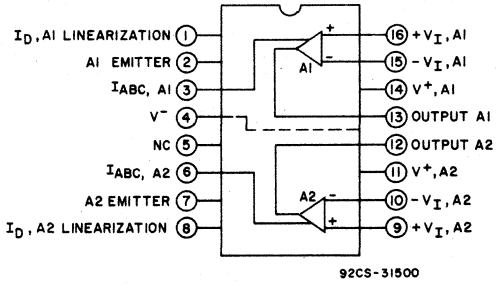
except that the forward transfer characteristic is best described by transconductance rather than voltage gain, and the output is current, not voltage. The magnitude of the output current is equal to the product of transconductance and the input voltage. This type of operational transconductance amplifier was first introduced by RCA in 1969*, and it has since gained wide acceptance as a gateable, gain-controlled building block for instrumentation and audio applications, such as linearization of transducer outputs, standardization of widely changing signals for data processing, multiplexing, instrumentation amplifiers operating from the nanopower range to high current and high-speed comparators.

* "OTA Obsoletes Op Amp," by C.F. Wheatley and H.A. Wittlinger, NEC Proceedings, December, 1969.

The CA3280 and CA3280A are supplied in the 16-lead dual-in-line plastic package (E suffix). The operating-temperature ranges are -55 to +125° C for the CA3280A and 0 to +70° C for the CA3280. The CA3280 is also supplied as a hermetic (H suffix).

Applications:

- **Voltage-controlled amplifiers**
- **Voltage-controlled filters**
- **Voltage-controlled oscillators**
- **Multipliers**
- **Demodulators**
- **Sample and hold**
- **Instrumentation amplifiers**
- **Function generators**
- **Triangle wave-to-sine wave converters**
- **Comparators**
- **Audio preamplifiers**



Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE RANGE	V^+ to V^-
INPUT SIGNAL CURRENT AT $I_D = 0$	100 μA
AMPLIFIER BIAS CURRENT	10 mA
OUTPUT SHORT CIRCUIT DURATION*	Indefinite
LINEARIZING DIODE BIAS CURRENT, I_D	5 mA
PEAK INPUT CURRENT WITH LINEARIZING DIODE	$\pm I_D$
POWER DISSIPATION, P_D:	
Either Amplifier	600 mW
Total Package	750 mW
Above 55°C	Derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE, T_A:	
Operating:	
CA3280	0 to +70°C
CA3280A	−55 to +125°C
Storage, All Types	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10 sec. max.	+265°C

* Short circuit may be applied to ground or to either supply.

CA3280, CA3280A

ELECTRICAL CHARACTERISTICS at T_A = 25°C, $V^{\pm}$ = 15 V (Unless Otherwise Stated) For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA3280			CA3280A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}	I_{ABC}=1 mA	–	–	3	–	–	0.5	mV
	I_{ABC}=100μA	–	0.7	3	–	0.25	0.5	
	I_{ABC}=10μA	–	–	3	–	–	0.5	
	I_{ABC}=1mA to 10μA T_A=full temp. range	–	0.8	4	–	0.8	1.5	
Input Offset Voltage Change, $\lvert\Delta V_{IO}\rvert$	I_{ABC}=1μA to 1mA	–	0.5	1	–	0.5	1	mV
	I_{ABC}=100μA T_A=full temp. range	–	5	–	–	3	5	μV/°C
Amplifier Bias Voltage, V_{ABC}	I_{ABC}=100μA	–	1.2	–	–	1.2	–	V
Peak Output Voltage: Positive VOM^+	I_{ABC}=500μA	12	13.7	–	12.5	13.7	–	V
Negative VOM^-		12	−14.3	–	−13.3	−14.3	–	
Positive VOM^+	I_{ABC}=5μA	12	13.9	–	12.5	13.9	–	
Negative VOM^-		12	−14.5	–	−13.5	−14.5	–	
Common-Mode Input Voltage Range, V_{ICR}	I_{ABC}=100μA	−13	–	13	−13	–	13	V
Noise Voltage, e_N: 10 Hz	I_{ABC}=500μA	–	20	–	–	20	–	$nV/\sqrt{Hz}$
1 kHz		–	8	–	–	8	–	$\mu V/\sqrt{Hz}$
10 kHz		–	7	–	–	7	–	$nV/\sqrt{Hz}$
Input Offset Current, I_{IO}	I_{ABC}=500μA	–	0.3	0.7	–	0.3	0.7	μA
Input Bias Current, I_{IB}	I_{ABC}=500μA	–	1.8	5	–	1.8	5	μA
	I_{ABC}=500μA T_A=full temp. range	–	3	8	–	3	8	
Peak Output Current: Source IOM^+	I_{ABC}=500μA	350	410	650	350	410	650	μA
Sink IOM^-		−350	−410	−650	−350	−410	−650	
Source IOM^+	I_{ABC}=5μA	3	4.1	7	3	4.1	7	
Sink IOM^-		−3	−4.1	−7	−3	−4.1	−7	
Sink and Source, IOM^-, IOM^+	I_{ABC}=500μA T_A=full temp. range	350	450	550	350	450	550	
Linearization Diodes: Dynamic Impedance	I_D = 100μA	–	700	–	–	700	–	Ω
Offset Current	I_D =100μA	–	10	–	–	10	–	μA
	I_D=10μA	–	0.5	1	–	0.5	1	

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA3280			CA3280A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Diode Network Supply Current	I_{ABC}=100μA	250	400	800	250	400	800	μA
Amplifier Supply Current (Per amplifier)	I_{ABC}=500μA	–	2	2.4	–	2	2.4	mA
Amplifier Output Leakage Current, I_{OL}	I_{ABC}=0, V_O=0V	–	0.015	0.1	–	0.015	0.1	nA
	I_{ABC}=0, V_O=30V	–	0.15	1	–	0.15	1	
Common-Mode Rejection Ratio, CMRR	I_{ABC}=100μA	80	100	–	94	100	–	dB
Power-Supply Rejection Ratio, PSRR	I_{ABC}=100μA	86	105	–	94	105	–	dB
Open-Loop Voltage Gain, A_{OL}	I_{ABC}=100μA, R_L=∞,	94	100	–	94	100	–	dB
	V_O=20 Vp-p	50K	100K	–	50K	100K	–	V/V
Forward Transconductance: Large Signal, Gm	I_{ABC}=50μA	–	0.8	1.2	–	0.8	1.2	mmho
Small Signal, gm	I_{ABC}=1mA	–	16	22	–	16	22	
Input Resistance, R_I	I_{ABC}=10μA	0.5	–	–	0.5	–	–	MΩ
Channel Separation	f=1 kHz	–	94	–	–	94	–	dB
Open-Loop Total Harmonic Distortion	f=1 kHz, I_{ABC}= 1.5 mA, R_L=15kΩ, V_O= 20 Vp-p	–	0.4	–	–	0.4	–	%
Bandwidth	I_{ABC}=1mA, R_L=100Ω	–	9	–	–	9	–	MHz
Slew Rate, SR: Open Loop	I_{ABC}=1mA	–	125	–	–	125	–	V/μs
Capacitance: Input, C_I	I_{ABC}=100μA	–	4.5	–	–	4.5	–	pF
Output, C_O		–	7.5	–	–	7.5	–	
Output Resistance, R_O	I_{ABC}=100μA	–	63	–	–	63	–	MΩ

Figs. 2 and 3 show the equivalent circuits for the current source and linearization diodes in the CA3280. The current through the linearization network is approximately equal to the programming current. There are several advantages to driving these diodes with a current source. First, only the offset current from the biasing network flows through the input resistor. Second, another input is provided to extend the gain control dynamic range. And third, the input is truly differential and can accept signals within the common-mode range of the CA3280.

The structure of the variable operational amplifier eliminates the need for matched resistor networks in differential to single-ended converters, as shown in Fig. 4. A matched resistor network requires ratio matching of 0.01% or trimming for 80 dB of common-mode rejection. The CA3280, with its excellent common-mode rejection ratio, is capable of converting a small (±25 mV) differential input signal to a single-ended output without the need for a matched resistor network.

Fig. 5 shows the CA3280 in a typical gain-control application. The input-signal range as a function of distortion at various levels of linearization diode current is shown in Fig. 6. This curve shows only the AGC capability of the diode network, but gain control can also be performed with the amplifier bias current (I_{ABC}). With no diode bias current, the gain is merely gmR_L. For example, with an I_{ABC} of 1 mA, the gm is approximately 16 mmhos. With the CA3280 operating into a 5 kΩ resistor, the gain is 80.

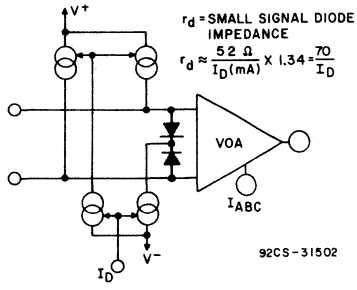


Fig. 2 – VOA showing linearization diodes and current drive.

The need for external buffers can be eliminated by the use of low-value load resistors, but the resulting increase in the required amplifier bias current reduces the input impedance of the CA3280. The linearization diode impedance also decreases as the diode bias current increases, which further loads the input. The diodes, in addition to acting as a linearization network, also operate as an additional attenuation system to accommodate input signals in the volt range when they are applied through appropriate input resistors.

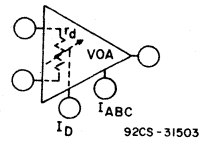


Fig. 3 – Block diagram of linearized VOA.

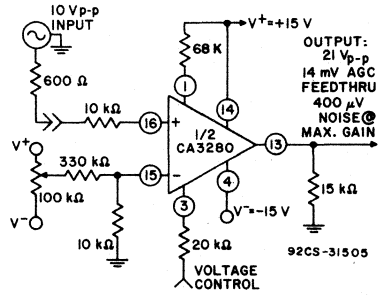


Fig. 5 – Typical gain control circuit.

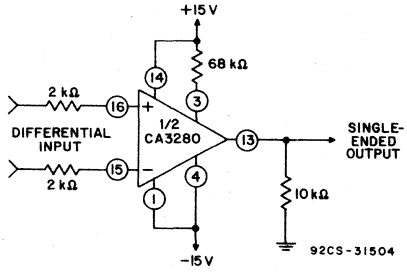


Fig. 4 – Differential to single-ended converter.

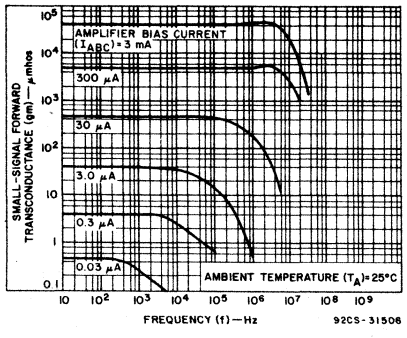


Fig. 6 – Amplifier gain as a function of frequency.

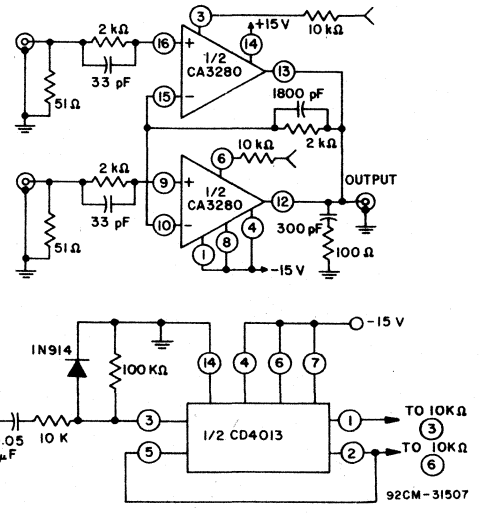


Fig. 7 – Two-channel linear multiplexer.

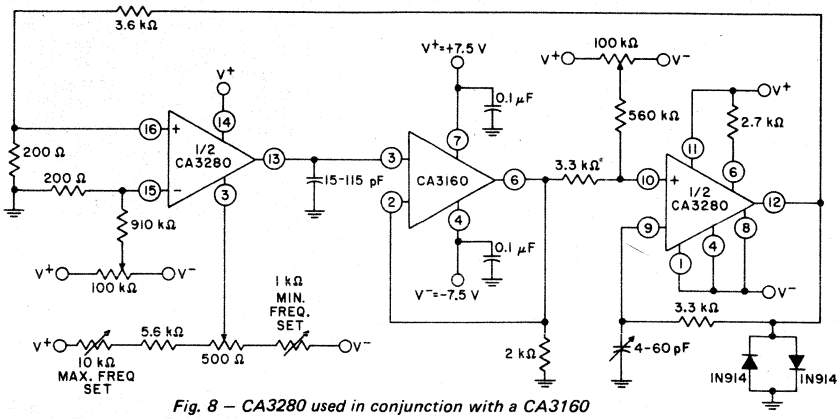


Fig. 8 – CA3280 used in conjunction with a CA3160 to provide a function generator with a tunable range of from 2 Hz to 1 MHz.

Fig. 9 shows a triangle wave-to-sine wave converter using the CA3280. Two 100KΩ resistors are connected between the differential amplifier emitters and V^+ to reduce the current flow through the differential amplifier. This allows the amplifier to fully cut off during peak input signal excursions. THD is approximately 0.37% for this circuit.

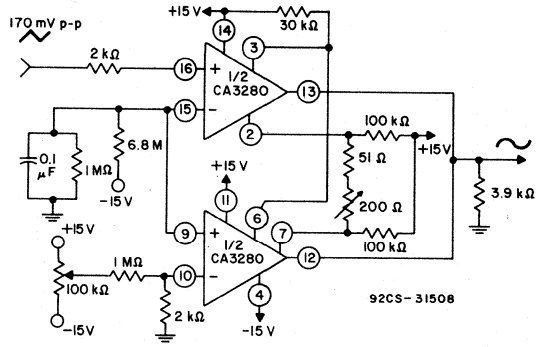


Fig. 9 – Triangle wave-to-sine wave converter.

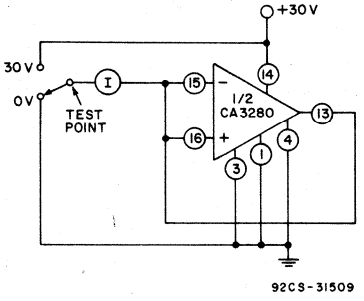


Fig. 10 – Leakage current test circuit.

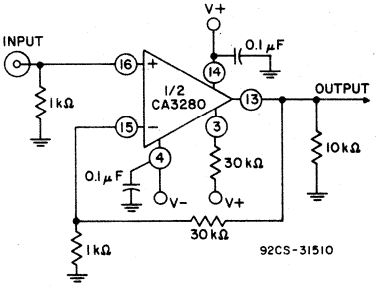
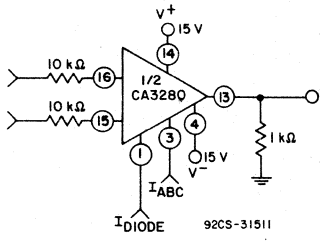
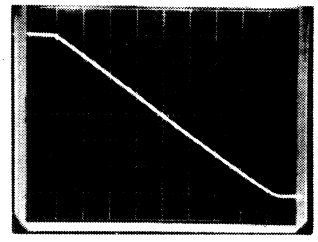
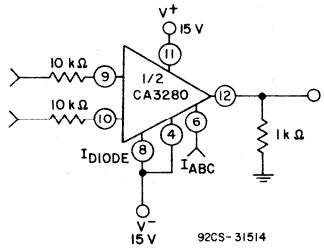


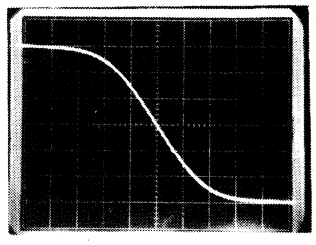
Fig. 11 – Channel separation test circuit.





a) With diode programming terminal active





b) With diode programming terminal cut-off

Fig. 12 – CA3280 transfer characteristics.

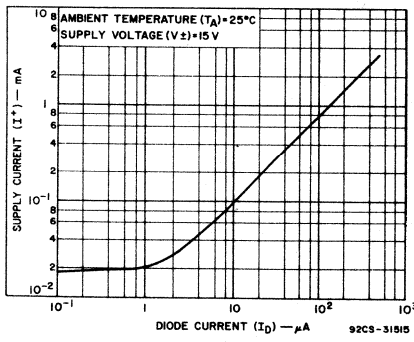


Fig. 13 – Supply current as a function of diode current.

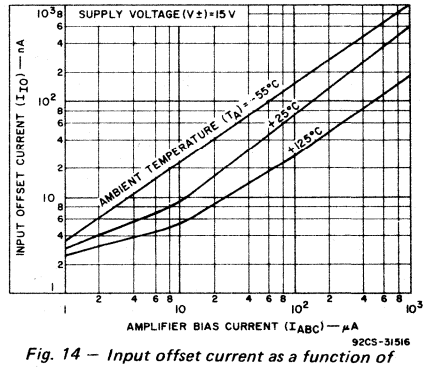


Fig. 14 – Input offset current as a function of amplifier bias current.

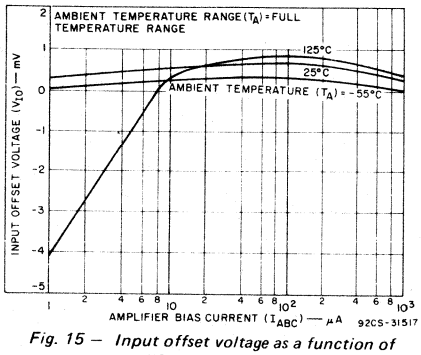


Fig. 15 – Input offset voltage as a function of amplifier bias current.

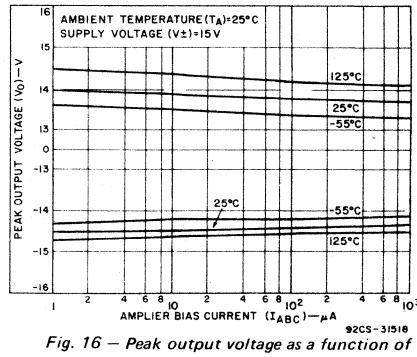


Fig. 16 – Peak output voltage as a function of amplifier bias current.

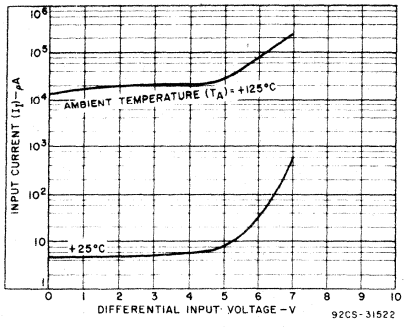


Fig. 17 – Input current as a function of input differential voltage.

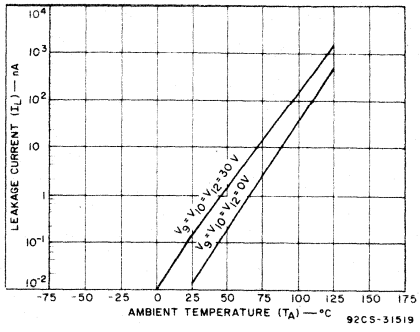


Fig. 18 – Leakage current as a function of temperature.

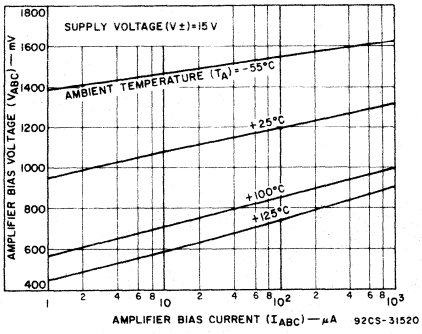


Fig. 19 – Amplifier bias voltage as a function of amplifier bias current.

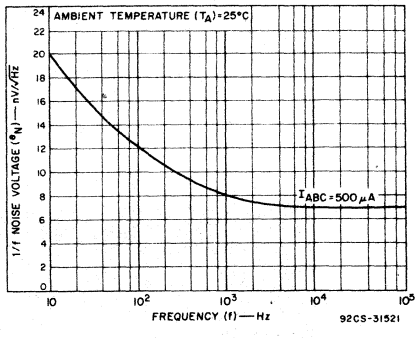


Fig. 20 – I/F noise as a function of frequency.

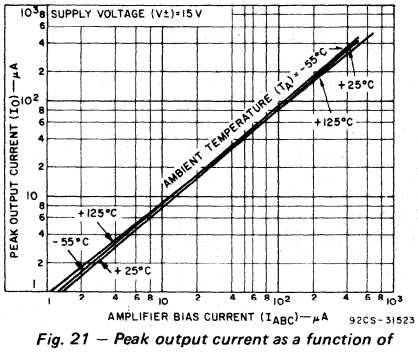


Fig. 21 – Peak output current as a function of amplifier bias current.

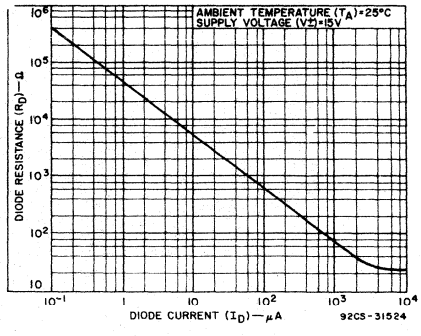


Fig. 22 – Diode resistance as a function of diode current.

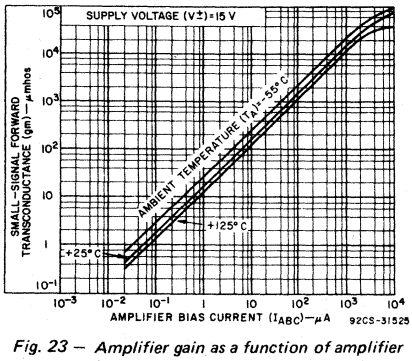


Fig. 23 – Amplifier gain as a function of amplifier bias current.

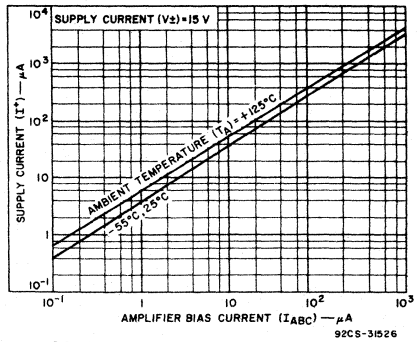


Fig. 24 – Supply current as a function of amplifier bias current.

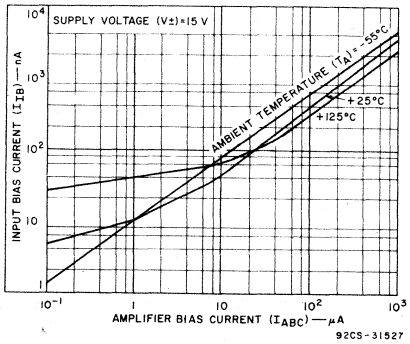
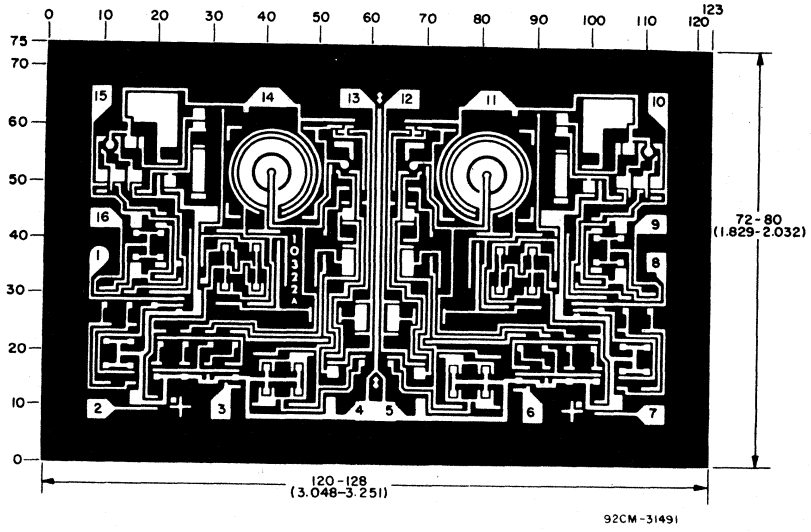


Fig. 25 – Input bias current as a function of amplifier bias current.



Dimensions and pad layout for CA3280H.

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Voltage Comparators
Technical Data

+Programmable
*BIMOS types

CA311

S-Suffix Types
(DIL-CAN)

H-1787

T-Suffix Types
(TO-5 Style)

H-1528

E-Suffix Types
(Mini-DIP)

H-1817

Voltage Comparator

For Commercial and Industrial Applications

Features:

- *Single- or dual-supply operation*
- *Power consumption - 135 mW at ±15 V*
- *Strobe capability*
- *Low input-offset current - 6 nA(typ.)*
- *Differential input-voltage range - ±30 V*
- *Directly interchangeable with National Semiconductor LM311 Series*

Applications:

- *Multivibrators*
- *Positive and negative peak detectors*
- *Crystal oscillators*
- *Zero-crossing detectors*
- *Solenoid, relay, and lamp drivers*

The RCA CA311 is a monolithic voltage comparator that operates from dual supplies up to ±15 V, or from single supplies down to 5 V. This single supply capability makes the outputs of these devices compatible with RTL, DTL, TTL, and MOS circuits. In addition they can drive lamps or relays, and switch voltages up to 40 V at currents as high as 50 mA.

The inputs and outputs of the CA311 can be isolated from system ground, allowing the output to drive loads referred to ground V^+, or V^-.

The CA311 is available in 8-lead TO-5 style packages with standard leads (T suffix), dual-in-line formed leads ("DIL-CAN", S suffix), 8-lead dual-in-line plastic package ("MINI-DIP", E suffix), and in chip form (H suffix).

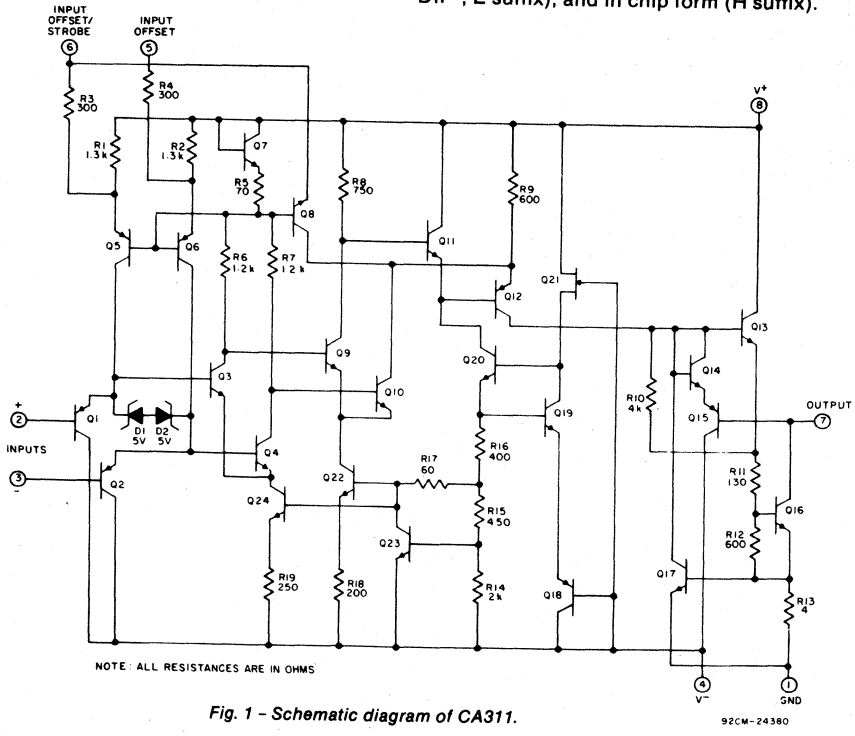


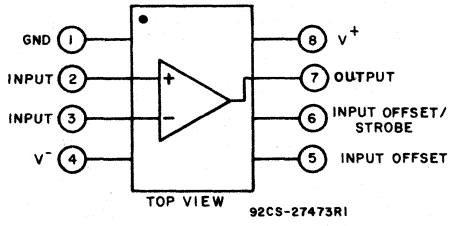
Fig. 1 - Schematic diagram of CA311.

Maximum Ratings, *Absolute Maximum Values at T_A = 25°C:*

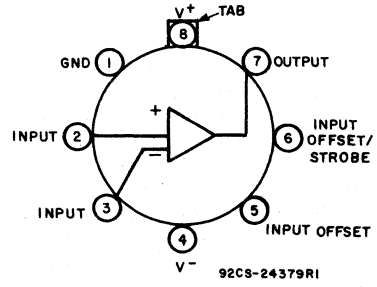
DC SUPPLY VOLTAGE (between V+ and V⁻ terminals) ..... 36 V
DC INPUT VOLTAGE* ..... ±15 V
DIFFERENTIAL INPUT VOLTAGE ..... ±30 V
OUTPUT TO NEGATIVE SUPPLY VOLTAGE (V_{7-4}) ..... 40 V
GROUND TO NEGATIVE SUPPLY VOLTAGE (V_{1-4}) ..... 30 V
OUTPUT SHORT-CIRCUIT DURATION ..... 10 s
DEVICE DISSIPATION:
  UP TO T_A = 25°C ..... 500 mW
  Above T_A = 25°C ..... derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:
  Operating ..... 0 to +70°C†
  Storage ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

*This rating applies for ±15 V supplies. The positive input-voltage limit is 30 V above the negative supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.

†Types CA311 E, S, and T can be operated over the temperature range of -55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70°C.



FUNCTIONAL DIAGRAM FOR PLASTIC PACKAGE.



FUNCTIONAL DIAGRAM FOR TO-5 STYLE PACKAGE.

TYPICAL CHARACTERISTICS

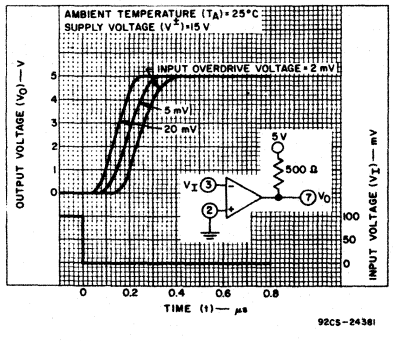


Fig. 2 - Response time for various input overdrive voltages - positive input.

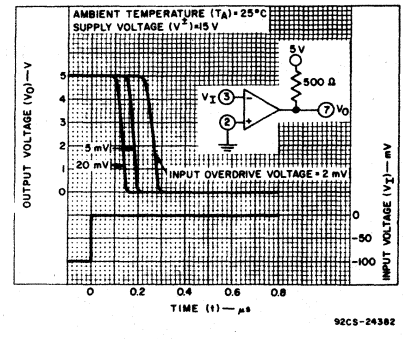


Fig. 3 - Response time for various input overdrive voltages - negative input.

CA311

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS		LIMITS			UNITS
		SUPPLY VOLTAGE (V±) = 15V UNLESS OTHERWISE SPECIFIED		CA311			
				MIN.	TYP.	MAX.	
Input Offset Voltage	V_{IO}	$R_S \leq 5$ kΩ, Note 2	T_A = 25°C	—	2	7.5	mV
			Note 1	—	—	10	
Saturation Voltage		$V_I \leq$ -10 mV, I_O = 50 mA	T_A = 25°C	—	0.75	1.5	V
		$V^+ \geq 4.5$ V, V^- -0, $V_I \leq$ -10 mV, $I_{SINK} \leq 8$ mA	Note 1	—	0.23	0.4	
Input Voltage Range	V_{IPP}		Note 1	—	±14	—	V
Input Offset Current	I_{IO}	Note 2	T_A = 25°C	—	6	50	nA
			Note 1	—	—	70	
Input Bias Current	I_{IB}	Note 2	T_A = 25°C	—	100	250	nA
			Note 1	—	—	300	
Postive Supply Current	I^+		T_A = 25°C	—	5.1	7.5	mA
Negative Supply Current	I^-		T_A = 25°C	—	4.1	5	mA
Output Leakage Current		$V_I \geq$ 10 mV, V_O = 35 V	T_A = 25°C	—	—	50	nA
Strobe on Current			T_A = 25°C	—	3	—	mA
Voltage Gain, A			T_A = 25°C	40	200	—	V/mV
Response Time		100 mV Input Step with 5 mV Overdrive Voltage	T_A = 25°C	—	200	—	ns
Input Voltage Range			T_A = 25°C	-14.5	13.8- -14.7	13	V

Note 1: Ambient temperature (T_A) over applicable operating temperature of 0 to + 70° C.

Note 2: The input offset characteristics given are the values required to drive the output to within 1 V of either supply with a 1 mA load. These characteristics define an error band which takes into account the worst-case effects of voltage gain and input impedance. The input offset voltage, input offset current, and input bias current specifications apply for any supply voltage from a 5 V single supply up to a ± 15 V dual supply.

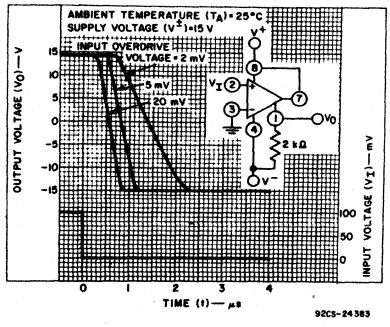


Fig. 4 - Response time for various input overdrive voltages - positive input.

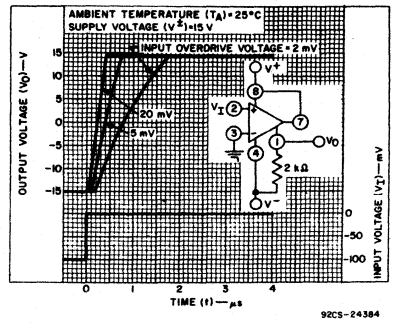


Fig. 5 - Response time for various input overdrive voltages - negative input.

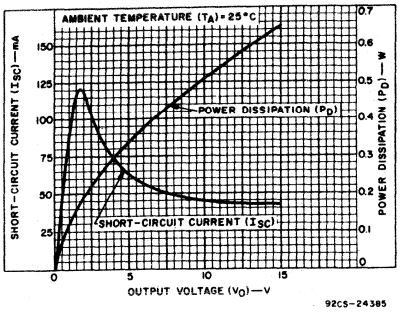


Fig. 6 - Output limiting characteristics.

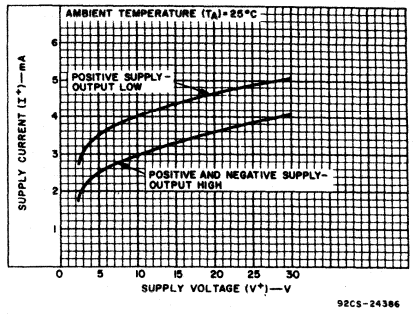


Fig. 7 - Supply current vs. supply voltage.

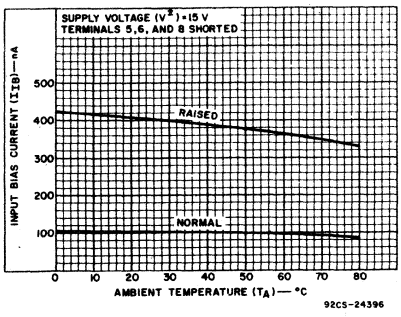


Fig. 8 - Input bias current vs. ambient temperature.

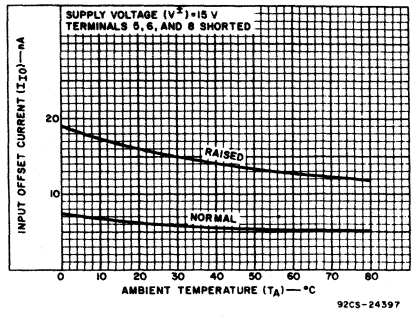


Fig. 9 - Input offset current vs. ambient temperature.

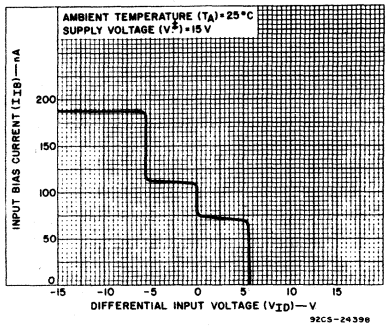


Fig. 10 - Input characteristics.

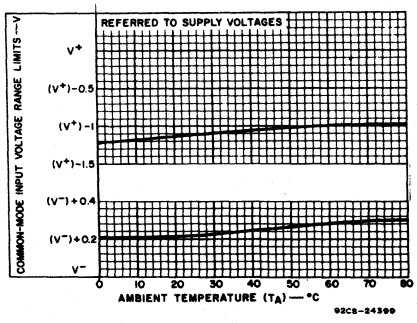


Fig. 11 - Common-mode voltage range limits vs. ambient temperature.

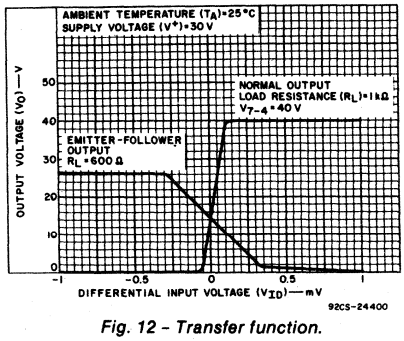


Fig. 12 - Transfer function.

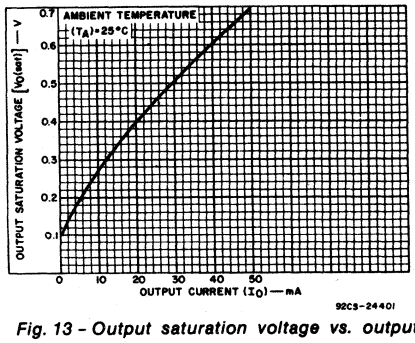


Fig. 13 - Output saturation voltage vs. output current.

CA311

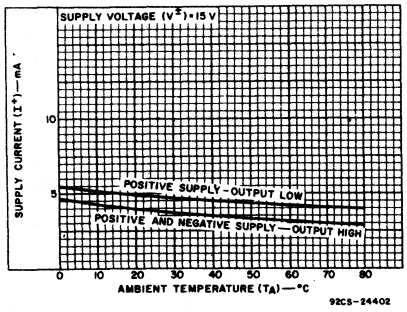


Fig. 14 - Supply current vs. ambient temperature.

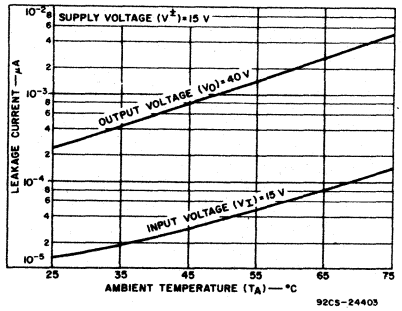


Fig. 15 - Input and output leakage current vs. ambient temperature.

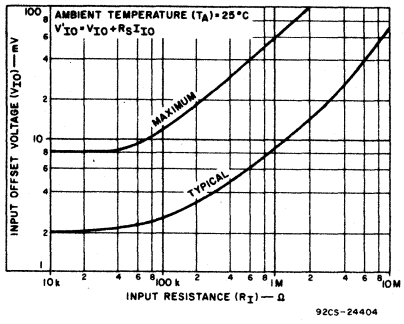


Fig. 16 - Offset error.

TYPICAL APPLICATIONS

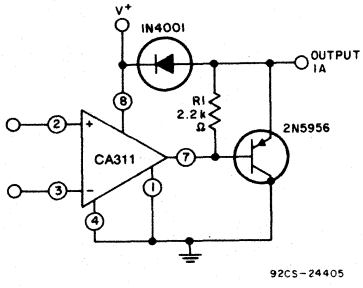


Fig. 17 - Comparator and solenoid driver.

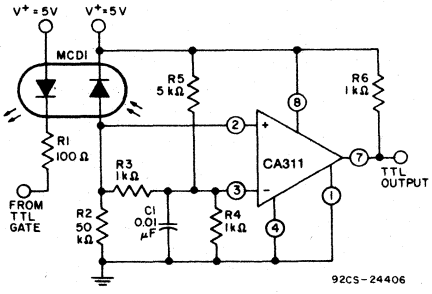


Fig. 18 - Digital transmission isolator.

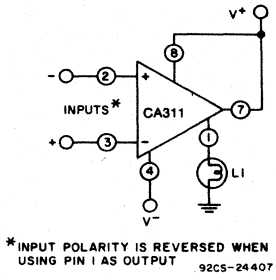


Fig. 19 - Driving a ground-referred load.

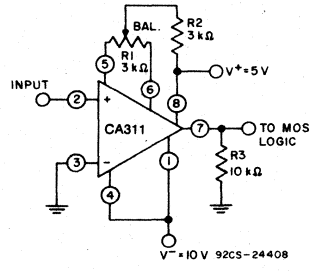


Fig. 20 - Zero-crossing detector driving MOS logic.

TYPICAL APPLICATIONS (cont'd)

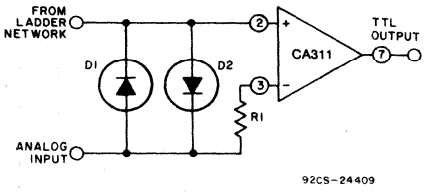


Fig. 21 - Using clamp diodes to improve response.

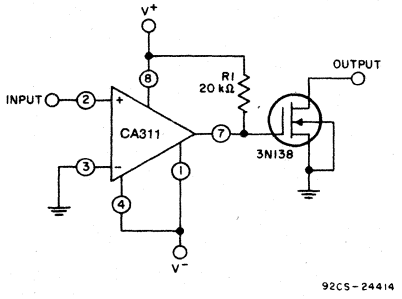


Fig. 23 - Zero-crossing detector driving and MOS switch.

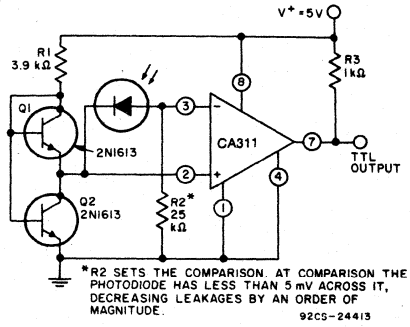


Fig. 25 - Precision photodiode comparator.

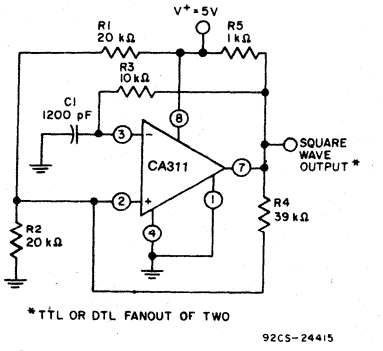


Fig. 26 - 100-kHz free-running multivibrator.

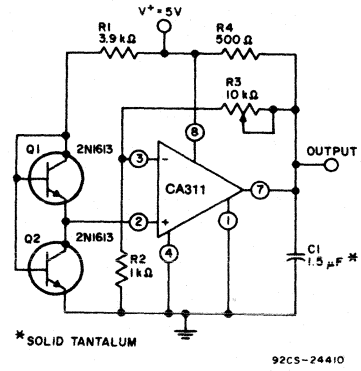


Fig. 22 - Low-voltage adjustable-reference supply.

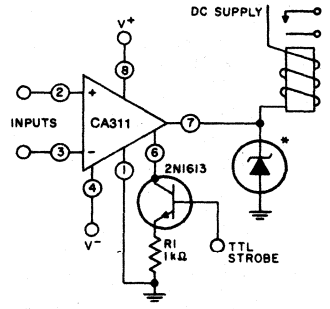


Fig. 24 - Relay driver with strobe.

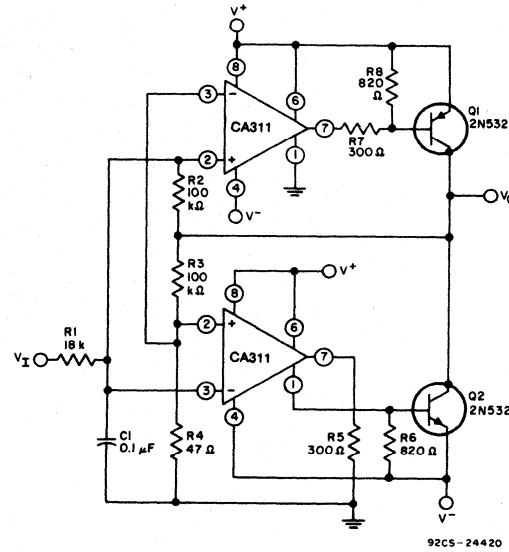


Fig. 27 - Switching power amplifier.

TYPICAL APPLICATIONS (cont'd)

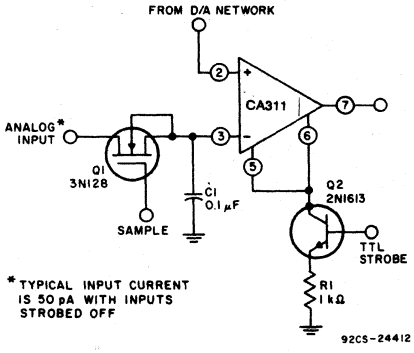


Fig. 28 - Strobing off both input and output stages.

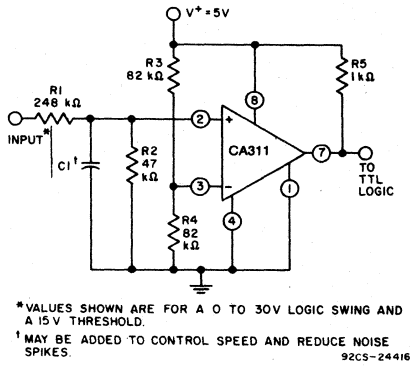


Fig. 29 - TTL interface with high-level logic.

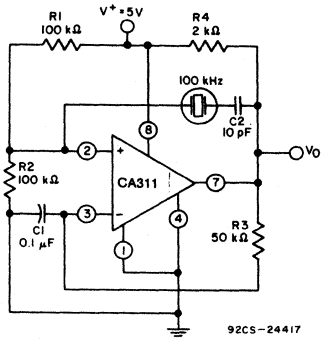


Fig. 30 - Crystal oscillator.

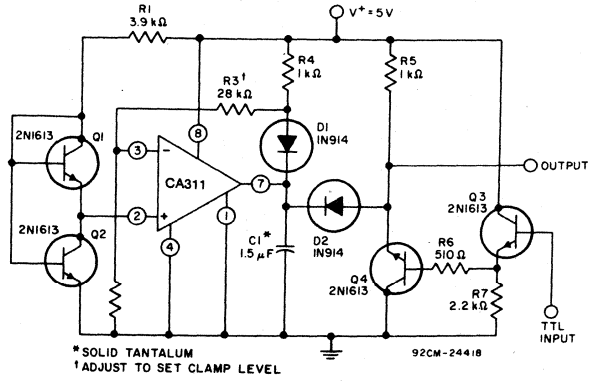


Fig. 31 - Precision squarer.

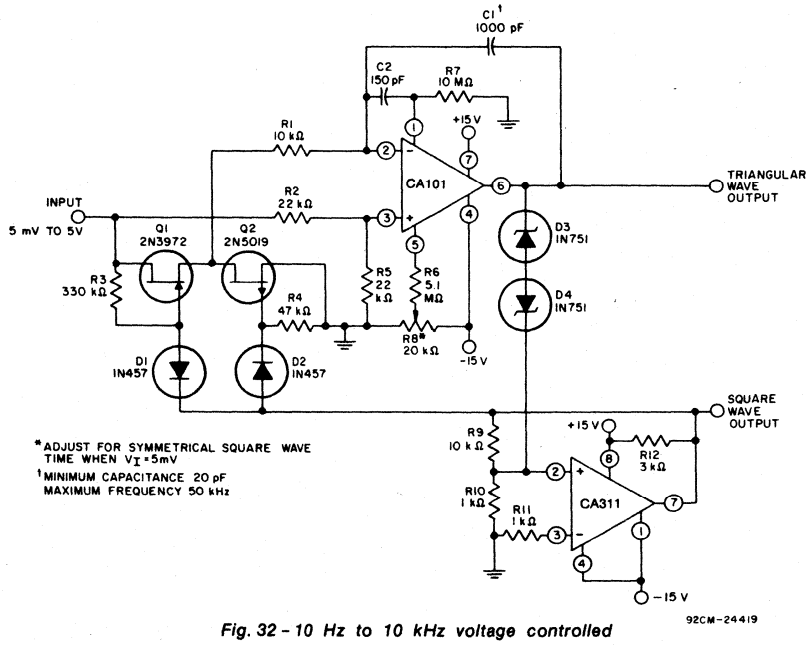


Fig. 32 - 10 Hz to 10 kHz voltage controlled oscillator.

TYPICAL APPLICATIONS (cont'd)

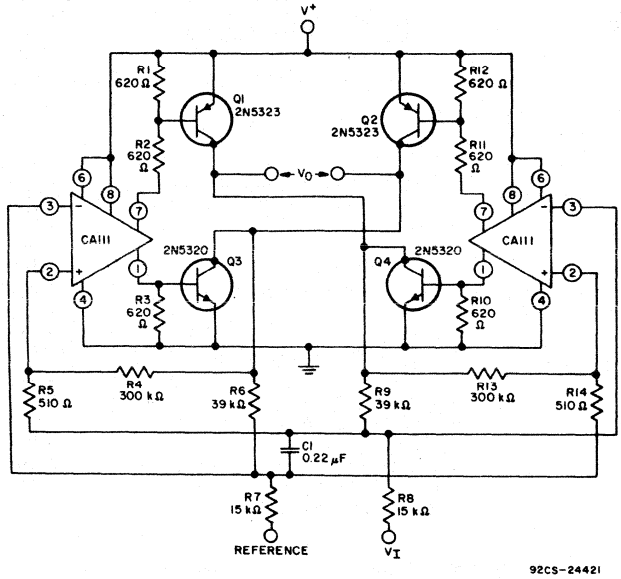
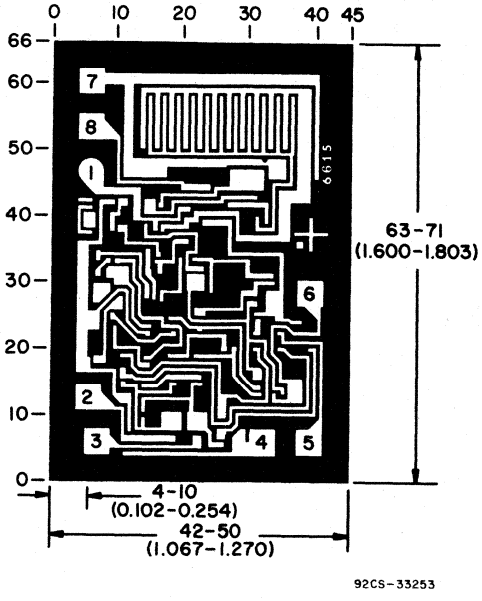


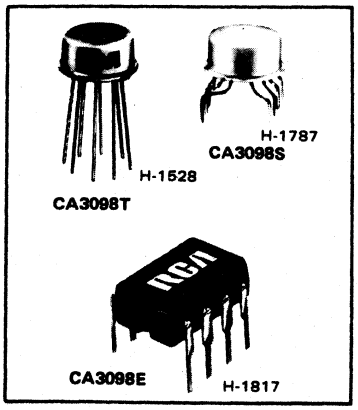
Fig. 33 - Switching power amplifier.



Dimensions and pad layout for CA311H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3098



Programmable Schmitt Trigger — With Memory

— Dual-Input Precision Level Detectors

Features:

- *Programmable operating current*
- *Micropower standby dissipation*
- *Direct control of currents up to 150 mA*
- *Low input on/off current of less than 1 nA for programmable bias current of 1 μA*
- *Built-in hysteresis: 20 mV max.*
- *Programmable hysteresis: 20 mV to V+*
- *Dual reference input*
- *High sensor range: 100 Ω to 100 MΩ*
- *Stable predictable switching levels*
- *Temperature-compensated reference voltage*
- *Power can be strobed off via term. 2*

Applications:

- *Control of relays, heaters, LED's lamps, photo-sensitive devices, thyristors, solenoids, etc.*
- *Signal reconditioning*
- *Phase and frequency modulators*
- *On/off motor switching*
- *Schmitt triggers, level detectors*
- *Time delays*
- *Overvoltage, overcurrent, over-temperature protection*
- *Battery-operated equipment*
- *Square and triangular-wave generators*

The RCA-CA3098 Programmable Schmitt Trigger is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3098 can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with maximum operating voltage of ±8 volts. It can directly control currents up to 150 mA and operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3098 contains the following major circuit-function features (see Fig. 1):

1. Differential amplifiers and summer: the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.

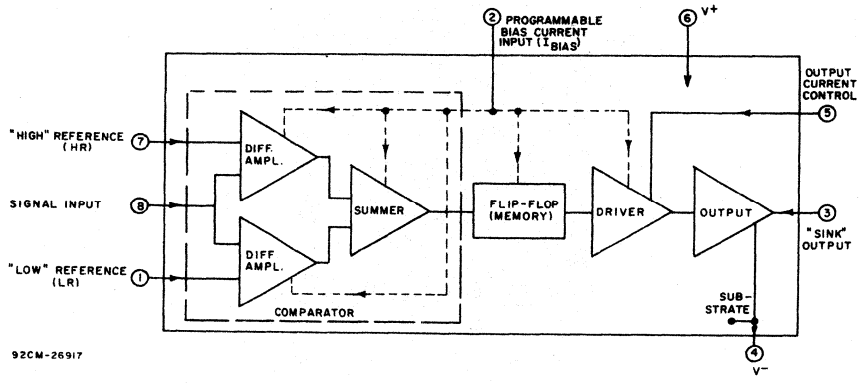


Fig. 1 — Block diagram of CA3098 programmable Schmitt trigger.

2. Flip-flop: the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. Driver and otuput stages: these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. Programmable operating current: the circuit incorporates access at terminal 2 to permit programming the desired quiescent operating current and performance parameters.

The CA3098 is supplied in the 8-lead dual-in-line plastic package ("Mini-Dip", E suffix), 8-lead TO-5 style package (T suffix), 8-lead TO-5-style package with formed leads "DIL-CAN" (S suffix), and in chip form (H suffix).

For information on another RCA Dual-Input Precision Level Detector, see the data bulletin for the RCA-CA3099E, File No. 620.

ELECTRICAL CHARACTERISTICS at T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	Fig. No.	LIMITS			UNITS
			Min.	Typ.	Max.	
Input Offset Voltage: "Low" Ref., $V_{IO(LR)}$	V_{LR} = Gnd, V_{HR} = 3 V, I_{BIAS} = 100 μA	5	−15	−3	6	mV
"High" Ref., $V_{IO(HR)}$	V_{HR} = Gnd, V_{LR} = −3 V, I_{BIAS} = 100 μA	6	−10	±10	10	
Temp. Coeff: "Low" Ref.	−55 °C to + 125 °C	7	–	4.5	–	μV/°C
"High" Ref.	−55 °C to + 125 °C	8	–	±8.2	–	
Min. Hysteresis Voltage $V_{IO(HR-LR)}$:	V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	9	–	3	20	mV
Temp. Coeff.	−55°C to + 125 °C	10	–	6.7	–	μV/°C
Output Saturation Voltage, $V_{CE(SAT)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	11,12	–	0.72	1.2	V
Total Supply Current, I_{TOTAL}: "ON"	V_I = 4 V, V_{REG} = 6 V; V^+ = 12 V, I_{BIAS} = 100 μA	13,14	500	710	800	μA
"OFF"	V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA		400	560	750	μA
Input Bias Current, I_{IB}: $I_{B(p-n-p)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	15	–	42	100	nA
$I_{B(n-p-n)}$	V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA		–	28	100	nA
Output Leakage Current, $I_{CE(OFF)}$	Current from Term. 3 when Q46 is "OFF"	–	–	–	10	μA
Switching Times: Delay, t_d	I_C = 100 μA, I_{BIAS} = 100 μA, V^+ = 5 V, V_{REG} = 2.5 V	18	–	600	–	ns
Fall, t_f			–	50	–	ns
Rise, t_r			–	500	–	ns
Storage, t_s			–	4.5	–	μs
Output Current, I_O	V^+ = 12 V, I_{BIAS} = 50 μA	–	100	–	–	mA

Maximum Ratings, *Absolute-Maximum Values at* $T_A = 25°C$*:*

Supply Voltage Between Terminals 6 and 4,	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4	16	V
Differential Input Voltage Between Terminals 8 and 1, and Terminals 7 and 8	10	V
Operating Voltage Range:		
Term. 8	V^- to V^+	
Term. 7	(V^- plus 2.0 V) to V^+	
Term. 1	(V^-) to (V^+ minus 2.0 V)	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programmable Bias Current (Term. 2)	1	mA
Output Current Control (Term. 5)	15	mA
Power Dissipation:		
Without Heat Sink:		
Up to $T_A = 55°C$		
CA3098S, CA3098T	630	mW
CA3098E	630	mW
Above $T_A = 55°C$ Derate linearly at	6.67	mW/°C
With Heat Sink:		
Up to $T_A = 55°C$		
CA3098S, CA3098T	1.6	W
Above $T_A = 55°C$		
CA3098S, CA3098T Derate linearly at	16.67	mW/°C
Ambient Temperature Range (All Packages):		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

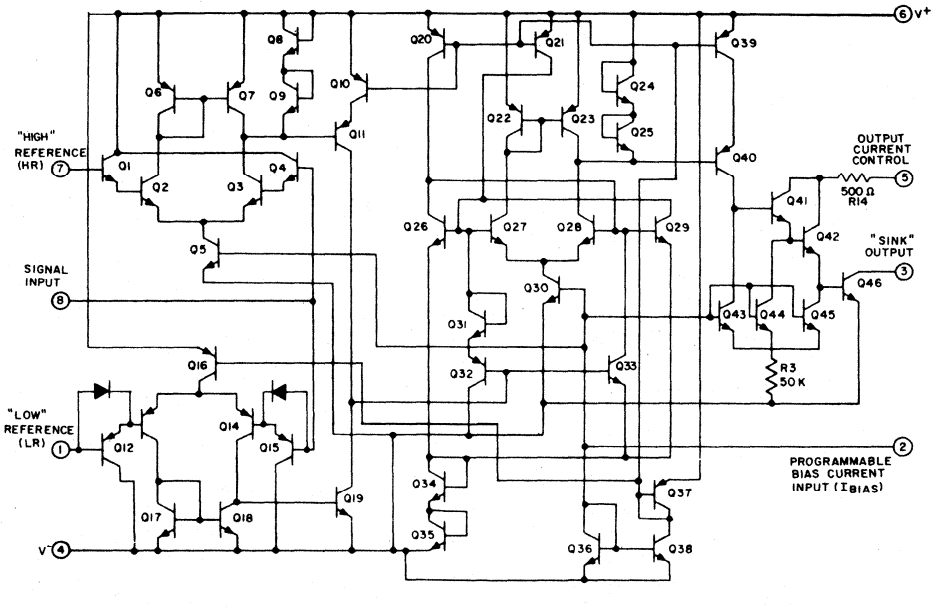


Fig. 2 – Schematic Diagram of CA3098.

General Description of Circuit Operation (Refer to Figs. 2, 3, 4)

When the signal-input voltage of the CA3098 is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

The CA3098 comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{bias}) supplied to terminal 2.

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 5. Figs. 3 and 4 highlight the operation of the CA3098 when connected as a simple hysteresis switch (Schmitt trigger).

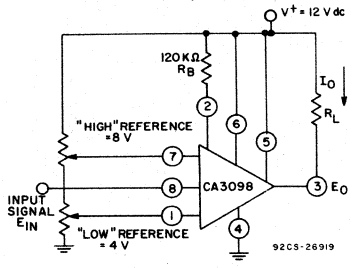


Fig. 3 – Basic hysteresis switch (Schmitt trigger).

Sequence	Input Signal Level	Output Voltage (V) (Term. 3)
1	$4 \geqslant E_{IN} > 0$	0
2	$8 \geqslant E_{IN} > 4$	0
3	$E_{IN} > 8$	12
2	$8 \geqslant E_{IN} > 4$	12
1	$4 \geqslant E_{IN} > 0$	0

Fig. 4 – Resultant output states of the CA3098, shown in Fig. 3 as a function of various input signal levels.

TYPICAL CHARACTERISTIC CURVES

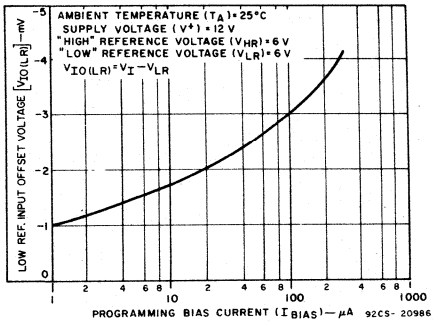


Fig. 5 – Input-offset voltage ("low" reference) vs. programming bias current.

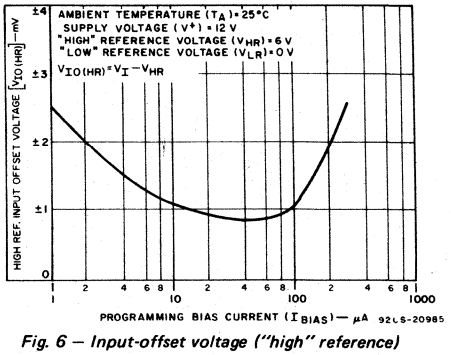


Fig. 6 – Input-offset voltage ("high" reference) vs. programming bias current.

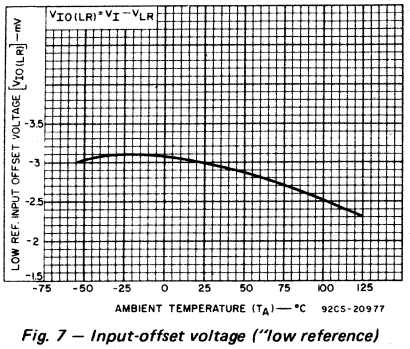


Fig. 7 – Input-offset voltage ("low reference) vs. ambient temperature.

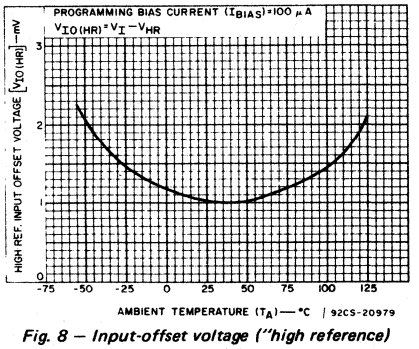


Fig. 8 – Input-offset voltage ("high reference) vs. ambient temperature.

TYPICAL CHARACTERISTIC CURVES (Cont'd)

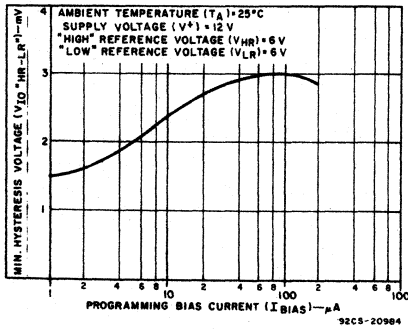


Fig. 9 – Min. hysteresis voltage vs. programming bias current.

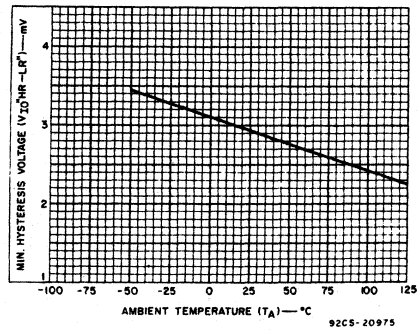


Fig. 10 – Min. hysteresis voltage vs. ambient temperature.

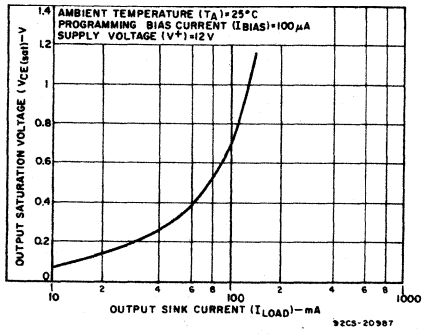


Fig. 11 – Output saturation voltage vs. output sink current.

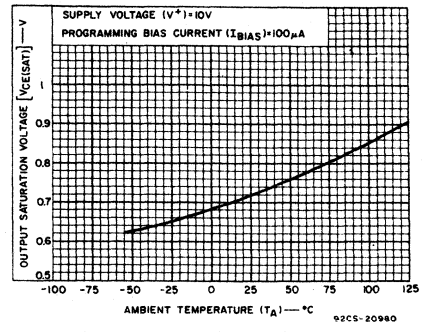


Fig. 12 – Output saturation voltage vs. ambient temperature.

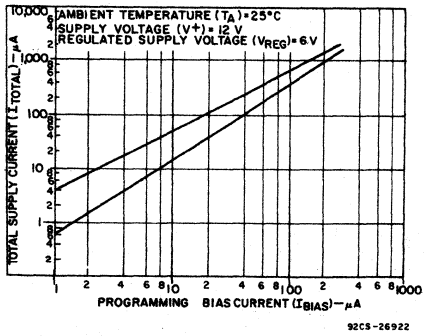


Fig. 13 – Total supply current vs. programming bias current.

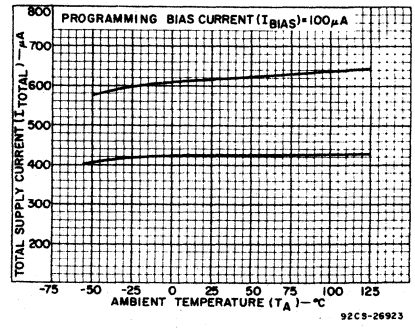


Fig. 14 – Total supply current vs. ambient temperature.

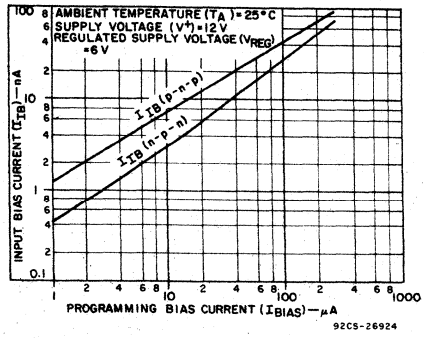


Fig. 15 – Input bias current vs. programming bias current.

TEST CIRCUIT

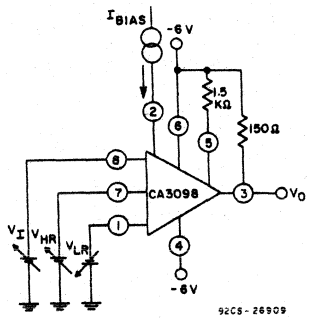


Fig. 16 – Input-offset voltage test circuit.

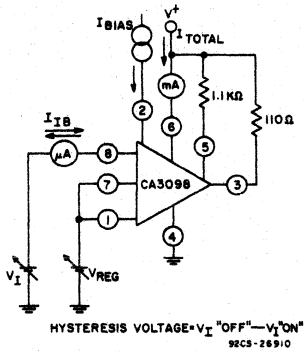


Fig. 17 – Min. hysteresis voltage, total supply current, and input-bias-current test circuit.

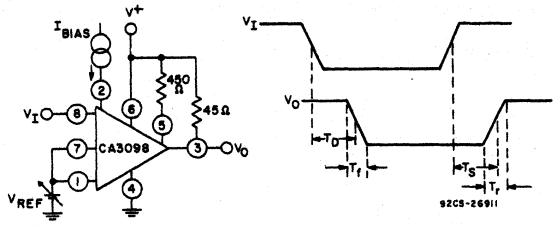


Fig. 18 – Switching time test circuit.

TYPICAL APPLICATIONS

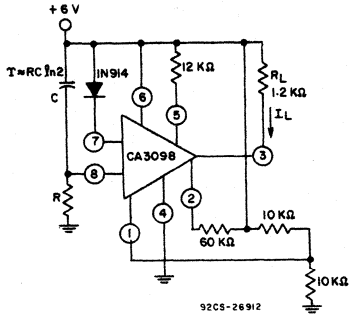


Fig. 19 – Time delay circuit: Terminal 3 "sinks" after τ seconds.

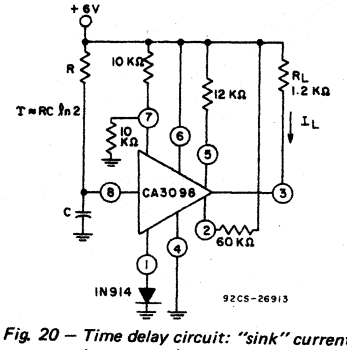


Fig. 20 – Time delay circuit: "sink" current interrupted after τ seconds.

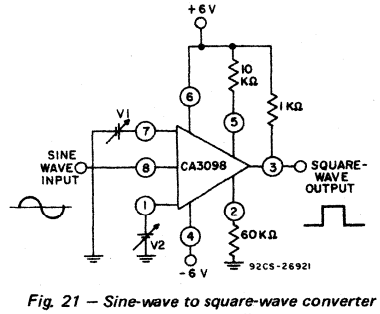
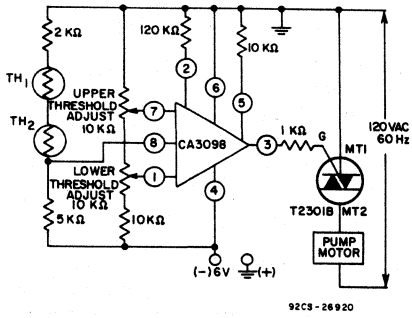


Fig. 21 – Sine-wave to square-wave converter with duty-cycle adjustment (V_1 and V_2).

TYPICAL APPLICATIONS (Cont'd)



Notes (a) Motor pump is "ON" when water level rises above thermistor TH_2.
(b) Motor pump remains "ON" until water level falls below thermistor TH_1.
(c) Thermistors, operate in self-heating mode.

Fig. 22(a) – Water-level control.

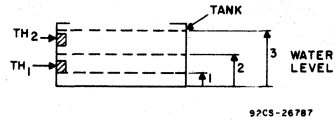


Fig. 22(b) – Water level diagram for circuit of Fig. 22(a).

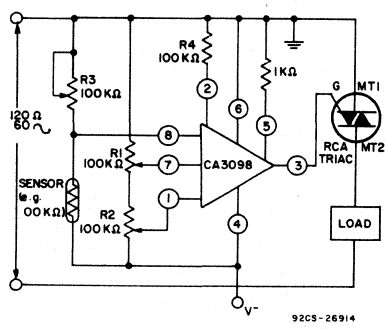


Fig. 23 – OFF/ON control of triac with programmable hysteresis.

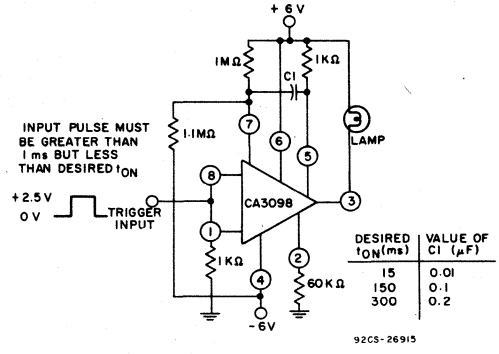
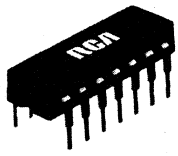


Fig. 24 – One-shot multivibrator.

CA3099E

Programmable Comparator - - With Memory



14-Lead Dual-in-Line Plastic Package H-1517

Features:

- Programmable operating current
- Micro-power standby dissipation
- Directly controls current up to 150 mA
- Low input on/off current of less than 1 nA for programmable bias current of 1 μA
- Built-in hysteresis: 10 mV max.
- Programmable hysteresis: 10 mV to V^+
- Dual reference input
- High sensor range: 100 Ω to 100 MΩ
- Stable predictable switching levels
- Temperature-compensated reference voltage

Applications:

- Control of relays, heaters, LED's, lamps, photo-sensitive devices, thyristors, solenoids, etc.
- Signal reconditioning
- Phase and frequency modulators
- On/off motor switching
- Schmitt triggers, level detectors
- Time delays
- Overvoltage, overcurrent, overtemperature protection
- Battery-operated equipment
- Square and triangular-wave generators

RCA-CA3099E* Programmable Comparator is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3099E can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with a maximum operating voltage of ± 8 volts. It can directly control currents up to 150 mA. It operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3099E contains the following six (6) major circuit-function features (Figure 1):

1. **Differential amplifiers and summer;** the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.

* Formerly Developmental No. TA6189.

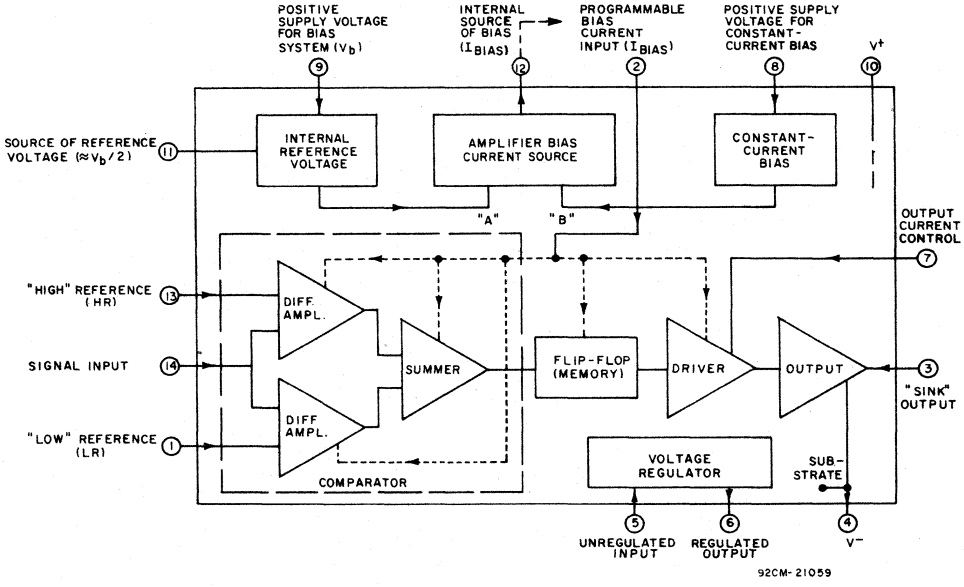


Fig. 1—Block diagram of CA3099E programmable comparator.
(See page 3 for general description of circuit operation.)

CA3099E

Major Circuit-Function Features (Cont'd)

2. **Flip-flop;** the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. **Driver and output stages;** these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. **Programmable operating current;** the circuit incorporates a separate terminal to permit programming the desired quiescent operating current and performance parameters.
5. **Internal sources of reference voltage and programmable bias current;** an integral circuit supplies a temperature-compensated reference voltage ($V_b/2$) which is about 1/2 of the externally applied bias voltage (V_b). Additionally, integral circuitry can optionally be used to supply an uncompensated constant-current source of bias (I_{bias}).
6. **Voltage regulator;** provides optional on-chip voltage regulation when power for the CA3099E is provided by an unregulated supply.

Maximum Ratings, *Absolute-Maximum Values at $T_A = 25^oC$:*

Supply Voltage Between Terminals 10 and 4, 9 and 4, 8 and 4	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4.	16	V
Differential Input Voltage Between Terminals 14 and 1, and Terminals 13 and 14	10	V
Operating Voltage Range:		
Term. 14	0 V to V^+	
Term. 13	2.0 V to V^+	
Term. 1	0 V to V^+ minus 2.0 V	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programming Bias Current (Term. 2)	1	mA
Output Current Control (Term. 7)	15	mA
Power Dissipation:		
Up to $T_A = 55^oC$	750	mW
Above $T_A = 55^oC$. Derate Linearly at	6.67	mW/^oC
Ambient Temperature Range:		
Operating	−55 to +125	^oC
Storage	−65 to +150	^oC
Lead Termperature (During Soldering): At distance not less than 1/32 inch (3.17 mm) from seating plane for 10 s maximum	+265	^oC

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$ *(Unless otherwise indicated)*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS $T_A = 25^oC$ Unless Otherwise Indicated	FIG. No.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Reference Voltage	V_{REF}	Term. 9 = 12 V, Term.4 = Grd, Term.11 = Test	–	5.7	6	6.3	V
Reference Voltage Temperature Coefficient			–	–	100	–	μV/^oC
Regulated Supply Voltage	V_{REG}	Term.5 1K to 12V, Term.4 = Grd, Term.6 10K to Grd	5	6	7.2	8	V
Regulated Supply Voltage Temperature Coefficient			5	–	2.9	–	mV/^oC
Input Offset Voltage: "Low" Reference	V_{IO} (LR)	V_{LR} = Grd, V_{HR} = 3 V, I_{BIAS} = 100 μA	20, 6	−8	−3	2	mV
"High" Reference	V_{IO} (HR)	V_{HR} = Grd, V_{LR} = −3 V, I_{BIAS} = 100 μA	20, 7	−5	±1	5	mV
"Low" Reference Temp. Coefficient		−55°C to +125°C	20, 8	–	4.5	20	μV/^oC
"High" Reference Temp. Coefficient		−55°C to +125°C	20, 9	–	±8.2	±20	μV/^oC
Min. Hysteresis Voltage	$V_{IO(HR-LR)}$	V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21, 10	–	3	10	mV
Min. Hysteresis Voltage Temperature Coefficient		−55°C to +125°C	11	–	6.7	20	μV/^oC
Output Saturation Voltage	$V_{CE(SAT)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,12,13	–	0.72	1.2	V
Total Supply Current: I_{TOTAL} "ON"	I_{TOTAL}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,14,15	600	710	800	μA
I_{TOTAL} "OFF"		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,14,15	420	560	750	μA
Input Bias Current: $I_{B(p-n-p)}$	I_{IB}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,16,17	–	33	200	nA
$I_{B(n-p-n)}$		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,16,17	–	20	60	nA
Output Leakage Current	$I_{CE(OFF)}$	Current from Term.3 when Q46 is "OFF"	–	–	–	10	μA
Internal Bias Current	I_{IBC}		18,19	120	200	280	μA
Switching Times:		I_C = 100 μA, I_{BIAS} = 100 μA, V^+ = 5 V, V_{REG} = 2.5 V					
Delay	t_d		22	–	600	–	ns
Fall	t_f		22	–	50	–	ns
Rise	t_r		22	–	500	–	ns
Storage	t_s		22	–	4.5	–	ns

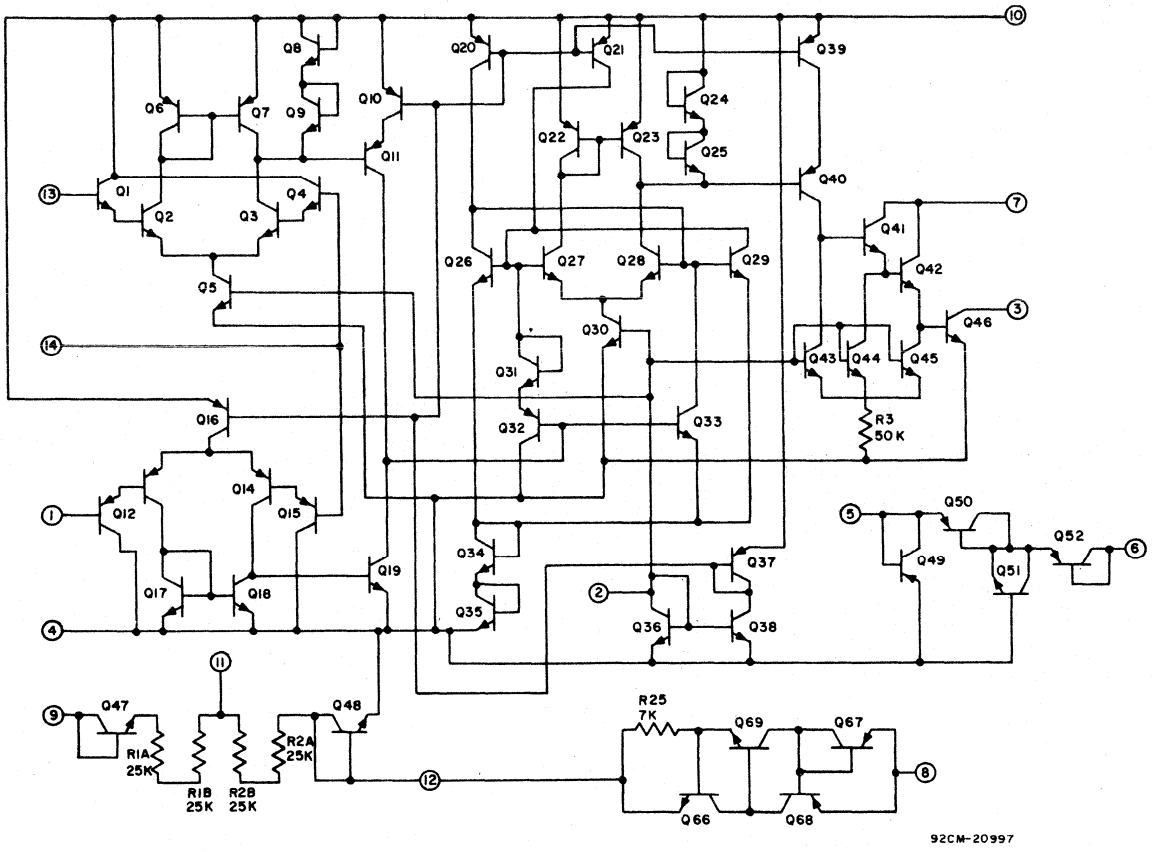


Fig.2–Schematic diagram of CA3099E.

General Description of Circuit Operation (Refer to Fig.1)

When the signal-input voltage of the CA3099E is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

The CA3099E comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{bias}) supplied to terminal 2. As an alternative to externally supplied bias current, the CA3099E contains an internal source of regulated bias current accessible at terminal 12. This internal source of bias current is developed by two alternative methods; in the first method, bias voltage (V_b) applied at terminal 9 develops a source of temperature-compensated reference voltage ($\approx V_b/2$) at terminal 11 and additionally supplies a source of bias current at terminal 12 via line "A". Alternately, when a positive supply voltage is applied at terminal 8, a source of constant-current biasing is provided at terminal 12 via line "B".

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 7. The CA3099E contains an on-chip voltage regulator which may optionally be used to regulate the voltages and bias currents (exclusive of the load current at terminal 3) needed for the operation of the IC.

Fig. 2 is the schematic diagram of the CA3099E. Figs. 3 and 4 are, respectively, functional and logic diagrams of CA3099E operation.

CA3099E

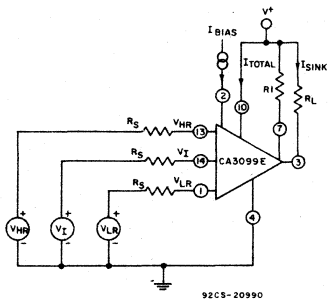


Fig.3—Functional diagram.

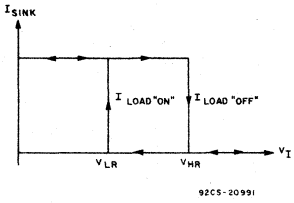


Fig.4—Logic diagram.

TYPICAL CHARACTERISTIC CURVES

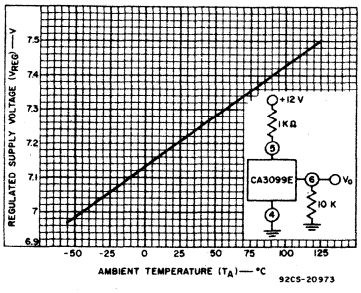


Fig.5—Regulated supply voltage vs. ambient temperature.

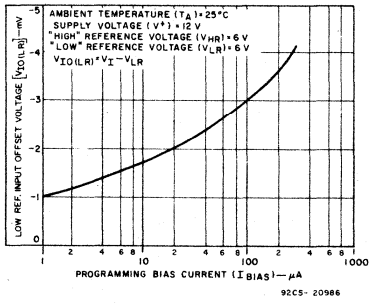


Fig.6—Input-offset voltage ("low" reference) vs. programming bias current.

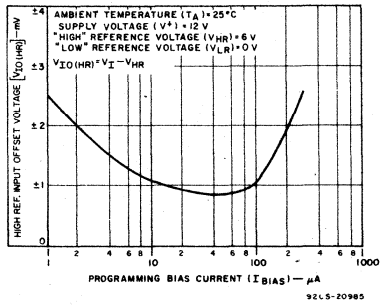


Fig.7—Input-offset voltage ("high" reference) vs. programming bias current.

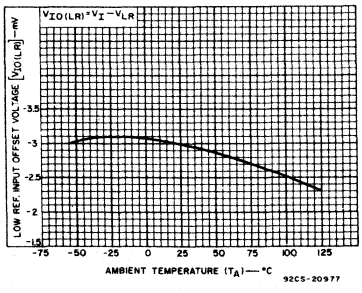


Fig.8—Input-offset voltage ("low" reference) vs. ambient temperature.

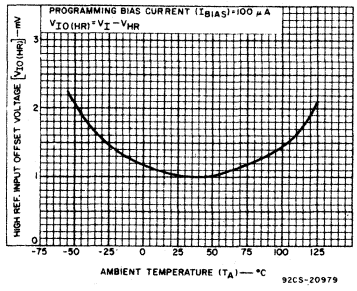


Fig.9—Input-offset voltage ("high" reference) vs. ambient temperature.

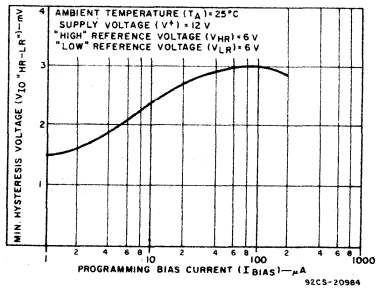


Fig.10—Min. hysteresis voltage vs. programming bias current.

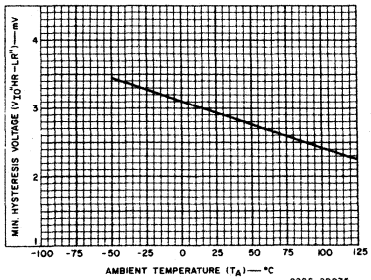


Fig.11—Min. hysteresis voltage vs. ambient temperature.

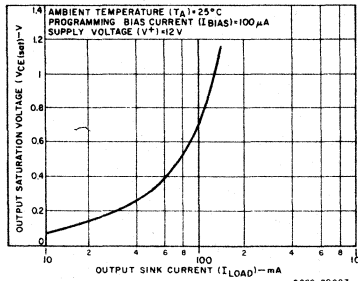


Fig.12—Output saturation voltage vs. output sink current.

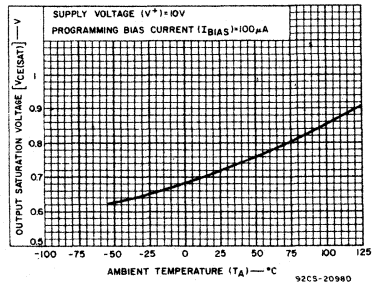


Fig.13—Output saturation voltage vs. ambient temperature.

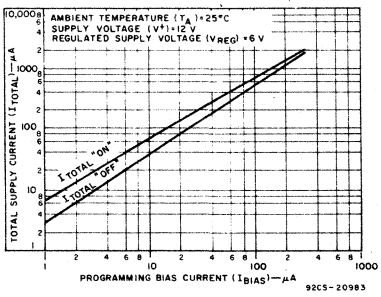


Fig.14—Total supply current vs. programming bias current.

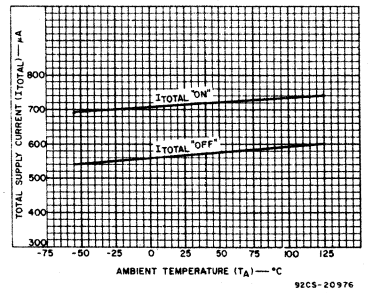


Fig.15—Total supply current vs. ambient temperature.

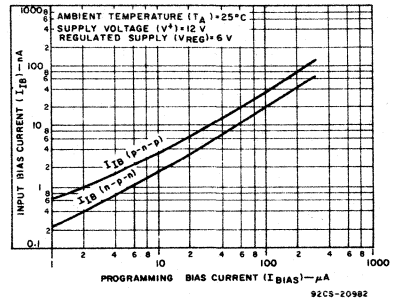


Fig.16—Input bias current vs. programming bias current.

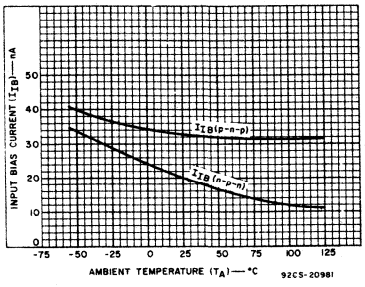


Fig.17—Input bias current vs. ambient temperature.

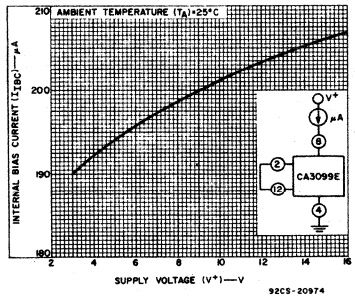


Fig.18—Internal bias current vs. supply voltage.

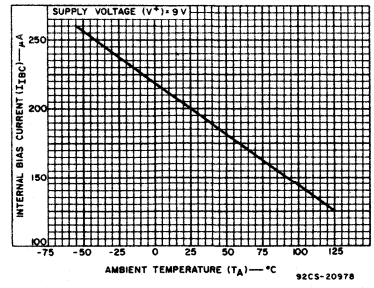


Fig.19—Internal bias current vs. ambient temperature.

TEST CIRCUITS

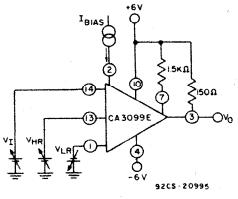


Fig.20—Input-offset voltage test circuit.

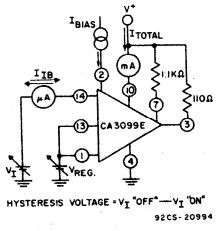


Fig.21—Min. hysteresis voltage, total supply current, and input-bias-current test circuit.

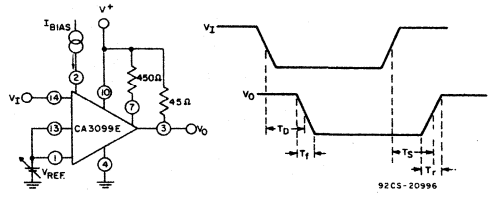


Fig.22—Switching time test circuit.

TYPICAL APPLICATIONS

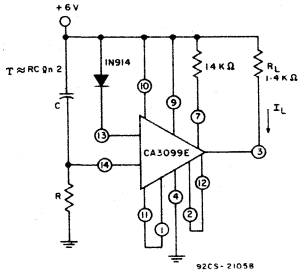


Fig.23(a)—Time delay circuit: Terminal 3 "sinks" after T seconds.

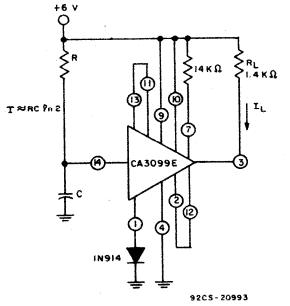


Fig.23(b)—Time delay circuit: "sink" current interrupted after T seconds.

CA3099E

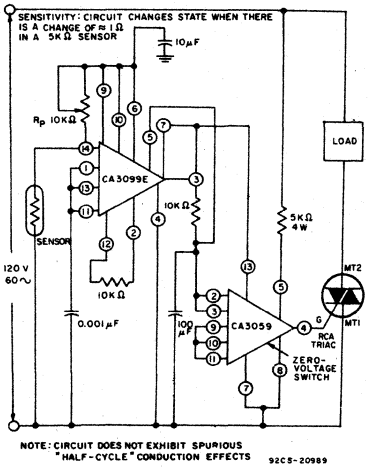


Fig.24—Sensitive temperature control.

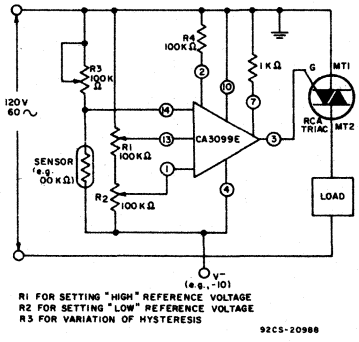


Fig.25—OFF/ON control of triac with programmable hysteresis.

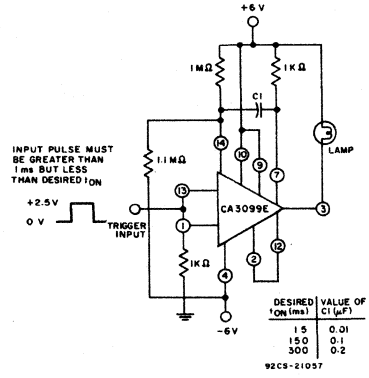


Fig.26—One-shot multivibrator.

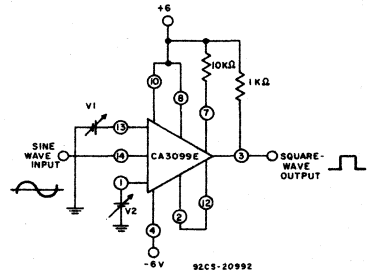
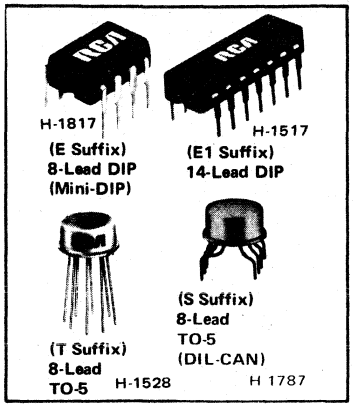


Fig.27—Sine-wave to square-wave converter with duty-cycle adjustment (V_1 and V_2).



BiMOS Dual Voltage Comparators

With MOS/FET Input, Bipolar Output

Features:

- *MOS/FET input stage:*
  - (a) *Very high input impedance (Z_{IN}) - 1.7 TΩ typ.*
  - (b) *Very low input current - 3.5 pA typ. at +5 V supply voltage*
  - (c) *Low input-offset voltage (V_{IO}) - to 6 mV max. (CA3290B)*
  - (d) *Wide common-mode input-voltage range (V_{ICR}) - can be swung 1.5 V (typ.) below negative supply-voltage rail*
  - (e) No phase reversal of output signal for input signals down to 5 V below negative supply-voltage rail
  - (f) *MOS/FET input stage - zener diode protected*
  - (g) *Virtually eliminates errors due to flow of input currents*
- *Wide supply-voltage range:*
  Single supply - 4 to 36 V dc
  Dual supply - $^{+3.5}_{-0.5}$ to ±18 V dc
  (B-types up to 44 or ±22 V dc)
- *Very low supply-current drain - 0.8 mA at +5 V*
- *Differential input-voltage range - up to ±36 V*
- *Low output saturation voltage - 120 mV at 4 mA*
- *Output voltage compatible with TTL, DTL, ECL, MOS, and CMOS logic systems*
- *All types are rated for operation over the range of −55 to +125° C*
- *Stable V_{IO} vs. time due to source-follower inputs*

Applications:

- *High-source-impedance voltage comparators*
- *Long time delay circuits*
- *Square-wave generators*
- *A/D converters*
- *Window comparators*

SELECTION CHART

Selection	Characteristic				Package & Suffix			
					TO-5		Plastic	
	Max. V_{IO} (mV)	Max. I_I (pA)	Min. A_{OL}	V^+ (V)	Std.	DIL-CAN	8-Ld.	14-Ld.
CA3290B	6	30	50K	44	T	S	—	—
CA3290A	10	40	25K	36	T	S	E	E1
CA3290	20	50	25K	36	T	S	E	E1

The CA3290 is also available in chip form (H suffix)

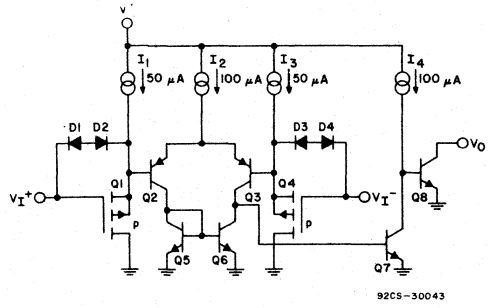


Fig. 1 – Basic CA3290 comparator.

CA3290, CA3290A, CA3290B

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
- Single Supply:
  - CA3290B . . . . . +44 V
  - CA3290A, CA3290 . . . . . +36 V
- Dual Supply:
  - CA3290B . . . . . ±22 V
  - CA3290A, CA3290 . . . . . ±18 V

DIFFERENTIAL INPUT VOLTAGE . . . . . ±36 V or ± [(V^+–V^-)+5 V] (whichever is less)

COMMON-MODE INPUT VOLTAGE . . . . . V^++5 V to V^-–5 V

DEVICE DISSIPATION:
- Up to 55°C . . . . . 630 mW
- Above 55°C . . . . . Derate linearly at 6.67 mW/°C

OUTPUT-TO-V^- SHORT CIRCUIT DURATION* . . . . . CONTINUOUS

TEMPERATURE RANGE, ALL TYPES:
- Operating . . . . . –55 to +125°C
- Storage . . . . . –65 to +150°C

INPUT TERMINAL CURRENT . . . . . 1 mA

LEAD TEMPERATURE (DURING SOLDERING):
- AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX. . . . . 265°C

*Short circuits from the output to V^+ can cause excessive heating and eventual destruction of the device.

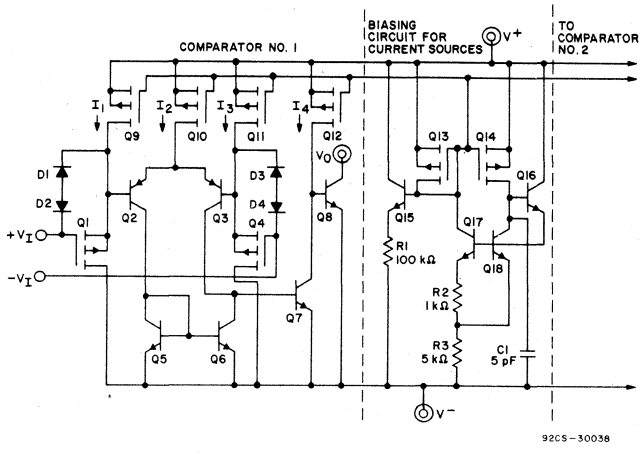


Fig. 2 – Schematic diagram of CA3290 (only one is shown).

CIRCUIT DESCRIPTION

The Basic Comparator

Fig. 1 shows the basic circuit diagram for one of the two comparators in the CA3290. It is generically similar to the industry-type "139" comparators, with PMOS transistors replacing p-n-p transistors as input stage elements. Transistors Q1 through Q4 comprise the differential input stage, with Q5 and Q6 serving as a mirror-connected active load and differential-to-single-ended converter. The differential input at Q1 and Q4 is amplified so as to toggle Q6 in accordance with the input-signal polarity. For example, if $+V_{IN}$ is greater than $-V_{IN}$, Q1, Q2, and current mirror transistors Q5 and Q6 will be turned off; transistors Q3, Q4, and Q7 will be turned on, causing Q8 to be turned off. The output is pulled positive when a load resistor is connected between the output and V^+.

In essence, Q1 and Q4 function as source-followers to drive Q2 and Q3, respectively, with zener diodes D1 through D4 providing gate-oxide protection against input voltage transients (e.g., static electricity). The current flow in Q1 and Q2 is established at approximately 50 microamperes by constant-current sources I_1 and I_3, respectively. Since Q1 and Q4 are operated with a constant current load, their gate-to-source voltage drops will be effectively constant as long as the input voltages are within the common-mode

range. As a result, the input offset voltage ($V_{GS(Q1)} + V_{BE(Q2)} - V_{BE(Q3)} - V_{GS(Q4)}$) will not be degraded when a large differential dc voltage is applied to the device for extended periods of time at high temperatures.

Additional voltage gain following the first stage is provided by transistors Q7 and Q8. The collector of Q8 is open, offering the user a wide variety of options in applications. An additional discrete transistor can be added if it becomes necessary to boost the output sink-current capability.

The detailed schematic diagram for one comparator and the common current-source biasing is shown in Fig. 2. PMOS transistors Q9 through Q12 are the current-source elements identified in Fig. 1 as I_1 through I_4, respectively. Their gate-source potentials (V_{GS}) are supplied by a common bus from the biasing circuit shown in the right-hand portion of the Fig. 2. The currents supplied by Q10 and Q12 are twice those supplied by Q9 and Q11. The transistor geometries are appropriately scaled to provide the requisite currents with common V_{GS} applied to Q9 through Q12.

ELECTRICAL CHARACTERISTICS at T_A = –55 to +125°C

CHARACTERISTIC	TEST CONDITIONS		VALUES						UNITS
			CA3290B		CA3290A		CA3290		
		V^+	Typ.	Max.	Typ.	Max.	Typ.	Max.	
Input Offset Voltage, V_{IO}	V_{CM}=1.4 V, V_O=1.4 V	5 V	3.5	–	4.5	–	8.5	–	mV
	V_{CM}=0 V, V_O=0 V	±15 V	3.5	–	8.5	–	8.5		
Temp. Coefficient of Input Offset Voltage, $\Delta V_{IO}/\Delta T$			8	–	8	–	8	–	µV/°C
Input Offset Current, I_{IO}	V_{CM}=1.4 V	5 V	2	22	2	28	2	32	nA
	V_{CM}=0 V	±15 V	7	22	7	28	7	32	
Input Current, I_I▲	V_{CM}=1.4 V	5 V	2.8	32	2.8	45	2.8	55	nA
	V_{CM}=0 V	±15 V	13	32	13	45	13	55	
Supply Current, I^+*	$R_L = \infty$	5 V	0.85	1.6	0.85	1	0.85	1.6	mA
		30 V	1.62	3.5	1.62	3	1.62	3.5	
Voltage Gain, A_{OL}	R_L=15 kΩ	±15 V	150	–	150	–	150	–	V/mV
			103	–	103	–	103	–	dB
Saturation Voltage I_{SINK} = 4 mA	V^+=5 V, $+V_I$=0 V, $-V_I$=1 V	+125°C	0.22	0.7	0.22	0.7	0.22	0.7	V
		–55°C	0.1	–	0.1	–	0.1	–	
Output Leakage Current, I_{OL}		15 V	65	–	65	–	65	–	nA
		36 V	130	1k	130	1k	130	1k	

▲At T_A = +125°C
*At T_A = –55°C

CA3290, CA3290A, CA3290B

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

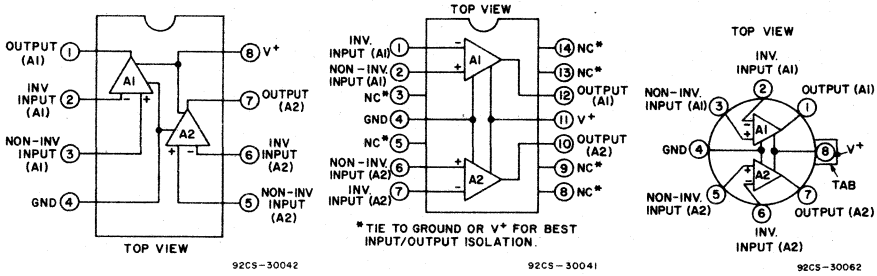
CHARACTERISTIC	TEST COND. V^+	LIMITS						UNITS
		CA3290B			CA3290A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, V_{IO} V_{CM}=1.4 V, V_O=1.4 V	5 V	–	3	6	–	4	10	mV
V_{CM}=0 V, V_O=0 V	±15 V	–	3	6	–	4	10	mV
Input Current, I_I V_{CM}=1.4 V	5 V	–	3.5	30	–	3.5	40	pA
V_{CM}=0 V	±15 V	–	12	30	–	12	40	pA
Input Offset Current, I_{IO} V_{CM}=1.4 V	5 V	–	2	20	–	2	25	pA
V_{CM}=0 V	±15 V	–	7	20	–	7	25	pA
Common-Mode Input-Voltage Range, V_{ICR} V_O=1.4 V	5 V	V^+–3.5 to V^-	V^+–3.1 to V^-–1.5	–	V^+–3.5 to V^-	V^+–3.1 to V^-–1.5	–	V
V_O=0 V	±15 V	V^+–3.8 to V^-	V^+–3.4 to V^-–1.6	–	V^+–3.8 to V^-	V^+–3.4 to V^-–1.6	–	V
Supply Current, I^+ R_L = ∞	30 V	–	1.35	3	–	1.35	3	mA
	5 V	–	0.8	1.4	–	0.8	1.4	mA
Voltage Gain, A_{OL} R_L=15 kΩ	±15 V	50	800	–	25	800	–	V/mV
		94	118	–	88	118	–	dB
Output Sink Current V_O=1.4 V	5 V	6	30	–	6	30	–	mA
Saturation Voltage $+V_I$=0 V, $-V_I$=1 V, I_{SINK} = 4 mA	5 V	–	0.12	0.4	–	0.12	0.4	V
Output Leakage Current, I_{OL}	15 V	–	100	–	–	100	–	pA
	36 V	–	500	–	–	500	–	pA
Response Time R_L=5.1 kΩ Rising Edge	15 V	–	1.2	–	–	1.2	–	μs
Falling Edge		–	200	–	–	200	–	ns
Common-Mode Rejection Ratio, CMRR	±15 V	–	44	316	–	44	562	μV/V
	5 V	–	100	316	–	100	562	μV/V
Power-Supply Rejection Ratio, PSRR	±15 V	–	15	316	–	15	316	μV/V
Large-Signal Response Time R_L=5.1 kΩ	15 V	–	500	–	–	500	–	ns
	5 V	–	400	–	–	400	–	ns

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$

CHARACTERISTIC	TEST COND. V^+	LIMITS CA3290 Min.	LIMITS CA3290 Typ.	LIMITS CA3290 Max.	UNITS
Input Offset Voltage, V_{IO} V_{CM}=1.4 V, V_O=1.4 V	5 V	–	7.5	20	mV
V_{CM}=0 V, V_O=0 V	±15 V	–	7.5	20	mV
Input Current, I_I V_{CM}=1.4 V	5 V	–	3.5	50	pA
V_{CM}=0 V	±15 V	–	12	50	pA
Input Offset Current, I_{IO} V_{CM}=1.4 V	5 V	–	2	30	pA
V_{CM}=0 V	±15 V	–	7	30	pA
Common-Mode Input-Voltage Range, V_{ICR} V_O=1.4 V	5 V	V^+–3.5 V^-	V^+–3.1 V^-–1.5	–	V
V_O=0 V	±15 V	V^+–3.8 V^-	V^+–3.4 V^-–1.6	–	V
Supply Current, I^+ $R_L = \infty$	30 V	–	1.35	3	mA
	5 V	–	0.8	1.4	mA
Voltage Gain, A_{OL} R_L = 15 kΩ	±15 V	25	800	–	V/mV
		88	118	–	dB
Output Sink Current V_O=1.4 V	5 V	6	30	–	mA
Saturation Voltage $+V_I$=0 V, $-V_I$=1 V, I_{SINK} = 4 mA	5 V	–	0.12	0.4	V
Output Leakage Current, I_{OL}	15 V	–	100	–	pA
	36 V	–	500	–	pA
Response Time R_L=5.1 kΩ Rising Edge	15 V	–	1.2	–	μs
Falling Edge		–	200	–	ns
Common-Mode Rejection Ratio, CMRR	±15 V	–	44	562	μV/V
	5 V	–	100	562	μV/V
Power-Supply Rejection Ratio, PSRR	±15 V	–	15	316	μV/V
Large-Signal Response Time R_L=5.1 kΩ	15 V	–	500	–	ns
	5 V	–	400	–	ns

CA3290, CA3290A, CA3290B

TERMINAL ASSIGNMENTS



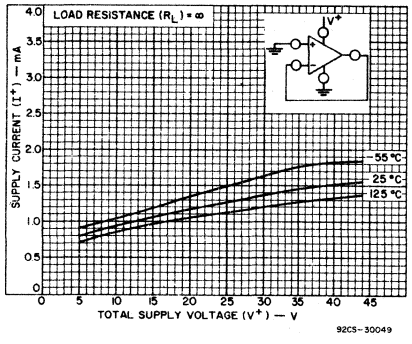


Fig. 3 — Supply current as a function of supply voltage (both amplifiers).

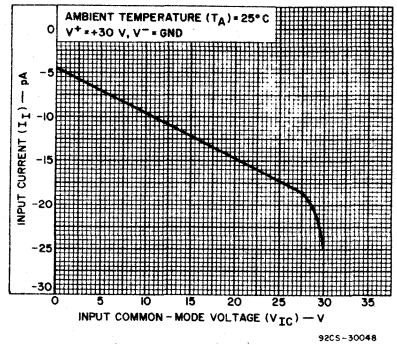


Fig. 4 — Input current as a function of input common-mode voltage.

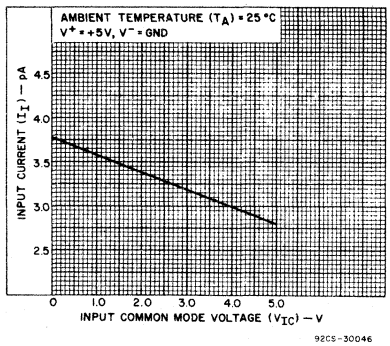


Fig. 5 — Input current as a function of input common-mode voltage.

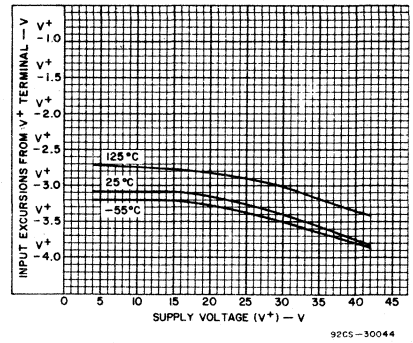


Fig. 6 — Positive common-mode input voltage range as a function of supply voltage.

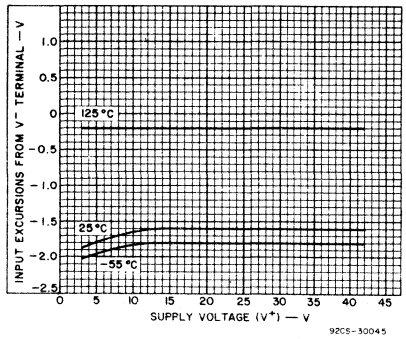


Fig. 7 — Negative common-mode input voltage range as a function of supply voltage.

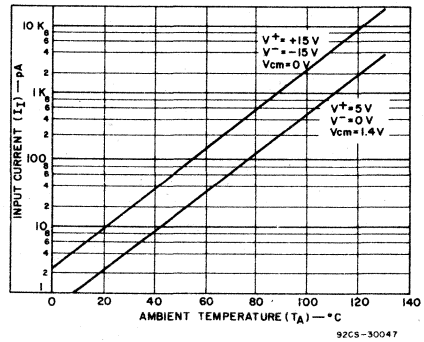


Fig. 8 — Input current as a function of ambient temperature.

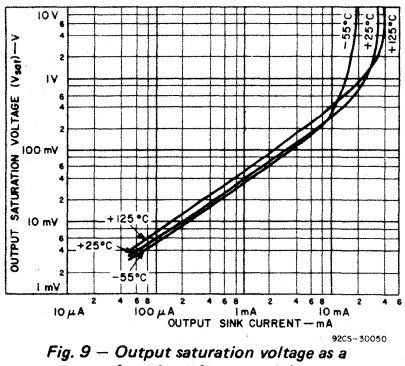


Fig. 9 – Output saturation voltage as a function of output sink current.

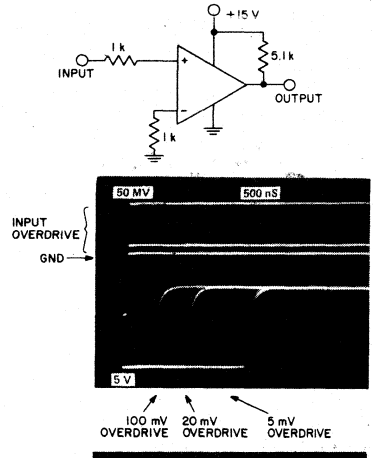
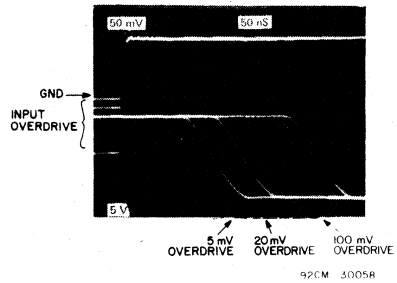
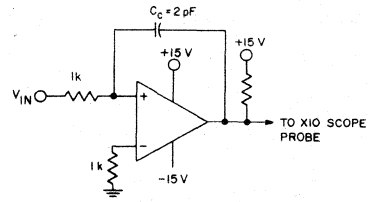
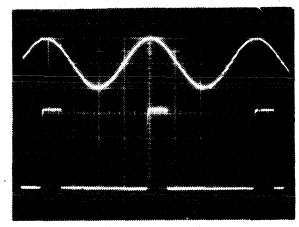


Fig. 11 – Non-inverting comparator response-time test circuit and waveforms.

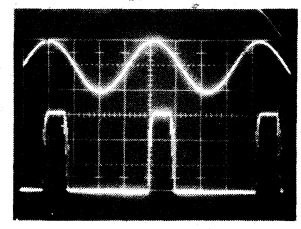






WITH C_C

TOP TRACE ≈ 4.5 mV/DIV = V_{IN}
BOTTOM TRACE = 10 V/DIV = V_{OUT}
H = 5 μs/DIV

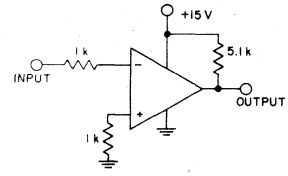


WITHOUT C_C

TOP TRACE ≈ 4.5 mV/DIV
BOTTOM TRACE = 10 V/DIV
H = 5 μs/DIV

92CM-30059R1

Fig. 10 – Parasitic-oscillations test circuit and associated waveforms.



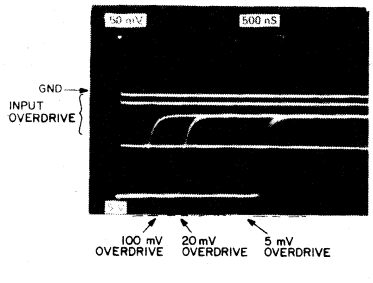


Fig. 12 – Inverting comparator response-time test circuit and waveforms.

OPERATING CONSIDERATIONS

Input Circuit

The use of MOS transistors in the input stage of the CA3290 series circuits provides the user with the following features for comparator applications:

1. Ultra-high input impedance ($\cong 1.7\ T\Omega$);
2. The availability of common-mode rejection for input signals at potentials below that of the negative power-supply rail;
3. Retention of the in-phase relationship of the input and output signals for input signals below the negative rail.

Although the CA3290 employs rugged bipolar (zener) diodes for protection of the input circuit, the input-terminal currents should not exceed 1 mA. Appropriate series-connected limiting resistors should be used in circuits where greater current flows might exist, allowing the signal input voltage to be greater than the supply voltage without damaging the circuit.

Output Circuit

The output of the CA3290 is the open collector of an n-p-n transistor, a feature providing flexibility in a broad range of comparator applications. An output ORing function can be implemented by parallel-connection of the open collectors. An output pull-up resistor can be connected to a power supply having a voltage range within the rating of the particular CA3290 in use; the magnitude of this voltage may be set at a value which is independent of that applied to the V^+ terminal of the CA3290.

Parasitic Oscillations

The ideal comparator has, among other features, ultra-high input impedance, high gain, and wide bandwidth. These desirable characteristics may, however, produce parasitic oscillations unless certain precautions are observed to minimize the stray capacitive coupling between the input and output terminals. Parasitic oscillations manifest themselves during the output voltage transition intervals as the comparator switches states. For high source impedances, stray capacitance can induce parasitic oscillations. The addition of a small amount (1 to 10 mV) of positive feedback (hysteresis) produces a faster transition, thereby reducing the likelihood of parasitic oscillations. Furthermore, if the input signal is a pulse waveform, with relatively rapid rise and fall times, parasitic tendencies are reduced.

When dual comparators, like the CA3290, are packaged in an 8-lead configuration, the output terminal of each comparator is adjacent to an input terminal. The lead-to-lead capacitance is approximately 1 pF, which may be sufficient to cause undesirable feedback effects in certain applications. Circuit factors such as impedance levels, supply voltage, toggling rate, etc., may increase the possibility of parasitic oscillations. To minimize this potential oscillatory condition, it is recommended that for source impedances greater than 1 $k\Omega$ a capacitor ($\geqslant$ 1-2 pF) be connected between the appropriate input terminal and the output terminal. (See Fig. 10.)

The CA3290A and CA3290 are also supplied in a 14-lead dual-in-line plastic package. To minimize the possibility of parasitic oscillations the input and output terminals are positioned on opposite sides of the package. In addition, there are two leads between the output terminal of each comparator and its corresponding inverting input terminal, reducing the input/output coupling significantly. These leads (8, 9, 13, 14) should be tied to either the V^+ or V^- supply rail. If either comparator is unused, its input terminals should also be tied to either the V^+ or V^- supply rail.

TYPICAL APPLICATIONS

Light-Controlled One-Shot Timer

In Fig. 13 one comparator (A1) of the CA3290 is used to sense a change in photo diode current. The other comparator (A2) is configured as a one-shot timer and is triggered by the output of A1. The output of the circuit will switch to a low state for approximately 60 seconds after the light source to the photo diode has been interrupted. The circuit operates at normal room lighting levels. The sensitivity of the circuit may be adjusted by changing the values of R1 and R2. The ratio of R1 to R2 should be constant to insure constant reverse voltage bias on the photo diode.

Low-Frequency Multivibrator

In this application, one-half of the CA3290 is used as a conventional multivibrator circuit. Because of the extremely high input impedance of this device, large values of timing resistor (R1) may be used for long time delays with relatively small leakage timing capacitors. The second half of the CA3290 is used as an output buffer to insure that the multivibrator frequency will not be affected by output loading.

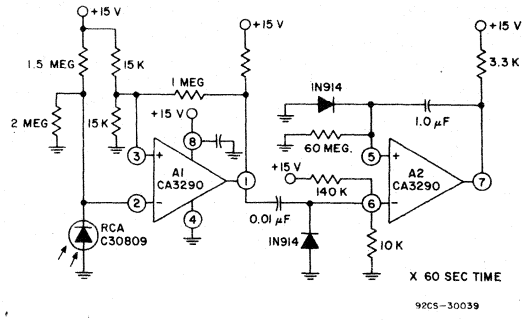


Fig. 13 – Light-controlled one-shot timer.

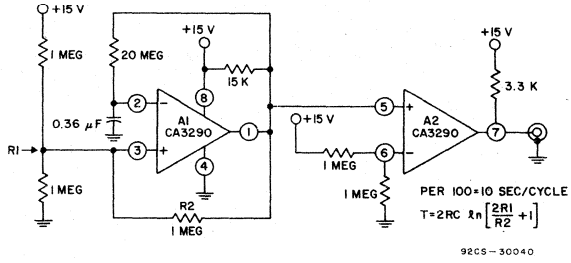


Fig. 14 – Low-frequency multivibrator.

Window Comparator

Both halves of the CA3290 can be used in a high input-impedance window comparator as shown in Fig. 15. The LED will be turned "on" whenever the input signal is above the lower limit (V_L) but below the upper limit (V_U), as determined by the R1/R2/R3 resistor divider.

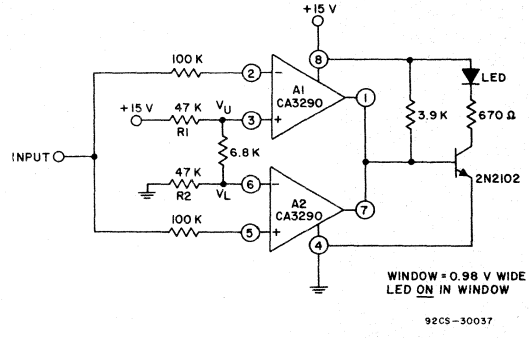


Fig. 15 – Window comparator.

CA3290, CA3290A, CA3290B

LED Bar Graph Driver

The circuit in Fig. 16 demonstrates the use of the CA3290 in a bar graph display. The non-inverting inputs of both comparators are tied to the voltage divider reference and the input signal is applied to both of the inverting inputs. The LED for a particular comparator will be turned "on" when the input voltage reaches the voltage on the resistor divider reference. The CA3290 is ideal for this application where input-signal loading is critical even though many comparator inputs are driven in parallel.

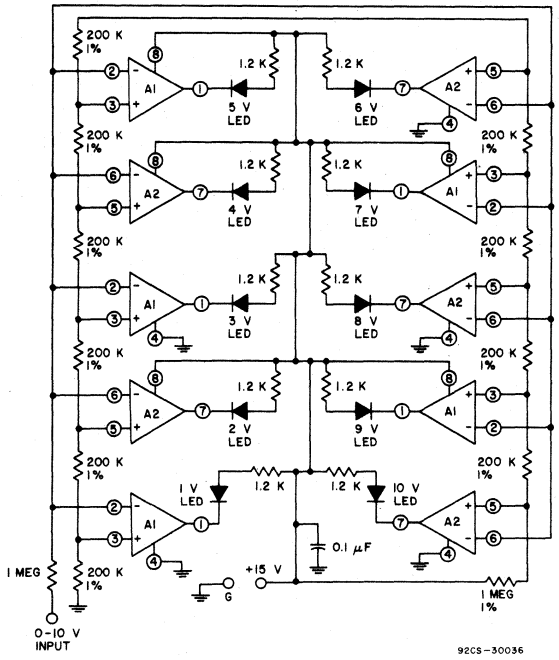
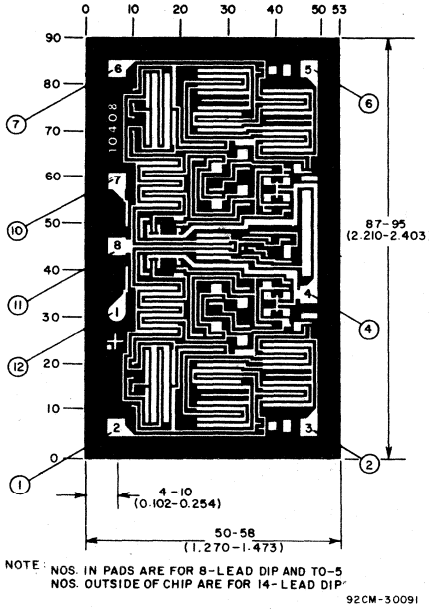


Fig. 16 – LED bar-graph driver.

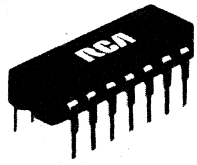


Dimensions and pad layout for the CA3290H.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA139, CA239, CA339 Types



14-Lead Dual-In-Line
"E" Suffix — Standard
Plastic Package

H-1517

Quad Voltage Comparators

For Industrial, Commerical, and Military Applications

"E" Suffix Types — Standard Dual-In-Line Plastic Package

Features:

- *Operation from single or dual supplies*
- *Common-mode input-voltage range to ground*
- *Output voltage compatible with TTL, DTL, ECL, MOS and CMOS*
- *Differential input-voltage range equal to the supply voltage*
- *Maximum input-offset voltage (V_{IO}):*
  CA139A, CA239A, CA339A - 2 mV
  CA139, CA239, CA339 - 5 mV
- *Replacement for industry types 139, 239, 339, 139A, 239A, and 339A*

The RCA-CA139, CA239, CA339, CA139A, CA239A, and CA339A types consist of four independent single- or dual-supply voltage comparators on a single monolithic substrate. The common-mode input voltage range includes ground even when operated from a single supply, and the low power supply current drain makes these comparators suitable for battery operation. These types were designed to directly interface with TTL and CMOS.

Types CA139A, CA239A, and CA339A have all the features and characteristics of their prototype counter parts CA139, CA239, and CA339 plus an even lower input-offset-voltage characteristic. These devices are supplied in a 14-lead dual-in-line plastic package (E suffix). The CA339 is also available in chip form (H suffix).

Applications:

- *Square-wave generators*
- *Time-delay generators*
- *Pulse generators*
- *Multivibrators*
- *High-voltage digital logic gates*
- *A/D converters*
- *MOS clock timers*

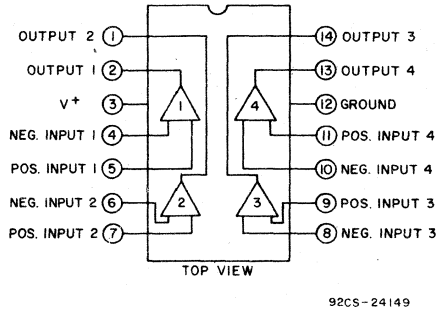


Fig. 1 - Functional diagram.

CA139, CA239, CA339 Types

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^oC$*:*

DC SUPPLY VOLTAGE	36 V or ±18 V
DC DIFFERENTIAL INPUT VOLTAGE	±36 V
INPUT VOLTAGE	−0.3 V to +36 V
INPUT CURRENT ($V_I < -0.3$ V)*	50 mA
OUTPUT SHORT CIRCUIT TO GROUND▲	
(Single Supply)	Continuous
DEVICE DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

* Inputs must not go more negative than −0.3 V.

▲Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current independent of V^+ is approximately 20 mA.

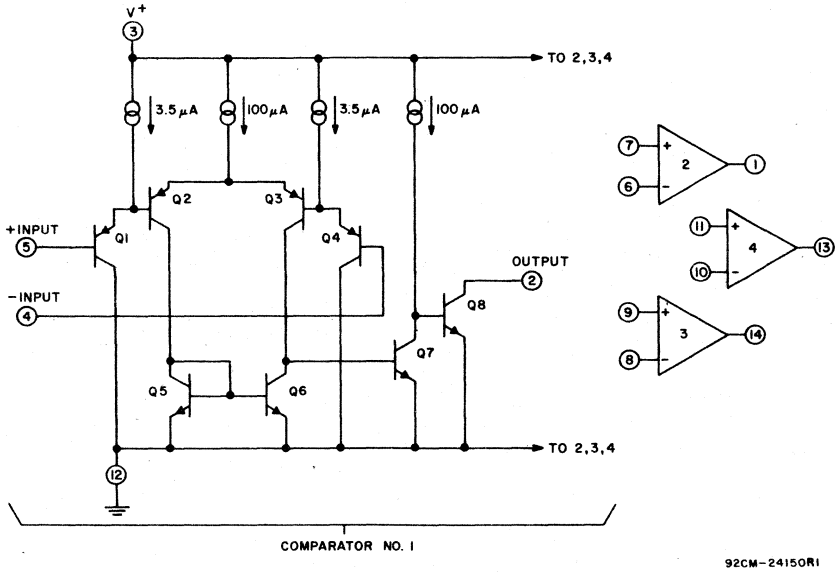


Fig. 2—Schematic diagram.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS ($V^+ = 5$ V Unless otherwise indicated)		LIMITS						UNITS
			CA139			CA139A			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage (V_{IO}) At Output Switch Point $V \cong 1.4$ V	V_{REF} = 1.4 V, $R_S = 0$	25°C	–	2	5	–	1	2	mV
		Note 1	–	–	9	–	–	4	
Differential Input Voltage (V_{ID})	Keep all inputs ≥0 V for V^- (If used), Notes 1, 2		–	–	36	–	–	36	V
Saturation Voltage (V_{sat})	$V_I^- = 1$ V, $V_I^+ = 0$ V, $I_{SINK} \leq$ 4 mA	25°C	–	250	400	–	250	400	mV
		Note 1	–	–	700	–	–	700	
Common-Mode Input Voltage Range (V_{ICR})	Note 3	25°C	0	–	$V^+-1.5$	0	–	$V^+-1.5$	V
		Note 1	0	–	V^+-2	0	–	V^+-2	
Input Offset Current (I_{IO})	$I_I^+ - I_I^-$	25°C	–	3	25	–	3	25	nA
		Note 1	–	–	100	–	–	100	
Input Bias Current (I_{IB})	I_I^+ or I_I^- with Output in Linear Range	25°C	–	25	100	–	25	100	nA
		Note 1	–	–	300	–	–	300	
Supply Current (I^+)	$R_L = \infty$ on all comparators, T_A = 25°C		–	0.8	2	–	0.8	2	mA
Output Leakage Current	$V_I^+ \geq 1$ V, $V_I^- = 0$, $V_O = 5$ V	25°C	–	0.1	–	–	0.1	–	nA
	$V_I^+ \geq 1$ V, $V_I^- = 0$, $V_O = 30$ V	Note 1	–	–	1	–	–	1	μA
Output Sink Current	$V_I^- \geq 1$ V, $V_I^+ = 0$, $V_O \leq +1.5$ V, T_A = 25°C		6	16	–	6	16	–	mA
Voltage Gain (A_{OL})	$R_L \geq 15$ kΩ, $V^+ = 15$ V, T_A = 25°C		–	200	–	50	200	–	V/mV
Large Signal Response Time	V_I = TTL Logic Swing, V_{REF} = +1.4 V, $V_{RL} = 50$ V, $R_L = 5.1$ kΩ, T_A = 25°C		–	300	–	–	300	–	ns
Response Time See Figs. 5 & 6	$V_{RL} = 5$ V, $R_L = 5.1$ kΩ, T_A = 25°C		–	1.3	–	–	1.3	–	μs

Note 1: Ambient Temperature (T_A) applicable over operating temperature range as shown below.

CA139 / CA139A (–55 to +125°C) | CA239 / CA239A (–25 to +85°C) | CA339 / CA339A (0 to +70°C)

Note 2: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than –0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

Note 3: The upper end of the common-mode voltage range is (V^+) – 1.5 V, but either or both inputs can go to +30 V without damage.

CA139, CA239, CA339 Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS (V^+ = 5 V, Unless otherwise indicated)		CA239, CA339 Min.	CA239, CA339 Typ.	CA239, CA339 Max.	CA239A, CA339A Min.	CA239A, CA339A Typ.	CA239A, CA339A Max.	UNITS
Input Offset Voltage (V_{IO}) At Output Switch Point V ≅ 1.4 V	V_{REF} = 1.4 V, R_S = 0	25°C	–	2	5	–	1	2	mV
		Note 1	–	–	9	–	–	4	
Differential Input Voltage (V_{ID})	Keep all inputs ≥0 V for V^- (If used), Notes 1, 2		–	–	36	–	–	36	V
Saturation Voltage (V_{sat})	V_I^- = 1 V, V_I^+ = 0 V, I_{SINK} ≤ 4 mA	25°C	–	250	400	–	250	400	mV
		Note 1	–	–	700	–	–	700	
Common-Mode Input Voltage Range (V_{ICR})	Note 3	25°C	0	–	V^+–1.5	0	–	V^+–1.5	V
		Note 1	0	–	V^+–2	0	–	V^+–2	
Input Offset Current (I_{IO})	$I_I^+ - I_I^-$	25°C	–	5	50	–	5	50	nA
		Note 1	–	–	150	–	–	150	
Input Bias Current (I_{IB})	I_I^+ or I_I^- with Output in Linear Range	25°C	–	25	250	–	25	250	nA
		Note 1	–	–	400	–	–	400	
Supply Current (I^+)	R_L = ∞ on all comparators, T_A = 25°C		–	0.8	2	–	0.8	2	mA
Output Leakage Current	V_I^+ ≥1 V, V_I^- = 0, V_O = 5 V	25°C	–	0.1	–	–	0.1	–	nA
	V_I^+ ≥1 V, V_I^- = 0, V_O = 30 V	Note 1	–	–	1	–	–	1	μA
Output Sink Current	V_I^- ≥1 V, V_I^+ = 0, V_O ≤+1.5 V, T_A = 25°C		6	16	–	6	16	–	mA
Voltage Gain (A_{OL})	R_L ≥15 kΩ, V^+=15 V, T_A = 25°C		–	200	–	50	200	–	V/mV
Large Signal Response Time	V_I = TTL Logic Swing, V_{REF} = +1.4 V, V_{RL} = 50 V, R_L = 5.1 kΩ, T_A = 25°C		–	300	–	–	300	–	ns
Response Time See Figs. 5 & 6	V_{RL} = 5 V, R_L = 5.1 kΩ, T_A = 25°C		–	1.3	–	–	1.3	–	μs

Note 1: Ambient Temperature (T_A) applicable over operating temperature range as shown below.
CA139, CA139A (–55 to +125°C) CA239, CA239A (–25 to +85°C) CA339, CA339A (0 to +70°C)

Note 2: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than –0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

Note 3: The upper end of the common-mode voltage range is (V^+) – 1.5 V, but either or both inputs can go to +30 V without damage.

TYPICAL CHARACTERISTICS

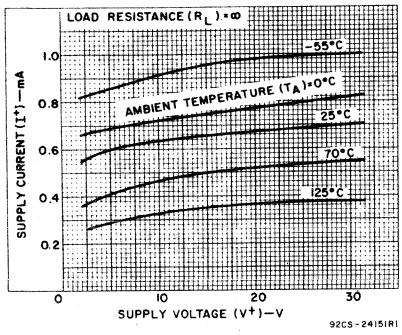


Fig. 3—Supply current vs. supply voltage.

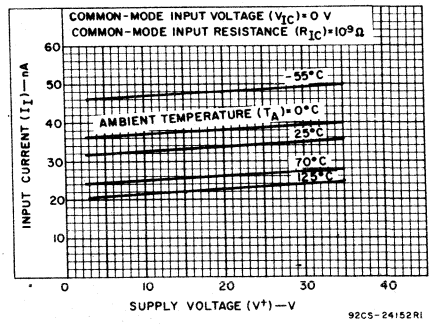


Fig. 4—Input current vs. supply voltage.

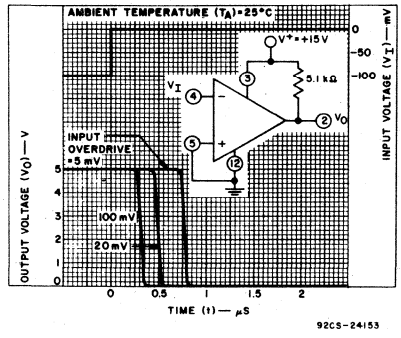


Fig. 5—Response time for various input overdrives—negative transition.

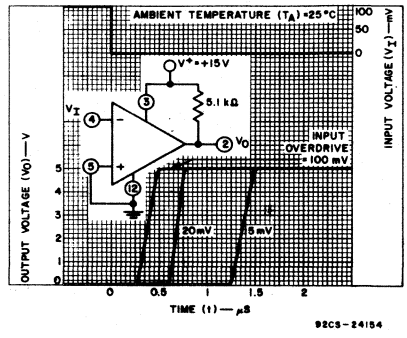


Fig. 6—Response time for various input overdrives—positive transition.

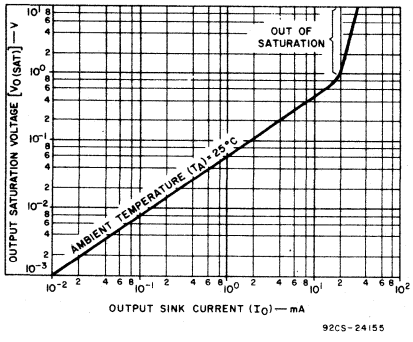
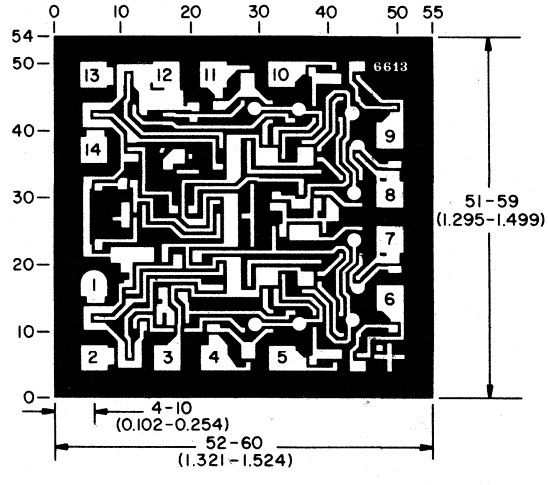


Fig. 7—Output saturation voltage vs. output sink current.

Chip Version (CA339H)



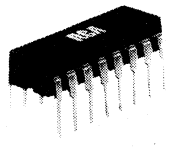
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Data Conversion Circuits
Technical Data

4

*BiMOS types

CA3162E



16-Lead Dual-In-Line Plastic Package

H-1622

A/D Converter for 3-Digit Display

Features:

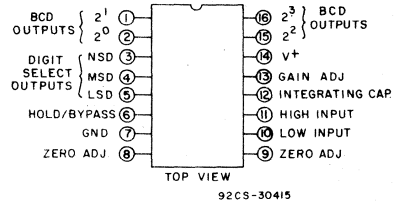
- *Dual-slope A/D conversion*
- *Multiplexed BCD display*
- *Ultra-stable internal band-gap voltage reference*
- *Capable of reading 99 mV below ground with single supply*
- *Differential input*
- *Internal timing - no external clock required*
- *Choice of low-speed [4-Hz] or high-speed [96-Hz] conversion rate*
- *"Hold" inhibits conversion but maintains delay*
- *Overrange indication - "EEE" for reading greater than + 999 mV, "-" for reading more negative than -99 mV when used with CA3161E BCD-to-Seven Segment Decoder/Driver*

The CA3162E is an I^2L monolithic A/D converter that provides a 3-digit multiplexed BCD output. It is used with the CA3161E BCD-to-Seven-Segment Decoder/Driver* and a minimum of external parts to implement a complete 3-digit display.

The CA3162 is supplied in 16-lead dual-in-line plastic package (E suffix). The CA3162 is also available in chip form (H suffix).

*The CA3161E is described in RCA data bulletin File No. 1079.

TERMINAL ASSIGNMENT
CA3162E



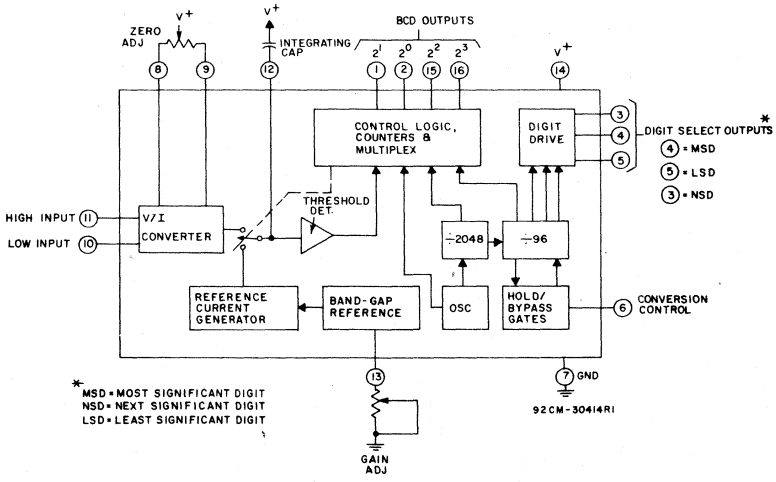


Fig. 1 — Functional block diagram of the CA3162E.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (between terminals 7 and 14) ..... +7 V
INPUT VOLTAGE (terminal 10 or 11 to ground) ..... ±15 V
DEVICE DISSIPATION:
Up to T_A = +55°C ..... 750 mW
Above T_A = +55°C ..... derate linearly at 7.9 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating ..... 0 to +75°C
Storage ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 5 V, Zero pot centered, gain pot = 2.4 kΩ unless otherwise stated

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Operating Supply Voltage Range, V^+		4.5	5	5.5	V
Supply Current, I^+	100 kΩ to V^+ on terms. 3,4,5	—	—	17	mA
Input Impedance, Z_I		—	100	—	MΩ
Input Bias Current, I_{IB}	Terms. 10 and 11	—	−80	—	nA
Unadjusted Zero Offset	$V_{11} - V_{10}$ = 0 V, read decoded output	−12	—	+12	mV
Unadjusted Gain	$V_{11} - V_{10}$ = 900 mV, read decoded output	846	—	954	mV
Linearity	See Notes 1 and 2	−1	—	+1	Count
Conversion Rate: Slow Mode	Term. 6 = open or gnd	—	4	—	Hz
Fast Mode	Term. 6 = 5 V	—	96	—	Hz
Conversion Control Voltage (Hold Mode) at Terminal 6		0.8	1.2	1.6	V
Common-Mode Input Voltage Range, V_{ICR}	See Note 3, 4	−0.2	—	+0.2	V
BCD Sink Current at terms. 1,2,15,16	$V_{BCD} \geq$ 0.5 V, at logic zero state	0.4	1.6	—	mA
Digit Select Sink Current at terms. 3,4,5	$V_{Digit\ Select}$ = 4 V at logic zero state	1.6	2.5	—	mA
Zero Temperature Coefficient	V_I = 0 V, zero pot centered	—	10	—	μV/°V
Gain Temperature Coefficient	V_I = 900 mV, gain pot = 2.4 kΩ	—	0.005	—	%/°C

Notes:

1. Apply zero volts across V_{11} to V_{10}. Adjust zero potentiometer to give 000 mV reading. Apply 900 mV to input and adjust gain potentiometer to give 900 mV reading.
2. Linearity is measured as a difference from a straight line drawn through zero and positive full scale. Limits do not include ±0.5 count bit digitizing error.
3. For applications where negative terminal 10 is not operated at terminal 7 potential, a return path of not more than 100 kΩ resistance must be provided for input bias currents.
4. The common-mode input voltage above ground cannot exceed +0.2 V if the full input signal range of 999 mV is required at terminal 11. That is, terminal 11 may not operate higher than 1.2 V positive with respect to ground or 0.2 V negative with respect to ground. If the maximum input signal is less than 999 mV, the common-mode input voltage may be raised accordingly.

CA3162E

Circuit Description

The functional block diagram of the CA3162E is shown in Fig. 1. The heart of the system is the V/I converter and reference-current generator. The V/I converter converts the input voltage applied between terminals 10 and 11 to a current that charges the integrating capacitor on terminal 12 for a predetermined time interval. At the end of the charging interval, the V/I converter is disconnected from the integrating capacitor, and a band-gap reference constant-current source of opposite polarity is connected. The number of clock counts that elapse before the charge is restored to its original value is a direct measure of the signal induced current. The restoration is sensed by the comparator, which in turn latches the counter. The count is then multiplexed to the BCD outputs.

The timing for the CA3162E is supplied by a 786-Hz ring oscillator, and the input at terminal 6 determines the sampling rate. A 5-V input provides a high-speed sampling rate (96 Hz), and grounding or floating terminal 6 provides a low-speed (4 Hz) sampling rate. When terminal 6 is fixed at +1.2 V (by placing a 12 K resistor between terminal 6 and the +5-V supply) a "hold" feature is available. While the CA3162E is in the hold mode, sampling continues at 4 Hz but the display data are latched to the last reading prior to the application of the 1.2 V. Removal of the 1.2 V restores continuous display changes. Note, however, that the sampling rate remains at 4 Hz.

Fig. 3 shows the timing of sampling and digit select pulses for the high-speed mode. Note that the basic A/D conversion process requires approximately 5 ms in both modes.

The "EEE" or "---" displays indicate that the range of the system has been exceeded in the positive or negative direction, respectively. Negative voltages to −99 mV are displayed with the minus sign in the MSD. The BCD code is 1010 for a negative overrange (---) and 1011 for a positive overrange (EEE).

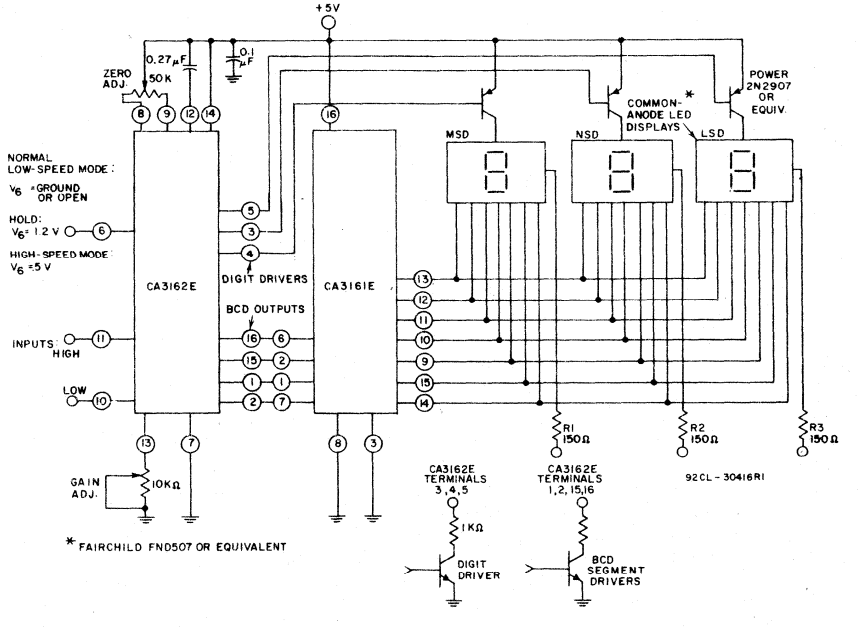


Fig. 2—Basic digital readout system using the CA3162E and the CA3161E.

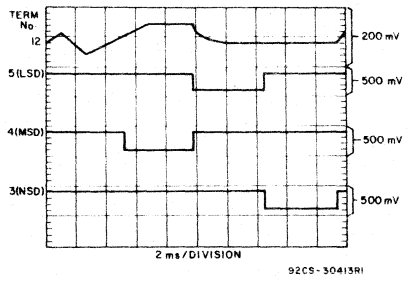


Fig. 3—High speed mode timing diagram.

CA3162E Liquid Crystal Display (LCD) Application

Fig. 4 shows the CA3162E in a typical LCD application. LCD's may be used in favor of LED displays in applications requiring lower power dissipation, such as battery-operated equipment, or when visibility in high-ambient-light conditions is desired.

Multiplexing of LCD digits is not practical, since LCD's must be driven by an ac signal and the average voltage across each segment is zero. Three CD4056B liquid-crystal decoder/drivers are therefore used. Each CD4056B contains an input latch so that the BCD data for each digit may be latched into the decoder. using the inverted digit-select outputs of the CA3162E as strobes.

Inverters G1 and G2 are used as an astable multivibrator to provide the ac drive to the LCD backplane. Inverters G3, G4, and G5 are the digit-select inverters

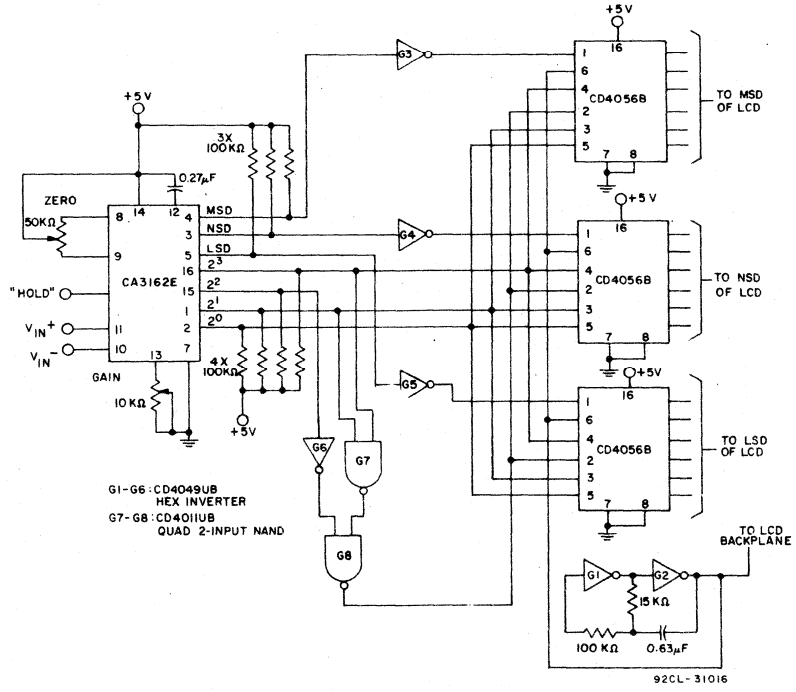


Fig. 4—Typical LCD application.

and require pull-up resistors to interface the open-collector outputs of the CA3162E to COS/MOS logic. The BCD outputs of the CA3162E may be connected directly to the corresponding CD4056B inputs (using pull-up resistors). In this arrangement, the CD4056B decodes the negative sign (—) as an "L" and the positive overlaod indicator (E) as an "H".

CA3162E Common-Cathode, LED Display Application

Fig. 5 shows the CA3162E connected to a CD4511B decode/driver to operate a common-cathode LED display. Unlike the CA3161E, the CD4511B remains blank for all BCD codes greater than nine. After 999 mV the display blanks rather than displaying EEE, as with the CA3161E. When displaying negative voltage, the first digit remains blank instead of (—), and during a negative or positive overrange the display blanks.

The additional logic shown within the dotted area of Fig. 5 restores the negative sign (—), allowing the display of negative numbers as low as —99 mV. Negative overrange is indicated by a negative sign (—) in the MSD position. The rest of the display is blanked. During a positive overrange, only segment b of the MSD is displayed. One inverter from the CD4049B is used to operate the decimal points. By connecting the inverter input to either the MSD or NSD line either DP1 or DP2 will be displayed. Fig. 7 shows the P.C. board and component placement.

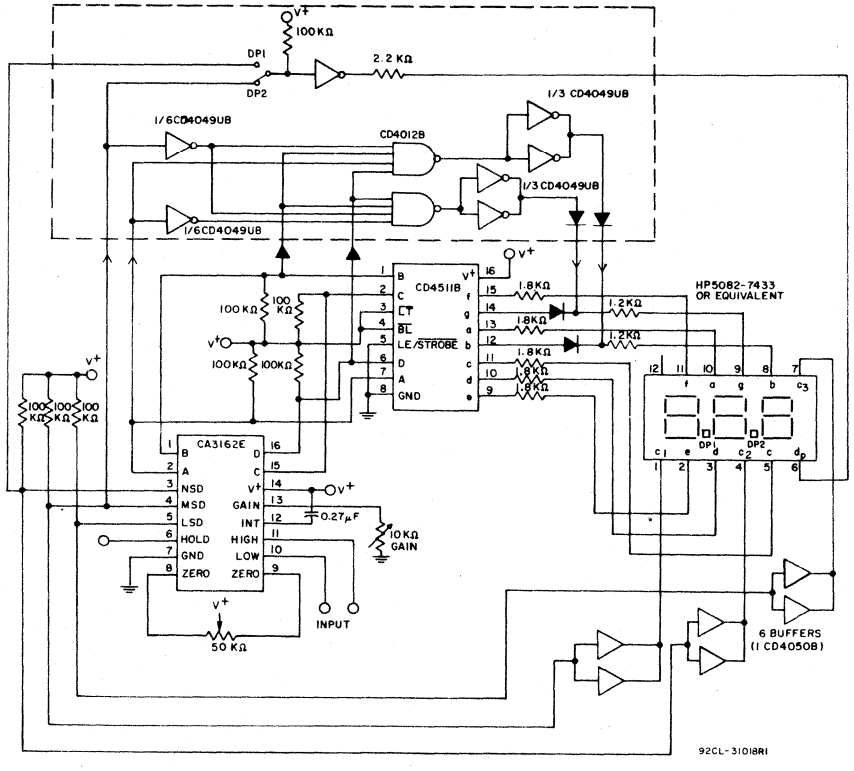
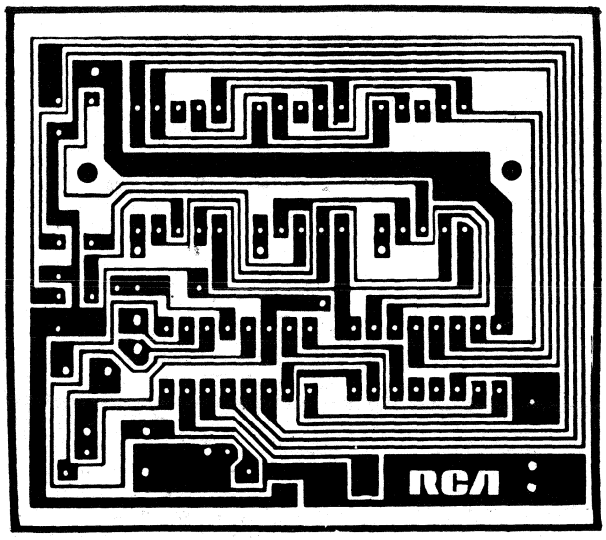
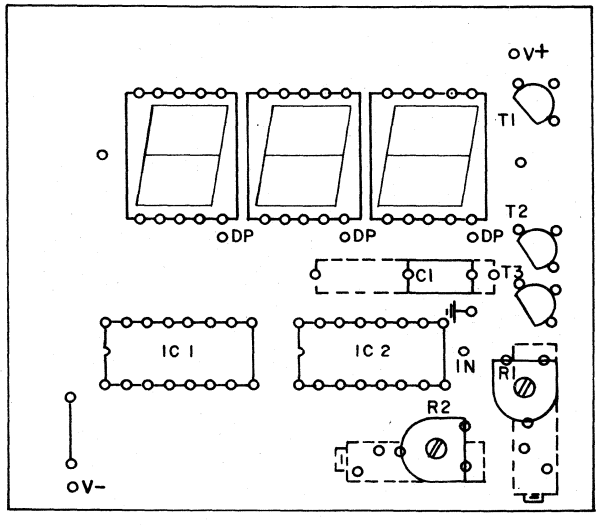


Fig. 5—Typical common-cathode LED application.



92CS-32692

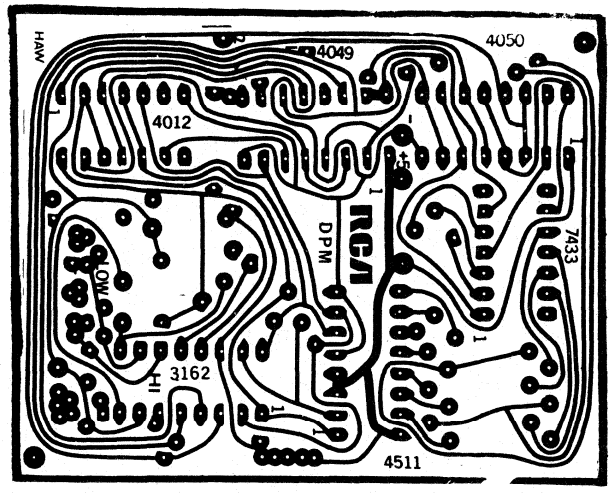


92CS-32693

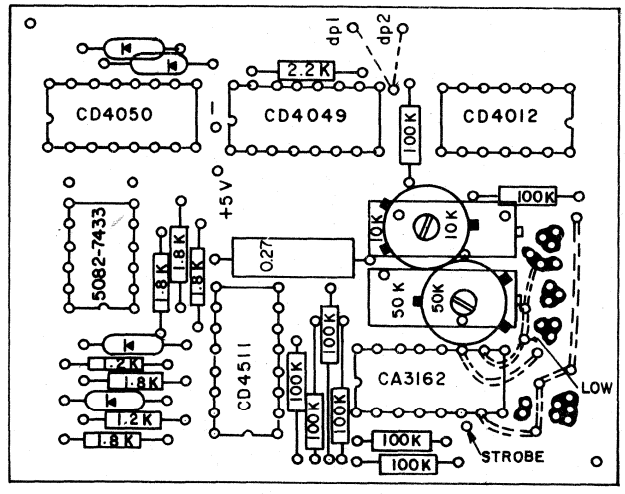
Fig. 6—P.C. board template (actual size ±3%) and component layout guide for circuit shown in Fig. 2.*

**P.C. board courtesy ETS. Velleman P.V.B.A., St. Amandsberg, Belgium*

CA3162E

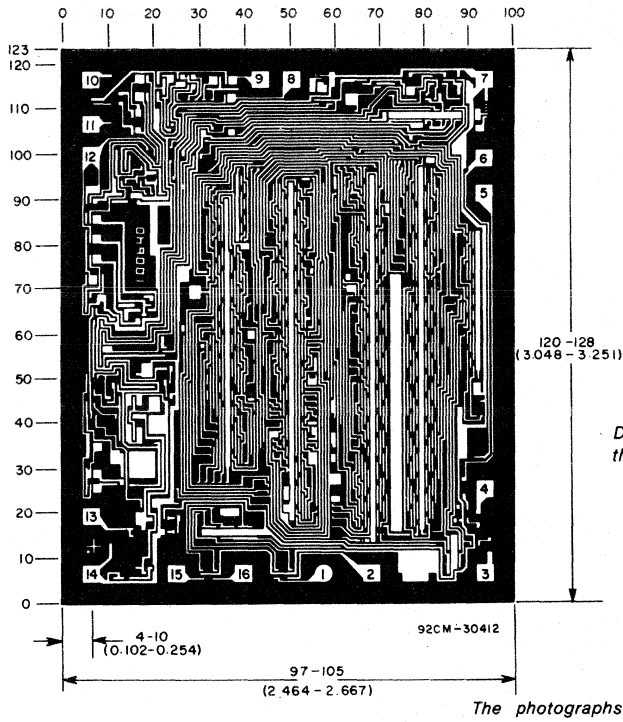


92CS-32691



92CS-32694

Fig. 7—P.C. board template (actual size ±3%) and component layout guide for circuit shown in Fig. 5.

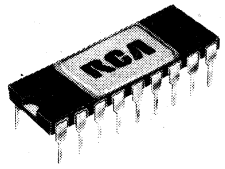


Dimensions and pad layout for the CA3162H Chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each Linear chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3300



18-LEAD DUAL-IN-LINE
SIDE-BRAZED
CERAMIC PACKAGE H-1910

CMOS Video Speed 6-Bit Flash Analog-to-Digital Converter

For Use in Low-Power Consumption, High-Speed Digitization Applications

FEATURES:

- *CMOS low power with speed*
- *Parallel conversion technique*
- *15-MHz sampling rate (66-ns conversion time)*
- *6-bit latched 3-state output with overflow bit*
- *±½ LSB accuracy*
- *Single supply voltage (3 to 10 V)*
- *2 units in series allow 7-bit output*
- *2 units in parallel allow 30-MHz sampling rate*
- *Internal VREF with ext VREF option*

The RCA-CA3300 is a CMOS 50-mW parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high-speed digitization.

The CA3300 operates over a wide full-scale input-voltage range of 2.4 volts up to the dc supply voltage with maximum power consumptions as low as 50 to 200 mW, depending upon the clock frequency selected. When operated from a 5-volt supply at a clock frequency of 11 MHz, the power consumption of the CA3300 is less than 50 mW. When operated from an 8-volt supply at a frequency of 15 MHz, the power consumption is less than 150 mW.

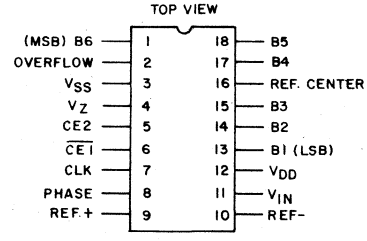
The intrinsic high conversion rate makes the CA3300 ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3300s in series to increase the resolution of the conversion system. A series connection of two CA3300s may be used to produce a 7-bit high-speed converter. Operation of two CA3300s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz). CA3300s in parallel may be combined with a high-speed 6-bit D/A converter, a binary adder, control logic, and an op amp to form a very high-speed A/D converter.

Sixty-four paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3300. Sixty-three comparators are required to quantize all input voltage levels in this 6-bit converter, and the additional comparator is required for the overflow bit.

The CA3300 type is available in an 18-lead dual-in-line ceramic package (D suffix) or in chip form (H suffix).

APPLICATIONS

- *The CA3300 is especially suited for high-speed conversion applications where low power is also important*
- *TV video digitizing (industrial/security)*
- *High-speed A/D conversion*
- *Ultrasound signature analysis*
- *Transient signal analysis*
- *High-energy physics research*
- *High-speed oscilloscope storage/display*
- *General-purpose hybrid ADCs*
- *Optical character recognition*
- *Radar pulse analysis*
- *Motion signature analysis*



92CS-32263RI

TERMINAL ASSIGNMENT

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	6	Bits
Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=15 MHz, gain adjusted	—	±0.5	±0.8	LSB
Differential Linearity Error	V_{DD}=8, V_{REF}=7.68 V CLK=15 MHz	—	±0.5	±0.8	
Quantizing Error		-1/2	—	1/2	
Analog Input: Full Scale Range	V_{DD}=8 V CLK=15 MHz	2.4	—	V_{DD} +0.5	V
Input Capacitance		—	50	—	pF
Input Current		—	600	1000	μA
Gain Temperature Coefficient	V_{DD}=8 V, CLK=15 MHz	—	0.016	—	LSB/°C
Maximum Conversion Speed	V_{DD}=5 V	—	12M	—	SPS
	V_{DD}=8 V	15M	19M	—	
Device Current (Excludes I_{REF}, I_Z)	V_{DD}=5 V (CLK=11 MHz)	—	7	—	mA
	V_{DD}=8 V (CLK=15 MHz)	—	22	—	
	V_{DD}=5 V (Auto Balance State)	—	6.4	16	
	V_{DD}=8 V (Auto Balance State)	—	24	40	
Ladder Impedance		1000	1400	1800	Ω
Digital Inputs: Low Voltage	V_{DD}=5 V	—	—	1.5	V
	V_{DD}=8 V	—	—	2.5	V
High Voltage	V_{DD}=5 V	3.5	—	—	V
	V_{DD}=8 V	5.5	—	—	V
Input Current	V_{DD}=8 V	—	±1	—	μA
Digital Outputs: Output Low (Sink) Current	V_{DD}=5 V, V_O=0.4 V	1.6	10	—	mA
	V_{DD}=8 V, V_O=0.5	3.2	15	—	
Output High (Source) Current	V_{DD}=5 V, V_O=4.6 V	-0.8	6	—	
	V_{DD}=8 V, V_O=7.5 V	-1.6	9	—	
Zener Voltage	I_Z=10 mA	6.2	6.8	7.4	V
Zener Dynamic Impedance	I_Z=10 mA	—	10	30	Ω
Zener Temperature Coefficient		—	0.5	—	mV/°C
Digital Output Delay, t_d	V_{DD}=8 V	—	20	—	ns
Aperture Time	V_{DD}=8 V	—	25	—	

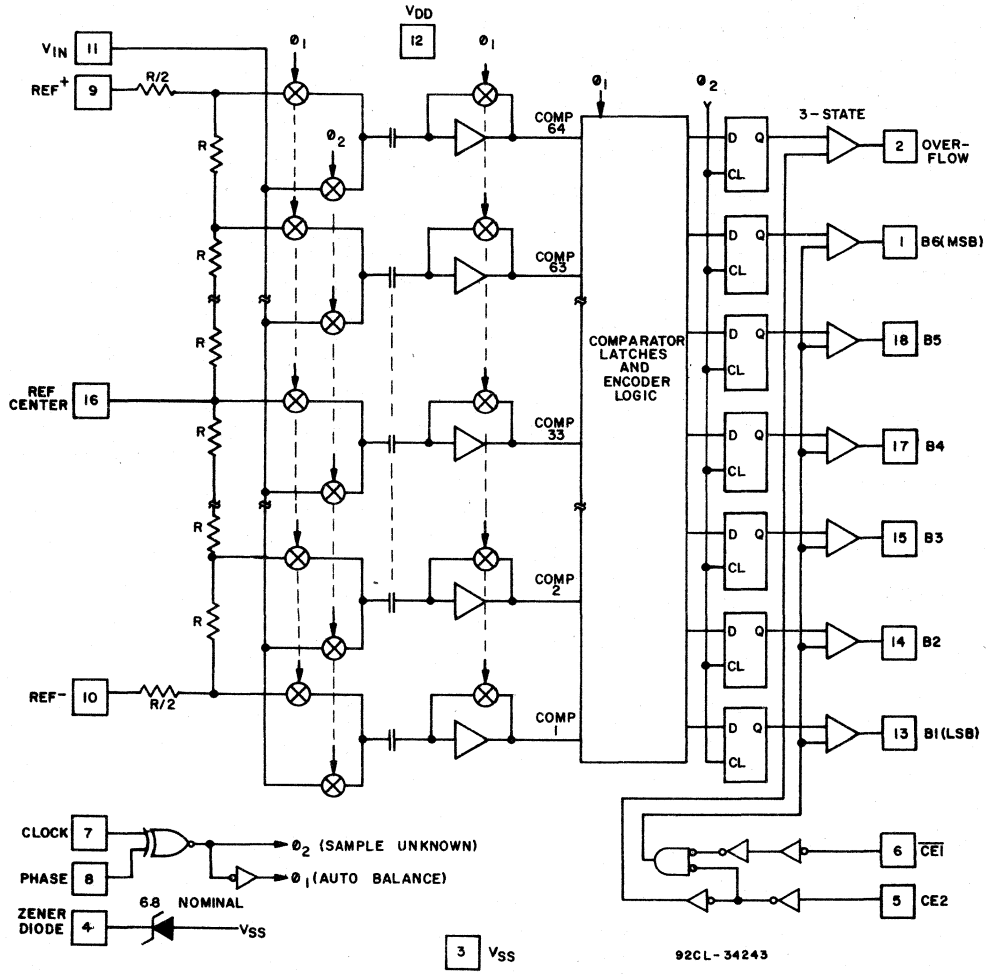
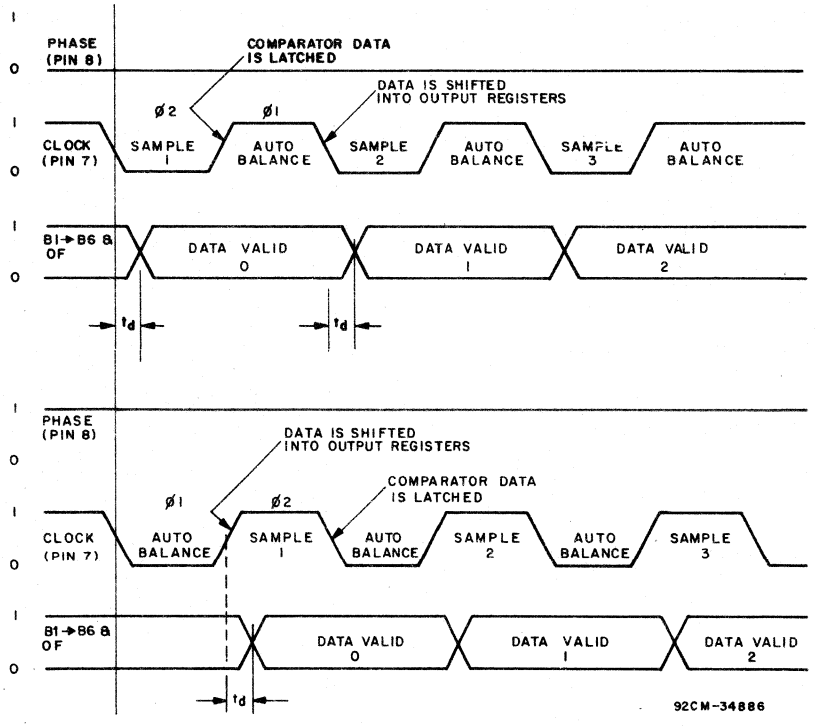


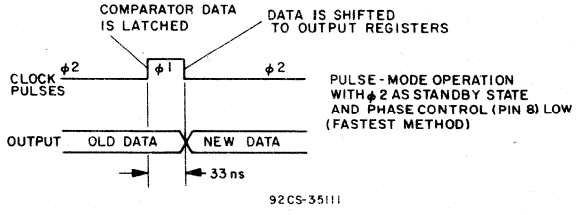
Fig. 1 - Block diagram for the CA3300.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

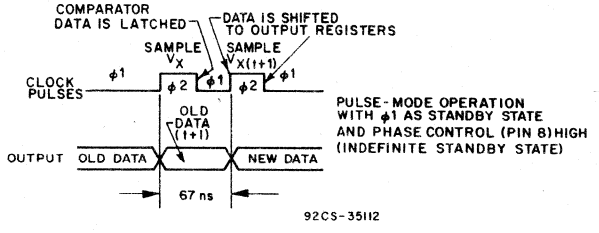
DC SUPPLY VOLTAGE RANGE (V_{DD})
(VOLTAGE REFERENCED TO V_{SS} TERMINAL) ..... -0.5 to 10 V
INPUT VOLTAGE RANGE
ALL INPUTS EXCEPT ZENER (PIN 4) ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT
CLK, PH, $\overline{CE1}$, CE2, V_{IN} ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = -40 to 55°C ..... 315 mW
FOR T_A = 55°C to 85°C ..... Derate linearly at 3.3 mW/°C
TEMPERATURE RANGE
OPERATING ..... -40 to +85°C
STORAGE ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
AT DISTANCE 1/16 ± 1/32 in. (1.59 ± 0.79 mm) FROM CASE FOR 10 s MAX. ..... +265°C



(a)



(b)



(c)

Fig. 2 - Timing diagrams for the CA3300.

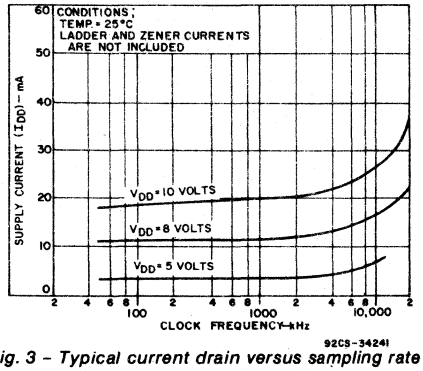


Fig. 3 - Typical current drain versus sampling rate as a function of supply voltage.

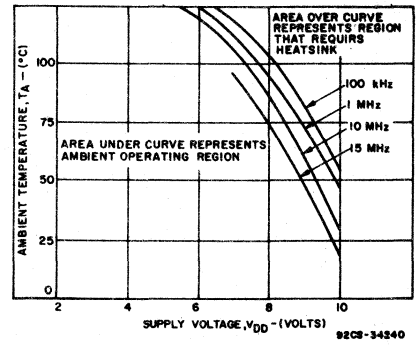


Fig. 4 - Maximum ambient temperature versus supply voltage. (Above curve includes ladder dissipation but not the zener dissipation.)

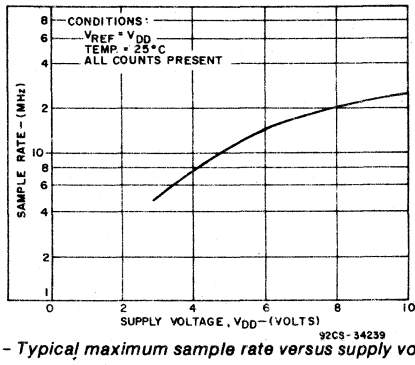


Fig. 5 - Typical maximum sample rate versus supply voltage.

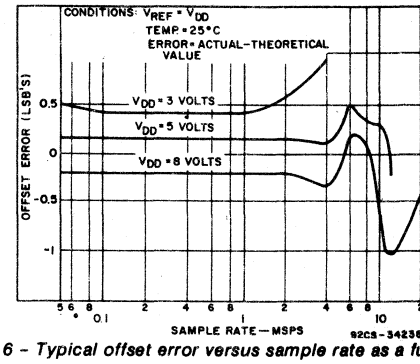


Fig. 6 - Typical offset error versus sample rate as a function of supply voltage. (See literature for offset trim.)

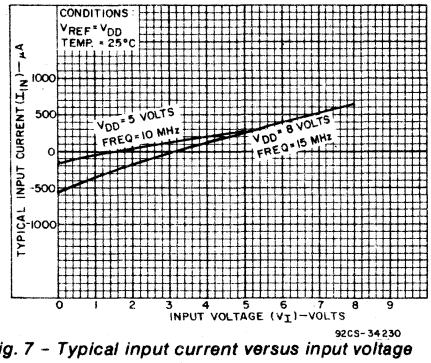


Fig. 7 - Typical input current versus input voltage as a function of supply voltage.

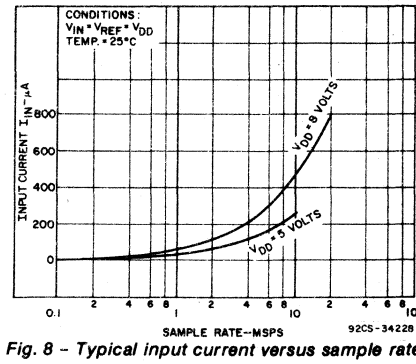


Fig. 8 - Typical input current versus sample rate as a function of supply voltage.

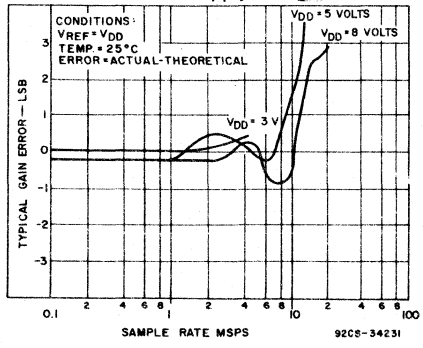


Fig. 9 - Typical gain error versus sample rate as a function of supply voltage. (See literature for gain trim.)

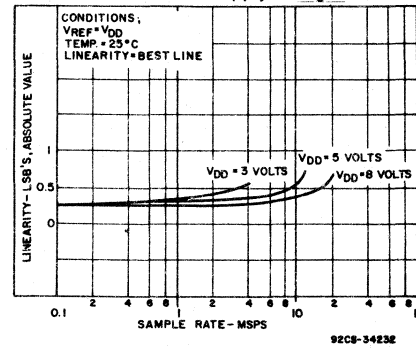


Fig. 10 - Typical linearity versus sample rate as a function of supply voltage.

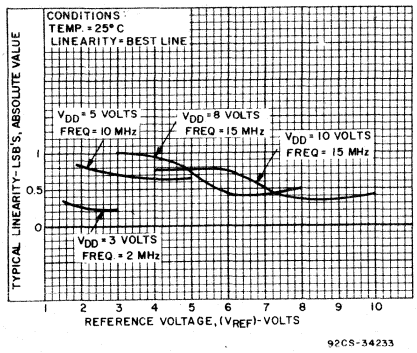


Fig. 11 - Typical linearity versus reference voltage as a function of supply voltage.

Device Operation

A sequential parallel technique is used by the CA3300 converter to obtain its high-speed operation. The sequence consists of the "Auto Balance" phase, Ø1, and the "Sample Unknown" phase Ø2. (Refer to the circuit diagram.) Each conversion takes one clock cycle.* With the phase control (pin 8) low, the "Auto Balance" (Ø1) occurs during the High period of the clock cycle, and the "Sample Unknown" (Ø2) occurs during the low period of the clock cycle.

During the "Auto Balance" phase, a transmission switch is used to connect each of 64 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{tap}(N) = [(V_{REF}/64) \times N] - [V_{REF}/(2 \times 64)]$$
$$= V_{REF}[(2N - 1)/128]$$

Where: $V_{tap}(n)$=reference ladder tap voltage at point n.
V_{REF}=voltage across R^- to R^+
N=tap number (1 through 64)

The other side of the capacitor is connected to a single stage amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately, $(V_{DD}-V_{SS})/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Sample Unknown" phase, all ladder tap switches are opened, the comparator amplifiers are no longer shorted, and V_{IN} is switch to all 64 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators with tap voltages greater than V_{IN} will drive the comparator outputs to a "low" state, all comparators with tap voltage lower than V_{IN} will drive the comparator outputs to a "high" state.

*This device requires only a single phase clock. The terminology of $\phi 1$ and $\phi 2$ refers to the High and Low periods of the same clock.

The status of all these comparator amplifiers are stored at the end of this phase (Ø2), by a secondary latching amplifier stage. Once latched, the status of the 64 comparators is decoded by a 64 to 7 bit decode array and the results are clocked into a storage register at the rising edge of the next Ø2.

A 3-state buffer is used at the output of the 7 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B6 when it is in a high state. CE2 will independently disable B1 through B6 and the OF buffers when it is in the low state.

To facilitate usage of this device a phase control input is provided which can effectively complement the clock as it enters the chip. Also, an onboard zener is provided for use as a reference voltage.

Continuous Clock Operation

One complete conversion cycle can be traced through the CA3300 via the following steps. (Refer to timing diagram Fig. 2a.) With the phase control in a 'High' state, the rising edge of the clock input will start a "sample" phase. During this entire 'High' state of the clock, the 64 comparators will track the input voltage and the 64 latches will track the comparator outputs. At the falling edge of the clock, all 64 comparator outputs are captured by the 64 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this 'Low' state of the clock the output of the latches propagates through the decode array and a 7-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 7-bit code is shifted into the output registers and appears with time delay t_d as valid data at the output of the 3-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse Mode Operation

For sampling high-speed nonrecurrent or transient data, the converter may be operated in a pulse mode in one of two ways. The fastest method is to keep the converter in the Sample Unknown phase, Ø2, during the standby state. The device can now be pulsed through the Auto Balance phase with as little as 33 ns. The analog value is captured on the leading edge of Ø1 and is transferred into the output registers on the trailing edge of Ø1. We are now back in the standby state, Ø2, and another conversion can be started within 33 ns, but not later than 10 μs due to the eventual droop of the commutating capacitors. Another advantage of this method is that it has the potential of having the lowest power drain. The larger the time ratio between Ø2 and Ø1, the lower the power consumption. (See timing diagram Fig. 2b.)

The second method uses the Auto Balance phase, Ø1, as the standby state. In this state the converter can stay indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two Ø2 pulses. The first pulse starts a Sample Unknown phase and captures the analog value in the comparator latches on the trailing edge. A second Ø2 pulse is needed to transfer the data into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes place in 67 ns, but the repetition rate may be as slow as desired. The disadvantage to this method is the higher device dissipation due to the low ratio of Ø2 to Ø1. (See timing diagram Fig. 2c.)

Increased Accuracy

In most cases the accuracy of the CA3300 should be

sufficient without any adjustments. In applications where accuracy is of utmost importance, three adjustments can be made to obtain better accuracy; i.e., offset trim, gain trim, and midpoint trim.

Offset Trim

In general offset correction can be done in the preamp circuitry by introducing a DC shift to V_{IN} or by the offset trim of the op-amp. When this is not possible the R^- (pin 10) input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is ½ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = \tfrac{1}{2} \text{ LSB} = \tfrac{1}{2}(V_{REF}/64)$$
$$= V_{REF}/128$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50-ohm pot connected between R^- and ground will accomplish the adjustment. Set V_{IN} to ½ LSB and trim the pot until the 0 to 1 transition occurs.

If V_{IN} for the first transition is greater than the theoretical, then the 50-ohm pot should be connected between R^- and a negative voltage of about 2 LSB's. The trim procedure is as stated previously.

Gain Trim

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op-amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 63 to overflow transition. That voltage is ½ LSB less than V_{REF} and is calculated as follows:

$$V_{IN} \text{ (63 to 64 transition)} = V_{REF} - V_{REF}/128$$
$$= V_{REF}\,(127/128)$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 63 to overflow transition. Now adjust V_{REF} until that transition occurs on the outputs.

Midpoint Trim

The reference center (RC), pin 16, is available to the user as the approximate midpoint of the resistor ladder. The actual count that is brought out is count 33. To trim the midpoint the offset and gain trims should be done first. The theoretical transition from count 32 to 33 occurs at 32½ LSB's. That voltage is as follows:

$$V_{IN} \text{ (32 to 33 transition)} = 32.5\,(V_{REF}/64)$$

An adjustable voltage follower can be connected to the RC pin or a 2K pot can be connected between R^+ and R^- with the wiper connected to RC. Set V_{IN} to the 32 to 33 transition voltage, then adjust the voltage follower or the pot until the transition occurs on the output bits.

The Reference Center point can also be used to create some unique transfer functions. For example, if R^- is grounded, RC is connected to 3.25 volts, and R^+ is connected to 4.8 volts then the lower order counts, 1 through 33, will have an LSB value of 100 mV while the upper order counts, 34 through Overflow, will have an LSB value of 50 mV. This effectively provides twice the sensitivity in the upper counts as compared to the lower counts.

7-Bit Resolution

To obtain 7-bit resolution, two CA3300s can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enabler controls—all of which are available on the CA3300.

The first step for connecting a 7-bit circuit is to totem-pole the ladder networks, as illustrated in Fig. 13. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the seventh bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower a-d converter and the CE2 control of the upper a-d converter. The three-state outputs of the two devices (bits 1 through 6) are now connected in parallel to complete the circuitry. The complete circuit for a 7-bit a-d converter is shown in Fig. 14.

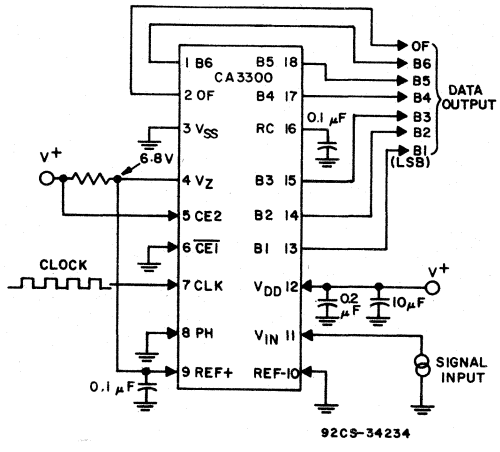


Fig. 12 - Typical CA3300 6-bit configuration 15-MHz sampling rate.

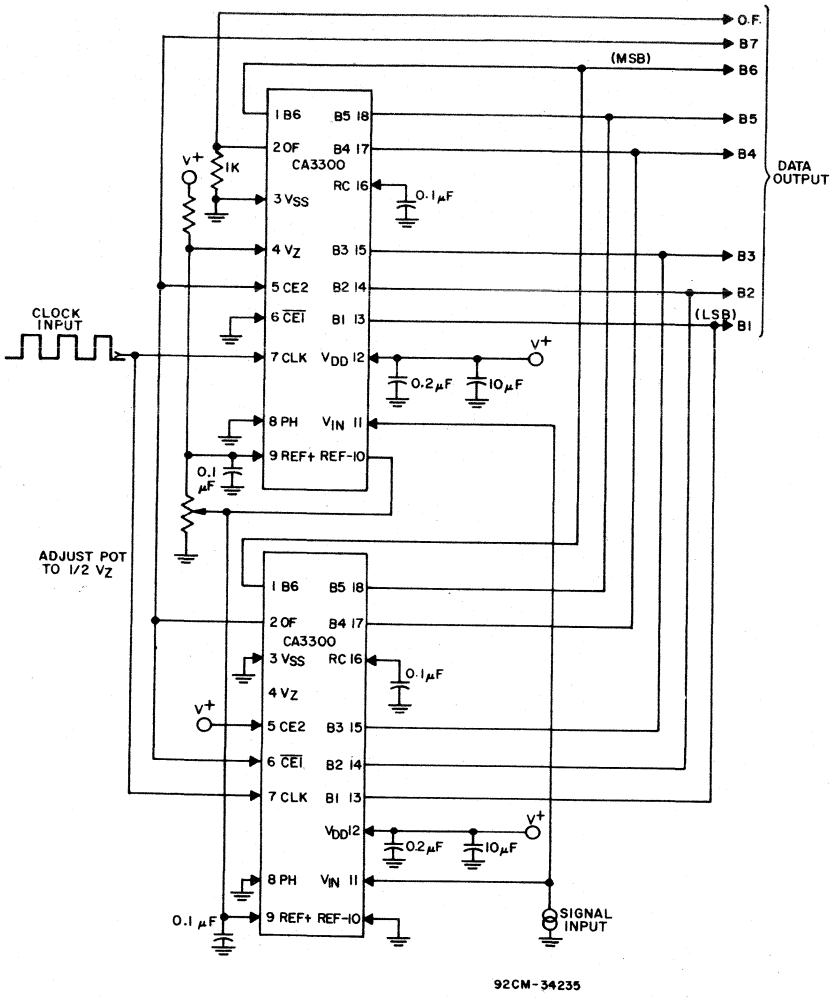


Fig. 13 - Typical CA3300 7-bit resolution configuration 15-MHz sampling rate.

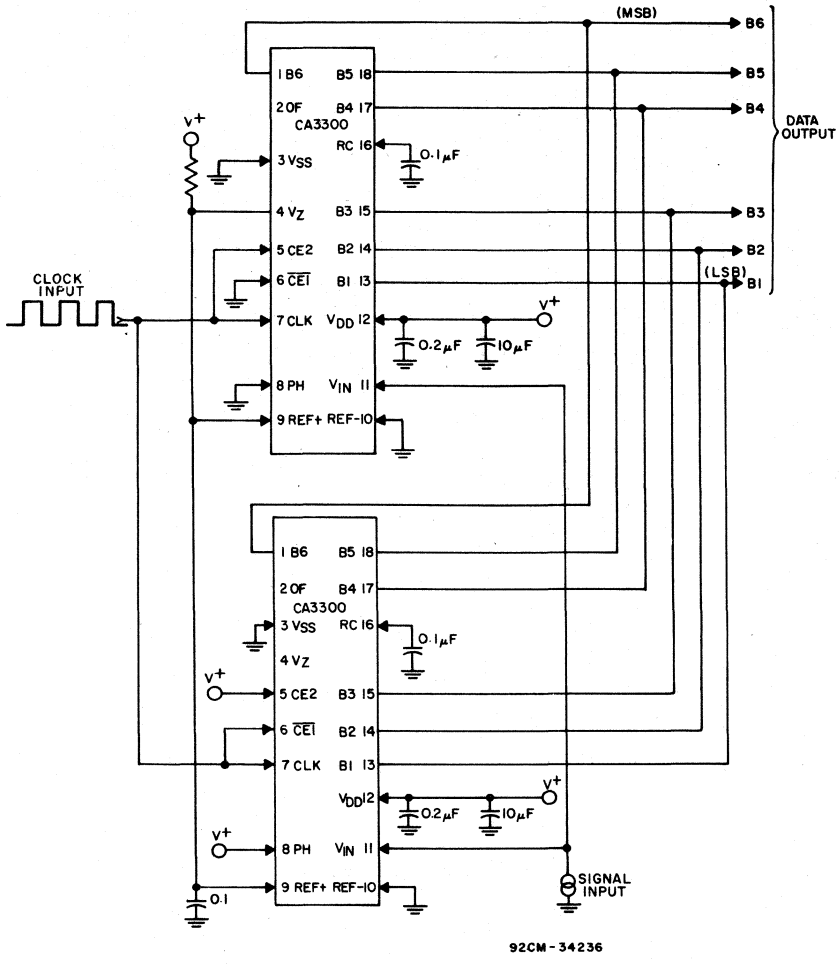


Fig. 14 - Typical CA3300 6-bit resolution configuration 30-MHz sampling rate.

8-Bit to 12-Bit Conversion Techniques

To obtain 8 to 12-bit resolution and accuracy, use a feed-forward conversion technique. Two a-d converters will be needed to convert up to 11 bits; three a-d converters to convert 12 bits. The high speed of the CA3300 allows 12-bit conversions in the 500 to 900-ns range.

The circuit diagram of a high-speed 12-bit a-d converter is shown in Fig. 15. In the feed-forward conversion method two sequential conversions are made. Converter A first does a coarse conversion to 6 bits. The output is applied to a 6-bit d-a converter whose accuracy level is good to 12 bits. The d-a converter output is then subtracted from the input voltage, multiplied by 32, and then converted by a second flash a-d converter, which is connected in a 7-bit configuration. The answers from the first and second conversions are added together with bit 1 of the first conversion overlapping bit 7 of the second conversion.

When using this method, take care that:

- The linearity of the first converter is better than ½ LSB.
- An offset bias of 1 LSB (1/64) is subtracted from the first conversion since the second converter is unipolar.
- The d-a converter and its reference are accurate to the total number of bits desired for the final conversion (the a-d converter need only be accurate to 6 bits).

  The first converter can be offset-biased by adding a 20-Ω resistor at the bottom of the ladder and increasing the reference voltage by 1 LSB. If a 6.40-voltage reference is used in the system, for example, then the first CA3300 will require a 6.5-V reference.

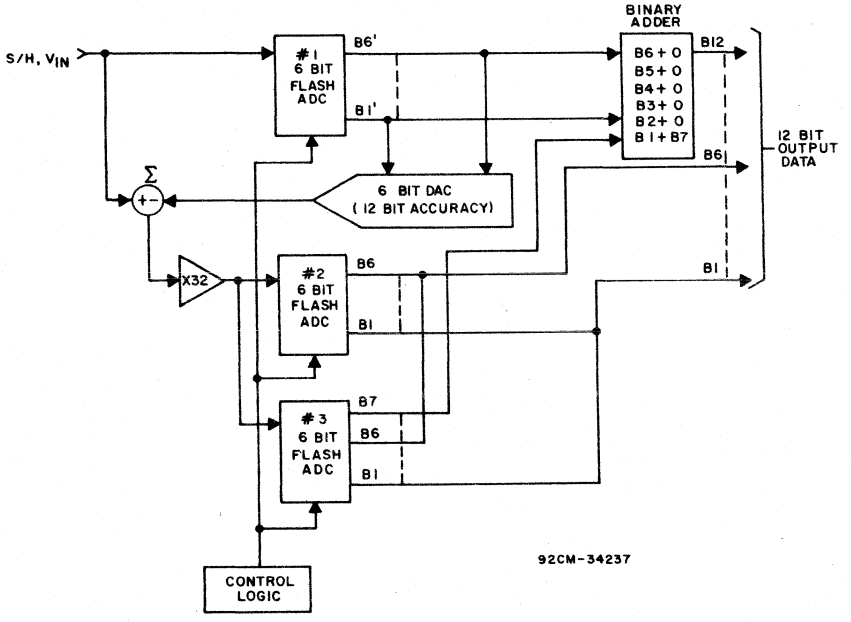


Fig. 15 - Typical CA3300 800-nanosecond 12-bit ADC system.

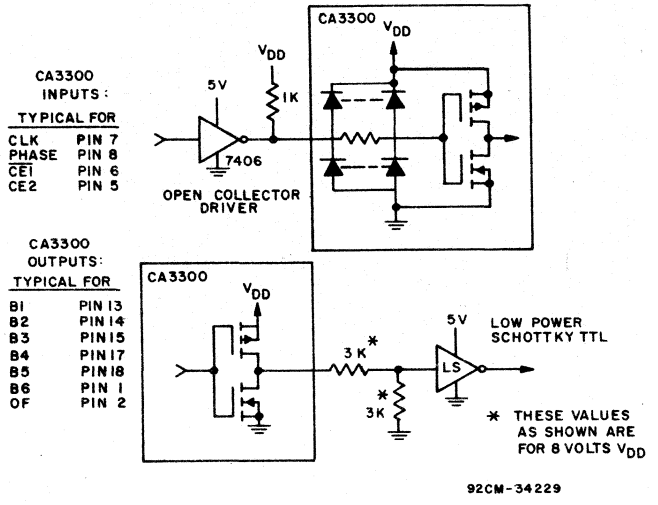
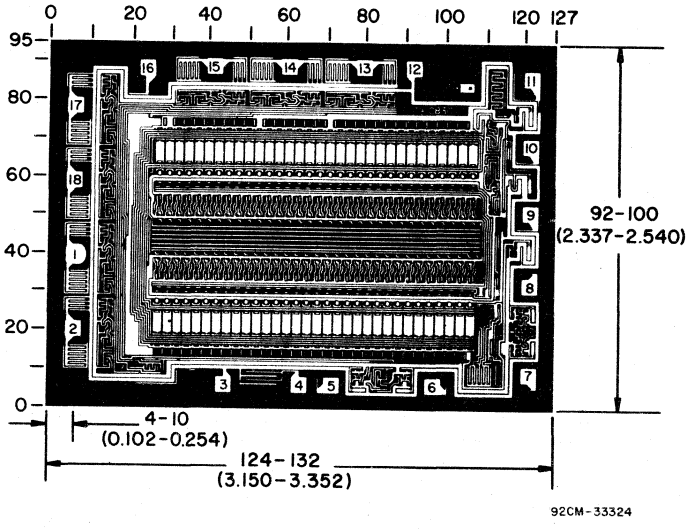


Fig. 16 - TTL interface circuit for V_{DD} >5.5 volts.

OUTPUT CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE* VREF 7.68 (VOLTS)	VREF 6.40 (VOLTS)	VREF 5.12 (VOLTS)	VREF 3.20 (VOLTS	BINARY OUTPUT CODE 0.F	B6	B5	B4	B3	B2	(LSB) B1	DECIMAL COUNT
ZERO	0.00	0.00	0.00	0.00	0	0	0	0	0	0	0	0
1 LSB	0.12	0.10	0.08	0.05	0	0	0	0	0	0	1	1
2 LSB	0.24	0.20	0.16	0.10	0	0	0	0	0	1	0	2
'	'	'	'	'	'	'	'	'	'	'	'	'
'	'	'	'	'	'	'	'	'	'	'	'	'
'	'	'	'	'	'	'	'	'	'	'	'	'
'	'	'	'	'	'	'	'	'	'	'	'	'
½ Full Scale — 1 LSB	3.72	3.10	2.48	1.55	0	0	1	1	1	1	1	31
½ Full Scale	3.84	3.20	2.56	1.60	0	1	0	0	0	0	0	32
½ Full Scale +1 LSB	3.96	3.30	2.64	1.65	0	1	0	0	0	0	1	33
'	'	'	'	'	'	'	'	'	'	'	'	'
'	'	'	'	'	'	'	'	'	'	'	'	'
'	'	'	'	'	'	'	'	'	'	'	'	'
'	'	'	'	'	'	'	'	'	'	'	'	'
Full Scale — 1 LSB	7.44	6.20	4.96	3.10	0	1	1	1	1	1	0	62
Full Scale	7.56	6.30	5.04	3.15	0	1	1	1	1	1	1	63
Overflow	7.68	6.40	5.12	3.20	1	1	1	1	1	1	1	127

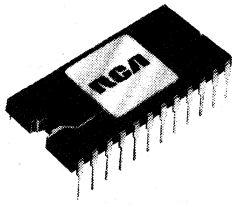
*THE VOLTAGES LISTED BELOW ARE THE IDEAL CENTERS OF EACH OUTPUT CODE SHOWN AS A FUNCTION OF ITS ASSOCIATED REFERENCE VOLTAGE.



Dimensions and pad layout for CA3300H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



(D) SUFFIX
24-Lead Dual-In-Line
Side-Brazed Ceramic Package

CMOS Video Speed 8-Bit Flash Analog-to-Digital Converter

For Use in Low-Power Consumption, High-Speed Digitization Applications

Features:
- *CMOS low power with SOS speed*
- *Parallel conversion technique*
- *15-MHz sampling rate (66-ns conversion time)*
- *8-bit latched 3-state output with overflow bit*
- *± ½ LSB accuracy (typ.)*
- *Single supply voltage (4 to 8 V)*
- *2 units in series allow 9-bit output*
- *2 units in parallel allow 30-MHz sampling rate*

The RCA CA3308* is a CMOS 240-mW parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high-speed digitization.

The CA3308 operates over a wide full-scale input-voltage range of 4 volts up to 8 volts with maximum power consumptions as low as 240 mW, depending upon the clock frequency selected. When operated from a 5-volt supply at a clock frequency of 15 MHz, the power consumption of the CA3308 is typically 240 mW.

The intrinsic high conversion rate makes the CA3308 ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3308s in series to increase the resolution of the conversion system. A series connection of two CA3308s may be used to produce a 9-bit high-speed converter. Operation of two CA3308s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz). CA3308s may be combined with a high-speed 8-bit D/A converter, a binary adder, control logic, and an op amp to form a very high-speed 15-bit A/D converter.

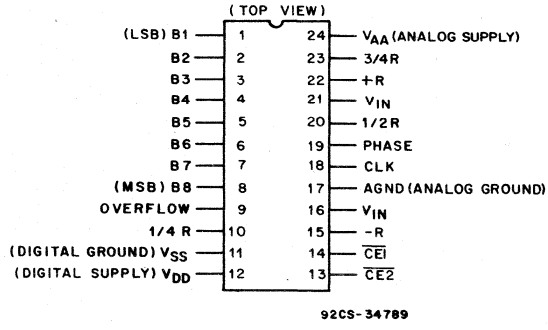
256 paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3308.

255 comparators are required to quantize all input voltage levels in this 8-bit converter, and the additional comparator is required for the overflow bit.

The voltage supply for analog circuitry is termed V_{AA} and AGND. The voltage supply for digital circuitry is termed V_{DD} and V_{SS}.

The CA3308 type is available in a 24-lead dual-in-line ceramic package (D suffix).

Applications:
- *The CA3308 is especially suited for high-speed conversion applications where low power is also important*
- *TV video digitizing (industrial/security/broadcast)*
- *High-speed A/D conversion*
- *Ultrasound signature analysis*
- *Transient signal analysis*
- *High-energy physics research*
- *High-speed oscilloscope storage/display*
- *General-purpose hybrid ADCs*
- *Optical character recognition*
- *Radar pulse analysis*
- *Motion signature analysis*
- *µP data acquisition systems*



TERMINAL ASSIGNMENT

* Formerly Developmental Type No. TA11279.

CA3308

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE (V_{DD} AND V_{AA})
(VOLTAGE REFERENCED TO V_{SS} TERMINAL) ..... −0.5 to +8 V

INPUT VOLTAGE RANGE
ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

DC INPUT CURRENT
CLK, PH, CE1, CE2, V_{IN} ..... ±10 mA

POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A=−40 to 55°C ..... 315 mW
FOR T_A=55°C to 85°C ..... Derate linearly at 3.3 mW/°C

TEMPERATURE RANGE
OPERATING ..... −40 to +85°C
STORAGE ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING)
AT DISTANCE 1/16 ± 1/32 in. (1.59 ± 0.79 mm) FROM CASE FOR 10 s MAX. ..... +265°C

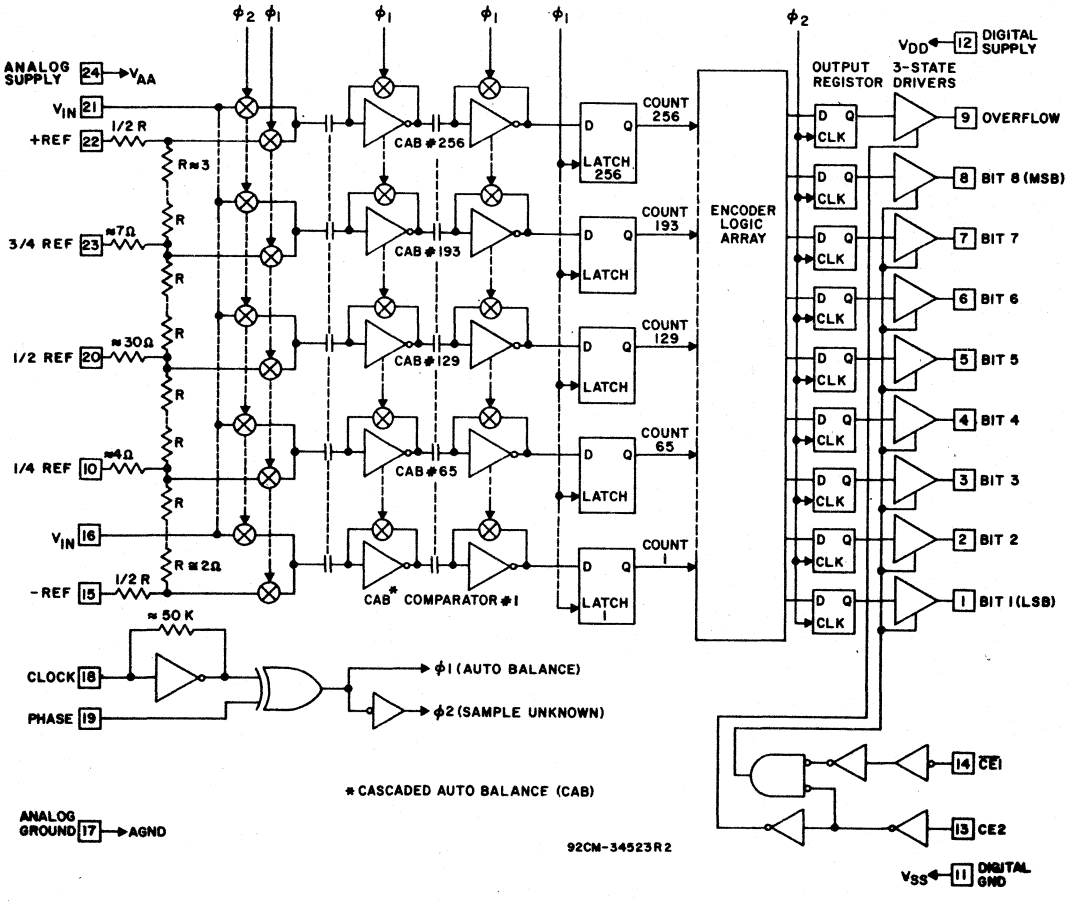


Fig. 1-Block diagram for the CA3308.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS $V_{AA} = V_{DD}$	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	8	Bits
Linearity Error	V_{DD}=5 V, V_{REF}=6.4 V CLK=15 MHz, gain adjusted	—	—	±1	(CA3308D)
Differential Linearity Error	V_{DD}=5 V_{REF}=6.4 V CLK=15 MHz	—	—	±1	(CA3308D)
Quantizing Error		−½	—	½	LSB
Analog Input:	V_{DD}=5 V				
Full Scale Range	CLK=15 MHz	4	—	8	V
Input Capacitance		—	50	—	pF
Input Current	V_{IN}= 6.4 V	—	1000	2000	μA
Maximum Conversion Speed	V_{DD}=5 V	15 M	17 M	—	SPS
Device Current (Excludes I_{REF})	V_{DD}=5 V (CLK=15 MHz)	—	30	—	mA
Ladder Impedance		300	600	900	Ω
Digital Inputs:					
Low Voltage		—	—	1.5	V
High Voltage	V_{DD}=5 V	3.5	—	—	V
Input Current (Except Pin 18)		—	±1	—	μA
Digital Outputs:					
Output Low (Sink) Current	V_{DD}=5 V, V_O=0.4 V	3.2	10	—	mA
Output High (Source) Current	V_{DD}=5 V, V_O=4.6 V	1.6	−6	—	
Digital Output Delay, t_d	V_{DD}=5 V	—	25	—	ns

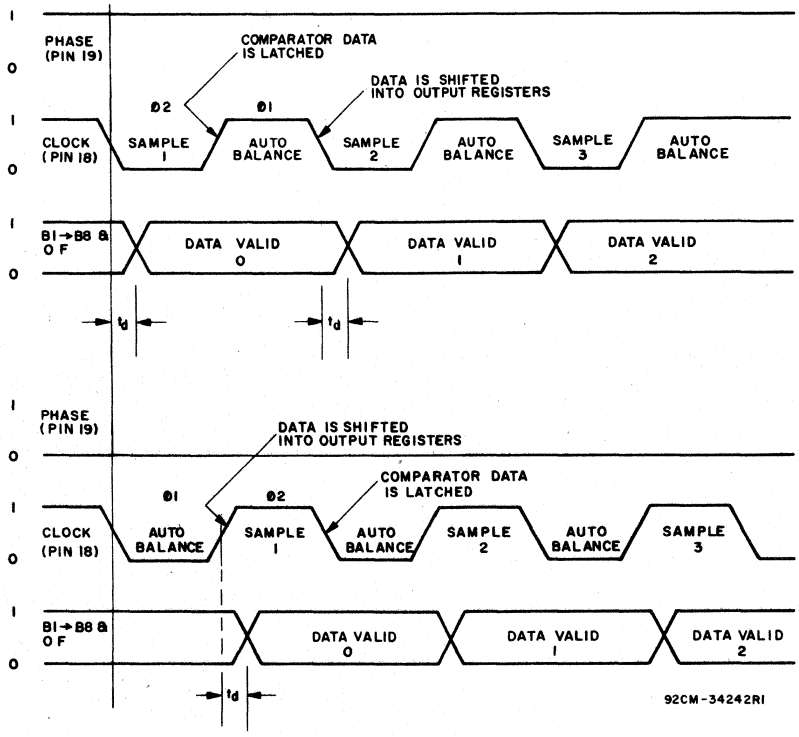


Fig. 2-Timing diagram for the CA3308.

CA3308

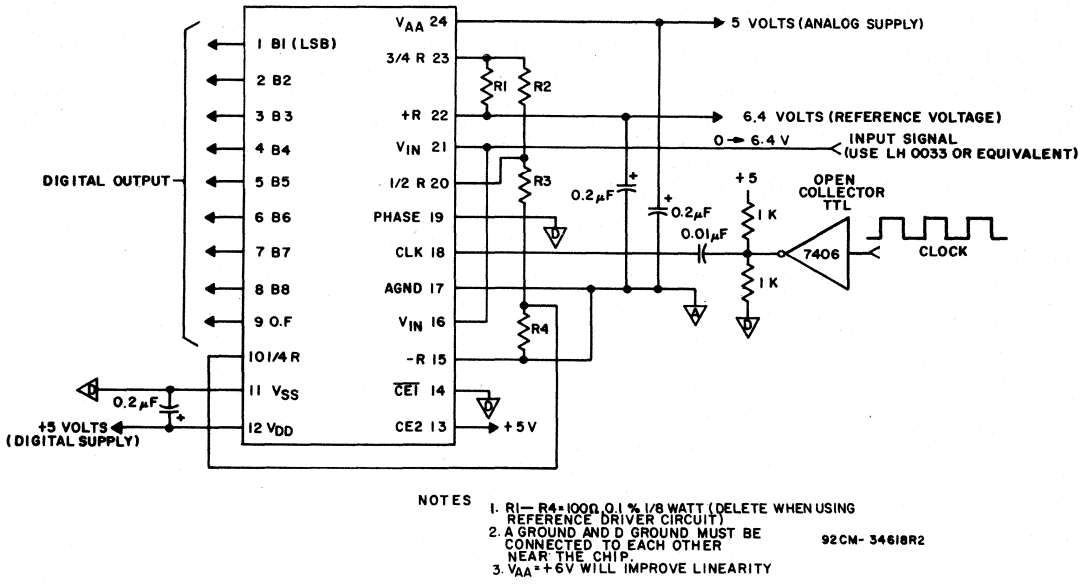


Fig. 3-Typical circuit configuration for the CA3308.
(15-MHz sampling rate)

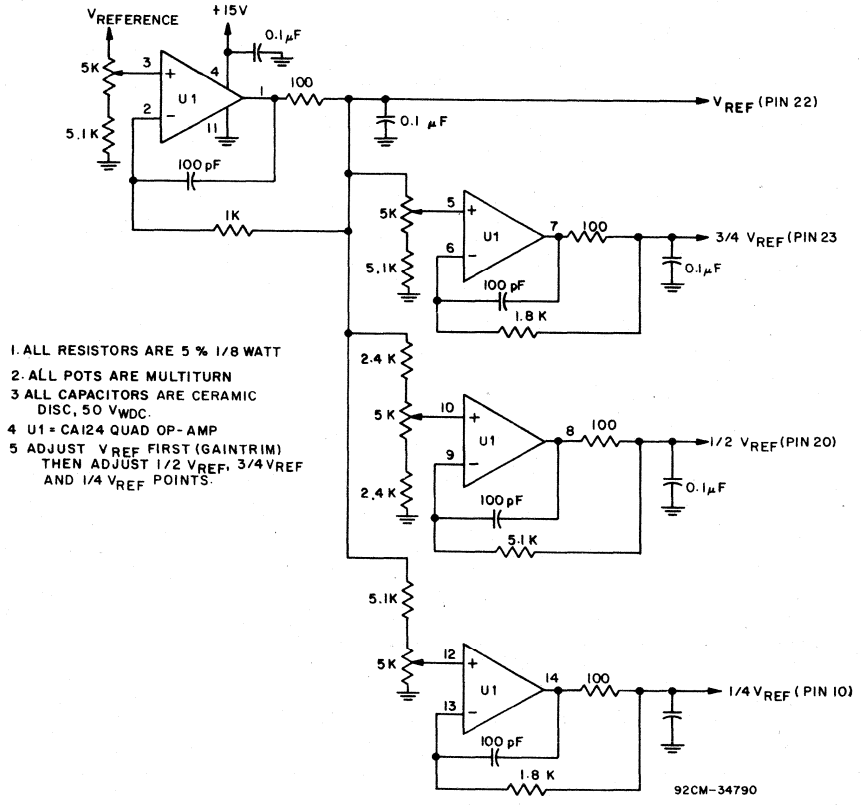


Fig. 4-Reference driver circuit.
(Use for maximum linearity)

Device Operation

A sequential parallel technique is used by the CA3308 converter to obtain its high-speed operation. The sequence consists of the "Auto Balance" phase, Ø1, and the "Sample Unknown" phase Ø2. (Refer to the circuit diagram.) Each conversion takes one clock cycle.* With the phase control (pin 8) high, the "Auto Balance" (Ø1) occurs during the High period of the clock cycle, and the "Sample Unknown" (Ø2) occurs during the low period of the clock cycle.

During the "Auto Balance" phase, a transmission switch is used to connect each of the first set of 256 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{tap}(N)=[(N/256)\,V_{REF}]-[(1/512)\,V_{REF}]$$
$$=[(2N-1/512]V_{REF}$$

Where:

$V_{tap}(n)$=reference ladder tap voltage at point n.

V_{REF}=voltage across −REF to +REF

N=tap number (1 through 256)

The other side of these capacitors are connected to single stage amplifiers whose outputs are shorted to their inputs by switches. This balances the amplifiers at their intrinsic trip points, which is approximately, $V_{DD}-V_{SS}/2$. The first set of capacitors now charge to their associated tap voltages.

At the same time a second set of commutating capacitors and amplifiers are also auto-balanced. The balancing of the second stage amplifier at its intrinsic trip point removes any tracking differences between the first and second amplifier stages. The cascaded auto-balance (CAB) technique, used here, increases comparator sensitivity and temperature tracking.

In the "Sample Unknown" phase, all ladder tap switches and comparator shorting switches are opened. At the same time V_{in} is switched to the first set of commutating capacitors. Since the other end of the capacitors are now looking into an effectively open circuit, any input voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators that had tap voltages greater than V_{in} will go to a "low" state at their outputs. All comparators that had tap voltages lower than V_{in} will go to a "high" state.

The status of all these comparator amplifiers are ac coupled through the second stage comparator and stored at the end of this phase (Ø2), by a latching amplifier stage. Once latched, the status of the comparators are decoded by a 256 to 9-bit decode array and the results are clocked into a storage register at the rising edge of the next Ø2.

A 3-state buffer is used at the output of the 9 storage registers which are controlled by two chip-enable signals. CE1 will independently disable B1 through B8 when it is in a high state. CE2 will independently disable B1 through B8 and the OF buffers when it is in the low state.

To facilitate usage of this device a phase control input is provided which can effectively complement the clock as it enters the chip.

Continuous Clock Operation

One complete conversion cycle can be traced through the CA3308 via the following steps. (Refer to timing diagram No. 1.) With the phase control in a "low" state, the rising edge of the clock input will start a "sample" phase. During this entire "high" state of the clock, the comparators will track the input voltage and the latches will track the comparator outputs. At the falling edge of the clock, all 256 comparator outputs are captured by the 256 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this "low" state of the clock the output of the latches propagates through the decode array and a 9-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 9-bit code is shifted into the output registers and appears with time delay t_d as valid data at the output of the 3-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

*This device requires only a single phase clock. The terminology of 01 and 02 refers to the High and Low periods of the same clock.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD}—V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

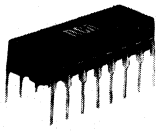
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

CA3081, CA3082 Types

16-Lead Dual-In-Line
Frit-Seal (Hermetic)
Package H-1807



16-Lead Dual-In-Line
Plastic Package H-1622

General-Purpose High-Current N-P-N Transistor Arrays

CA3081 — Common-Emitter Array
CA3082 — Common-Collector Array

Directly Drive 7-Segment Incandescent Displays and Light-Emitting-Diode (LED) Displays

Features:

- *7 transistors permit a wide range of applications in either a common-emitter [CA3081] or common-collector [CA3082] configuration*
- *High I_C: 100 mA max.*
- *Low V_{CE} sat (at 50 mA): 0.4 V typ.*

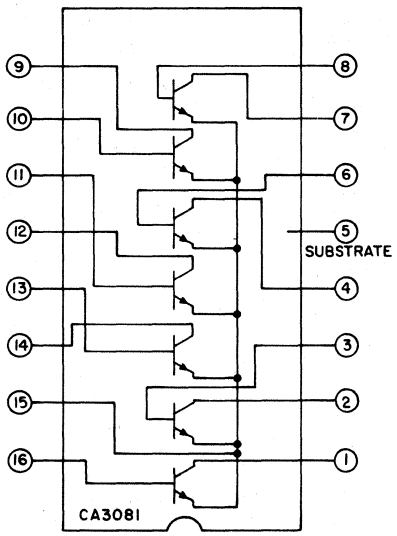
Applications:

- *Drivers for:*
  - *Incandescent display devices [e.g. RCA NUMITRON DR2000 Series and lamps]*
  - *LED [e.g. RCA-40736R GaAs High-Efficiency Emitting Diode]*
  - *Relay control*
  - *Thyristor firing*

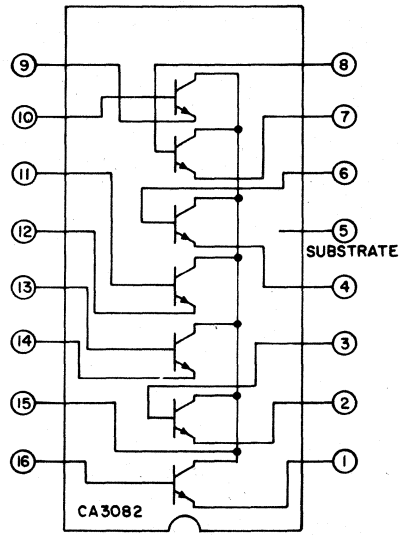
RCA-CA3081 and CA3082 consist of seven high-current (to 100 mA) silicon n-p-n transistors on a common monolithic substrate. The CA3081 is connected in a common-emitter configuration and the CA3082 is connected in a common-collector configuration.

The CA3081 and CA3082 are capable of directly driving seven-segment displays, such as the RCA NUMITRON devices (DR2000 and DR2010), and light-emitting diode (LED) displays. These types are also well-suited for a variety of other drive applications, including relay control and thyristor firing.

The CA3081 and CA3082 are supplied in a 16-lead dual-in-line plastic package, and the CA3081F and CA3082F in a 16-lead dual-in-line frit-seal ceramic package, which includes a separate substrate connection for maximum flexibility in circuit design. Both types are also available in chip form.



(a)
COMMON-EMITTER CONFIGURATION
92CS-17958



(b)
COMMON-COLLECTOR CONFIGURATION
92CS-17957

Fig. 1 — Functional diagrams of types CA3081 and CA3082.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:		
Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to + 150	°C
Lead Temperature (During Soldering):		
At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 seconds max.	265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO})	16	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})*	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

* The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CES}$	I_C = 500 μA, I_E = 0	–	20	60	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 500 μA, I_E = 0, I_B = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	16	24	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_C = 500 μA	–	5	6.9	–	V
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 0.5 V, I_C = 30 mA	–	30	68	–	
		V_{CE} = 0.8 V, I_C = 50 mA	–	40	70	–	
Base-to-Emitter Saturation Voltage	$V_{BE\ sat}$	I_C = 30 mA, I_B = 1 mA	3	–	0.87	1.0	V
Collector-to-Emitter Saturation Voltage: CA3081, CA3082	$V_{CE\ sat}$	I_C = 30 mA, I_B = 1 mA	–	–	0.27	0.5	V
CA3081		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.7	
CA3082		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.8	
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	–	–	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	–	1	μA

CA3081, CA3082 Types

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR OF TYPES CA3081 AND CA3082

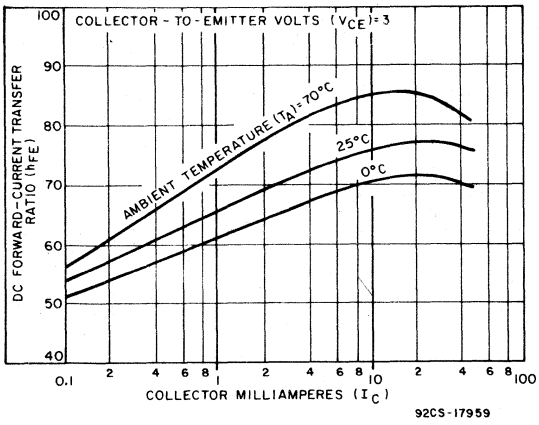


Fig.2—h_{FE} vs. I_C

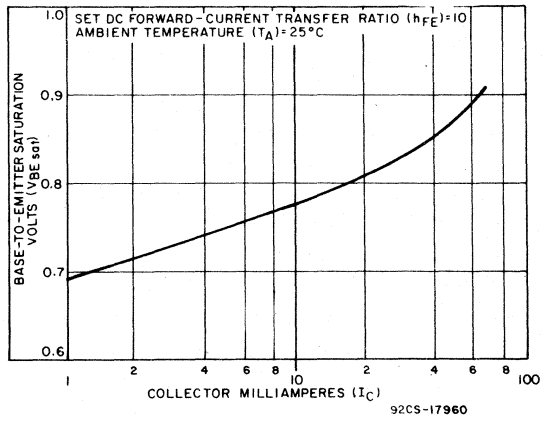


Fig.3—V_{BEsat} vs. I_C

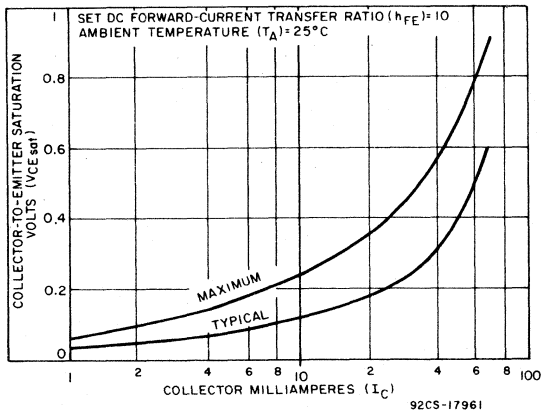


Fig.4—V_{CEsat} vs. I_C at T_A = 25°C.

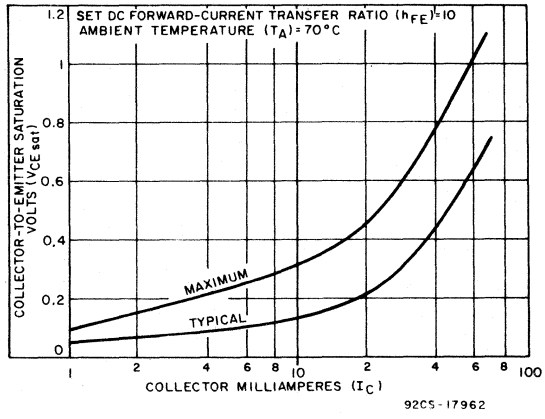


Fig.5—V_{CEsat} vs. I_C at T_A = 70°C.

TYPICAL READ-OUT DRIVER APPLICATIONS

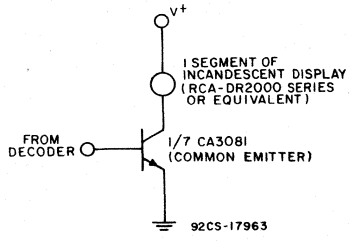
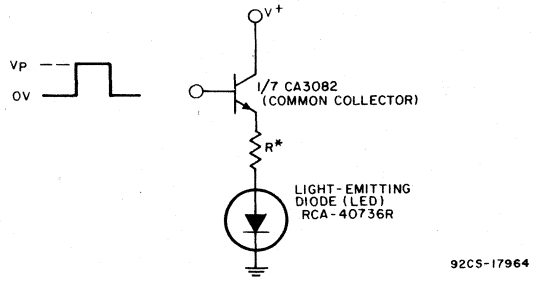


Fig.6—Schematic diagram showing one transistor of the CA3081 driving one segment of an incandescent display.



*THE RESISTANCE FOR R IS DETERMINED BY THE RELATIONSHIP

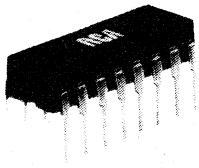
$$R = \frac{V_P - V_{BE} - V_F(LED)}{I\,(LED)}$$

WHERE: V_P = INPUT PULSE VOLTAGE

V_F = FORWARD VOLTAGE DROP ACROSS THE DIODE

$R = 0$ FOR $V_P = V_{BE} + V_F(LED)$

Fig.7—Schematic diagram showing one transistor of the CA3082 driving a light-emitting diode (LED).



16-Lead Dual-In-Line Plastic Package H-1622

BCD-to-Seven-Segment Decoder/Driver

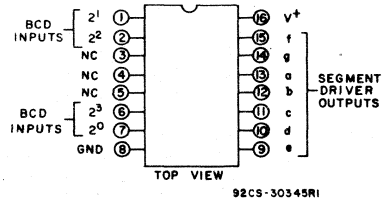
Features:

- *TTL-compatible input logic levels*
- *25-mA [typ.] constant-current segment outputs*
- *Eliminates need for output current-limiting resistors*
- *Pin compatible with other industry standard decoders*
- *Low standby power dissipation – 18 mW (typ.)*

The RCA-CA3161E is a monolithic intergrated circuit that performs the BCD-to-seven-segment decoding function and features constant-current segment drivers. When used with the CA3162E A/D Converter* the CA3161E provides a complete digital readout system with a minimum number of external parts.

The CA3161 is supplied in the 16-lead dual-in-line plastic package (E suffix). The CA3161 is also available in chip form (H suffix).

*The CA3162E is described in RCA data bulletin File No. 1080.



TERMINAL ASSIGNMENT
CA3161E

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (between terminals 1 and 10) ..... +7 V

INPUT VOLTAGE (terminals 1, 2, 6, 7) ..... +5.5 V

OUTPUT VOLTAGE:

Output "Off" ..... +7 V

Output "On" (See note 1) ..... +10 V

DEVICE DISSIPATION:

Up to T_A = +55°C ..... 1 W

Above T_A = +55°C ..... derate linearly at 10.5 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... 0 to +75°C

Storage ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

NOTE 1: This is the maximum output voltage for any single output. The output voltage must be consistent with the maximum dissipation and derating curve for worst-case conditions. Example: All segments "on", 100% duty cycle.

CA3161E

TRUTH TABLE

BINARY STATE	INPUTS				OUTPUTS							DISPLAY
	2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	
0	L	L	L	L	L	L	L	L	L	L	H	0
1	L	L	L	H	H	L	L	H	H	H	H	1
2	L	L	H	L	L	L	H	L	L	H	L	2
3	L	L	H	H	L	L	L	L	H	H	L	3
4	L	H	L	L	H	L	L	H	H	L	L	4
5	L	H	L	H	L	H	L	L	H	L	L	5
6	L	H	H	L	L	H	L	L	L	L	L	6
7	L	H	H	H	L	L	L	H	H	H	H	7
8	H	L	L	L	L	L	L	L	L	L	L	8
9	H	L	L	H	L	L	L	L	H	L	L	9
10	H	L	H	L	H	H	H	H	H	H	L	—
11	H	L	H	H	L	H	H	L	L	L	L	E
12	H	H	L	L	H	L	L	H	L	L	L	H
13	H	H	L	H	H	H	H	L	L	L	H	L
14	H	H	H	L	L	L	H	H	L	L	L	P
15	H	H	H	H	H	H	H	H	H	H	H	BLANK

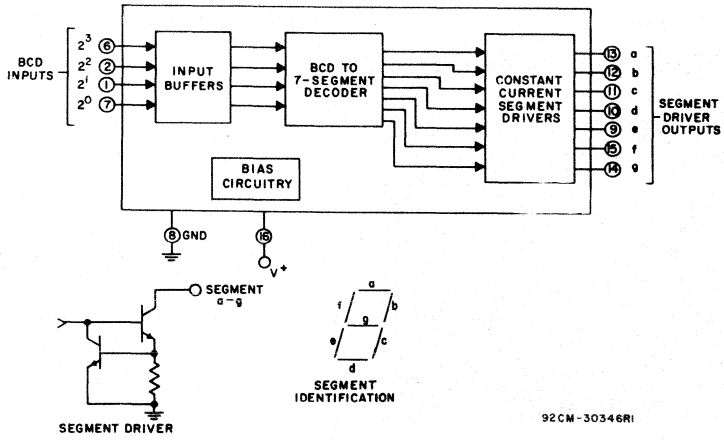
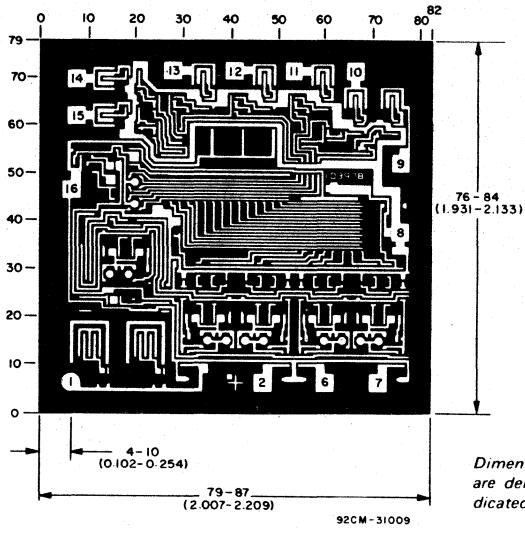


Fig. 1-Functional block diagram of the CA3161E.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTIC		LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Voltage Operating Range, V^+		4.5	5	5.5	V
Supply Current, I^+ (all inputs high)		–	3.5	8	mA
Output Current Low (V_O = 2 V)		18	25	32	mA
Output Current High (V_O = 5.5 V)		–	–	250	μA
Input Voltage High (logic "1" level)		2	–	–	V
Input Voltage Low (logic "0" level)		–	–	0.8	V
Input Current High (logic "1")	2 V	–30	–	–	μA
Input Current Low (logic "0")	0 V	–40	–	–	μA
Propagation Delay Time	t_{PHL}	–	2.6	–	μs
	t_{PLH}	–	1.4	–	

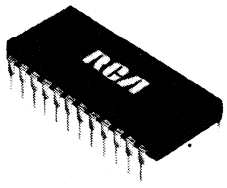
CA3161E



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for the CA3161H.



24-Lead Dual-In-Line Plastic Package

H-1855

2-Digit BCD-to-7-Segment Decoder/Driver

For Common-Anode LED Displays

Features

- *Separate BCD inputs and segment outputs for each digit*
- *Input loading less than 15 μA*
- *I^2L logic with buffered inputs and outputs*
- *Internal input overrange protection circuit*
- *5-V supply operation*
- *Internal biasing circuits*
- *Output drive capability of 25 mA per segment*
- *Open collector outputs drive indicators directly*

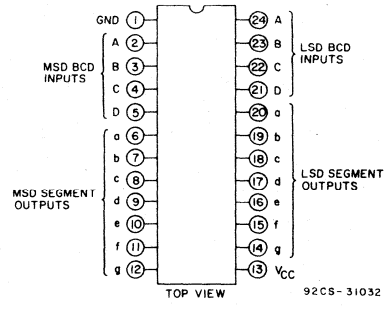
The RCA-CA3168E• is a monolithic integrated circuit intended for 2-digit display such as "numbers" for TV and "CB" channel selection, and other 0-99 numerical or counting for consumer or industrial indicator applications. It consists of two independent BCD-to-7-segment decoder/drivers. Two sets of BCD inputs are buffered with p-n-p differential amplifier stages internally referenced to 1.7 V. Each of the eight input terminals draws less than 15 μA and is provided with an internal protection circuit.

Decoding is accomplished with I^2L ROM's. The fourteen output terminals are buffered with Darlington pairs driving common-emitter output transistors. Each output is capable of sinking 25 mA for an LED common-anode display device. The supply-voltage range (V_{CC}) is intended to be 4.5 V to 6 V. The output voltage (V_O) must not exceed 12 V, which provides for a wide range of common-anode voltage sources.

The CA3168E is supplied in the 24-lead dual-in-line plastic package.

•Formerly RCA Dev. Type No. TA10337

CA3168E
TERMINAL ASSIGNMENT



MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY-VOLTAGE, V_{CC} ..... 6 V
INPUT-VOLTAGE (MIN./MAX.) ..... $-0.3/V_{CC}$ V
INPUT CURRENT (PROTECTION CIRCUIT) ..... ±10 mA
OUTPUT VOLTAGE, V_O ..... 12 V
OUTPUT SEGMENT CURRENT, $I_{DISPLAY}$ ..... 25 mA
AMBIENT TEMPERATURE RANGE:
  Operating ..... 0 to +70°C
  Storage ..... -55 to +150°C
POWER DISSIPATION:
  Up to +70°C ..... 400 mW
  Above +70°C ..... derate linearly at 8.7 mW/°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for
  10 seconds max. ..... +265°C

CA3168E

TYPICAL ELECTRICAL CHARACTERISTICS at V_{CC} = 5 V, V_1 = GND, $V_{DISP.}$ = 12 V, and T_A = 25°C, See Fig. 2
Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Input Voltage High, V_{IH}		2.4	5	V_{CC}	V
Input Voltage Low, V_{IL}		0	–	0.6	V
Input Current High, I_{IH}	All BCD Inputs = 5 V	–	–	15	μA
Input Current Low, I_{IL}	All BCD inputs = 0 V	−10	–	–	μA
On-State Output Voltage, V_{OL}	$I_{O(Sink)}$ = 25 mA	–	–	1	V
Off-State Output Current, I_{OH}		–	5	50	μA
Power Supply Drain Current, I_{CC}	V_{CC} = 6 V	–	17	25	mA
Input Capacitance, C_I		–	5	–	pF

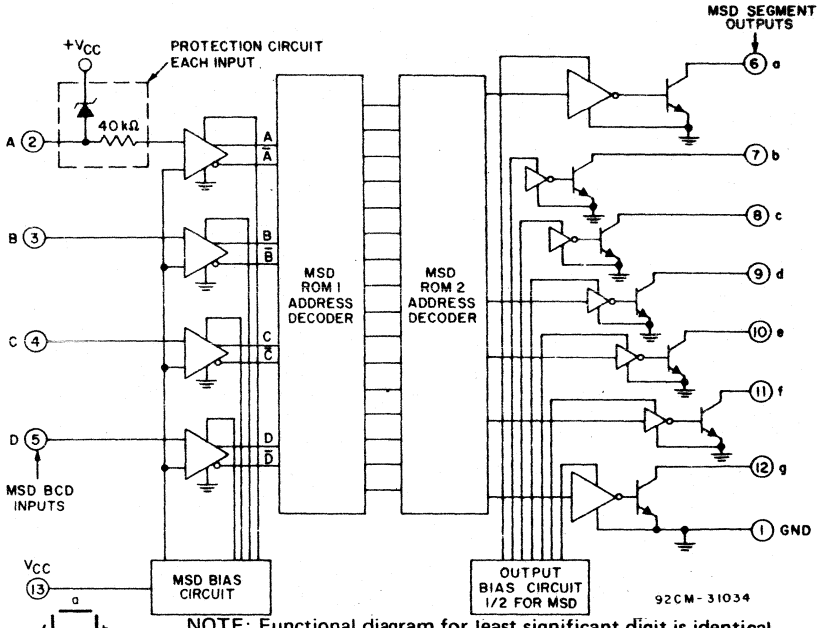
TRUTH TABLES

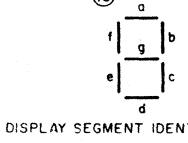
Most Significant Digit (MSD)

INPUTS	OUTPUTS							DISPLAY
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	0	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	0	1	0	0	9
1	0	1	0	0	1	1	0	0	0	1	C
1	0	1	1	0	0	0	1	0	0	0	A
1	1	0	0	0	0	1	1	0	0	0	P
1	1	0	1	0	1	1	0	0	0	0	E
1	1	1	0	1	1	1	1	1	1	0	–
1	1	1	1	1	1	1	1	1	1	1	BLANK

Least Significant Digit (LSD)

INPUTS	OUTPUTS							DISPLAY
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	0	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	0	1	0	0	9
1	0	1	0	1	0	0	1	0	0	0	H
1	0	1	1	1	0	0	0	0	1	1	J
1	1	0	0	1	1	1	0	0	0	1	L
1	1	0	1	0	1	1	1	0	0	0	F
1	1	1	0	1	1	1	1	1	1	0	–
1	1	1	1	1	1	1	1	1	1	1	BLANK

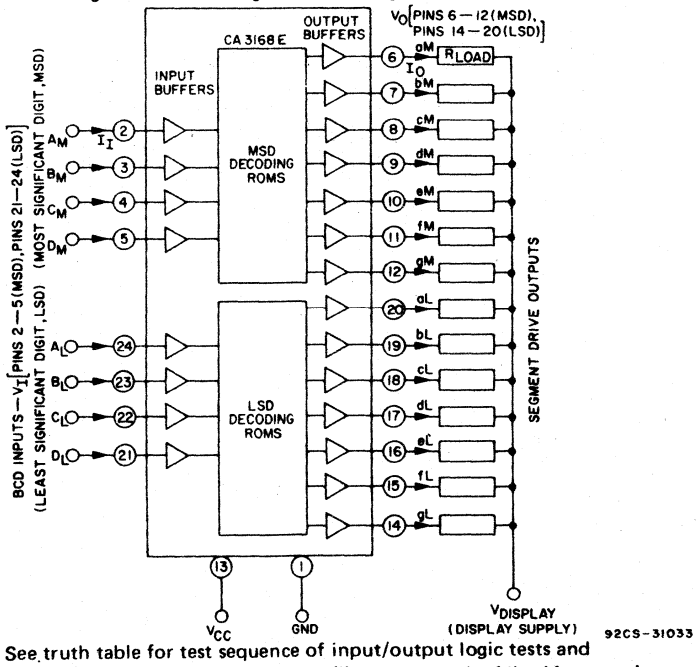




DISPLAY SEGMENT IDENTIFICATION

NOTE: Functional diagram for least significant digit is identical to functional diagram used for MSD with the exception of Terminal Assignments (see Terminal Assignment diagram). A separate LSD Bias circuit, and ½ of the Output Bias Circuit is used for LSD.

Fig. 1 - Functional diagram for Most Significant Digit (MSD).



NOTE: See truth table for test sequence of input/output logic tests and

Minimum $R_{LOAD} = \frac{V_{DISPLAY} - V_{OL}}{\text{Max. } I_{DISPLAY}}$ **for each of the 14 segment**

drive output terminals. (LED is not used in test circuit)

Fig. 2 - Test circuit.

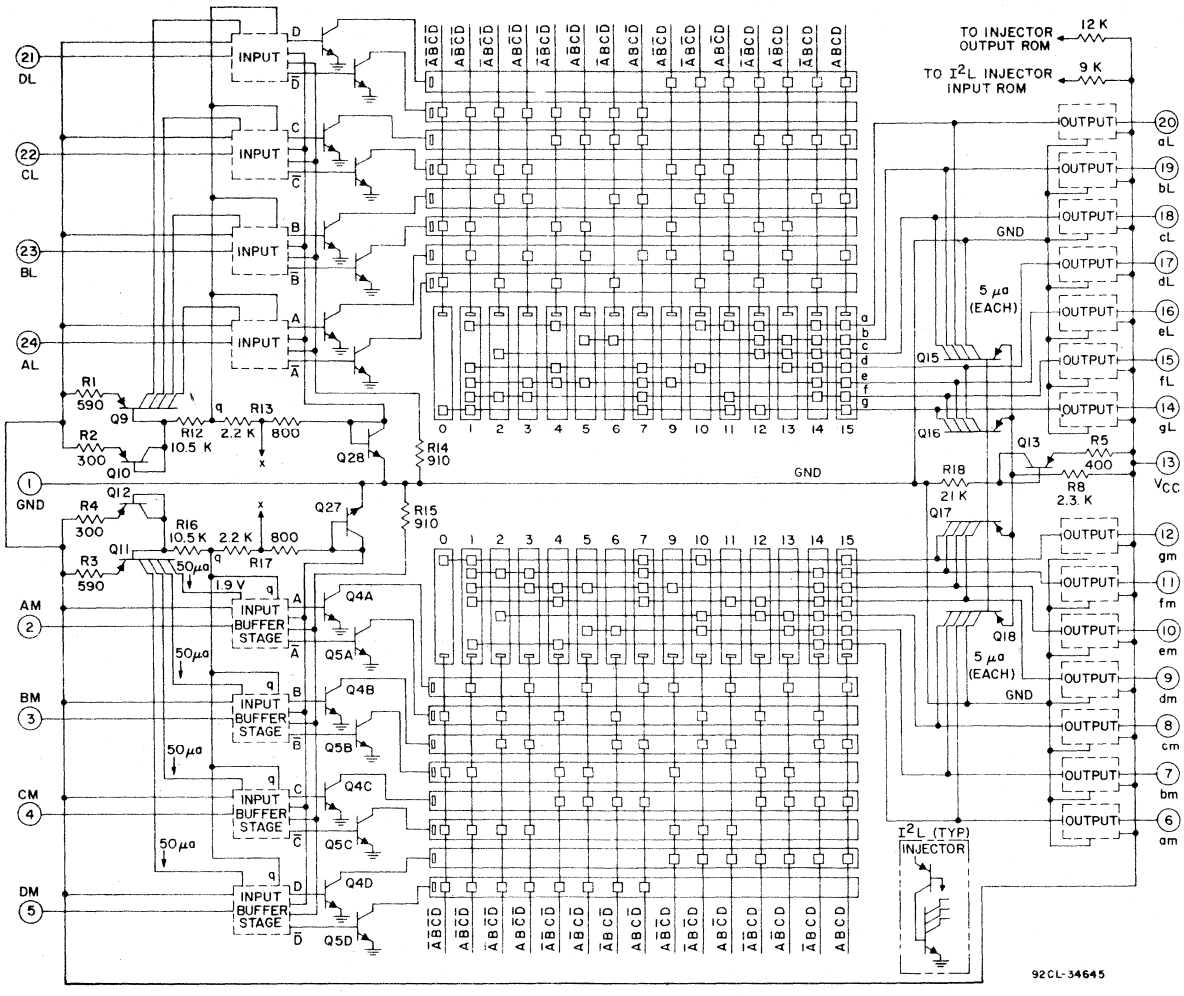


Fig. 3 - Schematic diagram of CA3168E.

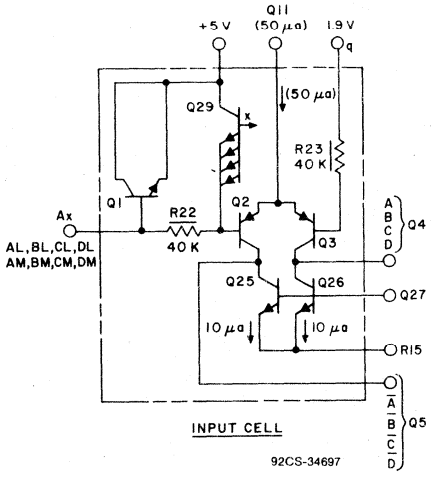


Fig. 4 - Schematic diagram of CA3168E input cell.

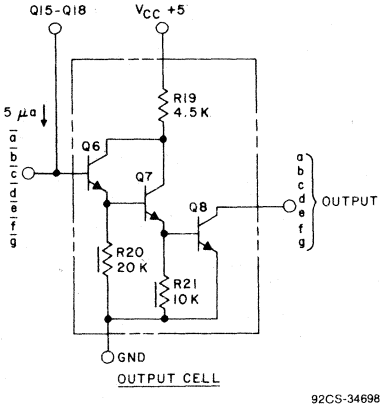


Fig. 5 - Schematic diagram of CA3168E output cell.

CA3207E, CA3208E

H-1917

22-Lead Dual-In-Line Plastic Package (E)

BiMOS Sequencer Driver and Segment Latch-Driver for Vacuum Fluorescent Displays

Features:
- *Serial input, parallel output*
- *Total of 14 outputs*
- *CMOS and T^2L compatible inputs*
- *Low-power CMOS Logic–Bipolar high-voltage output BiMOS process*
- *Use with vacuum fluorescent display*
- *Will operate in an output voltage range of 35 V to 55 V*

Sequencer Driver (CA3207E)
- *Sequentially turns on 1 of 14 characters (or 2 of 28 when used with 2 CA3208E's)*
- *Signal dimming through Gates 1 or 2*

Latch Driver (CA3208E)
- *Drives any combination of 14 outputs selected by DATA input*
- *Two or more devices may be interconnected by means of the CE and $\overline{CE}$ inputs to drive more than 14 characters*

The RCA-CA3207E and CA3208E★, sequence-driver and segment latch-driver, respectively, are used in combination to drive vacuum fluorescent display devices of up to 14 segments with up to 14 characters of display. The CA3207E selects the digit or character to be displayed in sequence and the CA3208E turns on the required number of segments of the character selected.

Each sequencer-driver will sequentially activate 14 characters. The sequencer-driver clock line may be used to drive the cross-coupled $\overline{CE}$ and CE inputs of 2 segment-latch drivers to provide for the display of up to 28 characters (see Fig. 12). The logic portion of both circuits use CMOS technology operating at 5 volts. The output drivers use bipolar technology and operate at supply voltages up to 55 volts. The CA3207E will source 40-mA per character and the CA3208E will source 7.5-mA per segment.

Both types are supplied in the 22-lead dual-in-line plastic package (E suffix), and they are also available in chip form (H suffix).

★Formerly Dev. Type No. TA10563 and TA10564, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:

V_{CC}, Pin 3 to GND, Pin 10	55 V
V_{DD}, Pin 4 to GND, Pin 10	6 V

DEVICE DISSIPATION:

Up to T_A=+85°C	750 mW
Above T_A=+85°C	13 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating	-40 to +85°C
Storage	-55 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	265°C

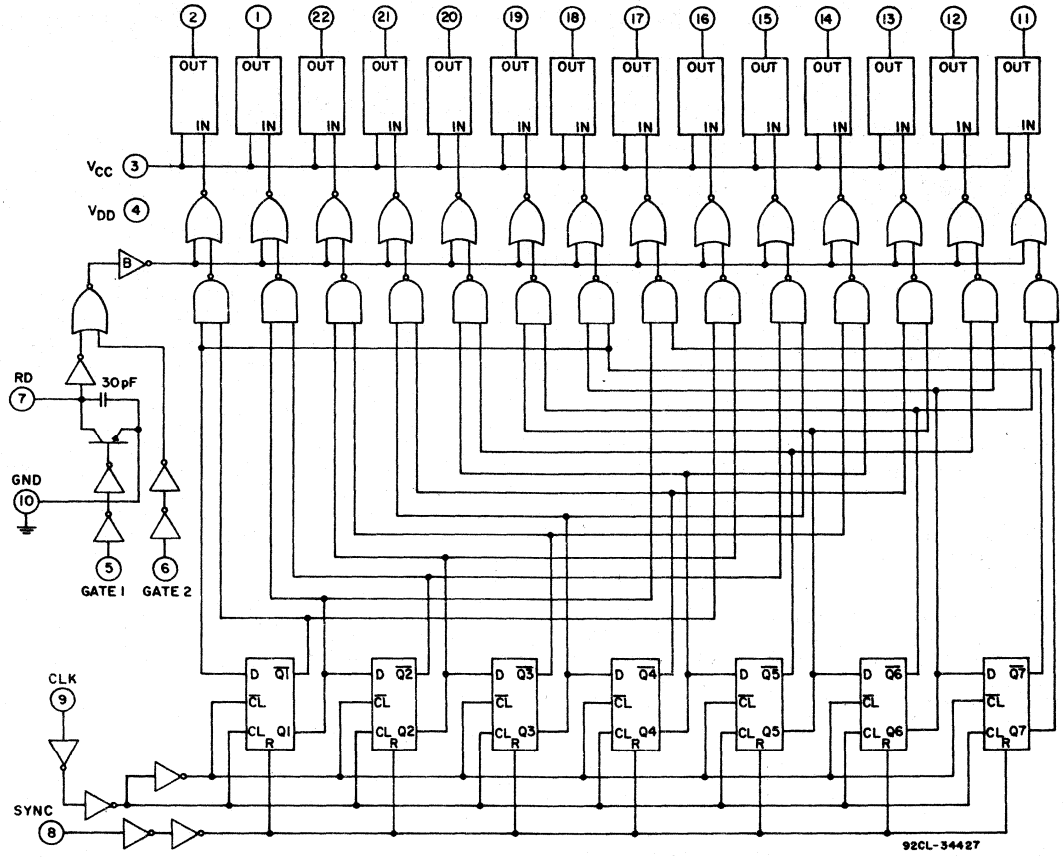
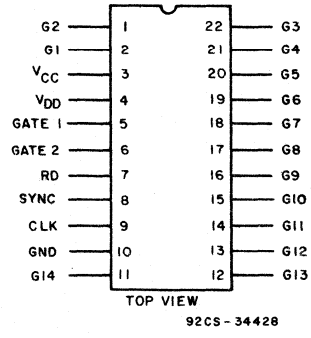


Fig. 1 - Sequencer-driver (CA3207E) logic diagram.



TERMINAL ASSIGNMENT
CA3207E

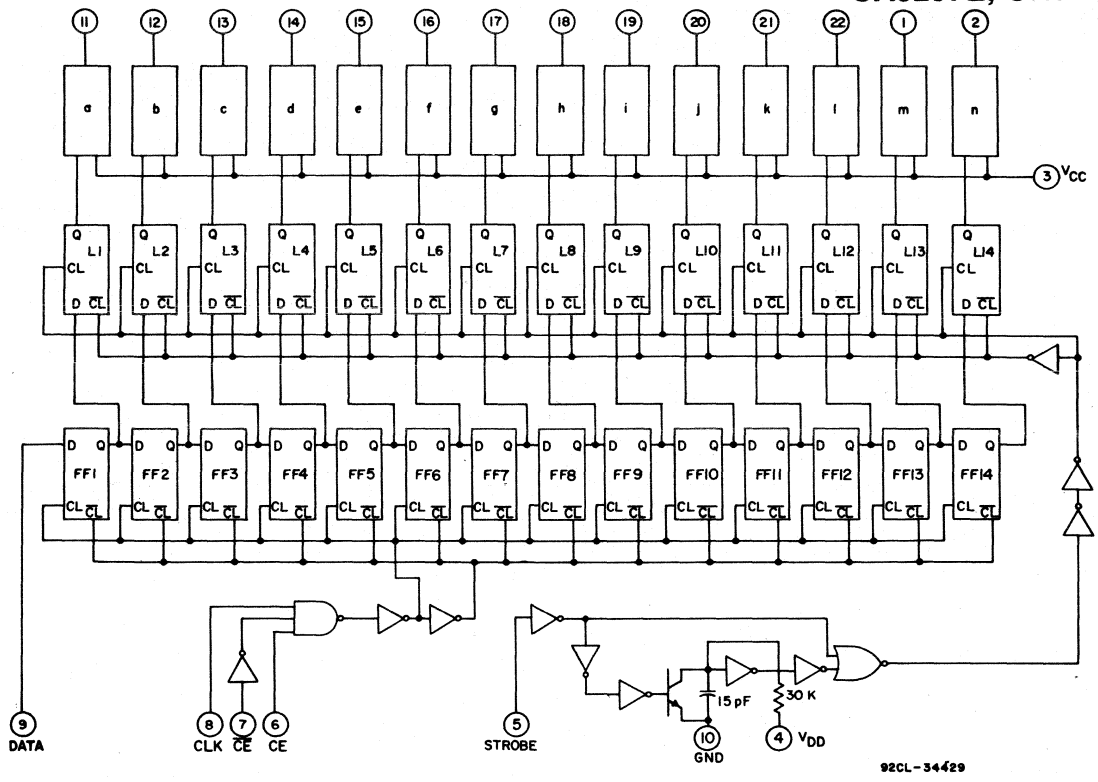
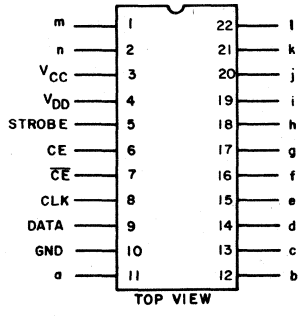


Fig. 2 - Segment-latch driver (CA3208E) logic diagram.

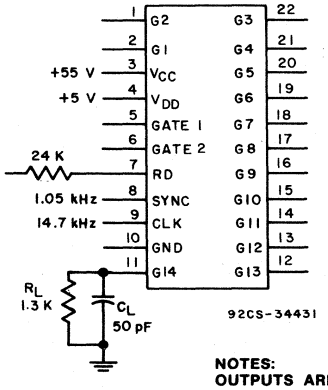


TERMINAL ASSIGNMENT
CA3208E

CA3207E, CA3208E

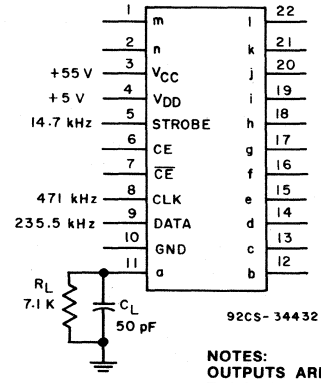
STATIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=+55 V, V_{DD}=+5 V, C_L=50 pF, See Fig. 3 and Fig. 4.

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			CA3207E		CA3208E		
			Min.	Max.	Min.	Max.	
V_{CC} Supply Current	I_{CC}	No outputs "ON"	—	10	—	—	mA
		Half outputs HIGH "ON"	—	—	—	65	
V_{DD} Supply Current	I_{DD}	All inputs HIGH	—	1	—	—	mA
		All inputs LOW	—	—	—	800	μA
		All inputs HIGH	—	—	—	1	
Input Current, Low-Level	I_{IL}	V_{IN}=0 V	—	1	—	1	μA
Input Current, High-Level	I_{IH}	V_{IN}=5 V	—	1	—	1	
Output Voltage, Low-Level	V_{OL}	R_L=1.3K	—	1	—	—	V
		R_L=7.1K	—	—	—	1	
Output Voltage, High-Level	V_{OH}	I_{OH}=40 mA	53	—	—	—	
		I_{OH}=7.5 mA	—	—	53	—	
Input Low Voltage	V_{IL}		—	1.5	—	1.5	V
Input High Voltage	V_{IH}		3.5	—	3.5	—	



NOTES:
OUTPUTS ARE PINS 1, 2 AND 11 THROUGH 22.
OUTPUT LOADS ARE R_L (1.3 K) AND C_L (50 pF) WHICH RESULTS IN A 40-mA LOAD CURRENT.
INPUT VOLTAGE LEVELS ARE 0 V and 5 V.

Fig. 3 - Sequencer-driver (CA3207E) test circuit.



NOTES:
OUTPUTS ARE PINS 1, 2 AND 11 THROUGH 22.
OUTPUT LOADS ARE R_L (7.1 K) AND C_L (50 pF) WHICH RESULTS IN A 7.5-mA LOAD CURRENT.
INPUT VOLTAGE LEVELS ARE 0 V AND 5 V.

Fig. 4 - Segment-latch driver (CA3208E) test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=+55 V, V_{DD}=+5 V, C_L=50 pF, R_L=1.3K

CHARACTERISTIC		LIMITS CA3207E Min.	LIMITS CA3207E Max.	UNITS
Sequencer-Driver, See Fig. 5				
Sync Pulse Width	t_{SW}	2	—	μs
Time Delay Gate 1:				
Input-to-Output Inhibit	t_{GI}	—	1.5	μs
Input-to-Output Enable	t_{GE}	—	2.3	μs
Lead Time Sync to Gate	t_{SG}	0.5	—	μs
Lead Time Clock to Gate	t_{CG}	0.5	—	μs
Clock Frequency	f_{CL}	—	14	kHz

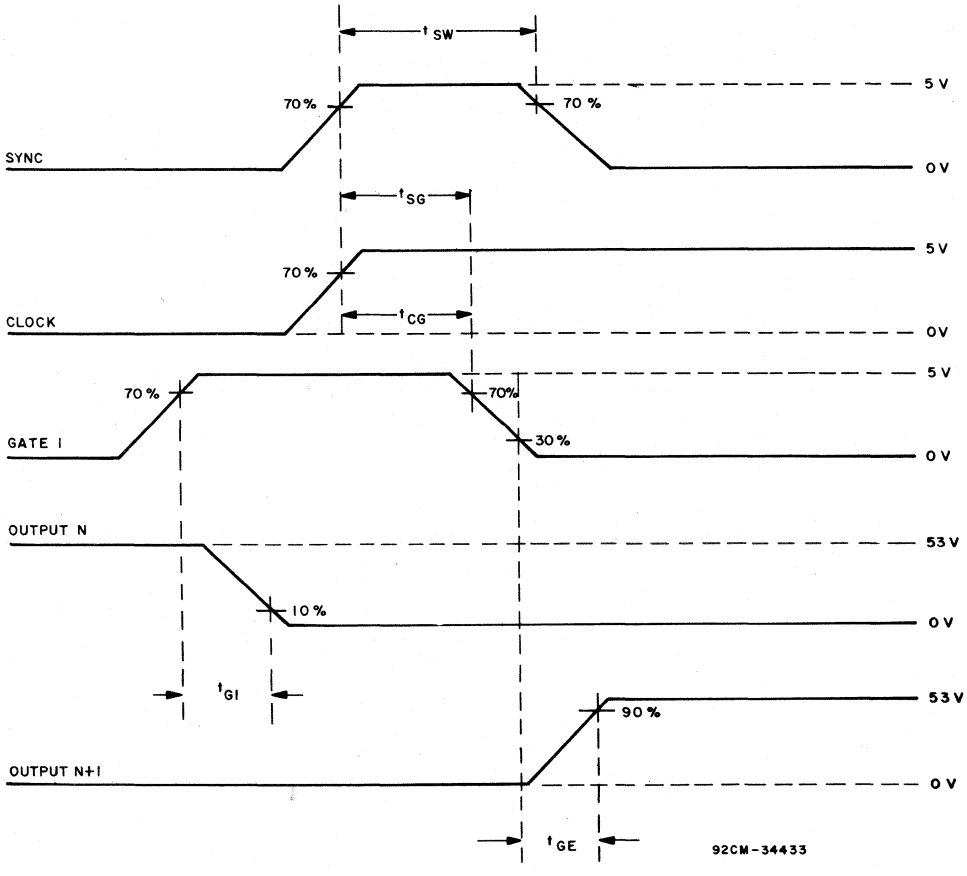


Fig. 5 - Sequencer-driver (CA3207E) timing waveforms.

CA3207E, CA3208E

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=+55 V, V_{DD}=+5 V, C_L= 50 pF, R_L=7.1 K

CHARACTERISTIC		LIMITS CA3208E Min.	LIMITS CA3208E Max.	UNITS
Segment-Latch Driver, See Fig. 6				
Time Delay:				
Strobe to Output	t_{PLH}	0.4	1.8	
Strobe to Output	t_{PHL}	—	2.6	μs
CE or $\overline{CE}$ to Clock	t_{CE}	0.8	—	
Input Data Set-Up Time	t_{SU}	0.5	—	μs
Input Data Hold Time	t_H	0.5	—	
Clock Frequency	f_{CL}	—	448	kHz
Data Frequency	f_D	—	224	

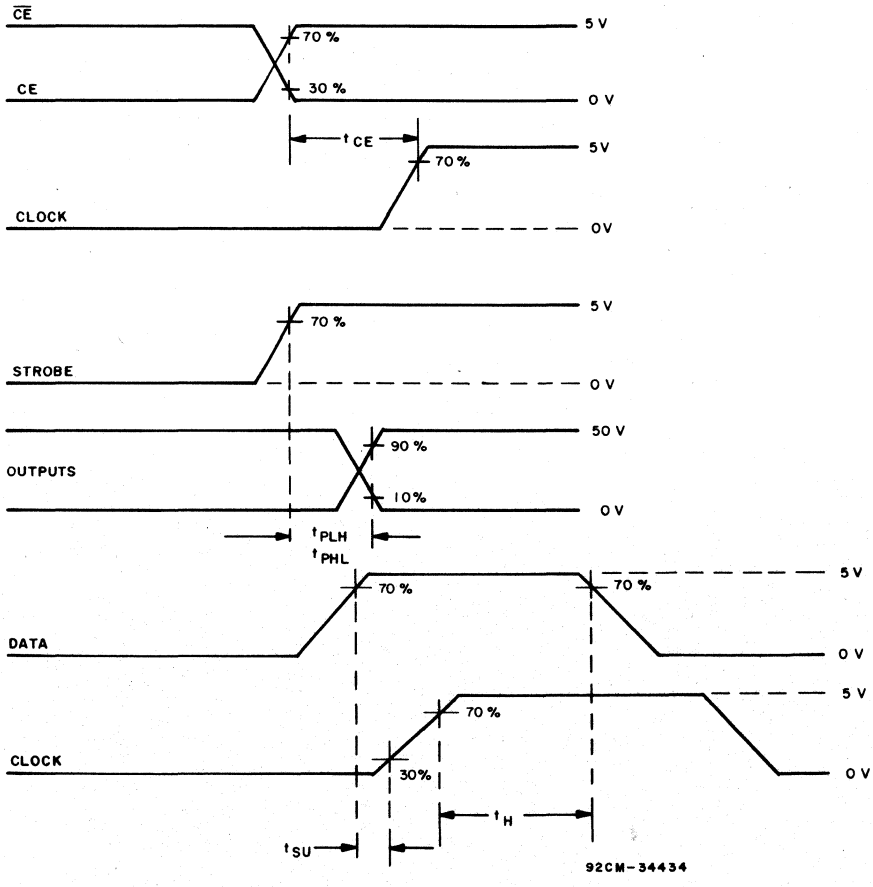


Fig. 6 - Segment-latch driver (CA3208E) timing waveforms.

Circuit Descriptions

Sequencer-Driver (CA3207E)

The CA3207E circuit consists of a 7-stage Johnson counter, which is reset by the positive transition of the sync pulse and which is clocked on the positive transitions of the clock pulse. The outputs of the counter are decoded to turn on one output driver at a time in sequence, for the period of one clock pulse (normally 70 μs). The 14 output drivers are each capable of sourcing 40 mA of current and in a typical application will be connected to the grids of a vacuum fluorescent display, thereby performing a digit select function on a display of up to 14 characters. All outputs are set to zero by the application of a positive "1" level to either of the gate terminals, 5 and 6. The action of the 7-stage counter is unaffected by the presence of inhibit levels on the gate terminals. The gate terminals can be used for a controlled power down or for chopping where display dimmer is desired. The only difference between the two terminals is that gate 1, pin 5, has a delayed falling edge, which delays the release of the output drivers for a time determined by the value of the resistor connected between pin 7 and V_{DD}.

Segment-Latch Driver (CA3208E)

This circuit consists of a 14-bit shift register accepting serial data at pin 9 at a typical rate of 224 kHz and being clocked on the rising edge of the 448-kHz clock signal.

The leading edge of a 14-kHz strobe signal generates an internal strobe pulse through the one shot, which shifts the data, in parallel, from the shift register to the output latches, which in turn set the output drivers to the corresponding state. There are 14 output drivers, each capable of driving 7.5-mA at 55 volts, simultaneously. The drivers are normally connected to the anodes or segments of the vacuum fluorescent display. In a multi-character display, all corresponding segments in each character would be linked together. Activation of a particular character is made by the CA3207E Sequencer-Driver turning on the appropriate output and raising the grid of the display to a positive value.

Clock Enable (CE) and Clock Enable Not ($\overline{CE}$) pins are available for use in system applications. The first enables the chip with a logic level "1" and the second with a logic level"0".

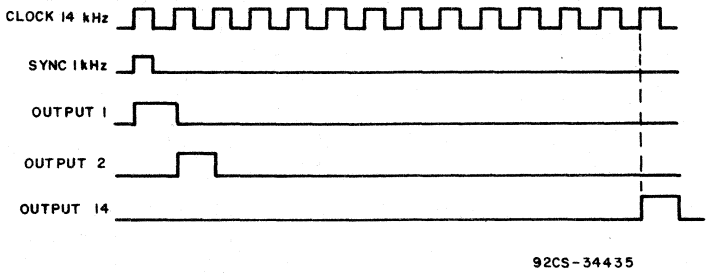


Fig. 7 - Sequencer driver (CA3207E) timing waveforms.

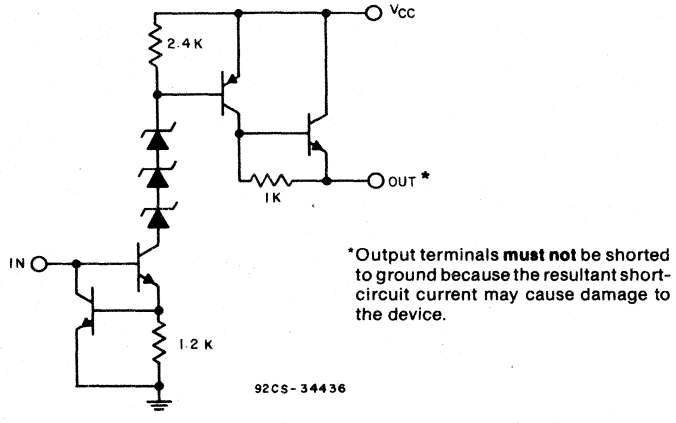


Fig. 8 - Sequencer driver (CA3207E) output circuit.

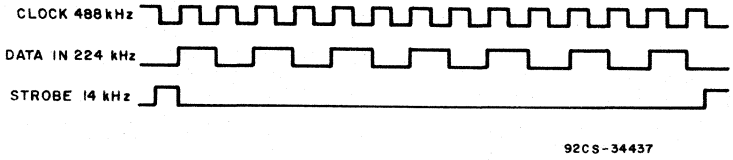
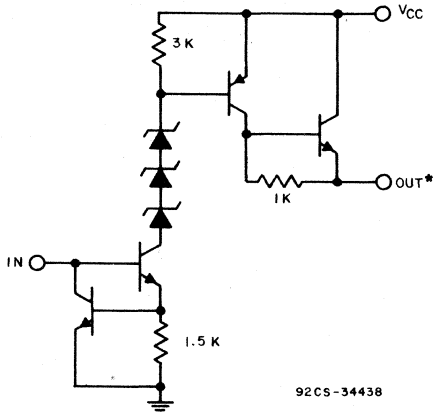


Fig. 9 - Segment-latch driver (CA3208E) timing waveforms.



*Output terminals **must not** be shorted to ground because the resultant short-circuit current may cause damage to the device.

Fig. 10 - Segment latch-driver (CA3208E) output circuit.

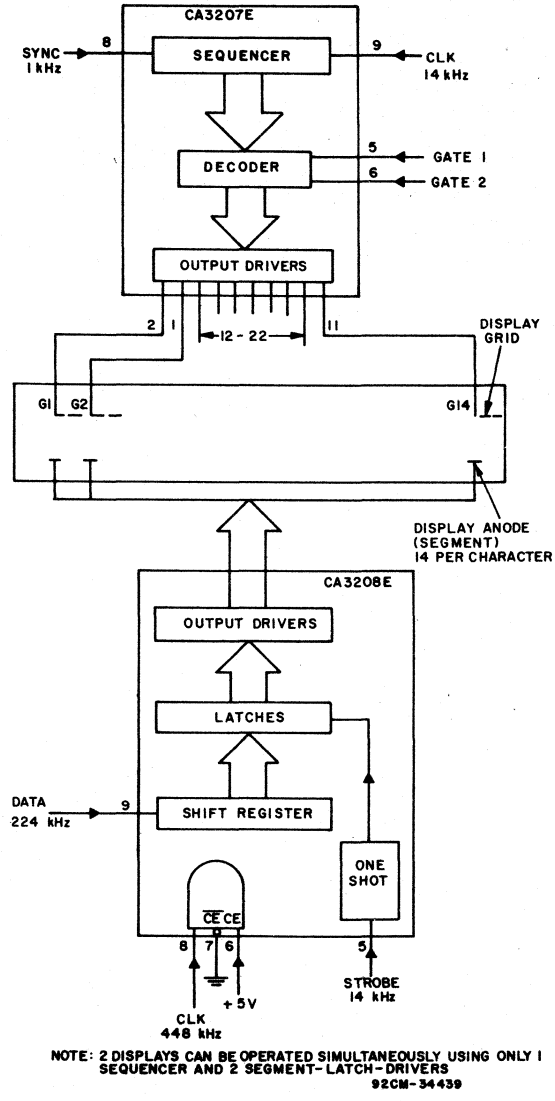


Fig. 11 - Typical systems application of the CA3207E and CA3208E display circuits.

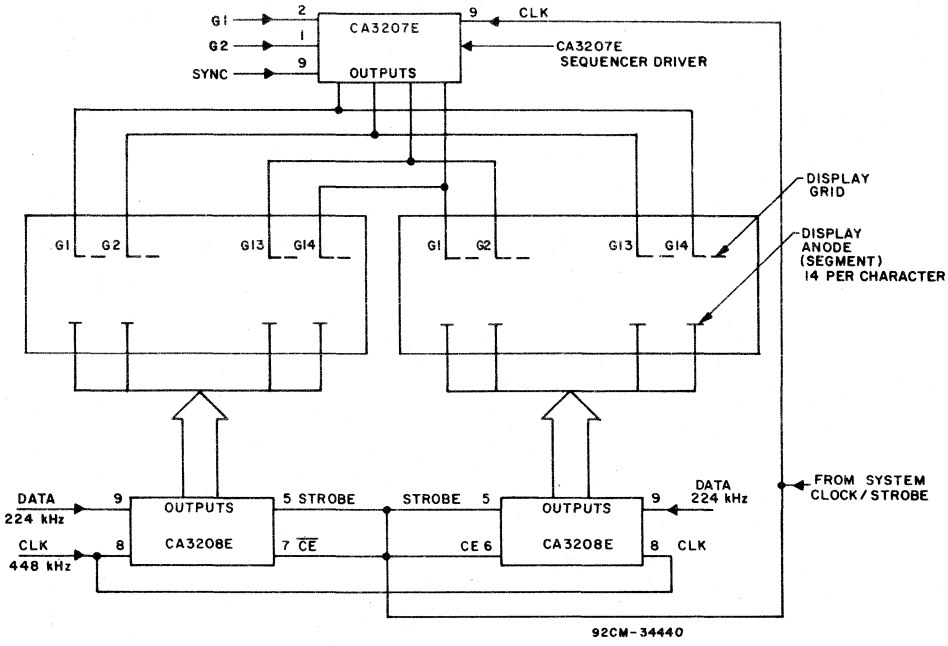
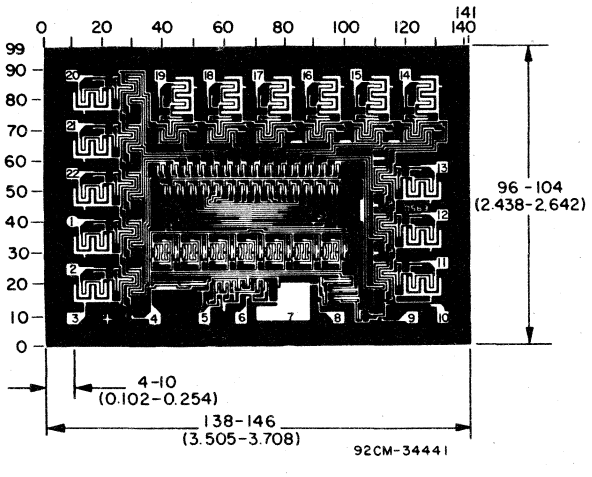
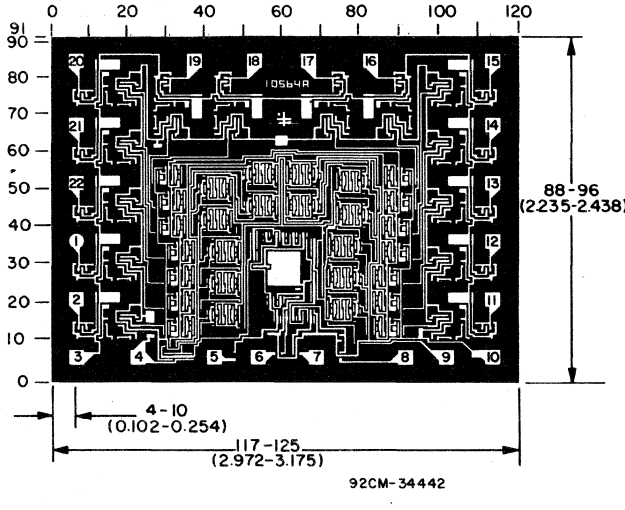


Fig. 12 - Typical systems application of the CA3207E and 2 CA3208E circuits for a total 28-character display.



Dimensions and pad layout for the CA3207H.



Dimensions and pad layout for the CA3208H.

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Arrays
Technical Data

Amplifier/ Diode

Transistor

5

ΔCMOS types

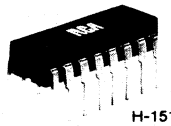
CA3026, CA3054

CA3026

H-1463

12-Lead TO-5

CA3054



H-1517

14-Lead Dual-In-Line Plastic Package

Transistor Array - Dual Independent Differential Amplifiers

For Low Power Applications at Frequencies from DC to 120 MHz

Features

- *Two differential amplifiers on a common substrate*
- *Independently accessible inputs and outputs*
- *Maximum input offset voltage - ± 5 mV*
- *Full military temperature-range capability - −55°C to +125°C*
- *Limited temperature range - 0°C to 85°C for CA3054*

The CA3026 and CA3054 each consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six n-p-n transistors which comprise the amplifiers are general-purpose devices which exhibit low 1/f noise and a value of f_T in excess of 300 MHz. These features make the CA3026 and CA3054 useful from dc to 120 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3026 and CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3026 is supplied in a hermetic 12-lead TO-5-style package and is rated for full military operating-temperature range of −55°C to +125°C.

The CA3054 is supplied in a 14-lead plastic dual-in-line package with a limited temperature range. The availability of extra terminals allows the introduction of an independent substrate connection for maximum flexibility.

Applications

- *Dual sense amplifiers*
- *Dual Schmitt triggers*
- *Multifunction combinations - RF/Mixer/Oscillator; Converter/IF*
- *IF amplifiers (differential and/or cascode)*
- *Product detectors*
- *Doubly balanced modulators and demodulators*
- *Balanced quadrature detectors*
- *Cascade limiters*
- *Synchronous detectors*
- *Pairs of balanced mixers*
- *Synthesizer mixers*
- *Balanced (push-pull) cascode amplifiers*

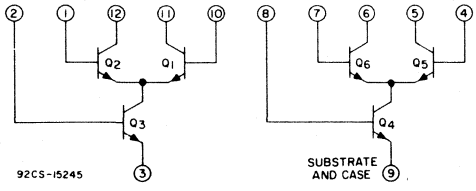


Fig.1a - Schematic Diagram for CA3026.

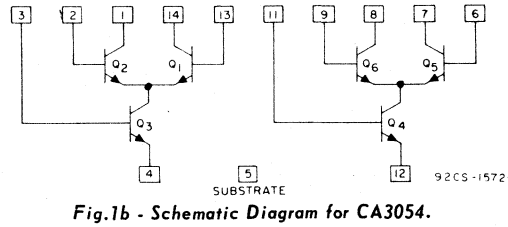


Fig.1b - Schematic Diagram for CA3054.

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device. See Maximum Voltage Ratings chart.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C

Power Dissipation, P:	CA3026	CA3054	
Any one transistor	300	300	mW
Total package	600	750	mW
For T_A > 55°C	Derate at 5	6.67	mW/°C
Temperature Range:			
Operating	-55 to + 125	-40 to +85	°C
Storage	-65 to + 150	-65 to +150	°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3026 and CA3054 is isolated from the substrate by an integral diode. *The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.*

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 1† and horizontal terminal 3† is +15 to -5 volts.

† For CA3026; corresponding terminals for CA3054 are vertical terminal 2 and horizontal terminal 4.

CA3054 TERMINAL No. →		13	14	1	2	3	4	6	7	8	9	11	12	5
↓	CA3026 → TERMINAL No. ↓	10	11	12	1	2	3	4	5	6	7	8	Note 1 9	Note 1 9
13	10		0 -20	*	+5 -5	*	+15 -5	*	*	*	*	*	*	*
14	11			*	*	*	+20 0	*	*	*	*	*	*	+20 0
1	12				+20 0	*	+20 0	*	*	*	*	*	*	+20 0
2	1					*	+15 -5	*	*	*	*	*	*	*
3	2						+1 -5	*	*	*	*	*	*	*
4	3							*	*	*	*	*	*	*
6	4								0 -20	*	+5 -5	*	+15 -5	*
7	5									*	*	*	*	+20 0
8	6										+20 0	*	*	+20 0
9	7											*	+15 -5	*
11	8												+1 -5	*
12	9													*
5	9													Ref Sub-strate

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Note 1: In the CA3026 terminal No.9 is connected to the emitter of Q_4, the reference substrate, and the case; therefore, the case should not be grounded. Two terminal 9 columns (CA3026) appear in the voltage rating chart because it is a composite chart for both the CA3026 and the CA3054. Wherever an asterisk is shown in one column 9 and a rating is shown in the other column 9, the asterisk should be ignored.

Maximum Current Ratings

CA3054 TERMINAL No.●	CA3026 TERMINAL No.	I_{IN} mA	I_{OUT} mA
13	10	5	0.1
14	11	50	0.1
1	12	50	0.1
2	1	5	0.1
3	2	5	0.1
4	3	0.1	-50
6	4	5	0.1
7	5	50	0.1
8	6	50	0.1
9	7	5	0.1
11	8	5	0.1
12	9	0.1	50

● Terminal No.10 of CA3054 is not used

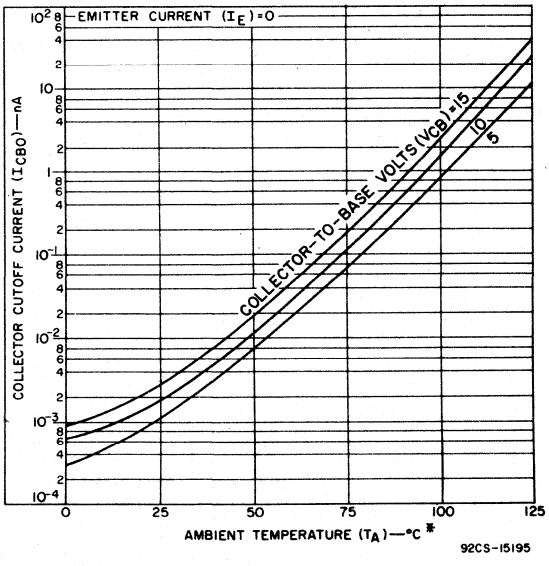
CA3026, CA3054

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	CA3026 CA3054 LIMITS			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC CHARACTERISTICS								
For Each Differential Amplifier								
Input Offset Voltage	V_{IO}	V_{CB} = 3 V $I_{E(Q3)} = I_{E(Q4)}$ = 2 mA	-	-	0.45	5	mV	6
Input Offset Current	I_{IO}		-	-	0.3	2	μA	7
Input Bias Current	I_I		-	-	10	24	μA	3
Quiescent Operating Current Ratio	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$ or $\frac{I_{C(Q5)}}{I_{C(Q6)}}$		-	-	0.98 to 1.02	-	-	3
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		-	-	1.1	-	μV/°C	5
For Each Transistor								
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CB} = 3 V, I_C = 50 μA	-	-	0.630	0.700	V	6
		I_C = 1 mA	-	-	0.715	0.800		
		I_C = 3 mA	-	-	0.750	0.850		
		I_C = 10 mA	-	-	0.800	0.900		
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3 V, I_C = 1 mA	-	-	-1.9	-	μV/°C	4
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	-	0.002	100	nA	2
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	-	15	24	-	V	-
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	-	20	60	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	-	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	-	5	7	-	V	-
DYNAMIC CHARACTERISTICS								
Common-Mode Rejection Ratio For Each Amplifier	CMR	V_{CC} = 12 V V_{EE} = -6 V V_X = -3.3 V f = 1 kHz	8a	-	100	-	dB	8b
AGC Range, One Stage	AGC		9a	-	75	-	dB	9b
Voltage Gain, Single Stage Double-Ended Output	A		9a	-	32	-	dB	9b
AGC Range, Two Stage	AGC		10a	-	105	-	dB	10b
Voltage Gain, Two Stage Double-Ended Output	A		10a	-	60	-	dB	10b
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (For Single Transistor)								
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	-	110	-	-	11
Short-Circuit Input Impedance	h_{ie}		-	-	3.5	-	kΩ	11
Open-Circuit Output Impedance	h_{oe}		-	-	15.6	-	μmho	11
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	-	1.8×10^{-4}	-	-	11

DYNAMIC CHARACTERISTICS CONT'D.								
1/f Noise Figure (For Single Transistor)	NF	f = 1 kHz, V_{CE} = 3 V	-	-	3.25	-	dB	-
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 3 V, I_C = 3 mA	-	-	550	-	MHz	12
Admittance Characteristics; Differential Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Each Collector $I_C \approx$ 1.25 mA f = 1 MHz	-	-	-20+j0	-	mmho	13a
Input Admittance	y_{11}		-	-	0.22+j0.1	-	mmho	13b
Output Admittance	y_{22}		-	-	0.01+j0	-	mmho	13c
Reverse Transfer Admittance	y_{12}		-	-	-0.003 +j0	-	mmho	13d
Admittance Characteristics; Cascode Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Total Stage $I_C \approx$ 2.5 mA f = 1 MHz	-	-	68-j0	-	mmho	14a
Input Admittance	y_{11}		-	-	0.55+j0	-	mmho	14b
Output Admittance	y_{22}		-	-	0+j0.02	-	mmho	14c
Reverse Transfer Admittance	y_{12}		-	-	0.004-j0.005	-	μmho	14d
Noise Figure	NF	f = 100 MHz	-	-	8	-	dB	-

TYPICAL STATIC CHARACTERISTICS



* For CA3054: use data from 0°C to 85°C only

Fig.2 - Collector-to-base cutoff current vs ambient temperature for each transistor.

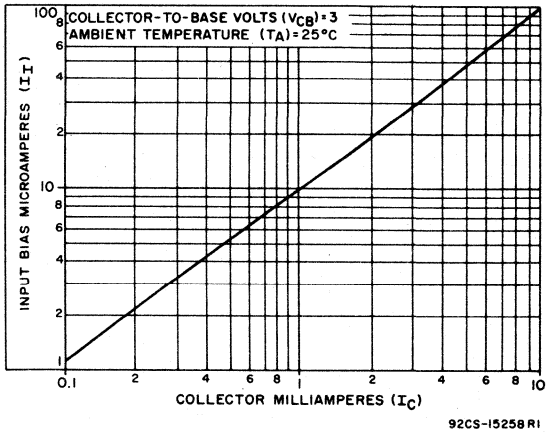


Fig.3 - Input bias current characteristic vs collector current for each transistor.

TYPICAL STATIC CHARACTERISTICS

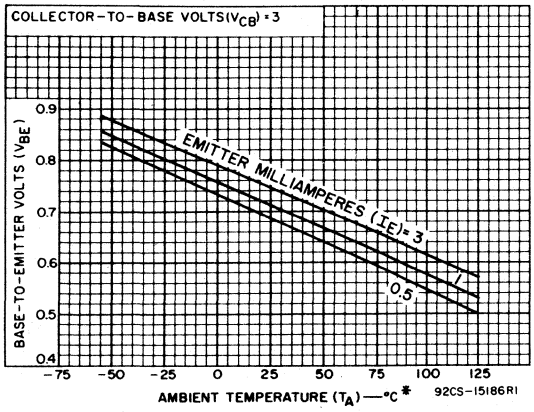


Fig.4 - Base-to-emitter voltage characteristic for each transistor vs ambient temperature.

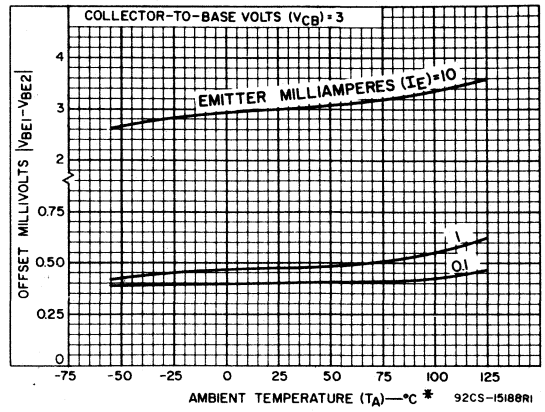


Fig.5 - Offset voltage characteristic vs ambient temperature for differential pairs.

* For CA3054: use data from 0°C to 85°C only

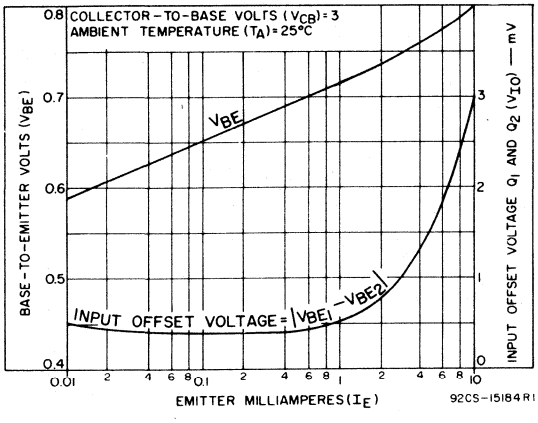


Fig.6 - Static base-to-emitter voltage characteristic and input offset voltage for differential pairs vs emitter current.

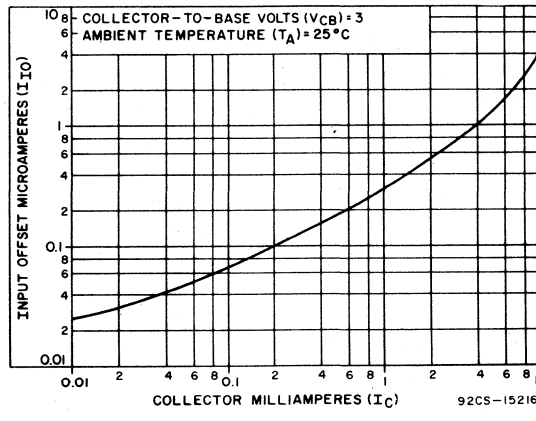
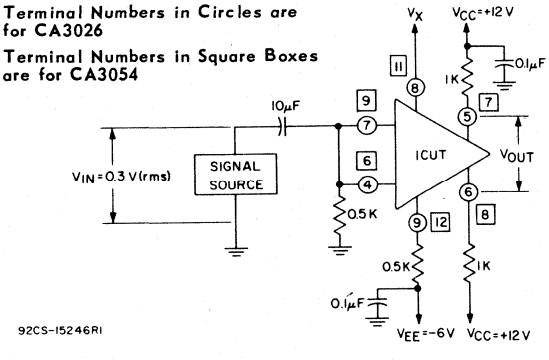


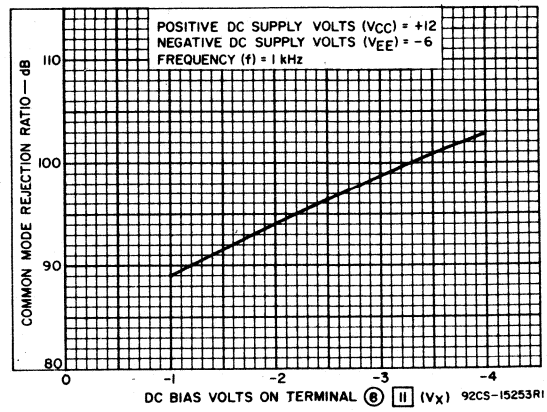
Fig.7 - Input offset current for matched differential pairs vs collector current.

TYPICAL DYNAMIC CHARACTERISTICS

COMMON MODE REJECTION RATIO



(a) Test setup

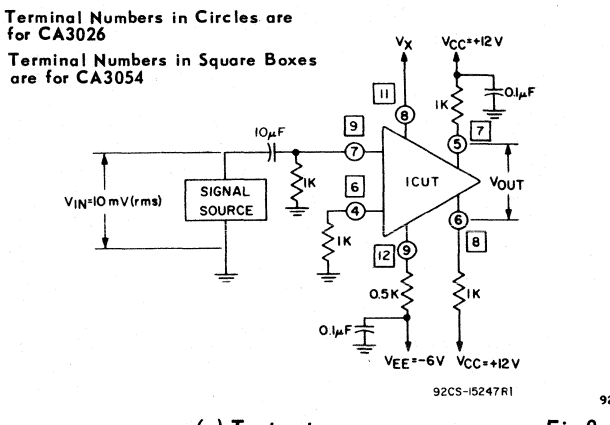


(b) Characteristic

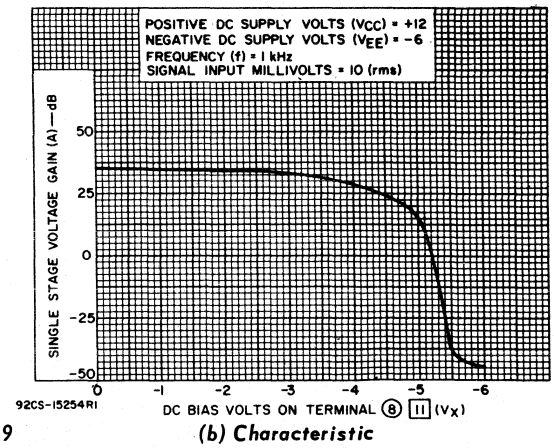
Fig.8

TYPICAL DYNAMIC CHARACTERISTICS (cont'd)

SINGLE-STAGE VOLTAGE GAIN



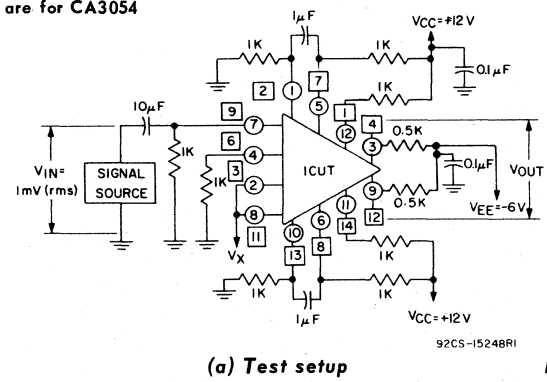
(a) Test setup



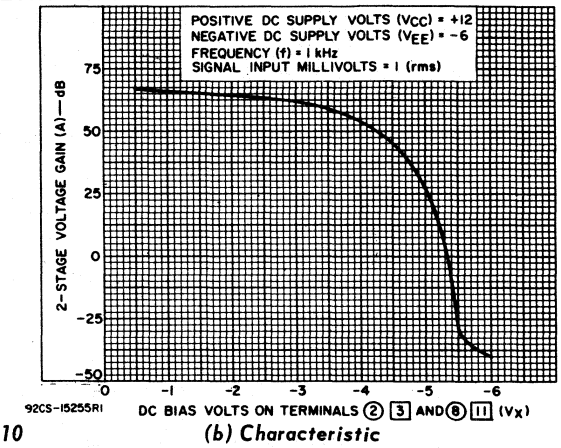
(b) Characteristic

Fig.9

TWO-STAGE VOLTAGE GAIN



(a) Test setup



(b) Characteristic

Fig.10

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

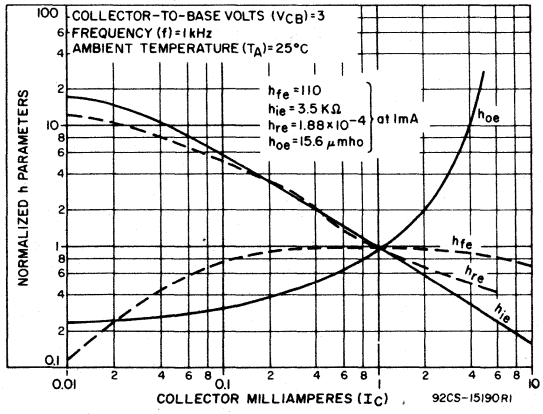


Fig.11 - Forward current-transfer ratio (h_{fe}), short-circuit input impedance (h_{ie}), open-circuit output impedance (h_{oe}), and open-circuit reverse voltage-transfer ratio (h_{re}) vs collector current for each transistor.

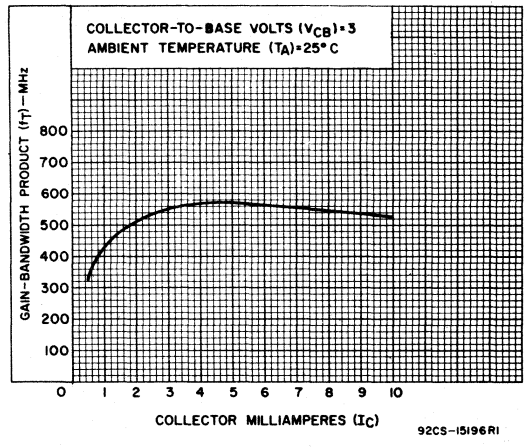


Fig.12 - Gain-bandwidth product (f_T) vs collector current.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER

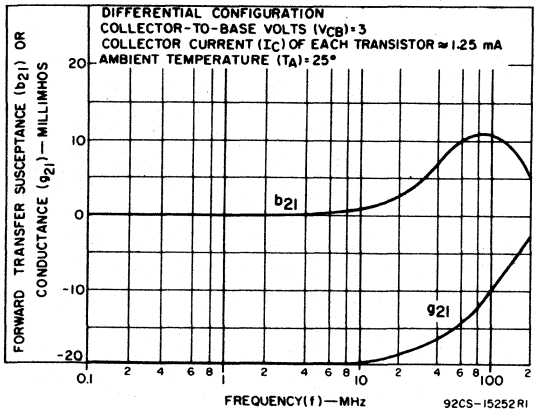


Fig.13(a) - Forward transfer admittance (Y_{21}) vs frequency.

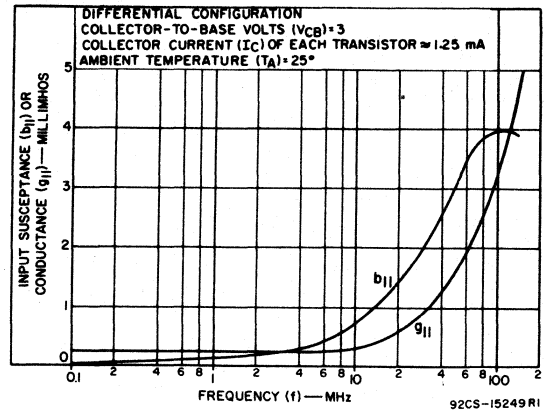


Fig.13(b) - Input admittance (Y_{11}).

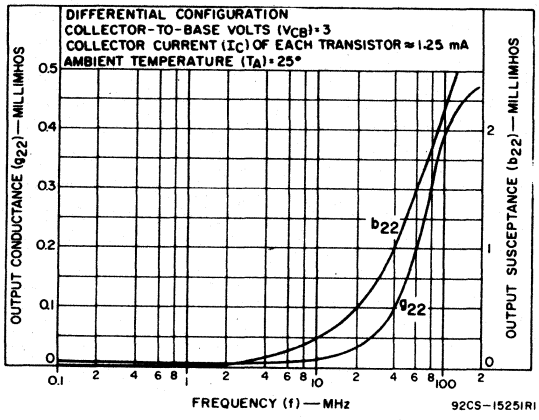


Fig.13(c) - Output admittance (Y_{22}) vs frequency.

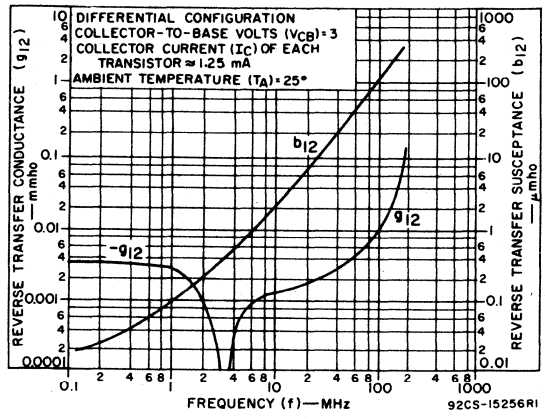


Fig.13(d) - Reverse transfer admittance (Y_{12}) vs frequency.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH CASCODE AMPLIFIER

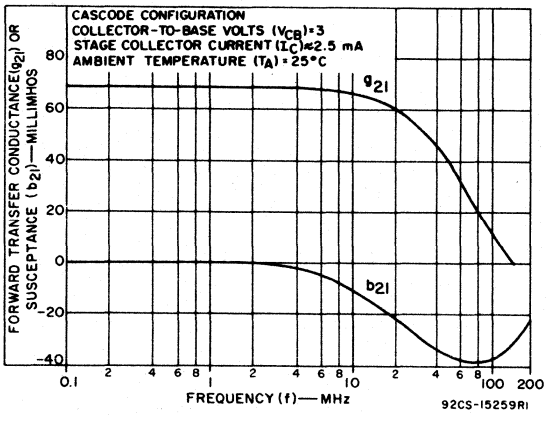


Fig.14(a) - Forward transfer admittance (Y_{21}) vs frequency.

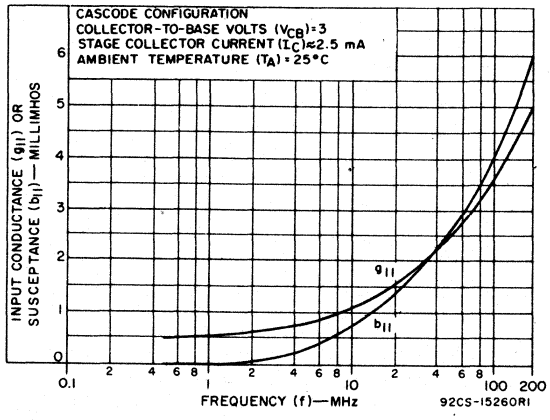


Fig.14(b) - Input admittance (Y_{11}) vs frequency.

TYPICAL CHARACTERISTICS FOR EACH CASCODE AMPLIFIER (cont'd)

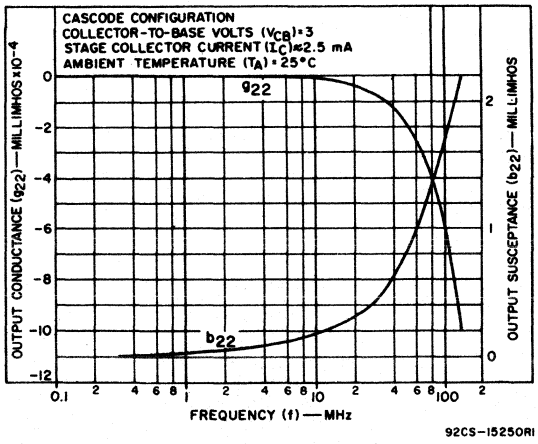


Fig.14(c) - Output admittance (Y_{22}) vs frequency.

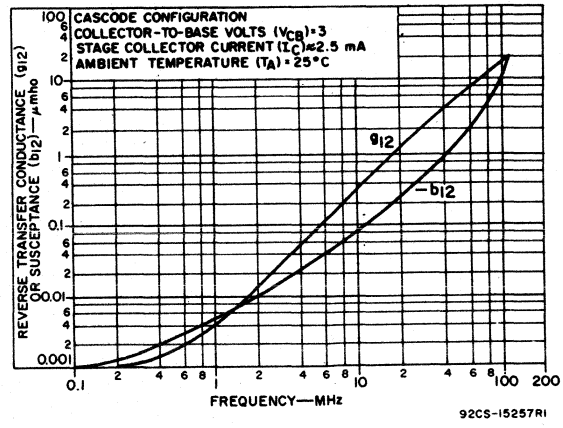


Fig.14(d) - Reverse transfer admittance (Y_{12}) vs frequency.

CA3035, CA3035V1

10-Lead TO-5

H-1384

Ultra-High-Gain Wide-Band Amplifier Array

Features:

- *Three separate amplifiers - gain and bandwidth for each amplifier can be adjusted with suitable external circuitry*
- *Amplifiers operable independently or in cascade*
- *Exceptionally high cascade voltage gain - 129 dB typ. at 40 kHz*
- *Low noise performance*
- *Wide-band response*
- *All amplifiers single-ended - only one power supply required*
- *Wide operating temperature range - -55° C to +125° C*
- *Built-in temperature compensation*
- *Hermetically sealed, all-welded 10-lead TO-5 style metal package with straight or formed leads*

Applications:

- *Three individual general-purpose amplifiers*
- *Ideal for service in remote-control amplifiers - e.g., TV receivers*
- *Available in two electrically identical versions: CA3035 with straight leads; CA3035V1 with formed leads*

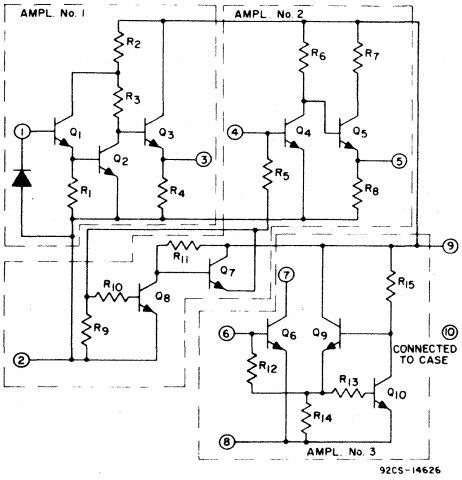


Fig. 1 — Schematic Diagram for CA3035 and CA3035V1

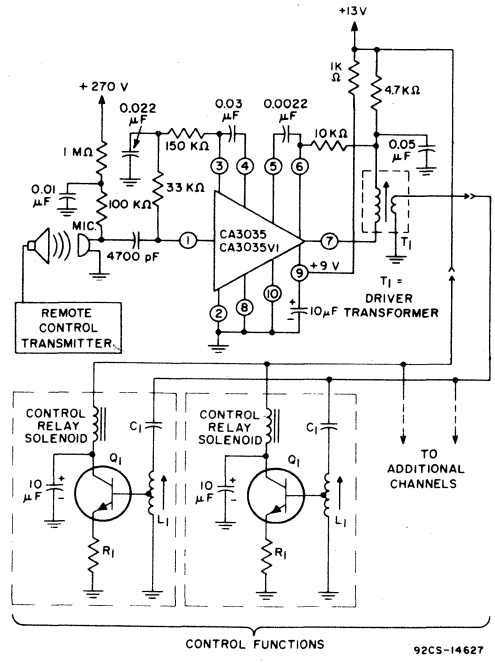


Fig. 2 — Typical Remote Control System

ABSOLUTE-MAXIMUM RATINGS:

Operating Temperature Range . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +200°C
Device Dissipation . . . . . 300 mW
Input Voltage . . . . . 1 V p-p
Supply Voltage . . . . . +15 V

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	TEST CIRCUITS AND CHARAC-TERISTICS CURVES	LIMITS CA3035, CA3035V1 Min.	Typ.	Max.	UNITS
STATIC CHARACTERISTICS							
Quiescent Operating Voltage	V3 V5 V7	V_{CC} = +9V	Fig.3	– – –	2 1.9 4.9	– – –	V V V
Total Current Drain	I_d	V_{CC} = +9V, R_{L3} = 5KΩ	Fig.3	3.5	5	7.5	mA
DYNAMIC CHARACTERISTICS							
Voltage Gain: Amplifier No.1 Amplifier No.2 Amplifier No.3	 A_1 A_2 A_3	 f = 40 kHz, V_{CC} = +9V		 40 40 38	 44 46 42	 – – –	 dB dB dB
Output Voltage Swing	V_{out} V_{1out} V_{2out} V_{3out}	 R_{L1} = 10KΩ R_{L2} = 10KΩ R_{L3} = 5KΩ Sinusoidal Output, V_{CC} = +9V		 – – –	 2 2.6 8	 – – –	 Vp-p Vp-p Vp-p
Input Resistance: Amplifier No.1 Amplifier No.2 Amplifier No.3	 R_1in R_2in R_3in	 f = 40 kHz		 – – –	 50K 2K 670	 – – –	 Ω Ω Ω
Output Resistance	R_1out R_2out R_3out	 f = 40 kHz		 – – –	 270 170 100K	 – – –	 Ω Ω Ω
Bandwidth at -3dB point: Amplifier No.1 Amplifier No.2 Amplifier No.3	 BW_1 BW_2 BW_3	 V_{CC} = +9V	 Fig.5 Fig.6 Fig.7	 – – –	 500 2.5 2.5	 – – –	 kHz MHz MHz
Noise Figure Amplifier No.1	 NF_1	 f = 1 kHz, R_S = 1 KΩ	 Fig.4	 –	 6	 7	 dB
Sensitivity		V_{CC} = +13 V Relay (K_1) Current = 7.5 mA	Fig.2	–	100	150	μV

STATIC CHARACTERISTICS

TEST CIRCUIT

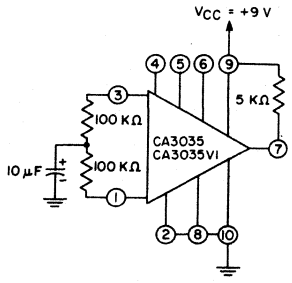
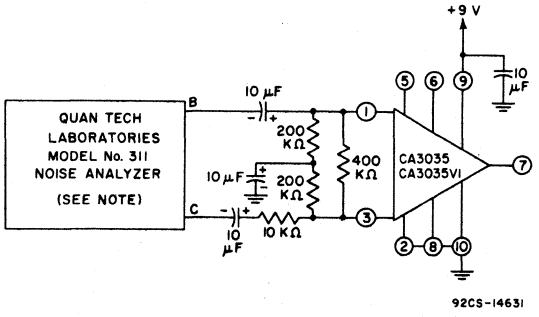


Fig.3

NOISE FIGURE TEST CIRCUIT



NOTE: SET ALL INTERNAL POWER SUPPLIES ON QUAN TECH NOISE ANALYZER TO ZERO VOLTS.

Fig.4

TYPICAL 1st-AMPLIFIER RESPONSE

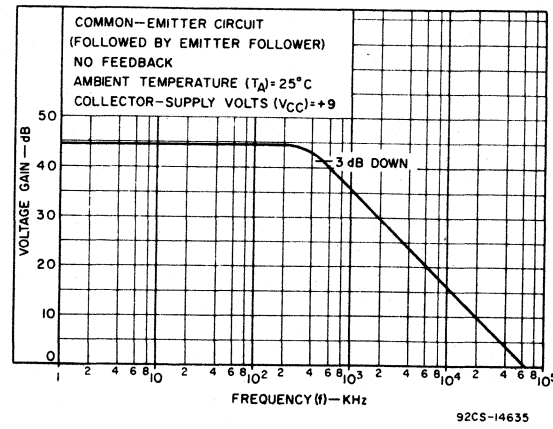


Fig.5

TYPICAL 2nd-AMPLIFIER RESPONSE

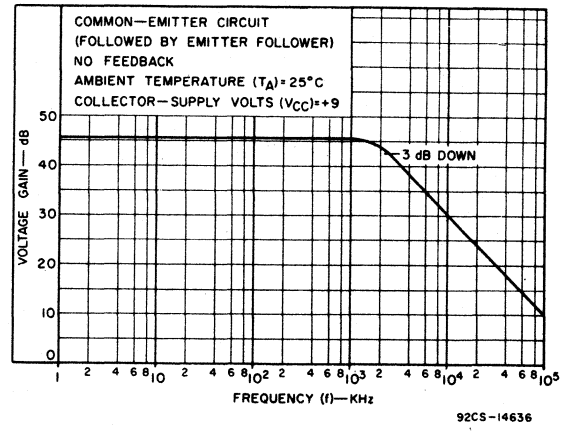


Fig.6

TYPICAL 3rd-AMPLIFIER RESPONSE

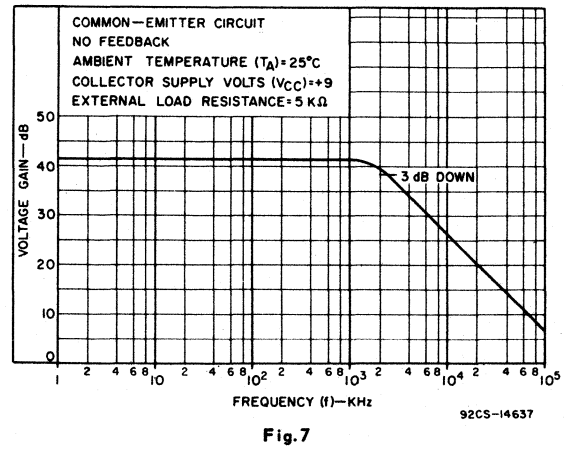
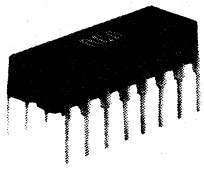


Fig.7



16-Lead Dual-in-Line Plastic Package

CA3048 H-1622

Four Independent AC Amplifiers

For Low-Noise and General AC Applications In Industrial Service

FEATURES

- Four AC amplifiers on a common substrate
- Independently accessible inputs and outputs
- Operates from single-ended supply

EACH AMPLIFIER

- Noise figure at 1 kHz ..... 2 dB typ.
- High voltage gain ..... 53 dB min.
- High input resistance ..... 90 kΩ typ.
- Undistorted output voltage 2 V rms min.
- Output Impedance ..... 1 kΩ typ.
- Open-loop bandwidth ..... 300 kHz typ.

The RCA CA3048 is a silicon monolithic integrated circuit consisting of four independent identical AC amplifiers which can operate from a single-ended power supply..

The amplifiers include internal DC bias and feedback to provide temperature-stabilized operation. They may be used in a wide variety of AC applications in which operational amplifiers have previously been used.

Each high gain amplifier has a high impedance non-inverting input, and a lower impedance inverting input for the application of feedback. Two power-supply terminals and two ground terminals are provided to reduce internal and external coupling between amplifiers.

The CA3048 is supplied in a 16-lead dual-in-line plastic package.

APPLICATIONS

- Multi-channel or cascade operation
- Low-level preamplifiers
- Equalizers
- Linear signal mixers
- Tone generators
- Multivibrators
- AC integrators

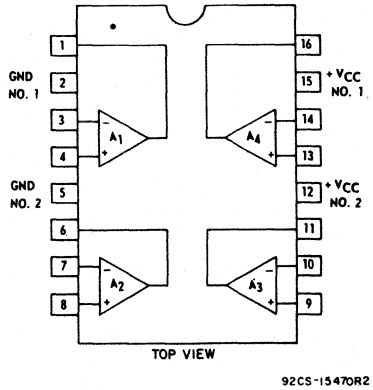


Fig. 1 - Block diagram for CA3048.

CA3048

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C:

DISSIPATION:

At T_A = 55°C . . . . . 750 mW

Above T_A = 55°C. . . . . Derate linearly at 7.7 mW/°C

TEMPERATURE RANGE:

Operating . . . . . -40°C to +85°C

Storage . . . . . -65°C to +150°C

POWER SUPPLY VOLTAGE . . . . . +16 V

AC INPUT VOLTAGE . . . . . 0.5 V rms

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 -16	*
2			*	+2 -3.6	0	*	*	+2 -3.6	-3.6	*	*	+16 0	+2 -3.6	*	+16 0	0 -16
3				+5 -5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 -2	*	*	*	*	*	*	*	*	*	*	*
5						0 -16	*	+2 -3.6	+2 -3.6	*	0 -16	+16 0	+2 -3.6	*	+16 0	*
6							*	*	*	*	*	*	0 -16	*	*	*
7								+5 -5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 -5	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 -16	*	*	*
13														+5 -5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	LIMITS CA3048			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC								
Current drain per amplifier pair	I_{12} or I_{15}	V_{CC} = +12V	3	9.5	13.5	17.5	mA	4,5
DC Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	V_{CC} = +12V	3	6.1	6.9	8.1	V	-
DC Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	V_{CC} = +12V	3	1.7	2.0	2.3	V	-
DC Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	V_{CC} = +12V	3	2.2	2.5	2.8	V	-
DYNAMIC (Characteristics given are for each amplifier with no AC feedback)								
Open-Loop Gain	A_{OL}	V_{CC} = +12V, E_{IN} = 2mV, f = 10kHz	6	53	58	-	dB	7,8
Output Voltage Swing	V_O(rms)	V_{CC} = +12V, f = 1kHz, THD = 5%	6	2.0	2.4	-	V	-
Open-Loop -3dB Bandwidth	BW	V_{CC} = +12V, E_{IN} = 2mV	6	250	300	-	kHz	9
Total Harmonic Distortion	THD	V_{CC} = +12V, f = 1kHz, E_{OUT} = 2V rms	6	-	0.65	-	%	10
Input Resistance	R_{IN}	OPEN LOOP Terminals 3, 7, 10, and 14 are by-passed to ground, f = 1kHz	-	-	90	-	kΩ	-
Input Capacitance	C_{IN}	f = 1MHz	-	-	9	-	pF	-
Output Resistance	R_{OUT}	Terminals 3, 7, 10 and 14 are by-passed to ground	-	-	1	-	kΩ	-
Output Capacitance	C_{OUT}	f = 1MHz	-	-	18	-	pF	-
Feedback Capacitance (Output to non-inverting Input)	C_{FB}	V_{CC} = +12V, f = 1MHz	-	-	<0.1	-	pF	-
Broad-Band Output Noise Voltage	E_N	V_{CC} = +12V, R_S = 10kΩ, A = 40dB, Equivalent Noise BW = 50kHz	11	-	0.3	1	mV	-
Output Noise Voltage "Weighted"	$E_{N(WT)}$		12	-	0.5	2.2	mV	-
Noise Figure	NF (R_S = 5kΩ)	f = 10Hz	-	-	10	-	dB	-
		f = 100Hz	-	-	5.8	-	dB	
		f = 1kHz	-	-	2	-	dB	
		f = 10kHz	-	-	1.1	-	dB	
		f = 100kHz	-	-	0.6	-	dB	
Inter-Amplifier Audio Separation "Cross Talk"		V_{CC} = +12V, f = 1kHz, 0dB = 0.78V	13	-	<-45	-	dB	-
Inter-Amplifier Capacitance (Any amplifier output to any *other* amplifier input)	C	V_{CC} = +12V, f = 1MHz	-	-	<0.02	-	pF	-

CA3048

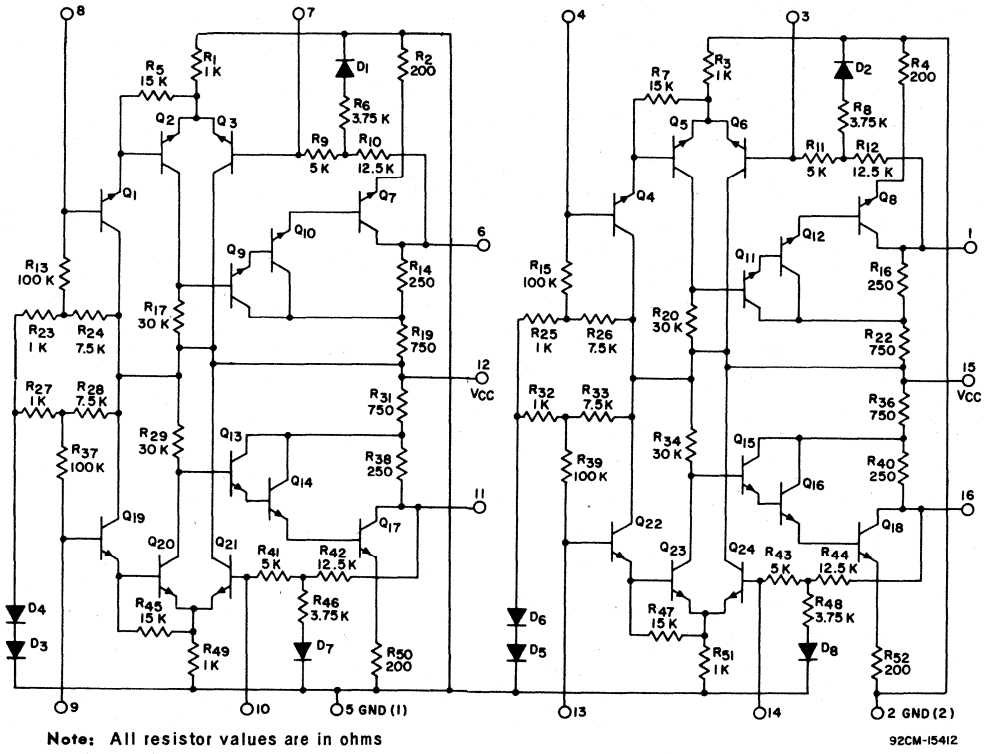


Fig.2 - Schematic diagram for CA3048.

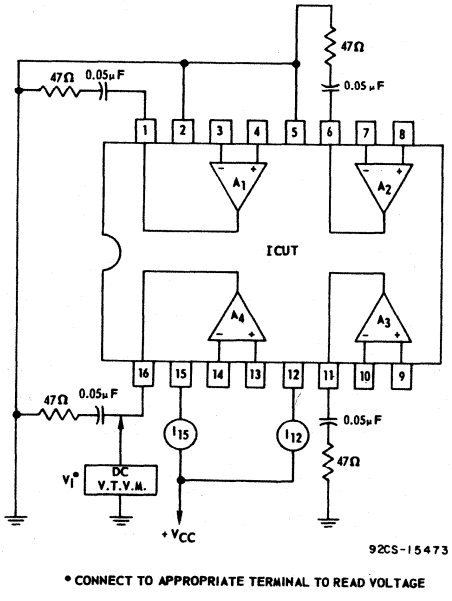


Fig.3 - Test circuit for measurement of collector supply voltage and currents.

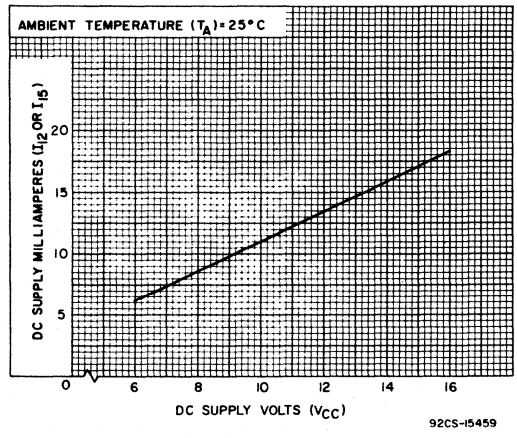


Fig.4 - Typical DC supply current vs supply voltage.

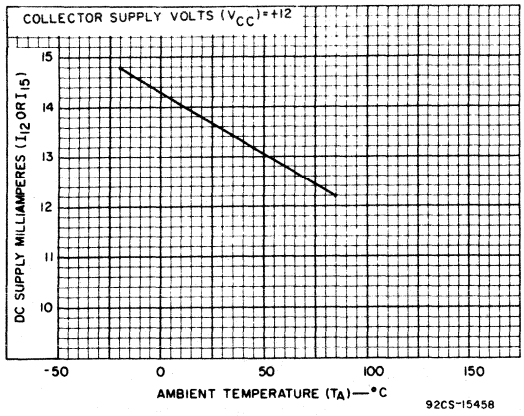


Fig.5 - Typical DC supply current vs ambient temperature.

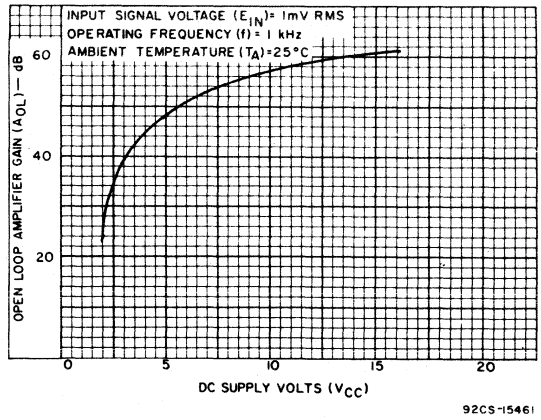
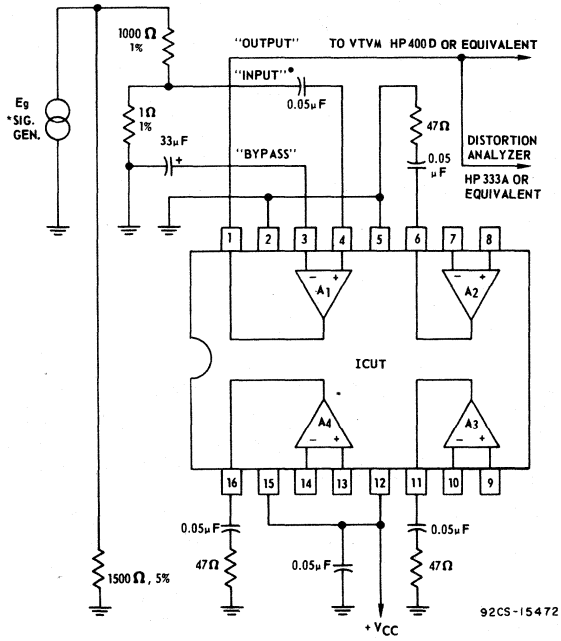


Fig.7 - Typical amplifier gain vs DC supply voltage.



* Sig Gen should be a low distortion type (0.2% THD or less) HP206A or equivalent.

● Adjustment of E_g to 2 volts will make E_S = 2mV.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.6 - Test circuit for measurement of distortion, open-loop gain and bandwidth characteristics.

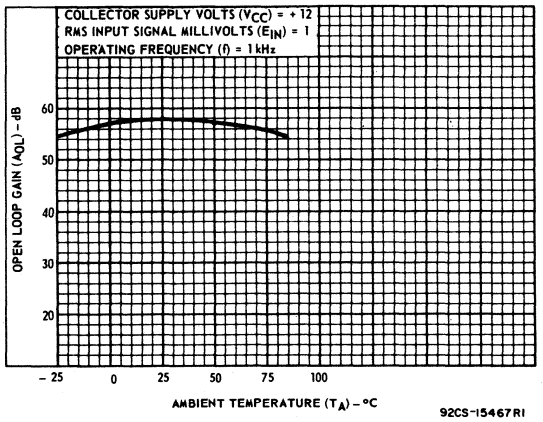


Fig.8 - Typical open-loop gain vs ambient temperature.

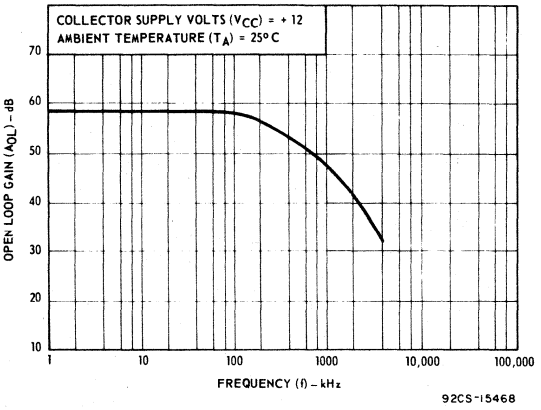


Fig.9 - Typical open-loop gain vs frequency.

CA3048

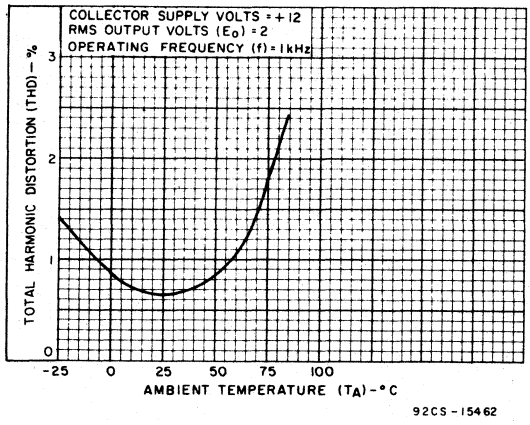
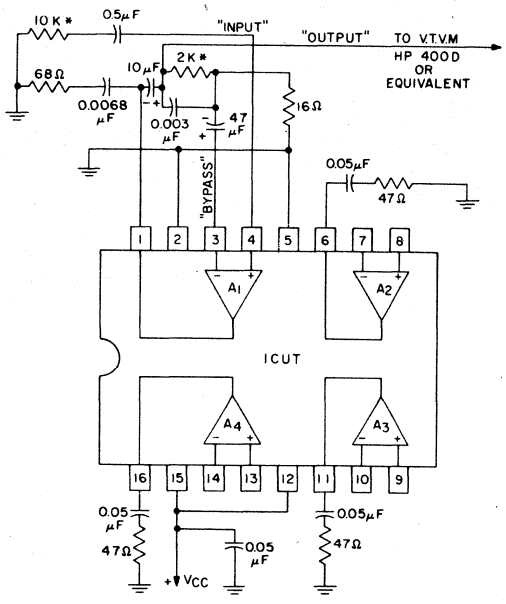


Fig.10 - Typical total harmonic distortion vs ambient temperature.



* RESISTORS ARE METALFILM TYPE, 1%

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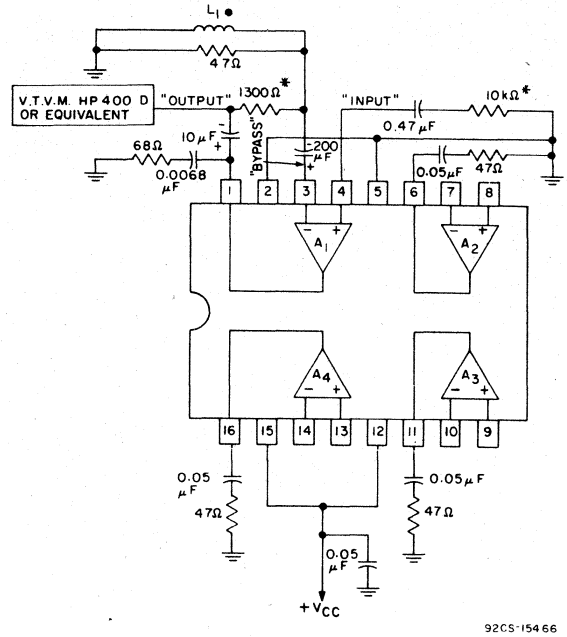
To test Amplifiers 1, 2, 3, or 4, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.11 - Test circuit for measurement of broadband noise characteristic.

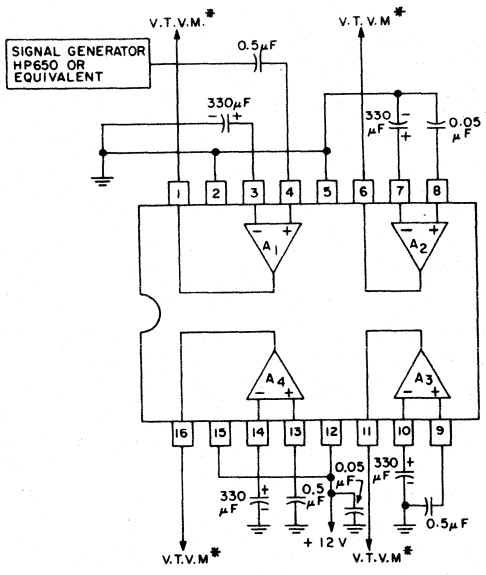


● L_1 - 2.5 millihenry inductor, dc resistance 0.3 ohms or less.

* Resistors metal film type, 1%. To test amplifiers, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.12 - Test circuit for measurement of "weighted" output noise voltage characteristic.



* V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig.13 - Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.

OPERATING CONSIDERATIONS

Economical Gain Control

The CA3048 is designed to permit flexibility in the methods by which amplifier gain can be controlled. Fig.14 shows a curve of the gain of an amplifier when the internal resistive feedback of the device is used in conjunction with an external resistor. Although measured gain of various amplifiers will not be uniform, because of tolerances of internal resistances, this method is very economical and easy to apply.

Stability

The CA3048, as in other devices having high gain-bandwidth product, requires some attention to circuit layout, design, and construction to achieve stability.

Should the CA3048 be left unterminated, socket capacitance alone will provide sufficient feedback to cause high frequency oscillations; therefore, all test circuits in this data bulletin include loading networks that provide stability under all conditions.

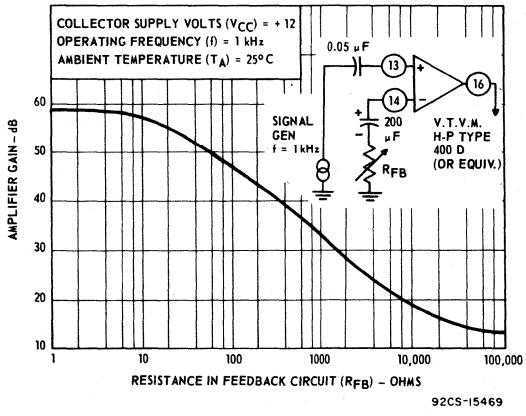
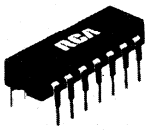


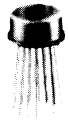
Fig.14 - Typical amplifier gain vs feedback resistance.

CA3049T, CA3102E

14-Lead DIP
CA3102E



12-Lead TO-5



CA3049T

DUAL HIGH-FREQUENCY DIFFERENTIAL AMPLIFIERS

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- **Power Gain 23 dB (typ.) at 200 MHz**
- **Noise Figure 4.6 dB (typ.) at 200 MHz**
- **Two differential amplifiers on a common substrate**
- **Independently accessible inputs and outputs**
- **Full military-temperature-range capability- (−55°C to + 125°C) for the CA3102E and for the CA3049T**

RCA-CA3049T and CA3102E* consist of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general-purpose devices which exhibit low I/f noise and a value of f_T in excess of 1 GHz. These features make the CA3049T and CA3102E useful from dc to 500 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

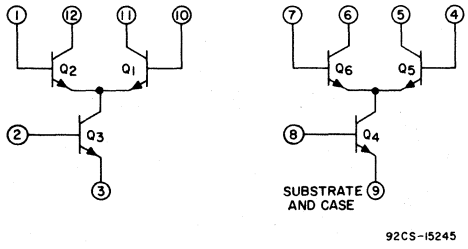
The monolithic construction of the CA3049T and CA3102E provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3102E is like the CA3049T except that it has a separate substrate connection for greater design flexibility. The CA3049T is supplied in the 12-lead TO-5 package; the CA3102E, in the 14-lead plastic dual-in-line package.

Applications

- **VHF amplifiers**
- **VHF mixers**
- **Multifunction combinations – RF/Mixer/Oscillator; Converter/IF**
- **IF amplifiers (differential and/or cascode)**
- **Product detectors**
- **Doubly balanced modulators and demodulators**
- **Balanced quadrature detectors**
- **Cascade limiters**
- **Synchronous detectors**
- **Balanced mixers**
- **Synthesizers**
- **Balanced (push-pull) cascode amplifiers**
- **Sense amplifiers**

*Formerly Developmental No. TA6228.



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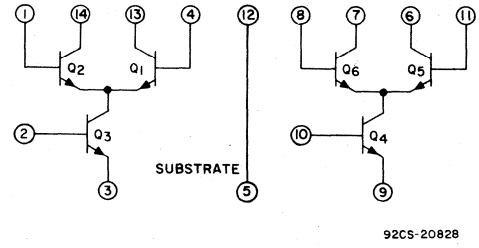
Schematic Diagram for CA3049T



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Schematic Diagram for CA3102E

MAXIMUM RATINGS, *ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C*

Power Dissipation, P:	CA3049T	CA3102E	
Any one transistor	300	300	mW
Total package	600	750	mW
For $T_A > 55°C$ Derate at:	5	6.67	mW/°C
Temperature Range:			
Operating	−55 to + 125	−55 to + 125	°C
Storage	−65 to + 150	−65 to + 150	°C

The following ratings apply for each transistor in the devices

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor of the CA3049T and CA3102E is isolated from the substrate by an integral diode. The substrate (terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIR-CUIT	CA3102E LIMITS			CA3049T LIMITS				TYPICAL CHARAC-TERISTICS CURVES
				FIG.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	FIG.
STATIC CHARACTERISTICS												
For Each Differential Amplifier												
Input Offset Voltage	V_{IO}			1	---	0.25	5	---	0.25	---	mV	-4
Input Offset Current	I_{IO}	$I_3 = I_9$ = 2 mA		1	---	0.3	3	---	0.3	---	μA	---
Input Bias Current	I_{IB}			1	---	13.5	33		13.5	33	μA	5
Temperature Coefficient Magnitude of Input-Offset Voltage	$\left\|\frac{\Delta V_{IO}}{\Delta T}\right\|$			1	---	1.1	---	---	1.1	---	μV/°C	4
For Each Transistor												
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 6 V, I_C = 1 mA		---	674	774	874	---	774	---	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 6 V, I_C = 1 mA		---	---	-0.9	---	---	-0.9	---	mV/°C	6
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		---	---	0.0013	100	---	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0		---	15	24	---	15	24	---	V	---
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		---	20	60	---	20	60	---	V	---
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_B = 0, I_E = 0		---	20	60	---	20	60	---	V	---
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0		---	5	7	---	5	7	---	V	---
DYNAMIC CHARACTERISTICS												
1/f Noise Figure (For Single Transistor)	NF	f = 100 KHz, R_S = 500 Ω, I_C = 1 mA		---	---	1.5	---	---	1.5	---	dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 6 V, I_C = 5 mA		---	---	1.35	---	---	1.35	---	GH_z	11
Collector-Base Capacitance	C_{CB}	I_C = 0	V_{CB} = 5V	*	---	0.28	---	---	0.28	---	pF	8
				**	---	0.15	---	---	0.28	---	pF	
Collector-Substrate Capacitance	C_{CI}	I_C = 0	V_{CI} = 5V		---	1.65	---	---	1.65	---	pF	8
For Each Differential Amplifier												
Common-Mode Rejection Ratio	CMR	$I_3 = I_9$ = 2 mA		---	---	100	---	---	100	---	dB	---
AGC Range, One Stage	AGC	Bias Voltage = -6V		2	---	75	---	---	75	---	dB	---
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V, f = 10 MHz		2	18	22	---	---	22	---	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz	Cascode	3	---	23	---	---	23	---	dB	---
Noise Figure	NF	V_{CC} = 12V	Cascode	3	---	4.6	---	---	4.6	---	dB	---
Input Admittance	Y_{11}	For Cascode Configuration, $I_3 = I_9$ = 2 mA	Cascode	---	---	1.5 + j 2.45	---	---	1.5 + j 2.45	---	mmho	14, 16, 18
			Diff.Amp.	---	---	0.878 + j 1.3	---	---	0.878 + j 1.3	---		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff. Amplifier Configuration, $I_3 = I_9$ = 4mA (each collector $I_C \simeq$ 2mA)	Cascode	---	---	0 - j 0.008	---	---	0 - j 0.008	---	mmho	---
			Diff.Amp.	---	---	0 - j 0.013	---	---	0 - j 0.013	---		---
Forward Transfer Admittance	Y_{21}		Cascode	---	---	17.9 - j 30.7	---	---	17.9 - j 30.7	---	mmho	26, 28, 30
			Diff. Amp.	---	---	- 10.5 + j 13	---	---	- 10.5 + j 13	---		27, 29, 31
Output Admittance	Y_{22}		Cascode	---	---	- 0.503 - j 15	---	---	- 0.603 - j 15	---	mmho	20, 22, 24
			Diff.Amp.	---	---	0.071 + j 0.62	---	---	0.071 + j 0.62	---		21, 23, 25

*Terminals 1 & 14, or 7 & 8. (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11. (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

CA3049T, CA3102E

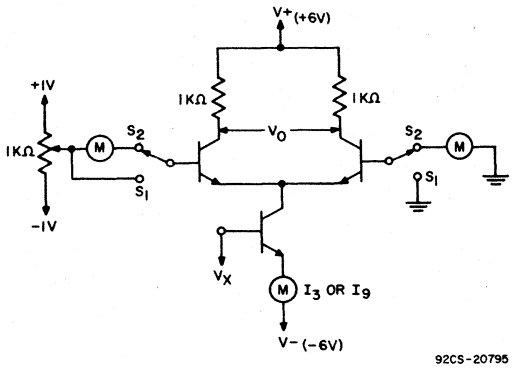


Fig.1—Static characteristics test circuit for CA3102E.

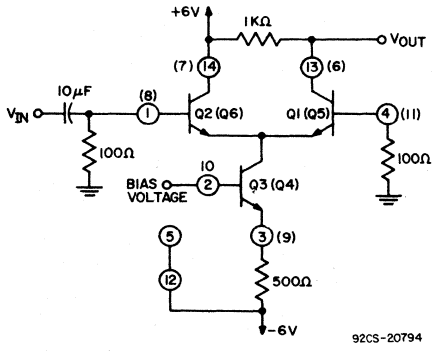
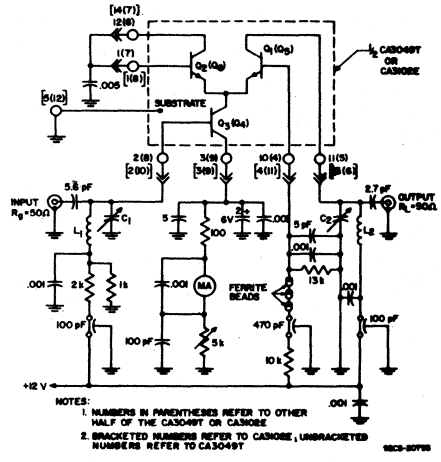


Fig.2—AGC range and voltage gain test circuit for CA3102E.



L_1, L_2 – Approx. 1/2 Turn #18 Tinned Copper Wire, 5/8" Dia.

C_1, C_2 – 15 pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent)

All Capacitors in μF Unless Otherwise Indicated

All Resistors in Ohms Unless Otherwise Indicated

Fig.3—200 MHz cascode power gain and noise figure test circuit.

Typical Characteristics for CA3049T and CA3102E

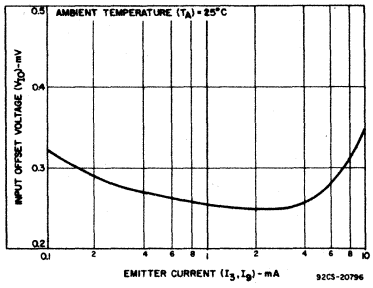


Fig. 4—Input offset voltage vs. emitter current.

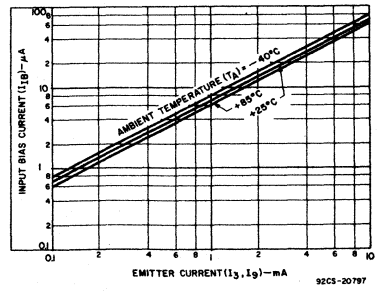


Fig. 5—Input bias current vs. emitter current.

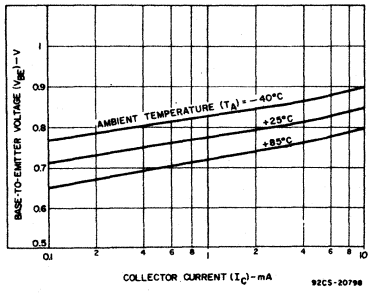


Fig. 6—Base-to-emitter voltage vs. collector current.

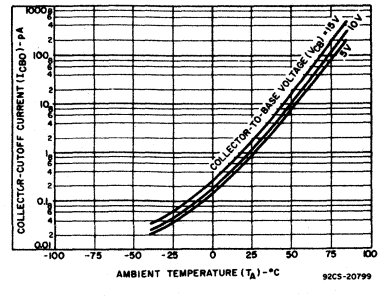


Fig. 7—Collector-cutoff current vs. temperature.

Typical Characteristics for CA3049T and CA3102E (cont'd)

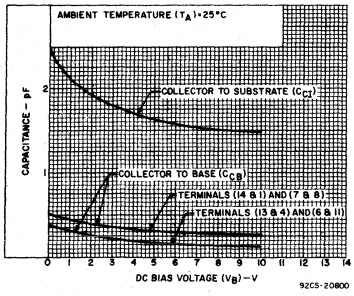


Fig. 8—Capacitance vs. dc bias voltage.

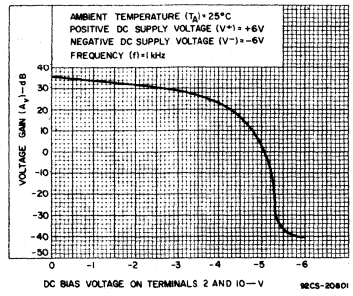


Fig. 9—Voltage gain vs. dc bias voltage.

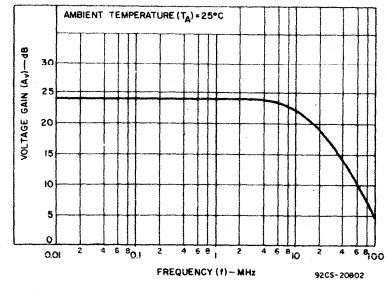


Fig. 10—Voltage gain vs. frequency.

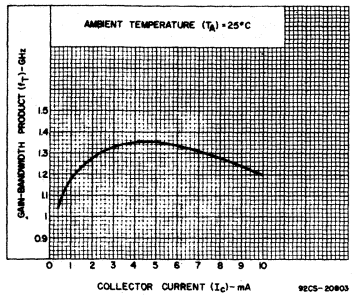


Fig. 11—Gain-bandwidth product vs. collector current.

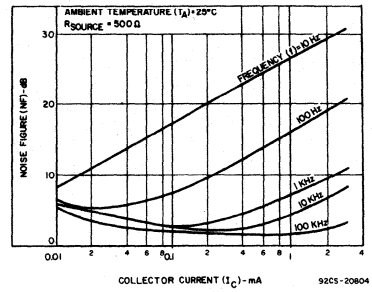


Fig. 12—1/f noise figure vs. collector current.

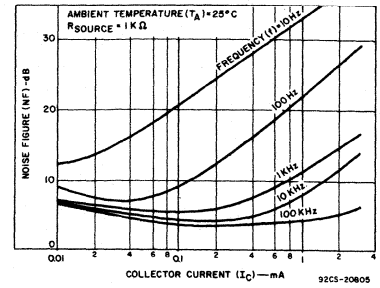


Fig. 13—1/f noise figure vs. collector current.

Typical Input Admittance Characteristics for CA3049T and CA3102

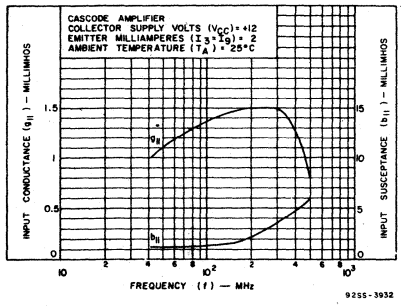


Fig. 14—Input admittance (Y_{11}) vs. frequency.

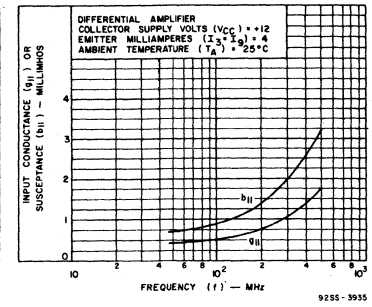


Fig. 15—Input admittance (Y_{11}) vs. frequency.

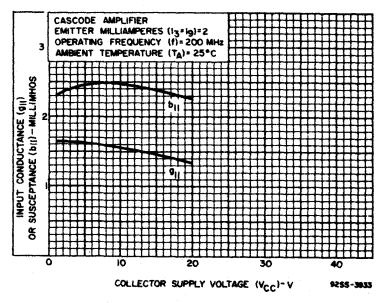


Fig. 16—Input admittance (Y_{11}) vs. collector supply voltage.

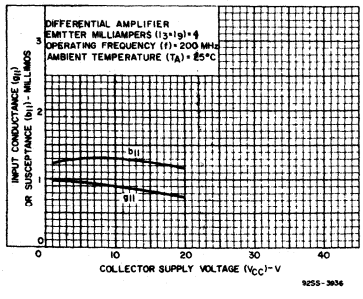


Fig. 17—Input admittance (Y_{11}) vs. collector supply voltage.

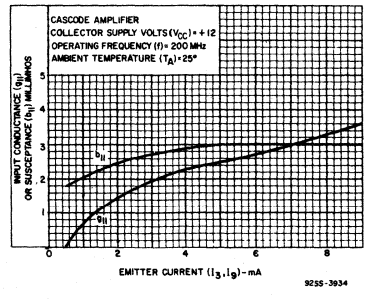


Fig. 18—Input admittance (Y_{11}) vs. emitter current.

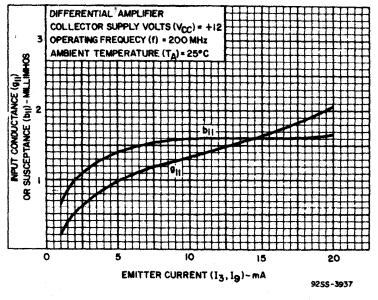


Fig. 19—Input admittance (Y_{11}) vs. emitter current.

Typical Output Admittance Characteristics for CA3049T and CA3102E

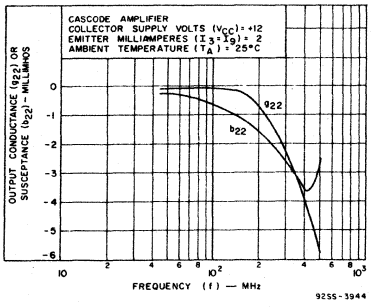


Fig. 20—Output admittance (Y_{22}) vs. frequency.

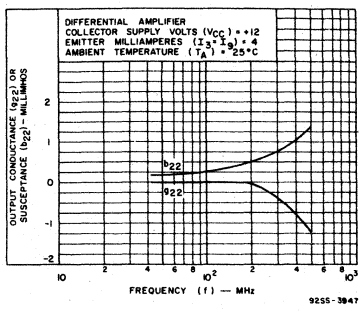


Fig. 21—Output admittance (Y_{22}) vs. frequency.

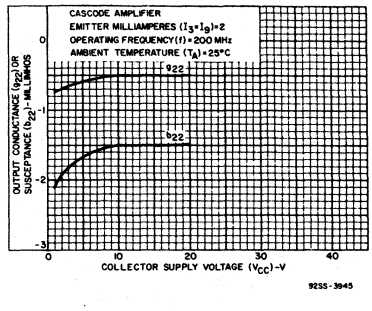


Fig. 22—Output admittance (Y_{22}) vs. collector supply voltage.

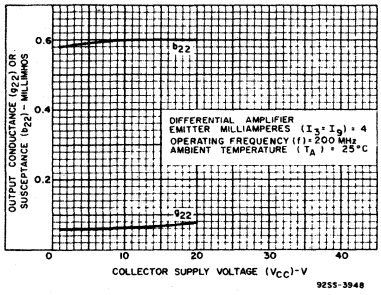


Fig. 23—Output admittance (Y_{22}) vs. collector supply voltage.

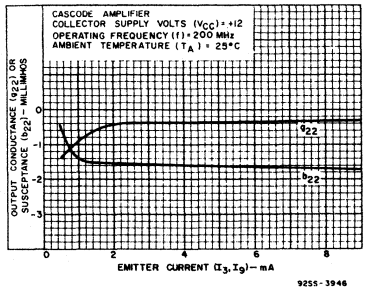


Fig. 24—Output admittance (Y_{22}) vs. emitter current.

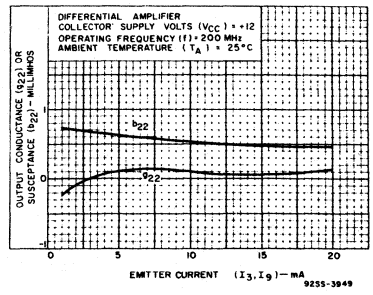


Fig. 25—Output admittance (Y_{22}) vs. emitter current.

Typical Forward Transfer Characteristics for CA3049T and CA3102E

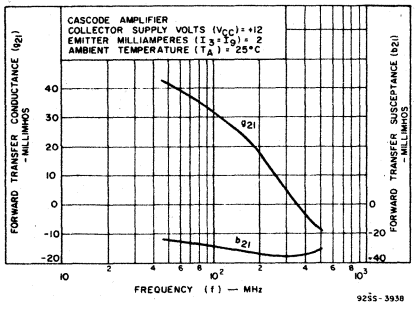


Fig. 26—Forward transfer admittance (Y_{21}) vs. frequency.

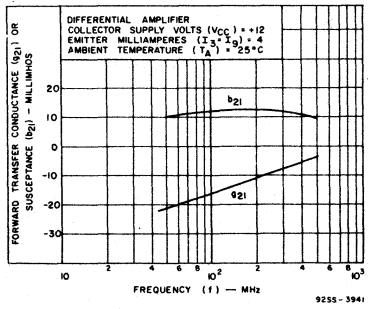


Fig. 27—Forward transfer admittance (Y_{21}) vs. frequency.

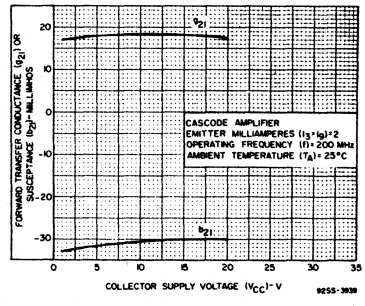


Fig. 28—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

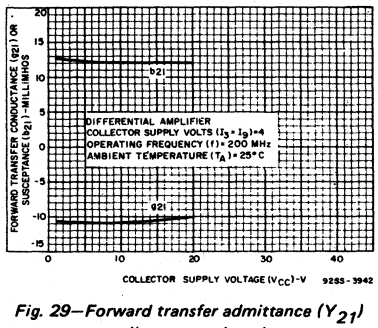


Fig. 29—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

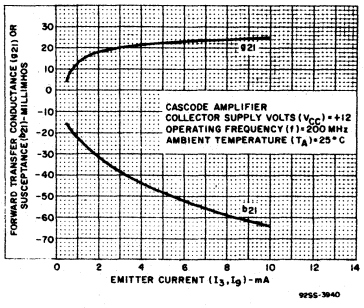


Fig. 30—Forward transfer admittance (Y_{21}) vs. emitter current.

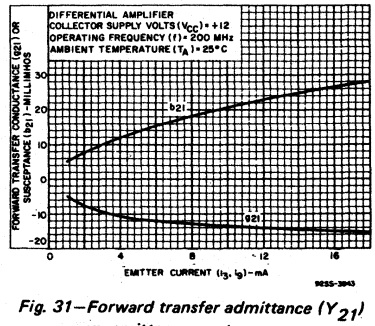
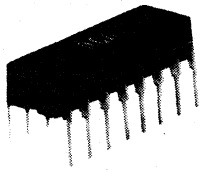


Fig. 31—Forward transfer admittance (Y_{21}) vs. emitter current.



H-1622

16-Lead Dual-In-Line Plastic Package

Four Independent AC Amplifiers

Special-Function Sub-System for Stereo Preamplifiers, Magnetic Pickups, Tape Heads, etc.

Features:

- *Four AC amplifiers on a common substrate*
- *Independently accessible inputs and outputs*
- *Operates from single-ended supply*

EACH AMPLIFIER

- *High voltage gain - 53 dB min.*
- *High input resistance - 90 kΩ typ.*
- *Undistorted output voltage - 2 V rms min.*
- *Output impedance - 1 kΩ typ.*
- *Open-loop bandwidth - 300 kHz typ.*

Applications:

- *Full-function stereo preamplifiers*
- *Tape recorder and playback preamplifiers*
- *Tone generators*

The RCA-CA3052 is a silicon monolithic integrated circuit designed specifically for stereo preamplifier service. The circuit consists of four independent ac amplifiers which can operate from a single-ended supply.

The CA3052 can operate as an equalizer amplifier in tape recorders, magnetic cartridge phonograph applications, and tone control amplifiers. It can provide all of the amplification necessary for a full-function stereo preamplifier.

The CA3052 is supplied in a 16-lead dual-in-line plastic package.

RCA-CA3052 is schematically identical with the CA3048 Amplifier Array (File No. 377). Each amplifier of the CA3048 is tightly specified for equivalent output noise under a variety of test methods. The CA3052 is specified using RIAA test methods for equivalent input noise using one test method for amplifiers 1 and 4, and an appropriately different method for amplifiers 2 and 3.

ABSOLUTE-MAXIMUM RATING *at* $T_A = 25°C$:

DISSIPATION:

Up to $T_A = 55°C$ ..... 750 mW

Above $T_A = 55°C$ ..... Derate linearly at 7.7 mW/°C

TEMPERATURE RANGE:

Operating ..... −40°C to +85°C

Storage ..... −65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)

from case for 10 seconds max. ..... +265°C

POWER SUPPLY VOLTAGE ..... +16 V

AC INPUT VOLTAGE ..... 0.5 V rms

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 -16	*
2			*	+2 -3.6	0	*	*	+2 -3.6	+2 -3.6	*	*	+16 0	+2 -3.6	*	+16 0	0 -16
3				+5 -5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 -2	*	*	*	*	*	*	*	*	*	*	*
5						0 -16	*	+2 -3.6	+2 -3.6	*	0 -16	+16 0	+2 -3.6	*	+16 0	*
6							*	*	*	*	*	*	0 -16	*	*	*
7								+5 -5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 -5	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 -16	*	*	*
13														+5 -5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

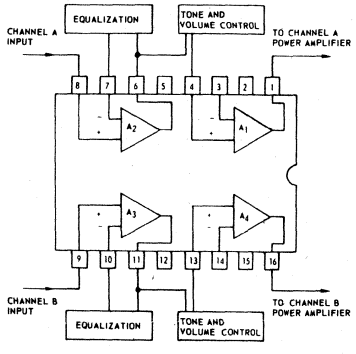


Fig. 1 – Block diagram of stereo preamplifier using CA3052.

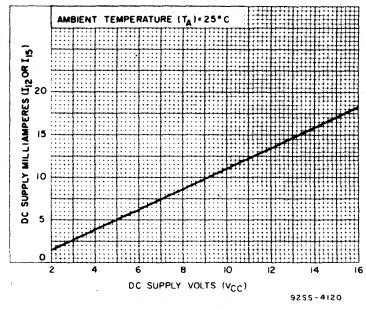


Fig. 2 – Typical DC supply current vs supply voltage.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS CA3052			UNITS
			MIN.	TYP.	MAX.	
STATIC						
Current drain per amplifier pair	I_{12} or I_{15}	V_{CC} = +12 V	9.5	13.5	17.5	mA
DC Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	V_{CC} = +12 V	6.1	6.9	8.1	V
DC Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	V_{CC} = +12 V	1.7	2.0	2.3	V
DC Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	V_{CC} = +12 V	2.2	2.5	2.8	V
DYNAMIC each amplifier with no AC feedback unless otherwise noted--terminals 3, 7, 10, & 14 bypassed to ground						
Open-Loop Gain	A_{OL}	V_{CC} = +12 V E_{IN} = 2 mV f = 10 kHz	53	58	–	dB
Open-Loop Output Voltage Swing	V_O(rms)	V_{CC} = +12 V f = 1 kHz THD = 5%	2.0	2.4	–	V
Open-Loop -3 dB Bandwidth	BW	V_{CC} = +12 V E_{IN} = 2 mV	–	300	–	kHz
Open-Loop Total Harmonic Distortion	THD	V_{CC} = +12 V, f = 1 kHz E_{OUT} = 2 V rms	–	0.65	–	%
Input Resistance	R_I	V_{CC} = +12 V, f = 1 kHz	–	90	–	kΩ
Input Capacitance	C_I	V_{CC} = +12 V, f = 1 MHz	–	9	–	pF
Output Resistance	R_O	V_{CC} = +12 V, f = 1 kHz	–	1	–	kΩ
Feedback Capacitance (Output to non-inverting Input)	C_{FB}	V_{CC} = +12 V f = 1 MHz	–	<0.1	–	pF
Equivalent Input Noise Voltage (Amplifiers 1 & 4), "C" Filter at Output*	E_{N1}‡	V_{CC} = +10 V R_S = 5 kΩ A = 45 dB	–	1.7	6.4	μV
Equivalent Input Noise Voltage (Amplifiers 2 & 3) RIAA Compensated*	E_{N2}‡	V_{CC} = +10 V R_S = 5 kΩ A = 64 dB (1 kHz)	–	4	15.0	μV
Inter-Amplifier Audio Separation "Cross Talk"[11]		V_{CC} = +12 V f = 1 kHz 0 dB = 0.78 V	–	<-45	–	dB
Inter-Amplifier Capacitance (Any amplifier output to any *other* amplifier input)	C	V_{CC} = +12 V f = 1 MHz	–	< 0.02	–	pF

*Per IHF Standard Methods of Measurement for Audio Amplifiers IHF–A–201, 1966

‡ ac feedback included in test circuit

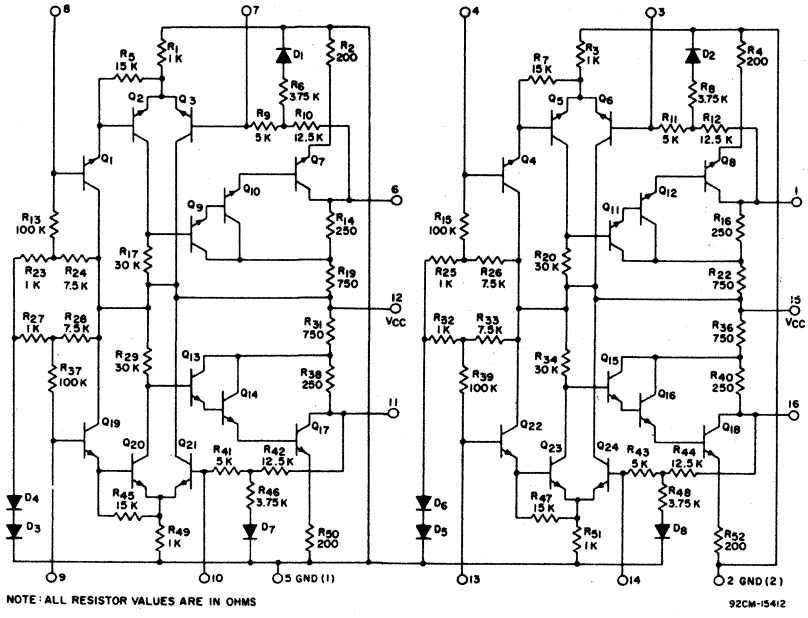


Fig. 3 – Schematic diagram for CA3052.

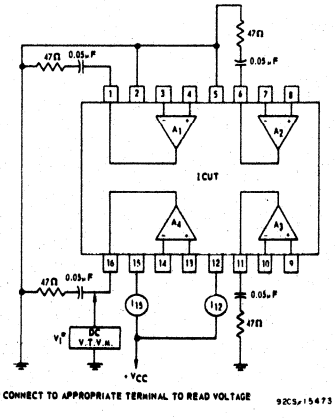


Fig. 4 – Test circuit for measurement of collector supply voltage and currents.

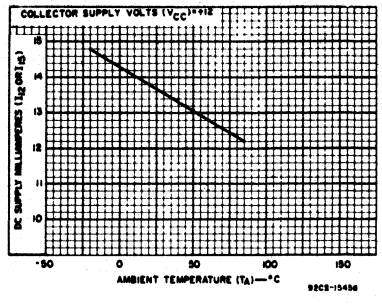
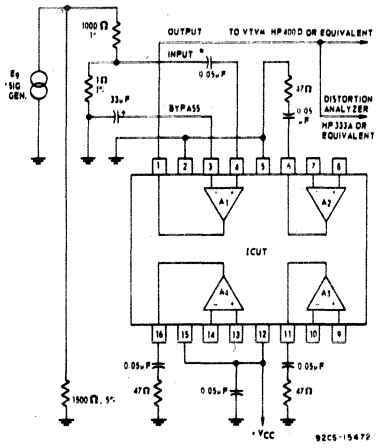


Fig. 5 – Typical DC supply current vs ambient temperature.



* Sig Gen should be a low distortion type (0.2% THD or less) HP206A or equivalent.

● Adjustment of E_g to 2 volts will make E_s = 2mV.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig. 6 – Test circuit for measurement of distortion, open-loop gain, and bandwidth characteristics.

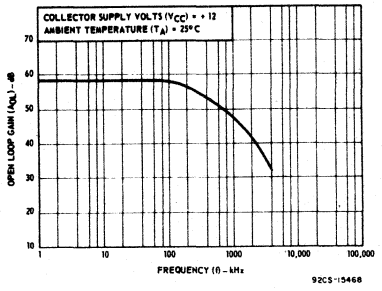


Fig. 9 – Typical open-loop gain vs frequency.

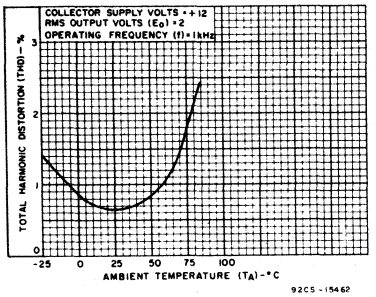


Fig. 10 – Typical total harmonic distortion vs ambient temperature.

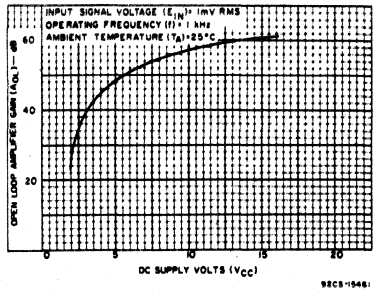


Fig. 7 – Typical amplifier gain vs DC supply voltage.

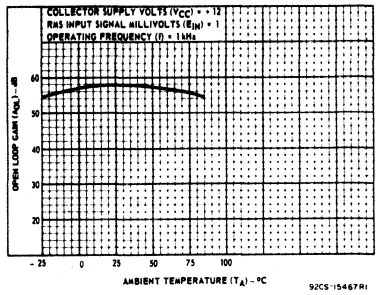
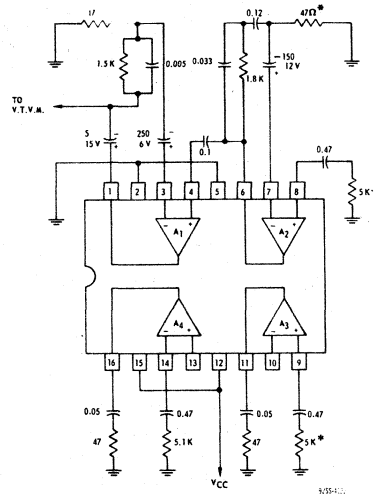
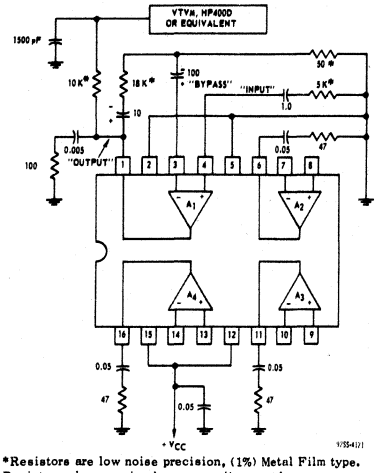


Fig. 8 – Typical open-loop gain vs ambient temperature.



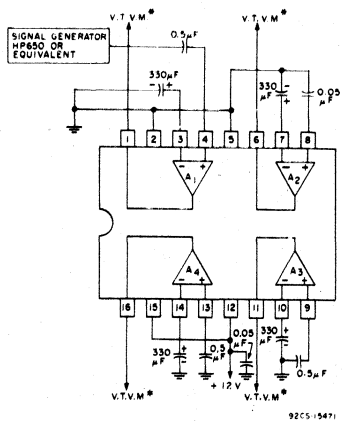
*Resistors are low noise precision (1%) Metal Film type.

Fig. 11 – Test circuit for equivalent input noise voltage measurement, RIAA compensated.



*Resistors are low noise precision, (1%) Metal Film type. Resistor values are in ohms; capacitance values are in microfarads, unless otherwise specified.

Fig. 12— Test circuit for measurement of equivalent input noise voltage of amplifiers 1 and 4.

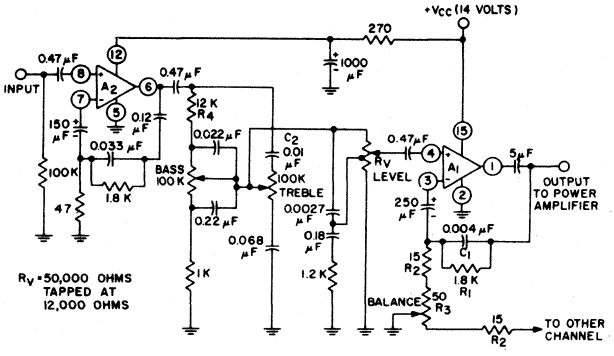


*V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig. 13 — Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.



Performance Data

Gain at 1-kHz reference	47 dB
Boost at 100 Hz	11.5 dB
Boost at 10 kHz	11.5 dB
Cut at 100 Hz	10 dB
Cut at 10 kHz	9 dB
Noise:	
At maximum volume (input shorted)	> 70 dB below 1 volt
At minimum volume	> 80 dB below 1 volt
Total harmonic distortion (at 1-kHz reference and an output of 1 volt)	< 0.3 per cent

92CM-29305

Fig. 14 — Schematic of one channel of a complete stereo preamplifier.

OPERATING CONSIDERATIONS

Economical Gain Control

The CA3052 is designed to permit flexibility in the methods by which amplifier gain can be controlled. Fig. 15 shows a curve of the gain of an amplifier when the internal resistive feedback of the device is used in conjunction with an external resistor. Although measured gain of various amplifiers will not be uniform, because of tolerances of internal resistances, this method is very economical and easy to apply.

Stability

The CA3052, as in other devices having high gain-band-width product, requires some attention to circuit layout, design, and construction to achieve stability.

Should the CA3052 be left unterminated, socket capacitance alone will provide sufficient feedback to cause high frequency oscillations; therefore, all test circuits in this data bulletin include loading networks that provide stability under all conditions.

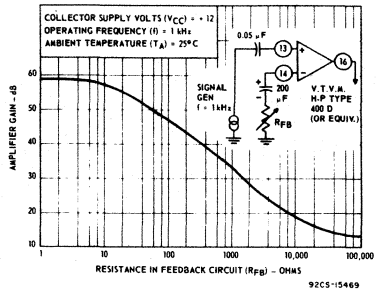
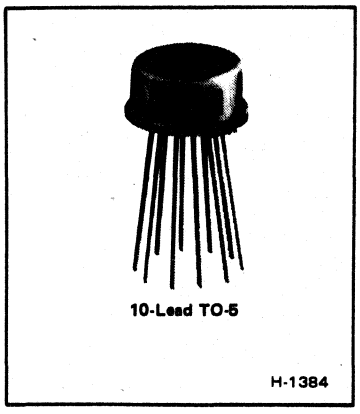


Fig. 15 — Typical amplifier gain vs feedback resistance.

CA3019



Ultra-Fast Low-Capacitance Matched Diodes

For Applications in Communications and Switching Systems

Features:

- *Excellent diode match*
- *Low leakage current*
- *Low pedestal voltage when gating*
- *Companion Application Note, ICAN-5299: "Application of the RCA-CA3019 Integrated-Circuit Diode Array"*

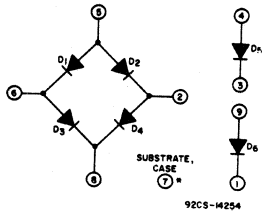
Applications:

- *Modulator*
- *Mixer*
- *Balanced modulator*
- *Analog switch*
- *Diode gate for chopper-modulator applications*

The RCA-CA3019 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Four of the diodes are internally connected as a "quad" and two are independently accessible. The substrate is internally connected to the 10-lead TO-5-style case.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.



*Connect to most negative circuit potential.

Fig. 1 — Schematic Diagram.

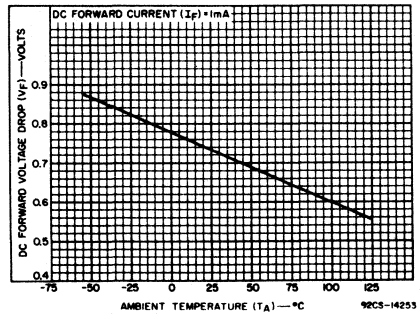


Fig. 2 – DC forward voltage drop (any diode) as a function of temperature.

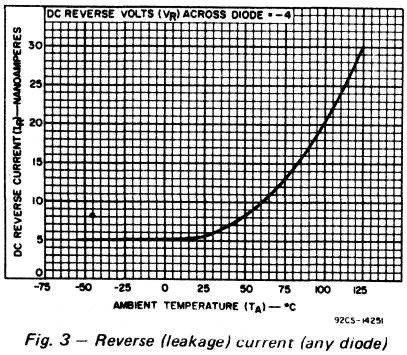


Fig. 3 – Reverse (leakage) current (any diode) as a function of temperature.

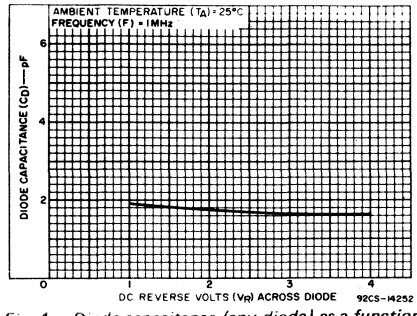


Fig. 4 – Diode capacitance (any diode) as a function of reverse voltage.

Absolute-Maximum Ratings:

DISSIPATION:
- Any one diode unit . . . 20 max. mW
- Total for device . . . . 120 max. mW

TEMPERATURE RANGE:
- Storage . . . . . −65 to +200 °C
- Operating . . . . . −55 to +125 °C

DC Forward Current, I_F . . 25 mA

Peak Recurrent Forward Current, I_f . . . . . 100 mA

Peak Forward Surge Current, I_f (surge) . . . 100 mA

VOLTAGE: See Table

Absolute-Maximum Voltage Limits:

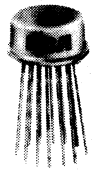
TERM.	VOLTAGE LIMITS		CONDITIONS	
	NEG.	POS.	TERM.	VOLT.
1	−3	+12	7	−6
2	−3	+12	7	−6
3	−3	+12	7	−6
4	−3	+12	7	−6
5	−3	+12	7	−6
6	−3	+12	7	−6
7	−18	0	1,2, 3,6, 8	0
8	−3	+12	7	−6
9	−3	+12	7	−6
10	NO CONNECTION			
CASE	INTERNALLY CONNECTED TO TERMINAL 7 **DO NOT GROUND**			

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$

Characteristics Apply for Each Diode Unit, Unless Otherwise Specified

CHARACTERISTICS	SPECIAL TEST CONDITIONS	LIMITS TYPE CA3019			Units
		Min.	Typ.	Max.	
DC Forward Voltage Drop	DC Forward Current (I_F) = 1 mA	–	0.73	0.78	V
DC Reverse Breakdown Voltage	DC Reverse Current (I_R) = −10 μA	4	6	–	V
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	DC Reverse Current (I_R) = −10 μA	25	80	–	V
DC Reverse (Leakage) Current	DC Reverse Voltage (V_R) = −4 V	–	0.0055	10	μA
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	DC Reverse Voltage (V_R) = −4 V	–	0.010	10	μA
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	DC Forward Current (I_F) = 1 mA	–	1	5	mV
Single Diode Capacitance	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) = −2V	–	1.8	–	pF
Diode Quad-to-Substrate Capacitance	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) between Terminal 2,5,6, or 8 of Diode Quad and Terminal 7 (Substrate) = −2 V				
	Terminal 2 or 6 to Terminal 7	–	4.4	–	pF
	Terminal 5 or 8 to Terminal 7	–	2.7	–	pF
Series Gate Switching Pedestal Voltage		–	10	–	mV

CA3039



12-Lead TO-5

H-1463

Diode Array

Six Matched Diodes on a Common Substrate

Ultra-Fast Low-Capacitance Matched Diodes For Applications in Communications and Switching Systems

Features:

- *Excellent reverse recovery time - 1 ns typ.*
- *Matched monolithic construction - V_F matched within 5 mV*
- *Low diode capacitance - C_D = 0.65 pF typical at V_R = −2 V*

The RCA-CA3039 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

Applications

- *Balanced modulators or demodulators*
- *Ring modulators*
- *High speed diode gates*
- *Analog switches*

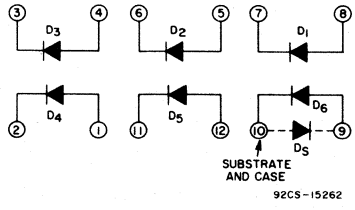


Fig. 1 — Schematic Diagram for CA3039.

ABSOLUTE MAXIMUM RATINGS at T_A = 25 °C

Dissipation:
- Any one diode unit . . . . . 100 mW
- Total for device . . . . . 600 mW
- For T_A > 55 °C . . . . . derate linearly 5.7 mW/°C

Temperature Range:
- Operating . . . . . -55 to +125 °C
- Storage . . . . . -65 to +150°C

Peak Inverse Voltage, PIV for: D_1-D_5 . . . 5 V
D_6 . . . . . 0.5 V

Peak Diode-to-Substrate Voltage, V_{DI}
for D_1-D_5 (term. 1,4,5,8 or 12 to term. 10) +20, -1 V

DC Forward Current, I_F . . . . . 25 mA

Peak Recurrent Forward Current, I_f . . . . . 100 mA

Peak Forward Surge Current, I_f (surge) . . . 100 mA

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . + 265 °C

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

Characteristics apply for each diode unit, unless otherwise specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS			UNITS	CHARACTERISTIC CURVES
			MIN.	TYP.	MAX.		FIG.
DC Forward Voltage Drop	V_F	I_F = 50 μA	–	0.65	0.69	V	2
		1 mA	–	0.73	0.78	V	
		3 mA	–	0.76	0.80	V	
		10 mA	–	0.81	0.90	V	
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = -10 μA	5	7	–	V	–
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	I_R = -10 μA	20	–	–	V	–
DC Reverse (Leakage) Current	I_R	V_R = -4 V	–	0.016	100	nA	3
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	V_R = -10 V	–	0.022	100	nA	4
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F_1} - V_{F_2} \rvert$	I_F = 1 mA	–	0.5	5	mV	2
Temperature Coefficient of $\lvert V_{F_1} - V_{F_2} \rvert$	$\frac{\Delta \lvert V_{F_1} - V_{F_2} \rvert}{\Delta T}$	I_F = 1 mA	–	1	–	μV/°C	5
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	I_F = 1 mA	–	-1.9	–	mV/°C	6
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1 mA	–	0.65	–	V	–
Reverse Recovery Time	t_{rr}	I_F = 10 mA, I_R = 10 mA	–	1	–	ns	–
Diode Resistance	R_D	f = 1 kHz, I_F = 1 mA	25	30	45	Ω	7
Diode Capacitance	C_D	V_R = -2 V, I_F = 0	–	0.65	–	pF	8
Diode-to-Substrate Capacitance	C_{DI}	V_{DI} = +4 V, I_F = 0	–	3.2	–	pF	9

TYPICAL CHARACTERISTICS

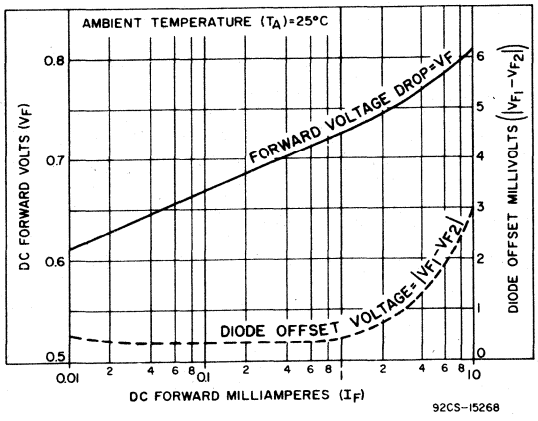


Fig. 2 - DC forward voltage drop (any diode) and diode offset voltage vs DC forward current

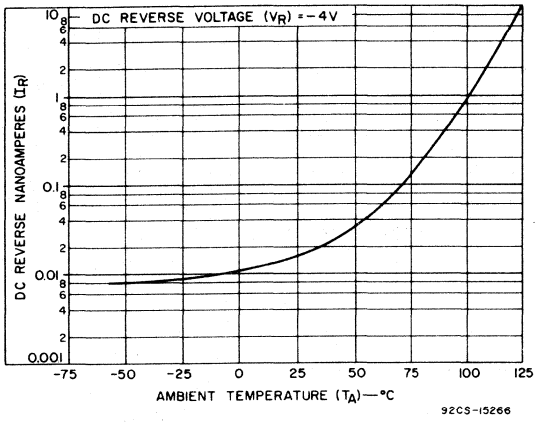


Fig. 3 - DC reverse (leakage) current (diodes 1,2,3,4,5) vs temperature

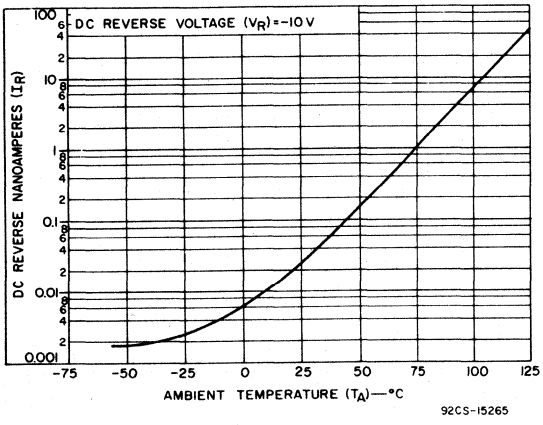


Fig. 4 - DC reverse (leakage) current between diodes (1,2,3,4,5) and substrate vs temperature

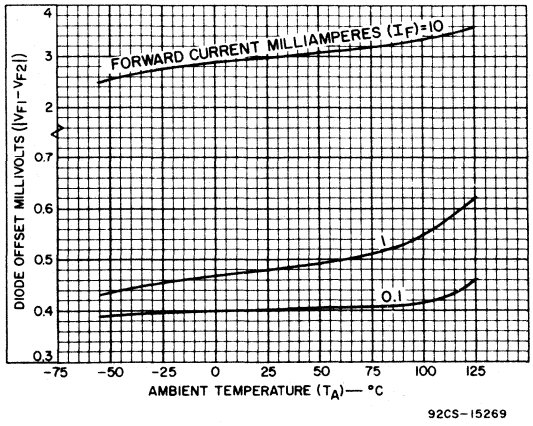


Fig. 5 - Diode offset voltage (any diode) vs temperature

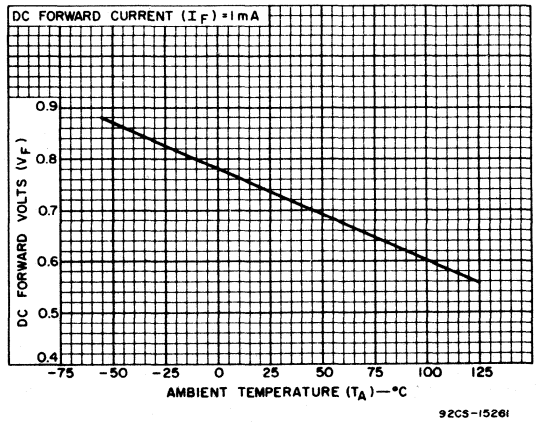


Fig. 6 - DC forward voltage drop (any diode) vs temperature

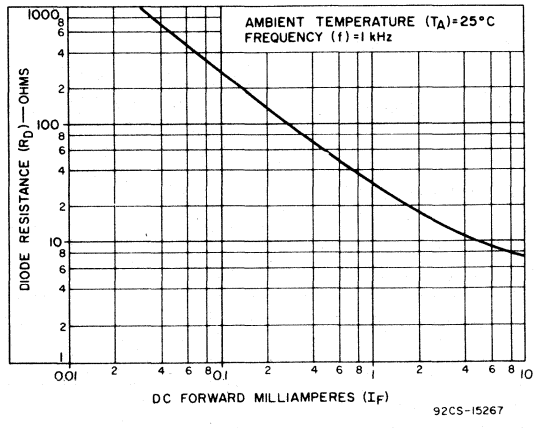


Fig. 7 - Diode resistance (any diode) vs DC forward current

TYPICAL CHARACTERISTICS

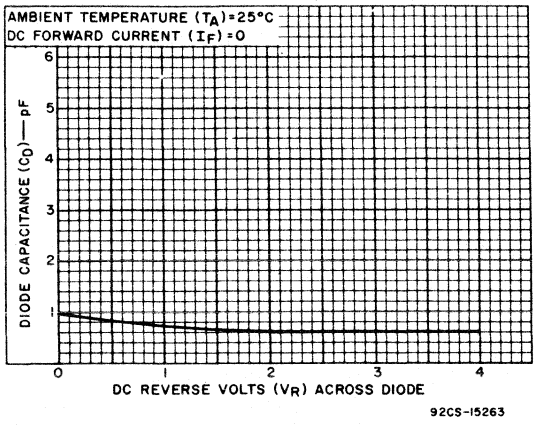


Fig. 8 - Diode capacitance (diodes 1,2,3,4,5) vs reverse voltage

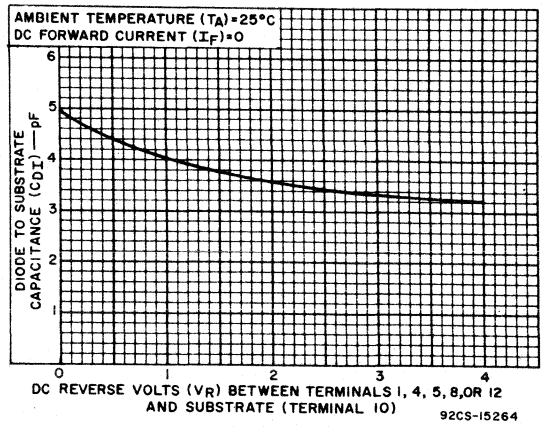
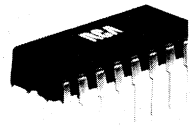


Fig. 9 - Diode-to-substrate capacitance vs reverse voltage

CA3141E



16-Lead Dual-in-Line
Plastic Package
(E suffix)

H-1622

High-Voltage Diode Array

For Commercial, Industrial, and Military Applications

Features:

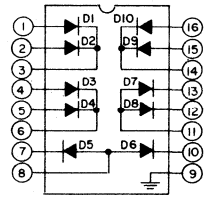
- *Matched monolithic construction - V_F for each diode pair matched to within 0.55 mV (typ.) at I_F = 1 mA*
- *Low diode capacitance - 0.3 pF (typ.) at V_R = 2 V*
- *High diode-to-substrate breakdown voltage - 30 V (min.)*
- *Low reverse (leakage) current - 100 nA (max.)*

Applications:

- *Balanced modulators or demodulators*
- *Analog switches*
- *High-voltage diode gates*
- *Current ratio detectors*

The RCA-CA3141E High-Voltage Diode Array consists of ten general-purpose high-reverse-breakdown diodes. Six diodes are internally connected to form three common-cathode diode pairs, and the remaining four diodes are internally connected to form two common-anode diode pairs. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the CA3141E extremely useful for a wide variety of applications in communications and switching systems.

The CA3141 is supplied in the 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).



92CS-27173

Fig. 1 — Terminal assignment.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

PEAK INVERSE VOLTAGE (PIV) ..... 30 V

PEAK DIODE-TO-SUBSTRATE VOLTAGE ..... 30 V

PEAK FORWARD SURGE CURRENT [I_F (SURGE)] ..... 100 mA

DC FORWARD CURRENT (I_F) ..... 25 mA

DISSIPATION:

Any one diode unit ..... 50 mW

Total Package:

Up to 55° C ..... 650 mW

For $T_A > 55°$ C ..... Derate linearly at 6.67 mW/° C

AMBIENT TEMPERATURE RANGE:

Operating ..... −55 to +125° C

Storage ..... −65 to +150° C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max. ..... +265° C

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTIC	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNIT
DC Forward Voltage Drop, V_F	I_F (Anode)	100 μA	–	0.7	0.9	V
		1 mA	–	0.78	1	
		10 mA	–	0.93	1.2	
DC Reverse Breakdown Voltage, $V_{(BR)R}$	$I_F = -10$ μA		30	50	–	V
DC Breakdown Voltage Between Any Diode and Substrate, $V_{(BR)DI}$	$I_{DI} = 10$ μA		30	50	–	V
DC Reverse (Leakage) Current, I_R	$V_F = -20$ V		–	–	100	nA
DC Reverse (Leakage) Current Between Any Diode and Substrate, I_{DI}	$V_{DI} = 20$ V		–	–	100	nA
Magnitude of Diode Offset Voltage Between Diode Pairs	$V_{DI} = 20$ V, $I_{FA} = 1$ mA		–	0.55	–	mV
Temperature Coefficient of Forward Voltage Drop, $\Delta V_F/\Delta T$	$I_F = 1$ mA		–	−1.5	–	mV/°C
Reverse Recovery Time, t_{rr}	$I_F = 2$ mA, $I_R = 2$ mA		–	50	–	ns
Diode Capacitance, C_D			See Fig. 5			pF
Diode Anode-to-Substrate Capacitance, C_{DAI}			See Fig. 6			pF
Diode Cathode-to-Substrate Capacitance, C_{DCI}			See Fig. 7			pF
Magnitude of Cathode-to-Anode Current Ratio, $\lvert I_{FC}/I_{FA} \rvert$	$I_{FA} = 1$ mA, $V_{DS} = 10$ V		0.9	0.96	–	

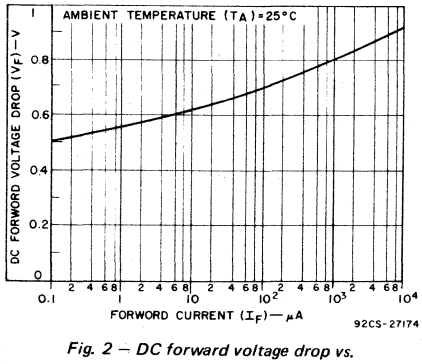


Fig. 2 – DC forward voltage drop vs. forward current.

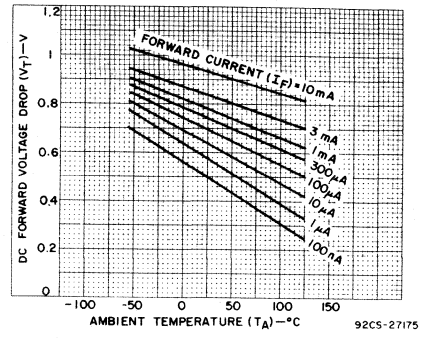


Fig. 3 – DC forward voltage drop vs. ambient temperature.

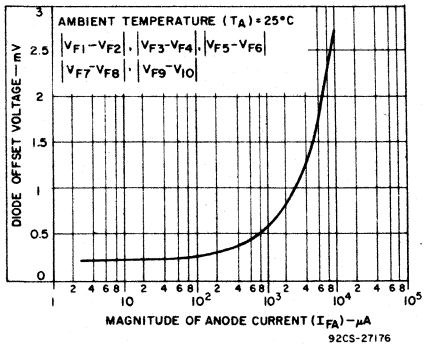


Fig. 4 — Diode offset voltage vs. magnitude of anode current.

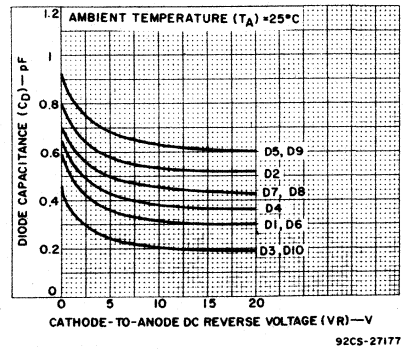


Fig. 5 — Diode capacitance vs. cathode-to-anode reverse voltage.

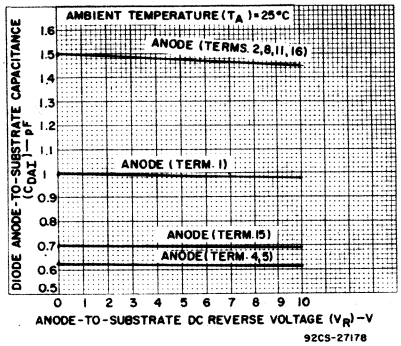


Fig. 6 — Diode anode-to-substrate capacitance vs. reverse voltage.

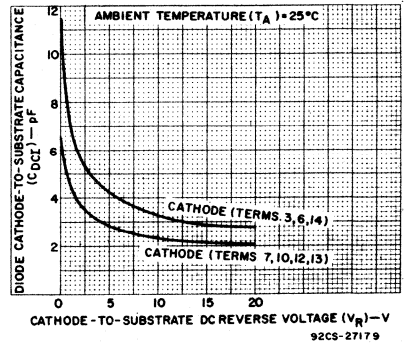


Fig. 7 — Diode cathode-to-substrate capacitance vs. cathode-to-substrate DC reverse voltage.

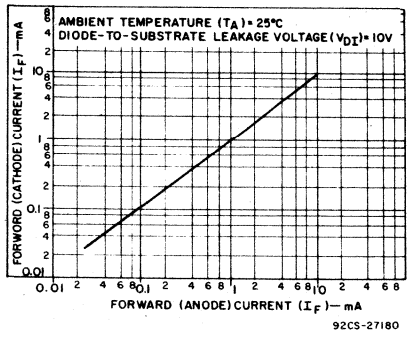


Fig. 8 — Forward (cathode) current vs. forward (anode) current.

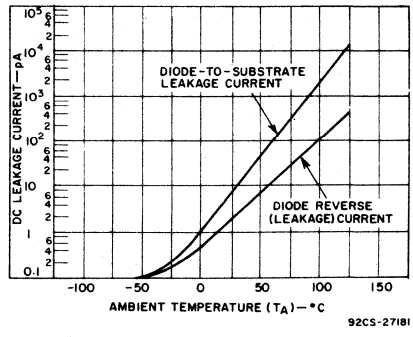
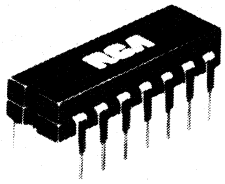


Fig. 9 — DC leakage current vs. ambient temperature.



14-Lead Dual-In-Line
Plastic Package
(E Suffix)
H-1517

High-Current N-P-N Transistor Arrays

Four Individual Sealed-Junction
High-Current N-P-N Transistors

Features:

- **High Current — 1 A**
- **High Breakdown Voltage:**
  CA1725 = 80 V dc min. $V_{(BR)CES}$ @ I_C = 10 μA
  CA1724 = 70 V dc min. $V_{(VR)CES}$ @ I_C = 10 μA

The RCA-CA1724 and -CA1725 are high-current n-p-n transistor arrays each containing 4 individual sealed-junction high-current n-p-n transistors. They are intended for high-current driver applications.

These devices are alike except for breakdown voltage ratings.

The CA1724 and CA1725 are supplied in a 14-lead dual-in-line plastic package and operate over the full military temperature range of −55°C to +125°C.

- **Silicon Nitride Passivated**
- **Platinum Silicide Ohmic Contacts**
- **Electrically similar and pin compatible with industry types MPQ3724, MPQ3725; FPQ3724, FPQ3725; DH3724, DH3725; SP3724, SP3725 in similar packages**

Applications

- **High-Current LED Driver**
- **High-Voltage Switching**
- **Relay and Solenoid Driver**
- **Lamp Driver**

Comparison of High Current N-P-N Arrays

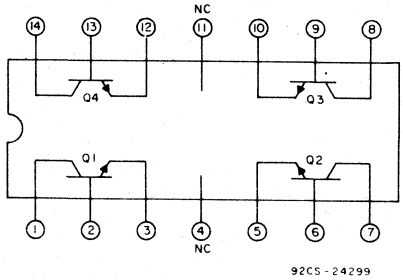
CHARACTERISTIC	CA1725			CA3725			CA3138A		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
V_{CEO}(sus)	50	58	—	50	—	—	15	20	—
$V_{(BR)CBO}$	80	94	—	80	—	—	25	60	—
$V_{(BR)EBO}$	6	6.9	—	6	—	—	5	7.2	—
h_{FE} @ 1A	20	25	—	20	—	—	40	170	—
h_{FE} @ 500 mA	30	35	—	30	—	—	95	170	—
h_{FE} @ 100 mA	35	40	—	35	—	—	80	160	450
V_{CE}(SAT) @ 500 mA	—	0.38	0.5	—	—	0.5	—	0.26	0.4
t_{ON} @ 500 mA	—	38	—	—	—	40	—	31	—
t_{OFF} @ 500 mA	—	185	—	—	—	60	—	105	—
C_{EB}	—	100	—	—	95	—	—	77	—
C_{CB}	—	12.5	—	—	12	—	—	18	—

CA1724, CA1725 Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristic	Test Conditions	LIMITS						Units
		CA1724			CA1725			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector-to-Emitter Sustaining Voltage, $V_{CEO(sus)}$*	I_C = 10 mA, I_B = 0	40	45	—	50	58	—	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$	I_C = 10 μA, I_B = 0	70	75	—	80	94	—	V
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	70	75	—	80	94	—	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	6	6.9	—	6	6.9	—	V
Base-to-Emitter Saturation Voltage, $V_{BE(sat)}$*	I_C = 500 mA, I_B = 50 mA	0.75	0.89	1.0	0.75	0.9	1.0	V
Collector-to-Emitter Saturation Voltage $V_{CE(sat)}$	I_C = 500 mA, I_B = 50 mA	—	0.36	0.5	—	0.38	0.5	V
Collector-Cutoff Current, I_{CBO}	V_{CB} = 40 V, I_E = 0	—	0.3	1.7	—	0.3	1.7	μA
Static Forward-Current Transfer Ratio (Beta), h_{FE}	I_C = 100 mA V_{CE} = 1.0 V I_C = 500 mA, V_{CE} = 1.0 V I_C = A, V_{CE} = 1.0 V	35 30 20	40 35 25	— — —	35 30 20	40 35 25	— — —	
Turn-On Time (See (Test Ckt.Fig.6), t_{on}	I_C = 500 mA, I_{B_1} = 50 mA	—	38	—	—	38	—	ns
Turn-Off Time (See Test Ckt.Fig.6), t_{off}	I_C = 500mA, I_{B_1} = I_{B_2} = 50 mA	—	185	—	—	185	—	ns
Emitter-to-Base Capacitance, C_{eb}	I_C = 0 V_{EB} = 0.5 V	—	102	—	—	100	—	pF
Collector-to-Base Capacitance, C_{cb}	I_E = 0, V_{CB} = 10 V	—	14	—	—	12.5	—	pF

* Pulse Conditions: width = 300 μs; duty cycle = 1%.



92CS-24299

Fig. 1—Terminal diagram (top view).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		CA1724	CA1725	
COLLECTOR-TO-EMITTER VOLTAGE With Base Open	V_{CEO}	40	50	V
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	70	80	V
EMITTER-TO-BASE VOLTAGE With Collector Open	V_{EBO}	6		V
COLLECTOR CURRENT	I_C	1.0		A
POWER DISSIPATION:	P_D			
For Each Transistor		1.0		W
Total Package		2.0		W
At T_A above 25°C derate linearly (Total Package)		20		mw/°C
AMBIENT TEMPERATURE RANGE:				
Operating		−55 to +125		°C
Storage		−65 to +150		°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/32" (3.17 mm) from seating plane for 10 s max.		300		°C

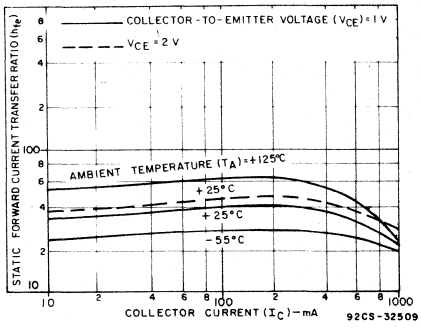


Fig. 2—Static forward current transfer ratio as a function of collector current.

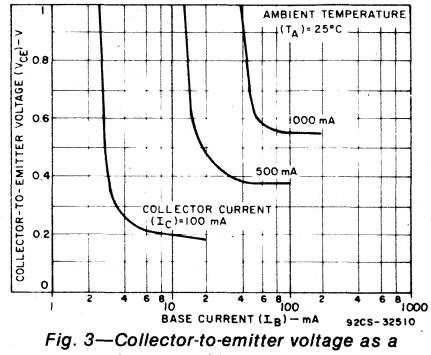


Fig. 3—Collector-to-emitter voltage as a function of base current.

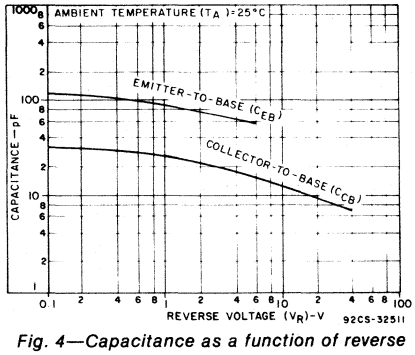


Fig. 4—Capacitance as a function of reverse voltage.

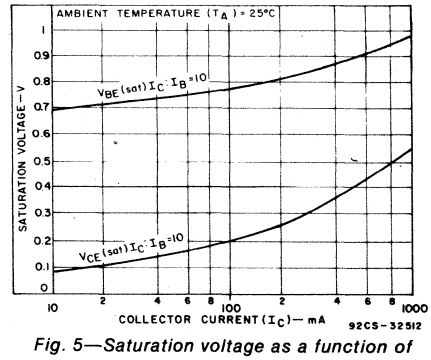


Fig. 5—Saturation voltage as a function of collector current.

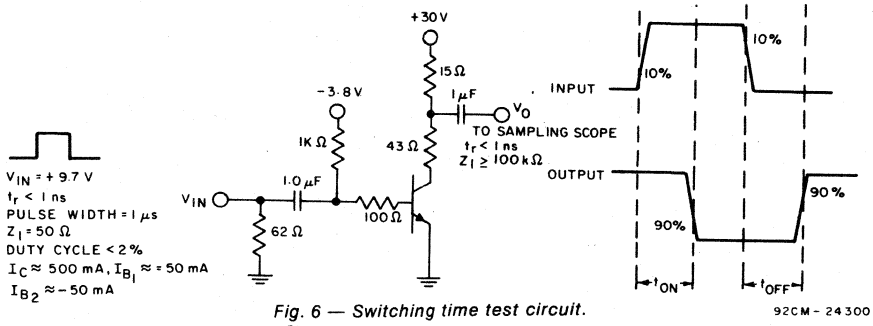


Fig. 6 — Switching time test circuit.

CA3018, CA3018A

12-Lead TO-5

H-1463

General-Purpose Transistor Arrays

Two Isolated Transistors and
a Darlington-Connected Transistor Pair

For Low-Power Applications at Frequencies
from DC Through the VHF Range

Features:

- *Matched monolithic general purpose transistors*
- *H_{FE} matched ± 10%*
- *V_{BE} matched ± 2 mV CA3018A (± 5m V CA3018)*
- *Operation from DC to 120 MHz*
- *Wide operating current range*
- *CA3018A performance characteristics controlled from 10 μA to 10 mA*
- *Low noise figure - 3.2 dB typical at 1KHz*
- *Full military temperature range capability (−55 to +125° C)*

Applications

- *General use in signal processing systems in DC through VHF range*
- *Custom designed differential amplifiers*
- *Temperature compensated amplifiers*
- *See RCA Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated-Circuit Transistor Array" for suggested applications.*

The CA3018 and CA3018A consist of four general purpose silicon n-p-n transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low-power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

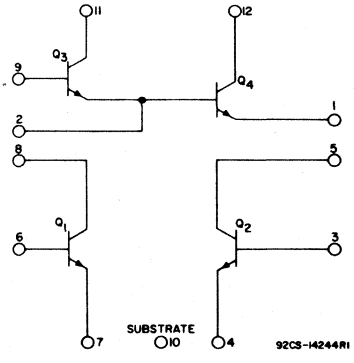


Fig. 1 — Schematic Diagram for CA3018 and CA3018A

CA3018, CA3018A

Maximum Ratings, Absolute-Maximum Values, at TA=25°C

	CA3018	CA3018A	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	450	450	mW
Derate at 5 mW/°C for $T_A > 85°C$			
Temperature Range:			
Operating	-55 to + 125	-55 to + 125	°C
Storage	-65 to + 150	-65 to + 150	°C

The following ratings apply for each transistor in the device:

	CA3018	CA3018A	
Collector-to-Emitter Voltage, V_{CEO}	15	15	V
Collector-to-Base Voltage, V_{CBO}	20	30	V
Collector-to-Substrate Voltage, V_{CIO}*	20	40	V
Emitter-to-Base Voltage, V_{EBO}	5	5	V
Collector Current, I_C	50	50	mA

*The collector of each transistor of the CA3018 and CA3018A is isolated from the substrate by an integral diode. *The substrate (terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

Characteristics apply for each transistor in the CA3018 and CA3018A as specified.

ELECTRICAL CHARACTERISTICS at T_A = 25°C	SYMBOLS	SPECIAL TEST CONDITIONS	CA3018 LIMITS			CA3018A LIMITS			Units	CHARACTERISTICS CURVES
			Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS										
Collector-Cutoff Current	I_{CBO}	V_{CB}=10V, I_E=0	–	0.002	100	–	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE}=10V, I_B=0	–	See Curve	5	–	See Curve	0.5	μA	3
Collector-Cutoff Current Darlington Pair	I_{CEOD}	V_{CE}=10V, I_B=0	–	–	–	–	–	5	μA	–
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	15	24	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10μA, I_E=0	20	60	–	30	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=10μA, I_C=0	5	7	–	5	7	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C=10μA, I_{CI}=0	20	60	–	40	60	–	V	–
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B=1mA, I_C=10mA	–	0.23	–	–	0.23	0.5	V	–
Static Forward Current Transfer Ratio	h_{FE}	V_{CE}=3V, I_C=10mA V_{CE}=3V, I_C=1mA V_{CE}=3V, I_C=10μA	– 30 –	100 100 54	– 200 –	50 60 30	100 100 54	– 200 –	– – –	4
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)		V_{CE}=3V, I_{C1}=I_{C2}=1mA	0.9	0.97	–	0.9	0.97	–	–	4
Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	h_{FED}	V_{CE}=3V I_C=1mA V_{CE}=3V I_C=100μA	1500 –	5400 –	– –	2000 1000	5400 2800	– –	–	5
Base-to-Emitter Voltage	V_{BE}	V_{CE}=3V I_E=1mA V_{CE}=3V I_E=10mA	– –	0.715 0.800	– –	0.600 –	0.715 0.800	0.800 0.900	V	6
Input Offset Voltage	$\lvert V_{BE_1} - V_{BE_2} \rvert$	V_{CE}=3V, I_E=1mA	–	0.48	5	–	0.48	2	mV	6,8
Temperature Coefficient: Base-to-Emitter Voltage Q_1,Q_2	$\frac{\lvert \Delta V_{BE} \rvert}{\Delta T}$	V_{CE}=3V, I_E=1mA	–	-1.9	–	–	-1.9	–	mV/°C	7
Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	V_{BED} (V_{9-1})	V_{CE}=3V I_E=10mA V_{CE}=3V I_E=1mA	– –	1.46 1.32	– –	– 1.10	1.46 1.32	1.60 1.50	V	9
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3,Q_4	$\frac{\lvert \Delta V_{BED} \rvert}{\Delta T}$	V_{CE}=3V, I_E=1mA	–	4.4	–	–	4.4	–	mV/°C	10
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert V_{BE_1} - V_{BE_2} \rvert}{\Delta T}$	V_{CC}=+6V, V_{EE}=-6V, I_{C1}=I_{C2}=1mA	–	10	–	–	10	–	μV/°C	–

CA3018, CA3018A

ELECTRICAL CHARACTERISTICS, (CONT'D)

DYNAMIC CHARACTERISTICS										
Low Frequency Noise Figure	NF	f=1 KHz, V_{CE}=3V, I_C=100μA Source resistance=1 KΩ	–	3.25	–	–	3.25	–	dB	11(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Forward Current-Transfer Ratio	h_{fe}	f=1kHz, V_{CE}=3V, I_C=1mA	–	110	–	–	110	–	–	12
Short-Circuit Input Impedance	h_{ie}		–	3.5	–	–	3.5	–	KΩ	12
Open-Circuit Output Impedance	h_{oe}		–	15.6	–	–	15.6	–	μmho	12
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		–	$1.8x10^{-4}$	–	–	$1.8x10^{-4}$	–	–	12
Admittance Characteristics:										
Forward Transfer Admittance	Y_{fe}	f=1MHz, V_{CE}=3V, I_C=1mA	–	31-j1.5	–	–	31-j1.5	–	mmho	13
Input Admittance	Y_{ie}		–	0.3+j0.04	–	–	0.3+j0.04	–	mmho	14
Output Admittance	Y_{oe}		–	0.001+j0.03	–	–	0.001+j0.03	–	mmho	15
Reverse Transfer Admittance	Y_{re}		See Curve			See Curve			mmho	16
Gain-Bandwidth Product	f_T	V_{CE}=3V, I_C=3mA	300	500	–	300	500	–	MHz	17
Emitter-to-Base Capacitance	C_{EB}	V_{EB}=3V, I_E=0	–	0.6	–	–	0.6	–	pF	–
Collector-to-Base Capacitance	C_{CB}	V_{CB}=3V, I_C=0	–	0.58	–	–	0.58	–	pF	–
Collector-to-Substrate Capacitance	C_{CI}	V_{CI}=3V, I_C=0	–	2.8	–	–	2.8	–	pF	–

STATIC CHARACTERISTICS

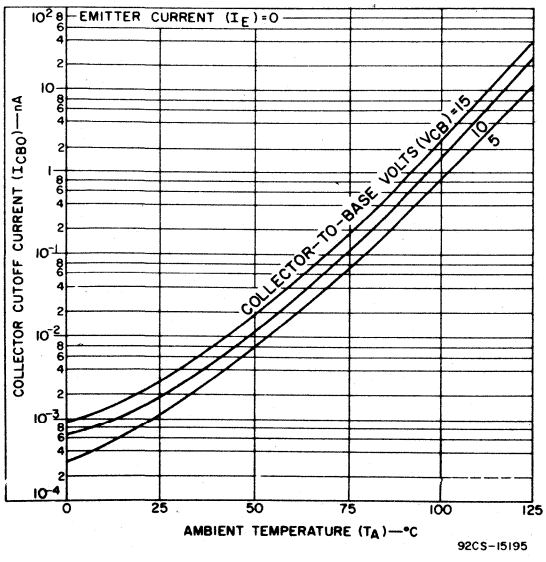


Fig.2 - Typical Collector-To-Base Cutoff Current vs Ambient Temperature for Each Transistor.

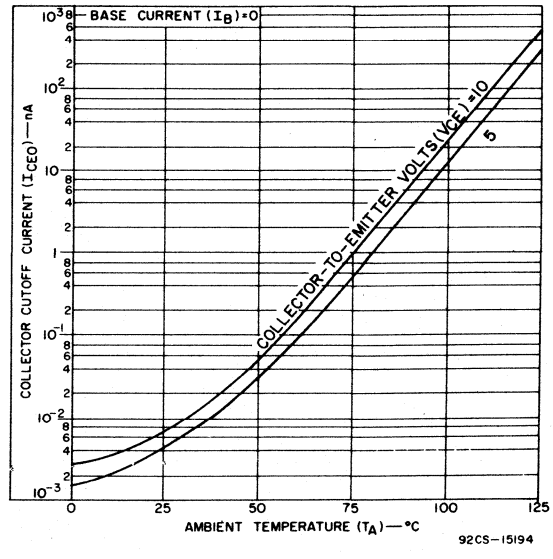


Fig.3 - Typical Collector-To-Emmiter Cutoff Current vs Ambient Temperature for Each Transistor.

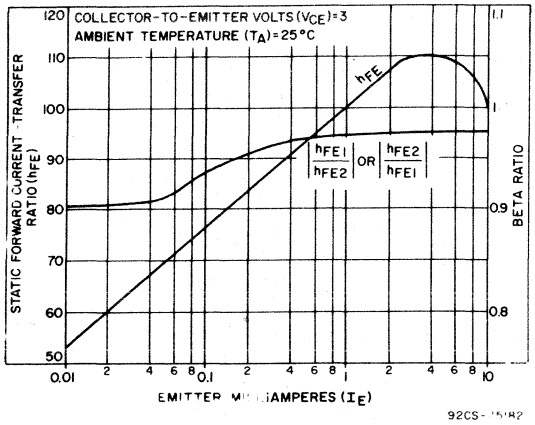


Fig.4 - Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q, and Q_2 vs Emitter Current.

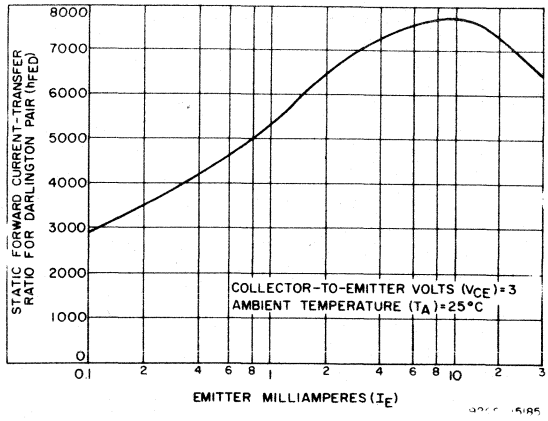


Fig.5 - Typical Static Forward Current - Transfer Ratio for Darlington-connected Transisters Q_3 and Q_4 vs Emitter Current.

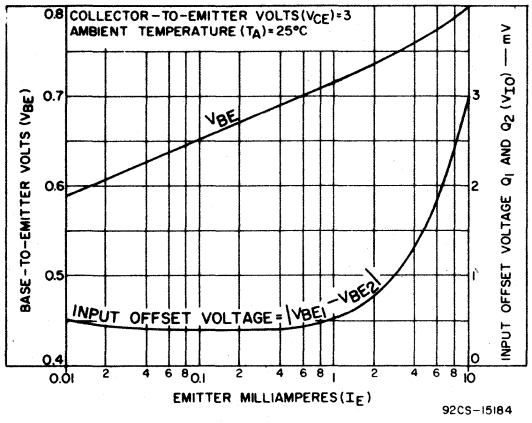


Fig.6 - Typical Static Base-to-Emitter Voltage Characteristic and Input Offset Voltage for Q_1 and Q_2 vs Emitter Current.

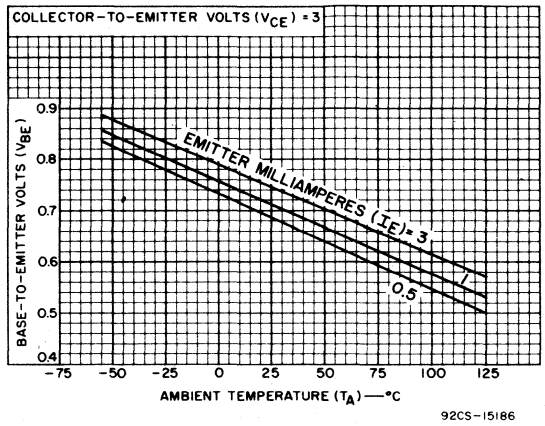


Fig.7 - Typical Base-To-Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature

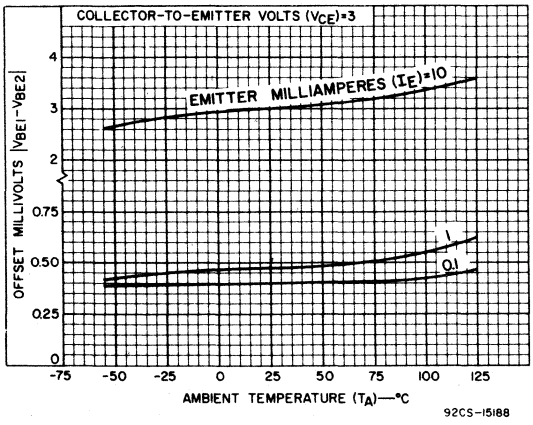


Fig.8 - Typical Offset Voltage Characteristic vs Ambient Temperature

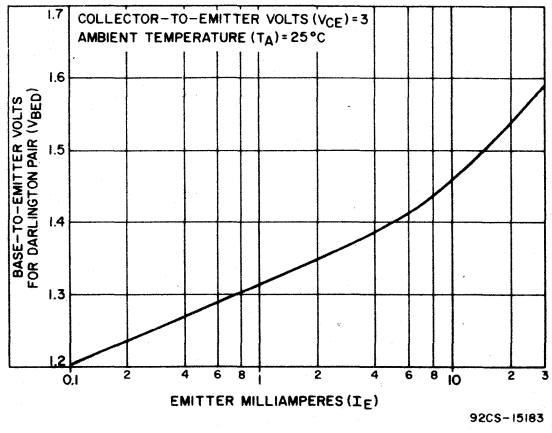


Fig.9 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Emitter Current

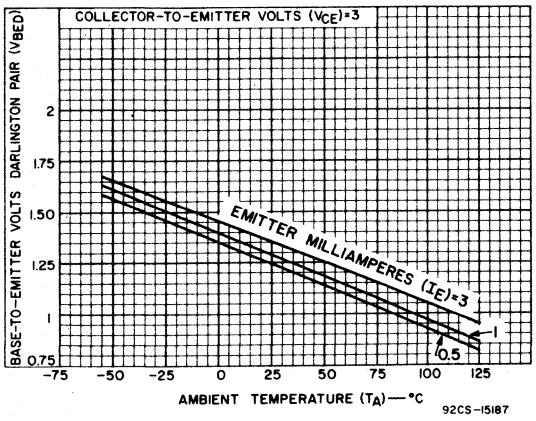


Fig.10 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Ambient Temperature.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

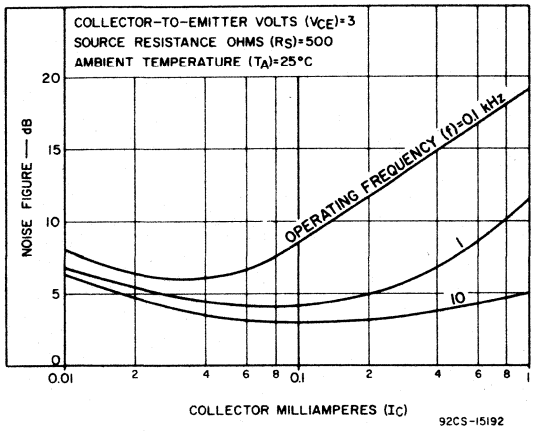


Fig.11(a) - Noise Figure vs Collector Current, R_S = 500 Ω.

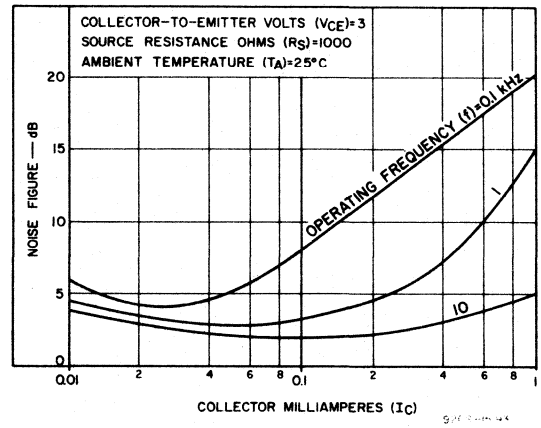


Fig.11(b) - Noise Figure vs Collector Current, R_S = 1 KΩ.

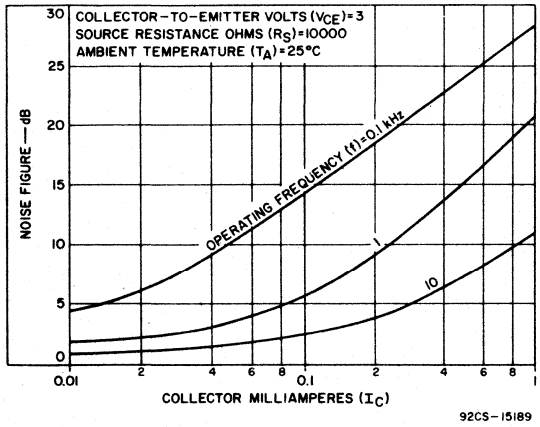


Fig.11(c) - Noise Figure vs Collector Current, R_S = 10 KΩ.

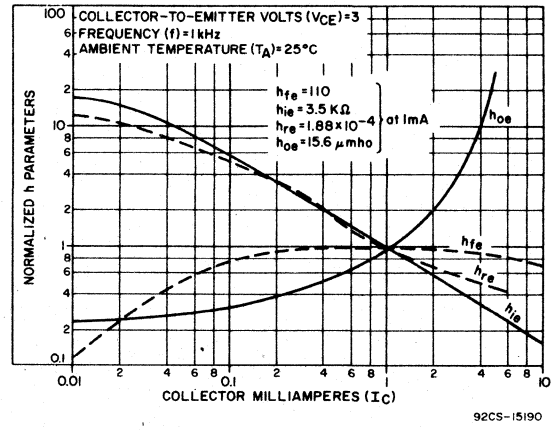


Fig.12 - Forward Current-Transfer Ratio (h_{fe}), Short-Circuit Input Impedance (h_{ie}), Open-Circuit Output Impedance (h_{oe}), and Open-Circuit Reverse Voltage-Transfer Ratio (h_{re}) vs Collector Current

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

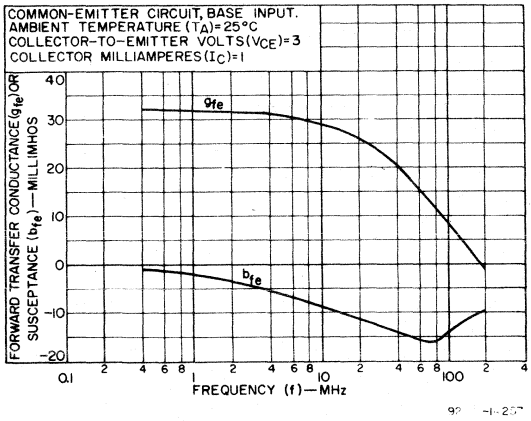


Fig. 13 - Forward Transfer Admittance (Y_{fe})

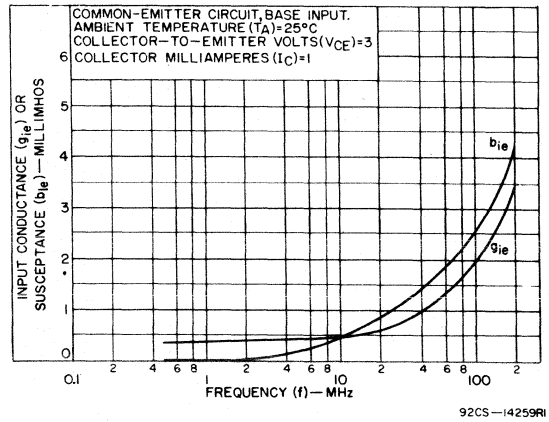


Fig. 14 - Input Admittance (Y_{ie})

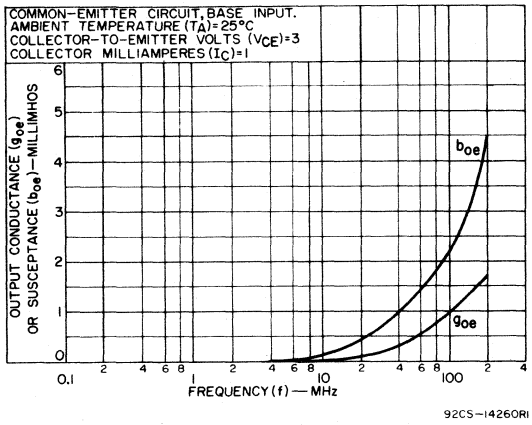


Fig. 15 - Output Admittance (Y_{oe})

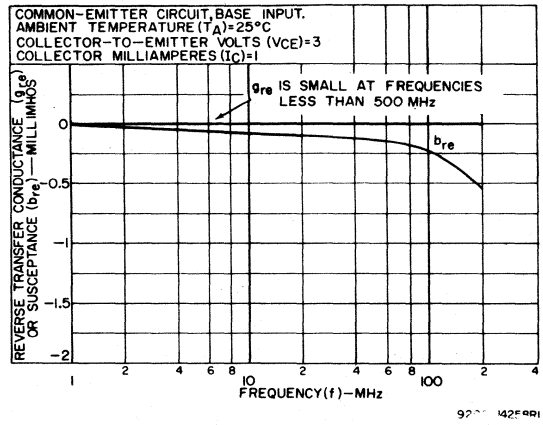


Fig. 16 - Reverse Transfer Admittance (Y_{re})

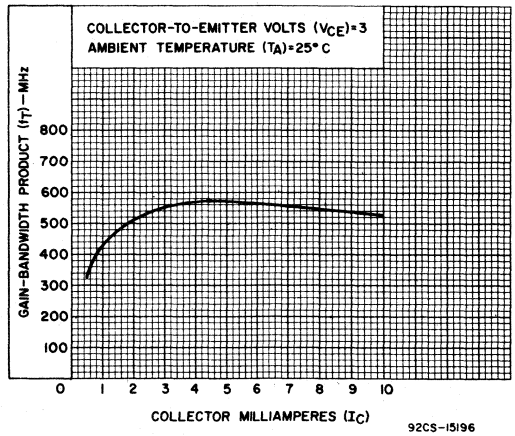
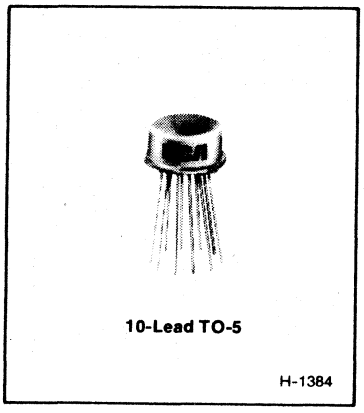


Fig. 17 - Typical Gain-Bandwidth Product (f_T) vs Collector Current

CA3036



10-Lead TO-5

H-1384

Dual Darlington Array

Features

- *Two independent low-noise wide-band amplifier channels*
- *Particularly useful for preamplifier and low-level amplifier applications in single-channel and stereo systems*
- *Wide application in low-noise industrial instrumentation amplifiers*

Applications

- *Stero phonograph preamplifiers*
- *Low-level stereo and single-channel amplifier stages*
- *Low-noise, emitter-follower differential amplifiers*
- *Operational amplifier drivers*

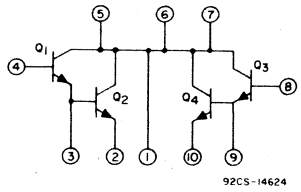


Fig. 1 - Schematic diagram for CA3036.

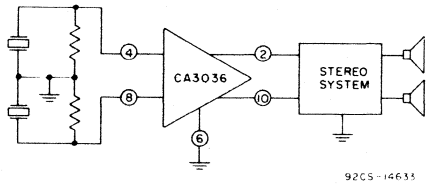


Fig. 2 - Block diagram of stereo system using CA3036 as phono preamplifier.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

POWER DISSIPATION, P:
- ANY ONE TRANSISTOR ..... 300 max. mW
- TOTAL FOR ARRAY ..... 300 max. mW

TEMPERATURE RANGE:
- OPERATING ..... −55 to +125°C
- STORAGE ..... − 65 to +200°C

THE FOLLOWING RATINGS APPLY FOR EACH TRANSISTOR IN THE ARRAY:
- COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO} ..... 15 max. V
- COLLECTOR-TO-BASE VOLTAGE, V_{CBO} ..... 30 max. V
- EMITTER-TO-BASE VOLTAGE, V_{EBO} ..... 5 max. V
- COLLECTOR CURRENT, I_C ..... 50 max. mA

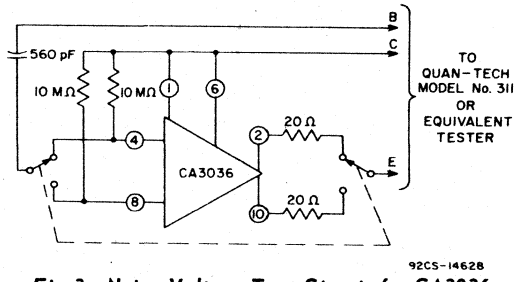


Fig.3 - Noise Voltage Test Circuit for CA3036.

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$

CHARACTERISTICS		SYMBOLS	TEST CONDITIONS	LIMITS TYPE CA3036			UNITS
				Min.	Typ.	Max.	
For Each Transistor (Q_1, Q_2, Q_3, Q_4)	Collector-Cutoff Current	I_{CBO}	$V_{CB} = 5V$, $I_E = 0$	--	--	0.5	μA
	Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	--	--	5	μA
	Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	15	20	--	V
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\ \mu A$, $I_E = 0$	30	44	--	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\ \mu A$, $I_C = 0$	5	6	--	V
For Either Input Transistor (Q_1 or Q_3)	Static Forward Current-Transfer Ratio	h_{FE}	I_{C1} or $I_{C3} = 1$ mA	30	82	--	--
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO(D)}$	I_{E2} or $I_{E4} = 10\ \mu A$	10	12.6	--	V
	Static Forward Current-Transfer Ratio	$h_{FE(D)}$	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ $= 1$ mA	1000	4540	--	--
For Each Input Transistor (Q_1 or Q_3)	Short-Circuit Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, I_{C1} or $I_{C3} = 1$ mA	--	82	--	--
	Short-Circuit Input Impedance	h_{ie}		--	2.6K	--	Ω
	Open-Circuit Output Admittance	h_{oe}		--	7	--	μmho
	Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		--	9.8×10^{-5}	--	--
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Short-Circuit Forward Current-Transfer Ratio	$h_{fe(D)}$	f = 1 kHz, $I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ $= 1$ mA	--	1300	--	--
	Short-Circuit Input Impedance	$h_{ie(D)}$		--	82K	--	Ω
	Open-Circuit Output Admittance	$h_{oe(D)}$		--	108	--	μmho
	Open-Circuit Reverse Voltage-Transfer Ratio	$h_{re(D)}$		--	2.7×10^{-3}	--	--
	Voltage Gain	$A_{(D)}$		--	26	--	dB
	Power Gain	$G_{p(D)}$		--	47	--	dB
	Noise Voltage See Fig.3 for Test Circuit	E_N	f = 100 Hz	--	0.2	3	$\frac{\mu V(rms)}{\sqrt{f(Hz)}}$
			f = 1 kHz	--	0.05	0.3	
			f = 10 kHz	--	0.012	0.1	
For Either Input Transistor (Q_1 or Q_3)	Forward Transfer Admittance	y_{fe}	f = 50 MHz, I_{C1} or $I_{C3} = 2$ mA	--	0.68 + j 7.9	--	mmho
	Input Admittance (Output Short-Circuited)	y_{ie}		--	4.14 + j 5.95	--	mmho
	Output Admittance (Input Short-Circuited)	y_{oe}		--	1.94 + j 2.64	--	mmho
	Reverse Transfer Admittance (Input Short-Circuited)	y_{re}		--	Negligible	--	mmho
For either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Input Admittance (Output Short-Circuited)	$y_{ie(D)}$	f = 50 MHz, $I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ $= 2$ mA	--	1.71 + j 2.8	--	mmho
	Output Admittance (Input Short-Circuited)	$y_{oe(D)}$		--	3.96 + j 2.6	--	mmho
	Gain-Bandwidth Product	$f_{T(D)}$		150	200	--	MHz

CA3045, CA3046 Types

14-Lead Dual-In-Line Ceramic

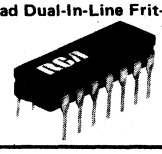
H-1553

14-Lead Dual-In-Line Plastic

H-1517

14-Lead Dual-In-Line Frit-Seal

Hermetic Package



H-1806

General-Purpose Transistor Arrays

THREE ISOLATED TRANSISTORS AND ONE DIFFERENTIALLY-CONNECTED TRANSISTOR PAIR

For Low-Power Applications at Frequencies from DC through the VHF Range

Features

- Two matched pairs of transistors
  V_{BE} matched ± 5 mV
  Input offset current 2 μA max. at I_C = 1 mA
- 5 general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure - - 3.2 dB typ. at 1 kHz
- Full military temperature range for CA3045
  -55 to +125°C

The CA3045 and CA3046 each consist of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

The CA3045 is supplied in a 14-lead dual-in-line hermetic (welded-seal) ceramic package and the CA3045F in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

The CA3046 is electrically identical to the CA3045 but is supplied in a dual-in-line plastic package for applications requiring only a limited temperature range.

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.

The CA3045 and CA3046 are available in the packages shown below

Package	Suffix Letter	CA3045	CA3046
14-Lead Dual-In-Line Plastic	E		√
14-Lead Dual-In-Line Ceramic	D	√	
14-Line Dual-In-Line Frit-Seal Ceramic	F	√	
Beam Lead	L	√	
Chip	H	√	

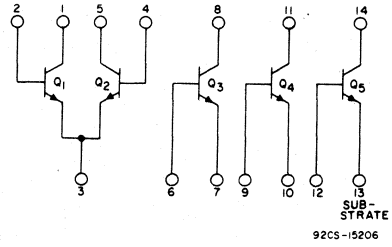


Fig.1 - Schematic diagram.

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C	CA3045		CA3046, CA3045F		
	Each Transistor	Total Package	Each Transistor	Total Package	
Power Dissipation:					
T_A up to 55°C	–	–	300	750	mW
T_A > 55°C	–	–	Derate at 6.67		mW/°C
T_A up to 75°C	300	750	–	–	mW
T_A > 75°C	Derate at 8		–	–	mW/°C
Collector-to-Emitter Voltage, V_{CEO}	15	–	15	–	V
Collector-to-Base Voltage, V_{CBO}	20	–	20	–	V
Collector-to-Substrate Voltage, V_{CIO}*	20	–	20	–	V
Emitter-to-Base Voltage, V_{EBO}	5	–	5	–	V
Collector Current	50	–	50	–	mA
Temperature Range:					
Operating	–55 to +125		–55 to +125		°C
Storage	–65 to +150		–65 to +150		°C
Lead Temperature (During Soldering): At distance 1/16 ±1/32" (1.59 ±0.79 mm) from case for 10 seconds max.	+265		+265		°C

* The collector of each transistor of the CA3045 and CA3046 is isolated from the substrate by an integral diode. *The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046 MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES FIG.
STATIC CHARACTERISTICS							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60	-	V	-
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7	-	V	-
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	-	See curve	0.5	μA	3
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE}	V_{CE} = 3 V, I_C = 10 mA	-	100	-	-	4
		V_{CE} = 3 V, I_C = 1 mA	40	100	-	-	
		V_{CE} = 3 V, I_C = 10 μA	-	54	-	-	
Input Offset Current for Matched Pair Q_1 and Q_2. $\lvert I_{IO_1} - I_{IO_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.3	2	μA	5
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_E = 1 mA	-	0.715	-	V	6
		V_{CE} = 3 V, I_E = 10 mA	-	0.800	-		
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV	6,8
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV	6,8
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	-1.9	-	mV/°C	7
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1 mA, I_C = 10 mA	-	0.23	-	V	-
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	1.1	-	μV/°C	8

CA3045, CA3046 Types

ELECTRICAL CHARACTERISTICS (Cont'd.)

DYNAMIC CHARACTERISTICS							
Low-Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA Source Resistance = 1 kΩ	-	3.25	-	dB	9(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:							
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	110	-	-	10
Short-Circuit Input Impedance	h_{ie}		-	3.5	-	kΩ	
Open-Circuit Output Impedance	h_{oe}		-	15.6	-	μmho	
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	1.8×10^{-4}	-	-	
Admittance Characteristics:							
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	-	31-j1.5	-	-	11
Input Admittance	Y_{ie}		-	0.3+j0.04	-	-	12
Output Admittance	Y_{oe}		-	0.001+j0.03	-	-	13
Reverse Transfer Admittance	Y_{re}		-	See curve	-	-	14
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	550	-	-	15
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	-	0.6	-	pF	-
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	-	0.58	-	pF	-
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	-	2.8	-	pF	-

STATIC CHARACTERISTICS

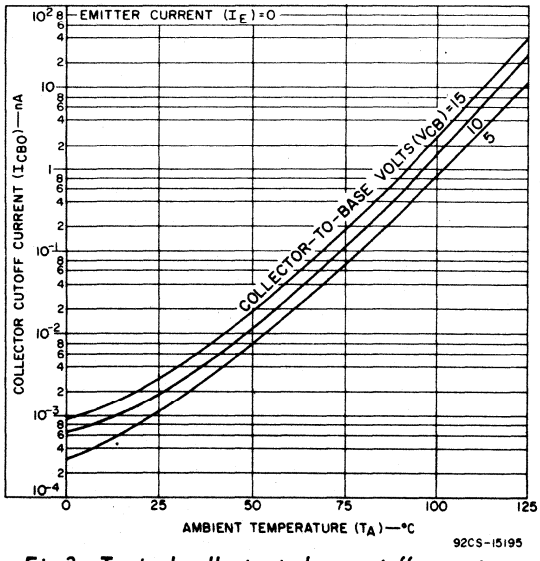


Fig.2 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

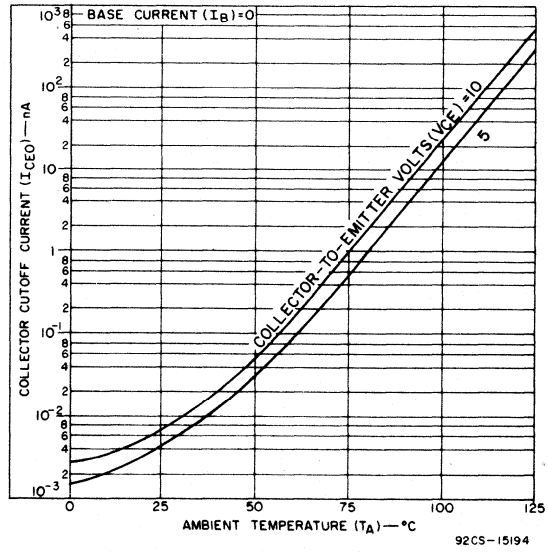


Fig.3 - Typical collector-to-emitter cutoff current vs ambient temperature for each transistor.

STATIC CHARACTERISTICS

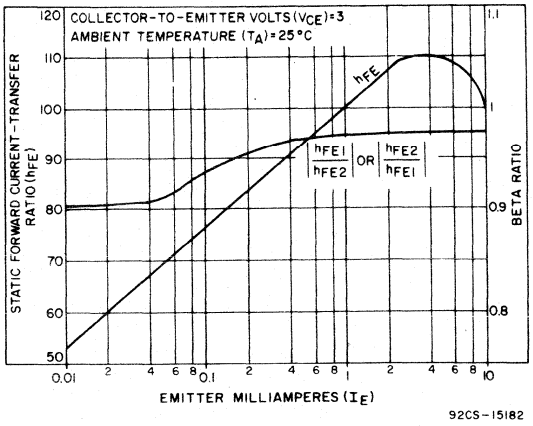


Fig.4 - Typical static forward current-transfer ratio and beta ratio for transistors Q_1 and Q_2 vs emitter current.

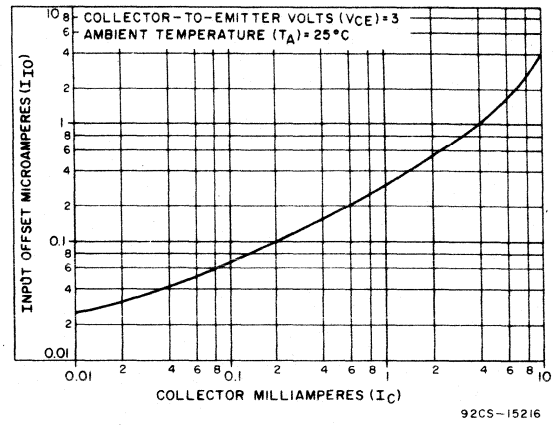


Fig.5 - Typical input offset current for matched transistor pair Q_1Q_2 vs collector current.

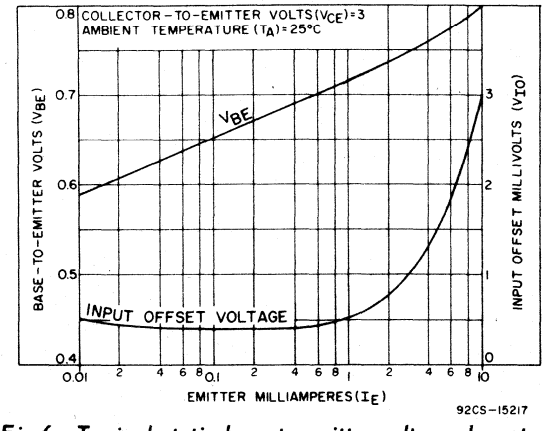


Fig.6 - Typical static base-to-emitter voltage characteristic and input offset voltage for differential pair and paired isolated transistors vs emitter current.

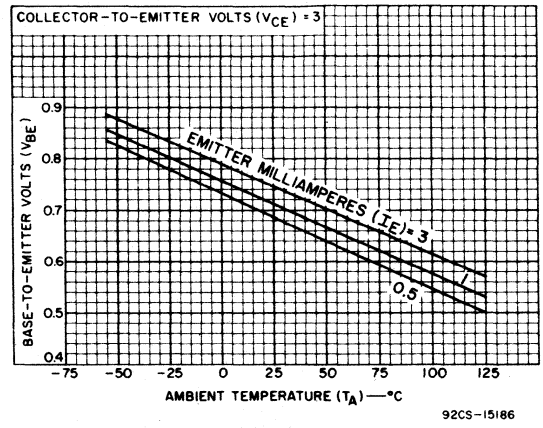


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

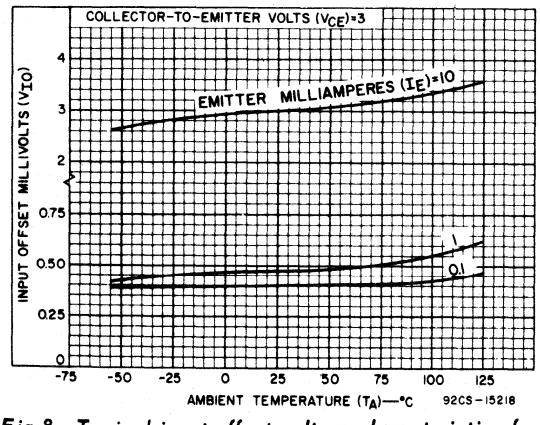


Fig.8 - Typical input offset voltage characteristics for differential pair and paired isolated transistors vs ambient temperature.

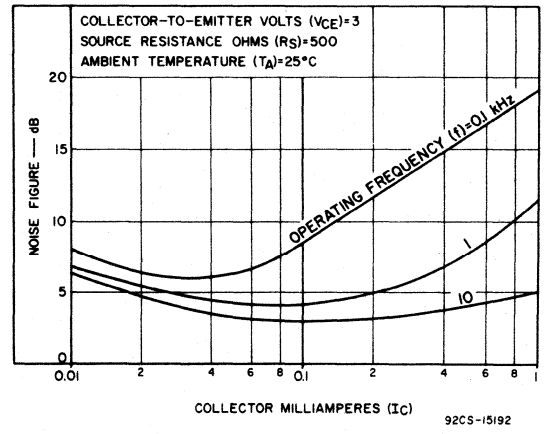


Fig.9(a) - Typical noise figure vs collector current.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

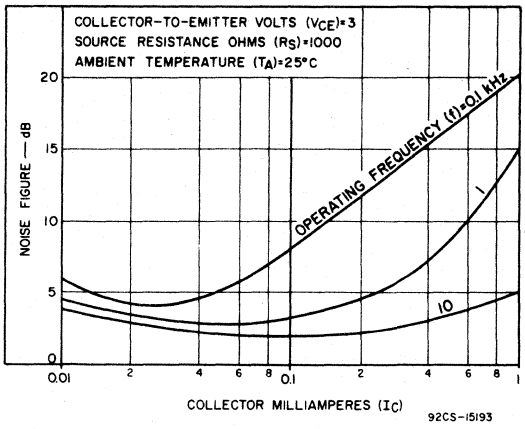


Fig.9(b) - Typical noise figure vs collector current.

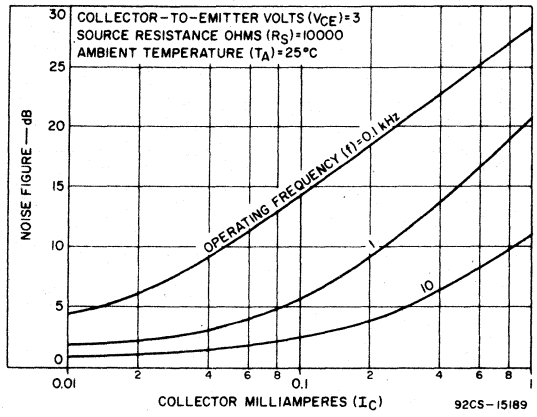


Fig.9(c) - Typical noise figure vs collector current.

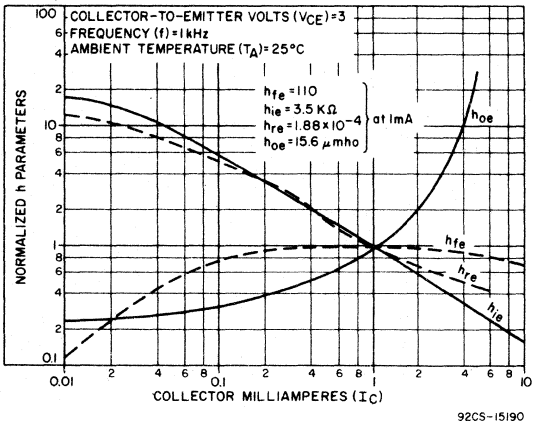


Fig.10 - Typical normalized forward current-transfer ratio, short-circuit input impedance, open-circuit output impedance, and open-circuit reverse voltage-transfer ratio vs collector current.

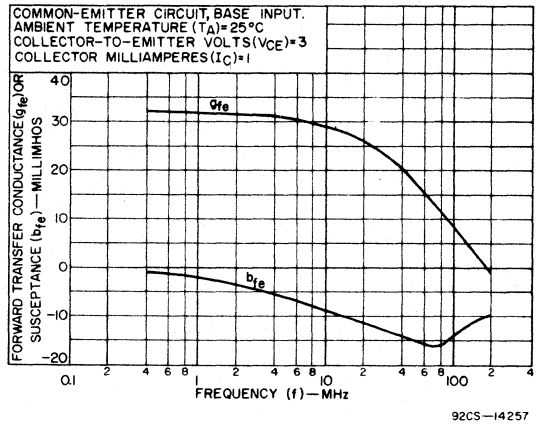


Fig.11 - Typical forward transfer admittance vs frequency.

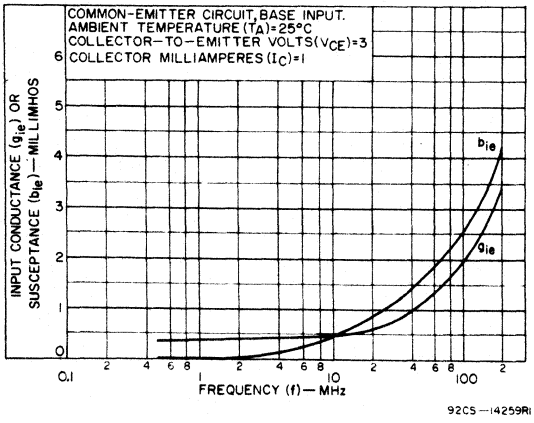


Fig.12 - Typical input admittance vs frequency.

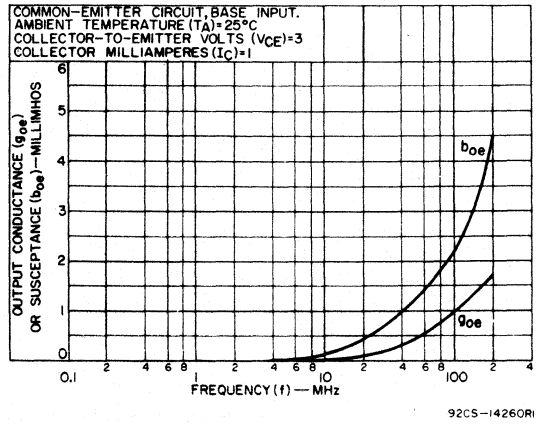


Fig.13 - Typical output admittance vs frequency.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

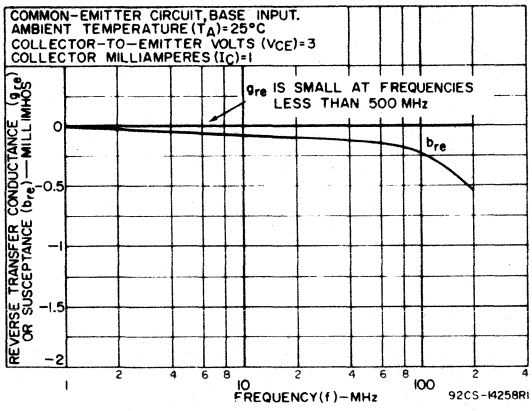


Fig.14 - Typical reverse transfer admittance vs frequency.

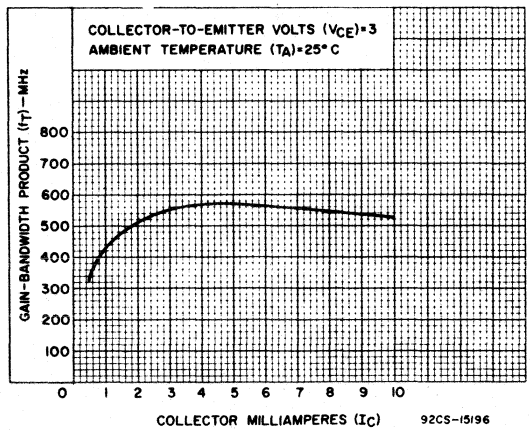
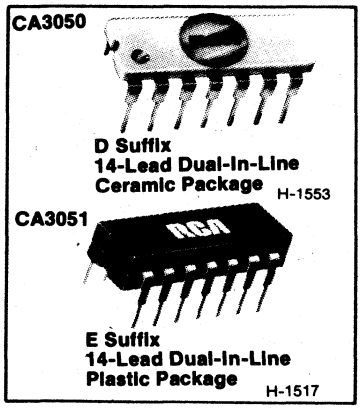


Fig.15 - Typical gain-bandwidth product vs collector current.

CA3050, CA3051



Dual Differential Amplifiers

Two Darlington-Connected Differential Amplifiers with Diode Bias String

For Low-Power Applications at Frequencies from DC to 20 MHz

Features:

- *Input offset current - 70 nA max.*
- *Input bias current - 500 nA max.*
- *Input offset voltage - 5 mV max.*
- *Input impedance - 460 kΩ typ.*
- *Independently accessible inputs and outputs*

Applications

- *Matched dual amplifiers*
- *Dual sense amplifiers*
- *Dual Schmitt triggers*
- *Dual multivibrators*
- *Doubly balanced detectors and modulators*
- *Balanced quadrature detectors*
- *Synthesizer mixers*
- *Product detectors*

The CA3050 and CA3051 each consists of two differential amplifiers with associated constant current transistors on a common substrate. Each amplifier is driven by Darlington-connected emitter follower inputs to provide high input impedance, low bias current, and low offset current. A string of diodes is included to provide temperature-compensated bias to the constant current transistors and a low impedance bias point for the inputs to the differential amplifiers when a single power supply is used.

The CA3050 is supplied in an hermetic 14-lead Dual-In-Line ceramic package rated for operation over the full military temperature range of −55°C to +125°C.

The CA3051 is supplied in a Dual-In-Line plastic package for applications requiring only a limited temperature range of −25°C to +85°C.

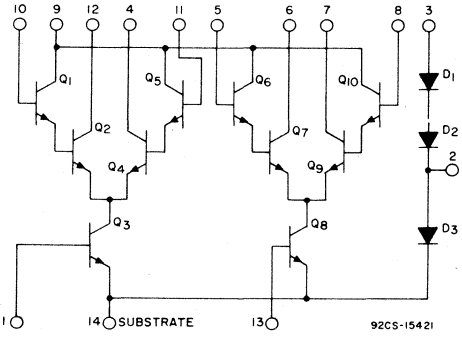


Fig. 1 — Schematic diagram.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C

	CA3050	CA3051	
Power Dissipation, P:			
Any one transistor	150	150	mW
Total package	900	750	mW
For T_A > 55°C, Derate at	8	6.67	mW/°C
Temperature Range:			
Operating	-55 to +125	-40 to +85	°C
Storage	-65 to +150	-65 to +150	°C
LEAD TEMPERATURE (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C		

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3050 and CA3051 is isolated from the substrate by an integral diode. *The substrate (terminal 14) must be more negative than all collectors to maintain isolation between transistors and to provide for normal transistor action.*

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 3 is +5 to -2 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	–	*	*	*	*	*	*	*	*	*	*	*	*	+1 -5
2			+5 -2	*	*	*	*	*	*	*	*	*	*	+1 -1
3				*	*	*	*	*	*	*	*	*	*	+3 -1
4					*	*	*	*	*	+14 -2.5 Note 3	+14 -2.5 Note 4	*	*	+20 -1
5						+2.5 -14 Note 1	+2.5 -14 Note 1	+10 -10	+1 -20	*	*	*	*	+16 -
6							*	+14 -2.5 Note 2	*	*	*	*	*	+20 -1
7								+14 -2.5 Note 2	*	*	*	*	*	+20 -1
8									+1 -20	*	*	*	*	+16 -
9										+20 -1	+20 -1	*	*	+20 -1
10											+10 -10	+2.5 -14 Note 3	*	+16 -
11												+2.5 -14 Note 4	*	+16 -
12														+20 -1
13														+1 -5
14														Ref. Substrate

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	0.1
2	50	50
3	50	1
4	50	1
5	5	0.1
6	50	1
7	50	1
8	5	0.1
9	50	1
10	5	0.1
11	5	0.1
12	50	1
13	5	0.1
14	100	5

Note 1: This rating is important only when terminal 5 is more positive than terminal 8.

Note 2: This rating is important only when terminal 8 is more positive than terminal 5.

Note 3: This rating is important only when terminal 10 is more positive than terminal 11.

Note 4: This rating is important only when terminal 11 is more positive than terminal 10.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

CA3050, CA3051

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	LIMITS CA3050/CA3051			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC								
Amplifier Characteristics								
Input Offset Voltage	V_{IO}		–	–	1.5	5	mV	2a,b
Input Offset Current	I_{IO}		–	–	7	70	nA	3a,b
Input Bias Current	I_I		–	–	200	500	nA	4a,b
Quiescent Operating Current Ratio	$\frac{(I_4+I_{12})}{I_3}$ or $\frac{(I_6+I_7)}{I_3}$	V_{CC} = + 6 V, I_3 = 2 mA	–	0.9	1.00	1.13	–	5a,b
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 50 μA	–	–	0.645	0.700	V	6
		V_{CE} = 3 V, I_C = 1 mA	–	–	0.725	0.800		
		V_{CE} = 3 V, I_C = 3 mA	–	–	0.760	0.850		
		V_{CE} = 3 V, I_C = 10 mA	–	–	0.805	0.900		
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	–	–	-1.9	–	mV/°C	7
Transistor Characteristics								
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	0.002	100	nA	8
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V	–
DYNAMIC								
Transistor Characteristics								
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	–	–	0.78	–	pF	9
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	–	–	0.47	–	pF	9
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	–	–	1.92	–	pF	9
Amplifier Characteristics								
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 5 V, I_C = 3 mA	–	–	600	–	MHz	10
Forward Transadmittance (With single-ended input and output)	$\lvert y_{21} \rvert$	V_{CC} = 10 V, I_3 = 2 mA, f = 1 MHz	11	7	9	11	mmho	11
Bandwidth at -3 dB Point	BW	V_{CC} = 10 V, I_3 = 2 mA	11	–	4.3	–	MHz	11
Input Impedance	Z_{IN}	V_{CC} = 10 V, I_3 = 2 mA, f = 1 KHz	12	–	460	–	kΩ	12
Output Impedance	Z_{OUT}	I_3 = 2 mA, f = 1 KHz	13	–	170	–	kΩ	13
Common-Mode Rejection Ratio	CMR	I_3 = 2 mA, f = 1 KHz	–	–	65	–	dB	–
AGC Range	AGC	I_3 = 2 mA, f = 1 KHz Terminal No.3 Grounded	11	–	60	–	dB	–

TYPICAL STATIC CHARACTERISTICS

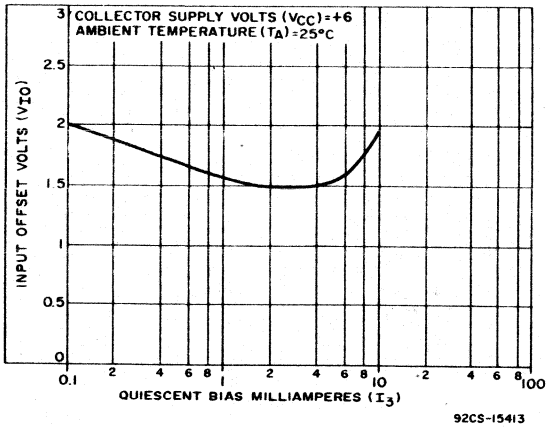


Fig.2(a) - Typical input offset voltage vs quiescent bias current.

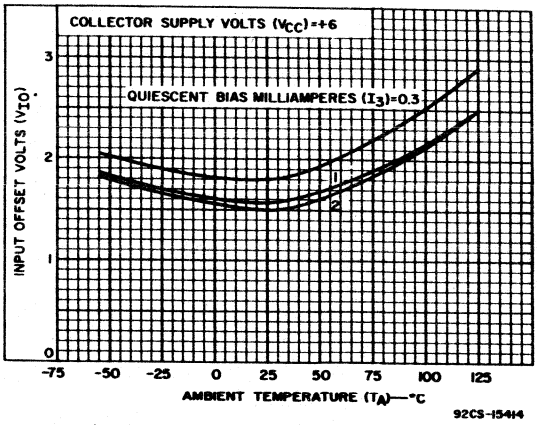


Fig.2(b) - Typical input offset voltage vs ambient temperature.

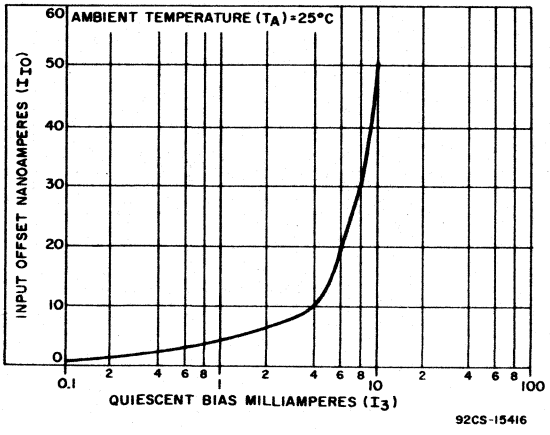


Fig.3(a) - Typical input offset current vs quiescent bias current.

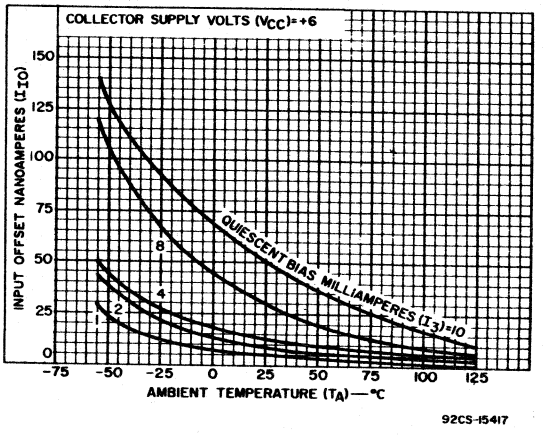


Fig.3(b) - Typical input offset current vs ambient temperature.

STATIC CHARACTERISTICS

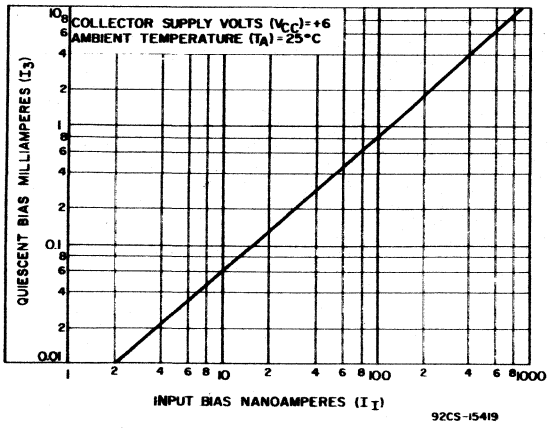


Fig.4(a) - Typical quiescent bias current vs input bias current.

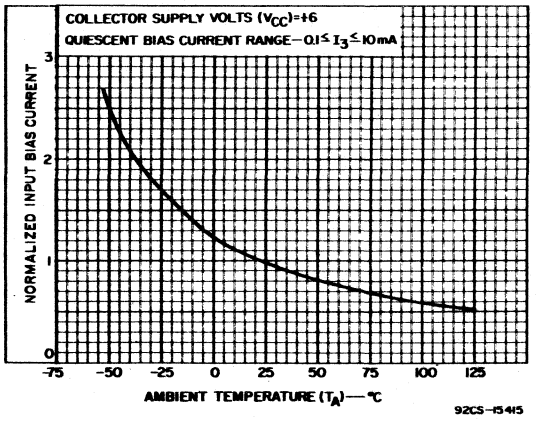


Fig.4(b) - Typical normalized input bias current vs ambient temperature.

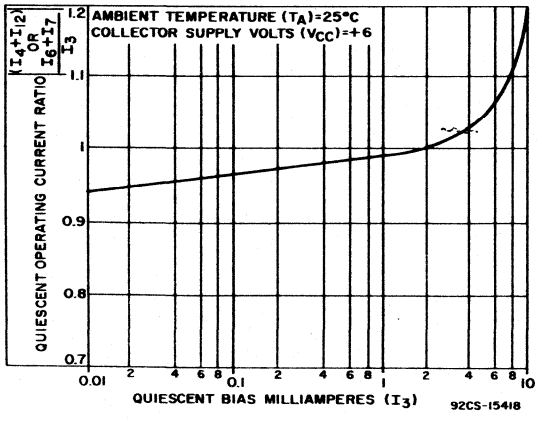


Fig.5(a) - Typical quiescent operating current ratio vs quiescent bias current.

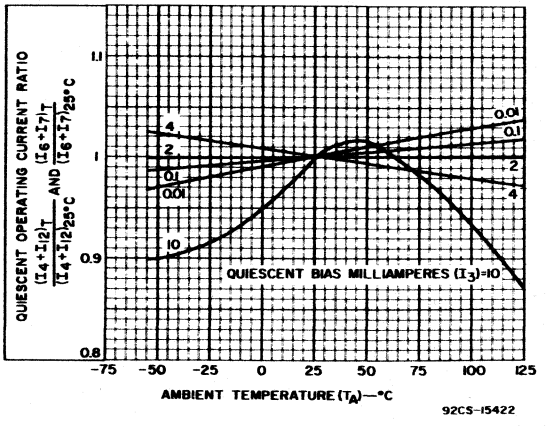


Fig.5(b) - Typical quiescent operating current ratio vs ambient temperature.

STATIC CHARACTERISTICS

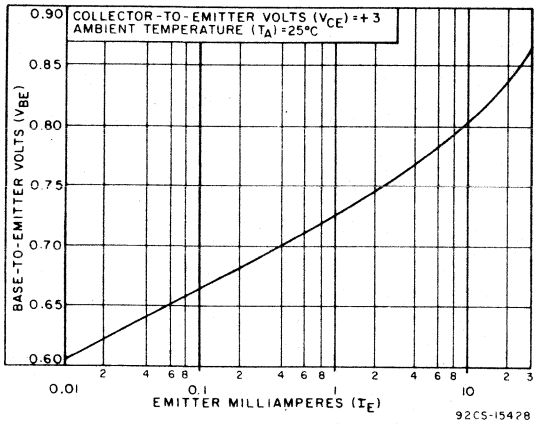


Fig.6 - Typical static base-to-emitter voltage characteristic vs emitter current for all transistors and forward diode voltage drops.

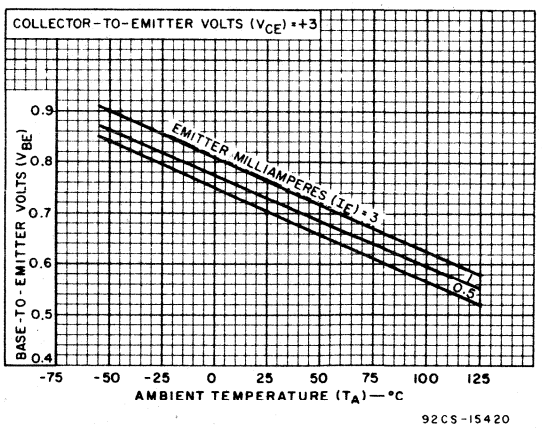


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

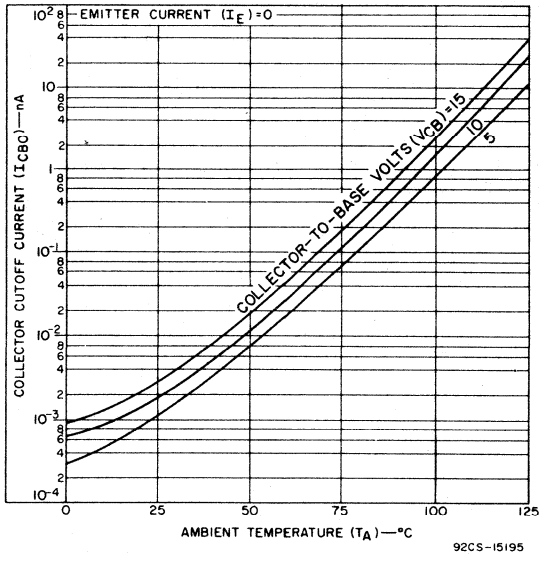


Fig.8 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

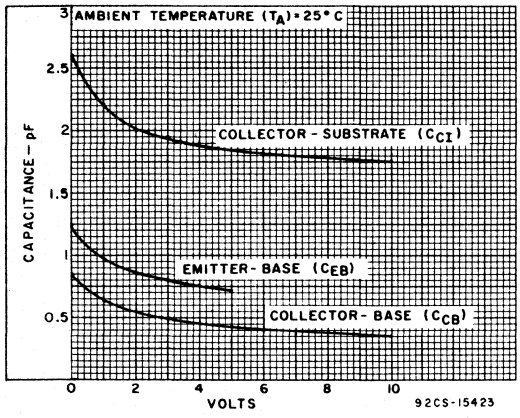


Fig.9 - Typical capacitance for each transistor.

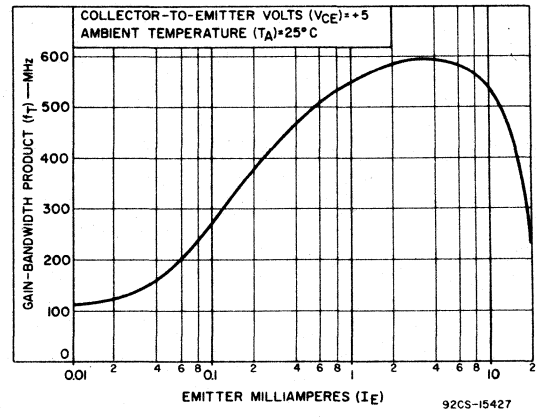
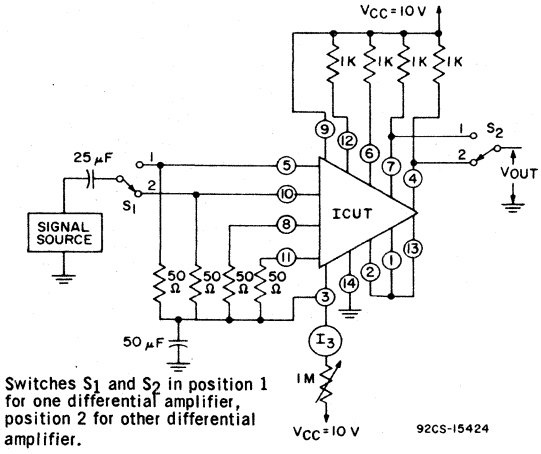


Fig.10 - Typical gain-bandwidth product (f_T) for each transistor vs emitter current.



Switches S_1 and S_2 in position 1 for one differential amplifier, position 2 for other differential amplifier.

Fig.11(a) - Test circuit for forward transadmittance, -3 dB bandwidth, and AGC range.

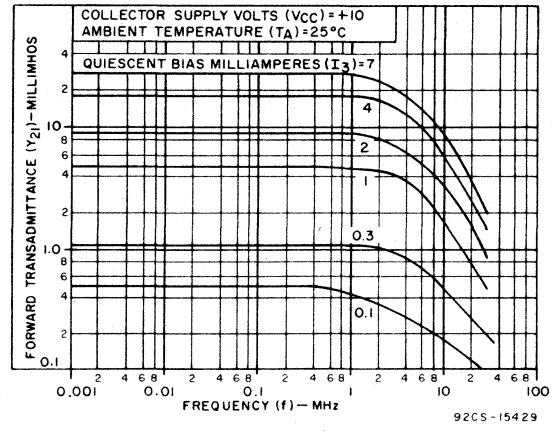


Fig.11(b) - Typical differential amplifier forward transadmittance with single-ended output vs frequency.

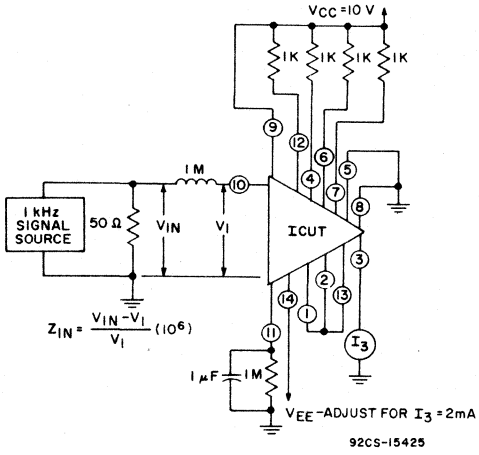


Fig.12(a) - Test circuit for input impedance.

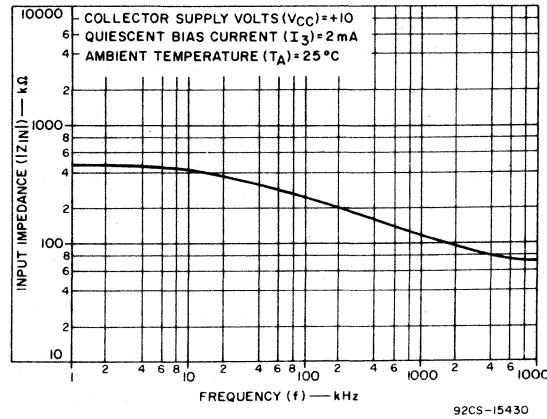
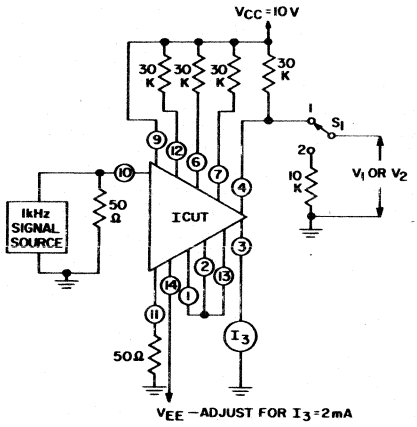


Fig.12(b) - Typical input impedance vs frequency with output short-circuited.

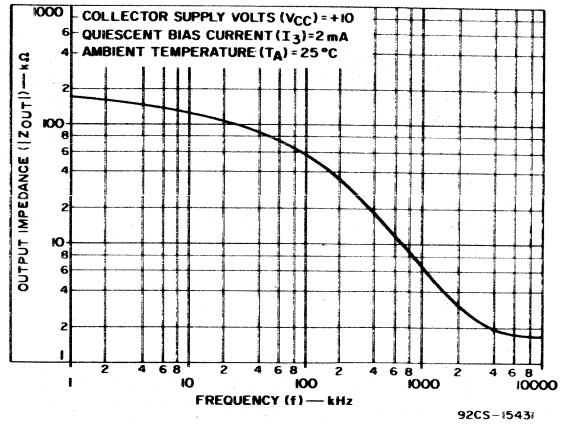
DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR



$$Z_{OUT} = \frac{(30K \times 10K)\frac{V_2}{V_1}}{\frac{V_2}{V_1}(30K+10K)-10K}$$

92CS-15426

Fig.13(a) - Test circuit for output impedance.

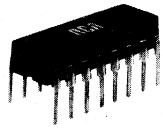


92CS-15431

Fig.13(b) - Typical output impedance vs frequency with input short-circuited.

CA3083

16-Lead Dual-In-Line Frit-Seal (Hermetic) Package H-1807



16-Lead Dual-In-Line Plastic Package H-1622

General-Purpose High-Current N-P-N Transistor Array

Features:

- *High I_C: 100 mA max.*
- *Low V_{CEsat} (at 50 mA): 0.7V max.*
- *Matched pair (Q1 and Q2) - V_{IO} (V_{BE} matched): ± 5 mV max. I_{IO} (at 1 mA): 2.5 μA max.*
- *5 independent transistors plus separate substrate connection*

Applications:

- *Signal processing and switching systems operating from DC to VHF*
- *Lamp and relay driver*
- *Differential amplifier*
- *Temperature-compensated amplifier*
- *Thyristor firing*
- *See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Circuit Transistor Array" for suggested applications*

RCA-CA3083 is a versatile array of five high-current (to 100mA) n-p-n transistors on a common monolithic substrate. In addition, two of these transistors (Q1 and Q2) are matched at low currents (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design. The CA3083 is supplied in a 16-lead dual-in-line frit-seal ceramic package. The CA3083 is also available in chip form.

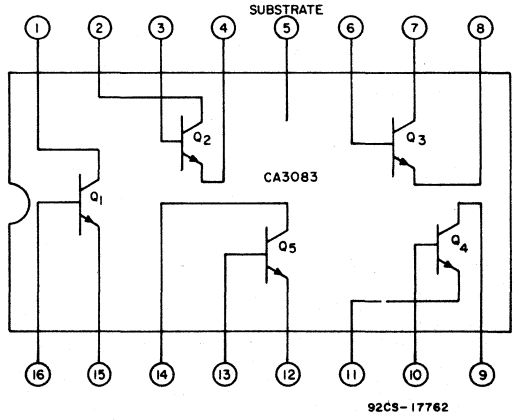


Fig. 1 — Functional diagram of the CA3083.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:

Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C

Ambient Temperature Range:

Operating	−55 to +125	°C
Storage	−65 to +150	°C

Lead Temperature (During Soldering):

At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 seconds max.	265	°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage (V_{CEO})	15	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})■	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

■ The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
For Each Transistor:							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	–	5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	–	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 10mA	2	40	76	–	
		V_{CE} = 3V, I_C = 50mA	2	40	75	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 50mA, I_B = 5mA	4	–	0.40	0.70	V
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 10 mA		–	450	–	MHz
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	7	–	1.2	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	8	–	0.7	2.5	μA

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

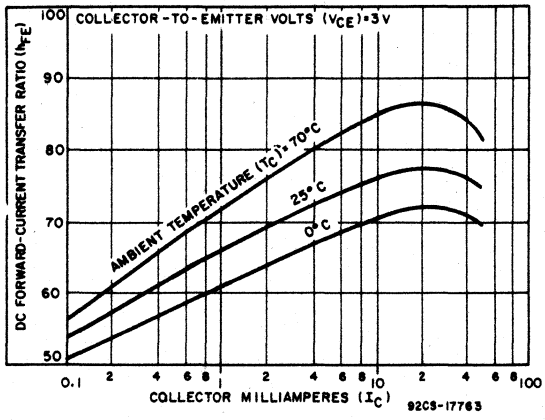


Fig.2 – h_{FE} vs I_C

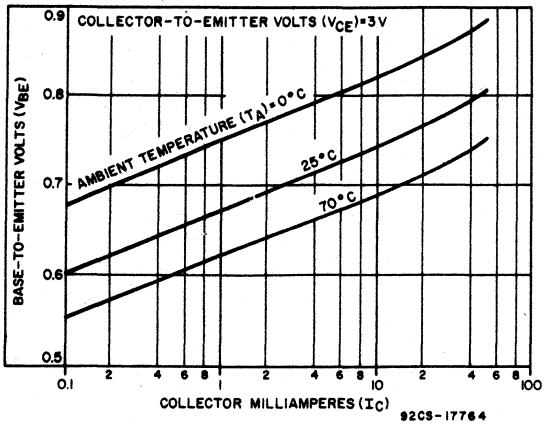


Fig.3 – V_{BE} vs I_C

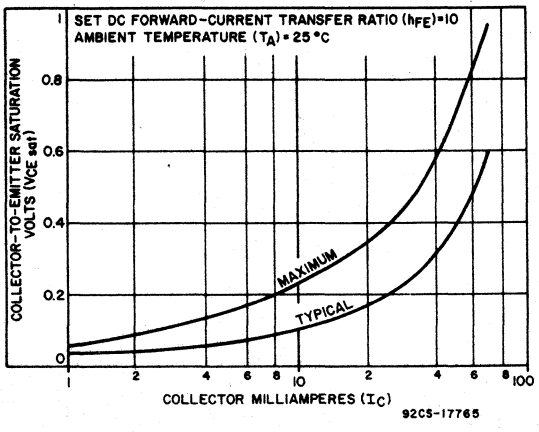


Fig.4 – V_{CEsat} vs I_C at 25°C

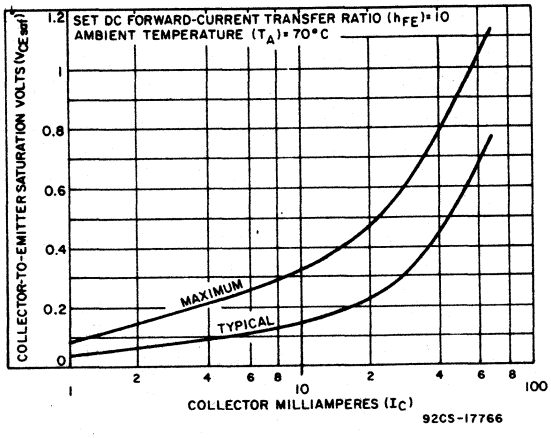


Fig.5 – V_{CEsat} vs I_C at 70°C

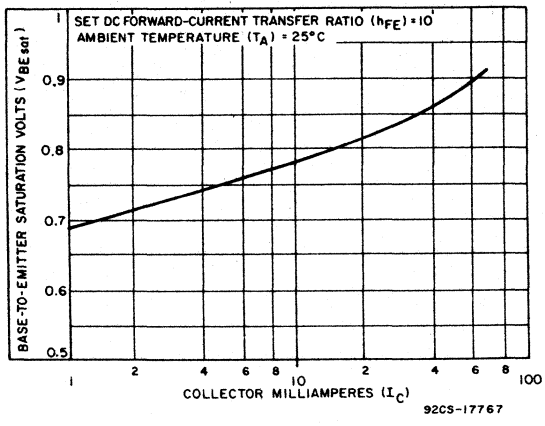


Fig.6 – V_{BEsat} vs I_C

TYPICAL STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

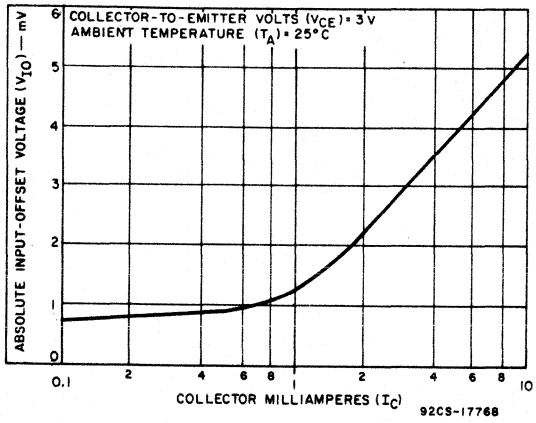


Fig.7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

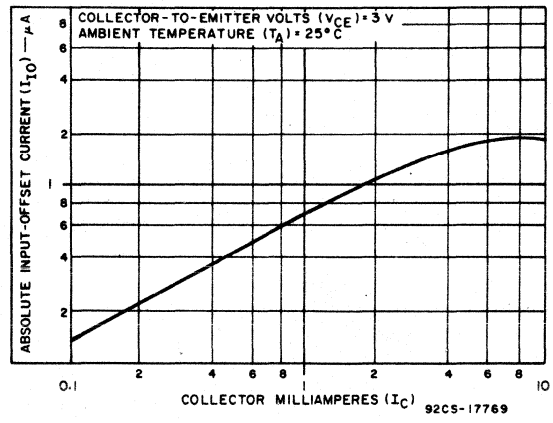
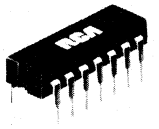


Fig.8 – I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).



H-1517

14-Lead Dual-In-Line
Plastic Package

General-Purpose P-N-P Transistor Array

FEATURES

- Matched transistor pair (Q1 and Q2)
  V_{IO} (V_{BE} matched): ± 6mV max.
  I_{IO} (at 100 μA): ± 0.6 μA
- Wide operating current range
- Low noise figure - - 3.2 dB typ. at 1 kHz

RCA-CA3084* is a general-purpose silicon p-n-p transistor array incorporating two independent transistors, a Darlington circuit, and a current-mirror pair with a shared diode.

The two independent transistors in the array may be used in a variety of circuit applications. The Darlington pair may be employed as the equivalent of a single high-beta transistor. The current-mirror pair is well suited for constant-current applications and can also be used as the active loads in a differential amplifier which uses n-p-n transistors.

The total array is especially useful for a wide range of applications in systems having low-power and low-frequency requirements. Although the transistors may be used as discrete units in conventional circuits, they offer the advantages inherent in integrated-circuit construction, that is, to provide close electrical and thermal matching.

The CA3084 utilizes the 14-lead dual-in-line plastic package.

*Formerly developmental type TA5799A.

APPLICATIONS

- General use in signal processing systems having low-power and low-frequency requirements
- Differential amplifiers
- Temperature compensated amplifiers
- Active loads for differential amplifiers using n-p-n transistors
- Complementary uses with RCA n-p-n transistor arrays

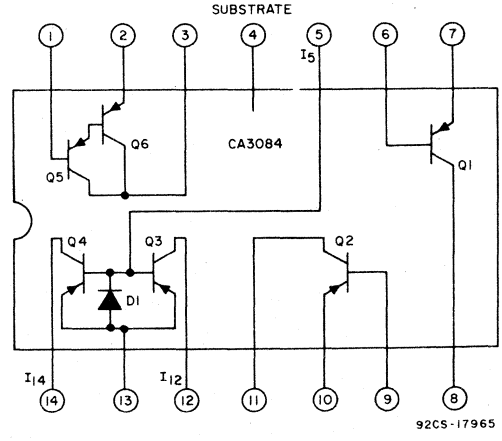


Fig. 1 -- Functional diagram of the CA3084.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Characteristics Curve Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Each Transistor:							
Collector-Cutoff Current	I_{CBO}	V_{CB} = −10V, I_E = 0	2	–	−0.055	−100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	3	–	−0.12	−100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_{CE} = −100μA, I_B = 0	–	−40	−70	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_{CB} = −100μA, I_E = 0	–	−40	−80	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_{EB} = −100μA, I_C = 0	–	−40	−100	–	V
Emitter-to-Substrate Breakdown Voltage	$V_{(BR)EIO}$	I_{EI} = 100μA	–	−40	−100	–	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_E = 1mA, I_B = 100μA	4	–	−0.125	−0.25	V
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = −10V	5	−0.50	−0.59	−0.68	V
DC Forward-Current Transfer Ratio	h_{FE}		7	15	40	–	
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Magnitude of Input Offset Voltage	$\lvert V_{IO} \rvert$	I_E = 100μA, V_{CE} = −10V	8	–	0.422	6	mV
Input Offset Current	I_{IO}		–	−0.6	0	0.6	μA
For Transistors Q3 and Q4 (Current-Mirror Configuration):							
Collector Current	I_C	V_{CE} = −10V, V_{CIO} = −10V,	10	0.85	1.00	1.15	μA
Magnitude of Collector Current Ratio	$\lvert I_C(Q3)/I_C(Q4) \rvert$	Term. 13 = Gnd. I_5 = −100μA,	11	0.90	1.00	1.10	
For Transistors Q5 and Q6 (Darlington Configuration):							
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	–	–	–	−1.0	μA
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = −10V	13	0.92	1.07	1.20	V
DC Forward-Current Transfer Ratio	h_{FE}		15	100	1230	–	

ELECTRICAL CHARACTERISTICS at T_A = 25°C
Typical Values Intended Only For Design Guidance

Magnitude of Temperature Coefficient:							
V_{BE} (for each transistor)	$\lvert \Delta V_{BE}/\Delta T \rvert$	I_E = 100μA,	6		−1.78		mV/°C
V_{IO} (as a differential amplifier)	$\lvert \Delta V_{IO}/\Delta T \rvert$	V_{CE} = −10V	9		0.54		μV/°C
V_{BE} (Darlington configuration)	$\lvert \Delta V_{BE}/\Delta T \rvert$		14		−3.7		mV/°C
For Each Transistor:							
Input Resistan e	R_I	f = 1kHz, V_{CE} = −10V,	19		9		kΩ
Output Resistance	R_O	I_C = −100μA	20	–	600	–	kΩ
Forward Transconductance	g_m		22	–	3	–	mmho
Collector-to-Base Capacitance	C_{CBO}	I_{CB} = 0	23	–	3.3	–	pF
Collector-to-Emitter Capacitance	C_{CEO}	I_{CE} = 0	23	–	2.5	–	pF
Base-to-Substrate Capacitance	C_{BIO}	I_{CIO} = 0	23	–	4.5	–	pF

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Dissipation:		
Any one transistor	200	mW
Total package	750	mW
Above T_A = 55°C	derate linearly6.67	mW/°C
Ambient Temperature Range:		
Operating	−40 to +85	°C
Storage	−55 to +150	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO})	−40	V
Collector-to-Base Voltage (V_{CBO})	−40	V
Base-to-Substrate Voltage (V_{BIO})*	−40	V
Emitter-to-Base Voltage (V_{EBO})	−40	V
Collector Current (I_C)	−10	mA

*The base of each transistor of the CA3084 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any base voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (4) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

STATIC CHARACTERISTICS FOR EACH TRANSISTOR

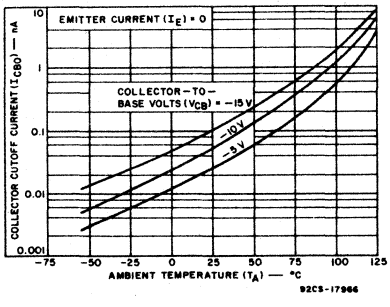


Fig.2 – I_{CBO} vs T_A.

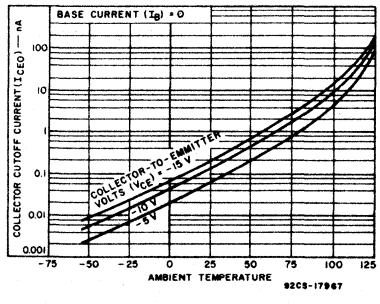


Fig.3 – I_{CEO} vs T_A.

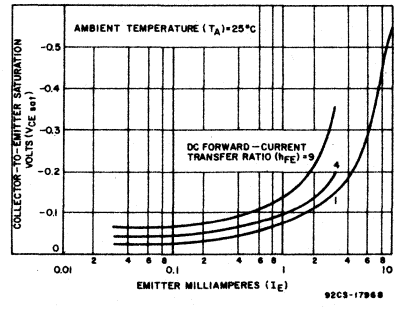


Fig.4 – V_{CEsat} vs I_E.

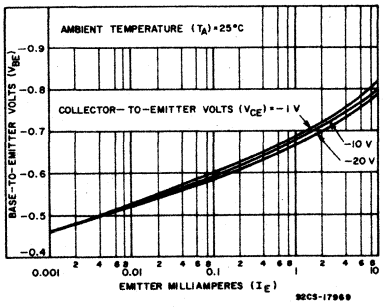


Fig.5 – V_{BE} vs I_E.

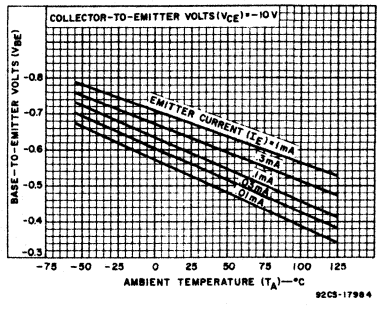


Fig.6 – V_{BE} vs T_A.

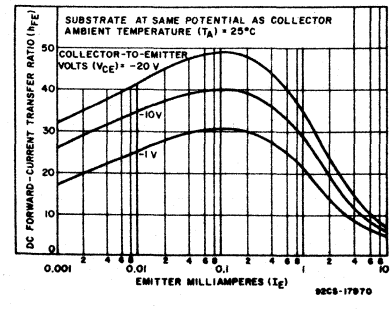


Fig.7 – h_{FE} vs I_E.

STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

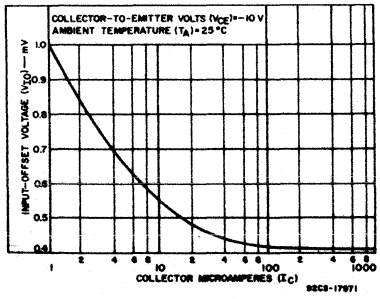


Fig.8–V_{IO} vs I_C, (transistors Q1 and Q2 as a differential amplifier).

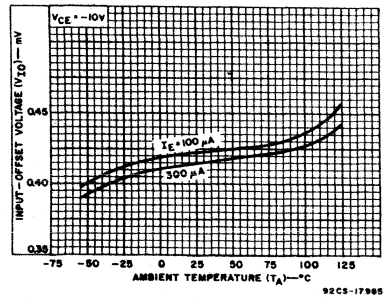


Fig.9–V_{IO} vs T_A (transistors Q1 and Q2 as a differential amplifier).

STATIC CHARACTERISTICS FOR CURRENT-MIRROR CONFIGURATION

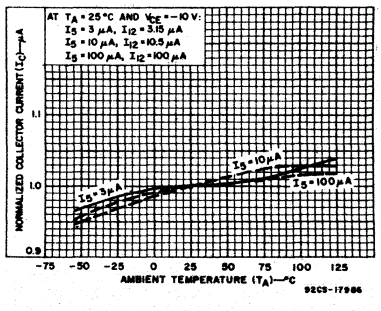


Fig.10–Normalized I_C vs T_A (transistors Q3 and Q4 in a current-mirror configuration.

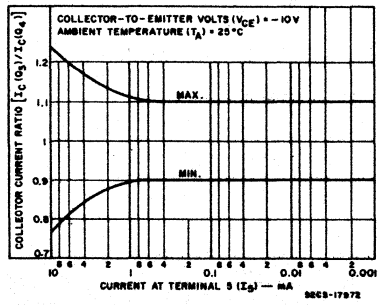


Fig.11–I_C ratio vs I_5 (transistors Q3 and Q4 in a current-mirror configuration.

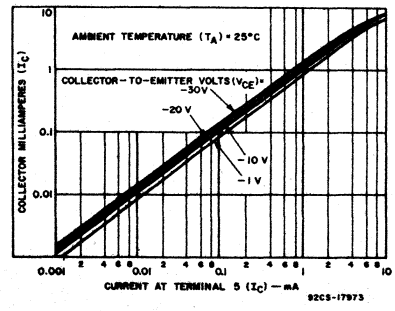


Fig.12–I_C vs I_5 (transistors Q3 and Q4 in a current-mirror configuration).

STATIC CHARACTERISTICS FOR DARLINGTON CONFIGURATION

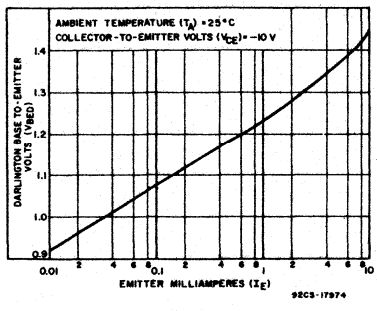


Fig.13–V_{BE} vs I_E (transistors Q5 and Q6 in a darlington configuration).

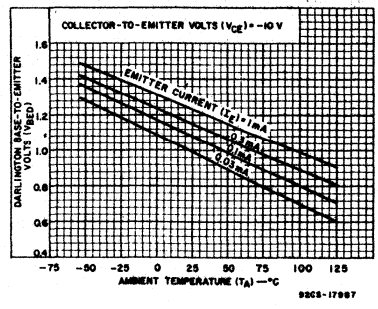


Fig.14–V_{BE} vs T_A (transistors Q5 and Q6 in a darlington configuration).

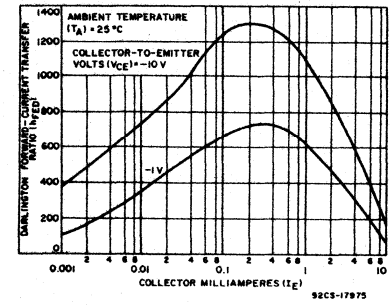


Fig.15–h_{FE} vs I_E (transistors Q5 and Q6 in a darlington configuration).

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

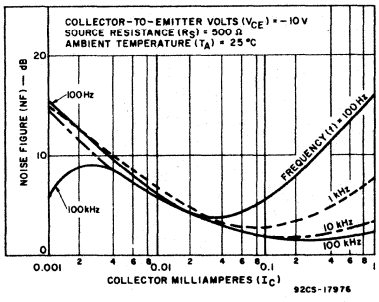


Fig.16 – NF vs I_C at R_S = 500Ω

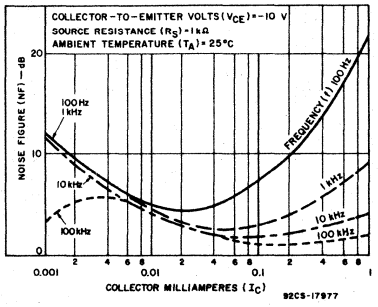


Fig.17 – NF vs I_C at R_S = 1kΩ

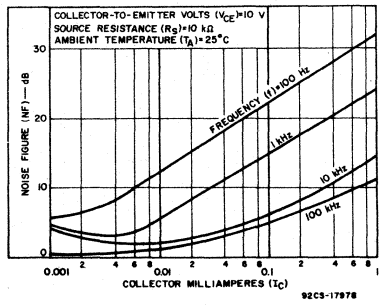


Fig.18 – NF vs I_C at R_S = 10kΩ

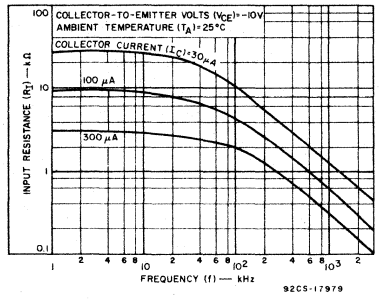


Fig.19 – R_I vs f

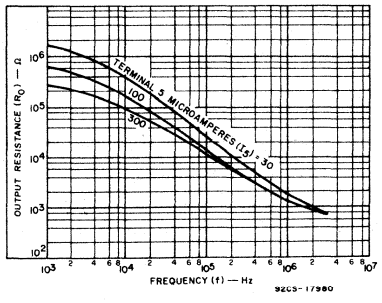


Fig.20 – R_O vs f

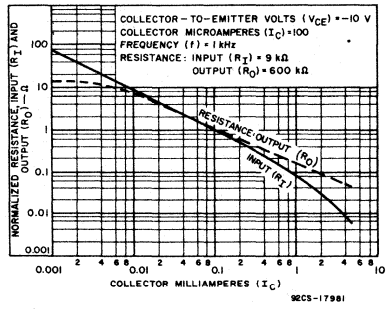


Fig.21 – Normalized R_I and R_O vs I_C

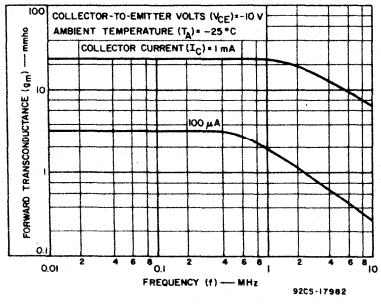


Fig.22 – g_m vs f

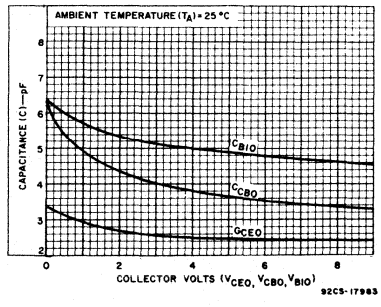
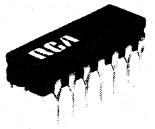


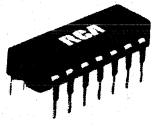
Fig.23 – Transistor capacitances vs collector voltages (V_{CEO}, V_{CBO}, V_{CIO})

14-Lead Dual-In-Line
Frit-Seal (Hermetic) Package



H-1806

14-Lead Dual-In-Line
Plastic Package



H-1517

General-Purpose N-P-N Transistor Array

Three Isolated Transistors and One Differentially–Connected Transistor Pair

For Low–Power Applications from DC to 120MHz

Applications

- **General-purpose use in signal processing systems operating in the DC to 120-MHz range**
- **Temperature compensated amplifiers**
- **See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.**

RCA-CA3086 consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120 MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching.

The CA3086 is supplied in a 14-lead dual-in line plastic package. The CA3086F is supplied in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

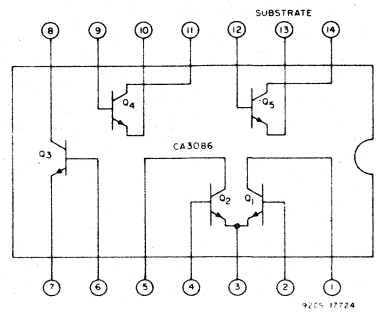


Fig. 1 – Functional diagram of the CA3086.

MAXIMUM RATINGS, Absolute–Maximum Values at T_A = 25°C

Dissipation:		
Any one transistor	300	mW
Total package up to T_A = 55°C	750	mW
Above T_A = 55°C	derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	–55 to + 125	°C
Storage	–65 to + 150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) From case for 10 seconds max.	+ 265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

CA3086

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	Typ. Characteristic Curves Fig. No.	LIMITS			UNITS
				Min.	Typ.	Max.	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	2	–	0.002	100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	3	—	See Curve	5	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 1mA	4	40	100	–	

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

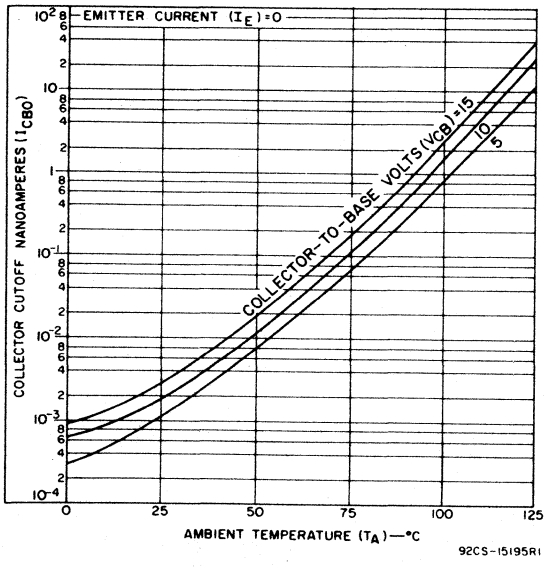


Fig.2– I_{CBO} vs T_A.

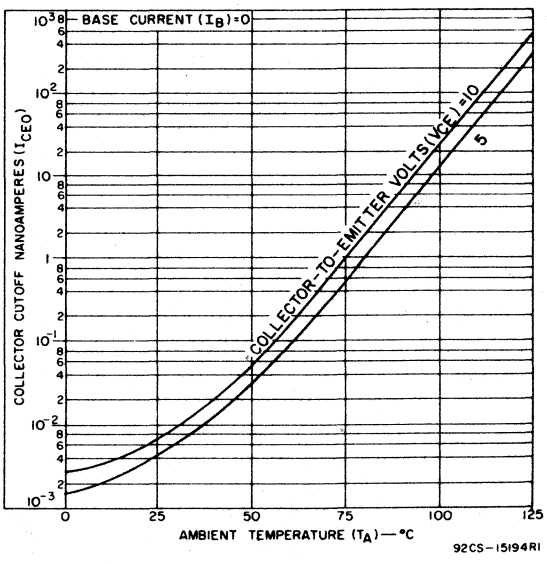


Fig.3– I_{CEO} vs T_A.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		Typ. Characteristics Curves Fig. No.	TYPICAL VALUES	UNITS
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3 V	I_C = 10 mA	4	100	
			I_C = 10 μA	4	54	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V	I_E = 1 mA	5	0.715	V
			I_E = 10 mA	5	0.800	V
V_{BE} Temperature Coefficient	$\Delta V_{BE}/\Delta T$	V_{CE} = 3V, I_C = 1mA		6	−1.9	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_B = 1mA, I_C = 10mA		—	0.23	V
Noise Figure (low frequency)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100μA, R_S = 1k Ω		—	3.25	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		7	100	—
Short-Circuit Input Impedance	h_{ie}			7	3.5	kΩ
Open-Circuit Output Impedance	h_{oe}			7	15.6	μmho
Open-Circuit Reverse-Voltage Transfer Ratio	h_{re}			7	1.8×10^{-4}	—
Admittance Characteristics:						
Forward Transfer Admittance	y_{fe}	f = 1MHz, V_{CE} = 3V, I_C = 1mA		8	31 − j1.5	mmho
Input Admittance	y_{ie}			9	0.3 + j0.04	mmho
Output Admittance	y_{oe}			10	0.001 + j0.03	mmho
Reverse Transfer Admittance	y_{re}			11	See Curve	—
Gain-Bandwidth Product	f_T	V_{CE} = 3V, I_C = 3mA		12	550	MHz
Emitter-to-Base Capacitance	C_{EBO}	V_{EB} = 3V, I_E = 0		—	0.6	pF
Collector-to-Base Capacitance	C_{CBO}	V_{CB} = 3V, I_C = 0		—	0.58	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 3V, I_C = 0		—	2.8	pF

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

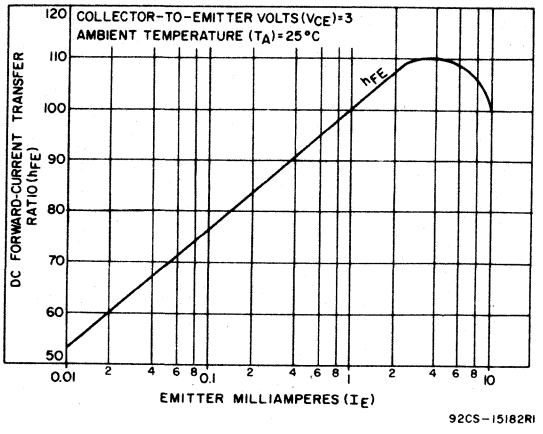


Fig.4 – h_{FE} vs I_E.

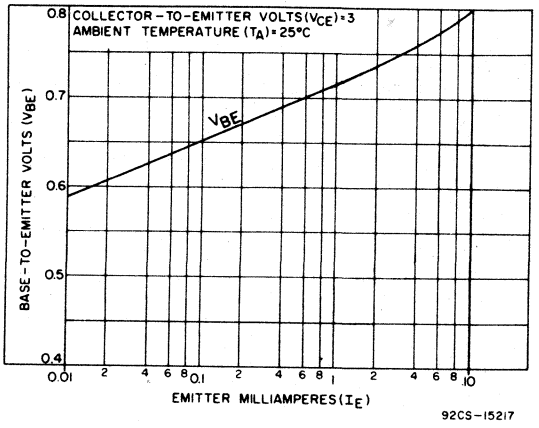


Fig.5 – V_{BE} vs I_E.

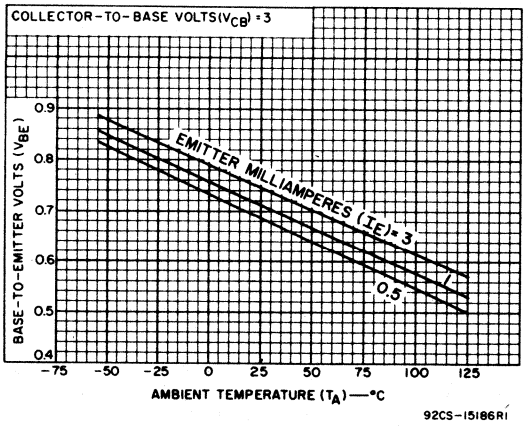


Fig.6 – V_{BE} vs T_A.

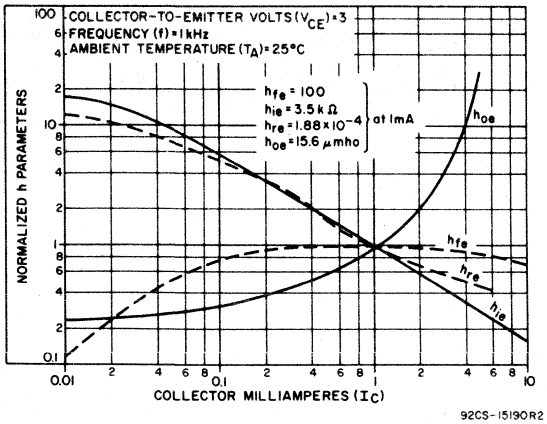


Fig.7 – Normalized h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C.

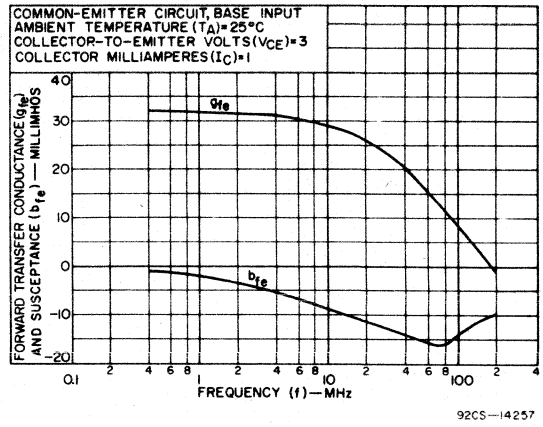


Fig.8 – y_{fe} vs f.

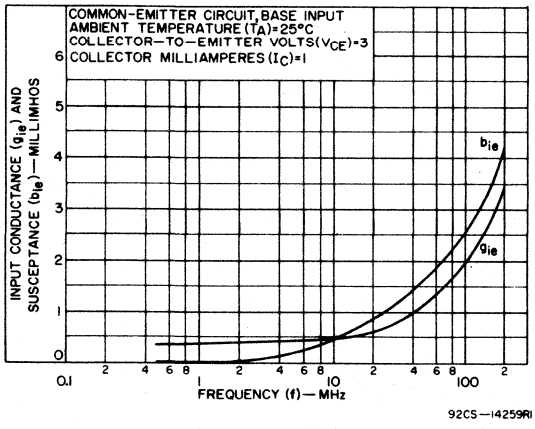


Fig.9 – y_{ie} vs f.

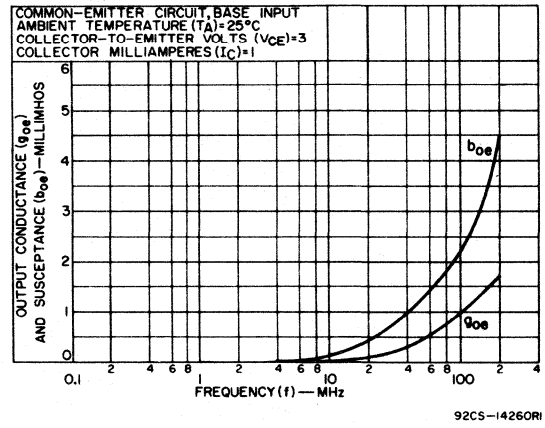


Fig.10 – y_{oe} vs f.

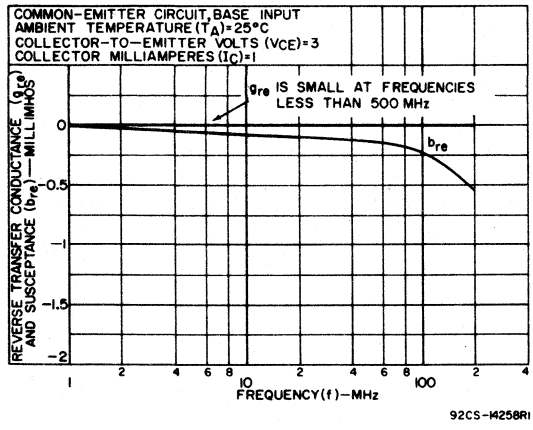


Fig.11 – y_{re} vs f.

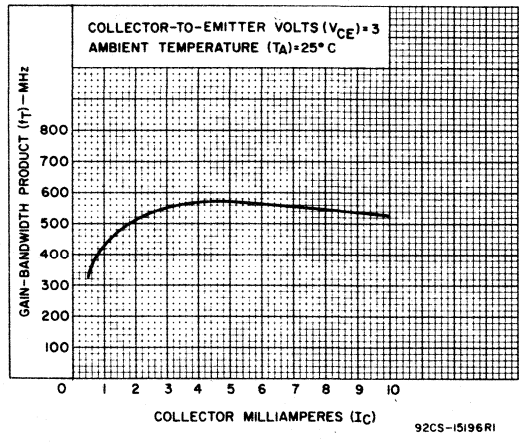
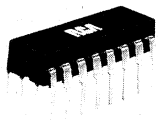


Fig.12 – f_T vs I_C.

CA3093E



16-Lead Dual-In-Line
Plastic Package H1622

General-Purpose High-Current N-P-N Transistor-Zener Diode-Diode Array

Applications

- Signal processing and switching systems operating from DC to VHF
- Lamp and relay driver
- Differential amplifier
- Temperature-compensated amplifier
- Thyristor firing
- Temperature-compensated shunt regulator
- Temperature-compensated series regulator
- Level shifting
- Voltage-level clamping

RCA CA3093E* is a versatile array of three high-current (to 100mA) NPN transistors, two 10%-tolerance Zener diodes and one conventional diode, all on a common monolithic substrate. Two of the transistors (Q_1 and Q_2) are matched at 1 mA for applications in which offset parameters are of special importance. The combination of positive Zener voltage temperature coefficients and negative forward base-emitter voltage temperature coefficients provides a unique temperature compensation capability.

Independent connections for each transistor and diode plus a separate terminal for the substrate permit maximum flexibility in circuit design.

*Formerly developmental type TA6119

#Z_1, Z_2 and D1 are transistors internally connected as shown below.

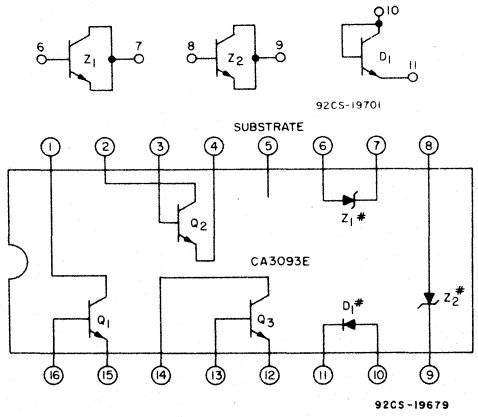


Fig. 1 — Functional diagram of the CA3093E (bottom view)

- Current regulator
- Voltage clamping
- Simple off-line regulated supply
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Circuit Transistor Array" for applications in addition to those given on pages 5 & 6 of this bulletin.

Features:

- **6 independent devices plus separate substrate connection**
- **Compensating temperature coefficients — V_{BE} and V_{D1} VS. V_Z**

Transistors

- **High I_C (100mA max)**
- **Matched pair (Q1 & Q_2)**
  V_{IO} = ± 5mV max, I_{IO} = 2.5 μA max } at I_C = 1mA
  $\Delta V_{IO}/\Delta T$ = 5 μV/°C typ
- **h_{FE} = 40 min @ I_C = 10mA or 50mA**
- **Low V_{CEsat} . . . 0.7V max @ 50mA**

Zener Diodes

- **Two 1/4W Zeners**
- **V_Z = 7V ± 10%**
- **z_Z = 15Ω typ**

Diode

- **Close forward voltage match to V_{BE}'s of Q_1 and Q_2**
- **V_{PIV} = 5.5V min.**

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

Power Dissipation:

Any one transistor	500	mW
Any one Zener Diode	250	mW
Total package	750	mW
Above 25°C ..... Derate linearly	6.67	mW/°C
Ambient Temperature Range:		
Operating	-40 to +85	°C
Storage	-55 to +150	°C

The following maximum ratings apply for each transistor

Collector-to-Emitter Voltage (V_{CEO})	15	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})*	20	V
Emitter-to-Base Voltage (V_{EBO})	5.5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	35	mA

The following maximum ratings apply for each Zener Diode or Diode

Zener Diode dc Current (I_Z)	35	mA
Zener Diode-to-Substrate Voltage (V_{ZIO})*	20	V
Diode (D1) Forward Current (I_{DF})	50	mA
Diode (D1) Reverse Voltage (V_{DR})	5.5	V
Diode (D1)-to-Substrate Voltage (V_{DIO})*	20	V

*The collector of each transistor, the cathode of each Zener diode, and the anode of the diode are isolated from the substrate by an internal diode. The substrate must be connected to a voltage which is more negative than any of these isolated terminals in order to maintain isolation between devices and provide normal transistor action. To avoid undesired coupling between devices, the substrate terminal (5) should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

CA3093E

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Each Transistor:							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	–	5.5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	–	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	–	1	μA
DC Forward Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 10mA	2	40	76	–	
		V_{CE} = 3V, I_C = 50mA	2	40	75	–	
Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 50mA, I_B = 5mA	4	–	0.40	0.70	V
Forward Base-to-Emitter Temp. Coefficient	$\Delta V_{BE}/\Delta T$	I_E = 10mA		–	-1.9	–	mV/°C
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	7	–	1.2	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	8	–	0.7	2.5	μA
Temp. Coefficient of Offset Voltage	$\lvert\Delta V_{IO}/\Delta T\rvert$	–	–	–	5	–	μV/°C
For Each Zener Diode							
Zener Voltage	V_Z	I_Z = 10mA	9	6.3	7	7.7	V
Zener Impedance	z_Z	I_Z = 10mA, f = 1 kHz	10	–	15	25	Ω
Zener Reverse Current	I_{ZR}	V_Z = +5V	–	–	–	1	μA
Zener Voltage Temp. Coefficient	$\Delta V_Z/\Delta T$	I_Z = 10mA	9	– i.e.	+3.6 +.05	–	mV/°C %/°C
Zener-to-Substrate Breakdown Voltage	$V_{(BR)ZIO}$	I_Z = 100μA (Terminals 7 & 9)	–	20	60	–	V
Dissipation		Refer to Example in Application "a"		–	–	250	mW
For Diode (D1)							
Diode Forward Voltage	V_{DF}	I_C = 10mA, V_{CE} = 3V	3	0.65	0.74	0.85	V
Diode Forward Current	I_{DF}		–	–	–	50	mA
Diode Reverse-Breakdown Voltage	$V_{(BR)DR}$	I_{DR} = 500μA	–	5.5	6.9	–	V
Diode-to-Substrate Breakdown Voltage	$V_{(BR)DIO}$	I_{Diode} = 100μA (Terminal 10)	–	20	60	–	V
Diode Forward-Voltage Temp. Coefficient	$\Delta V_{DF}/\Delta T$	I_{DF} = 5mA	3	–	-1.9	–	mV/°C

TYPICAL STATIC CHARACTERISTICS

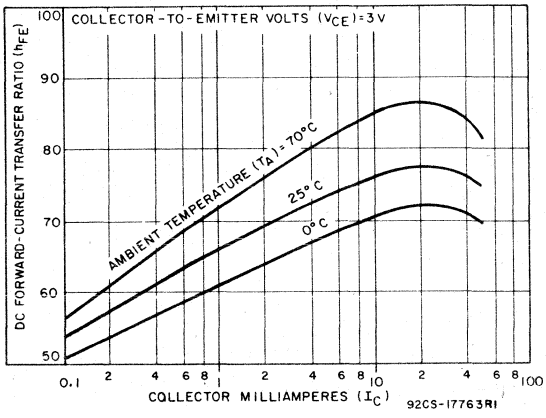


Fig. 2 – h_{FE} vs I_C

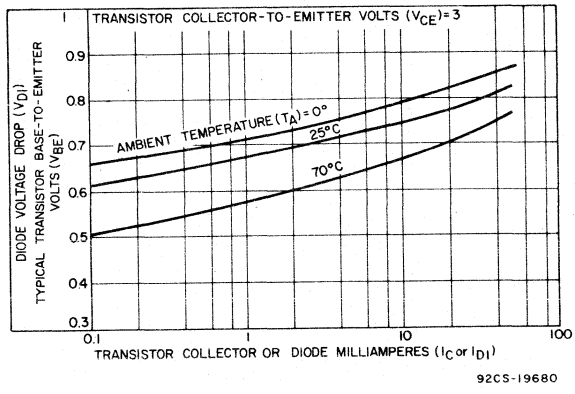


Fig. 3 – V_{BE} vs I_C and V_{D1} vs I_{D1}

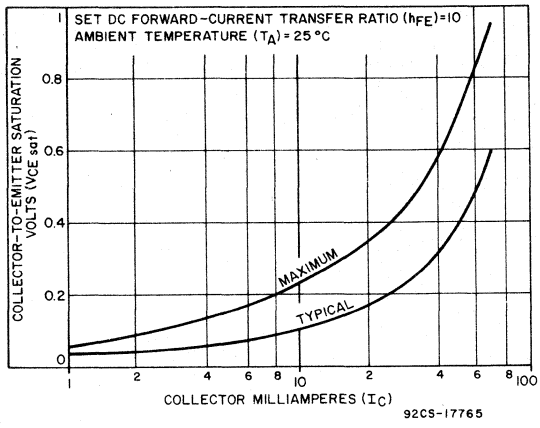


Fig. 4 – V_{CEsat} vs I_C at 25°C

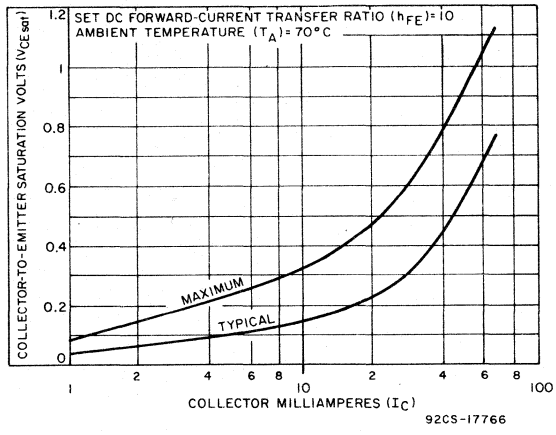


Fig. 5 – V_{CEsat} vs I_C at 70°C

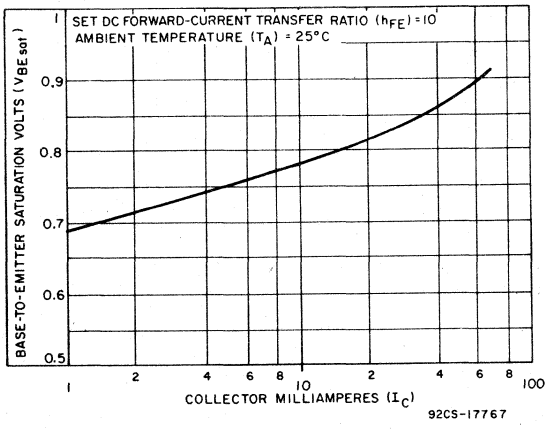


Fig. 6 – V_{BEsat} vs I_C

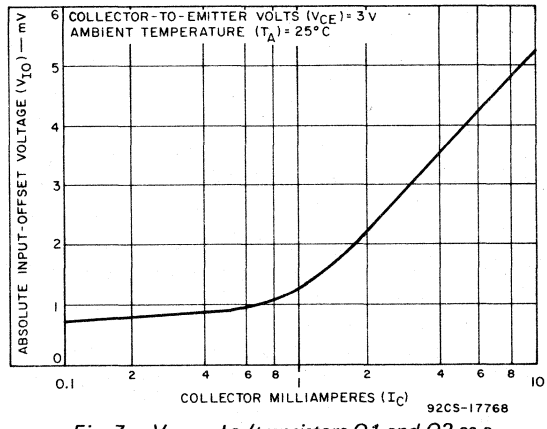


Fig. 7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier)

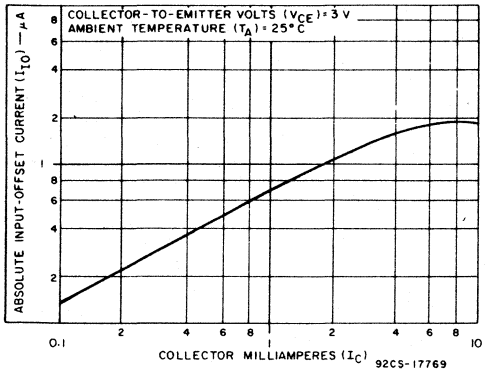


Fig. 8 – I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier)

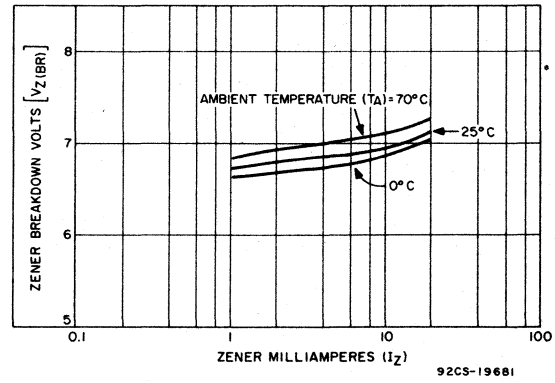


Fig. 9 – Typical Zener breakdown voltage vs current

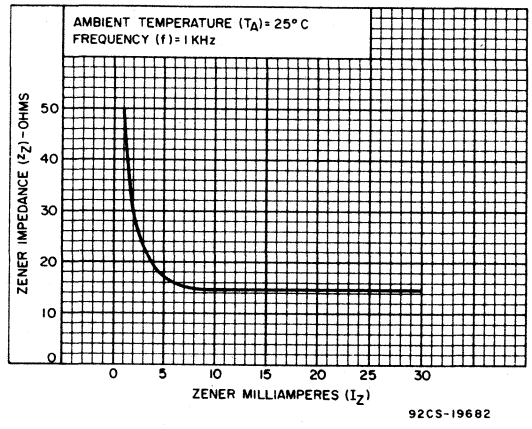
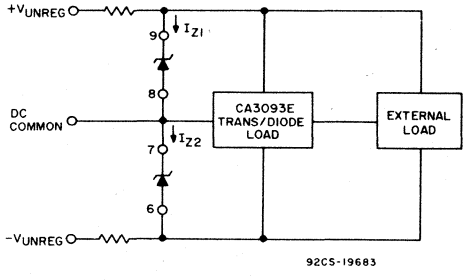


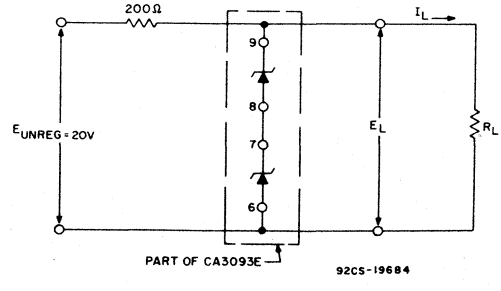
Fig. 10 – Typical Zener impedance vs current

TYPICAL APPLICATIONS

a) ±7V Regulator supplying CA3093E Transistors plus an external load.



b) 14V Regulator for Q1, Q2, Q3



Sample Computation for Determining Permissible Zener Dissipation at +25°C.

CA3093E Ratings at T_A = +25°C
Total Diss. Max = 750 mW (Derate @ 6.67 mW/°C above 25°C)
Each Zener Diss. Max = 250 mW
Max. Zener Current = 35 mA

Assume CA3093E Transistor/Diode Load Dissipation = 350 mW then max. total Zener Diss. ($P_{Z1} + P_{Z2}$) = 750 - 350 = 400 mW

$$(I_{Z1} + I_{Z2})\ max = \frac{400\ mW}{7V} = 57\ mA$$

(Note: Max. current rating on each Zener is 35 mA)

Typical Load Regulation for I_L = 0 to 25 mA

$\Delta E_L/E_L \times 100 \approx -6\%$
(no load to full load)

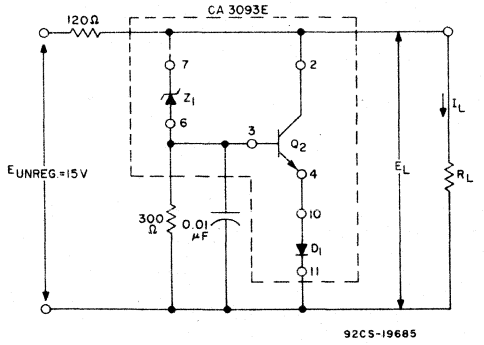
Typical Line Regulation

$$\frac{(\Delta E_L/E_L) \times 100}{\Delta E\ unreg.} \approx \pm 0.9\%/V$$

Typical Temperature Characteristic

$$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = +0.05\%/°C$$

c) 8.6V Temp.-Compensated Shunt Regulator



Typical Temperature Characteristic @ R_L = 330Ω

$$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = \pm\ 0.007\%/°C$$

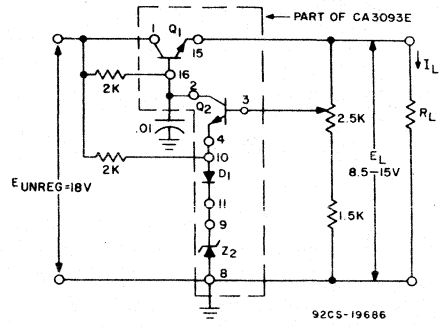
Typical Load Regulation I_L = 0 to 40 mA

$(\Delta E_L/E_L) \times 100 = -3\%$ (no load to full load)

Typical Line Regulation at R_L = 330Ω

$$\frac{\Delta E_L/E_L}{\Delta E \text{ unreg.}} \times 100 = \pm\ 0.55\%/V$$

d) Temp.-Compensated Series Voltage Regulator



Typical Temperature Characteristic @ E_L = 12V

$$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = \pm\ 0.009\%/°C$$

Typical Load Regulation @ E_L = 12V

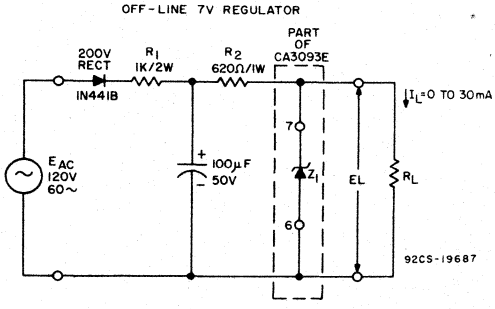
I_L = 0 to 40 mA

$$\frac{\Delta E_L}{E_L} \times 100 = \pm\ 0.4\% \text{ (no load to full load)}$$

Typical Line Regulation @ E_L = 12V

$$\frac{(\Delta E_L/E_L) \times 100}{\Delta E \text{ unreg.}} = \pm\ 0.45\%/V$$

e) Off-Line 7V Regulator



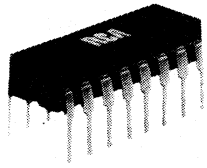
Typical E_L Ripple Voltage = 70 mV_{p-p}

Typical Load Regulation = $\frac{\Delta E_L}{E_L} \times 100 = -8.5\%$ (no load to full load)

I_L = 0 to 30 mA

Typical Line Regulation = $\frac{(\Delta E_L/E_L) \times 100}{\Delta E_{AC}} = \pm\ .075\%/V$

CA3096, CA3096A, CA3096C



(E SUFFIX)
16-Lead Dual-In-Line
Plastic Package

H-1622

N-P-N/P-N-P Transistor Array

Five-Independent Transistors: Three n-p-n and Two p-n-p

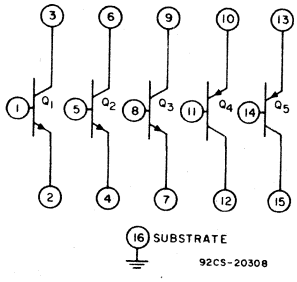
Applications:

- *Differential Amplifiers*
- *DC Amplifiers*
- *Sense Amplifiers*
- *Level Shifters*
- *Timers*
- *Lamp and Relay Drivers*
- *Thyristor Firing Circuits*
- *Temperature-Compensated Amplifiers*
- *Operational Amplifiers*

RCA-CA3096CE, CA3096E, and CA3096AE are general-purpose high-voltage silicon transistor arrays. Each array consists of five independent transistors (two p-n-p and three n-p-n types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096AE, CA3096E, and CA3096CE are identical, except that the CA3096AE specifications include parameter matching and greater stringency in I_{CBO}, I_{CEO}, and $V_{CE}(SAT)$. The CA3096CE is a relaxed version of the CA3096E.

The CA3096CE, CA3096E, and CA3096AE are supplied in 16-lead dual-in-line plastic packages. (E-suffix). The CA3096 is also available in chip form. (H suffix).



Schematic Diagram

CA3096AE, CA3096E, CA3096CE
ESSENTIAL DIFFERENCES

CHARACTERISTIC		CA3096AE	CA3096E	CA3096CE
$V_{(BR)CEO}$ (V) Min.	n-p-n	35	35	24
	p-n-p	−40	−40	−24
$V_{(BR)CBO}$ (V) Min.	n-p-n	45	45	30
	p-n-p	−40	−40	−24
h_{FE} @ 1 mA	n-p-n	150-500	150-500	100-670
	p-n-p	20-150	20-150	15-200
h_{FE} @ 100 μA	p-n-p	40-200	40-200	30-300
I_{CBO} (nA) Max.	n-p-n	40	100	100
	p-n-p	−40	−100	−100
I_{CEO} (nA) Max.	n-p-n	100	1000	1000
	p-n-p	−100	−1000	−1000
$V_{CE}(SAT)$ (V) Max.	p-n-p	0.5	0.7	0.7
$\lvert V_{IO}\rvert$ (mV) Max.	n-p-n	5	–	–
	p-n-p	5	–	–
$\lvert I_{IO}\rvert$ (μA) Max.	n-p-n	0.6	–	–
	p-n-p	0.25	–	–

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	EACH N-P-N	EACH P-N-P	
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}:			
CA3096AE, CA3096E	35	−40	V
CA3096CE	24	−24	V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}:			
CA3096AE, CA3096E	45	−40	V
CA3096CE	30	−24	V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}:			
CA3096AE, CA3096E	45	−	V
CA3096CE	30	−	V
EMITTER-TO-SUBSTRATE VOLTAGE, V_{EIO}:			
CA3096AE, CA3096E	−	−40	V
CA3096CE	−	−24	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}:			
CA3096E, CA3096E	6	−40	V
CA3096CE	6	−24	V
COLLECTOR CURRENT, I_C (All Types)	50	−10	mA
POWER DISSIPATION, P_D:			
Up to $T_A = 55°C$:			
Device (Total)	750		mW
Each Transistor	200		mW
Above $T_A = 55°C$ derate linearly at	6.67		mW/°C
AMBIENT-TEMPERATURE RANGE, T_A:			
Operating	−55 to +125°C		
Storage	−65 to +150°C		
LEAD TEMPERATURE (DURING SOLDERING):			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	265°C		

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096AE			CA3096E			CA3096CE			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each n-p-n Transistor											
I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	−	0.001	40	−	0.001	100	−	0.001	100	nA
I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	−	0.006	100	−	0.006	1000	−	0.006	1000	nA
$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	35	50	−	35	50	−	24	35	−	V
$V_{(BR)CBO}$	$I_C = 10\,\mu$A, $I_E = 0$	45	100	−	45	100	−	30	80	−	V
$V_{(BR)CIO}$	$I_{CI} = 10\,\mu$A, $I_B = I_E = 0$	45	100	−	45	100	−	30	80	−	V
$V_{(BR)EBO}$	$I_E = 10\,\mu$A, $I_C = 0$	6	8	−	6	8	−	6	8	−	V
V_Z	$I_Z = 10\,\mu$A	6	7.9	9.8	6	7.9	9.8	6	7.9	9.8	V
$V_{CE(SAT)}$	$I_C = 10$ mA, $I_B = 1$ mA	−	0.24	0.5	−	0.24	0.7	−	0.24	0.7	V
V_{BE}	$I_C = 1$ mA, $V_{CE} = 5$ V	0.6	0.69	0.78	0.6	0.69	0.78	0.6	0.69	0.78	V
h_{FE}		150	390	500	150	390	500	100	390	670	
$\lvert\Delta V_{BE}/\Delta T\rvert$	$I_C = 1$ mA, $V_{CE} = 5$ V	−	1.9	−	−	1.9	−	−	1.9	−	mV/°C

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ (Cont'd)
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096AE			CA3096E			CA3096CE			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each p-n-p Transistor											
I_{CBO}	$V_{CB} = -10$ V, $I_E = 0$	–	−0.006	−40	–	−0.06	−100	–	−0.06	−100	nA
I_{CEO}	$V_{CE} = -10$V, $I_B = 0$	–	−0.12	−100	–	−0.12	−1000	–	−0.12	−1000	nA
$V_{(BR)CEO}$	$I_C = -100\,\mu$A, $I_B = 0$	−40	−75	–	−40	−75	–	−24	−30	–	V
$V_{(BR)CBO}$	$I_C = -10\,\mu$A, $I_E = 0$	−40	−80	–	−40	−80	–	−24	−60	–	V
$V_{(BR)EBO}$	$I_E = -10\,\mu$A, $I_C = 0$	−40	−100	–	−40	−100	–	−24	−80	–	V
$V_{(BR)EIO}$	$I_{EI} = 10\,\mu$A, $I_B = I_C = 0$	−40	−100	–	−40	−100	–	−24	−80	–	V
$V_{CE(SAT)}$	$I_C = -1$ mA, $I_B = -100\,\mu$A	–	−0.16	−0.4	–	−0.16	−0.4	–	−0.16	−0.4	V
V_{BE}	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	−0.5	−0.6	−0.7	−0.5	−0.6	−0.7	−0.5	−0.6	−0.7	V
h_{FE}	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	40	85	250	40	85	250	30	85	300	
	$I_C = -1$ mA, $V_{CE} = -5$ V	20	47	200	20	47	200	15	47	200	
$\lvert\Delta V_{BE}/\Delta T\rvert$	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	–	2.2	–	–	2.2	–	–	2.2	–	mV/°C

I_{CBO} Collector-Cutoff Current

I_{CEO} Collector-Cutoff Current

$V_{(BR)CEO}$ Collector-to-Emitter Breakdown Voltage

$V_{(BR)CBO}$ Collector-to-Base Breakdown Voltage

$V_{(BR)CIO}$ Collector-to-Substrate Breakdown Voltage

$V_{(BR)EBO}$ Emitter-to-Base Breakdown Voltage

V_Z Emitter-to-Base Zener Voltage

$V_{CE(SAT)}$ Collector-to-Emitter Saturation Voltage

V_{BE} Base-to-Emitter Voltage

h_{FE} DC Forward-Current Transfer Ratio

$\lvert\Delta V_{BE}/\Delta T\rvert$ Magnitude of Temperature Coefficient: (for each transistor)

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ (CA3096AE Only)
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS	LIMITS CA3096AE			UNITS
			Min.	Typ.	Max.	
For Transistors Q1 and Q2 (as a Differential Amplifier)						
Absolute Input Offset Voltage,	$\lvert V_{IO}\rvert$	$V_{CE} = 5\,V$, $I_C = 1\,mA$	–	0.3	5	mV
Absolute Input Offset Current,	$\lvert I_{IO}\rvert$		–	0.07	0.6	μA
Absolute Input Offset Voltage Temperature Coefficient,	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		–	1.1	–	μV/°C
For Transistors Q4 and Q5 (As a Differential Amplifier)						
Absolute Input Offset Voltage,	$\lvert V_{IO}\rvert$	$V_{CE} = -5\,V$, $I_C = -100\,\mu A$, $R_S = 0$	–	0.15	5	mV
Absolute Input Offset Current,	$\lvert I_{IO}\rvert$		–	2	250	nA
Absolute Input Offset Voltage Temperature Coefficient,	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		–	0.54	–	μV/°C

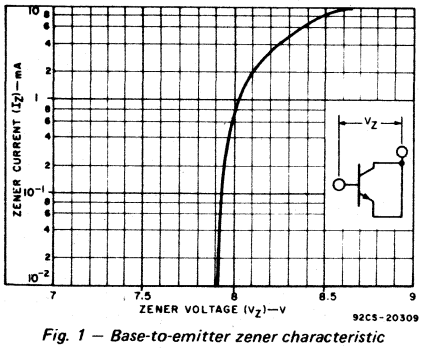


Fig. 1 – Base-to-emitter zener characteristic (n-p-n).

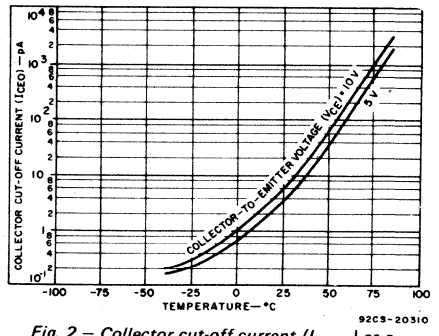


Fig. 2 – Collector cut-off current (I_{CEO}) as a function of temperature (n-p-n).

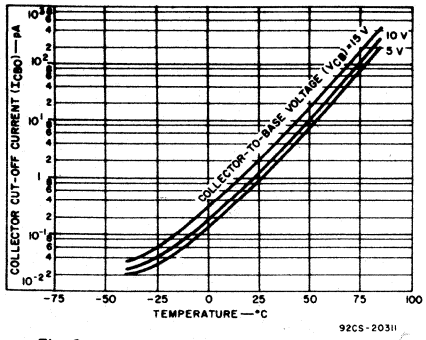


Fig. 3 – Collector cut-off current (I_{CBO}) as a function of temperature (n-p-n).

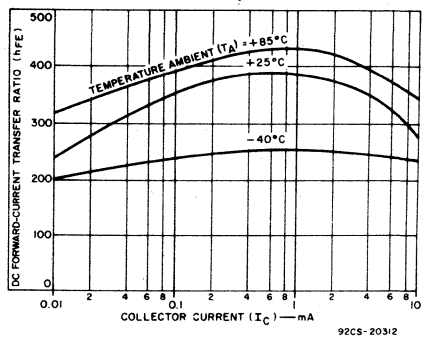


Fig. 4 – Transistor (n-p-n) h_{FE} as a function of collector current.

CA3096, CA3096A, CA3096C

DYNAMIC

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Typical Values Intended Only for Design Guidance

CHARACTERISTICS	TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each n-p-n Transistor			
Noise Figure (low frequency), NF	f = 1 kHz, V_{CE} = 5 V, I_C = 1 mA, R_S = 1 kΩ	2.2	dB
Low-Frequency, Input Resistance, R_i	f = 1.0 kHz, V_{CE} = 5 V, I_C = 1 mA	10	kΩ
Low-Frequency Output Resistance, R_o		80	kΩ
Admittance Characteristics:	f = 1 MHz, V_{CE} = 5 V, I_C = 1 mA		
Forward Transfer Admittance, $\frac{g_{fe}}{y_{fe}\ b_{fe}}$		7.5 −j13	mmho
Input Admittance, $\frac{g_{ie}}{y_{ie}\ b_{ie}}$		2.2 j3.1	mmho
Output Admittance, $\frac{g_{oe}}{y_{oe}\ b_{oe}}$		0.76 j2.4	mmho
Gain-Bandwidth Product, f_T	V_{CE} = 5 V, I_C = 1.0 mA	280	MHz
	V_{CE} = 5 V, I_C = 5 mA	335	
Emitter-to-Base Capacitance, C_{EB}	V_{EB} = 3 V	0.75	pF
Collector-to-Base Capacitance, C_{CB}	V_{CB} = 3 V	0.46	pF
Collector-to-Substrate Capacitance, C_{CI}	V_{CI} = 3 V	3.2	pF
For Each p-n-p Transistor			
Noise Figure (low frequency), NF	f = 1 kHz, I_C = 100 μA, R_S = 1 kΩ	3	dB
Low-Frequency Input Resistance, R_i	f = 1 kHz, V_{CE} = 5 V,	27	kΩ
Low-Frequency Output Resistance, R_o	I_C = 100 μA	680	kΩ
Gain-Bandwidth Product, f_T	V_{CE} = 5 V, I_C = 100 μA	6.8	MHz
Emitter-to-Base Capacitance, C_{EB}	V_{EB} = −3 V	0.85	pF
Collector-to-Base Capacitance, C_{CB}	V_{CB} = −3 V	2.25	pF
Base-to-Substrate Capacitance, C_{BI}	V_{BI} = 3 V	3.05	pF

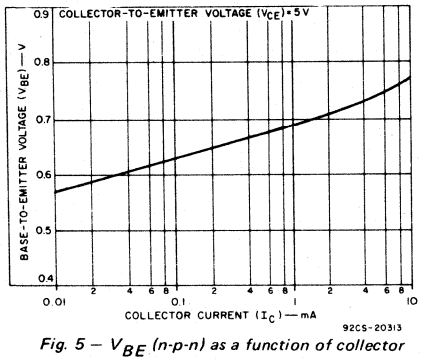


Fig. 5 – V_{BE} (n-p-n) as a function of collector current.

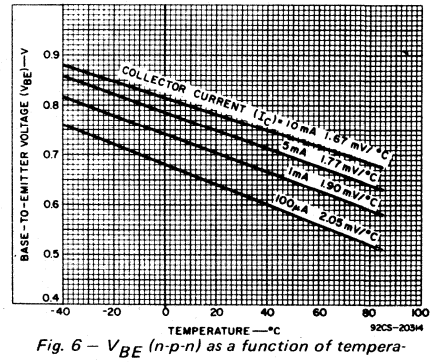


Fig. 6 – V_{BE} (n-p-n) as a function of temperature.

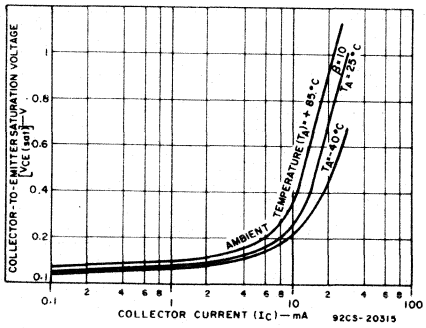


Fig. 7 – $V_{CE}(SAT)$ (n-p-n) as a function of collector current.

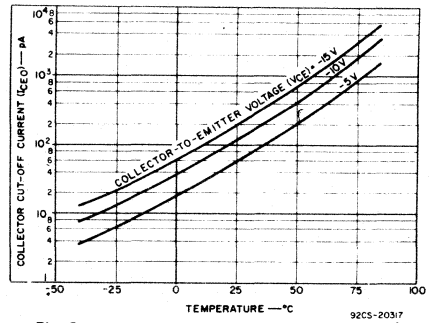


Fig. 8 – Collector cut-off current (I_{CEO}) as a function of temperature (p-n-p).

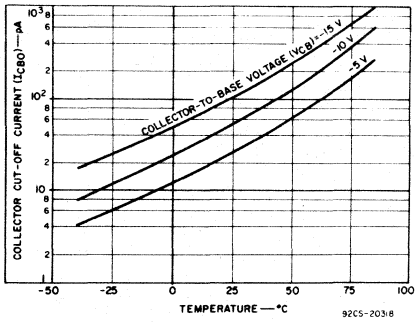


Fig. 9 – Collector cut-off current (I_{CBO}) as a function of temperature (p-n-p).

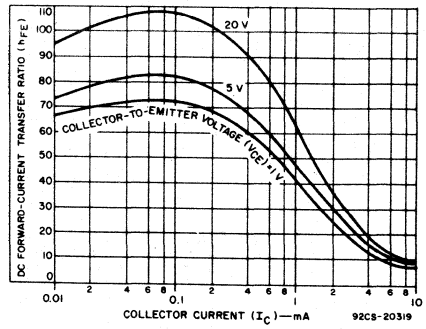


Fig. 10 – Transistor (p-n-p) h_{FE} as a function of collector current.

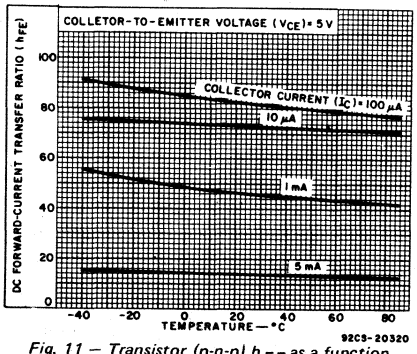


Fig. 11 – Transistor (p-n-p) h_{FE} as a function of temperature.

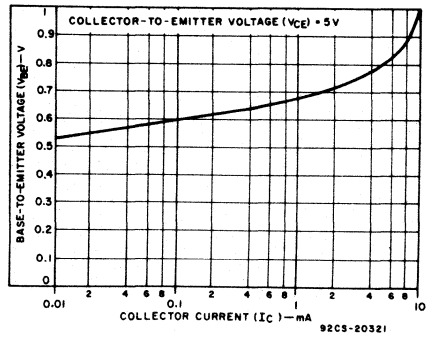


Fig. 12 – V_{BE} (p-n-p) as a function of collector current.

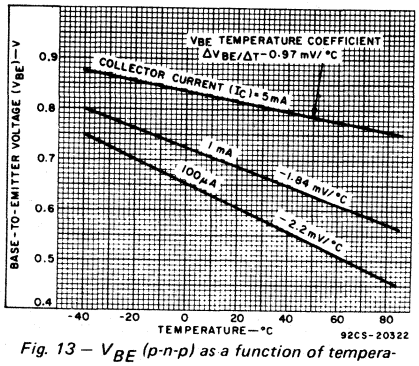


Fig. 13 – V_{BE} (p-n-p) as a function of temperature.

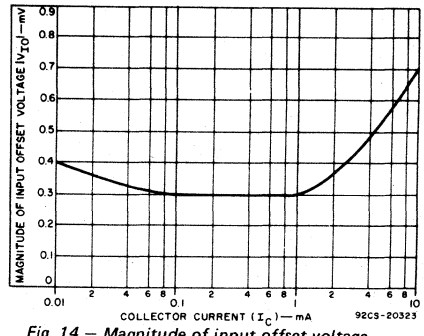


Fig. 14 – Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for n-p-n transistor Q_1–Q_2.

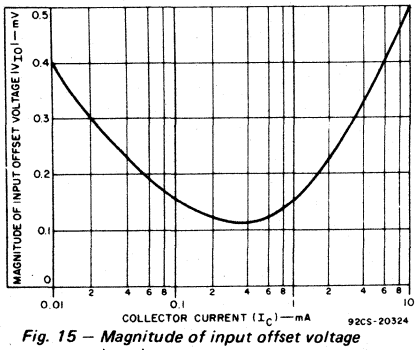


Fig. 15 – Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for p-n-p transistor Q_4–Q_5

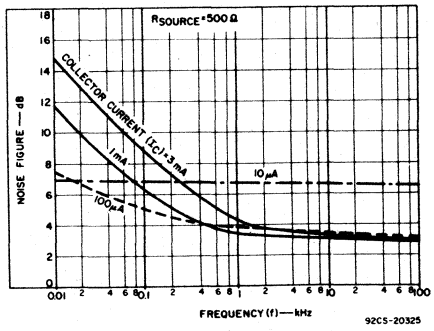


Fig. 16 – Noise figure as a function of frequency for n-p-n transistors.

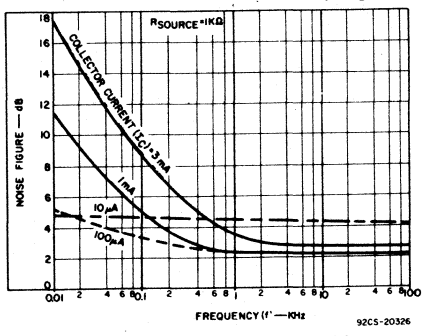


Fig. 17 – Noise figure as a function of frequency for n-p-n transistors.

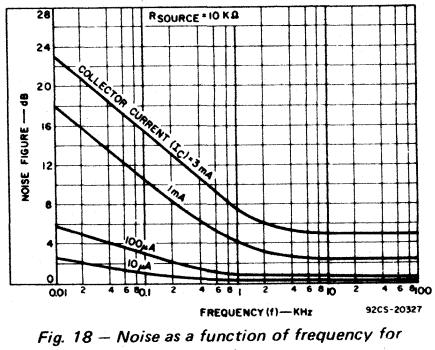


Fig. 18 – Noise as a function of frequency for n-p-n transistors.

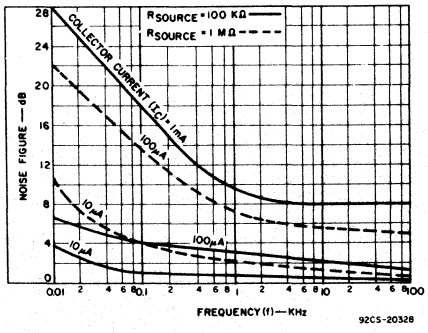


Fig. 19 – Noise figure as a function of frequency for n-p-n transistors.

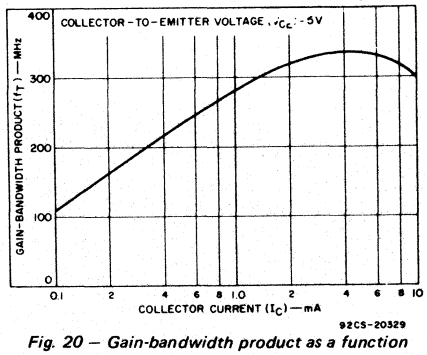


Fig. 20 – Gain-bandwidth product as a function of collector current (n-p-n).

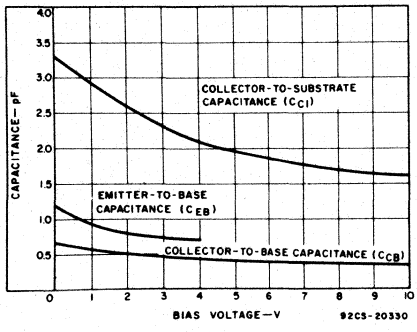


Fig. 21 – Capacitance as a function of bias voltage (n-p-n).

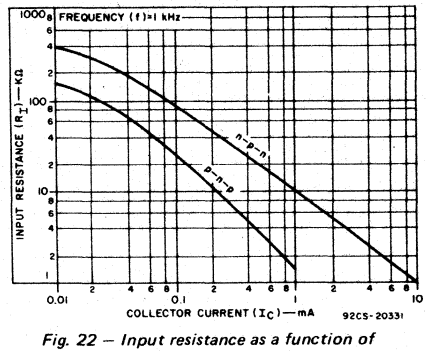


Fig. 22 – Input resistance as a function of collector current.

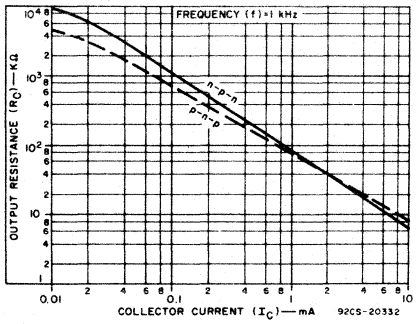


Fig. 23 – Output resistance as a function of collector current.

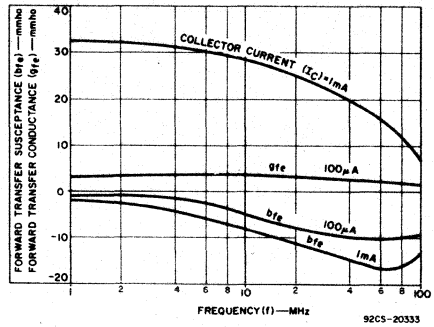


Fig. 24 – Forward transconductance as a function of frequency.

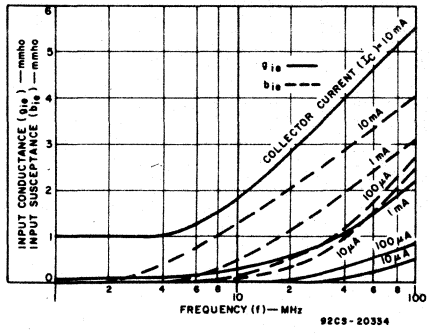


Fig. 25 – Input admittance as a function of frequency.

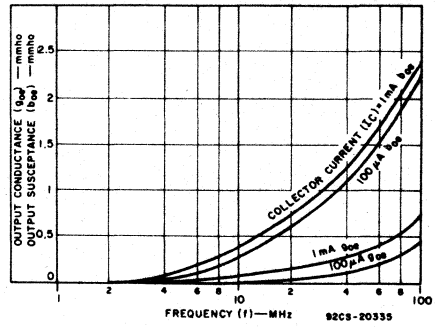


Fig. 26 – Output admittance as a function of frequency.

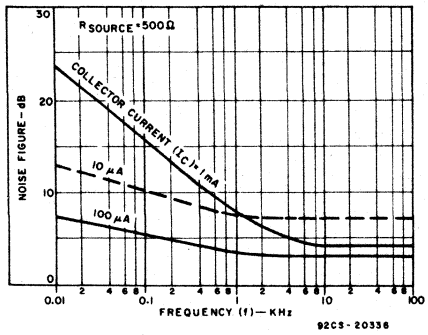


Fig. 27 – Noise figure as a function of frequency (p-n-p).

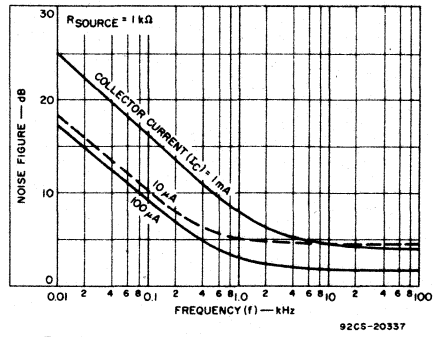


Fig. 28 – Noise figure as a function of frequency (p-n-p).

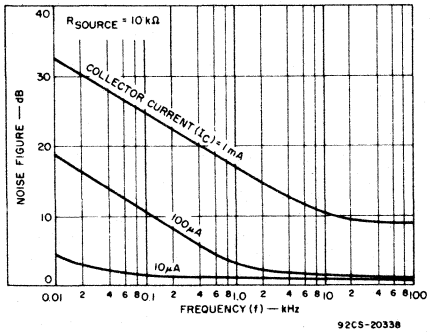


Fig. 29 – Noise figure as a function of frequency (p-n-p).

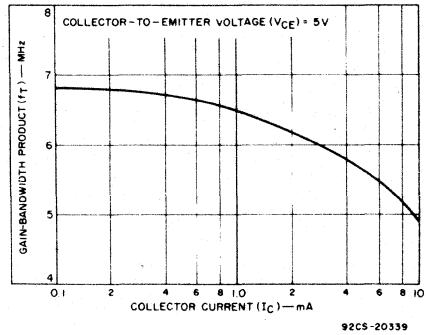


Fig. 30 – Gain-bandwidth product as a function of collector current (p-n-p).

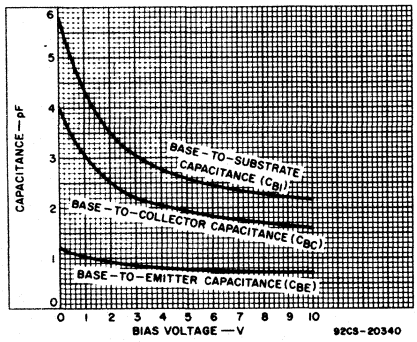


Fig. 31 – Capacitance as a function of bias voltage (p-n-p).

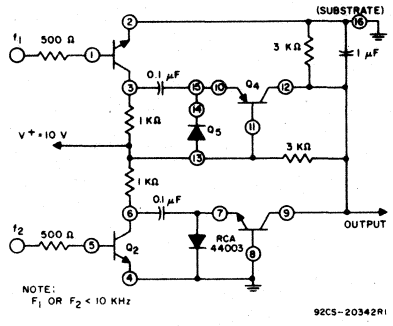


Fig. 32 – Frequency comparator using CA3096E.

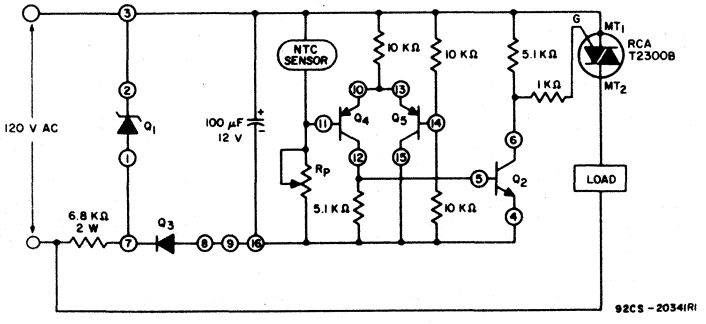


Fig. 33 – Line-operated level switch using CA3096AE or CA3096E.

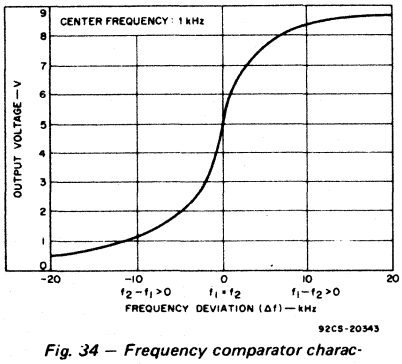


Fig. 34 – Frequency comparator characteristics.

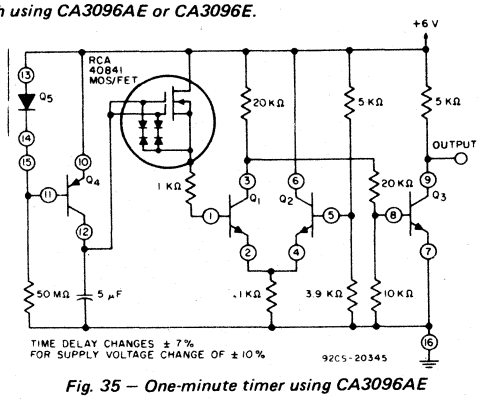


Fig. 35 – One-minute timer using CA3096AE and a MOS/FET.

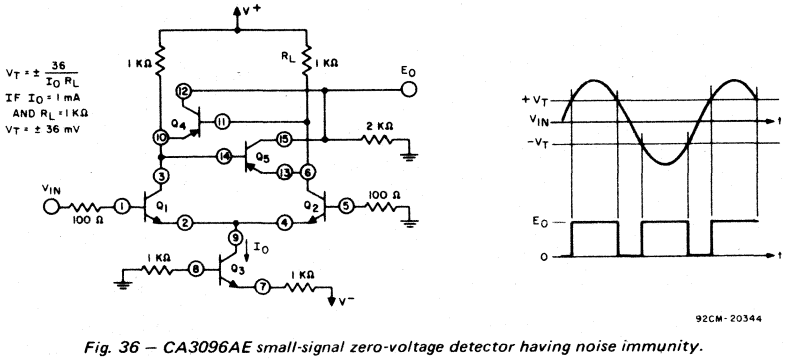


Fig. 36 – CA3096AE small-signal zero-voltage detector having noise immunity.

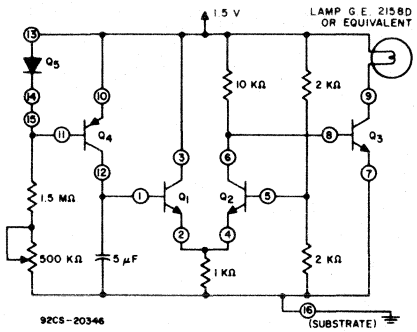


Fig. 37 – Ten-second timer operated form 1.5-volt supply using CA3096E.

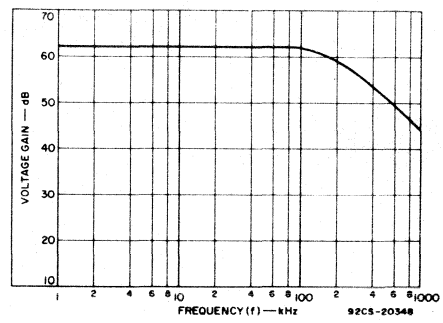


Fig. 38 – Gain-frequency characteristics.

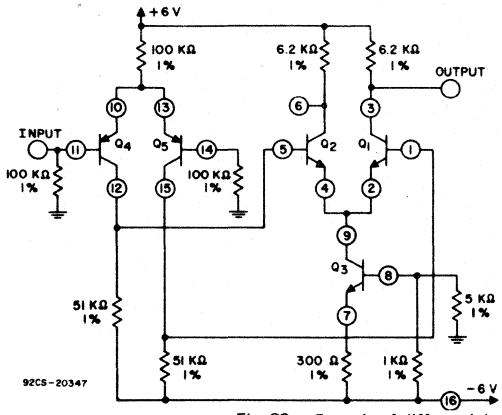
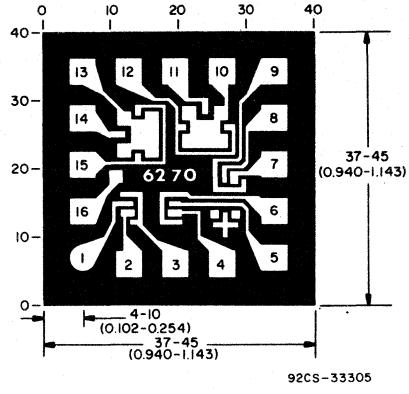


Fig. 39 – Cascade of differential amplifiers using CA3096AE.

Features:

1. Can be operated with either dual supply or single supply.
2. Wide-input common-mode range +5 V to −5 V.
3. Low bias current: $<1\ \mu A$.

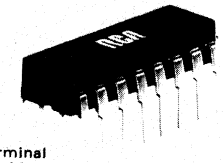


CA3096H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3097E



16-Lead Dual-In-Line Plastic Package

Thyristor/Transistor Array

For Military, Commercial, and Industrial Applications

Includes:

- *Uncommitted n-p-n transistor*
- *Sensitive-gate silicon controlled rectifier*
- *Programmable unijunction transistor (PUT)*
- *p-n-p/n-p-n transistor pair*
- *Zener diode*
- *Separate substrate connection*

Features:

- *Complete isolation between elements*
- *n-p-n transistor - V_{CEO} = 30 V (min.) I_C = 100 mA (max.)*
- *p-n-p/n-p-n transistor pair - beta ≥ 8000 (typ.) @ I_C = 10 mA, individual p-n-p, n-p-n, or transistor pair operation*
- *Programmable unijunction transistor [PUT] - peak-point current = 15 nA (typ.) at R_G = 1 MΩ; V_{AK} = ± 30 V*
- *(PUT) Extremely long RC time constants with low value of external capacitor*
- *Sensitive-gate silicon controlled rectifier (SCR) - 150 mA forward current (max.)*
- *Zener-diode impedance (Z_Z) = 15Ω (typ.) at 10 mA*

Applications:

- *Timers*
- *Light dimmers/motor controls*
- *Oscillators*
- *"One-shot" multivibrators*
- *Voltage regulators*
- *Comparators, Schmitt triggers*
- *Constant-current sources*
- *Amplifiers*
- *Logic circuits*
- *SCR triggering*
- *Pulse circuits*

RCA-CA3097E* Thyristor/Transistor Array is a monolithic integrated circuit that enables circuit designers to further integrate control systems. The CA3097E consists of five independent and completely isolated elements on one chip: an n-p-n transistor, a p-n-p/n-p-n transistor pair, a zener diode, a programmable unijunction transistor (PUT), and a sensitive-gate silicon controlled rectifier (SCR).

The CA3097 is supplied in either the 16-lead dual-in-line plastic package ("E" suffix) or the chip version ("H" suffix), and operates over the full military-temperature range of −55 to +125° C.

*Formerly Dev. No. TA6281.

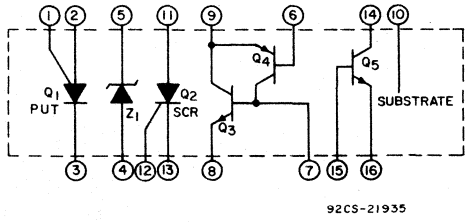


Fig. 1 — Schematic diagram of CA3097E.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

Isolation Voltage, any terminal to substrate*	+50 V
Dissipation, Total Package:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/°C
Ambient Temperature Range:	
Operating	−55 to +125°C
Storage	−65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265 °C
Each n-p-n Transistor (Q3,Q5)	
The following ratings apply with terminals 6 & 9 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	30 V
Collector-to-Base Voltage (V_{CBO})	50 V
Emitter-to-Base Voltage (V_{EBO})	5 V
Collector Current (I_C)	100 mA
Base Current (I_B)	20 mA
Dissipation (P_D)	500 mW
p-n-p Transistor (Q4)	
The following ratings apply with terminals 7 & 8 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	−40 V
Collector-to-Base Voltage (V_{CBO})	−50 V
Emitter-to-Base Voltage (V_{EBO})	−40 V
Collector Current (I_C)	−10 mA
Base Current (I_B)	−3 mA
Dissipation (P_D)	200 mW
p-n-p/n-p-n Transistor Pair (Q3,Q4)	
Dissipation (P_D)	500 mW
Programmable Unijunction Transistor, PUT (Q1)	
Gate-to-Cathode Positive Voltage (V_{GK})	30 V
Gate-to-Cathode Negative Voltage (V_{GKR})	5 V
Gate-to-Anode Negative Voltage (V_{GA})	30 V
Anode-to-Cathode Voltage (V_{AK})	±30 V
DC Anode Current	150 mA
Peak Anode Non-Recurrent Forward (On-State) Current (10 μs pulse)	2 A
Total Average Dissipation	300 mW
Silicon Controlled Rectifier, SCR (Q2)	
Repetitive Peak Reverse Voltage (V_{RRXM}), R_{GK} = 1 KΩ	30 V
Repetitive Peak Off-State Voltage (V_{DRXM}), R_{GK} = 1 kΩ	30 V
DC On-State Current (I_{TDC})	150 mA
Peak Surge (Non-Repetitive) On-State Current (10 μs pulse)	2 A
Forward Peak Gate Current (I_{GFM})	20 mA
Peak Gate-to-Cathode Reverse Voltage (V_{GRM})	5 V
Total Average Dissipation	300 mW
Zener Diode, (Z1)	
DC Current (I_Z)	25 mA
Dissipation (P_D)	250 mW

* One or more of the terminals of each element of the CA3097E is isolated from the substrate by a junction diode. In order to maintain electrical isolation between elements, the substrate terminal must be connected to a voltage which is no more positive than that of any other terminal. To avoid undesirable coupling between elements, the substrate terminal (terminal 10) should be maintained at either dc or signal (ac) ground.

CA3097E

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
n-p-n TRANSISTORS Q3, Q5 (TERMINALS 6 and 9 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = 10 V, I_E = 0		–	–	1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = 10 V, I_B = 0		–	–	10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = 100μA, I_B = 0		30	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0		50	–	–	V
COLLECTOR-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0		50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = 100μA, I_C = 0		5	7.5	10	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE(SAT)}$	I_C = 50mA, I_B = 5mA	5	–	–	0.65	V
		I_C = 10mA, I_B = 1 mA		–	0.10	–	
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE(SAT)}$	I_C = 10mA, I_B = 1mA	2	–	0.76	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.73	0.85	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = 3V, I_C = 10mA	4	100	130	–	
		V_{CE} = 3V, I_C = 50mA		80	120	–	
p-n-p TRANSISTOR Q4 (TERMINALS 7 and 8 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = -10 V, I_E = 0		–	–	–1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = -10 V, I_B = 0		–	–	–10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = -100μA, I_B = 0		–40	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = -10μA, I_E = 0		–50	–	–	V
EMITTER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)EIO}$	I_{EI} = 10μA, I_B = 0, I_E = 0		–50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = –10μA, I_C = 0		–40	–	–	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE(SAT)}$	I_C = -1mA, I_B = -100μA	6	–	–	–0.33	V
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE(SAT)}$	I_C = -1mA, I_B = –100μA	7	–	–0.7	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = -3 V, I_C = –100μA	8	–0.5	–0.6	–0.7	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = – 3 V, I_C = –100μA	9	30	60	–	
		V_{CE} = –3 V, I_C = –1 mA		40	–	–	
n-p-n/p-n-p TRANSISTOR PAIR Q3, Q4							
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} (n-p-n) = 3V, I_C = 10mA	10	–	8000	–	
		V_{CE} (n-p-n) = 3V, I_C = 50mA	10	–	6500	–	

ELECTRICAL CHARACTERISTICS (Cont'd.)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
PROGRAMMABLE UNIJUNCTION TRANSISTOR (PUT), Q1							
OFFSET VOLTAGE	V_T*	V_S = 10V, R_G = 10kΩ	11,22[a]	0.2	–	0.7	V
		V_S = 10V, R_G = 1MΩ		0.2	–	0.7	
ANODE-TO-CATHODE ON-STATE VOLTAGE	V_F	I_F = 50mA	12	–	0.90	1.5	V
		I_F = 100mA		–	1	–	
PEAK OUTPUT VOLTAGE	V_{OM}	C = 0.22μF Anode Supply Voltage = 20V	13,23	–	10	–	V
PEAK-POINT CURRENT	I_P	V_S = 10V, R_G = 10kΩ	14,22[a]	–	0.55	1	μA
		V_S = 10V, R_G = 1MΩ	–	–	0.015	0.15	
VALLEY-POINT CURRENT	I_V	V_S = 10V, R_G = 10kΩ	17,15	4	40	–	μA
		V_S = 10V, R_G = 1MΩ	16	–	–	25	
GATE REVERSE CURRENT	I_{GAO}	V_S = 30V	22[c]	–	0.02	–	nA
GATE REVERSE CURRENT	I_{GKS}	Anode-To-Cathode Short, V_S, = 30V	22[d]	–	0.2	–	nA
OUTPUT PULSE RISE TIME	t_r	Anode-Supply Voltage = 20V C = 0.22 μF	23	–	60	–	ns
SILICON CONTROLLED RECTIFIER (SCR), Q2							
PEAK OFF-STATE CURRENT: FORWARD	I_{DXM}	V_{DRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	μA
REVERSE	I_{RXM}	V_{RRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	
FORWARD DC VOLTAGE DROP	V_T	I_T = 50 mA	18	–	0.90	1.5	V
GATE-TO-SOURCE TRIGGER CURRENT	I_{GS}	T_A = 25°C	26	–	33	100	μA
		T_A = −55°C	26	–	50	–	
DC GATE-TRIGGER VOLTAGE	V_{GT}	V_L = 10V, R_L = 100Ω	19	–	0.55	0.75	V
HOLDING CURRENT	I_{HO}	R_{GK} = 1kΩ	20,24	–	1.2	–	mA
CRITICAL RATE-OF-RISE OF OFF-STATE VOLTAGE	dv/dt	EXPONENTIAL RISE, R_{GK} = 1kΩ, V_{DRXM} = 30V	25	–	150	–	V/μs
GATE-CONTROLLED TURN-ON TIME	t_{gt}	See Fig. 33	33	–	50	–	ns
CIRCUIT-COMMUTATED TURN-OFF TIME	t_q	See Fig. 33	33	–	10	–	μs
ZENER DIODE, Z1							
ZENER VOLTAGE	V_Z	I_Z = 10mA	21	7.2	8	8.8	V
ZENER IMPEDANCE	Z_Z	I_Z = 10mA, f = 1kHz		–	15	25	Ω
ZENER VOLTAGE TEMPERATURE COEFFICIENT	$(\Delta V_Z/V_Z)/\Delta T$	I_Z = 10mA		–	+0.05	–	%/°C
	$\Delta V_Z/\Delta T$			–	+4	–	mV/°C
ZENER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)ZIO}$	I_Z = 100μA TERM. 5 TO SUBSTRATE		50	80	– –	V

* $V_T = V_P - V_S$ (Fig. 22)

CA3097E

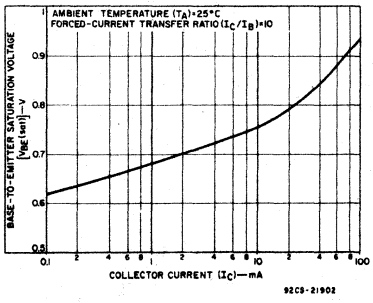


Fig. 2 – Base-to-emitter saturation voltage vs. collector current for n-p-n transistors Q3 & Q5.

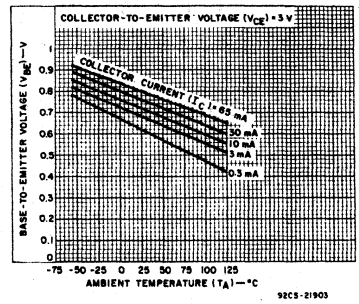


Fig. 3 – Base-to-emitter voltage vs. ambient temperature for n-p-n transistors Q3 & Q5.

TYPICAL CHARACTERISTICS

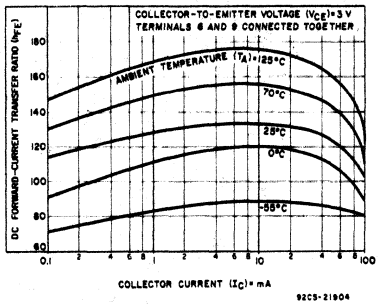


Fig. 4 – DC forward-current transfer ratio vs. collector current for n-p-n transistors Q3 & Q5.

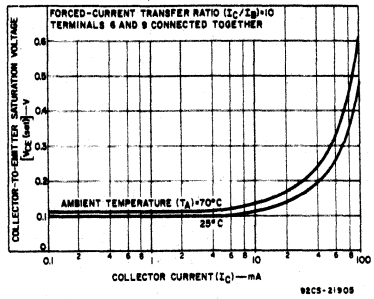


Fig. 5 – Collector-to-emitter saturation voltage vs. collector current for n-p-n transistors Q3 & Q5.

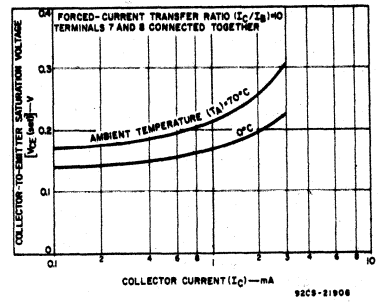


Fig. 6 – Collector-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.

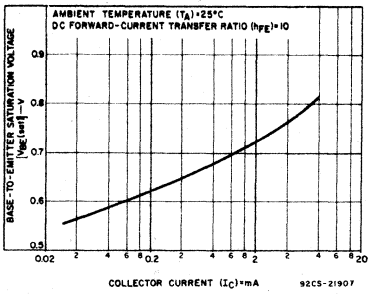


Fig. 7 – Base-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.

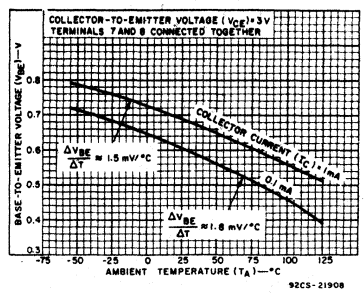


Fig. 8 – Base-to-emitter voltage vs. ambient temperature for p-n-p transistor Q4.

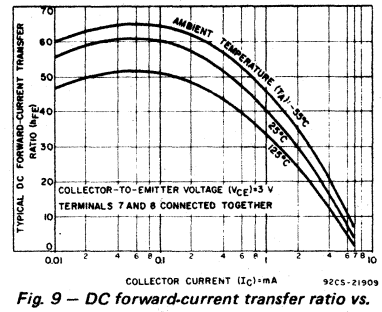


Fig. 9 – DC forward-current transfer ratio vs. collector current for p-n-p transistor Q4.

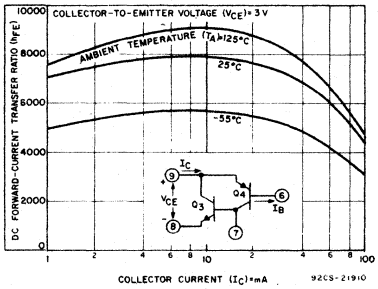


Fig. 10 – DC forward-current transfer ratio vs. collector current for transistor pair Q3, Q4.

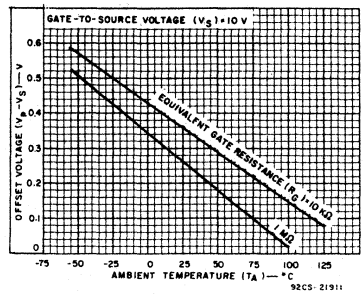


Fig. 11 – Offset voltage vs. ambient temperature for Q1 (PUT).

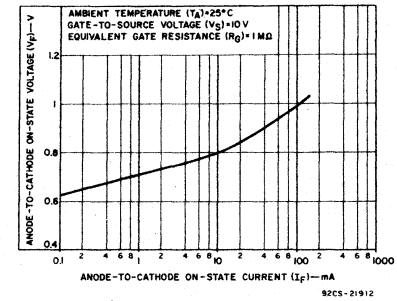


Fig. 12 – Anode-to-cathode on-state voltage vs. anode-to-cathode on-state current for Q1 (PUT).

TYPICAL CHARACTERISTICS (CONT'D)

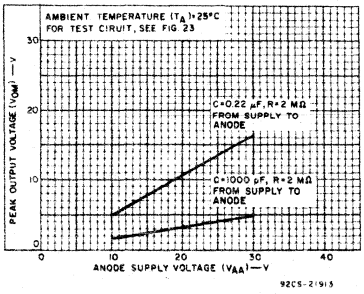


Fig. 13 – Peak output voltage vs. anode supply voltage for Q1 (PUT).

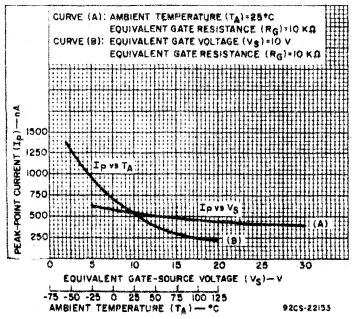


Fig.14 – Peak-point current vs. gate-source voltage and ambient temperature for Q1 (PUT).

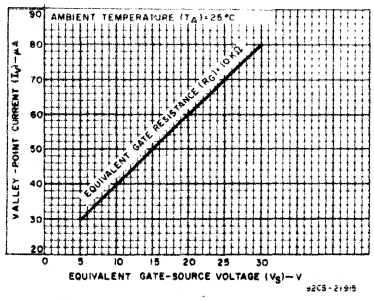


Fig.15 – Valley-point current vs. gate-source voltage for Q1 (PUT).

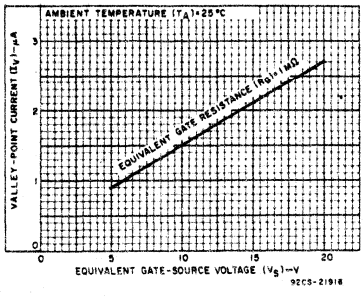


Fig.16 – Valley-point current vs. gate-source voltage for Q1 (PUT).

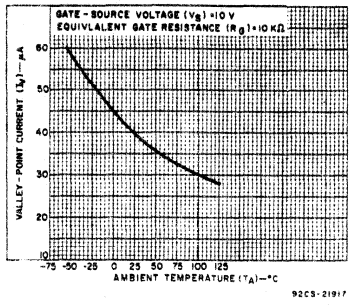


Fig. 17 – Valley-point current vs. ambient temperature for Q1 (PUT).

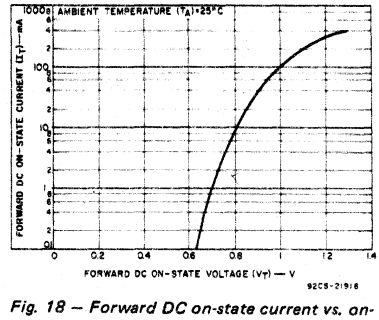


Fig. 18 – Forward DC on-state current vs. on-state voltage for Q2 (SCR).

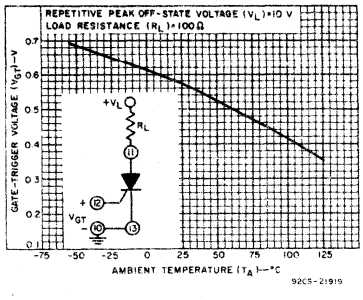


Fig. 19 – Gate-trigger voltage vs. ambient temperature for Q2 (SCR).

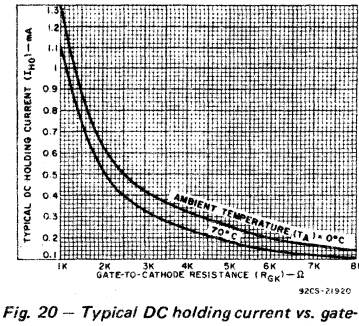


Fig. 20 – Typical DC holding current vs. gate-to-cathode resistance for Q2 (SCR).

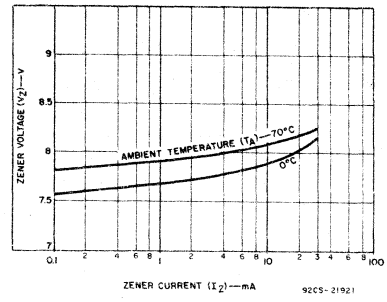


Fig. 21 – Zener voltage vs. zener current for Z1.

OPERATING CONSIDERATIONS FOR CA3097E

1. Composite p-n-p/n-p-n Transistors Q3, Q4 (See Fig. 3)

To use Q3 as an individual n-p-n transistor, join terminals no. 6 and no. 9 to disable p-n-p transistor Q4.

The appropriate terminal connections are then:

Collector..... terminal 9
Base ..... terminal 7
Emitter..... terminal 8

To use Q4 as an individual p-n-p transistor, join terminals no. 7 and no. 8 to disable n-p-n transistor Q3.

The appropriate terminal connections are then:

Collector..... terminal 7
Base ..... terminal 6
Emitter..... terminal 9

To use Q3 and Q4 as a composite use terminals 6, 7, 8, and 9 as required.

2. Programmable Unijunction Transistor Q1 (PUT)

The programmable unijunction transistor is essentially an anode-gate SCR. The volt-ampere characteristic of the device is shown in Fig. 22. When an equivalent Thevenin source (V_S, R_G), as shown in Fig. 22, is applied to the gate terminal the device will be "off" if the anode-voltage is negative with respect to the gate voltage. Under this condition, any current flow is exclusively leakage current. When the anode voltage becomes more positive than the gate voltage by an increment equal to the threshold voltage (V_T = 0.4 V typ.), the device can turn "on" only if the current available at the anode terminal **is greater** than the specified peak-point current. The PUT will then switch through its negative-resistance region to the "on" state (low anode-to-gate voltage). It should be noted that I_P is not the maximum current allowed through the device, but is the current required at the peak of the V-I curve. I_P is typically a very low value of current.

After the PUT has switched to its low-impedance state, the device will remain "on" if the anode-current (I_A) exceeds the valley-point current (I_V). If $I_A < I_V$, the PUT will switch back to its high-impedance "off" state. Thus, the PUT can be made to "latch" or recover, depending on I_V. Since I_V is a function of the "on"-state gate current (which depends on R_G and V_S) a choice of R_G and/or V_S will determine the operating mode, i.e., "off" state→"on" state or "off" state → "on" state → "off" state. The value of I_V increases directly as a function of V_G and inversely with R_G. The PUT in the CA3097E has a low I_P.....I_P = 15 nA at V_S = 10 V, R_G = 1 MΩ. This low value of I_P indicates that an extremely large value of anode-supply resistor, e.g. 60 MΩ (typ.), can be used in timing circuits requiring long RC time constants. This becomes important when considering the size of the external

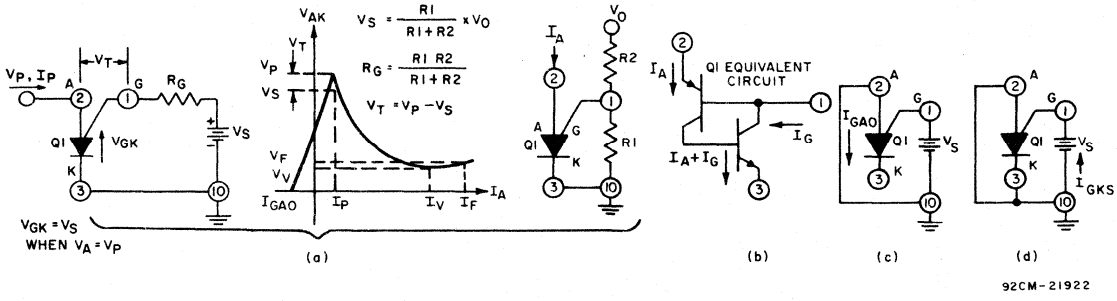


Fig. 22 – General anode characteristics for Q1 (PUT).

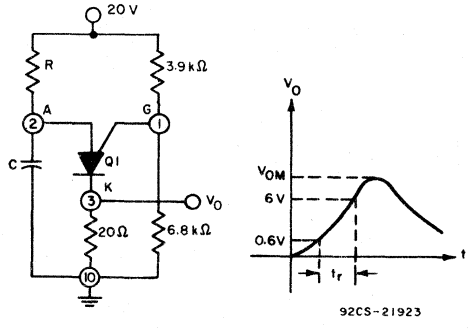


Fig. 23 – Output pulse characteristics for Q1 (PUT).

OPERATING CONSIDERATIONS (CONT'D)

timing capacitor to be used. Consequently, the use of the PUT in the CA3097E is advantageous since it has a lower I_P than most discrete PUT's.

Temperature Compensation of Switching Point

As described previously, the PUT will switch to its low-impedance state when its anode voltage is approximately a diode-drop above the gate voltage. Since the anode-to-gate threshold voltage vs. temperature characteristic is similar to that of a typical silicon-diode junction, a compensating series diode such as used in the circuit of Fig. 29 (Z1 connected as forward-biased diode) considerably reduces the effect of temperature on the switching point.

Bypassing Anode Current

If the PUT gate equivalent source is such that $I_A > I_V$, the PUT will remain "on". A method for turning the PUT off is by shunting current away from the anode until $I_A < I_V$. An example of this technique is the oscillator circuit of Fig. 29. Q3 transistor is turned "on" after the PUT fires and shunts current away from the anode, thereby forcing $I_A < I_V$. The PUT then turns "off" allowing C_T to recharge through R_T, to repeat the cycle.

Protecting The PUT Against Discharge Current Of The Capacitor

A current-limiting resistor in series with the PUT is normally required to dissipate capacitive discharge energy (see Figs. 23 and 29).

Silicon Controlled Rectifier, Q2 (SCR)

The SCR should be used with a 1 kΩ (or less) resistor connected between the cathode and gate terminals if the SCR is to be subjected to its maximum forward and reverse voltage ratings (V_{DXM} and V_{RXM}). Selecting a value for R_{GK} of 1 kΩ (or lower) increases the capability of the device to withstand greater dv/dt and increases the noise immunity of the SCR against false triggering at the gate. Practical considerations such as available current drive from the triggering devices (e.g., a PUT) will determine the lowest value of R_{GK} at which the SCR will fire with a $V_{GK} \approx 0.55$ V. With a value of 500Ω for R_{GK}, the trigger source must be capable of supplying 1.1 mA. R_{GK} should be non-inductive within the frequency band of the noise transients normally encountered in a particular application.

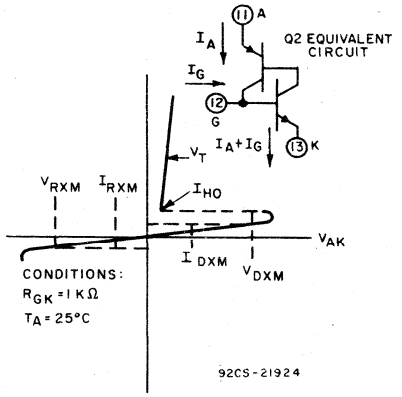


Fig. 24 – Principle voltage-current characteristics for Q2 (SCR).

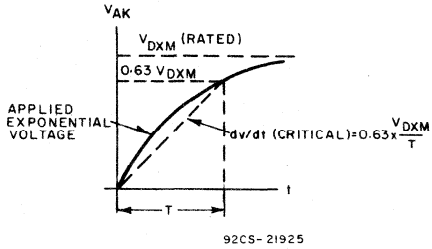
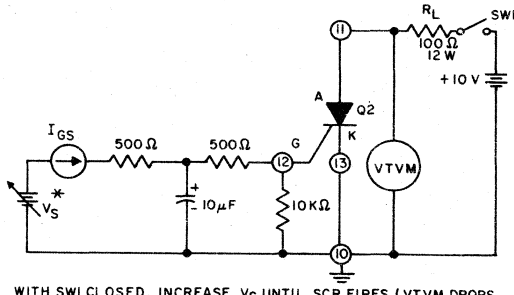


Fig. 25 – Definition of critical rate of rise of off-state voltage for Q2 (SCR).



WITH SWI CLOSED, INCREASE V_S UNTIL SCR FIRES (VTVM DROPS FROM 10V TO APPROXIMATELY 1V). I_{GS} (TRIGGER) IS MEASURED JUST PRIOR TO THIS TRIGGERING POINT. NOTE THAT I_{GS} MAY DECREASE AS V_S IS INCREASED DUE TO CURRENT DRAWN OUT OF THE GATE TERMINAL OF THE SCR AS IT TURNS ON. TO UNLATCH THE SCR OPEN SWI.

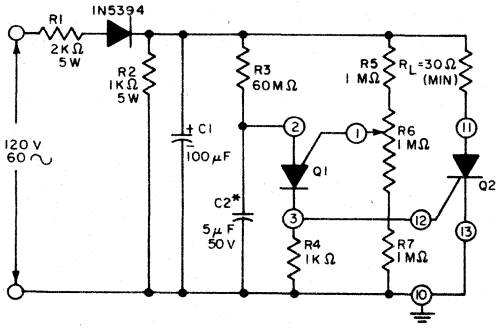
* V_S SHOULD BE CAPABLE OF SUPPLYING MILLIVOLT INCREMENTS NEAR THE TRIGGER POINT

92CS-21926

Fig. 26 – Test circuit for determining I_{GS} in Q2 (SCR).

CA3097E

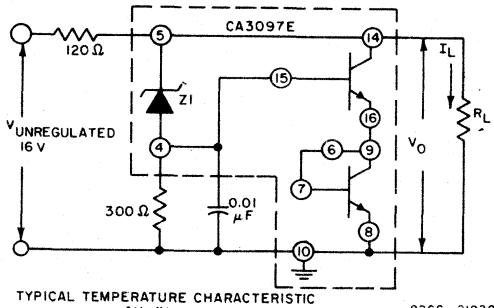
APPLICATIONS CIRCUITS



TIMING PERIOD ≈ 200 SEC. WITH 1 MΩ POT CENTERED
TIMING CYCLE BEGINS WHEN AC IS APPLIED
* SPRAGUE TYPE 4308, 5 μF AT 50 V
SPRAGUE TYPE 6308, 5 μF AT 50 V
OR EQUIVALENT

92CS-21927

Fig. 27 – AC line-operated one-shot timer.



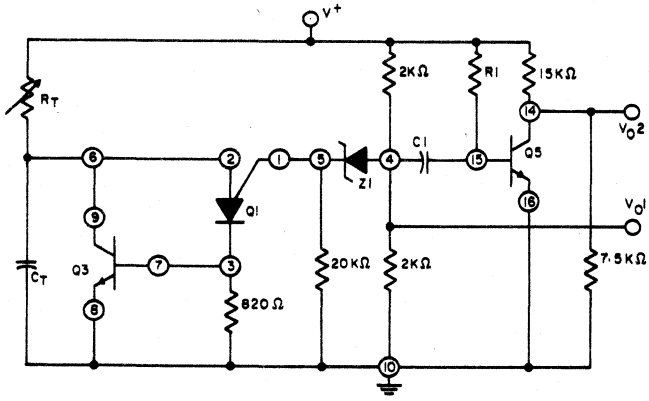
TYPICAL TEMPERATURE CHARACTERISTIC
@ $R_L = 330\,\Omega$, $\frac{\Delta V_O/V_O}{\Delta T} \times 100 = \pm 0.01\,\%/°C$

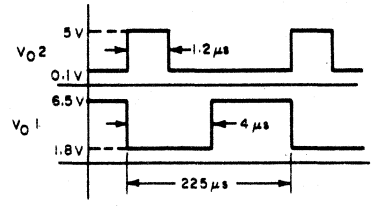
92CS-21928

TYP. LOAD REGULATION @ $I_L = 0$ TO 40 mA, $(\Delta V_O/V_O) \times 100 = -3\,\%$ (NO LOAD TO FULL LOAD)

TYP. LINE REGULATION @ $R_L = 330\,\Omega$, $\frac{\Delta V_O/V_O}{\Delta V_{UNREG.}} \times 100 = \pm 0.55\,\%/V$

Fig. 28 – Temperature-compensated shunt regulator.





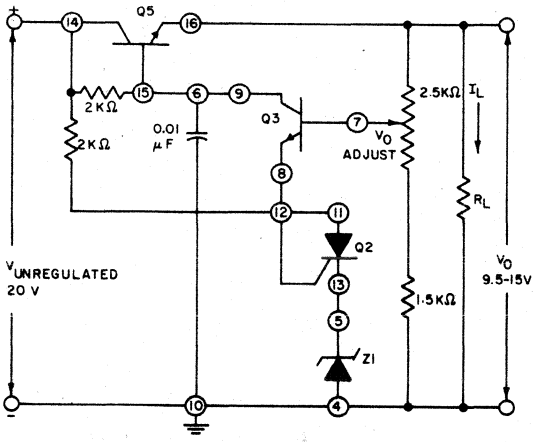
PULSE RATE ADJUSTED BY VARYING R_T OR C_T.
OUTPUT PULSE WIDTH ADJUSTED BY R_1C_1 DIFFERENTIATING TIME CONSTANT

TYPICAL OPERATION FOR:
$V^+ = 15$ V, $C_T = 0.1\,\mu F$, $R_T = 4.3\,K\Omega$
$C_1 = 82$ pF, $R_1 = 60K\Omega$

92CM-21929

Fig. 29 – Pulse generator.

APPLICATIONS CIRCUITS



TYPICAL LOAD REGULATION @ V_O = 12 V, I_L = 0 TO 40 mA

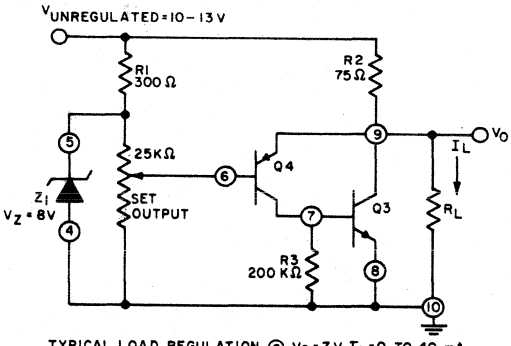
$$\frac{\Delta V_O}{V_O} \times 100 = \pm 0.4\ \%$$ (NO LOAD TO FULL LOAD)

TYPICAL LINE REGULATION @ V_O = 12 V

$$\frac{\Delta V_O / V_O}{\Delta V_{UNREG.}} \times 100 = \pm 0.45\ \%/V$$

92CS-21930

Fig. 30 – Series voltage regulator.



TYPICAL LOAD REGULATION @ V_O = 7 V, I_L = 0 TO 40 mA

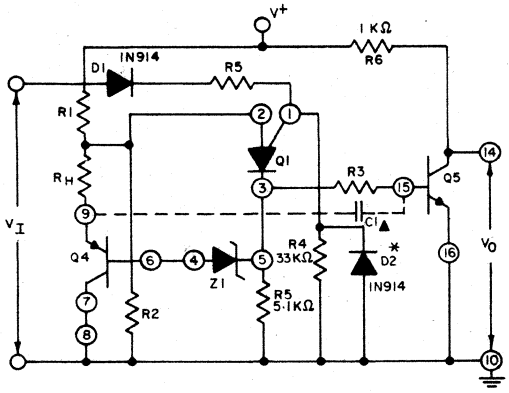
$$\frac{\Delta V_O}{V_O} \times 100 = -1.1\ \%$$

TYPICAL LINE REGULATION @ V_O = 7 V, I_L = 20 mA

$$\frac{\Delta V_O}{\Delta V_{UNREGULATED}} = \pm 0.85\ \%/VOLT$$

92CS-21931

Fig. 31 – 5 to 7.5 V shunt regulator.

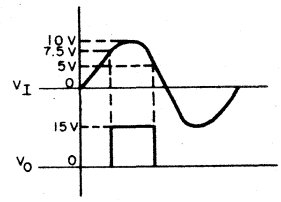


▲ OPTIONAL SPEED-UP CAPACITOR
* REQUIRED IF V_I SWINGS BELOW GROUND

TYPICAL OPERATING CONDITIONS:
FREQUENCY IN = 0 – 10 KHz
SUPPLY VOLTAGE (V^+) = 15 V
R1, R2, R_H = 5.1 KΩ
R3 = 6.2 KΩ, R_S = 300 Ω
C_I = 820 pF
$V_{TH}U$ = 7.5 V, $V_{TH}L$ = 5 V
HYSTERESIS VOLTAGE = 2.5 V
UPPER THRESHOLD VOLTAGE ($V_{TH}U$) $\approx V^+ \frac{R2}{R1+R2}$

LOWER THRESHOLD VOLTAGE ($V_{TH}L$) $\approx \frac{(V^+)\left(\frac{R2\,R_H}{R2+R_H}\right)}{\frac{R2\,R_H}{R2+R_H}+R1}$

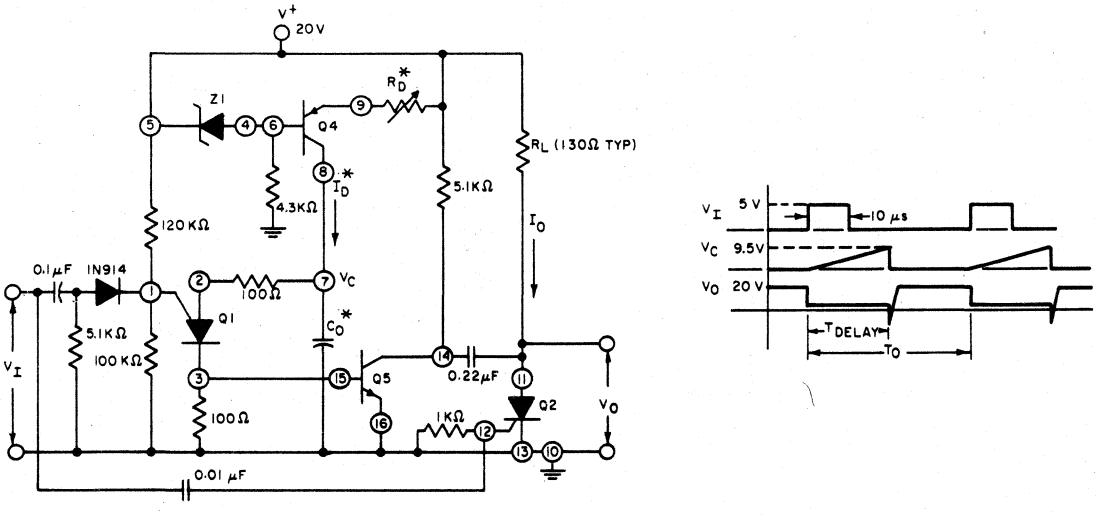
HYSTERESIS VOLTAGE = $V_{TH}U - V_{TH}L$



92CM-21932

Fig. 32 – Schmitt trigger.

APPLICATIONS CIRCUITS (CONT'D)

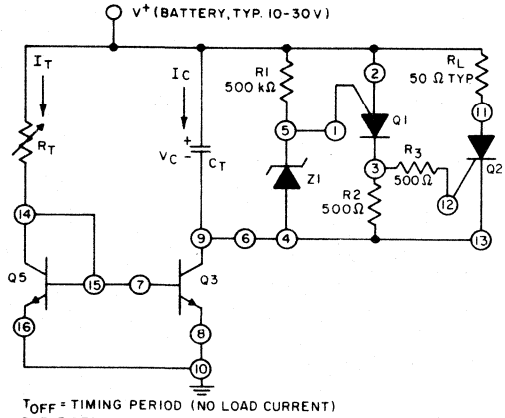


*MONOSTABLE DELAY TIME SET BY ADJUSTMENT OF I_D (VARY R_D) OR BY $C_D.I_D$ MUST BE GREATER THAN I_V OF Q1 (PUT) FOR MONOSTABLE OPERATION.

Q2 (SCR) SWITCHING TIMES:
GATE-CONTROLLED TURN-ON TIME (t_{gt}) = 50 ns (TYP.)
CIRCUIT-COMMUTATED TURN-OFF TIME (t_q) = 10 μs (TYP)

92CM-21933

Fig. 33 – Monostable multivibrator with variable delay.



T_{OFF} = TIMING PERIOD (NO LOAD CURRENT)
PUT FIRES WHEN $V_C \approx 8$ V

$V_C = \frac{I_C (T_{OFF})}{C_T}$, $I_C \approx I_T$ (Q3, Q5 MATCHED)

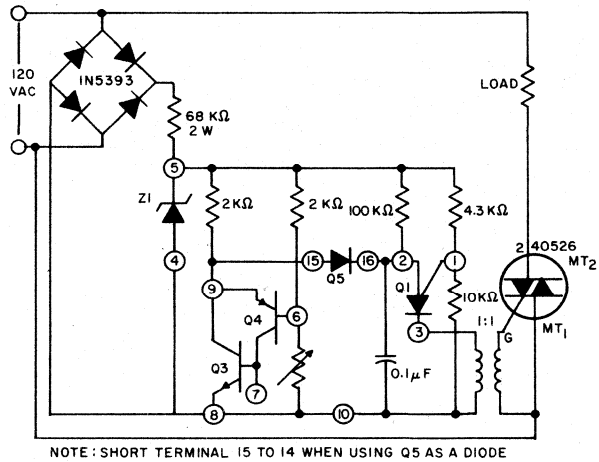
I_T SET BY ADJUSTING R_T, $I_T \approx \frac{V^+ - 0.7}{R_T}$

T_{ON} = CAPACITOR DISCHARGE TIME THROUGH LOAD. LOAD TURNS OFF WHEN SCR ANODE CURRENT FALLS BELOW HOLDING CURRENT (I_{HO}). TYPICAL I_{HO} = 1.2 mA

EXAMPLE: FOR TIMING PERIOD OF 8.3 MIN
C_T = 1000 μF, I_T = 16 μA
$R_T = \frac{V^+ - 0.7}{I_T}$ (FOR V^+ = 16 V, $R_T \approx$ 1 MΩ)

92CS-21934

Fig.34 – Low-current-drain battery-operated long interval astable timer.



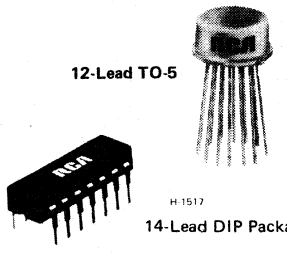
NOTE: SHORT TERMINAL 15 TO 14 WHEN USING Q5 AS A DIODE

92CS-22178

Fig.35 – Phase control circuit.

CA3118, CA3146, CA3183 Types

High-Voltage Transistor Arrays



Applications

- General use in signal processing systems in DC through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- Lamp and relay drivers (CA3183AE, E)
- Thyristor firing (CA3183AE, E)

Features

- Matched general-purpose transistors
- V_{BE} matched ±5mV max.
- Operation from DC to 120 MHz (CA3118AT, T; CA3146AE, E)
- Low-noise figure: 3.2dB typ. at 1kHz (CA3118AT, T; CA3146AE, E)
- High I_C: 75mA max. (CA3183AE, E)

RCA-CA3118AT, CA3118T, CA3146AE, CA3146E, CA-3183AE, and CA3183E* are general-purpose high-voltage silicon n-p-n transistor arrays on a common monolithic substrate.

Types CA3118AT and CA3118T consist of four transistors with two of the transistors connected in a Darlington configuration. These types are well suited for a wide variety of applications in low-power systems in the DC through VHF range. Both types are supplied in a hermetically sealed 12-lead TO-5 type package and operate over the full military temperature range. (CA3118AT and CA3118T are high-voltage versions of the popular predecessor type CA3018.

Types CA3146AE and CA3146E consist of five transistors with two of the transistors connected to form a differentially-connected pair. These types are recommended for low-power applications in the DC through VHF range. Both types are supplied in a 14-lead dual-in-line plastic package and operate over the ambient temperature range of −40°C to +85°C. (CA3146AE and CA3146E are high-voltage versions of the popular predecessor type CA3046.)

Types CA3183AE and CA3183E consist of five high-current transistors with independent connections for each transistor. In addition two of these transistors (Q1 and Q2) are matched at low-current (i.e. 1mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design. Both types are supplied in a 16-lead dual-in-line plastic package and operate over the ambient temperature range of −40°C to +85°C. (CA3183AE and CA3183E are high-voltage versions of the popular predecessor type CA3083.)

The types with an "A" suffix are premium versions of their non-"A" counterparts and feature tighter control of breakdown voltages making them more suitable for higher voltage applications.

For detailed application information, see companion Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated Circuit Transistor Array."

*Formerly Developmental Types Nos.

CA3118AT	– TA6091	CA3146E	– TA6181
CA3118T	– TA6182	CA3183AE	– TA6094
CA3146AE	– TA6084	CA3183E	– TA6183

TYPE	P_T● max. mW	I_C max. mA	V_{CEO} max. V	V_{CBO} max. V	$V_{CE\ sat.}$ at 10 mA typ. V	h_{FE} at 1mA, & V_{CE}=5V typ.	V_{IO} Diff. Pair at 1mA max. mV	I_{IO} Diff. Pair at 1mA max. μA	T_A Range (Operating) °C
VALUES APPLY FOR EACH TRANSISTOR									
CA3118AT	300	50	40	50	0.33	95	±5	2	−55 – +125
CA3118T	300	50	30	40	0.33	95	±5	2	−55 – +125
CA3146AE	300	50	40	50	0.33	95	±5	2	−40 – +85
CA3146E	300	50	30	40	0.33	95	±5	2	−40 – +85
CA3183AE	500	75	40	50	0.16	75	±5	2.5	−40 – +85
CA3183E	500	75	30	40	0.16	75	±5	2.5	−40 – +85

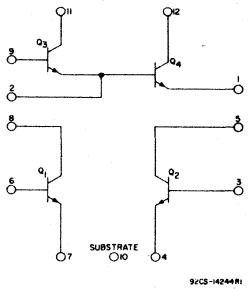
● Caution on Total Package Power Dissipation: The maximum total package dissipation rating for the CA3118 Series circuits is 450 mW at temperatures up to +85°C, then derate linearly at 5 mW°C. The maximum total package dissipation rating for the CA3146 and CA3183 Series circuits is 750 mW at temperatures up to +55°C, then derate linearly at 6.67 mW°C.

CA3118, CA3146, CA3183 Types

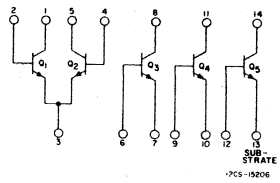
MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:		
Any one transistor –		
CA3118AT, CA3118T, CA3146AE, CA3146E	300	mW
CA3183AE, CA3183E	500	mW
Total package –		
Up to 85°C (CA3118AT, CA3118T)	450	mW
Up to 55°C (CA3146AE, CA3146E, CA3183AE, CA3183E)	750	mW
Above 85°C (CA3118AT, CA3118T)	derate linearly 5	mW/°C
Above 55°C (CA3146AE, CA3146E, CA3183AE, CA3183E)	derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating –		
CA3118AT, CA3118T	–55 to +125	°C
CA3146AE, CA3146E, CA3183AE, CA3183E	–40 to +85	°C
Storage (all types)	–65 to +150	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO}):		
CA3118AT, CA3146AE, CA3183AE	40	V
CA3118T, CA3146E, CA3183E	30	V
Collector-to-Base Voltage (V_{CBO}):		
CA3118AT, CA3146AE, CA3183AE	50	V
CA3118T, CA3146E, CA3183E	40	V
Collector-to-Substrate Voltage (V_{CIO}): ■		
CA3118AT, CA3146AE, CA3183AE	50	V
CA3118T, CA3146E, CA3183E	40	V
Emitter-to-Base Voltage (V_{EBO}) all types	5	V
Collector Current –		
CA3118AT, CA3118T, CA3146AE, CA3146E	50	mA
CA3183AE, CA3183E	75	mA
Base Current (I_B) – CA3183AE, CA3183E	20	mA

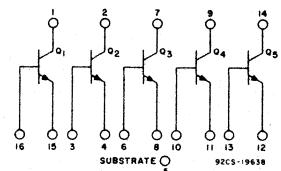
■ The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.



CA3118AT, CA3118T



CA3146AE, CA314E



CA3183AE, CA3183E

Fig. 1 – Schematic diagrams of high-voltage arrays.

COMPARISON OF RELATED PREDECESSOR TYPE WITH TYPES IN THIS DATA BULLETIN

	DATA FILE NO.	V_{CEO} min.	V_{CBO} min.	V_{CE} sat. typ. V	V_{BE} typ. V	I_C max. mA	C_{CB} typ. pF	C_{CI} typ. pF	C_{EB} typ. pF
				I_C=10 mA	I_C=1 mA				
CA3018	338	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3018A	338	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3118AT		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3118T		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C=10 mA	I_C=1 mA				
CA3046	341	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3146AE		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3146E		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C=50 mA	I_C=10 mA				
CA3083	481	15	20	0.4	0.74	100	–	–	–
CA3183AE		40	50	1.7	0.75	75	–	–	–
CA3183E		30	40	1.7	0.75	75	–	–	–

NOTE: Related predecessor types are shown in shaded areas.

STATIC ELECTRICAL CHARACTERISTICS — CA3118 and CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS $T_A = 25^oC$	Typ. Char. Curve Fig. No.	LIMITS CA3118AT, CA3146AE Min.	CA3118AT, CA3146AE Typ.	CA3118AT, CA3146AE Max.	CA3118T, CA3146E Min.	CA3118T, CA3146E Typ.	CA3118T, CA3146E Max.	UNITS
For Each Transistor:										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	–	50	72	–	40	72	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	–	40	56	–	30	56	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 10\mu A$, $I_B = 0$, $I_E = 0$	–	50	72	–	40	72	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$	–	5	7	–	5	7	–	V
Collector-Cutoff Current	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	2	–	see curve	5	–	see curve	5	μA
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$	3	–	0.002	100	–	0.002	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=5V, I_C=10 mA	4	–	85	–	–	85	–	–
		V_{CE}=5V, I_C=1 mA	4	30	100	–	30	100	–	–
		V_{CE}=5V, I_C=10μA	4	–	90	–	–	90	–	–
Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 3V$, $I_C = 1mA$	5	0.63	0.73	0.83	0.63	0.73	0.83	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	$I_C = 10mA$, $I_B = 1mA$	6	–	0.33	–	–	0.33	–	V
For transistors Q3 and Q4 (Darlington Configeration):										
Collector-Cutoff Current (CA3118AT and CA3118T only)	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$	–	–	–	5	–	–	–	μA
DC Forward-Current Transfer Ratio (CA3118AT and CA3118T only)	h_{FE}	$V_{CE} = 5V$, $I_C = 1mA$	7	1500	9000	–	1500	9000	–	–
Base-to-Emitter (Q3 to Q4)	V_{BE}	V_{CE}=5V, I_E=10mA	8	–	1.46	–	–	1.46	–	V
		V_{CE}=5V, I_E=1mA	8,9	–	1.32	–	–	1.32	–	V
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\lvert\frac{\Delta V_{BE}}{\Delta T}\right\rvert$	$V_{CE} = 5V$, $I_E = 1mA$	–	–	4.4	–	–	4.4	–	mV/°C
For transistors Q1 and Q2 (AS a Differential Amplifier):										
Magnitude of Input Offset Voltage $\lvert V_{BE1} = V_{BE2}\rvert$	$\lvert V_{IO}\rvert$	$V_{CE} = 5V$, $I_E = 1mA$	10,11	–	0.48	5	–	0.48	5	mV
Magnitude of h_{FE} Ratio (CA3118AT and CA3118T only)		$V_{CE} = 5V$, $I_{C1} = I_{C2} = 1mA$	–	0.9	1.0	1.1	0.9	1.0	1.1	–
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\lvert\frac{\Delta V_{BE}}{\Delta T}\right\rvert$	$V_{CE} = 5V$, $I_E = 1mA$	–	–	1.9	–	–	1.9	–	mV/°C
Magnitude of V_{IO} ($V_{BE1} - V_{BE2}$) Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO}}{\Delta T}\right\rvert$	$V_{CE} = 5V$, $I_{C1} = I_{C2} = 1mA$	–	–	1.1	–	–	1.1	–	μV/°C
Magnitude of Input Offset Current $\lvert I_{IO_1} - I_{IO_2}\rvert$ (CA3146AE and CA3146E only)	I_{IO}	$V_{CE} = 5V$, $I_{C_1} = I_{C_2} = 1$ mA	12	–	0.3	2	–	0.3	2	μA

CA3118, CA3146, CA3183 Types

DYNAMIC ELECTRICAL CHARACTERISTICS – CA3118 and CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C	Typ. Char. Curve Fig.No.	CA3118AT CA3146AE			CA3118T CA3146E			UNITS
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Low Frequency Noise Figure	NF	f = 1kHz, V_{CE} = 5V, I_C = 100μA, Source resistance = 1 kΩ	14	–	3.25	–	–	3.25	–	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Foward-Current Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	16	–	100	–	–	100	–	–
Short-Circuit Input Impedance	h_{ie}		16	–	2.7	–	–	3.5	–	kΩ
Open-Circuit Output Impedance	h_{oe}		16	–	15.6	–	–	15.6	–	μmho
Open-Circuit Reverse Voltage Transfer Ratio	h_{re}		16	–	$1.8x10^{-4}$	–	–	$1.8x10^{-4}$	–	–
Admittance Characteristics:										
Foward Transfer Admittance	Y_{fe}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	17	–	31-j1.5	–	–	31-j1.5	–	mmho
Input Admittance	Y_{ie}		18	–	0.35+j0.04	–	–	0.3+j0.04	–	mmho
Output Admittance	Y_{oe}		19	–	0.001+j0.03	–	–	0.001+j0.03	–	mmho
Reverse Transfer Admittance	Y_{re}		20		See curve			See curve		mmho
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 3mA	21	300	500	–	300	500	–	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 5V, I_E = 0	22	–	0.70	–	–	0.70	–	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 5V, I_C = 0	22	–	0.37	–	–	0.37	–	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 5V, I_C = 0	22	–	2.2	–	–	2.2	–	pF

STATIC ELECTRICAL CHARACTERISTICS – CA3183 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C	Typ. Char Curve Fig. No.	LIMITS CA3183AE			CA3183E			UNITS
				Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each Transistor:										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=100μA, I_E=0	–	50	–	–	40	–	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	–	40	–	–	30	–	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI}=100μA, I_B=0, I_E = 0	–	50	–	–	40	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	–	5	–	–	5	–	–	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	23	–	–	10	–	–	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	24	–	–	1	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}= 3 V, I_C = 10mA	25,26	40	–	–	40	–	–	–
		V_{CE} = 5V, I_C = 50mA	–	40	–	–	40	–	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	27	0.65	0.75	0.85	0.65	0.75	0.85	V
Collector-to-Emitter Saturation Voltage	*V_{CEsat}	I_C = 50mA, I_B = 5mA	28	–	1.7	3.0	–	1.7	3.0	V
For Transistors Q1 and Q2 (As a Differential Amplifier):										
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	29	–	0.47	5	–	0.47	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		30	–	0.78	2.5	–	0.78	2.5	μA

* A maximum dissipation of 5 transistors x 150mW = 750mW is possible for a particular application.

TYPICAL STATIC CHARACTERISTICS CURVES – CA3118 and CA3146 SERIES

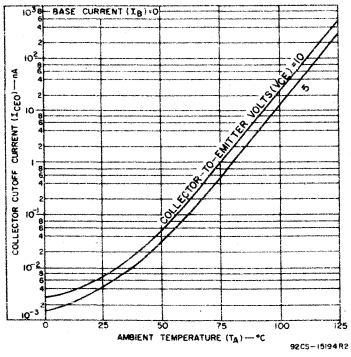


Fig. 2 – I_{CEO} vs. T_A for any transistor.

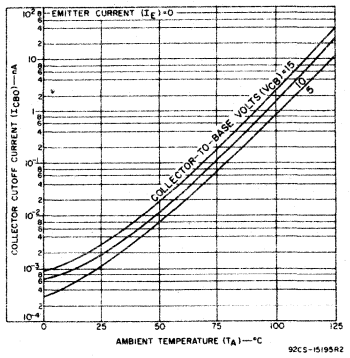


Fig. 3 – I_{CBO} vs. T_A for any transistor.

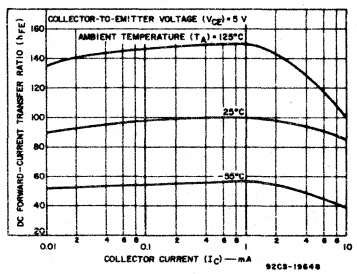


Fig. 4 – h_{FE} vs. I_C for any transistor.

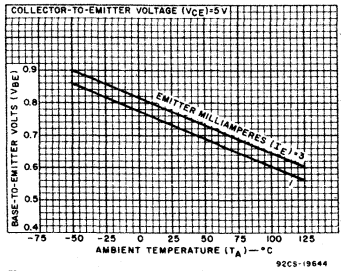


Fig. 5 – V_{BE} vs. T_A for any transistor.

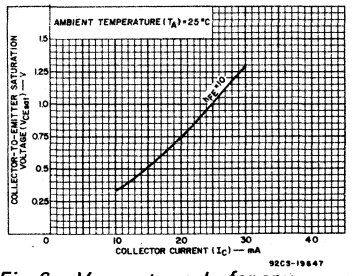


Fig. 6 – $V_{CE\ sat}$ vs. I_C for any transistor.

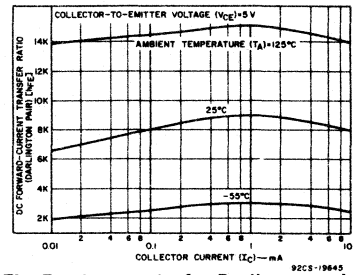


Fig. 7 – h_{FE} vs. I_C for Darlington pair (Q3 and Q4) for types CA3118AT and CA3118T.

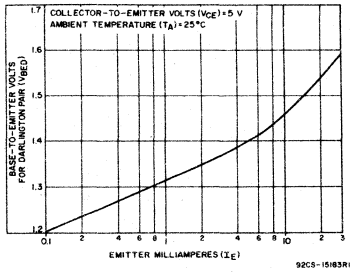


Fig. 8 – V_{BE} vs. I_E for Darlington pair (Q3 and Q4).

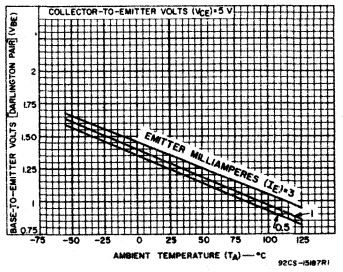


Fig. 9 – V_{BE} vs. T_A for Darlington pair (Q3 and Q4).

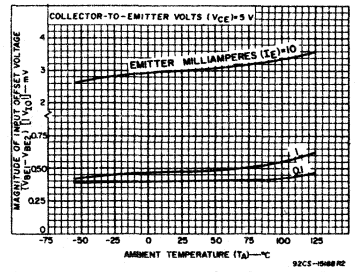


Fig. 10 – V_{IO} vs. T_A for Q1 and Q2.

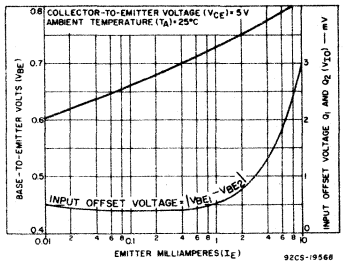


Fig. 11 – V_{BE} and V_{IO} vs. I_E for Q1 and Q2.

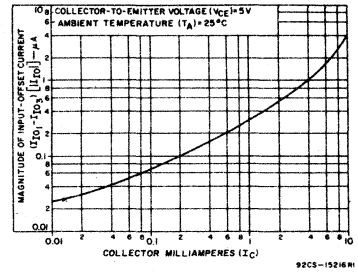


Fig. 12 – I_{IO} vs. I_C (Q1 and Q2) for types CA3146AE and CA3146E.

CA3118, CA3146, CA3183 Types

TYPICAL DYNAMIC CHARACTERISTICS CURVES (FOR ANY TRANSISTOR) – CA3118, CA3146 SERIES

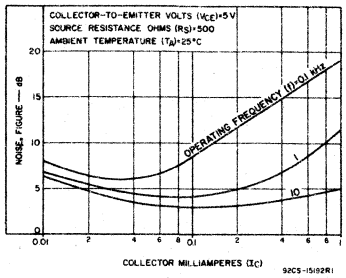


Fig. 13 – NF vs. I_C @ R_S = 500Ω.

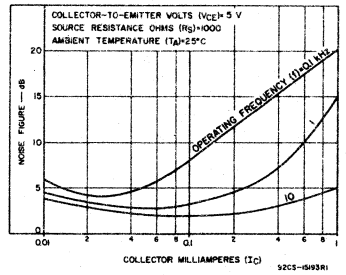


Fig. 14 – NF vs. I_C @ R_S = 1kΩ.

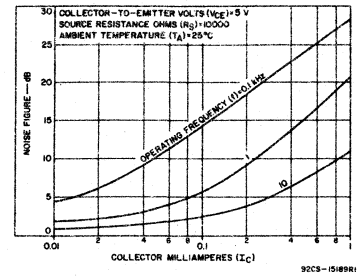


Fig. 15 – NF vs. I_C @ R_S = 10kΩ.

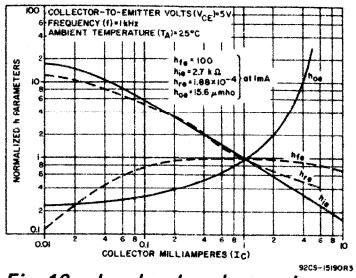


Fig. 16 – h_{fe}, h_{ie}, h_{oe}, h_{re} vs. I_C.

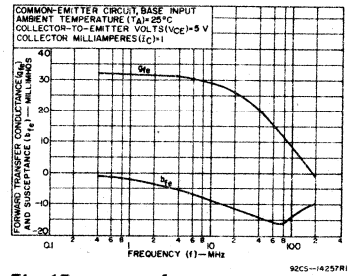


Fig. 17 – y_{fe} vs. f.

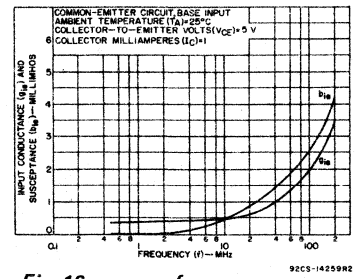


Fig. 18 – y_{ie} vs. f.

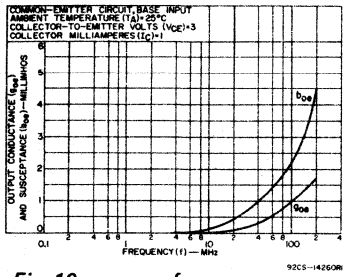


Fig. 19 – y_{oe} vs. f.

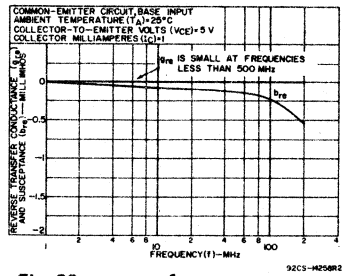


Fig. 20 – y_{re} vs. f.

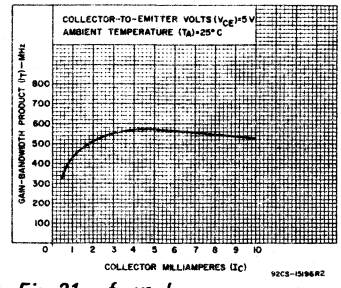


Fig. 21 – f_T vs. I_C.

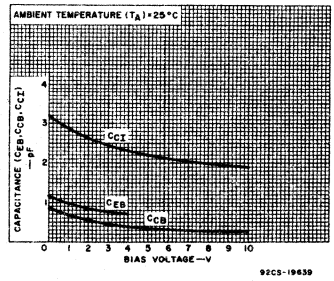


Fig. 22 – C_{EB}, C_{CB}, C_{CI} vs. bias voltage

TYPICAL STATIC CHARACTERISTICS CURVES – CA3183 SERIES

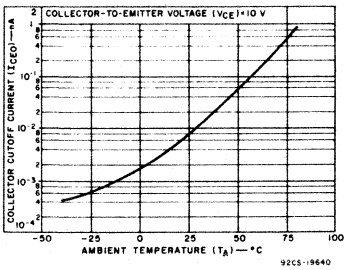


Fig. 23 – I_{CEO} vs. T_A for any transistor.

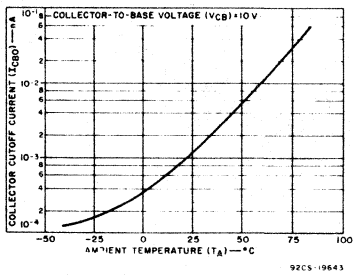


Fig. 24 – I_{CBO} vs. T_A for any transistor.

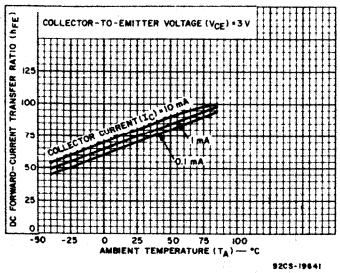


Fig. 25 – h_{FE} vs. T_A for any transistor.

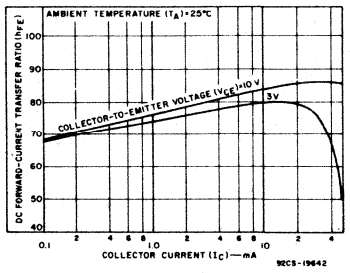


Fig. 26 – h_{FE} vs. I_C for any transistor.

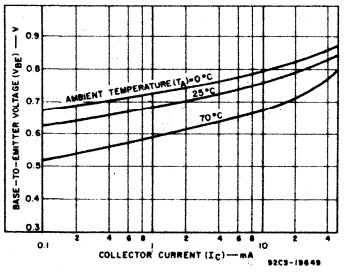


Fig. 27 – V_{BE} vs. I_C for any transistor.

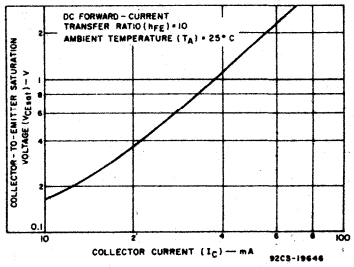


Fig. 28 – $V_{CE\ sat}$ vs. I_C for any transistor.

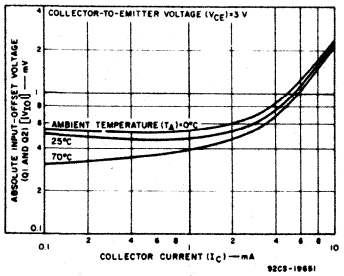


Fig. 29 – $|V_{IO}|$ vs. I_C for differential amplifier (Q1 and Q2).

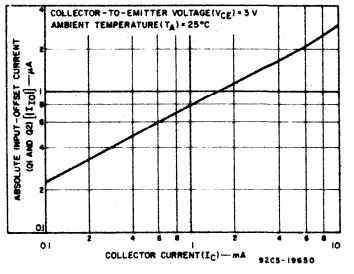
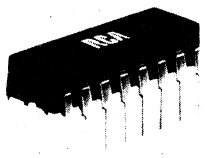


Fig. 30 – $|I_{IO}|$ vs. I_C for differential amplifier (Q1 and Q2).

CA3127E



16-Lead Dual-In-Line Plastic Package H-1622

High-Frequency N-P-N Transistor Array

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- *Gain-bandwidth product (f_T) > 1 GHz*
- *Power gain = 30 dB (typ.) at 100 MHz*
- *Noise figure = 3.5 dB (typ.) at 100 MHz*
- *Five independent transistors on a common substrate*

Applications:

- *VHF amplifiers*
- *Multifunction combinations - RF/mixer/oscillator*
- *Sense amplifiers*
- *Synchronous detectors*
- *VHF mixers*
- *IF converter*
- *IF amplifiers*
- *Synthesizers*
- *Cascade amplifiers*

RCA-CA3127E* consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1 GHz, making the CA3127E useful from dc to 500 MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127E provides close electrical and thermal matching of the five transistors.

The CA3127E is supplied in a 16-lead dual-in-line plastic package and operates over the full military temperature range of −55 to +125° C.

*Formerly RCA Dev. No. TA6206.

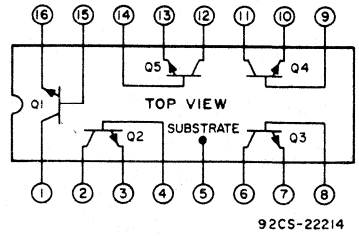


Fig. 1 — Schematic diagram of CA3127E.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

POWER DISSIPATION, P_D:

Any one transistor ..... 85 mW

Total Package:

For T_A up to 75° C ..... 425 mW

For T_A > 75° C Derate Linearly at ..... 6.67 mW/° C

AMBIENT TEMPERATURE RANGE:

Operating ..... −55 to +125° C

Storage ..... −65 to +125° C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265° C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO} ..... 15 V

Collector-to-Base Voltage, V_{CBO} ..... 20 V

Collector-to-Substrate Voltage, V_{CIO}* ..... 20 V

Collector Current, I_C ..... 20 mA

*The collector of each transistor of the CA3127E is isolated from the substrate by an integral diode. The substrate (terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	TEST CONDITIONS		LIMITS			UNITS
			Min.	Typ.	Max.	
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$I_C = 10\,\mu A$, $I_E = 0$		20	32	–	V
Collector-to-Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$		15	24	–	V
Collector-to-Substrate Breakdown Voltage	$I_{C1} = 10\,\mu A$, $I_B = 0$, $I_E = 0$		20	60	–	V
Emitter-to-Base Breakdown Voltage*	$I_E = 10\,\mu A$, $I_C = 0$		4	5.7	–	V
Collector-Cutoff-Current	$V_{CE} = 10$ V, $I_B = 0$		–	–	0.5	μA
Collector-Cutoff-Current	$V_{CB} = 10$ V, $I_E = 0$		–	–	40	nA
DC Forward-Current Transfer Ratio	$V_{CE} = 6$ V	$I_C = 5$ mA	35	88	–	
		$I_C = 1$ mA	40	90	–	
		$I_C = 0.1$ mA	35	85	–	
Base-to-Emitter Voltage	$V_{CE} = 6$ V	$I_C = 5$ mA	0.71	0.81	0.91	V
		$I_C = 1$ mA	0.66	0.76	0.86	
		$I_C = 0.1$ mA	0.60	0.70	0.80	
Collector-to-Emitter Saturation Voltage	$I_C = 10$ mA, $I_B = 1$ mA		–	0.26	0.50	V
Magnitude of Difference in V_{BE}	Q_1 & Q_2 Matched		–	0.5	5	mV
Magnitude of Difference in I_B	$V_{CE} = 6$ V, $I_C = 1$ mA		–	0.2	3	μA

*When used as a zener for reference voltage, the device must not be subjected to more than 0.1 millijoule of energy from any possible capacitance or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10 mA.

DYNAMIC CHARACTERISTICS at $T_A = 25^\circ C$

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
I/F Noise Figure	f = 100 kHz, $R_S = 500\,\Omega$, $I_C = 1$ mA	–	1.8	–	dB
Gain-Bandwidth Product	$V_{CE} = 6$ V, $I_C = 5$ mA	–	1.15	–	GHz
Collector-to-Base Capacitance	$V_{CB} = 6$ V, f = 1 MHz	–	See	–	pF
Collector-to-Substrate Capacitance	$V_{CI} = 6$ V, f = 1 MHz	–	Fig.	–	pF
Emitter-to-Base Capacitance	$V_{BE} = 4$ V, f = 1 MHz	–	5	–	pF
Voltage Gain	$V_{CE} = 6$ V, f = 10 MHz, $R_L = 1\,k\Omega$, $I_C = 1$ mA	–	28	–	dB
Power Gain	Cascode Configuration, f = 100 MHz, $V^+ = 12$ V	27	30	–	dB
Noise Figure	$I_C = 1$ mA	–	3.5	–	dB
Input Resistance	Common-Emitter	–	400	–	Ω
Output Resistance	Configuration	–	4.6	–	$k\Omega$
Input Capacitance	$V_{CE} = 6$ V	–	3.7	–	pF
Output Capacitance	$I_C = 1$ mA	–	2	–	pF
Magnitude of Forward Transadmittance	f = 200 MHz	–	24	–	mmho

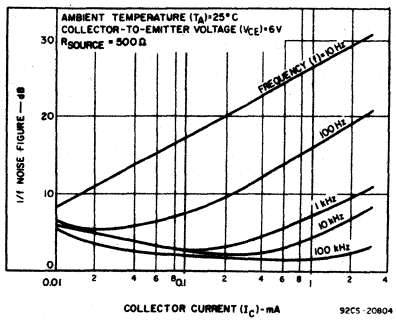


Fig. 2 – 1/f noise figure as a function of collector current at R_{SOURCE} = 500 Ω.

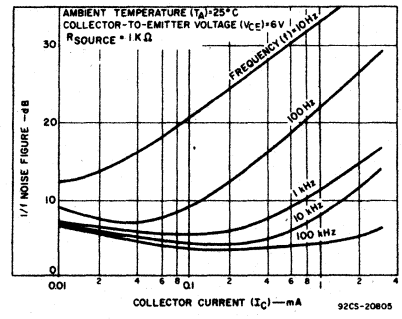


Fig. 3 – 1/f noise figure as a function of collector current at R_{SOURCE} = 1 kΩ.

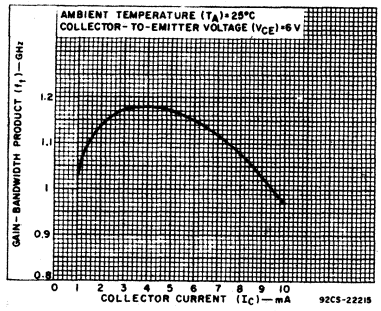


Fig. 4 – Gain-bandwidth product as a function of collector current.

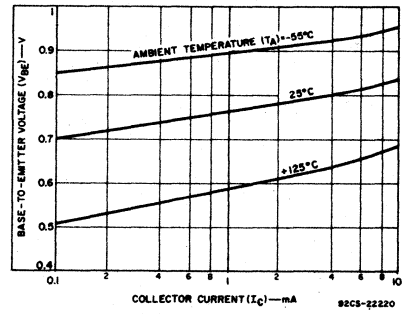


Fig. 5 – Base-to-emitter voltage as a function of collector current.

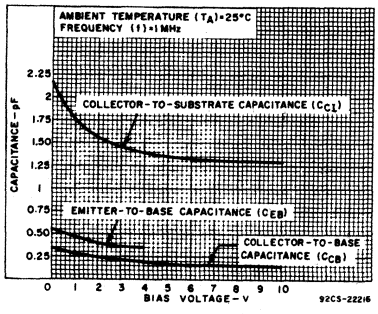


Fig. 6(a) – Capacitance as a function of bias voltage for Q_2.

Transistor	Capacitance (pF)							
	C_{CB}		C_{CE}		C_{EB}		C_{CI}	
	Pkg.	Total	Pkg.	Total	Pkg.	Total	Pkg.	Total
Bias Voltage	–	6 V	–	6 V	–	4 V	–	6 V
Q1	0.025	0.190	0.090	0.125	0.365	0.610	0.475	1.65
Q2	0.015	0.170	0.225	0.265	0.130	0.360	0.065	1.35
Q3	0.040	0.200	0.215	0.240	0.360	0.625	0.210	1.40
Q4	0.040	0.190	0.225	0.270	0.365	0.610	0.085	1.25
Q5	0.010	0.165	0.095	0.115	0.140	0.365	0.090	1.35

Fig. 6(b) – Typical capacitance values at f = 1 MHz. Three terminal measurement. Guard all terminals except those under test.

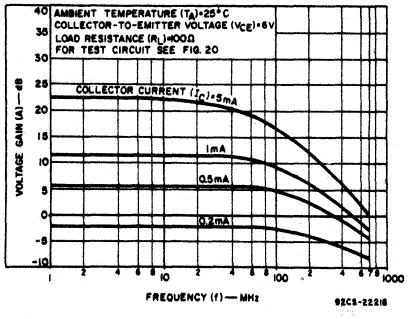


Fig. 7 – Voltage gain as a function of frequency at R_L = 100 Ω.

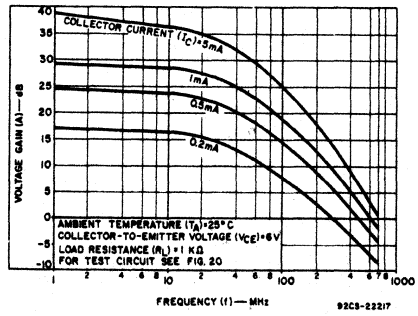


Fig. 8 – Voltage gain as a function of frequency at R_L = 1 kΩ.

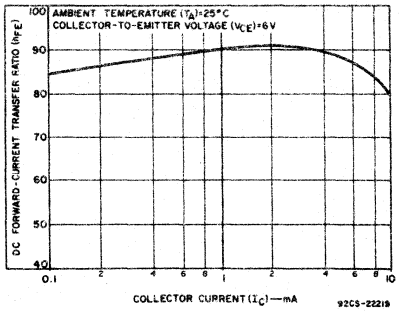


Fig. 9 – DC forward-current transfer ratio as a function of collector current.

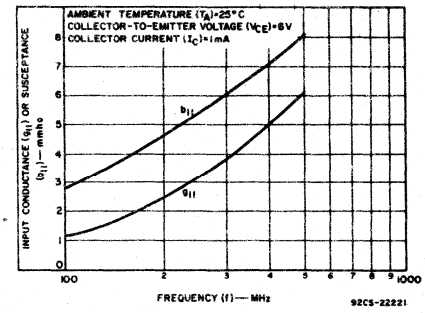


Fig. 10 – Input admittance (Y_{11}) as a function of frequency.

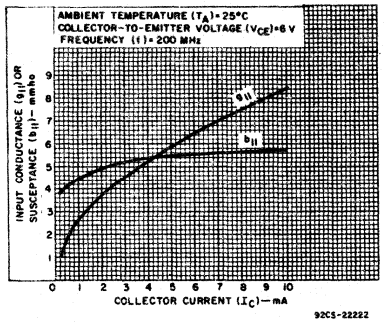


Fig. 11 – Input admittance (Y_{11}) as a function of collector current.

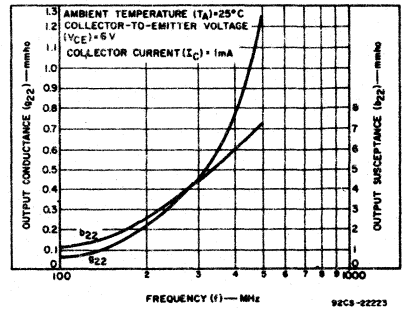


Fig. 12 – Output admittance (Y_{22}) as a function of frequency.

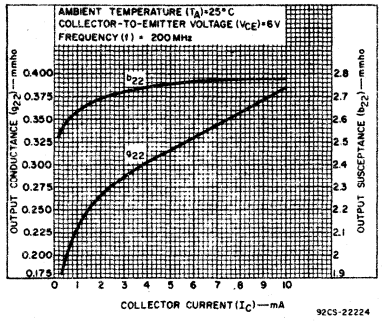


Fig. 13 – Output admittance (Y_{22}) as a function of collector current.

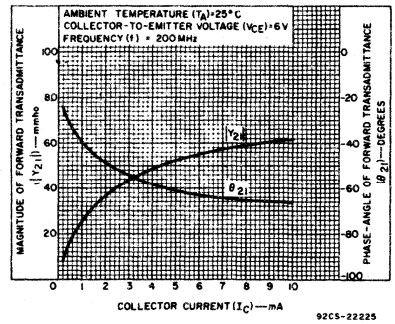


Fig. 14 – Forward transadmittance (Y_{21}) as a function of collector current.

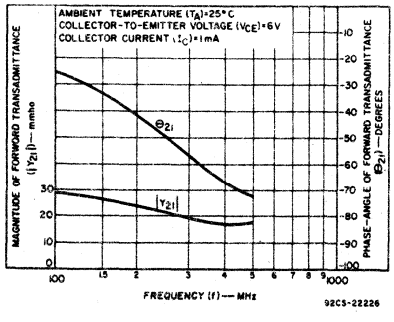


Fig. 15 – Forward transadmittance (Y_{21}) as a function of frequency.

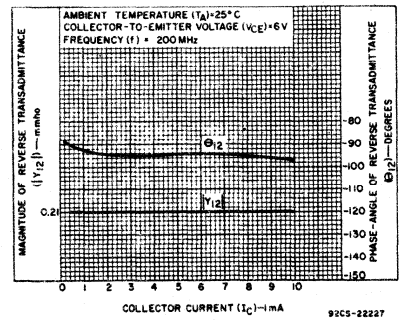


Fig. 16 – Reverse transadmittance (Y_{12}) as a function of collector current.

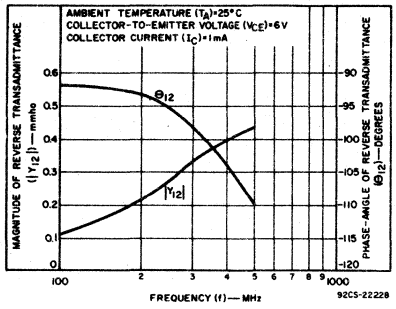


Fig. 17 – Reverse transadmittance (Y_{12}) as a function of frequency.

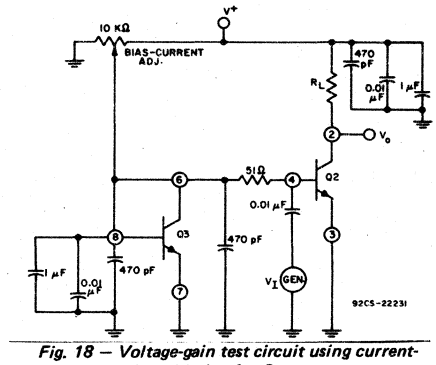
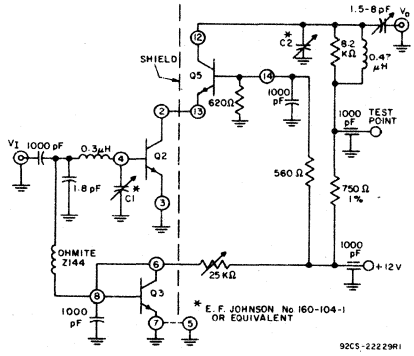


Fig. 18 – Voltage-gain test circuit using current-mirror biasing for Q_2.



This circuit was chosen because it conveniently represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q3 in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.

Fig. 19 – 100-MHz power-gain and noise-figure test circuit.

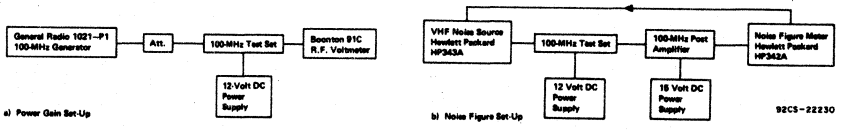
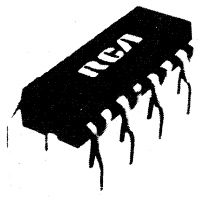


Fig. 20 – Block diagrams of power-gain and noise-figure test set-ups.

CA3128Q

TV Chroma Processor for PAL Systems



16-lead Quad-in-line palstic package

H-1706

Features:

- *Phase-locked subcarrier regeneration utilizes sample-and-hold techniques in the automatic frequency phase control [AFPC] servo loop*
- *Automatic chrominance control [ACC]/killer detector employs sample-and-hold techniques*
- *Supplementary ACC with an overload detector to prevent oversaturation of the picture tube*
- *Sinusoidal subcarrier output*
- *Keyed chroma output*
- *Emitter-follower buffered outputs for low output impedance*
- *Linear dc saturation control*
- *PAL indentification output*
- *Only the initial crystal filter tuning is required . . . no killer and ACC adjustments required at any time*
- *Few external components required*
- *Compensation for temperature and supply variations*
- *All terminals protected against short circuits*

The RCA-CA3128Q is a monolithic silicon integrated circuit designed primarily for PAL chroma processing applications in color TV receivers. For a circuit description of the CA3128Q and an explanation of this device in PAL systems, refer to "A New Chroma Processing IC Using Sample-and-Hold Techniques" by L.A. Harwood (ST6144).

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25°C$*

DC SUPPLY VOLTAGE (Between Terms. 12 and 15) ..... 13.2 V

DC VOLTAGE (Term. 9):

Positive Value ..... +3 V

Negative Value ..... −5 V

DEVICE DISSIPATION:

Up to $T_A = 55°C$ ..... 750 mW

Above $T_A = 55°C$ ..... derate linearly at 7.9 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... −40 to +85 °C

Storage ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At a distance not less than 1/32" (0.79 mm) from case for 10 seconds max. ..... +265°C

TYPICAL STATIC CHARACTERISTICS at T_A = 25°C:

DC Supply Current (I_{12}) with V_{12} = 11.2 V dc ..... 25 mA

TYPICAL DYNAMIC CHARACTERISTICS at T_A = 25°C with a Burst-to-Chroma Ratio of 46.5%:

100% Chroma Output Voltage at $V_{II(p-p)} = 0.5$ V ..... 3.5 V_{p-p}

Oscillator-Level Output Voltage ..... 1 V_{p-p}

Killer Threshold Input Voltage ..... 0.018 V_{p-p}

Pull-in Frequency ..... 500 Hz

PAL Identification Output Voltage ..... 1 V_{p-p}

CA3128Q

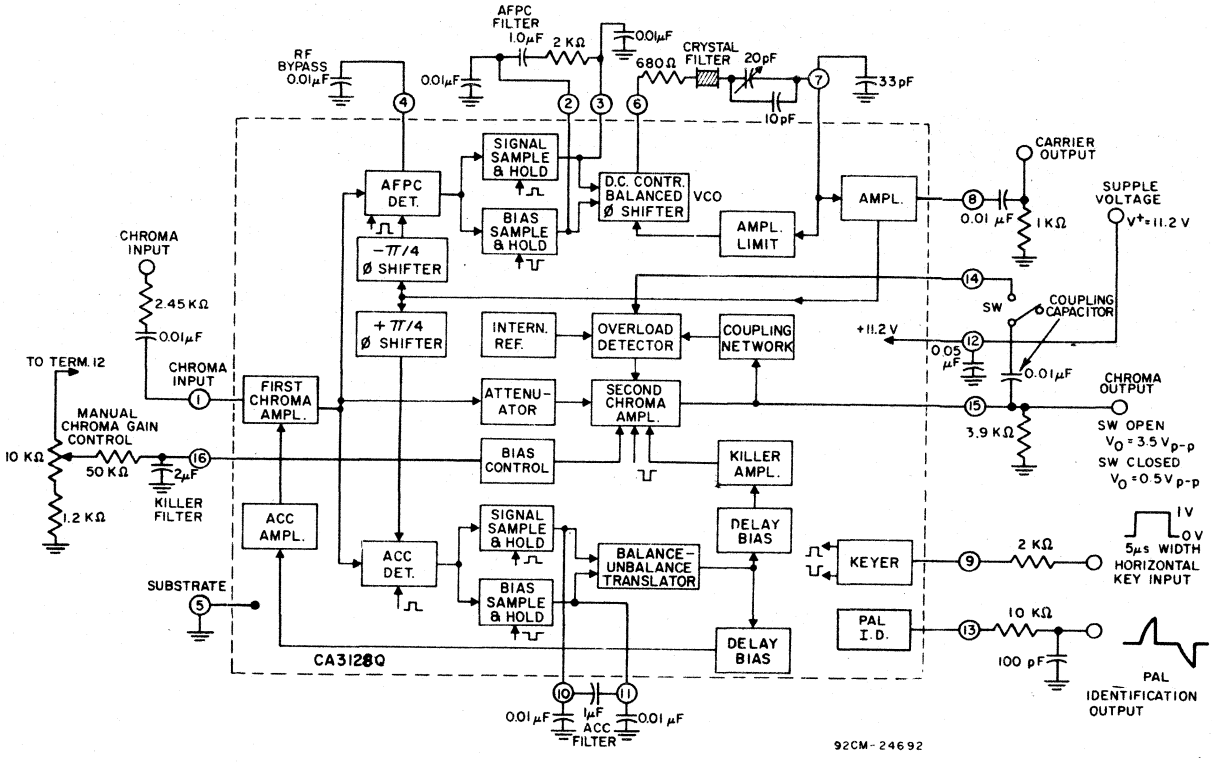
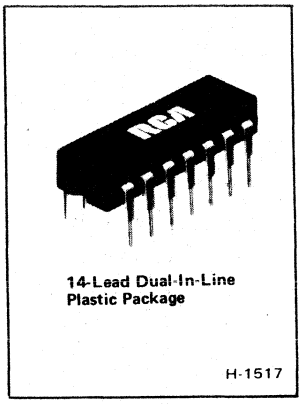


Fig. 1 — Block diagram of CA3128Q TV Chroma Processor.

CA3138E, CA3138AE



14-Lead Dual-In-Line Plastic Package

H-1517

High-Current, High-Beta N-P-N Transistor Arrays

For Industrial, Commercial, and Military Applications

Four Isolated Discrete Sealed-Junction High-Current N-P-N Transistors

Features:

- **High Current –1 A**
- **High Beta – 95 min. at I_C = 500 mA, V_{CE} = 5 V**
- **Low V_{CE}(SAT) –0.4 V max. at I_C = 500 mA, I_B = 12.5 mA**
- **Silicon Nitride Passivated**
- **Platinum Silicide Ohmic Contacts**

The RCA-CA3138 and CA3138A are high-current n-p-n transistor arrays containing four isolated (discrete) sealed-junction high-current n-p-n transistors. They are intended for high-current, high-speed switching and driver applications.

The CA3138A has all the features and characteristics of the CA3138 but is intended for applications requiring premium grade specifications — higher rating for V_{CBO} of 25 volts and limits established for I_{CEO}, I_{EBO}, and h_{FE} at 10 mA.

The CA3138 and CA3138A are supplied in a 14-lead dual-in-line plastic package and operate over the full military temperature range of –55°C to +125°C.

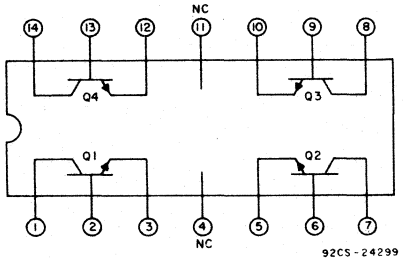


Fig. 1 – Terminal diagram (top view).

Applications:

- **High-Current LED Driver**
- **Relay and Solenoid Driver**
- **Lamp Driver**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE ..... With Base Open (V_{CEO})	15	V
COLLECTOR-TO-BASE VOLTAGE With Emitter Open (V_{CBO})		
CA3138	20	V
CA3138A	25	V
EMITTER-TO-BASE VOLTAGE ..... With Collector Open (V_{EBO})	5	V
COLLECTOR CURRENT (I_C)	1	A
POWER DISSIPATION (P_D):		
At T_A up to 25°C:		
For Each Transistor	1	W
Total Package	2	W
At T_A above 25°C derate linearly	20	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	–55 to +125	°C
Storage	–65 to +150	°C
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

CA3138E, CA3138AE

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Characteristic		Test Conditions	LIMITS						Units
			CA3138			CA3138A			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector-to-Emitter Sustaining Voltage, $V_{CEO}(sus)$*		I_C = 1 mA, I_B = 0	15	20	–	15	20	–	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$		I_C = 10 μA	20	55	–	25	60	–	V
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$		I_C = 10 μA, I_E = 0	20	55	–	25	60	–	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$		I_E = 10 μA, I_C = 0	5	7.2	–	5	7.2	–	V
Base-to-Emitter Saturation Voltage, $V_{BE}(sat)$*		I_C = 500 mA, I_B = 12.5 mA	0.7	0.81	1.1	0.7	0.81	1.1	V
Collector-to-Emitter Saturation Voltage, $V_{CE}(sat)$*		I_C=500 mA, I_B = 12.5 mA	–	0.26	0.4	–	0.26	0.4	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 15 V	–	0.03	1	–	0.02	0.1	μA
	I_{CEO}	V_{CE} = 10 V	–	0.5	–	–	0.3	1.0	
	I_{EBO}	V_{EB} = 4 V	–	0.01	–	–	0.01	0.1	
Static Forward-Current Transfer Ratio (Beta), h_{FE}*		I_C=10 mA, V_{CE} = 5 V	–	–	–	35	140	–	
		I_C = 100 mA, V_{CE} = 5 V	80	160	450	80	160	450	
		I_C = 500 mA, V_{CE} = 5 V	95	170	500	95	170	500	
		I_C = 1 A, V_{CE} = 5 V	40	170	–	40	170	–	
Small-Signal Forward Current Transfer Ratio, h_{fe}		I_C = 50 mA, V_{CE} = 10 V, f = 100 MHz	2	–	–	2	–	–	
Collector-to-Base Capacitance, C_{CB}		V_{CB} = 10 V, I_E = 0	–	18	–	–	18	–	pF
Emitter-to-Base Capacitance, C_{EB}		V_{EB} = 0.5 V, I_C = 0	–	77	–	–	77	–	pF
Rise Time (See Test Ckt. Fig. 6), t_r		I_C = 570 mA	–	6	–	–	6	–	ns
Fall Time (See Test Ckt. Fig. 6), t_f		I_{B1} = 30 mA	–	100	–	–	100	–	ns
Delay Time (See Test Ckt. Fig. 6), t_d		I_{B2} = 0	–	7.5	–	–	7.5	–	ns
Storage Time (See Test Ckt. Fig. 6), t_s			–	850	–	–	850	–	ns

*Pulse Conditions: width = 300 μs; duty cycle = 1%.

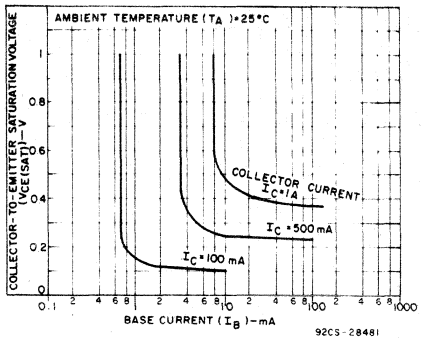


Fig. 2 – $V_{CE(sat)}$ vs I_B

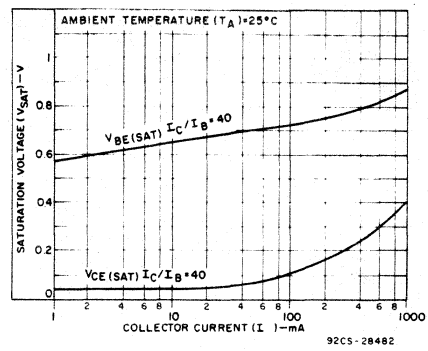


Fig. 3 – V_{sat} vs I_C

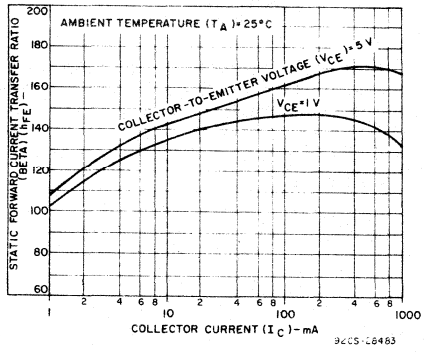


Fig. 4 – h_{FE} vs I_C

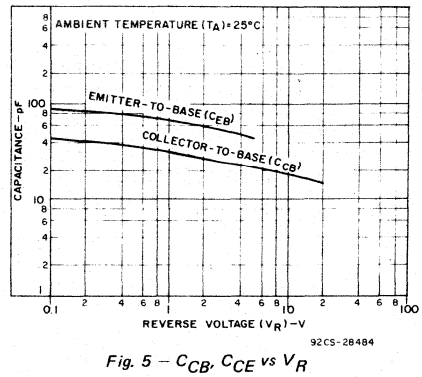


Fig. 5 – C_{CB}, C_{CE} vs V_R

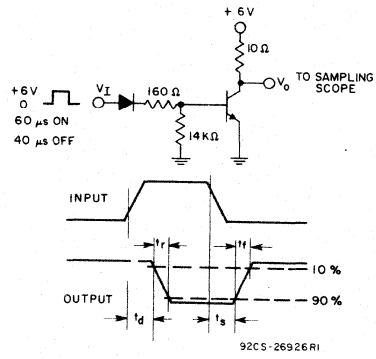
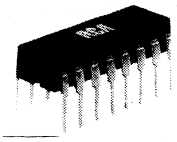


Fig. 6 – Switching time test circuit and waveforms.

CA3227E, CA3246E

CA3227E



H-1622

16-Lead Dual-In-Line Plastic Package

CA3246E

H-1517

14-Lead Dual-In-Line Plastic Package

High-Frequency N-P-N Transistor Arrays

For Low-Power Applications at Frequencies up to 1.5 GHz

Features:

- *Gain-bandwidth product (f_T) > 3 GHz*
- *Five transistors on a common substrate*

Applications:

- *VHF amplifiers*
- *VHF mixers*
- *Multifunction combinations - RF/mixer/oscillator*
- *IF converter*
- *IF amplifiers*
- *Sense amplifiers*
- *Synchronous detectors*
- *Synthesizers*
- *Cascade amplifiers*

The RCA-CA3227E and CA3246E* consist of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the transistors exhibits a value of f_T in excess of 3 GHz, making them useful from dc to 1.5 GHz. The monolithic construction of these devices provides close electrical and thermal matching of the five transistors.

The CA3227E is supplied in a 16-lead dual-in-line plastic package and the CA3246E is supplied in a 14-lead dual-in-line plastic package.

*Formerly RCA Developmental Nos. TA10854 and TA10855, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25°C:*

POWER DISSIPATION, P_D:

Any one transistor	85 mW
Total Package:	
For T_A up to 75°C	425 mW
For T_A > 75°C Derate Linearly at	6.67 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating	−55 to +125°C
Storage	−65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

The following ratings apply for each transistor in the device.

Collector-to-Emitter Voltage, V_{CEO}	8 V
Collector-to-Base Voltage, V_{CBO}	12 V
Collector-to-Substrate Voltage, V_{CIO}§	20 V
Collector Current, I_C	20 mA

§The collector of each transistor of these devices is isolated from the substrate by an integral diode. The substrate (terminal 5/CA3227E and terminal 13/CA3246E) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

STATIC ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10 μA, I_E=0	12	20	—	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1 mA, I_B=0	8	10	—	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{C1}=10 μA, I_B=0, I_E=0	20	—	—	V
Emitter-Cutoff-Current*	I_{EBO}	V_{EB}=4.5 V, I_C=0	—	—	10	μA
Collector-Cutoff-Current	I_{CEO}	V_{CE}=5 V, I_B=0	—	—	1	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB}=8 V, I_E=0	—	—	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=6 V, I_C=10 mA	—	110	—	
		V_{CE}=6 V, I_C=1 mA	40	150	—	
		V_{CE}=6 V, I_C=0.1 mA	—	150	—	
Base-to-Emitter Voltage	V_{BE}	V_{CE}=6 V, I_C=1 mA	0.62	0.71	0.82	V
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C=10 mA, I_B=1 mA	—	0.13	0.50	V
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	I_C=10 mA, I_B=1 mA	0.74	—	0.94	V

*On small-geometry, high-frequency transistors, it is very good practice never to take the Emitter Base Junction into reverse breakdown. To do so may permanently degrade the h_{FE}. Hence, the use of I_{EBO} rather than $V_{(BR)EBO}$. These devices are also susceptible to damage by electrostatic discharge and transients in the circuits in which they are used. Moreover, CMOS handling procedures should be employed.

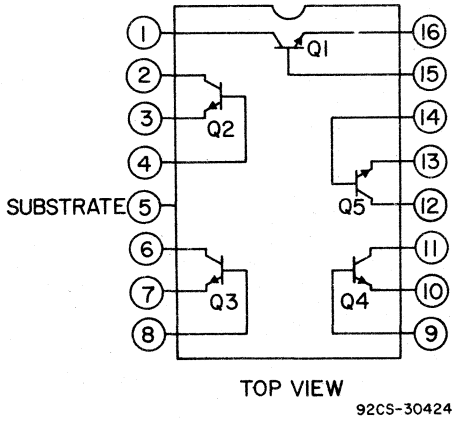


Fig. 1 - Schematic diagram of CA3227E.

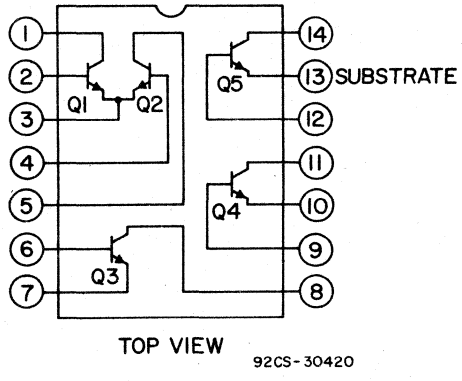


Fig. 2 - Schematic diagram of CA3246E.

CA3227E, CA3246E

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, 200 MHz, Common Emitter
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each Transistor			
Input Admittance, Y_{11} b_{11}	I_C=1 mA, V_{CE}=5 V	4	mmho
g_{11}		0.75	
Output Admittance, Y_{22} b_{22}		2.7	mmho
g_{22}		0.13	
Forward Transfer Admittance, Y_{21} Y_{21}		29.3	mmho
θ_{21}		−33	degrees
Reverse Transfer Admittance, Y_{12} Y_{12}		0.38	mmho
θ_{12}		−97	degrees
Input Admittance, Y_{11} b_{11}	I_C=10 mA, V_{CE}=5 V	4.8	mmho
g_{11}		2.85	
Output Admittance, Y_{22} b_{22}		2.75	
g_{22}		0.9	
Forward Transfer Admittance, Y_{21} Y_{21}		95	mmho
θ_{21}		−62	degrees
Reverse Transfer Admittance, Y_{12} Y_{12}		0.39	mmho
θ_{12}		−97	degrees
Small-Signal Forward Current Transfer Ratio h_{21}	I_C=1 mA, V_{CE}=5 V	7.1	
	I_C=10 mA, V_{CE}=5 V	17	
Typical Capacities @ 1 MHz, Three-Terminal Measurement			
Collector-to-Base Capacitance, C_{CB}	V_{CB}=6 V	0.3	pF
Collector-to-Substrate Capacitance, C_{CI}	V_{CI}=6 V	1.6	pF
Collector-to-Emitter Capacitance, C_{CE}	V_{CE}=6 V	0.4	pF
Emitter-to-Base Capacitance, C_{EB}	V_{EB}=3 V	0.75	pF

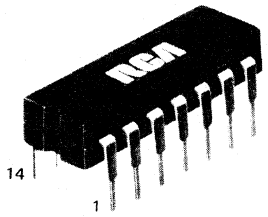
OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. **Operating**

   Operating Voltage

   During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{CC}—V_{EE} to exceed the absolute maximum rating.



14-Lead dual-in-line plastic package

H-1517

COS/MOS Transistor Array

For Linear Circuit Applications

Applications:

- High input impedance, general-purpose amplifiers
- Pre-amplifiers
- Differential amplifiers
- Op-amps and comparators
- Constant-current sources and current mirrors
- Micropower amplifiers and oscillators
- Control of lamps, LED's, relays, and thyristors
- Timers
- Choppers
- Mixers

RCA-CA3600E is an array of COmplementary-Symmetry MOS Field-Effect Transistors* on a monolithic silicon substrate. It is comprised of three n-channel and three p-channel enhancement-type MOS transistors arrayed as shown in Fig. 1, and specified and tested for linear circuit operation. These transistors are uniquely suitable for service in complementary-symmetry circuits at supply voltages in the range of 3 to 15 volts and are useful at frequencies up to 5 MHz (untuned). Each transistor in the CA3600E can conduct currents up to 10 mA. This device is supplied in the 14-lead dual-in-line plastic package.

Formerly RCA Dev. No. TA6368.

* The theory and construction of COS/MOS transistors are described in the "RCA COS/MOS Integrated Circuits Manual," RCA Solid State Division Technical Series Publication No. CMS-271.

Features:

- High input resistance . . . . . 100 GΩ (typ.)
- Low gate-terminal current . . . . 10 pA (typ.)
- Matched p-channel pair:
  Gate-voltage differential (I_D =-100 μA) ±20 mV (max.)
- No "Popcorn" (burst) noise
- Stable transfer characteristics over an operating temperature range of −55°C to +125°C when operated in complementary circuit configuration at supply voltages in the 5 to 15 volt range (see Fig. 14)
- Integrated integral gate-protection system (see Fig. 34)
- High voltage gain (see Fig. 11). . . up to 53 dB (typ.) per COS/MOS stage
- Individual MOS transistors have square-law characteristics, superior cross-modulation performance, and greater dynamic range than bipolar transistors

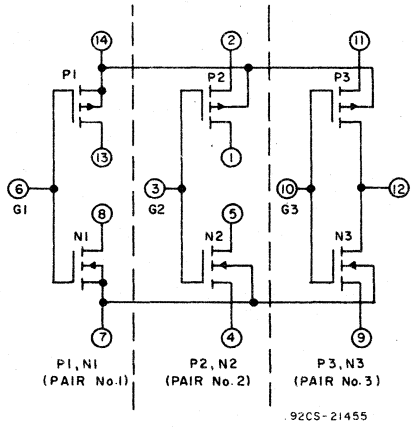


Fig.1 — Schematic diagram for CA3600E COS/MOS transistor array. (See Fig.34 for internal gate-and-channel-protection circuits)

1. Drain terminal, p-channel of pair no. 2
2. Source terminal, p-channel of pair no. 2
3. Common gate terminal of pair no. 2
4. Source terminal, n-channel of pair no. 2
5. Drain terminal, n-channel of pair no. 2
6. Common gate terminal of pair no. 1
7. Source terminal, n-channel of pair no. 1 and substrate connection for all n-channel transistors - - - V_{SS} terminal
8. Drain terminal, n-channel of pair no. 1
9. Source terminal, n-channel of pair no. 3
10. Common gate terminal of pair no. 3
11. Source terminal, p-channel of pair no. 3
12. Common drain terminal of pair no. 3
13. Drain terminal, p-channel of pair no. 1
14. Source terminal, p-channel of pair no. 1 and substrate connection for all p-channel transistors - - - V_{DD} terminal

Terminal Identification for Fig. 1.

CA3600E

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DISSIPATION:

Any one transistor at T_A up to 55°C	150 mW
Total package at T_A up to 55°C	750 mW
Above T_A = 55°C	derate linearly 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating	−55 to +125°C
Storage	−65 to +150°C

LEAD TEMPERATURE (During Soldering)

At distance not less than 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	265°C

The Following Ratings Apply for Each Transistor in the Device:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}:

n-channel	+15 V
p-channel	−15 V

DRAIN-TO-GATE VOLTAGE, V_{DG}:

n-channel	+15 V
p-channel	−15 V

SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}:

n-channel	+15 V
p-channel	−15 V

GATE-TO-SOURCE VOLTAGE, V_{GS}:

p-channel transistors (p_1, p_2, p_3)	0 V(min.),$-V_D$(max.)
n-channel transistors (n_1, n_2, n_3)	0 V(min.),$+V_D$(max.)
COS/MOS transistor-pairs (p_1-n_1, p_2-n_2, p_3-n_3)	0 V(min.),$+V_{DD}$(max.)

DRAIN CURRENT, $\|I_D\|$	10 mA
GATE CURRENT, $\|I_G\|$	100 μA

The Following Rating Applies for Each COS/MOS Transistor-Pair in the Device:

DC SUPPLY VOLTAGE ($V_{DD} - V_{SS}$)	+15 V

Rules for Maintaining Electrical Isolation Between Transistors and Monolithic Substrate

Terminal No. 14 must be maintained at the most positive potential (or equally positive potential) with respect to any other terminal in the CA3600E.

Terminal No. 7 must be maintained at the most negative potential (or equally negative potential) with respect to any other terminal in the CA3600E.

Violation of these rules will result in improper transistor operation, circuit "latching," and/or possible permanent damage to the CA3600E.

Note: Users should observe the "Considerations in Handling CA3600E Devices", discussed on page 13.

ELECTRICAL CHARACTERISTICS, *At T_A = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	TYPICAL CURVE OR CIRCUIT FIG. NO.	LIMITS			UNIT
				Min.	Typ.	Max.	
For Each p-Channel MOS Transistor							
Drain Current	I_D	V_{DS}=−10 V,V_{GS}=−3.6 V	2,3,4	−0.5	−1.1	−2.0	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	I_D=−10 μA	–	–	−1.75	–	V
Gate-to-Source Voltage Differential (p_1 vs. p_2)	$\lvert V_{GS1}-V_{GS2}\rvert$	I_D=−100 μA,V_{DS}=−10 V	5	–	±4	±20	mV
Forward Transconductance	g_{fs}	I_D=−1 mA,f=1 kHz	6	–	920	–	μmho
Low-Frequency Noise Voltage	e_N	I_D=−1 mA,f=1 kHz,R_s=0 Ω	7	–	0.03	–	μV $\sqrt{Hz}$
Low-Frequency Noise Current	i_N	I_D=−1 mA,f=1 kHz,R_s=1 MΩ	7	–	0.2	–	pA $\sqrt{Hz}$
Current-Mirror Transfer Ratio (p_1/p_2)	I_{MTR}	I_1=−100 μA,V_{DS}=−10 V	30	0.7	1.1	1.5	–
Gate-Terminal Current	I_{GT}	V_{DS}=−10 V,V_{GS}=−3.5 V	–	–	±0.015	−40	nA
Input Capacitance	C_I	–	–	–	6.3	–	pF
Output Capacitance	C_O	–	–	–	3	–	pF
Input-to-Output Capacitance	C_{I-O}	–	–	–	0.75	–	pF
For Each n-Channel MOS Transistor							
Drain Current	I_D	V_{DS}=+10 V,V_{GS}=+3.6 V	2,3,4	0.4	0.9	1.6	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	I_D=10 μA	–	–	1.5	–	V
Gate-to-Source Voltage Differential (n_1 vs n_2)	$\lvert V_{GS1}-V_{GS2}\rvert$	I_D=100 μA,V_{DS}=+10 V	5	–	±30	–	mV
Forward Transconductance	g_{fs}	I_D=1 mA,f=1 kHz	6	–	860	–	μmho
Low-Frequency Noise Voltage	e_N	I_D=1 mA,f=1 kHz,R_s=0 Ω	7	–	0.2	–	μV $\sqrt{Hz}$
Low-Frequency Noise Current	i_N	I_D=1 mA,f=1 kHz,R_s=1 MΩ	7	–	0.3	–	pA $\sqrt{Hz}$
Current-Mirror Transfer Ratio (n_1/n_2)	I_{MTR}	I_1=100 μA,V_{DS}=+10 V	29	0.7	1.3	2.0	–
Gate-Terminal Current	I_{GT}	V_{DS}=+10 V,V_{GS}=+3.7 V	–	–	±0.01	+40	nA
Input Capacitance	C_I	–	–	–	5.5	–	pF
Output Capacitance	C_O	–	–	–	2.0	–	pF
Input-to-Output Capacitance	C_{I-O}	–	–	–	0.35	–	pF
For Each COS/MOS Transistor Pair							
Drain Current	I_{DD}	V_{DD}=+10 V	9,10	1.0	2.2	4.0	mA
Drain-to-Source Cutoff Current	$I_{DD(off)}$	V_{DD}=+10 V,V_{SS}=0 V Gate Voltage(V_G)=+10 V or 0 V	8	–	0.5	100	nA
DC Output Voltage	V_O	V_{DD}=+10 V	10	4.2	5.0	5.8	V
Forward Transconductance	g_{fs}	V_{DD}=+10 V, f = 1 kHz	6	–	2300	–	μmho
Slew Rate (Open-Loop)	SR	V_{DD}=+15 V	10	–	95	–	V/μs
Amplifier Voltage Gain	A_{OL}	V_{DD}=+10 V,f=1 kHz,R_b=22 MΩ R_s=50 Ω	10,11	–	32	–	dB
Gate-Terminal Current	I_{GT}	V_{DD}=+10 V	10	–	±0.005	±20	nA
Broadband Output Noise Voltage	E_{ON}	V_{DD}=+10 V,R_b=22 MΩ,R_s=10 kΩ	10,11	–	500		μV
Input Capacitance	C_I	–	–	–	11.8		pF
Output Capacitance	C_O	–	–	–	5.0		pF
Input-to-Output Capacitance	C_{I-O}	–	–	–	1.1		pF

TYPICAL CHARACTERISTICS CURVES

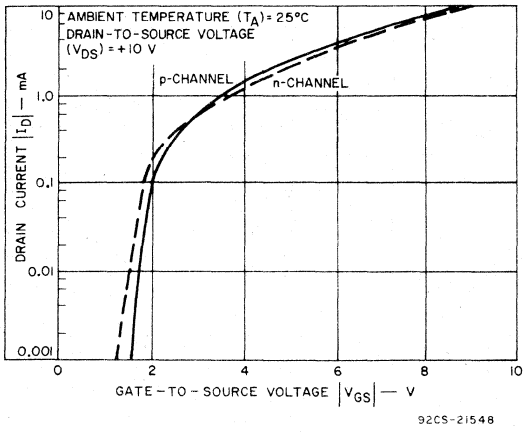


Fig. 2—Drain current vs. gate-to-source voltage.

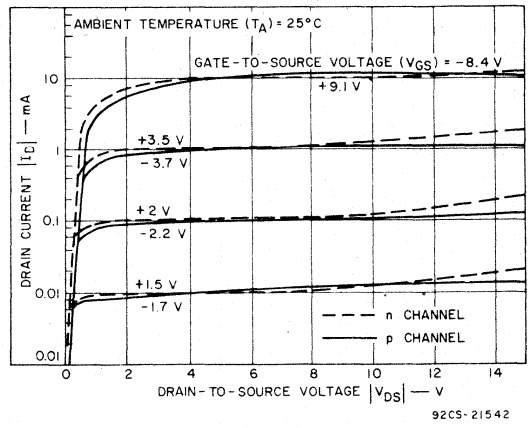


Fig. 3— Drain current vs. drain-to-source voltage.

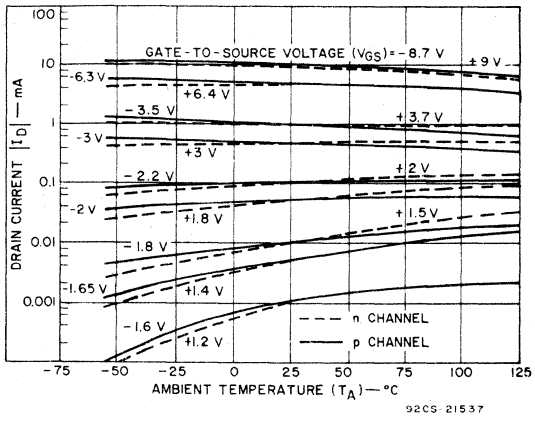


Fig. 4— Drain current vs. ambient temperature.

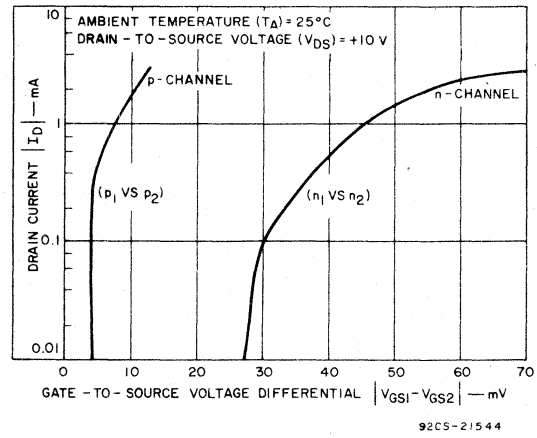


Fig. 5— Gate-to-source voltage differential vs. drain current.

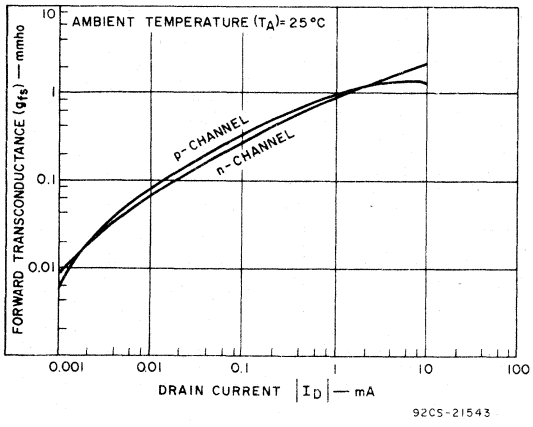


Fig. 6— Forward transconductance vs. drain current.

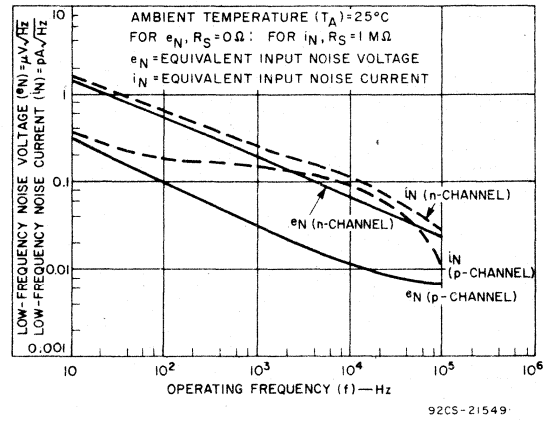


Fig. 7— Noise voltage and noise current vs. operating frequency.

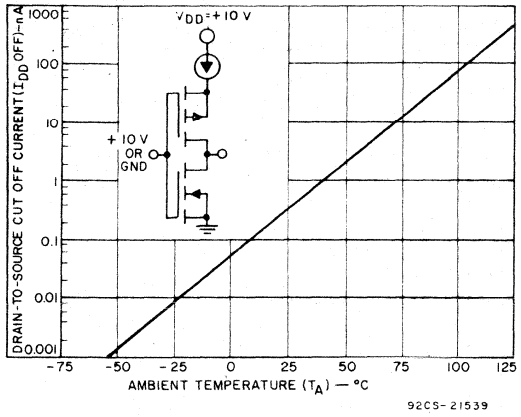


Fig. 8— Drain-to-source cutoff current vs. ambient temperature.

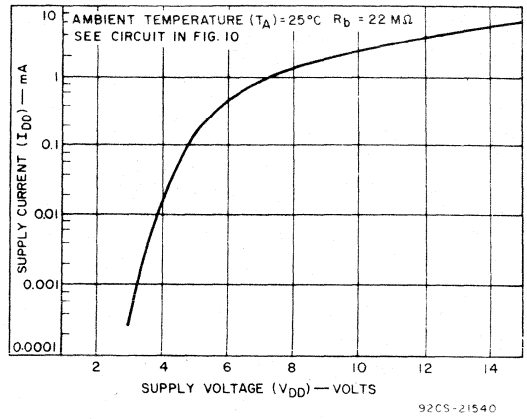


Fig.9 – Typical V_{DD} vs. I_{DD} characteristics for amplifier circuits of Fig.10 and Fig.15.

APPLICATIONS

The Basic COS/MOS Linear Amplifier

P-n-p and n-p-n bipolar transistors have been used for many years in the design of so-called "true-complementary" linear amplifier circuits[1]. Since mutually compatible p-channel and n-channel MOS/FET devices were not generally available, "true-complementary" amplifier circuits using MOS transistors were seldom used. Now, COS/MOS transistor technology[5] has made it possible to supply compatible p-channel/n-channel transistors in monolithic IC form such as the CA3600E COS/MOS transistor array shown in Fig. 1.

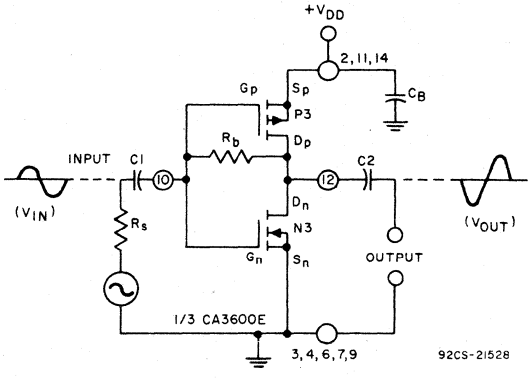


Fig. 10– COS/MOS transistor-pair biased for linear-mode operation.

A "True-Complementary" Linear Amplifier Using COS/MOS Transistors

Fig. 10 shows the schematic diagram of a single-stage "true-complementary" linear amplifier using one pair of the complementary MOS transistors in the CA3600E, connected in a common-source circuit. Resistor R_b is used to bias the complementary pair for Class A operation, as described subsequently, and R_s represents the source resistance of the signal source. This generic amplifier is suitable for operation with a single or split voltage supply in the range of 3 to 15 volts. Fig. 11 shows voltage gain as a function of operating frequency at various supply voltages for the single-stage amplifier. This amplifier is capable of producing very high output-swing voltages (V_{out}); for example, its output voltages can be swung to within several millivolts of either supply-voltage "rail". Fig. 9 shows typical supply voltage (V_{DD}) vs. supply current (I_{DD}) characteristics for the single-stage amplifier. The curves in Fig. 12 show the normalized amplifier supply current as a function of ambient temperature at various supply voltages. When the amplifier is operating at V_{DD} = 3 V, the supply current changes rapidly as a function of temperature because the MOS transistors are operating in the proximity of their individual gate-source threshold voltages.

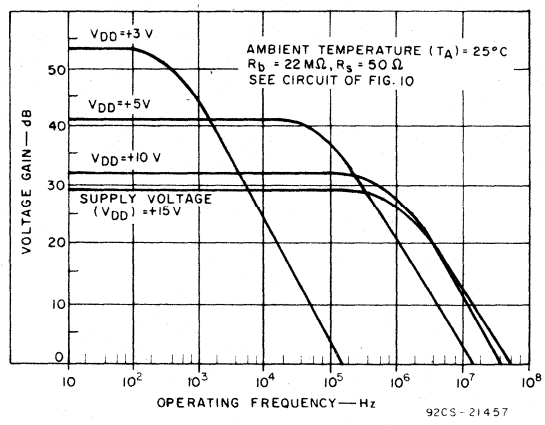


Fig. 11– Typical voltage gain vs. frequency characteristics for amplifier circuit of Fig. 10.

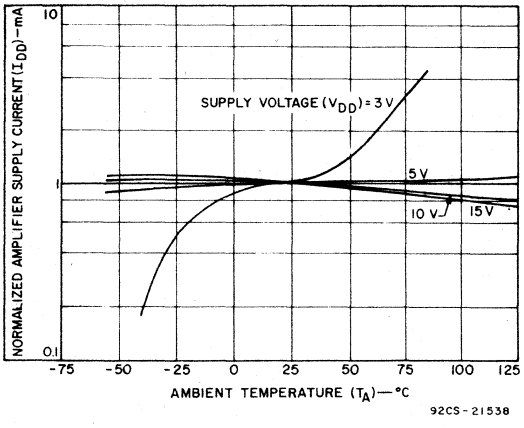


Fig. 12– Normalized amplifier supply current vs. ambient temperature characteristics for amplifier circuit of Fig. 10.

Voltage-Transfer Characteristics

Fig. 13 illustrates a voltage-transfer characteristic curve of a COS/MOS transistor pair connected in the amplifier circuit of Fig. 10, with a biasing resistor (R_b) connected between the drain and gate terminals (10,12). If the p- and n-channel transistors have identical characteristics, their channel resistances are equal, and the biasing method shown establishes a steady-state condition such that terminal 12 is at mid-potential between V_{DD} and ground. Thus, with negligibly small gate-source leakage resistances, under zero-signal conditions, the biasing resistor (R_b) establishes gate potential at the mid-point between V_{DD} and ground, i.e., $V_{in} = V_{out}$. Under these conditions the amplifier is biased for operation about the mid-point ("0") in the linear segment on the steep transition of the voltage-transfer characteristic as shown in Fig. 13. When the input signal (V_{in}) swings in the positive direction, there is a reduction in the instantaneous output voltage (V_{out}) with respect to ground. Negative-going input signals have inverse effects. Thus, phase-inversion occurs in the COS/MOS-pair amplifier. Power-supply current is constant during dynamic linear operation, i.e., Class A amplifier service. When the signal input-voltage level (V_{in}) becomes very large, the output signal (V_{out}) waveforms become distorted because the transistors are driven into the non-linear portions of their voltage-transfer characteristics. If the positive-going input-signal is sufficiently large, for example, the p-channel transistor can be driven to cutoff and the amplifier supply current (I_{DD}) is reduced to essentially zero.

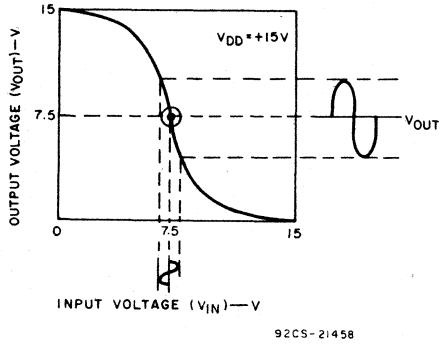


Fig. 13 – Representation of voltage-transfer characteristics for COS/MOS transistor pair.

Fig. 14 shows typical voltage-transfer characteristics of each COS/MOS pair in the CA3600E at several values of V_{DD}. The shape of these transfer characteristics is comparatively constant despite temperature changes from –55 to +125°C.

The biasing arrangement used in the circuit of Fig. 10 provides an easy method of establishing feedback for ac signals in accordance with the R_b/R_s ratio. When the feedback of ac signals is not desirable, the circuit of Fig. 15 may be used. The ac bypass capacitor (C_3) minimizes ac signal feedback.

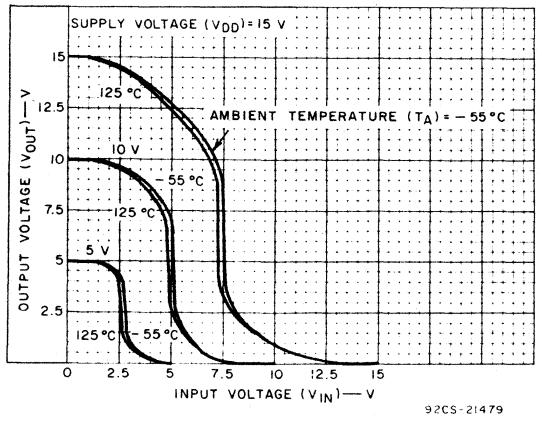


Fig. 14– Voltage transfer characteristics for COS/MOS transistor-pair amplifier in Fig. 10.

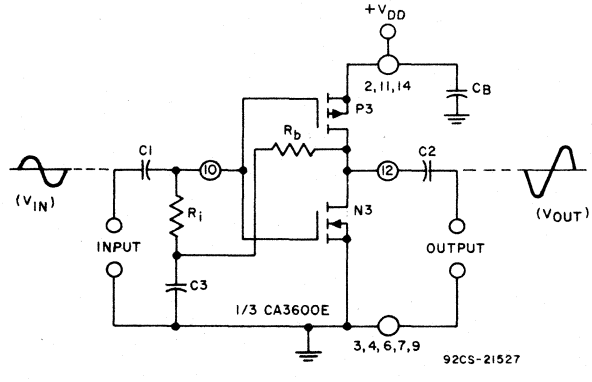


Fig. 15– Alternate method of biasing COS/MOS transistor-pair for linear-mode operation.

Cascading Amplifier Stages of COS/MOS Transistor Pairs

Ultra-high-gain amplifiers can be designed by cascading stages of COS/MOS transistor pairs as shown in Fig. 16. The biasing system used is similar to that described above in connection with Fig. 10. The supply current for the three-stage amplifier shown in Fig. 16 is typically three times the values shown in Fig. 9. Gain and frequency-response characteristics of the amplifier are shown in Fig. 17.

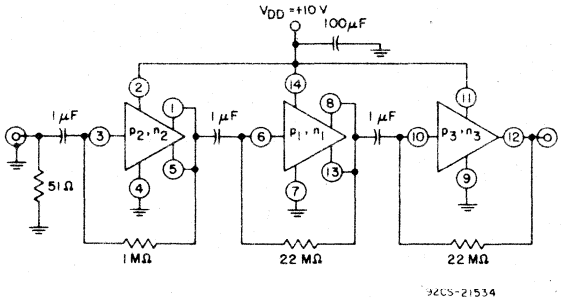


Fig. 16– High-gain amplifier uses cascaded COS/MOS transistor-pair in CA3600E.

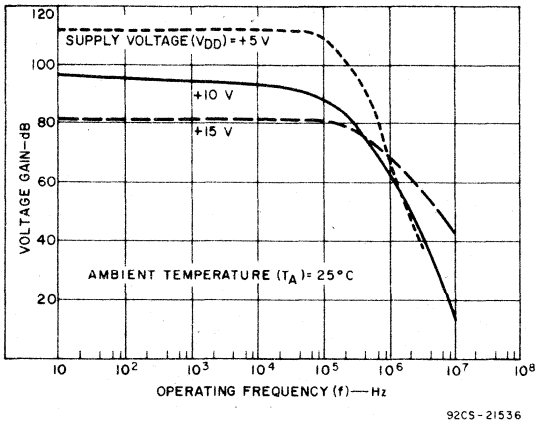


Fig. 17– Typical voltage gain vs. operating frequency characteristics for three-stage COS/MOS transistor-pair amplifier in Fig. 16.

Post-Amplifiers For Op-Amps

COS/MOS transistor-pairs can be advantageously applied as post-amplifiers for op-amps. Because the input impedance of the COS/MOS pair is comparatively high, the op-amp operates under essentially unloaded conditions. Each COS/MOS pair can sink and source output current up to about 10 mA. Additionally, the op-amp output can be directly coupled to bias the COS/MOS pair. A detailed description of the subject has been published previously.[2]

The schematic diagram in Fig. 18 shows a COS/MOS transistor-pair serving as a post-amplifier to an RCA-CA3080 Operational Transconductance Amplifier.[3] The approximate 30-dB gain in a single COS/MOS transistor-pair is an added increment to the 100-dB gain in the CA3080, yielding a total forward gain of about 130 dB. The open-loop slew rate of the circuit in Fig. 19 is approximately 65 V/μs. When compensated for the unity-gain voltage-follower mode shown in Fig. 19, the slew rate is about 1 V/μs. For greater current output, the two remaining transistor pairs of the CA3600E may be connected in parallel with the single stages shown in Figs. 18 and 19.

The use of the two-stage COS/MOS post-amplifier shown in Fig. 20 increases the total open-loop gain of the system to about 160 dB (100,000,000X). Open-loop slew rate remains at about 65 V/μs. A slew rate of about 1 V/μs is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Fig. 21. These circuits operate in concert with stability.

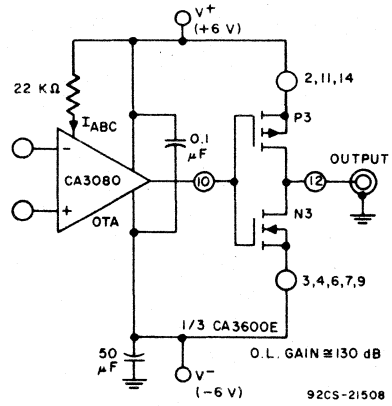


Fig. 18– COS/MOS transistor-pair used as post-amplifier to op-amp in open-loop circuit.

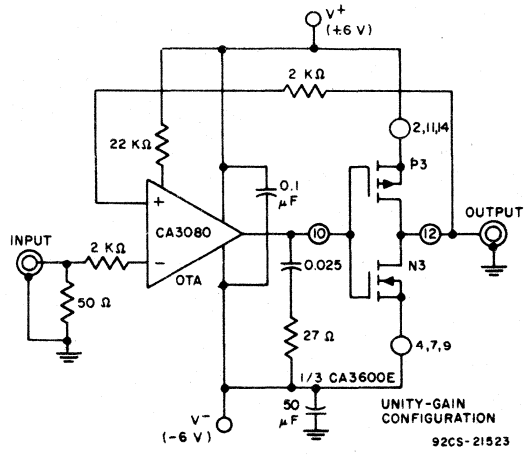


Fig. 19– COS/MOS transistor-pair used as post-amplifier to op-amp in unity-gain circuit.

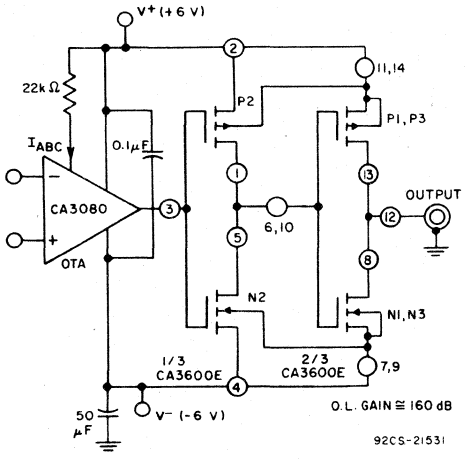


Fig. 20– COS/MOS transistor-pairs used as two-stage post-amplifier to op-amp in open-loop circuit.

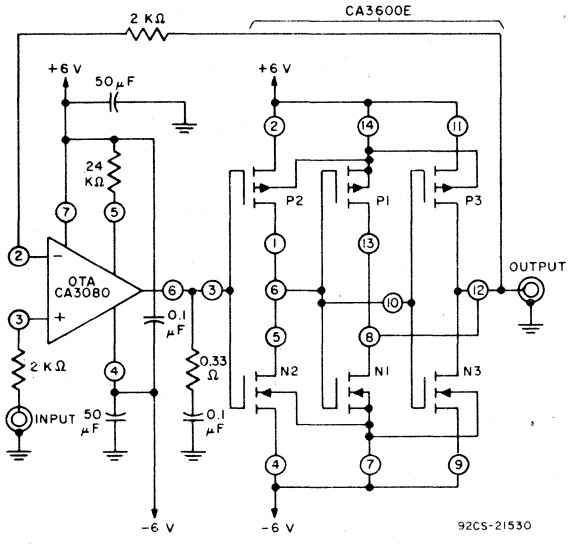


Fig. 21– Unity-gain amplifier uses COS/MOS transistor-pairs as two-stage post-amplifier to op-amp.

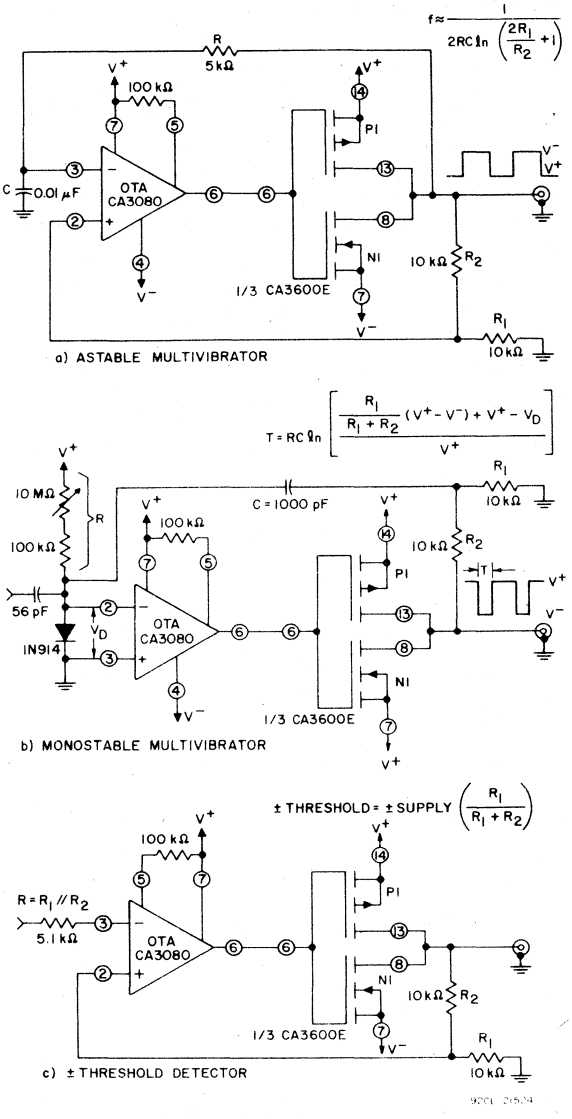


Fig. 22– Multistable circuits using COS/MOS transistor-pairs.

Multivibrators, Threshold Detectors, and Comparators

Descriptions of several circuits using COS/MOS transistor-pairs in both monostable and astable multivibrators have been published.[4,5] The characteristics of COS/MOS pairs are also ideal for mating with micropower op-amps in circuits such as the precision multistable circuits shown in Fig. 22. In these circuits precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080 Operational Transconductance Amplifier.[2,3] Moreover, speed vs. power consumption tradeoffs can be made by adjustment of the Amplifier-Bias-Current (I_{ABC}) supplied to terminal 5 of the CA3080. The quiescent power consumption of the circuits shown in Fig. 22 is typically 6 mW, but can be made to operate in the micropower region by suitable modifications.

The schematic diagram of a programmable micropower comparator, shown in Fig. 23 employs the combination of an op-amp (CA3080A) and COS/MOS transistor-pairs in the CA3600E. Quiescent power consumption of the circuit is about 10 μW(typ.). When the comparator is strobed "ON", transistor P1 is driven into conduction and the OTA becomes active. Under these conditions, the circuit consumes 420 μW and responds to a differential-input signal in about 8 μs. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150 ns but the power consumption is increased to 21 mW. The differential amplifier input common-mode range for this circuit is −1 V to +10.5 V. Voltage gain of this micropower comparator is typically 130 dB.

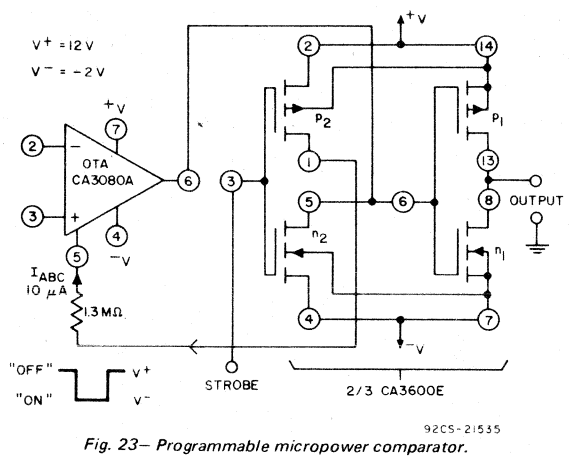


Fig. 23– Programmable micropower comparator.

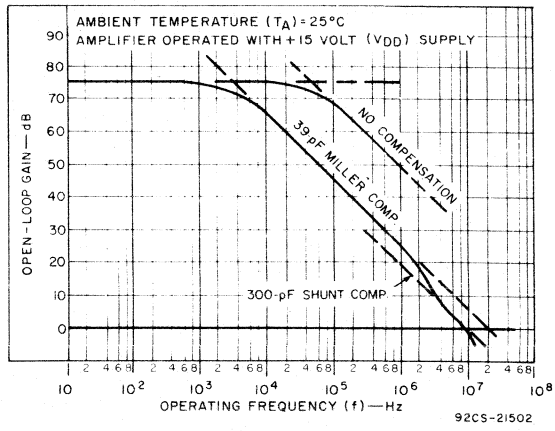


Fig. 25– Open-loop gain characteristic for op-amp in Fig. 24.

Operational Amplifiers

COS/MOS transistor-pairs can be used in conjunction with a bipolar transistor-array IC to build an op-amp as shown in Fig. 24. It is particularly suited for single-supply operation (e.g., mobile and aircraft service). The op-amp is unique in that it is responsive to small-signal ground-referenced inputs and the output stage can easily be driven within 1 mV of ground potential. Its open-loop gain characteristics are shown in Fig. 25; the open-loop slew rate is approximately 30 V/μs.

This circuit is ideal for use as a unity-gain voltage-follower and has been described for operation in connection with a 9-Bit Single-Supply Digital-to-Analog Converter (DAC) using COS/MOS transistors in the resistor-network switches.[6]

The op-amp in Fig. 24 has three stages; its first stage is a differential input circuit using two p-channel transistors (P_4,P_5) in a CA3600E. The second stage is an n-p-n

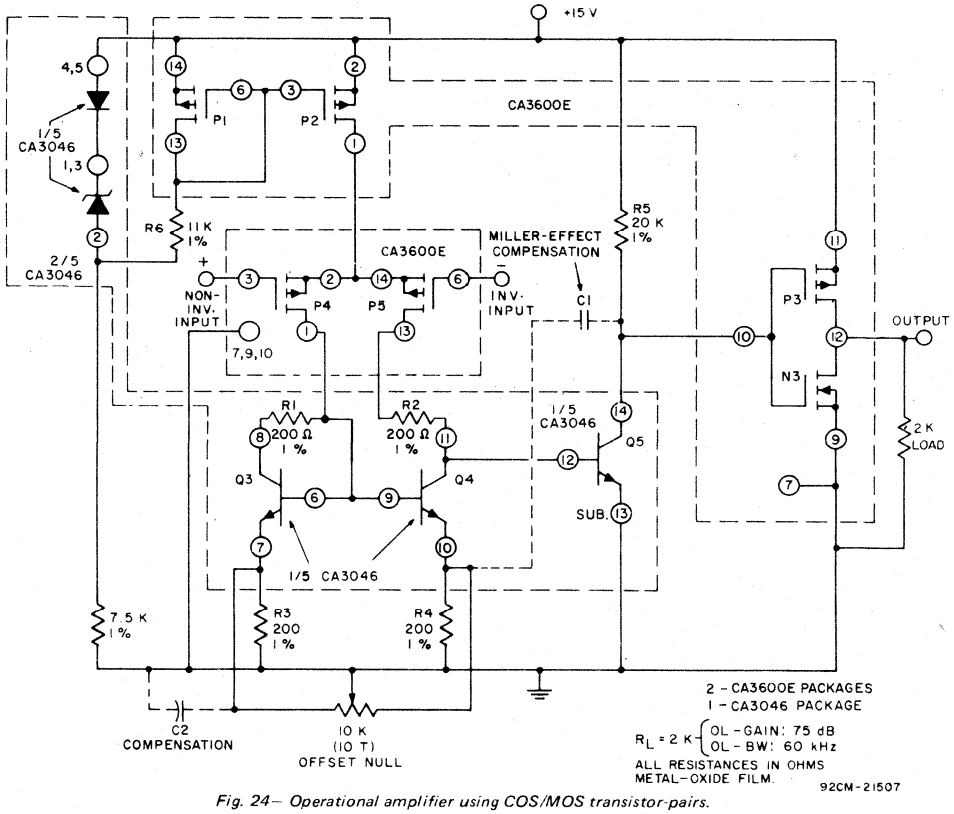


Fig. 24– Operational amplifier using COS/MOS transistor-pairs.

transistor (Q_5) and the output stage is a COS/MOS transistor-pair (P_3,N_3) operating in the manner described above. A constant current of about 400 μA is established in the differential input stage by the zener network in the upper-left portion of Fig. 24. The zener network energizes a current mirror comprised of two p-channel transistors (P_1,P_2) to establish constant-current flow in the differential amplifier stage (P_4,P_5). The drain load for the differential amplifier consists of resistors R_1R_4 and a current mirror (Q_3 Q_4) to optimize conditions for balanced operation of the differential amplifier. The operating theory of current-mirror circuits has been described in reference [2]. Amplifier voltage-offset is nulled with the 10-kilohm balance potentiometer. The second-stage current is established by R_5, and is selected to approximate the first-stage current level (400 μA), to assure similar positive and negative slew rates. The amplifier is shown driving a 2-kilohm load, a typical value used with monolithic op-amps. Voltage gain varies inversely with the choice of load resistance.

The amplifier can be compensated with a single capacitor (C_1), connected as shown by the dotted lines. However, optimum compensation for the unity-gain non-inverting mode is provided by two capacitors: Miller Effect feedback through a 39-pF capacitor C_1 (connected as shown), and a 300-pF capacitor connected between terminals 7 and 13 of the CA3046 transistor array to shunt one-half the driving current. Fig. 25 shows the open-loop gain characteristics with compensation for unity-gain operation. When the amplifier is operated as a voltage-follower, it is recommended that a 1-kilohm resistor, shunted with a 150-pF capacitor, be connected between the amplifier output terminal and terminal 6 of P_5 to avoid a potential latch situation involving the integral gate-protection network. The circuit can also be latched if either input terminal is driven more than about 0.7 volt below ground potential. This latch situation can be avoided by connecting a 1N914 diode from each input terminal to ground, with the diode anode grounded.

Analog Timer

The CA3600E is useful in the design of analog timer circuits. A typical circuit is shown in Fig. 26. For purposes of explanation, let it be assumed that capacitor C_1 initially is in a completely discharged condition; terminal 10, therefore, is initially at ground potential and transistor N_3 is non-conductive. The circuitry at the left of terminal 10 provides a source of constant-current flow through P_1 to charge capacitor C_1 increasingly positive with respect to ground. After the passage of time (T), capacitor C_1 is charged sufficiently in the positive direction so that transistor N_3 is driven into conduction by its gate and the lamp is lighted to signify the end of the time-delay period. The circuit is reset by momentarily closing switch S_1 to discharge capacitor C_1 through R_4.
Resistor-divider network R_1,R_2 establishes the supply voltage to a constant-current network comprised of resistor R_3 and the series-connected COS/MOS pair N_2,P_2, biased for linear operation by resistor R_b as previously described. This combination is connected to the gate terminal (No. 6) of transistor P_1 to form a current mirror, i.e., the current flowing through P_1 to charge C_1 will be essentially equal to the constant-current flow established through R_3, N_2, and P_2. A description of current-mirror operation with MOS transistors is given subsequently.

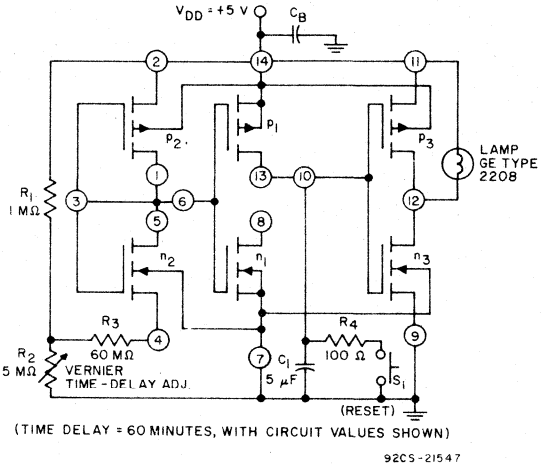


Fig. 26– Analog timer using CA3600E.

Oscillator Circuits

Oscillator circuits using COS/MOS transistor-pairs have been widely used for several years in clock and watch circuits because of their low power consumption and good frequency stability. Details of their operating theory and characteristics have been published.[5,7]

The design of COS/MOS oscillator circuits, like the design of any oscillator circuit, involves the provision of an amplifying section to operate compatibly with an appropriate feedback network. A single stage amplifier using a COS/MOS transistor-pair has already been described. A suitable feedback network to insure stable oscillator performance is easily added, as illustrated in connection with the crystal oscillator circuit shown in Fig. 27. The familiar pi-network has been connected between the input and output terminals, points "D" and "G", to provide the required 180° phase shift for stable oscillator performance. The frequency-determining crystal is an integral part of the pi-network feedback circuit. The resistors R_1 and R_2 decrease the total power consumption of the oscillator at a particular supply voltage and enhance the frequency stability. Variable frequency oscillators can be built by replacing the crystal with an appropriate inductance and tuning the pi-network by conventional means.

Current Mirrors Using MOS Transistors

Monolithic linear IC's using bipolar transistors frequently employ so-called "current-mirror" circuits. The theory and practical applications of current mirrors using bipolar transistors have been described in the literature.[2] As shown in

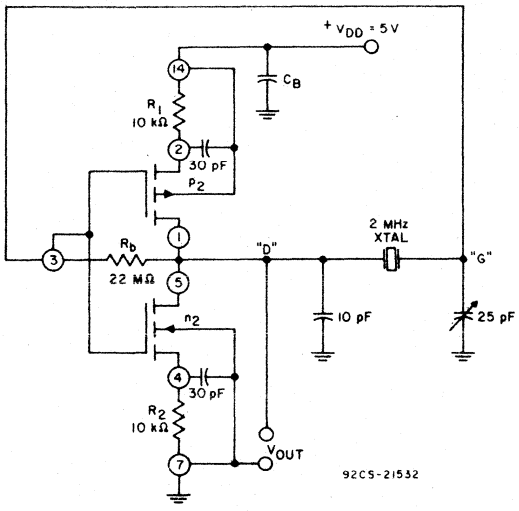


Fig. 27– Typical crystal-oscillator circuit using COS/MOS transistor-pair (1/3 CA3600E).

Fig. 28, a rudimentary form of "current-mirror" consists of a transistor Q_1 with a second transistor Q_2 connected as a diode. When both transistors have identical characteristics, a current I_1 forced to flow through Q_2 produces a current (I_2) of equal magnitude to flow in the collector of Q_1 (provided there is sufficient collector potential for Q_1). In a common form of application, a source of potential is used to force

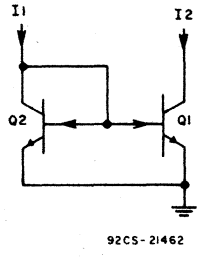


Fig. 28– Current mirror using n-p-n bipolar transistors.

constant-current flow I_1, and thus to establish the flow of constant current I_2 through Q_1. Arrangements of this generic current-mirror type are frequently used when Q_1 acts as the common-emitter impedance in a differential-amplifier circuit.

MOS transistors are also applicable as current mirrors, as shown in Fig. 29. The diode-connected MOS transistor N_2 functions as a transistor with 100 per-cent feedback. Therefore, the gate-to-source voltage (V_{GS}) in N_2 retains control of the drain current as in normal transistor action, i.e., $I_D \cong g_{fs}V_{GS}$, where g_{fs} is the forward transconductance of the device. If a current I_1 is forced into the diode-connected transistor (N_2), the gate-to-source voltage will rise until equilibrium is reached. Thus, a gate-to-source voltage is established in N_2 such that N_2 "sinks" the applied current I_1.

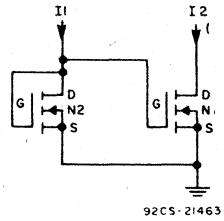


Fig. 29– Current mirror using n-channel MOS transistors.

If the gate and source terminals of another transistor (N_1) are connected in shunt with the gate and source terminals of N_2, as shown in Fig. 29, N_1 is also able to "sink" a mirror current approximately equal to that flowing in the drain lead of the diode-connected transistor N_2. It is assumed that both MOS transistors have identical characteristics, a prerequisite that is essentially established by the monolithic IC fabrication technology used in manufacturing the CA3600E COS/MOS transistor array.

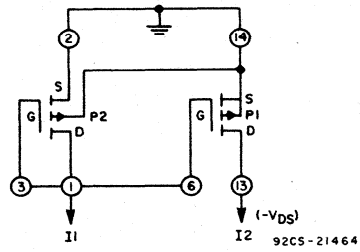


Fig. 30– Current mirror using p-channel MOS transistors in CA3600E.

Current mirrors can also be designed with p-channel MOS transistors as illustrated by the arrangement in Fig. 30 using transistors in the CA3600E. The characteristics of a current mirror using the p-channel transistors in the CA3600E are superior to those which can be achieved with a current mirror using the n-channel transistors because the characteristics of the p-channel transistors are more nearly matched. The data

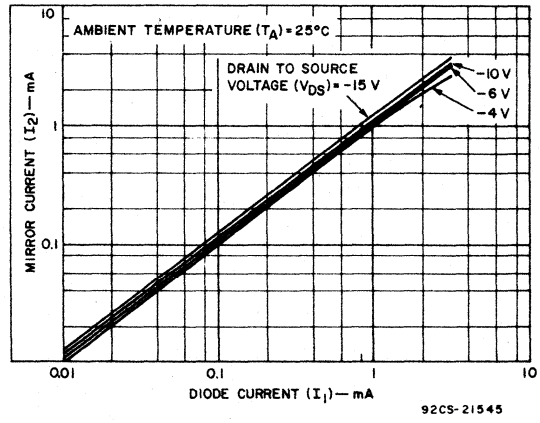


Fig. 31– Characteristics of current mirror circuit of Fig. 30 using p-channel transistors.

contained in Fig. 31 show the high degree of tracking between I_1 and I_2 for several values of drain voltage V_D. Fig. 32 also illustrates the fact that this high degree of tracking between I_1 and I_2 can be maintained to within about one per-cent despite wide variations in ambient temperature.

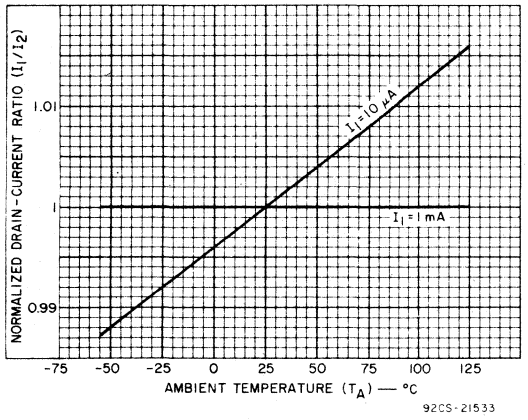


Fig. 32– Normalized drain current ratio vs. ambient temperature for typical current mirror using p-channel transistors (Fig. 30).

The op-amp circuit in Fig. 24 contains an illustrative example of a current-mirror circuit using two p-channel transistors in the CA3600E. Transistor P_2 serves as a constant-current source (≅ 400 μA) for the differential amplifier, consisting of transistors P_4 and P_5 and their drain-load network. Transistor P_2 is in a "mirrored" connection with transistor P_1. A stabilized source of supply potential is developed across the zener diode (terminals 11 and 12 of the CA3083) and drives about 400 μA of current through R_6 and P_1.

Complementary Current Mirrors Using COS/MOS Transistor-Pairs

COS/MOS transistor-pairs can be applied advantageously in the design of Complementary Current-Mirrors, as shown in Fig. 33. Transistors P_1 and N_1 are series-connected and biased for linear operation as previously described, so that there is a current flow I_{D1} through P_1 and N_1. The potential developed between terminals 13 and 14 is applied as gate-source (2,3) voltage for P_2, forcing "mirror" operation of P_2 to produce a current source I_{D2-P} equal to I_{D1}. Likewise, the potential developed between terminals 7 and 8 is applied as gate-source (3,4) voltage for N_2 forcing "mirror" operation of N_2 to produce a current-sink I_{D2-N} equal to I_{D1}.

A variant of this complementary current mirror is used in the analog timer circuit shown in Fig. 26. Transistors P_2 and N_2 are series-connected together with a 60-megohm resistor to establish their drain current at 5 nA. The potential developed across terminals 1 and 2 also appears as the gate-source voltage for transistor P_1, thereby establishing a mirror-current source of 5 nA at terminal 13 to charge capacitor C_1 linearily. In this circuit, the "mirrored" current-sink available at terminal 8 (transistor N_1) is unused. This type of current-mirror configuration is exceptionally stable with temperature variations.

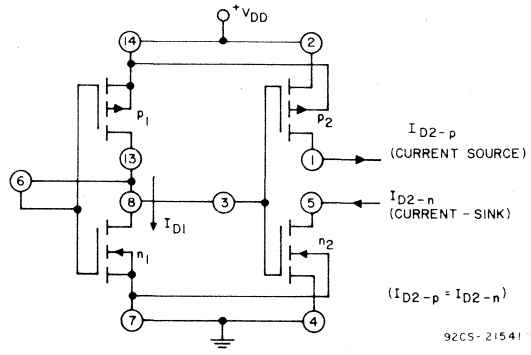


Fig. 33– Complementary current mirrors using COS/MOS transistor-pairs in CA3600E.

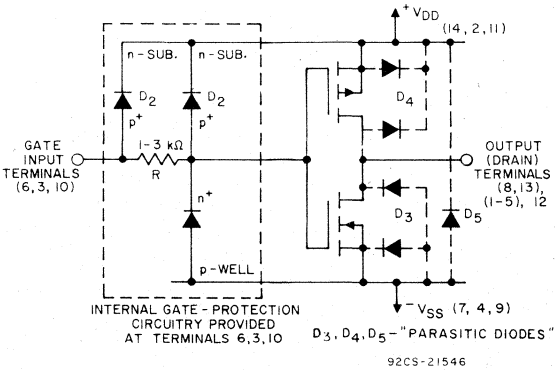


Fig. 34– Integral protection circuits used in CA3600E.

Considerations in Handling CA3600E Devices

Failure of the gate-channel oxide was a persistent problem in early MOS devices. The breakdown of the oxide is generally in the order of 100 volts, and the dc resistance is in the order of 10^{12} ohms. Because of this extremely high resistance, even a very-low-energy source (such as static charge) is capable of developing sufficient voltage to cause damage. Furthermore, the oxide can be punctured and damaged by a single voltage excursion beyond the breakdown limit.

Fig. 34 shows a protection circuit[5,8] which is incorporated at each gate-lead of the CA3600E. A typical value of 1 to 3 kilohms is used for the input resistor R, which functions in combination with the capacitance of the gate and the associated protective diode to integrate and clamp input voltages to a safe level. This circuit also shows the "substrate diodes" (D_3, D_4, and D_5) which provide protection to the MOS channels at the output terminals.

Although the gate-protection system is very effective in guarding against damage due to static charges, it is prudent to observe the following precautions:[5,9]

1. The leads of devices should be in contact with a conductive material, except when being tested or in actual operation. A conductive material such as "ECCOSORB LD26"* or equivalent is suggested for use during storage and/or handling. Devices should not be inserted in non-conductive containers such as conventional plastic "snow" or trays.
2. Soldering-iron tips, metal parts of fixtures and tools, and handling facilities should be grounded.
3. Devices should not be inserted into or removed from circuits with the power on because transient voltages may cause permanent damage.
4. Signals from low-impedance sources should not be applied to the gate terminals while the power supply is off. As a corollary, it follows that the power supply should not be turned off while a signal from a low-impedance source is being applied to any gate terminal. When the V_{DD} supply is off, the positive "back-bias" voltage is removed from the cathode of diode D_2 (see Fig. 34). Consequently, an input signal with positive-going polarity can drive D_2 into conduction. Under these conditions a low-impedance signal source can provide sufficient current to permanently damage D_2 and/or melt aluminum interconnection paths. Therefore, if, in any system design using the CA3600E, any gate input excursion is expected to exceed $+V_{DD}$ or fall below $-V_{SS}$, the current through the input diodes should be limited to 100 μA.
5. All unused gate-input terminals should be connected to V_{SS} (ground). When source terminals (e.g., Nos. 2 and 11) of p-channel transistors are unused in circuitry, they should be connected to terminal No. 14. Likewise, when source terminals (e.g., Nos. 4 and 9) of n-channel transistors are unused, they should be connected to terminal No. 7.
6. After CA3600E units have been mounted on circuit boards, proper handling precautions should still be observed. Until these subassemblies are inserted into a complete system, the board is no more than an extension of the device leads mounted on the board. It is a good practice to place conductive tape or jumpers on circuit-board terminals to "ground" gate terminals.
7. In some applications of the CA3600E separate positive and negative power supplies may be employed (e.g., see Fig.22). In such applications provisions must be made so that the positive supply voltage is applied prior to the application of negative supply voltage and vice versa on shutdown. This precaution is necessary to avoid possible damage due to "latching" involving the substrate and protective diode circuits.

* Trade Mark: Emerson and Cumming, Inc.

Power Control Circuits
Technical Data

CA3165

Mini-DIP
(E Suffix)
H-1817

14-Lead DIP
(E1 Suffix)
H-1517

Electronic Switching Circuit

FEATURES:

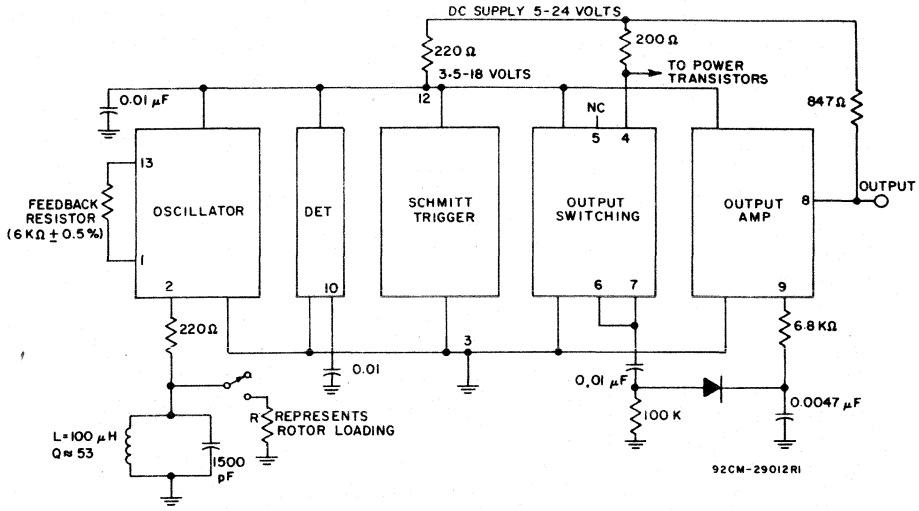
- *Switching initiated by damping of internal oscillator*
- *Proximity sensing of rotational motion*
- *Repeatable timing of switching states*
- *Five outputs — two complementary pairs and one non-inverting output (CA3165E1)*
- *Two outputs — one complementary pair (CA3165E)*

The RCA CA3165 is a single-chip electronic switching circuit intended primarily for ignition applications. It includes an oscillator that is amplitude-modulated by the rotor teeth of a distributor, a detector that develops the positive-going modulation envelope, a Schmitt trigger that eliminates switching uncertainties. Both types include two complementary high-current switched outputs for driving power transistors requiring up to 120 milliamperes. The CA3165E also includes two complementary low-current outputs that incorporate internal current limiting and a non-inverting output amplifier with uncommitted input capable of switching 27 milliamperes.

The CA3165 is supplied in the 8-lead dual-in-line plastic package (Mini-DIP, E suffix) and in the 14-lead dual-in-line plastic package (E1 suffix).

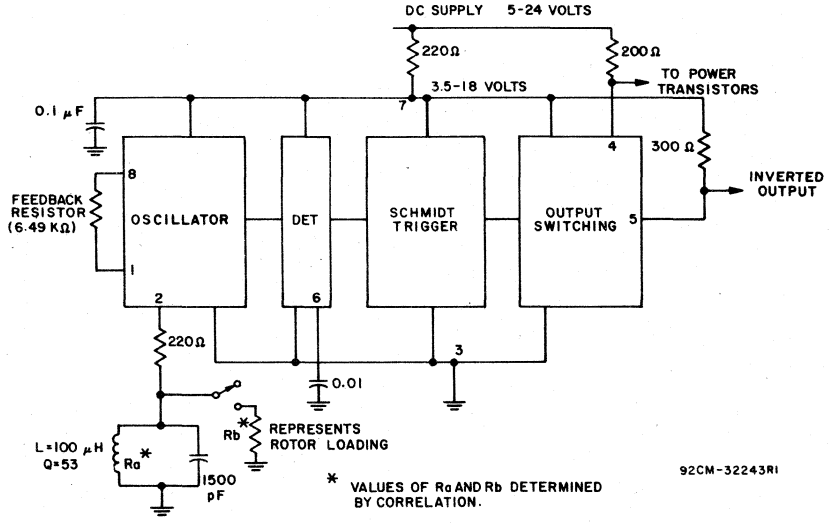
MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3165E1	CA3165E		
DC Voltage (With reference to terminal 3):				
Terminal	4,6,8	4,5	24	V
Terminal	5,7,12	7	18	V
Terminal	9	—	1.5	V
CURRENT (At terminals indicated):				
Terminal	4,6	4,5	120	mA
Terminal	5,7	—	-0.1 to 0.1	mA
Terminal	8	—	30	mA
DEVICE DISSIPATION:				
Up to T_A = 55° C			600	mW
Above T_A = 55°C		derate linearly at	6.67	mW/°C
AMBIENT TEMPERATURE RANGE:				
Operating			-40 to +85	°C
Storage			-65 to +150	°C
LEAD TEMPERATURE (During soldering):				
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.			265	°C



Oscillator Condition	Terminal 10	Terminal 4	Terminal 5	Terminal 6	Terminal 7	Terminal 8
Unloaded	Low	High	High	Low	Low	Low
Loaded	High	Low	Low	High	High	High

Fig. 1 - Functional block diagram for CA3165E1



Oscillator Condition	Terminal 4	Terminal 5	Terminal 6
Unloaded	High	High	Low
Loaded	Low	Low	High

Fig. 2 - Functional block diagram for CA3165E

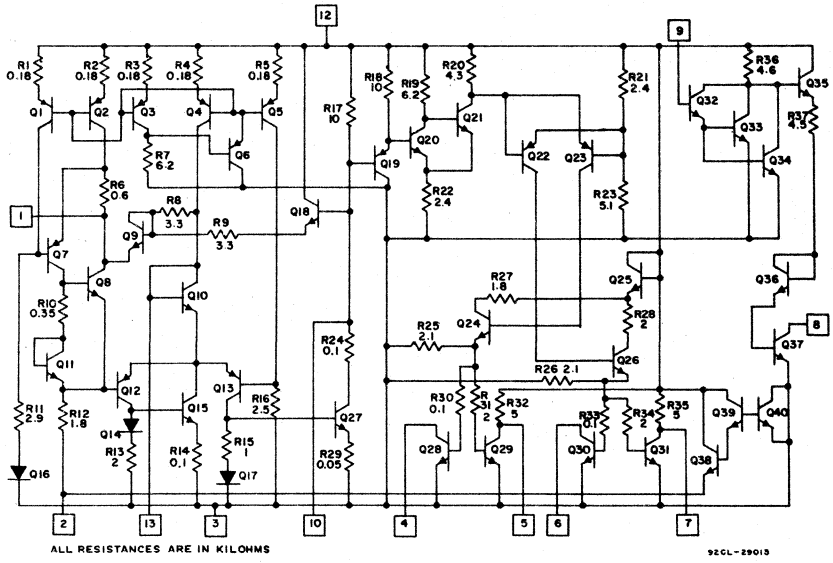


Fig. 3 - Schematic diagram for CA3165E1

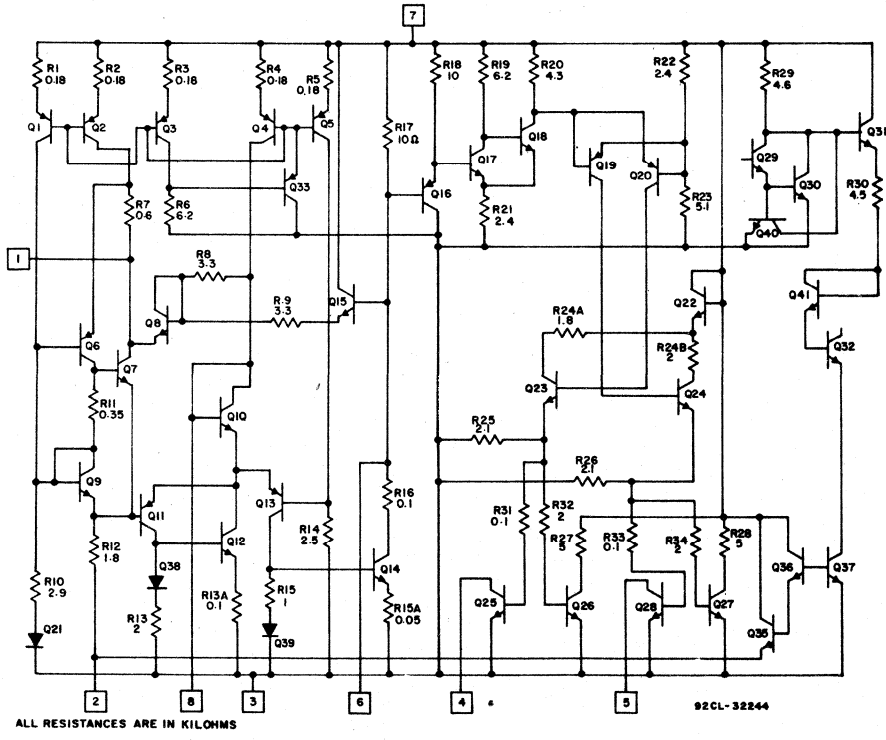


Fig. 4 - Schematic diagram for CA3165E

ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$, $V^* = 13$ V, Measured in the circuit of Fig. 5 (CA3165E1) or Fig. 6 (CA3165E)

CHARACTERISTIC	TEST PERIOD	LIMITS						UNITS
		CA3165E1			CA3165E			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Current at Term.* Δ	Dwell	—	18.4	—	—	18.4	—	mA
	Spark	—	17.5	—	—	17.5	—	
Output Voltage at Term. 4 V_4	Dwell	12.8	—	—	12.8	—	—	V
	Spark	—	—	0.5	—	—	0.5	
Output Voltage at Term. 7 V_7	Dwell	—	—	1	—	—	—	V
Output Voltage at Term. 8 V_8	Dwell Portion of Spark	—	—	0.9	—	—	—	V
		1.2	—	—				
Oscillator Voltage at Term. 2 V_2	Dwell	—	4.4	—	—	4.4	—	V_{p-p}
	Spark	—	0.6	—	—	0.6	—	

	*	Δ
CA3165E	7	I_7
CA3165E1	12	I_{12}

APPLICATION INFORMATION

Figs. 5 and 6 shows the application of the CA3165 in a typical ignition system.

TERMINAL DESCRIPTIONS		
Terminal		
CA3165E1	CA3165E	Function
1	1	Oscillator feedback resistor, R_f
2	2	220Ω protective resistor to tank circuit
3	3	Ground
4	4	Direct output — R_7 load resistor 200 ohms ± 5%, and R_8 to power Darlington 15 ohms ± 10%
5	—	Direct output — low current — not connected
6	5	Inverted high current output
7	—	Inverted low current output through C_1 (0.01 μF) to D_3 and R_3 (100 K ohm)
8	—	Output amplifier output — through R_6 and R_5 (27 ohms and 820 ohms to supply)
9	—	Output amplifier input — through R_4 (6800 ohms) to D_3 and C_5 (0.0047 μF)
10	6	Detector output — C_2 to ground (0.0022 μF)
11	—	No connection
12	7	Circuit supply voltage through R_1 (220 ohms protective resistor) to automotive supply
13	8	Oscillator feedback resistor R_f to terminal 1
14	—	No connection

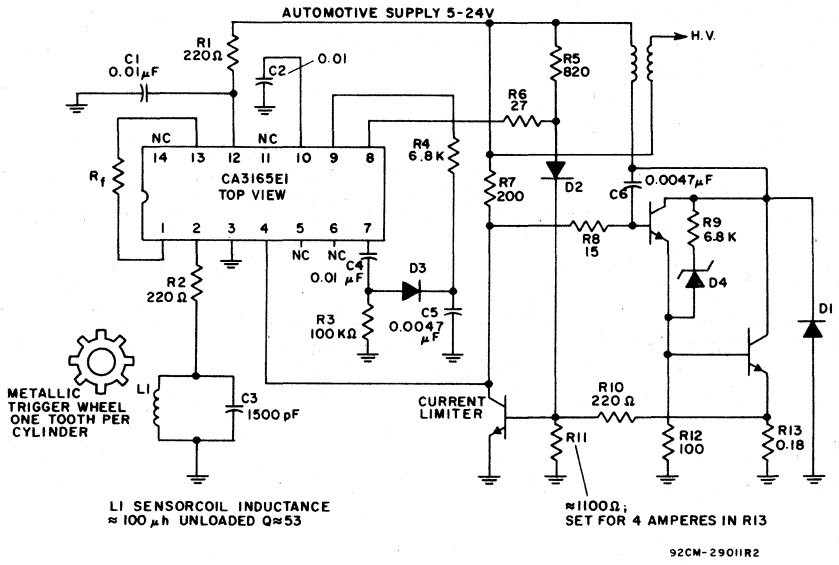


Fig. 5 - Typical ignition system using the CA3165E1

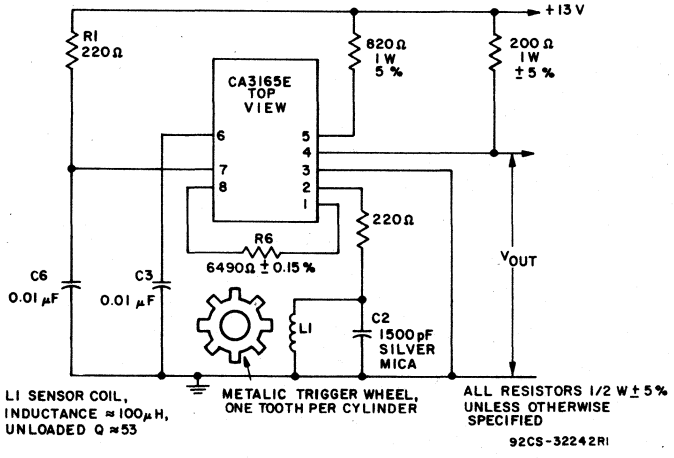


Fig. 6 - Typical ignition system using the CA3165E

APPLICATION INFORMATION

Figs. 5 and 6 shows the application of the CA3165 in a typical ignition system. The oscillator on the chip operates at about 400 kHz as determined by the tuned circuit L1, C3. The amplitude of the oscillation is detected on the chip and applied to a Schmitt trigger which sets the terminal voltage as shown in the chart in Figs. 1 and 2 for the unloaded condition of the oscillator. As a metallic tooth in the rotor passes the coil L1 eddy-current losses occur which reduce the Q of the resonant circuit and decrease the amplitude of the oscillations to a level below that of a reference in the detector circuit. The output terminals are then switched to states as shown in the chart in Figs. 1 and 2 for the loaded condition of the oscillator. The oscillation is maintained at this lower amplitude by switching in additional feedback in the oscillator circuit. The fact that the oscillator continues to operate at some minimum level during this dwell period eliminates timing variations which would occur if the oscillator had to be restarted by random noise.

Spark occurs as terminal 4 is switched from high to low. The output amplifier clamps terminal 4 low through the regulator during the duration of the spark.

The Dwell period represents the time that terminal 10 (CA3165E1) or terminal 6 (CA3165E) is high, terminal 4 is low, and the coil is charged.

The value of the oscillator feedback, resistor, R_f, is selected to set the dwell period. With a sintered-iron 8 f-tooth rotor, a typical value of R_f is 6500 ohms for 28.5 degrees of dwell out of a 45 degree cycle. For a star-type rotor and a particular coil in a typical distributor, the feedback resistor would be larger (typically 8800 ohms) depending on clearances, coil geometry and tooth shape.

Timing waveforms are shown in Fig. 7.

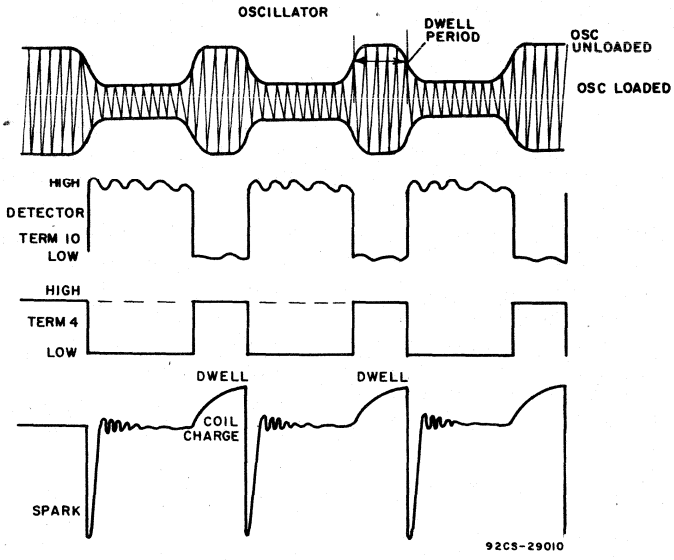
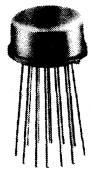


Fig. 7 - Timing sequence

CA3020, CA3020A



12-Lead TO-5

H-1528

Multipurpose Wide-Band Power Amplifiers

For Military, Industrial, and Commercial Equipment at Frequencies up to 8 MHz

Features:

- **High power output — class B amplifier. . . CA3020 — 0.5 W typ. at V_{CC} = +9 V CA3020A — 1.0 W typ. at V_{CC} = +12 V**
- **Wide frequency range. . . Up to 8 MHz with resistive loads**
- **High power gain. . .75 dB typ.**
- **Single power supply for class B operation with transformer. . . CA3020 — 3 to 9 V CA3020A — 3 to 12 V**
- **Built-in temperature-tracking voltage regulator provides stable operation over −55°C to +125°C temperature ran**

The RCA-CA3020 and CA3020A are integrated-circuit, multistage, multipurpose, wide-band power amplifiers on a single monolithic silicon chip. They employ a highly versatile and stable direct-coupled circuit configuration featuring wide frequency range, high voltage and power gain, and high power output. These features plus inherent stability over a wide temperature range make the CA3020 and CA3020A extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

The CA3020 and CA3020A are particularly suited for service as class B power amplifiers. The CA3020A can provide a maximum power output of 1 watt from a 12-volt dc supply with a typical power gain of 75 dB. The CA3020 provides 0.5-watt power output from a 9-volt supply with the same power gain.

These types are supplied in hermetically sealed TO-5 style 12-lead packages.

SCHEMATIC DIAGRAM FOR CA3020 AND CA3020A

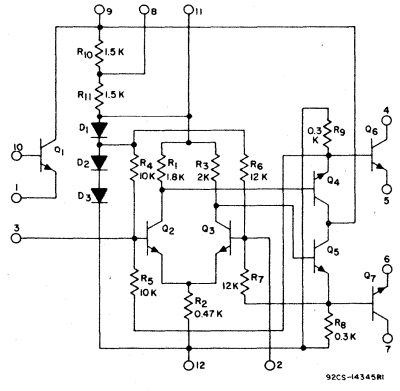


Fig.1

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ± 30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

Applications:

- **AF power amplifiers for portable and fixed sound and communications systems**
- **Servo-control amplifiers**
- **Wide-band linear mixers**
- **Video power amplifiers**
- **Transmission-line driver amplifiers (balanced and unbalanced)**
- **Fan-in and fan-out amplifiers for computer logic circuits**
- **Lamp-control amplifiers**
- **Motor-control amplifiers**
- **Power multivibrators**
- **Power switches**
- **Companion Application Note, ICAN-5766, "Application of CA3020 and CA3020A Integrated Circuit Multipurpose Wide-Band Power Amplifiers"**

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION:

WITHOUT HEAT SINK	WITH HEAT SINK
At T_A = 25°C . . . . . 1 W	At T_C = 25°C . . . . . 2 W
Above T_A = 25°C . . . . . derate linearly 6.7 mW/°C	At T_C = 25°C to T_C = 55°C . . . . . 2 W
	Above T_C = 55°C . . derate linearly 16.7 mW/°C

TEMPERATURE RANGE:

Operating . . . . . -55°C to +125°C
Storage . . . . . -65°C to +150°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to terminal 12 is 0 to +10 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
1		*	*	*	*	*	*	*	▲ 0 -10/-12	+3 Note 1	*	+10 0
2			*	*	*	*	*	*	*	*	*	+2 -2
3				*	*	*	*	*	*	*	*	+2 -2
4					▲ +18/+25 0	*	*	*	*	*	*	▲ +18/+25 0
5						*	*	*	*	*	*	+3 Note 2
6							▲ 0 -18/-25	*	*	*	*	+3 Note 2
7								*	*	*	*	▲ +18/+25 0
8									Note 3	*	*	Note 3 0
9										+10 0	Note 1 0	+10/+12 0
10											*	+10 0
11												*
12												REF. SUB-STRATE

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	-	20
2	-	-
3	-	-
4	300	-
5	-	300
6	-	300
7	300	-
8	-	-
9	20	-
10	1	-
11	20	-
12	-	-

Note 1: This voltage is established by the maximum current rating.

Note 2: The emitters of Q_6 and Q_7 may be returned to a negative voltage supply through emitter resistors. Current into terminal No.9 should not be exceeded and the total device dissipation should not be exceeded.

Note 3: Terminal No.8 may be connected to terminals Nos.9, 11, or 12.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

▲ Higher value is for CA3020A.

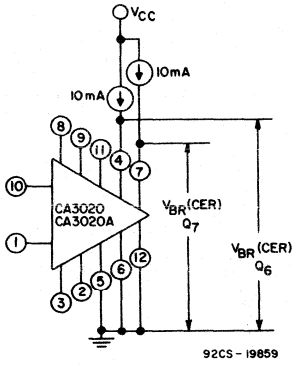
CA3020, CA3020A

ELECTRICAL CHARACTERISTICS AT $T_A = 25°C$

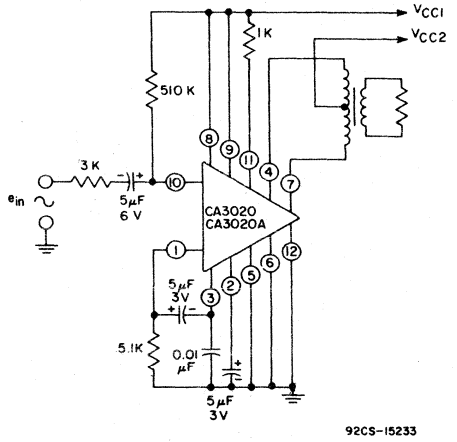
CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			LIMITS CA3020			LIMITS CA3020A			UNITS
		CIRCUIT AND PROCEDURE	DC SUPPLY VOLTAGE								
		FIG.	V_{CC1}	V_{CC2}	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Collector-to-Emitter Breakdown Voltage, Q_6 & Q_7 at 10 mA	$V_{(BR)CER}$	2a	-	-	18	-	-	25	-	-	V
Collector-to-Emitter Breakdown Voltage, Q_1 at 0.1 mA	$V_{(BR)CEO}$	-	-	-	10	-	-	10	-	-	V
Idle Currents, Q_6 & Q_7	I_4 IDLE I_7 IDLE	8	9.0	2.0	-	5.5	-	-	5.5	-	mA
Peak Output Currents, Q_6 & Q_7	I_4PK I_7PK	8	9.0	2.0	140	-	-	180	-	-	mA
Cutoff Currents, Q_6 & Q_7	I_4 CUTOFF I_7 CUTOFF	8	9.0	2.0	-	-	1.0	-	-	1.0	mA
Differetial Amplifier Current Drain	I_{CC1}	8	9.0	9.0	6.3	9.4	12.5	6.3	9.4	12.5	mA
Total Current Drain	I_{CC1} + I_{CC2}	8	9.0	9.0	8.0	21.5	35.0	14.0	21.5	30.0	mA
Differential Amplifier Input Terminal Voltages	V_2 V_3	8	9.0	2.0	-	1.11	-	-	1.11	-	V
Regulator Terminal Voltage	V_{11}	8	9.0	2.0	-	2.35	-	-	2.35	-	V
Q, Cutoff (Leakage) Currents: Collector-to-Emitter	I_{CEO}	-	10.0	-	-	-	100	-	-	100	μA
Emitter-to-Base	I_{EBO}		3.0	-	-	-	0.1	-	-	0.1	
Collector-to-Base	I_{CBO}		3.0	-	-	-	0.1	-	-	0.1	
Forward Current Transfer Ratio, Q_1 at 3 mA	h_{FE1}	-	6.0	-	30	75	-	30	75	-	
Bandwidth at -3 dB Point	BW	9	6.0	6.0	-	8	-	-	8	-	MHz
Maximum Power Output	$P_{O(MAX)}$	10	6.0	6.0	200	300[a]	-	200	300[a]	-	mW
			9.0	9.0	400	550[a]	-	400	550[a]	-	
			9.0	12.0	-	-	-	800	1000[b]	-	
Sensitivity for $P_{OUT} = 400$ mW	e_{IN}	10	9.0	9.0	-	35[a]	55	-	-	-	mV
Sensitivity for $P_{OUT} = 800$ mW	e_{IN}	10	9.0	12.0	-	-	-	-	50[b]	100	mV
Input Resistance---- Terminal 3 to Ground	R_{IN3}	11	6.0	6.0	-	1000	-	-	1000	-	Ω
Junction-to-Case Thermal Resistance	θ_{J-C}	-	-	-	-	-	60	-	-	60	°C/W

a $R_{CC} = 130\,\Omega$

b $R_{CC} = 200\,\Omega$



a. Collector-to-Emitter Breakdown Voltage (Q_6 and Q_7) Circuit



b. Typical Audio Amplifier Circuit Utilizing the CA3020 or CA3020A As An Audio Preamplifier and Class B Power Amplifier

Fig.2

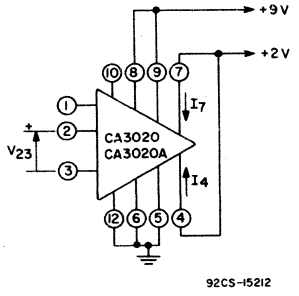
TYPICAL PERFORMANCE DATA*

An External Radiator is Recommended for High Ambient Temperature Operation

CHARACTERISTICS	SYMBOLS	CA3020	CA3020A	UNITS
Power Supply Voltage	V_{CC_1}	9.0	9.0	V
	V_{CC_2}	9.0	12.0	
Zero Signal Current Diff. Ampl.	I_{CC_1}	15	15	mA
Zero Signal Current Output Ampl.	I_{CC_2}	24	24	
Maximum Signal Current Diff. Ampl.	I_{CC_1}	16	16.6	mA
Maximum Signal Current Output Ampl.	I_{CC_2}	125	140	
Maximum Power Output at THD = 10%	P_O	550	1000	mW
Sensitivity	e_{IN}	35	45	mV
Power Gain	G_P	75	75	dB
Input Resistance	R_{IN}	55	55	kΩ
Efficiency	η	45	55	%
Signal-to-Noise Ratio	S/N	70	66	dB
THD at 150 mW level		3.1	3.3	%
Test Signal Frequency from 600Ω Generator		1000	1000	Hz
Equivalent Collector-to-Collector Load Resistance	R_{CC}	130	200	Ω

* Refer to Figs.8 through 12 for Measurement and Symbol Information.

TYPICAL TRANSFER CHARACTERISTICS



a. Test Setup

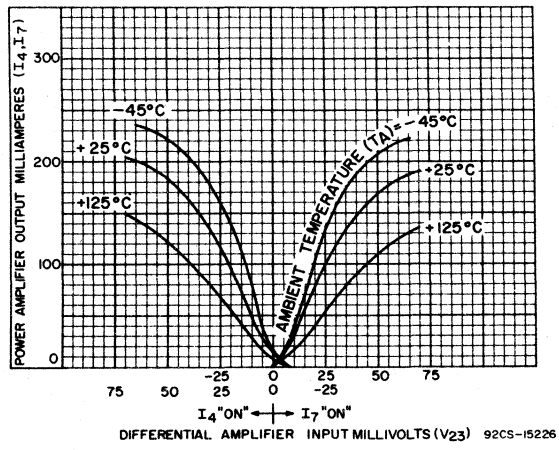
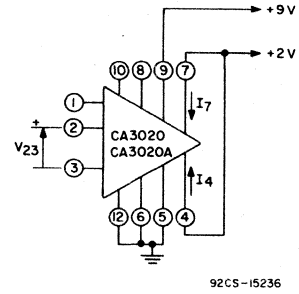


Fig.3 b. Characteristics with R_{10} shorted out



a. Test Setup

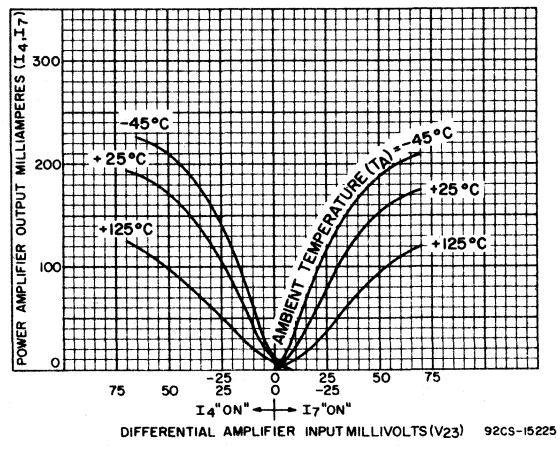
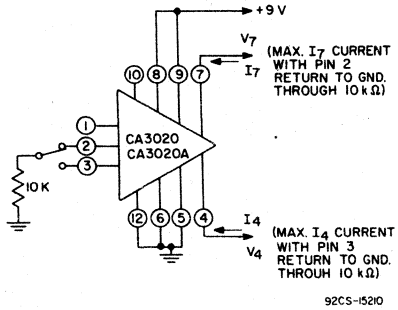


Fig.4 b. Characteristics with R_{10} in circuit

"MINIMUM DRIVE" TYPICAL CURRENT-VOLTAGE SATURATION CURVE



a. Test Setup

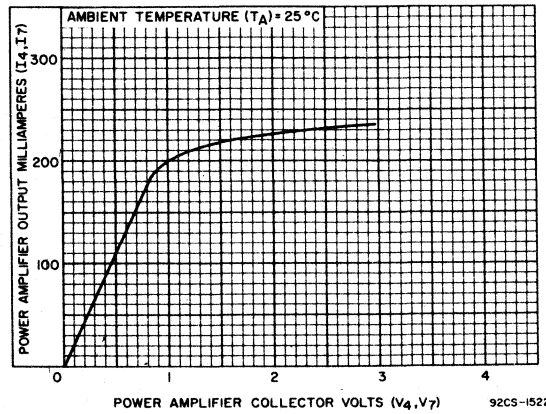
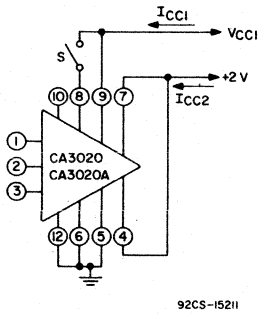
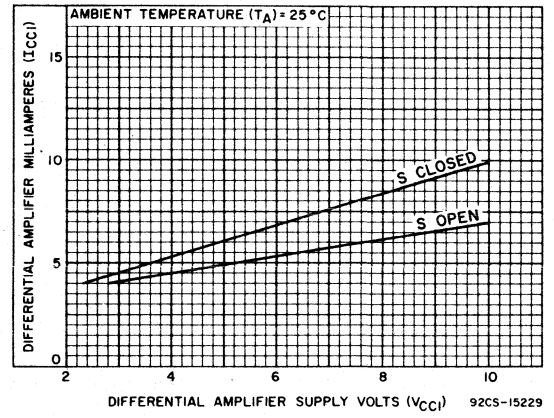


Fig.5 b. Characteristic

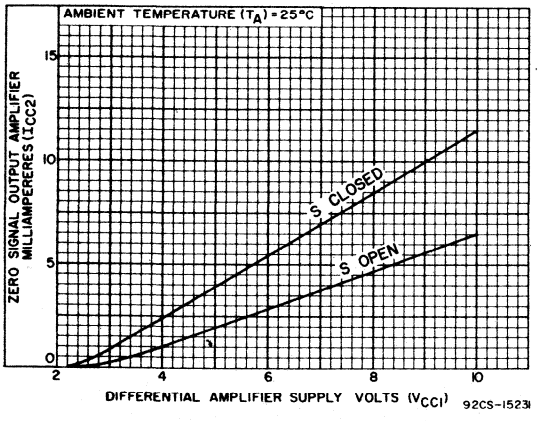
ZERO SIGNAL AMPLIFIER CURRENT vs DIFFERENTIAL AMPLIFIER SUPPLY VOLTAGE



a. Test Setup



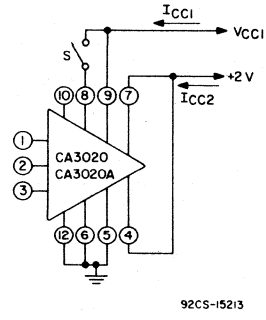
b. Differential Amplifier Characteristics



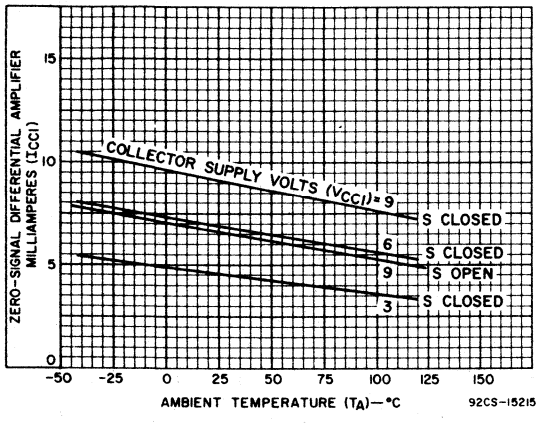
c. Output Amplifier Characteristics

Fig.6

ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE

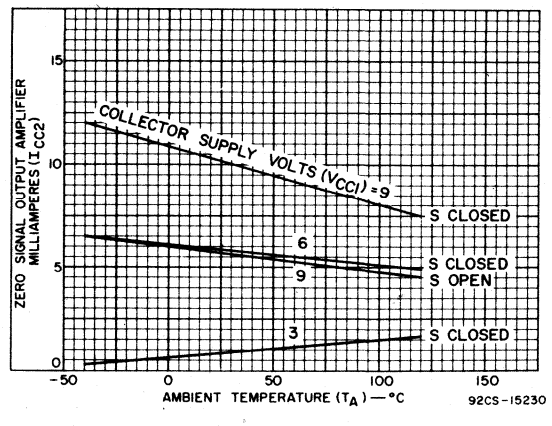


a. Test Setup



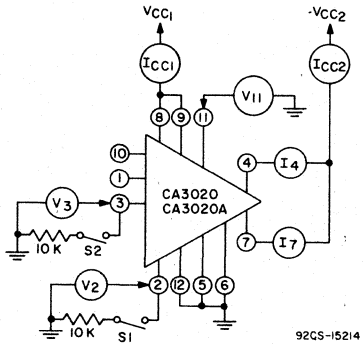
b. Differential Amplifier Characteristics

Fig.7



c. Output Amplifier Characteristics

STATIC CURRENT AND VOLTAGE TEST CIRCUIT



CURRENTS OR VOLTAGES	S1	S2
$I_{4\text{-IDLE}}$	open	open
$I_{7\text{-IDLE}}$	open	open
$I_{4\text{-PEAK}}$	open	close
$I_{7\text{-PEAK}}$	close	open
$I_{4\text{-CUTOFF}}$	close	open
$I_{7\text{-CUTOFF}}$	open	close

CURRENTS OR VOLTAGES	S1	S2
I_{CC1}	open	open
I_{CC2}	open	open
V_2	open	open
V_3	open	open
V_{11}	open	open

Fig.8

MEASUREMENT OF BANDWIDTH AT -3 dB POINTS

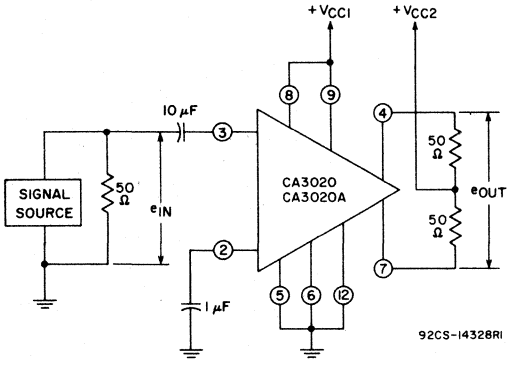
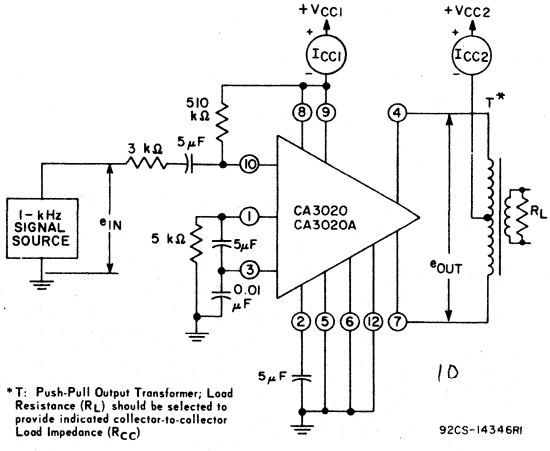


Fig.9

PROCEDURES:

1. Apply desired value of V_{CC_1} and V_{CC_2}
2. Apply 1 kHz input signal and adjust for e_{IN} = 5 mV (rms)
3. Record the resulting value of e_{OUT} in dB (reference value)
4. Vary input-signal frequency, keeping e_{IN} constant at 5 mV, and record frequencies above and below 1 kHz at which e_{OUT} decreases 3 dB below reference value.
5. Record bandwidth as frequency range between -3 dB points.

MEASUREMENTS OF ZERO-SIGNAL DC CURRENT DRAIN, MAXIMUM-SIGNAL DC CURRENT DRAIN, MAXIMUM POWER OUTPUT, CIRCUIT EFFICIENCY, SENSITIVITY, AND TRANSDUCER POWER GAIN



*T: Push-Pull Output Transformer; Load Resistance (R_L) should be selected to provide indicated collector-to-collector Load Impedance (R_{CC})

Fig.10

PROCEDURES:

Zero-Signal DC Current Drain

1. Apply desired Value of V_{CC_1} and V_{CC_2} and reduce e_{IN} to 0V
2. Record resulting values of I_{CC_1} and I_{CC_2} in mA as Zero-Signal DC Current Drain.

Maximum-Signal DC Current Drain, Maximum Power Output, Circuit Efficiency, Sensitivity, and Transducer Power Gain

1. Apply desired value of V_{CC_1} and V_{CC_2} and adjust e_{IN} to the value at which the Total Harmonic Distortion in the output of the amplifier = 10%
2. Record resulting value of I_{CC_1} and I_{CC_2} in mA as Maximum-Signal DC Current Drain
3. Determine resulting amplifier power output in watts and record as Maximum Power Output (P_{OUT})
4. Calculate Circuit Efficiency (η) in % as follows:

$$\eta = 100\,\frac{P_{OUT}}{V_{CC_1}I_{CC_1}+V_{CC_2}I_{CC_2}}$$

where P_{OUT} is in watts, V_{CC_1} and V_{CC_2} are in volts, and I_{CC_1} and I_{CC_2} are in amperes.

5. Record value of e_{IN} in mV^2 (rms) required in Step 1 as Sensitivity (e_{IN})
6. Calculate Transducer Power Gain (G_p) in dB as follows:

$$G_p = 10\log_{10}\frac{P_{OUT}}{P_{IN}}$$

where P_{IN} (in mW) $= \dfrac{e_{IN}^2}{3000 + R_{IN(10)}}$

MEASUREMENT OF INPUT RESISTANCE

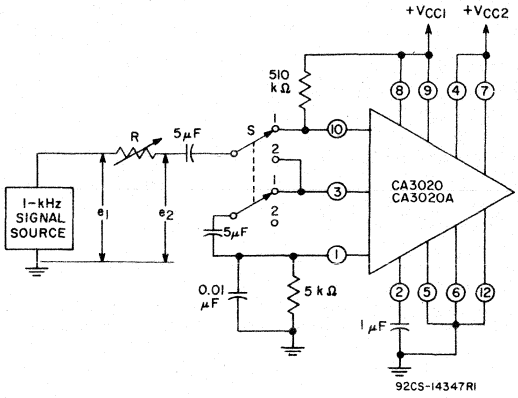


Fig.11

PROCEDURES:

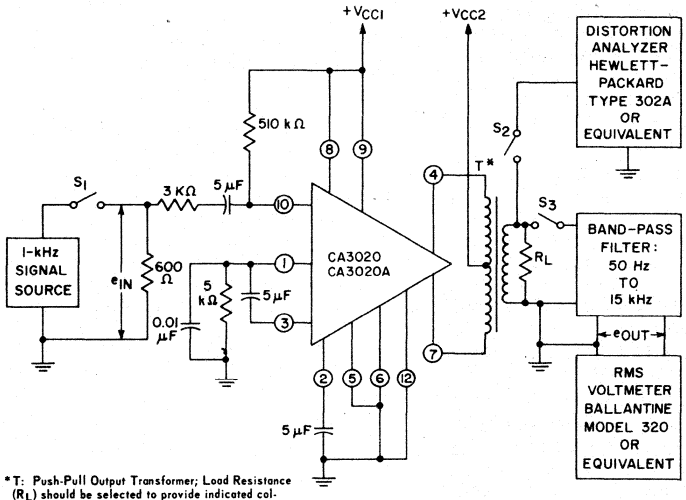
Input Resistance Terminal 10 to Ground ($R_{IN_{10}}$)

1. Apply desired value of V_{CC_1} and V_{CC_2} and set S in Position 1
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as $R_{IN_{10}}$

Input Resistance Terminal 3 to Ground (R_{IN_3})

1. Apply desired value of V_{CC_1} and V_{CC_2} set S in Position 2
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as R_{IN_3}

MEASUREMENT OF SIGNAL-TO-NOISE RATIO AND TOTAL HARMONIC DISTORTION



*T: Push-Pull Output Transformer; Load Resistance (R_L) should be selected to provide indicated collector-to-collector Load Impedance (R_{CC})

PROCEDURES:

Signal-to-Noise Ratio

1. Close S_1 and S_3; open S_2
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for an amplifier output of 150mW and record resulting value of E_{OUT} in dB as e_{OUT_1} (reference value)
4. Open S_1 and record resulting value of e_{OUT} in dB as e_{OUT_2}
5. Signal-to-Noise Ratio (S/N) = $20\log_{10}\frac{e_{OUT_1}}{e_{OUT_2}}$.

Total Harmonic Distortion

1. Close S_1 and S_2; open S_3
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for desired level amplifier output power
4. Record Total Harmonic Distortion (THD) in %

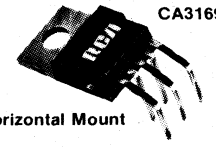
Fig.12

CA3169

CA3169

Vertical Mount H-1893

CA3169M



Horizontal Mount

VERSA-VI TO-220-Style Plastic Packages H-1894

Solenoid and Motor Driver (1/2 H Driver)

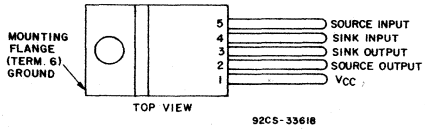
Features:
- *Chip encapsulated in a 5-lead plastic TO-220-style package (VERSA-VI)*
- *Output short-circuit protection*
- *Thermal overload protection*
- *Solenoid inductive "kick" protection with internal-clamp diodes*
- *Output sink and source capacity of 600-mA minimum overtemperature*
- *Horizontal and vertical mounting packages available*
- *Separate sink circuit and source circuit, each individually controlled*
- *Inputs can be driven by TTL logic levels and CMOS logic levels*
- *Low $V_{CE}(sat)$*

Applications:
- *Latching solenoid driver (single and multiple)*
- *Non-latching solenoid driver*
- *Relay driver*
- *Lamp controller*
- *Lamp driver*
- *Motor controller (forward and reverse)*
- *Stepper motor controller*
- *On-off logic controllers (TTL logic)*
- *Intermediate power driver*
- *Triac, SCR, and transistor drivers*

The RCA-CA3169 is a monolithic integrated circuit capable of driving lamps and other devices that can be changed between two states (on or off). Transistors, SCR's, and triacs are some of the solid-state devices that can be controlled by the CA3169. This device can also control relays, solenoids (latching or non-latching), motors (DC - forward and reverse) and DC stepping motors.

The CA3169 contains a separate source-driver circuit with internal current-limiting protection and a separate sink-driver circuit. The sink driver contains an energy-absorbing diode to protect the device against any inductive "kick" during state changes. The CA3169 is protected against overvoltage conditions on the output drivers and overtemperature conditions (thermal-shutdown protection).

The input operating levels are TTL compatible. The source and sink outputs are in their off condition (non-conducting) when their respective inputs are in a HI state, or open-circuited. The outputs are in their on state (conducting) when their respective inputs are LO. The VERSA-VI package is available with two lead configurations. The CA3169 has a vertical-mount lead form, and the CA3169M has a horizontal-mount lead form.



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY VOLTAGE (Pin 1 to GND) ..... Positive . . .41 V DC
Negative . . .1.4 V DC
SINK CURRENT ..... 1.9 A
SOURCE CURRENT ..... Controlled by Internal Current Limiting
INPUT VOLTAGE:
SINK INPUT (Pin 4 to GND) ..... 17 V
SOURCE INPUT (Pin 5 to GND) ..... 17 V
MAXIMUM FORWARD CURRENT—Diode D1 ..... 2.5 A
MAXIMUM FORWARD CURRENT—Diode D2 ..... 3 A
POWER DISSIPATION, P_D at T_A=90°C ..... 15 W
THERMAL RESISTANCE, JUNCTION TO CASE ..... 4°C/W
JUNCTION TEMPERATURE ..... 150°C
OPERATING TEMPERATURE ..... -40° to +85°C
STORAGE TEMPERATURE ..... -55° to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)
from case for 10 s max. ..... 265°C

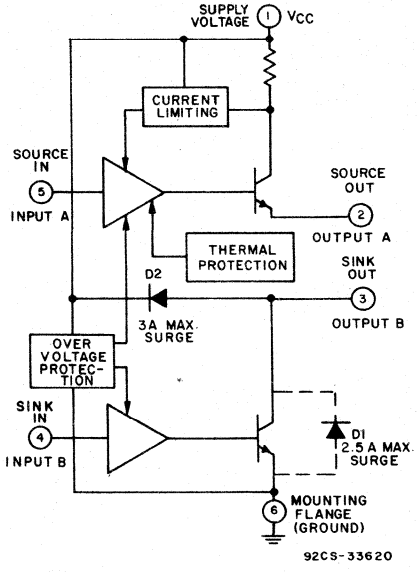
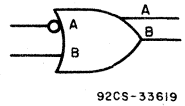


Fig. 1 - 1/2 H driver function diagram.

TRUTH TABLE FOR SOLENOID DRIVER
TTL Logic Conditions: $0 \leq V_L \leq 0.8$, $1.9 \leq V_H \leq 5.5$

INPUT A SOURCE IN	INPUT B SINK IN	OUTPUT A SOURCE OUT	OUTPUT B SINK OUT
V_L	V_L	HIGH (ON)	LOW (ON)
V_L	V_H	HIGH (ON)	(OFF)
V_H	V_L	(OFF)	LOW (ON)
V_H	V_H	(OFF)	(OFF)



CA3169

ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=10.5 V to 18 V
Unless otherwise specified

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Output Leakage Current, Pin 2 See Fig. 6	Inputs Open V_{CC}=4 V to 18 V Source and Sink Loads=20 Ω	-110	±0.5	110	μA
Output Leakage Current, Pin 3 See Fig. 6	Inputs Open V_{CC}=4 V to 18 V Source and Sink Loads=20 Ω	-110	±0.5	110	μA
Thermal Resistance, Junction to Case θ_{JC}		—	3	4	°C/W
Quiescent Current, Pin 1 See Fig. 5	Device "ON" Input Terminals Shorted, V_{CC}=14 V	—	70	100	mA
Quiescent Current, Pin 1 See Fig. 4	Device "OFF" Input Terminals Open, V_{CC}=14 V	—	17	40	mA
Thermal Shutdown Temperature	R_L=Short Circuit	128	140	162	°C
Overvoltage Shutdown-Circuit Upper Trip Point, Pin 1 Voltage See Fig. 8	R_L=20 Ω	20	25	27	V
Overvoltage Shutdown-Circuit Lower Trip Point, Pin 1 Voltage See Fig. 8	R_L=20 Ω	18	21.4	23	V
Input Logic Levels; Source Input - Pin 5, Sink Input - Pin 4					
Input Low Threshold Sink or Source V_{IL}	V_{CC}=14 V **See Note 1**	—	0.4	0.8	V
Input High Threshold Sink or Source V_{IH}	V_{CC}=14 V **See Note 2**	1.9	2.4	—	V
Input Low Current Sink or Source I_{LL}	$V_{IN} \leq$ 0.4 V	−0.9	−0.3	—	mA
Input High Current Sink or Source I_{IH}	$V_{IN} \leq$ 5.5 V	−110	−23	110	μA

NOTE 1: I_{SOURCE} or $I_{SINK} \leq$ 600 mA, $V_{OS} \leq$ 1.5 V, $V_{SINK} \leq$ 0.75 V.
NOTE 2: I_{SOURCE} or $I_{SINK} \leq$ 100 μA, V_{SOURCE} = GND, for V_{SINK} 20 Ω to V_{CC}.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Source Outputs					
Output Voltage, V_{OS} Pin 2 **See Note 3** See Fig. 7	Referenced to V_{CC} with I_{SOURCE}= 600 mA	—	1	1.6	V
Short-Circuit Current Limit, Pin 2 to Ground		0.65	1.11	2.6	A
Turn-On Delay to Output-On, Pin 2	C_L=100 pF, R_L=33 Ω	—	0.45	5.6	μs
Turn-Off Delay to Output-Off Pin 2	C_L=100 pF, R_L=33 Ω	—	5	55	μs
Sink Outputs					
Output Saturation Voltage V_3 **See Note 3** See Fig. 10	I_{SINK}=600 mA, $V_{IN} \leq$ 0.4 V	—	0.3	0.85	V
Output Saturation Voltage V_3 **See Note 3** See Fig. 10	I_{SINK}=1000 mA $V_{IN} \leq$ 0.4 V	—	0.8	1.65	V
Turn-On Delay to Output-On Pin 3 (T_{ON})	C_L=100 pF, R_L=33 Ω to V_{CC}	—	0.45	5.6	μs
Turn-Off Delay to Output-Off Pin 3 (T_{OFF})	C_L=100 pF, R_L=33 Ω to V_{CC}	—	0.95	25	μs

NOTE 3: Measured over temperature range of −40°C to 85°C.

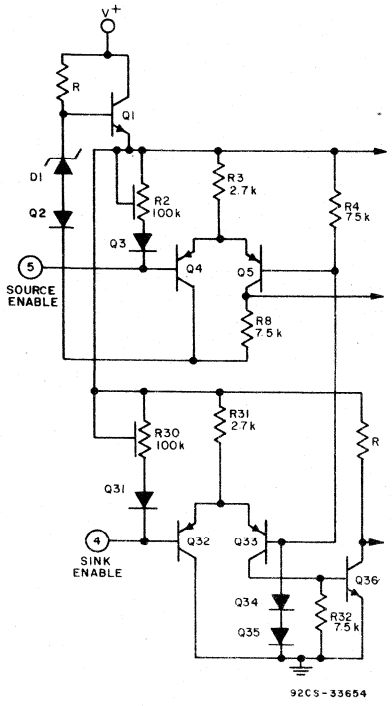


Fig. 2 - Detailed schematic of the input circuit for CA3169.

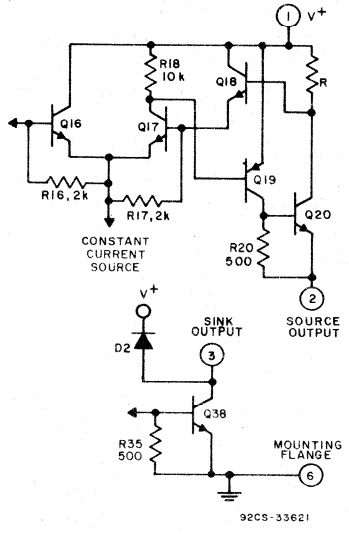


Fig. 3 - Detailed schematic of the output circuit for CA3169.

TEST CIRCUITS
(V_{CC} = V_{IN} = PIN 1 VOLTAGE)

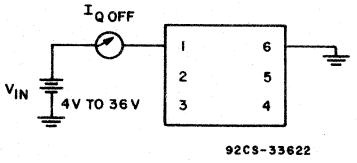


Fig. 4 - Quiescent current device "OFF".

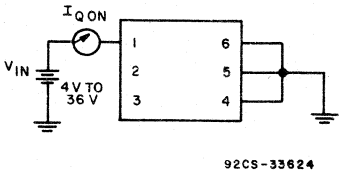


Fig. 5 - Quiescent current device "ON".

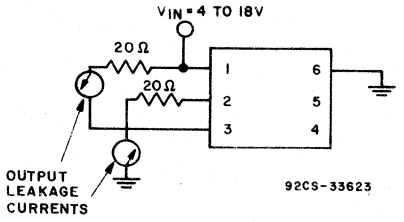


Fig. 6 - Output leakage currents.

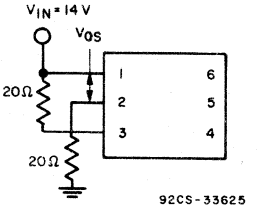
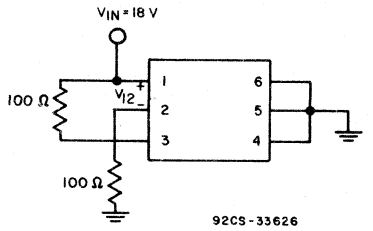


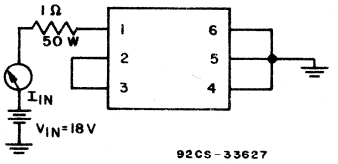
Fig. 7 - Output source voltage (referenced to V_{CC}).



PROCEDURE

1. Measure V_{12}.
2. Increase V_{CC} until $V_{12} \geq 2$ V.
3. Measure V_{CC}; this voltage is the high trip point. Pin 2 should be off; i.e., pin 3 should be high.
4. Observe and measure the voltage at pin 3.
5. Decrease V_{CC} until pin 3 switches, i.e., ≤ 18 V. The supply voltage will be the low trip point voltage.

Fig. 8 - Overvoltage protection.



When V_{CC} is turned on, I_{IN} should be equal to or greater than 1 A. Thermal shutdown will operate properly if the input current drops below 0.5 A (0.3 A typ.) in 10 to 15 seconds. Cover the unit during this test in the event that the thermal shutdown is not operating properly.

Fig. 9 - Thermal shutdown.

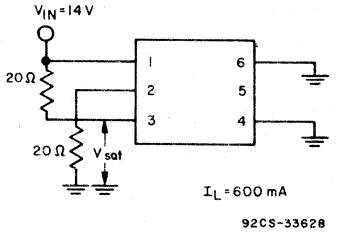
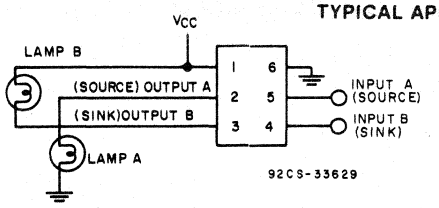


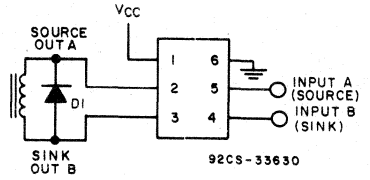
Fig. 10 - Output saturation voltage.

TYPICAL APPLICATIONS



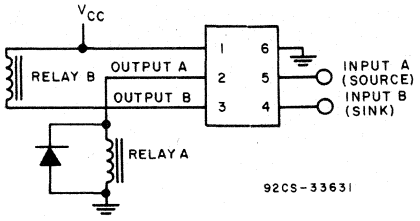
When input A goes low, lamp A will light.
When input B goes low, lamp B will light.

Fig. 11 - Lamp driver.



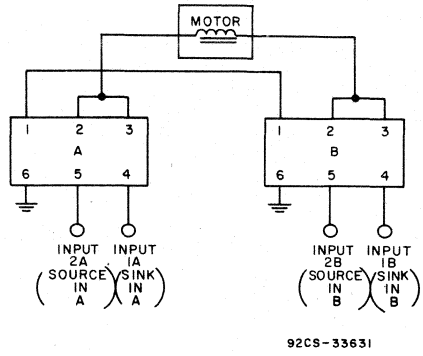
Input A and input B must both be low for the solenoid to switch.

Fig. 12 - Non-latching solenoid.



Relay A will close when input A goes low. Relay B will close when input B goes low. Both relays will close when both inputs go low.

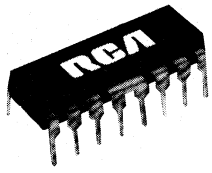
Fig. 13 - Relay driver.



When opposing inputs go low, the motor will switch direction; if source input A and sink input B both go low, current will flow from A to B. If source input B and sink input A both go low, current will flow from B to A.

Fig. 14 - Motor driver or latching solenoid driver.

CA3219E



H-1918

16-Lead Dual-In-Line Webbed Plastic Package ("E" Suffix)

Quad-Power NAND Driver

For Interfacing Low-Level Logic to High Current Loads

Features:

- *Driven outputs capable of switching 600 mA load currents without spurious changes in output state*
- *Inputs compatible with TTL or 5-volt CMOS logic*
- *Suitable for resistive or inductive loads*

The RCA CA3219E• quad power NAND driver contains four NAND gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters, incandescent displays, and vacuum fluorescent displays.

Diodes in the outputs protect the IC against voltage transients due to switching inductive loads.

To allow for maximum heat transfer from the chip, the two center leads are directly connected to the die substrate and to the ground bond pads. In free air, junction-to-air thermal resistance (θJ-A) is 50°C/W* (typical).

The CA3219E is supplied in the 16-lead dual-in-line plastic package with webbed-lead construction.

* This coefficient can be lowered to 40°C/W (typical) by suitable design of the PC board to which the CA3219E is soldered.

•Formerly RCA Dev. Type No. TA10982.

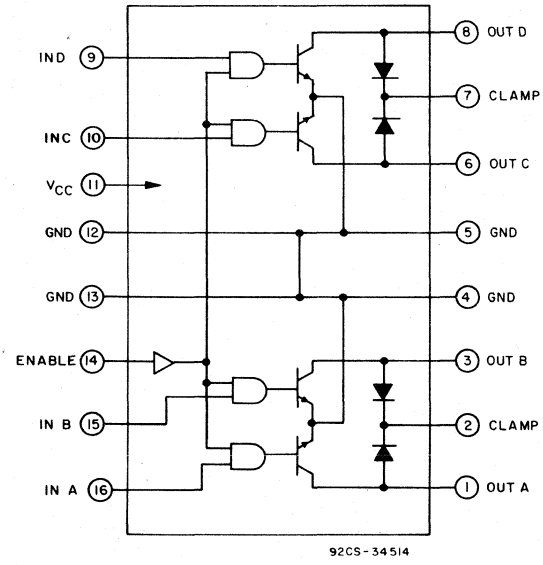


Fig. 1 - Block diagram for the CA3219E.

TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C:*

Logic Supply Voltage (V_{CC}) ..... 7 V
Logic Input Voltage (V_{IN}) ..... 15 V
Output Voltage (V_{CEX}) ..... 50 V_{DC}
Output Sustaining Voltage (V_{CC})sus ..... 35 V_{DC}
Output Current (I_O) ..... 1 ADC
Power Dissipation (P_D)
  Up to 55° C ..... 1.5 W
  Above 55° C ..... derate linearly at 16.6 mW/° C
  Up to 90° C with heat sink ..... derate linearly at 25 mW/° C
Ambient Temperature Range:
  Operating ..... -40 to +85° C
  Storage ..... -55 to +150° C
Maximum Junction Temperature ($T_{\theta J}$) ..... +150° C
Maximum Thermal Resistance
  Junction-to-Air (θ_{J-A}) ..... 60° C/W
  Junction-to-Case (θ_{J-C})
    to pins 4, 5, 12, 13 at seat ..... 12° C/W

ELECTRICAL CHARACTERISTICS at T_A = 25° C, V_{CC} = 5 V

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Output Leakage Current (I_{CEX}) V_{CE} = 50 V V_{IN} = 0.8 V	—	100	μA
Output Sustaining Voltage $V_{CE(sus)}$ I_C = 100 mA V_{IN} = 0.8 V	25	—	V
Collector Emitter Saturation Voltage $V_{CE(sat)}$			
I_C = 100 mA V_{IN} = 2.4 V	—	0.3	V
I_C = 400 mA V_{IN} = 2.4 V	—	0.5	V
I_C = 600 mA V_{IN} = 2.4 V	—	0.7	V
Input Low Voltage V_{IL}	—	0.8	V
Input Low Current I_{IL} V_{IN} = 0.8 V	—	+10	μA
Input High Voltage V_{IH} I_C = 600 mA	2	—	V
Input High Current I_{IH} I_C = 700 mA; V_{IN} = 5.5 V	—	40	μA
Supply Current — All Outputs ON, $I_{CC(ON)}$ I_C = 700 mA; V_{CC} = V_{IH} = 5.5 V	—	80	mA
Supply Current — All Outputs OFF, $I_{CC(OFF)}$	—	5	mA
Clamp Diode Leakage Current I_R V_R = 50 V	—	100	μA
Clamp Diode Forward Voltage V_F			
IF = 1 A	—	1.5	V
IF = 1.5 A	—	2	V
Turn-On Delay t_{PHL} Turn-Off Delay t_{PLH}		30	μs

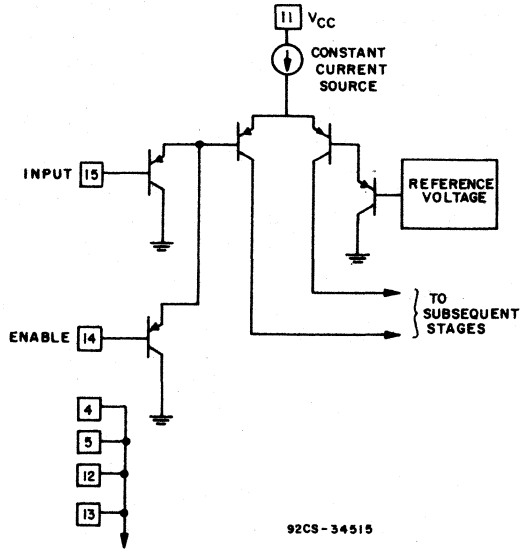
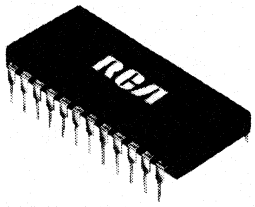


Fig. 2 - Schematic of one input section.



H-1855

24-Lead Dual-In-Line Plastic Package

Speed-Control System

Features

- *Low power dissipation*
- *I^2L control logic*
- *Power-ON reset*
- *On-chip oscillator for system time reference*
- *Single line command*
- *Amplitude encoded control signals*
- *Transient compensated input commands*
- *Controlled acceleration mode*
- *Internal redundant brake and low speed disable*
- *Braking disable*

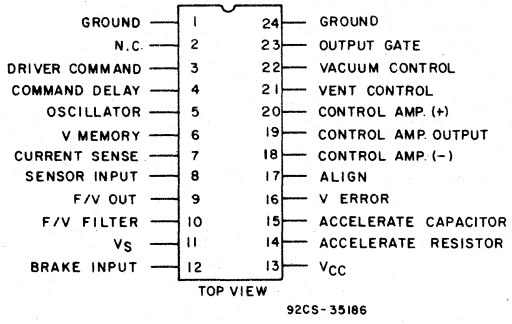
The RCA-CA3228 is a monolithic I^2L integrated circuit designed as an automotive speed-control system.

The system monitors vehicle speed and compares it to a set reference speed. Any deviation in vehicle speed causes a servo mechanism to open or close the engine throttle as required to eliminate the speed error. The reference speed is set by the driver to hold the existing speed and stored in a 9-bit counter.

The reference speed can be altered by the ACCEL and COAST driver commands. The ACCEL command causes the vehicle to accelerate at a controlled rate while the COAST command causes the servo to relax completely forcing the vehicle to slow down. Application of the brake causes the servo to relax immediately and places the system into the standby mode while the RESUME command returns the vehicle to the last stored speed.

Vehicle speed and driver commands are input into the integrated circuit via external sensors. Actuators are needed to convert the output signals into the mechanical action necessary to control vehicle speed.

The CA3228 is supplied in a 24-lead plastic package (E suffix).



TERMINAL ASSIGNMENT

CA3228

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25°C*

DC SUPPLY VOLTAGE RANGE (V_{DD}) ..... 7.4 to 9 V
DC SUPPLY CURRENT RANGE (I_{DD}) ..... 7.5 to 25 mA
POWER DISSIPATION PER PACKAGE:
For T_A=−40°C to 55°C ..... 125 mW
For T_A=55°C to 70°C ..... Derate linearly at 3.3 mW/°C
TEMPERATURE RANGE:
OPERATING ..... −40 to +85°C
STORAGE ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

SWITCHING CHARACTERISTICS, *T_A=25°C, V_{DD}=7.4 to 9 V*

ACCEL Input Hold Time ..... 50 ms
COAST Input Hold Time ..... 50 ms
RESUME Input Hold Time ..... 330 ms
ON Input Hold Time ..... 50 ms
OFF Input Hold Time ..... 50 ms
INTERNAL OSCILLATOR FREQUENCY:
C=0.005 μF at Pin 5 ..... 10,000 Hz
Speed Input Frequency ..... 32 to 222 Hz

SYSTEM PERFORMANCE, *T_A=25°C, V_{DD}=8.2 V, f_M=10 kHz, f_S=2.22 Hz/mph*

SPEED RESOLUTION ..... 0.45 mph
MINIMUM OPERATING SPEED ..... 25 mph
MAXIMUM STORED SPEED ..... 100 mph
REDUNDANT BRAKE SPEED ..... 11 mph

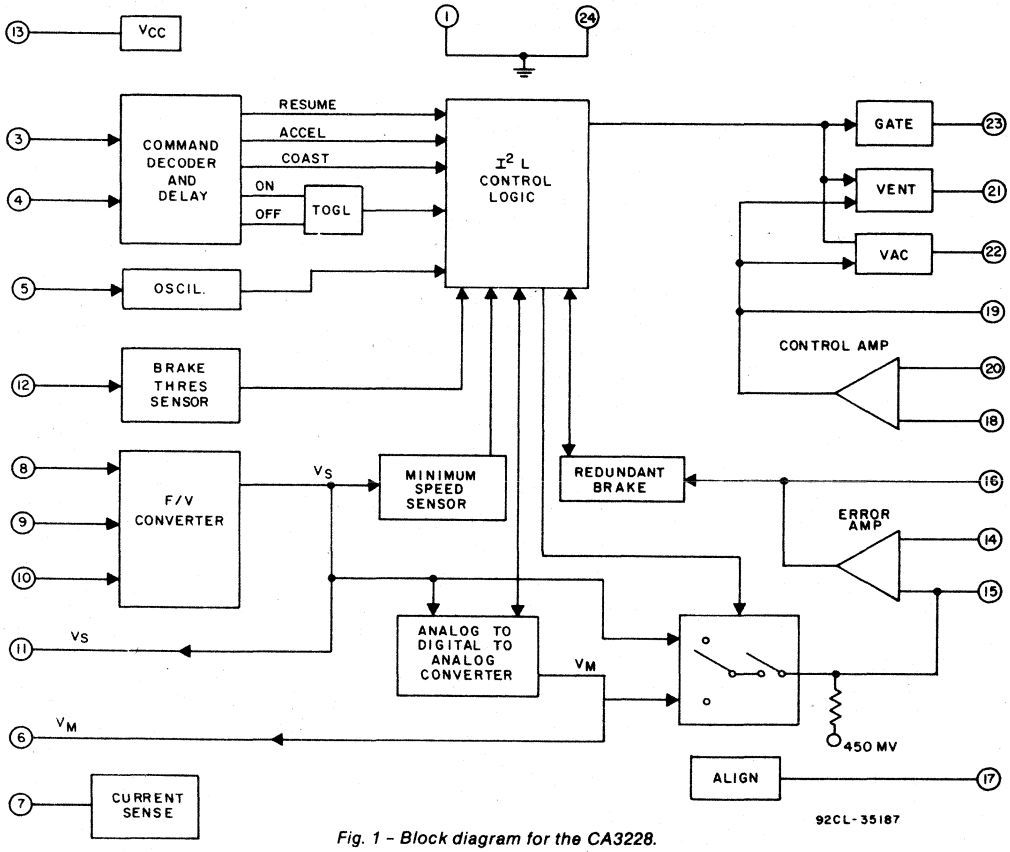


Fig. 1 - Block diagram for the CA3228.

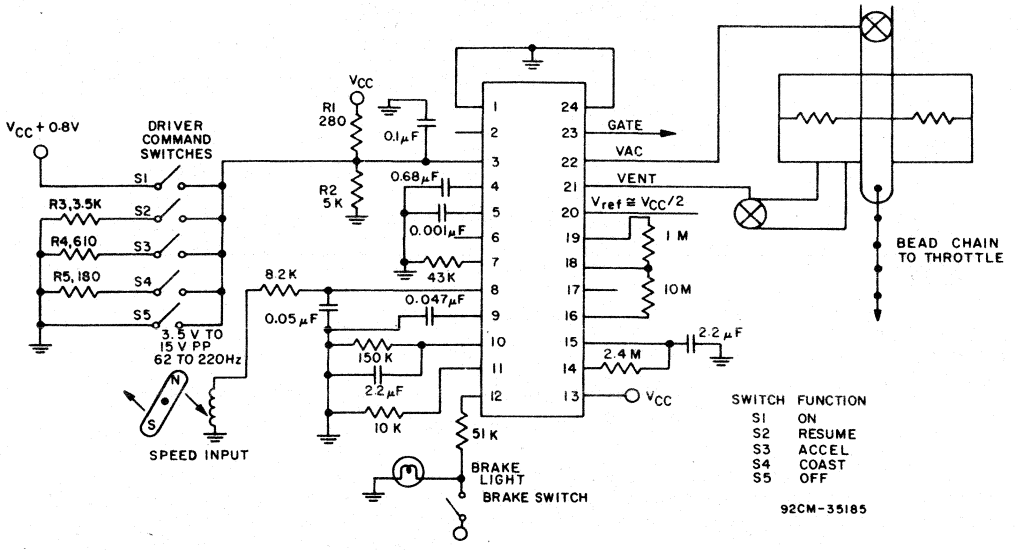


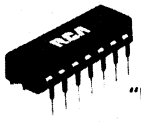
Fig. 2 - Typical automotive speed-control application.

CA723, CA723C Types

"T" Suffix

10-Lead TO-5

H-1384



"E" Suffix

14-Lead Dual-In-Line Plastic Package

H-1517

Voltage Regulators

For Regulated Output Voltages Adjustable from 2 V to 37 V at Output Currents up to 150 mA Without External Pass Transistors

Features:

- *Up to 150 mA output current*
- *Positive and negative voltage regulation*
- *Regulation in excess of 10A with suitable pass transistors*
- *Input and output short-circuit protection*
- *Load and line regulation: 0.03%*
- *Direct replacement for 723 and 723C industry types*
- *Adjustable output voltage: 2 to 37 V*

Applications:

- *Series and shunt voltage regulator*
- *Floating regulator*
- *Switching voltage regulator*
- *High-current voltage regulator*
- *Temperature controller*

RCA-CA723 and CA723C are silicon monolithic integrated circuits designed for service as voltage regulators at output voltages ranging from 2 to 37 volts at currents up to 150 milliamperes.

Each type includes a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and a current-limiting circuit. They also provide independently accessible inputs for adjustable current limiting and remote shutdown and, in addition, feature low standby current drain, low temperature drift, and high ripple rejection.

The CA723 and CA723C may be used with positive and negative power supplies in a wide variety of series, shunt, switching, and floating regulator applications. They can provide regulation at load currents greater than 150 milliamperes and in excess of 10 amperes with the use of suitable n-p-n or p-n-p external pass transistors.

The CA723 and CA723C are supplied in the 10-lead TO-5-style package (T suffix), and the 14-lead dual-in-line plastic package (E suffix), and are direct replacements for industry types 723, 723C, μA723, and μA723C in packages with similar terminal arrangements. They are also available in chip form ("H" suffix).

All types are rated for operation over the full military-temperature range of −55°C to +125°C.

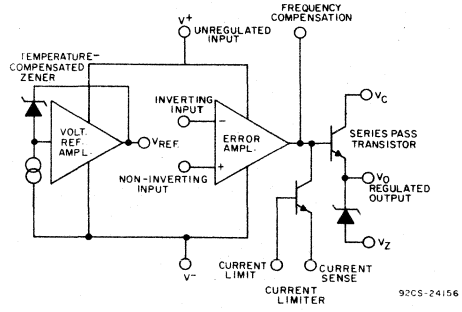


Fig. 1 — Functional diagram of the CA723 and CA723C.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (Between V^+ and V^- Terminals)	40	V
PULSE VOLTAGE FOR 50-ms PULSE WIDTH (Between V^+ and V^- Terminals)	50	V
DIFFERENTIAL INPUT–OUTPUT VOLTAGE	40	V
DIFFERENTIAL INPUT VOLTAGE: Between Inverting and Non-Inverting Inputs	±5	V
Between Non-Inverting Input and V^-	8	V
CURRENT FROM ZENER DIODE TERMINAL (V_Z)	25	mA
CURRENT FROM VOLTAGE REFERENCE TERMINAL (V_{REF})	15	mA

DEVICE DISSIPATION:		
Up to T_A = 25°C –		
CA723T, CA723CT	800	mW
CA723E, CA723CE	1000	mW
Above T_A = 25°C –		
CA723T, CA723CT Derate linearly	6.3	mW/°C
CA723E, CA723CE Derate linearly	8.3	mW/°C
AMBIENT TEMPERATURE RANGE (All Types):		
Operating	–55 to +125	°C
Storage	–65 to +150	°C
LEAD TEMPERATURE (During Soldering): At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

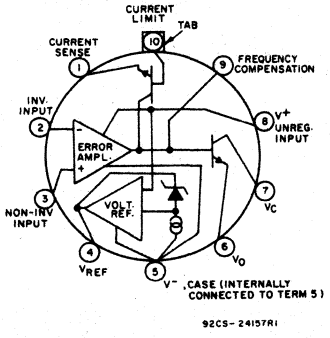


Fig. 2 – Terminal arrangement of the CA723T and CA723CT in the TO-5 style package.

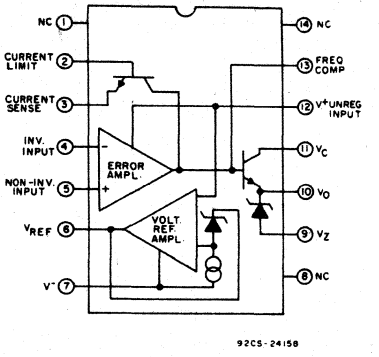


Fig. 3 – Terminal arrangement of the CA723E and CA723CE in the dual-in-line plastic package.

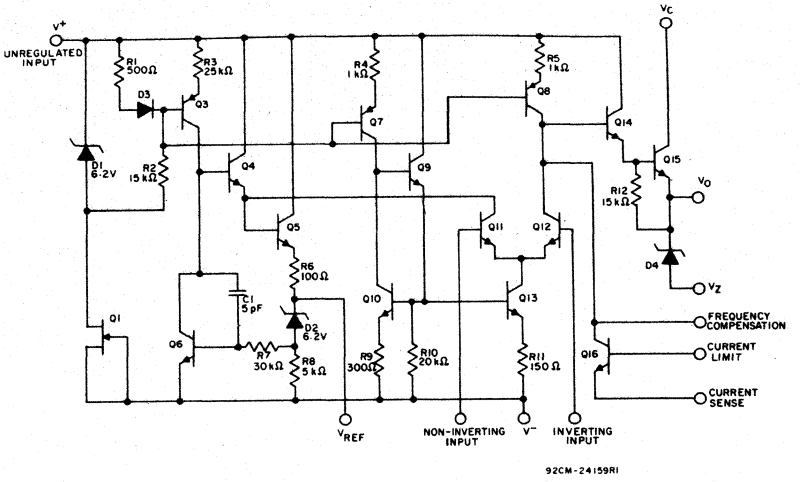


Fig. 4 – Equivalent schematic diagram of the CA723 and CA723C.

CA723, CA723C Types

ELECTRICAL CHARACTERISTICS at T_A = 25 C, $V^+ = V_C = V_I$ = 12 V, V^- = 0, V_O = 5 V, I_L = 1 mA, C_1 = 100 pF, C_{REF} = 0, R_{SCP} = 0, unless otherwise specified. Divider impedance $\frac{R_1R_2}{R_1+R_2}$ at non-inverting input, Term. 5, = 10 kΩ (see Fig. 23).

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA723			CA723C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Quiescent Regulator Current, I_Q	I_L = 0, V_I = 30 V	–	2.3	3.5	–	2.3	4	mA
Input Voltage Range, V_I		9.5	–	40	9.5	–	40	V
Output Voltage Range, V_O		2	–	37	2	–	37	V
Differential Input-Output Voltage, V_I-V_O		3	–	38	3	–	38	V
Reference Voltage, V_{REF}		6.95	7.15	7.35	6.8	7.15	7.5	V
Line Regulation (See Note 1)	V_I = 12 to 40 V	–	0.02	0.2	–	0.1	0.5	%V_O
	V_I = 12 to 15 V	–	0.01	0.1	–	0.01	0.1	
	V_I = 12 to 15 V, T_A = −55 to +125°C	–	–	0.3	–	–	–	
	V_I = 12 to 15 V, T_A = 0 to 70°C	–	–	–	–	–	0.3	
Load Regulation (See Note 1)	I_L = 1 to 50 mA	–	0.03	0.15	–	0.03	0.2	%V_O
	I_L = 1 to 50 mA, T_A = −55 to +125°C	–	–	0.6	–	–	–	
	I_L = 1 to 50 mA, T_A = 0 to 70°C	–	–	–	–	–	0.6	
Output-Voltage Temp. Coefficient, ΔV_O	T_A = −55 to +125°C	–	0.002	0.015	–	–	–	%/°C
	T_A = 0 to 70°C	–	–	–	–	0.003	0.015	
Ripple Rejection (See Note 2)	f = 50 Hz to 10 kHz	–	74	–	–	74	–	dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF	–	86	–	–	86	–	

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA723			CA723C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Short-Circuit Limiting Current, I_{LIM}	R_{SCP} = 10 Ω, V_O = 0	–	65	–	–	65	–	mA
Equivalent Noise RMS Output Voltage, V_N (See Note 2)	BW = 100 Hz to 10 kHz, C_{REF} = 0	–	20	–	–	20	–	μV
	BW = 100 Hz 10 kHz, C_{REF} = 5 μF	–	2.5	–	–	2.5	–	

Note 1: Line and load regulation specifications are given for condition of a constant chip temperature. For high-dissipation conditions, temperature drifts must be separately taken into account.

Note 2: For C_{REF}, see Fig. 23.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723

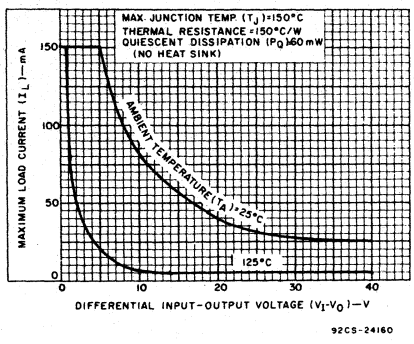


Fig. 5 – Max. load current vs differential input-output voltage.

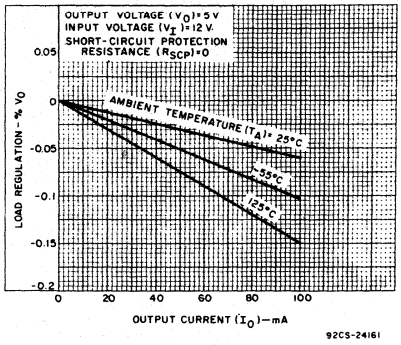


Fig. 6 – Load regulation without current limiting.

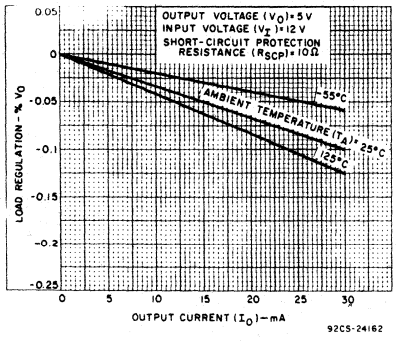


Fig. 7 – Load regulation with current limiting.

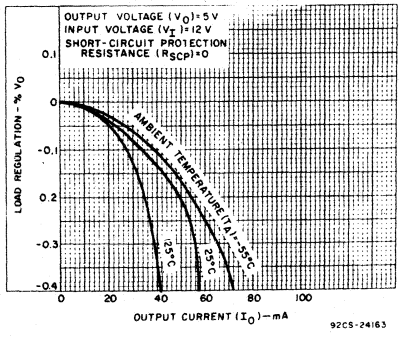


Fig. 8 – Load regulation with current limiting.

CA723, CA723C Types

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723 (Cont'd)

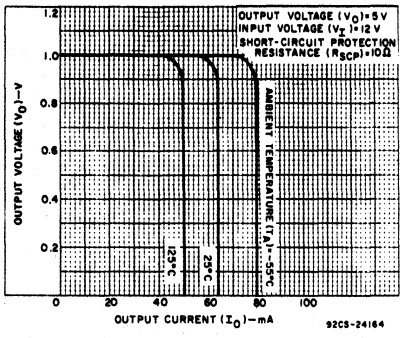


Fig. 9 – Current limiting characteristics.

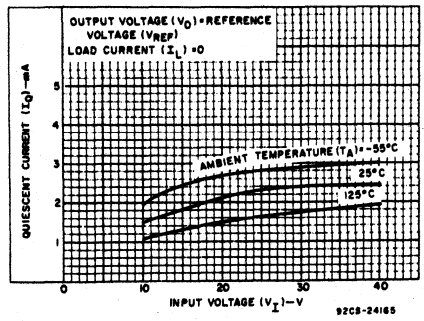


Fig. 10 – Quiescent current vs. input voltage.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723C

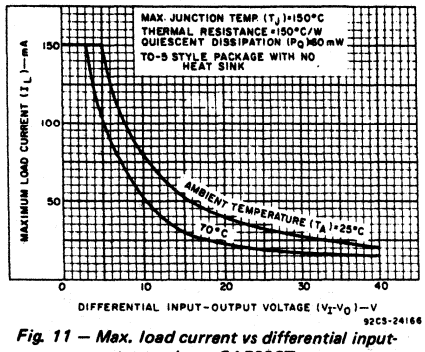


Fig. 11 – Max. load current vs differential input-output voltage CA723CT.

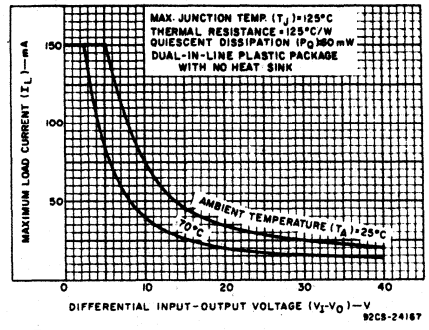


Fig. 12 – Max. load current vs differential input-output voltage for CA723CE.

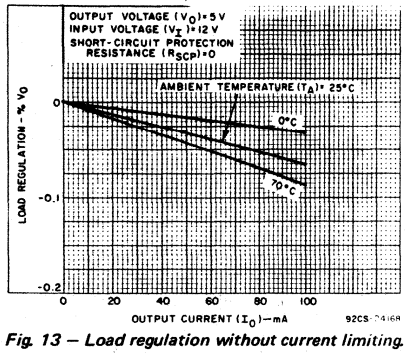


Fig. 13 – Load regulation without current limiting.

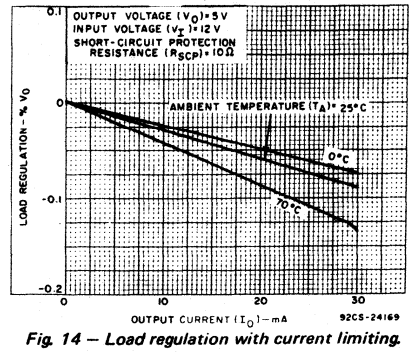


Fig. 14 – Load regulation with current limiting.

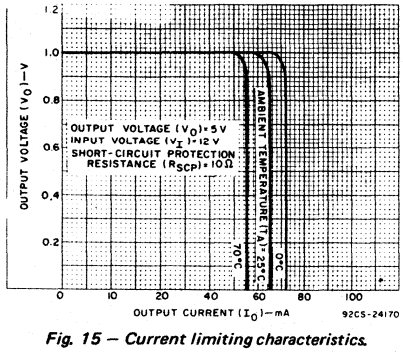


Fig. 15 – Current limiting characteristics.

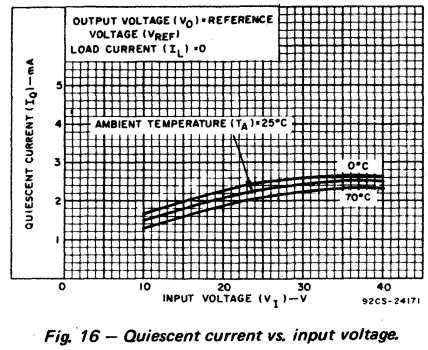


Fig. 16 – Quiescent current vs. input voltage.

TYPICAL CHARACTERISTICS CURVES FOR TYPES CA723 AND CA723C

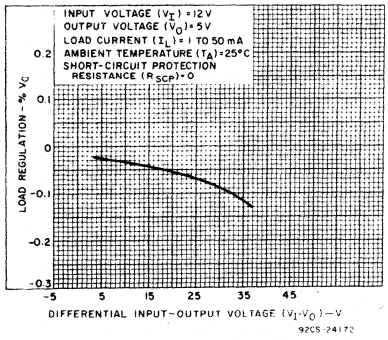


Fig. 17 – Load regulation vs. differential input-output voltage.

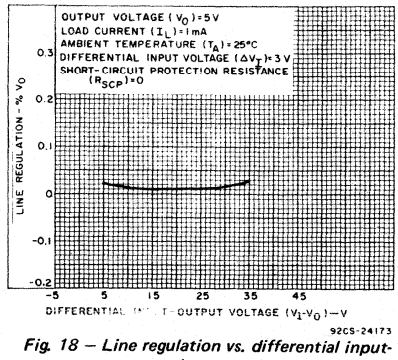


Fig. 18 – Line regulation vs. differential input-output voltage.

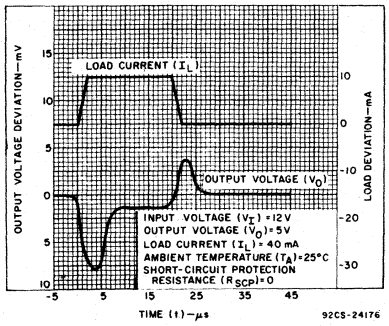


Fig. 19 – Line transient response.

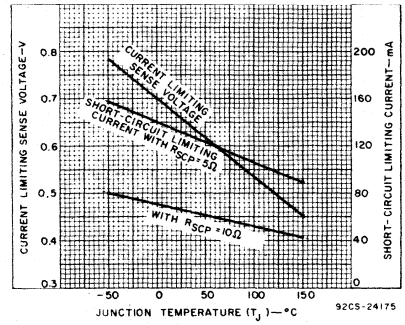


Fig. 20 – Current limiting characteristics vs. junction temperature.

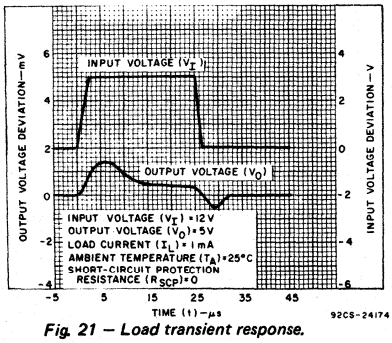


Fig. 21 – Load transient response.

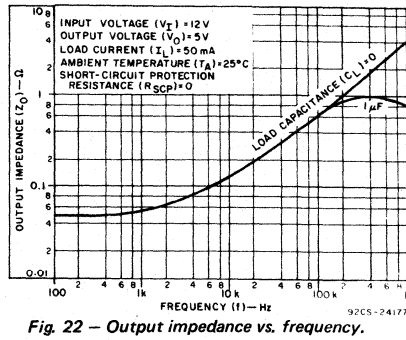


Fig. 22 – Output impedance vs. frequency.

TYPICAL APPLICATION CIRCUITS

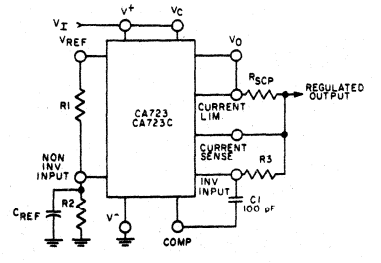


Fig. 23 – Low-voltage regulator circuit (V_O = 2 to 7 volts).

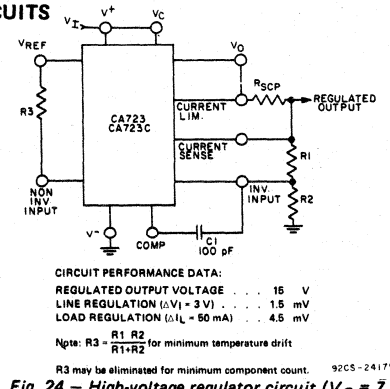
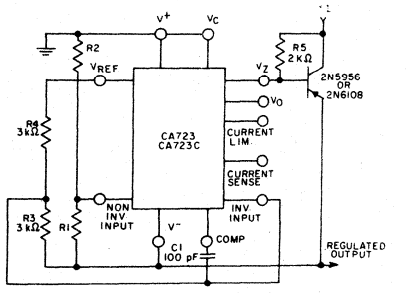


Fig. 24 – High-voltage regulator circuit (V_O = 7 to 37 volts).

TYPICAL APPLICATION CIRCUITS (Cont'd)



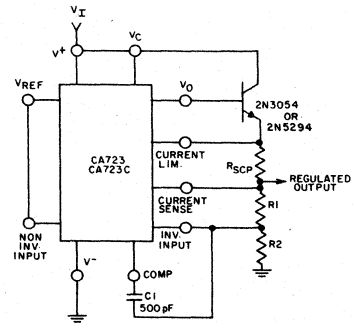
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	−15 V
LINE REGULATION (ΔV_I = 3 V)	1 mV
LOAD REGULATION (ΔI_L = 100 mA)	2 mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

92CS-24180R1

Fig. 25 – Negative-voltage regulator circuit.

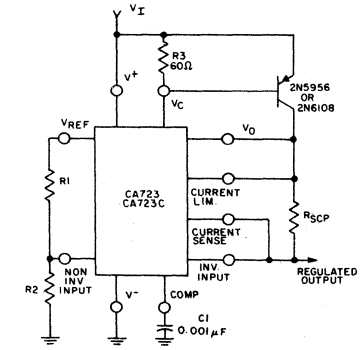


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	15 V
LINE REGULATION (ΔV_I = 3 V)	1.5 mV
LOAD REGULATION (ΔI_L = 1 A)	15 mV

92CS-24181R1

Fig. 26 – Positive-voltage-regulator circuit (with external n-p-n pass transistor).

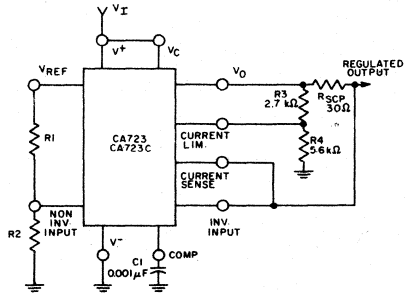


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 1 A)	5 mV

92CS-24182R1

Fig. 27 – Positive voltage-regulator circuit (with external p-n-p pass transistor).

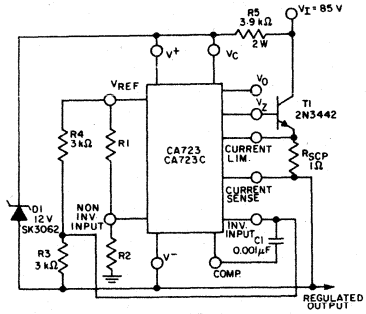


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 10 mA)	1 mV
SHORT-CIRCUIT CURRENT	20 mA

92CS-24183

Fig. 28 – Foldback current-limiting circuit.



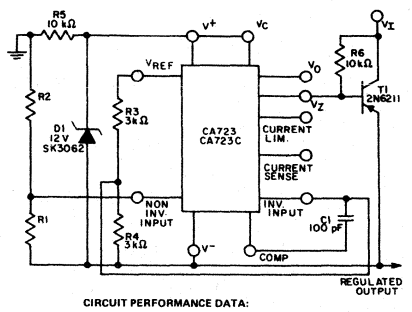
Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	50 V
LINE REGULATION (ΔV_I = 20 V)	15 mV
LOAD REGULATION (ΔI_L = 50 mA)	20 mV

92CS-24184

Fig. 29 – Positive-floating regulator circuit.



CIRCUIT PERFORMANCE DATA:

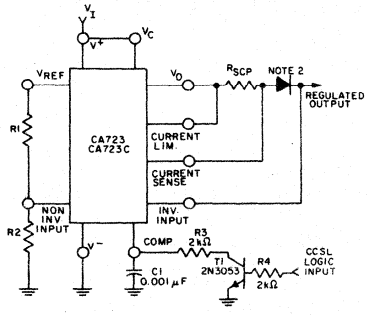
REGULATED OUTPUT VOLTAGE	−100 V
LINE REGULATION (ΔV_I = 20 V)	30 mV
LOAD REGULATION (ΔI_L = 100 mA)	20 mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

92CS-24185

Fig. 30 – Negative-floating regulator circuit.

TYPICAL APPLICATION CIRCUITS (Cont'd)



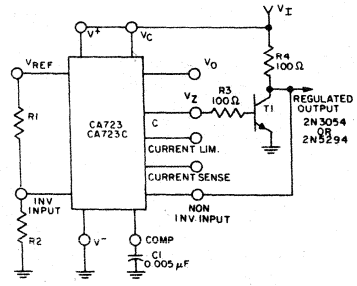
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 50 mA)	1.5 mV

Note 1: A current limiting transistor may be used for shutdown if current limiting is not required.
Note 2: Add a diode if V_O > 10 V.

92CS-24186R1

Fig. 31 – Remote shutdown regulator circuit with current limiting.



CIRCUIT PERFORMANCE DATA:

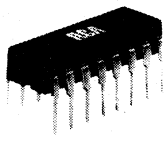
REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 10 V)	0.5 mV
LOAD REGULATION (ΔI_L = 100 mA)	1.5 mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

92CS-24187R1

Fig. 32 – Shunt regulator circuit.

CA1524, CA2524, CA3524 Types



16-Lead Dual-In-Line Plastic Package

H-1611

Regulating Pulse Width Modulator

Features:

- *Complete PWM power control circuitry*
- *Separate outputs for Single-ended or push-pull operation*
- *Line and load regulation of 0.2% typ.*
- *Internal reference supply with 1% max. oscillator and reference voltage variation over full temperature range*
- *Standby current of less than 10 mA*
- *Frequency of operation beyond 100 kHz*
- *Variable output dead time of 0.5 to 5 μs*
- *Low $V_{CE(sat)}$ over the temperature range*

The RCA-CA1524, CA2524, and CA3524 are silicon monolithic integrated circuits designed to provide all the control circuitry for use in a broad range of switching regulator circuits.

The CA1524, CA2524, and CA3524 have all the features of the industry types SG1524, SG2524, and SG3524 respectively. A block diagram of the CA1524 Series is shown in Fig. 1. The circuit includes a zener voltage reference, transconductance error amplifier, precision R-C oscillator, pulse-width modulator, pulse-steering flip-flop, dual alternating output switches, and current-limiting and shutdown circuitry. This device can be used for switching regulators of either polarity, transformer-coupled dc-dc converters, transformerless voltage doublers, dc-ac power inverters, highly efficient variable power supplies, and polarity converters, as well as other power-control applications.

The CA1524 is specified for the military temperature range of −55°C to +125°C.

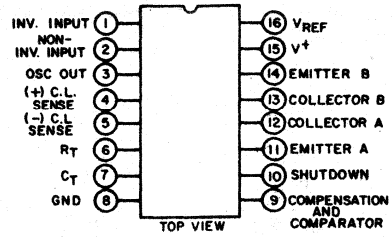
Applications:

- *Positive and negative regulated supplies*
- *Dual-output regulators*
- *Flyback converters*
- *DC-DC transformer-coupled regulating converters*
- *Single-ended DC-DC converters*
- *Variable power supplies*

The CA2524 and CA3524 are specified for the commercial temperature range of 0°C to 70°C. All types operate over a supply voltage range of 8 to 40 V, have a rated operating temperature range of −55°C to +125°C, and are supplied in 16-lead dual-in-line plastic packages (E suffix). The CA3524 is available in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

INPUT VOLTAGE (BETWEEN V_{IN} AND GROUND TERMINALS)	40 V
OPERATING VOLTAGE RANGE (V_{IN} TO GROUND)	8 to 40 V
OUTPUT CURRENT EACH OUTPUT: (TERMINALS 11,12 or 13,14)	100 mA
OUTPUT CURRENT (REFERENCE REGULATOR)	50 mA
OSCILLATOR CHARGING CURRENT	5 mA
DEVICE DISSIPATION:	
Up to T_A = 25°C	1 W
Above T_A = 25°C	Derate linearly 8 mW/°C
OPERATING TEMPERATURE RANGE	−55 to +125°C
STORAGE TEMPERATURE RANGE	−65 to +150°C



TOP VIEW
TERMINAL ASSIGNMENT

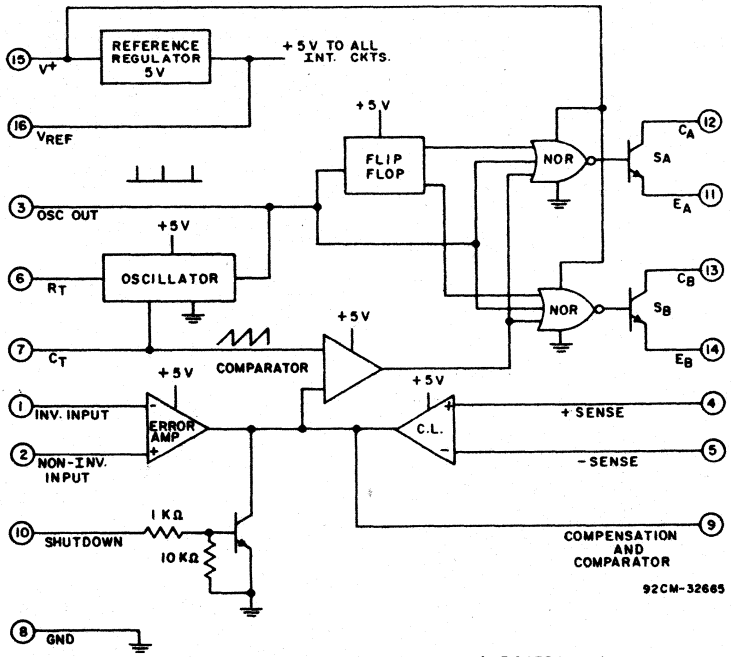


Fig. 1-Functional block diagram of CA1524 series.

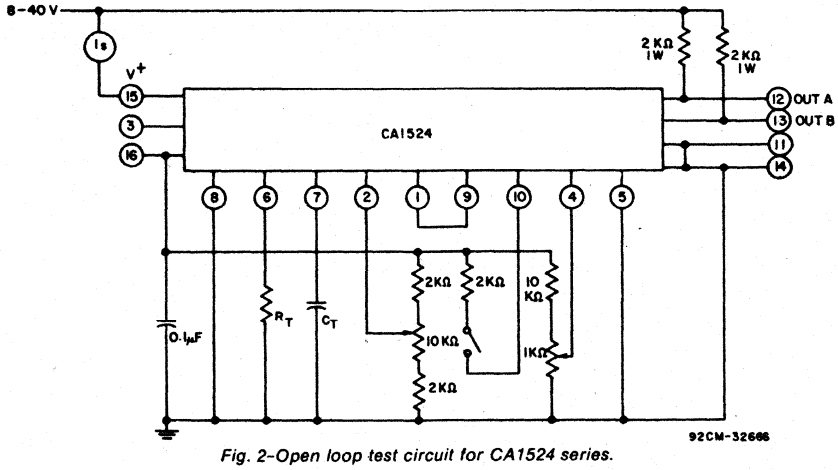


Fig. 2-Open loop test circuit for CA1524 series.

CIRCUIT DESCRIPTION

Voltage Reference Section (see Fig. 3).

The CA1524 Series contains an internal series voltage regulator employing a zener reference to provide a nominal 5 volts output, which is used to bias all internal timing and control circuitry. The output of this regulator is available at terminal 16 and is capable of supplying up to 50 mA. output current. For higher currents, the circuit of Fig. 3 may be used with an external p-n-p transistor and bias resistor. The internal regulator may be bypassed for operation from a fixed 5 volt supply by connecting both terminals 15 and 16 to the input voltage, which must not exceed 6 volts.

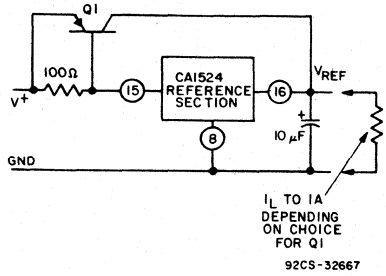


Fig. 3—Circuit for expanding the reference current capability.

Fig. 4 shows the temperature variation of the reference voltage with supply

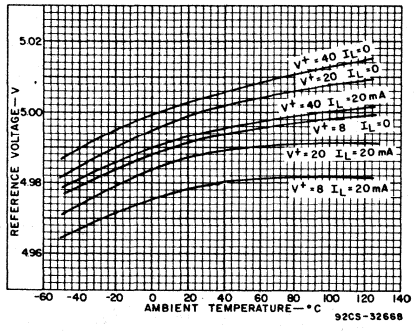


Fig. 4—Typical reference voltage as a function of ambient temperature.

voltages of 8 to 40 volts and load currents up to 20 mA. Load regulation and line regulation curves are shown in Figs. 5 and 6, respectively.

Oscillator Section (see Fig. 3)

Transistors Q42, Q43 and Q44, in conjunction with an external resistor R_T, establishes a constant charging current into an external capacitor C_T to provide a linear ramp voltage at terminal 7. The ramp voltage has a value that ranges from 0.6 to 3.5 volts and is used as the reference for the comparator in the device. The charging current is equal to (5 — $2V_{BE}$)/R_T or approximately 3.6/R_T and should be kept within the range of 30 μA to 2 mA by varying R_T. The discharge time of C_T determines the pulse width of the oscillator output pulse at terminal 3. This pulse has a practical range of 0.5 μs to 5μs for a capacitor range of 0.001 to 0.1 μF. The pulse has two internal uses: as a dead-time control or blanking pulse to the output stages to assure that both outputs

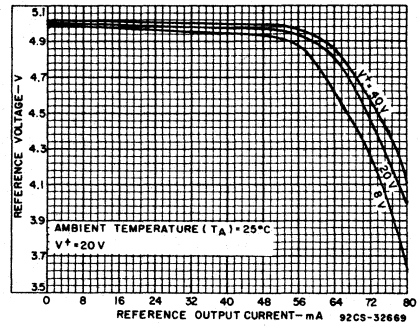


Fig. 5—Typical reference voltage as a function of reference output current.

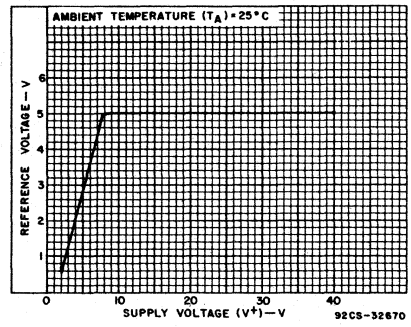


Fig. 6—Typical reference voltage as a function of supply voltage.

cannot be on simultaneously and as a trigger pulse to the internal flip-flop which controls the switching of the output between the two output channels. The output dead-time relationship is shown in Fig. 7. Pulse widths less than 0.5 μs may allow false triggering of one output by removing the blanking pulse prior to a stable state in the flip-flop.

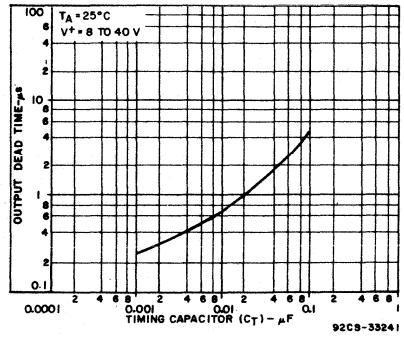


Fig. 7—Typical output stage dead time as a function of timing capacitor value.

ELECTRICAL CHARACTERISTICS *at T_A=-55 to +125°C for CA1524, 0 to +70°C for the CA2524 and CA3524; V^+=20 V and f=20 kHz, unless otherwise stated.*

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA1524, CA2524			CA3524			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section:								
Output Voltage:		4.8	5.0	5.2	4.6	5.0	5.4	V
Line Regulation	V+ = 8 to 40 Volts	—	10	20	—	10	30	mV
Load Regulation	I_L = 0 to 20 mA	—	20	50	—	20	50	mV
Ripple Rejection	f = 120Hz, T_A = 25°C	—	66	—	—	66	—	dB
Short Circuit Current Limit	V_{REF} = 0, T_A = 25°C	—	100	—	—	100	—	mA
Temperature Stability	Over Operating Temperature Range	—	0.3	1	—	0.3	1	%
Long Term Stability	T_A = 25°C	—	20	—	—	20	—	mV/khr
Oscillator Section:								
Maximum Frequency	C_T = 0.001 μF, R_T = 2 KΩ	—	300	—	—	300	—	kHz
Initial Accuracy	R_T and C_T constant	—	5	—	—	5	—	%
Voltage Stability	V+ = 8 to 40 Volts, T_A = 25°C	—	—	1	—	—	1	%
Temperature Stability	Over Operating Temperature Range	—	—	2	—	—	2	%
Output Amplitude	Term.3, T_A = 25°C	—	3.5	—	—	3.5	—	V
Output Pulse Width	C_T = 0.01 μF, T_A = 25°C	—	0.5	—	—	0.5	—	μs
Error Amplifier Section:								
Input Offset Voltage	V_{CM} = 2.5 Volts	—	0.5	5	—	2	10	mV
Input Bias Current	V_{CM} = 2.5 Volts	—	1	10	—	1	10	μA
Open Loop Voltage Gain		72	80	—	60	80	—	dB
Common Mode Voltage	T_A = 25°C	1.8	—	3.4	1.8	—	3.4	V
Common Mode Rejection Ratio	T_A = 25°C	—	70	—	—	70	—	dB
Small Signal Bandwidth	A_V = OdB, T_A = 25°C	—	3	—	—	3	—	MHz
Output Voltage	T_A = 25°C	0.5	—	3.8	0.5	—	3.8	V

If a small value of C_T must be used, the pulse width can be further expanded by the addition of a shunt capacitor in the order of 100 pF but no greater then 1000 pF, from terminal 3 to ground. When the oscillator output pulse is used as a sync input to an oscilloscope, the cable and input capacitances may increase the pulse width slightly. A 2 kΩ resistor at terminal 3 will usually provide sufficient decoupling of the cable. The upper limit of the pulse width is determined by the maximum duty cycle acceptable. To provide an expansion of the dead time without loading the oscillator, the circuit of Fig. 8 may be used.

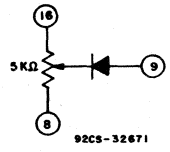


Fig. 8—Circuit for expansion of dead time.

The oscillator period is determined by R_T and C_T, with an approximate value of $t = R_T C_T$, where R_T is in ohms, C_T is in μF, and t is in μs. Excess lead lengths, which produce stray capacitances, should be avoided in connecting R_T and

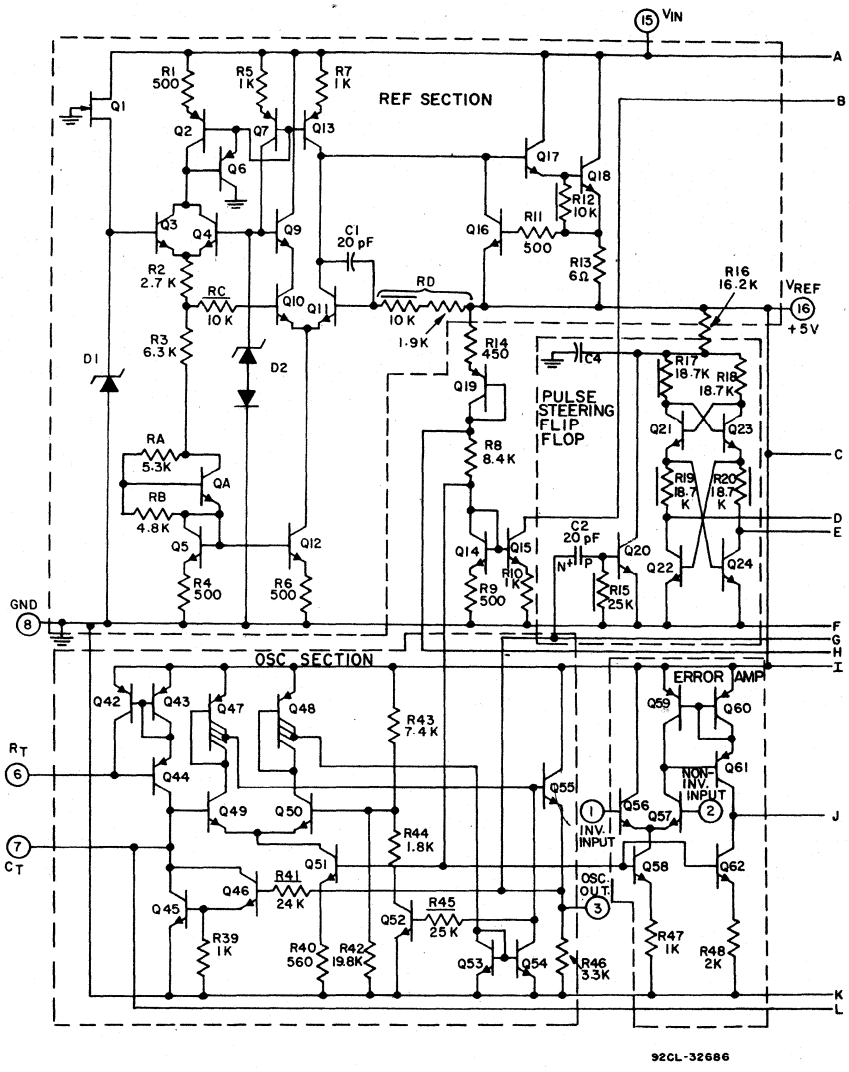


Fig. 9–Schematic diagram (continued on next page).

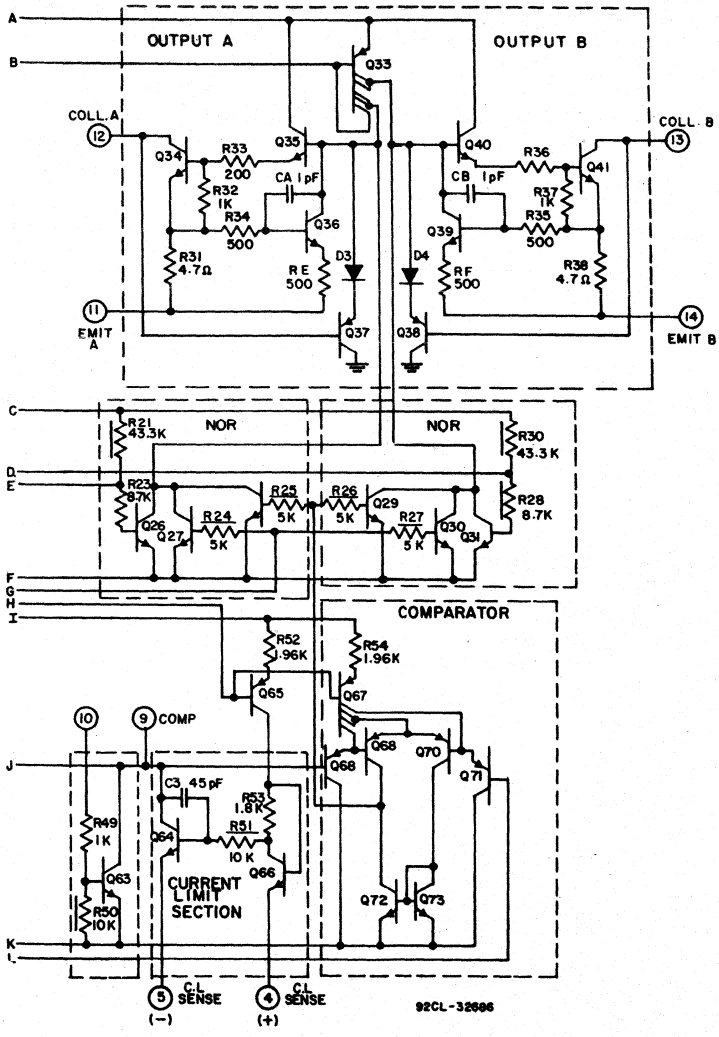


Fig. 9–Schematic diagram (continued from previous page).

ELECTRICAL CHARACTERISTICS *at T_A=-55 to +125°C for CA1524, 0 to +70°C for the CA2524 and CA3524; V^+=20 V and f=20 kHz, unless otherwise stated.*

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA1524, CA2524			CA3524			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Comparator Section:								
Duty Cycle	% Each Output On	0	—	45	0	—	45	%
Input Threshold	Zero Duty Cycle	—	1	—	—	1	—	V
Input Threshold	Max. Duty Cycle	—	3.5	—	—	3.5	—	V
Input Bias Current		—	1	—	—	1	—	μA
Current Limiting Section:								
Sense Voltage	Term. 9 = 2 V with Error Amplifier Set for Max Out, T_A = 25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.		—	0.2	—	—	0.2	—	mV/°C
Common Mode Voltage		-1	—	+1	-1	—	+1	V
Output Section: (Each Output)								
Collector-Emitter Voltage		40	—	—	40	—	—	V
Collector Leakage Current	V_{CE} = 40 V	—	0.1	50	—	0.1	50	μA
Saturation Voltage	V^+ = 40 V, I_C = 50 mA	—	0.8	2	—	0.8	2	V
Emitter Output Voltage	V^+ = 20 V	17	18	—	17	18	—	V
Rise Time	R_C = 2 KΩ T_A = 25°C	—	0.2	—	—	0.2	—	μs
Fall Time	R_C = 2 KΩ T_A = 25°C	—	0.1	—	—	0.1	—	μs
Total Standby Current: *Is	V^+ = 40 V	—	4	10	—	4	10	mA

* Excluding oscillator charging current, error and current limit dividers, and with outputs open.

C_T to their respective terminals. Fig. 10 provides curves for selecting these values for a wide range of oscillator periods. For series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle with the output stage frequency the same as the oscillator frequency. Since the outputs are separate, push-pull and flyback applications are possible. The flip-flop divides the frequency such that the duty cycle of each output is 0-45% and the overall frequency is half that of the oscillator. Curves of the output duty cycle as a function of the voltage at terminal 9 are shown in Fig. 11. To synchronize two or more CA1524's, one must be designated as master, with R_TC_T set for the correct period. Each of the remaining units (slaves) must have a C_T of 1/2 the value used in the master and approximately a 10% longer R_TC_T period than the master. Connecting terminal 3 together on all units assures that the master output pulse, which occurs first and has a wider pulse width, will reset the slave units.

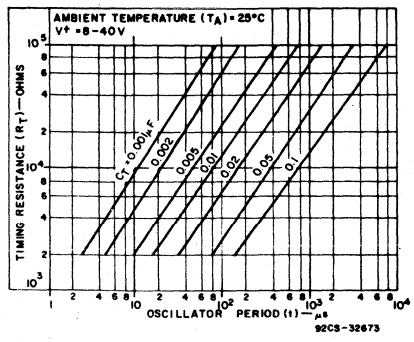


Fig. 10-Typical oscillator period as a function of R_T and C_T.

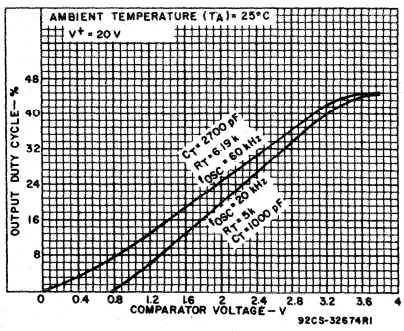


Fig. 11—Typical duty cycle as a function of comparator voltage (at terminal 9).

Error Amplifier Section (see Fig. 9)

The error amplifier consists of a differential pair (Q56, Q57) with an active load (Q61 and Q62) forming a differential transconductance amplifier. Since Q61 is driven by a constant current source, Q62, the output impedance R_{out}, terminal 9, is very high (≅5 MΩ).
The gain is:

$$A_V = g_m R = 8\, I_C\, R / 2KT = 10^4,$$

where $R = \dfrac{R_{out}\, R_L}{R_{out} + R_L}$, $R_L = \infty$, $A_V \cong 10^4$

Since R_{out} is extremely high, the gain can be easily reduced from a nominal 10^4 (80 dB) by the addition of an external shunt resistor from terminal 9 to ground as shown in Fig. 12.

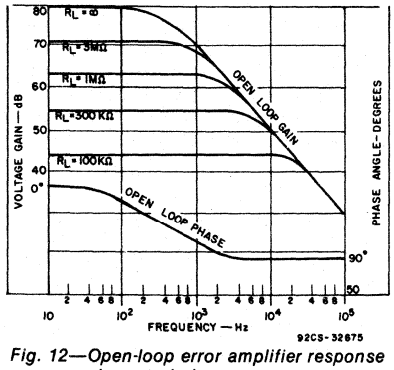


Fig. 12—Open-loop error amplifier response characteristics.

The output amplifier terminal is also used to compensate the system for ac stability. The frequency response and phase shift curves are shown in Fig. 12. The uncompensated amplifier has a single pole at approximately 250 Hz and a unity gain cross-over at 3 MHz.

Since most output filter designs introduce one or more additional poles at a lower frequency, the best network to stabilize the system is a series RC combination at terminal 9 to ground. This network should be designed to introduce a zero to cancel out one of the output filter poles. A good starting point to determine the external poles is a 1000 pF capacitor and a variable series 50 kΩ potentiometer from terminal 9 to ground. The compensation point is also a convenient place to insert any programming signal to override the error amplifier. Internal shutdown and current limiting are also connected at terminal 9. Any external circuit that can sink 200 μA can pull this point to ground and shut off both output drivers.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and will be stable in either the inverting or non-inverting mode. Input common-mode limits must be observed; if not, output signal inversion may result. The internal 5-volt reference can be used for conventional regulator applications if divided as shown in Fig. 13. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

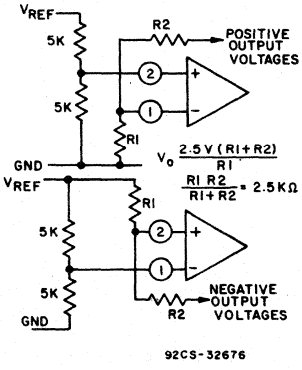


Fig. 13—Error amplifier biasing circuits.

Current Limiting Section (see Fig. 9)

The current limiting section consists of two transistors (Q64, Q66) connected to the error amplifier output terminal. By matching the base-to-emitter voltages of Q64 and Q66 and assuming negligible voltage drop across R51:

$$V_{THRESHOLD} = V_{BE(Q64)} + I_{(Q65)} R_{53} - V_{BE(Q66)}$$
$$= I_{(Q65)} R_{53} \cong 200\ mV$$

Although this circuit provides a small threshold with a negligible temperature coefficient, some limitations to its use must be considered. The circuit has a ±1 volt common mode range which requires sensing in the ground line. The other factor to consider is that the frequency compensation provided by $R_{51}C_3$ and Q64 produces a roll-off pole at approximately 300 Hz.

Due to the low gain of this circuit, there is a transition region as the current-limit amplifier takes over pulse width control from the error amplifier. For testing purposes, the threshold is defined as the input voltage to the current-limiting amplifier to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, terminals 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur (see Fig. 23). Another application is to ground terminal 5 and use terminal 4 as an additional shutdown terminal: i.e. the output will be off with terminal 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Fig. 14. This circuit can reduce the short-circuit current (I_{SC}) to approximately 1/3 the maximum available output current (I_{MAX}).

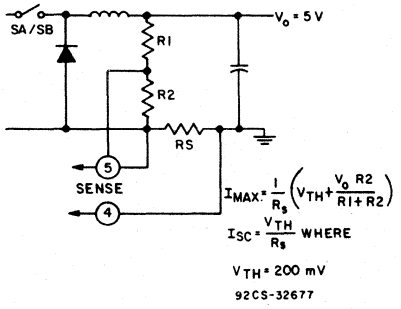


Fig. 14—Foldback current limiting circuit used to reduce power dissipation under shorted output conditions.

Output Section (see Fig. 9)

The CA1524 Series outputs are two identical n-p-n transistors with both collectors and emitters uncommitted. Each output transistor has antisaturation circuitry that enables a fast transient response for the wide range of oscillator frequencies. Current limiting of the output section is set at 100 mA for each output and 100 mA total if both outputs are paralleled. Having both emitters and collector available provides the versatility to drive either n-p-n or p-n-p external transistors. Curves of the output saturation voltage as a function of temperature and output current are shown in Figs. 15 and 16 respectively.

There are a number of output configurations possible in the application of the CA1524 to voltage regulator circuits which fall into three basic classifications:

1. Capacitor-diode coupled voltage multipliers
2. Inductor-capacitor single-ended circuits
3. Transformer-coupled circuits

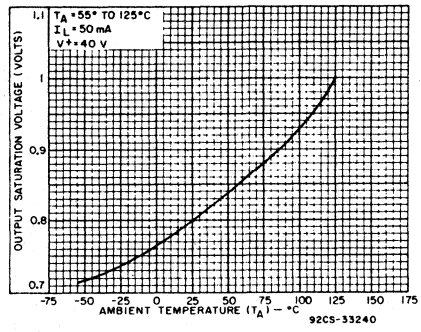


Fig. 15—Typical output saturation voltage as function of ambient temperature.

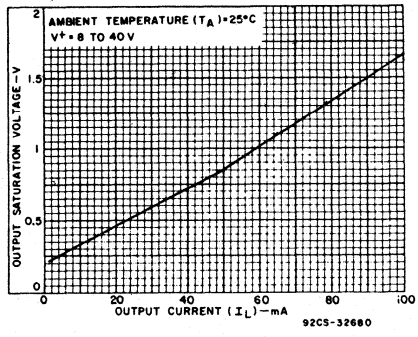


Fig. 16—Typical output saturation voltage as a function of output current.

Examples of these configurations are shown in Fig. 17, 18, and 19. In each case, the switches can be either the output transistors in the CA1524 or added external transistors, depending on the load current requirements.

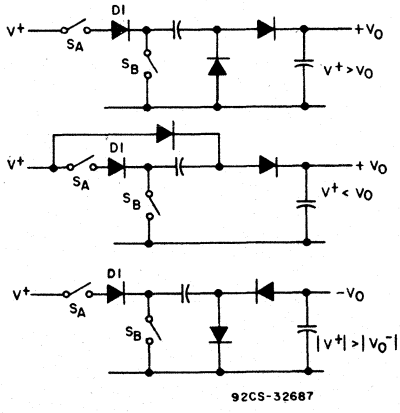


Fig. 17—Capacitor-diode coupled voltage multiplier output stages. (Note: Diode D1 is necessary to prevent reverse emitter-base breakdown of transistor switch S_A).

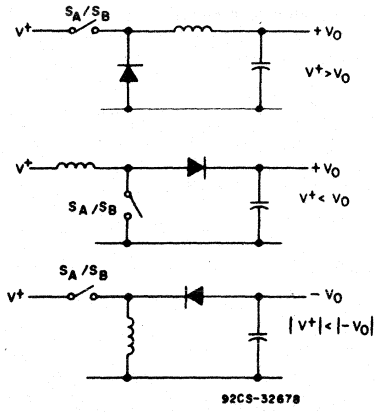


Fig. 18—Single-ended inductor circuits where the two outputs of the 1524 are connected in parallel.

TABLE I - Input vs. Output voltage, and Feedback Resistor Values for I_L = 40 mA. (For capacitor-diode output circuit in Fig. 20)

V_O (V)	R2 (kΩ)	V+ (min.) (V)
-0.5	6	8
-2.5	10	9
-3	11	10
-4	13	11
-5	15	12
-6	17	13
-7	19	14
-8	21	15
-9	23	16
-10	25	17
-11	27	18
-12	29	19
-13	31	20
-14	33	21
-15	35	22
-16	37	23
-17	39	24
-18	41	25
-19	43	26
-20	45	27

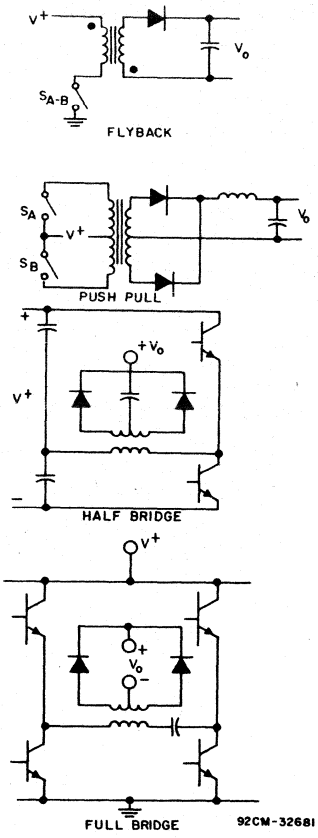


Fig. 19—Transformer-coupled outputs.

APPLICATIONS

Capacitor-Diode Output Circuit

A capacitor-diode output filter is used in Fig. 20 to convert +15 Vdc to −5 Vdc at output currents up to 50 mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table I gives the required minimum input voltage and feedback resistor values, R_2, for an output voltage

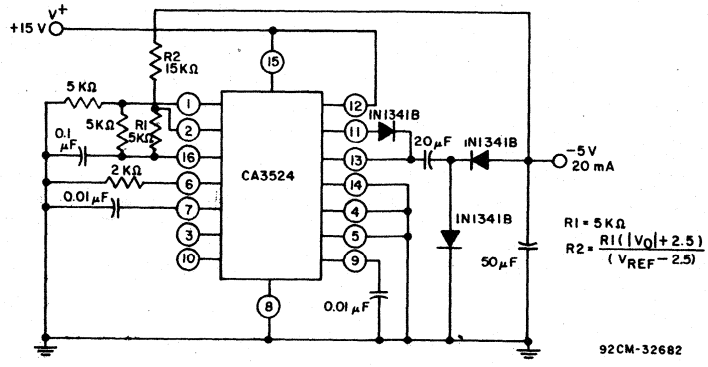


Fig. 20—Capacitor-diode output circuit.

range of −0.5 V to −20 V with an output current of 40 mA.

Single-Ended Switching Regulator

The CA1524 in the circuit of Fig. 21 has both output stages connected in parallel to produce an effective 0-90% duty cycle. Transistor Q1 is pulsed on and off by these output stages. Regulation is achieved from the feedback provided by R1 and R2 to the error amplifier which adjusts the on-time of the output transistors according to the load current being drawn. Various output voltages can be obtained by adjusting R1 and R2. The use of an output inductor requires an R-C phase compensation network to stabilize the system. Current limiting is set at 1.9 amperes by the sense resistor R3.

Flyback Converter

Fig. 22 shows a flyback converter circuit for generating a dual 15-volt output at 20 mA from a 5-volt regulated line. Reference voltage is provided by the input and the internal reference generator is unused. Current limiting in this circuit is accomplished by sensing current in the primary line and resetting the soft-start circuit.

Push-Pull Converter

The output stages of the CA1524 provide the drive for transistors Q1 and Q2 in the push-pull application of Fig. 23. Since the internal flip-flop divides the oscillator frequency by two, the oscillator must be set at twice the output frequency. Current limiting for this circuit is done in the primary of transformer T1 so that the pulse width will be reduced if transformer saturation should occur.

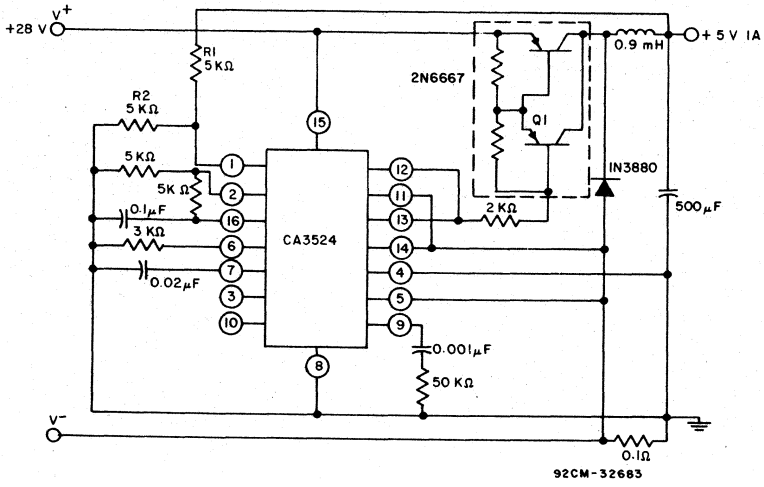


Fig. 21—Single-ended LC switching regulator circuit.

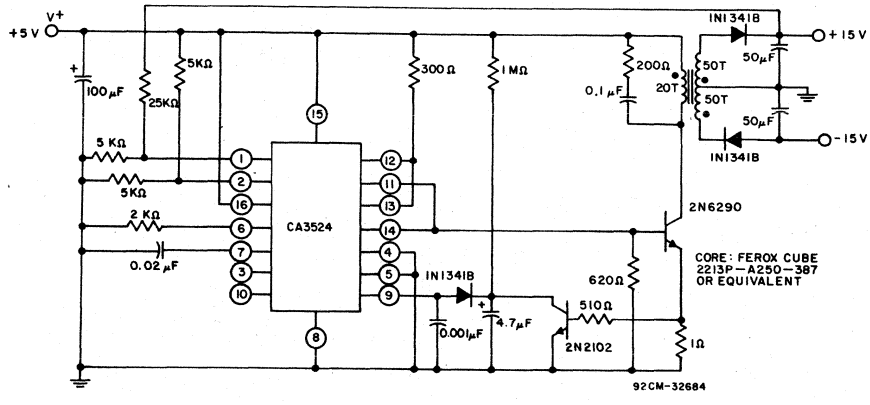


Fig. 22—Flyback converter circuit.

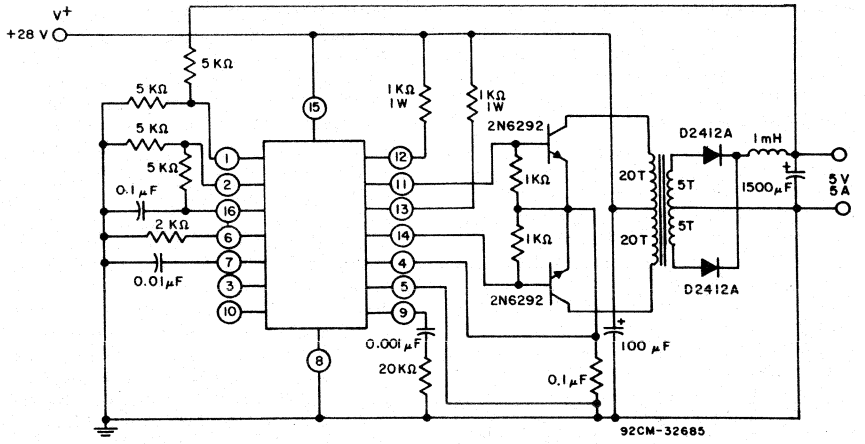


Fig. 23-Push-pull transformer-coupled converter.

Low-Frequency Pulse Generator

Fig. 24 shows the CA1524 being used as a low-frequency pulse generator. Since all components (error amplifier, oscillator, oscillator reference regulator, output transistor drivers) are on the IC, a regulated 5 V (or 2.5 V) pulse of 0%-45% (or 0%-90%) on time is possible over a frequency range of 150 to 500 Hz. Switch S_1 is used to go from a 5-V output pulse (S_1 closed) to a 2.5-V output pulse (S_1 open) with a duty cycle range of 0% to 45%. The output frequency will be roughly half of the oscillator frequency when the output transistors are not connected in parallel (75 Hz to 250 Hz respectively). Switch S_2 will allow both output stages to be paralleled for an effective duty cycle of 0%-90% with the output frequency range from 150 to 500 Hz. The frequency is adjusted by R_1; the duty cycle is controlled by R_2.

Efficient Laboratory Power Supply

The CA1524 as a highly-efficient laboratory supply is shown in Fig. 25. The output voltage can range from 7 to 30 volts for an input voltage range from 33 to 40 volts. Output current of up to 5 amperes is possible. The circuit operates as follows: The two output transistors of the CA1524 are connected in parallel to achieve a maximum duty cycle of 90%. They drive the 2N6650 p-n-p Darlington transistor. The error amplifier's input terminal, pin 1, is first adjusted to 3.4 volts through divider R_3, R_4 and R_5. R_4 is provided so the maximum output can be varied. For this application, the maximum output voltage is 30 volts. The internal reference level of the CA1524's reference regulator is varied, via R_7, over the amplifier's input span. This in turn varies the comparator voltage at pin 9 from a level of 0.5 to 3.8 volts, thus moving the

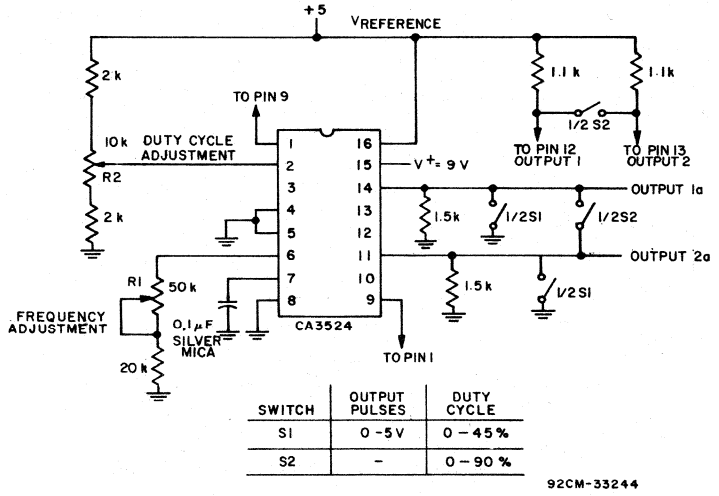


Fig. 24-Low-frequency pulse generator.

output section's on time. Since the reference level is varied, the feedback voltage will track that level and cause the output voltage to change respectively in track with the reference's change at pin 2.

Digital Readout Scale

The CA1524 can be used as the driving source for an electronic scale application. The circuit shown in Figs. 26 and 27 uses half (Q_2) of the CA1524 output in a low-voltage switching regulator (2.2 V) application to drive the LED's displaying the weight. The remaining output stage (Q_1) is used as a driver for the sampling plates PL1 and PL2. Since the CA1524 contains a 5-volt internal regulator and a wide operating range of 8 to 40 volts, a single 9-volt battery can power the total system. The two plates, PL1 and PL2, are driven with opposite phase signals (frequency held constant but duty cycle may change) from the pulse-width modulator IC (1524). The sensor, S, is located between the two plates. Plates PL1, S and PL2 form an effective capacitance bridge-type divider network. As plate S is moved according to the object's weight, a change in capacitance is noted between PL1, S and PL2. This change is reflected as a voltage to the ac amplifier (CA3160). At the null position the signals from PL1 and PL2 as detected by S are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal at S becomes greater. The CA3160 ac amplifier provides a buffer for the small signal change noted at S. The output of the CA3160 is converted to a dc voltage by a peak-to-peak detector. A peak-to-peak detector is needed, since the duty cycle of the sampled waveform is subject to change. The detector output is filtered further and displayed via the CA3161E and CA3162E digital readout system, indicating the weight on the scale.

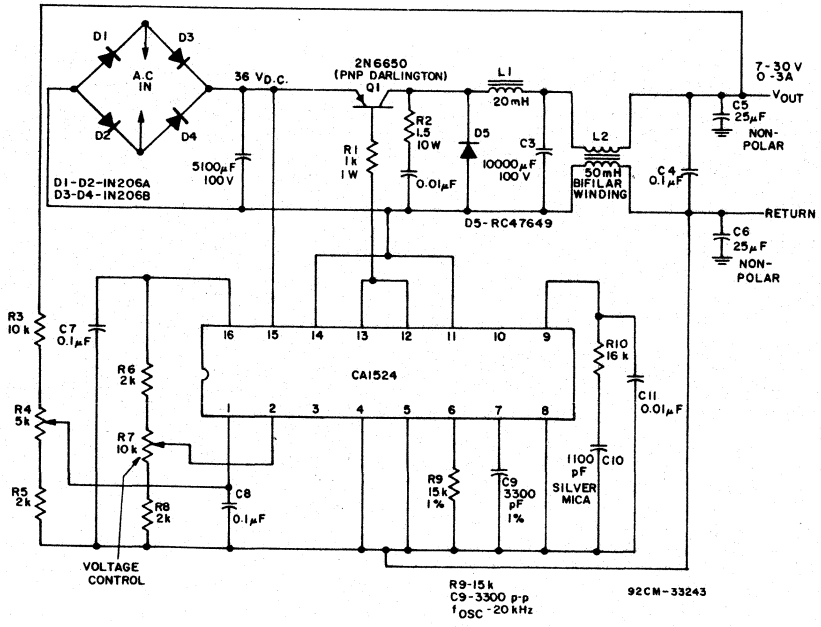


Fig. 25-The CA1524 used as a OA-5A, 7-30-V laboratory supply.

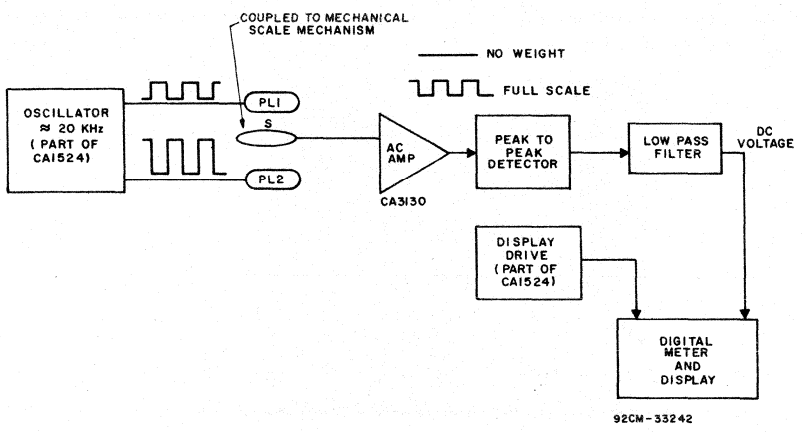


Fig. 26-Basic digital readout scale.

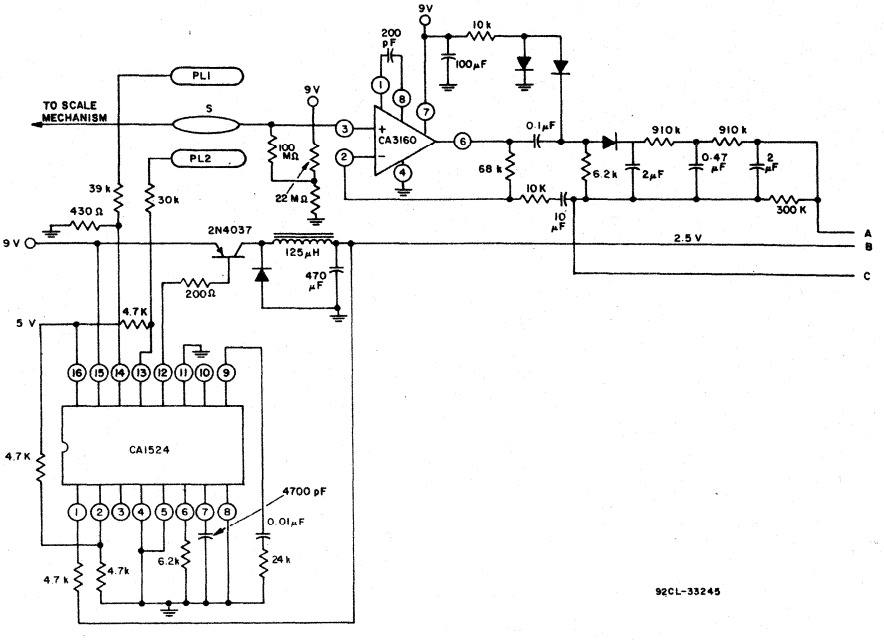
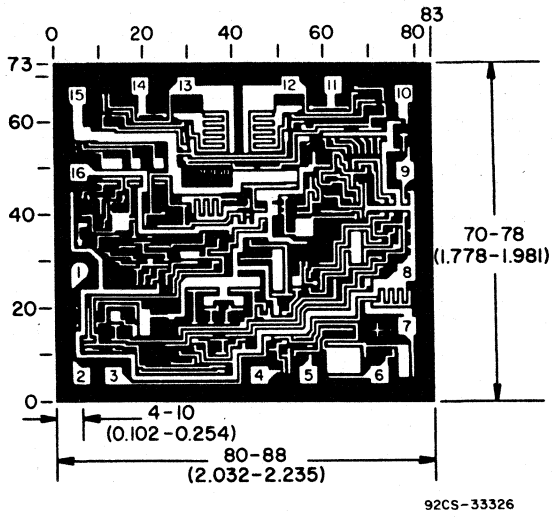


Fig. 27-Schematic diagram of digital readout scale.



Dimensions and pad layout for CA3524H chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

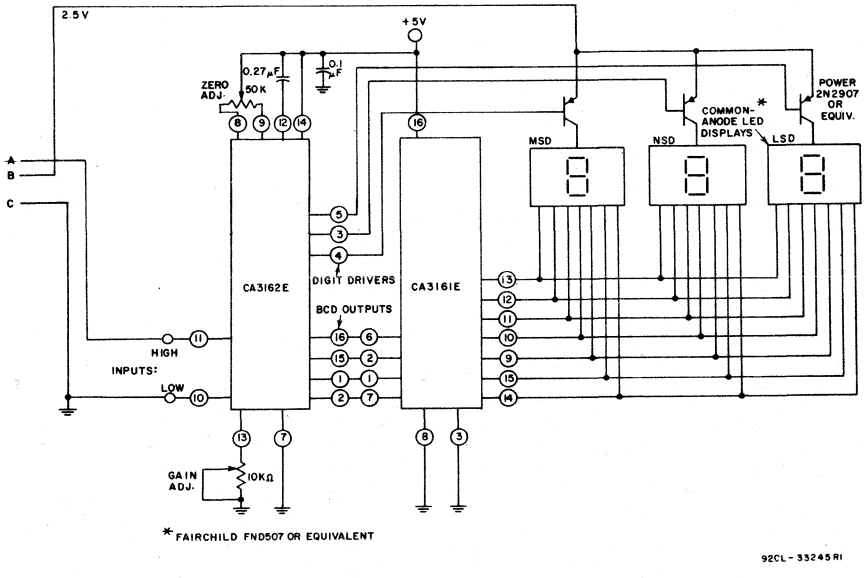
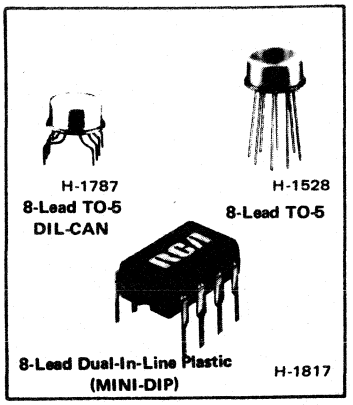


Fig. 27-Schematic diagram of digital readout scale.



Positive Voltage Regulators

For Regulated Voltages from 1.7 V to 46 V
at Currents up to 100 mA

Features

- Up to 100 mA output current
- Input and output short-circuit protection
- Load and line regulation: 0.025%
- Pin compatible with LM100 Series
- Adjustable output voltage

Applications

- Shunt voltage regulator
- Current regulator
- Switching voltage regulator
- High-current voltage regulator
- Combination positive and negative voltage regulator
- Dual tracking regulator

RCA-CA3085, CA3085A, and CA3085B are silicon monolithic integrated circuits designed specifically for service as voltage regulators at output voltages ranging from 1.7 to 46 volts at currents up to 100 milliamperes.

A block diagram of the CA3085 Series is shown in Fig. 1. The diagram shows the connecting terminals that provide access to the regulator circuit components. The voltage regulators provide important features such as: frequency compensation, short-circuit protection, temperature-compensated reference voltage, current limiting, and booster input. These devices are useful in a wide range of applications for regulating high-current, switching, shunt, and positive and negative voltages. They are also applicable for current and dual-tracking regulation.

The CA3085A and CA3085B have output current capabilities up to 100 mA and the CA3085 up to 12 mA without the use of external pass transistors. However, all the devices can provide voltage regulation at load currents greater than 100 mA with the use of suitable external pass transistors. The CA3085 Series has an unregulated input voltage ranging from 7.5 to 30 V (CA3085), 7.5 to 40 V (CA3085A), and 7.5 to 50 V (CA3085B) and a minimum regulated output voltage of 26 V (CA3085), 36 V (CA3085A), and 46 V (CA3085B).

The CA3085A is unilaterally interchangeable with the CA3055.

These types are supplied in the 8-lead TO-5 style package (CA3085, CA3085A, CA3085B, and the 8-lead TO-5 with dual-in-line formed leads ("DIL-CAN", CA3085S, CA3085AS, CA3085BS). The CA3085 is also supplied in the 8-lead dual-in-line plastic package ("MINI-DIP", CA3085E), and in chip form (CA3085H).

Type	V_{IN} Range V	V_{OUT} Range V	Max. I_{OUT} mA	Max. Load Regulation % V_{OUT}
CA3085	7.5 to 30	1.8 to 26	12*	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

* This value may be extended to 100 mA; however, regulation is not specified beyond 12 mA.

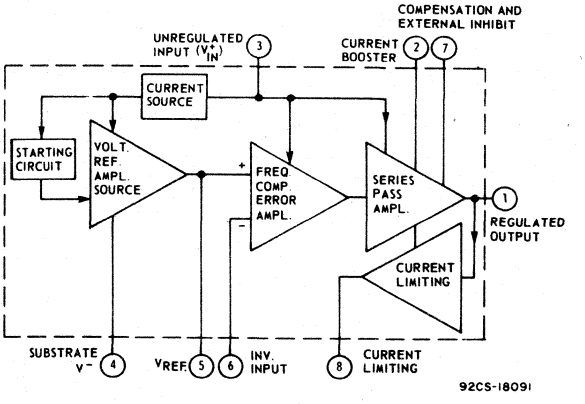


Fig. 1—Block diagram of CA3085 Series.

CA3085, CA3085A, CA3085B Types

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES at T_A = 25°C

POWER DISSIPATION: WITHOUT HEAT SINK

up to T_A = 55°C ..... 630 mW

above T_A = 55°C derate linearly @6.67 mW/°C

WITH HEAT SINK (TO-5 ONLY)

up to T_C = 55°C .... 1.6 W

above T_C = 55°C .... derate linearly at 16.7 mW/°C

TEMPERATURE RANGE:

Operating ..... −55 to +125°C

Storage ..... −65 to +150°C

UNREGULATED INPUT VOLTAGE:

CA3085 ..... 30 V

CA3085A ..... 40 V

CA3085B ..... 50 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal No. 7 and horizontal Terminal No. 1 is +3 to −10 volts.

MAXIMUM VOLTAGE RATINGS

TERMINAL No.	5	6	7	8	1	2	3	4
5	–	+5 −5	•	•	•	•	•	+10 0
6	–	–	•	•	•	•	•	•
7	–	–	–	+3 −10	+3 −10	•	•	+‡ 0
8	–	–	–	–	+5 −1	•	•	•
1	–	–	–	–	–	10 −‡	0 −‡	+‡ 0
2	–	–	–	–	–	–	0 –	+‡ 0
3	–	–	–	–	–	–	–	+‡ 0
4	–	–	–	–	–	–	–	Substrate & Case

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

‡30 V for CA3085
40 V for CA3085A
50 V for CA3085B

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
5	10	1.0
6	1.0	−0.1
7	1.0	−1.0
8	0.1	10
1	20	150
2	150	60
3	150	60
4	–	–

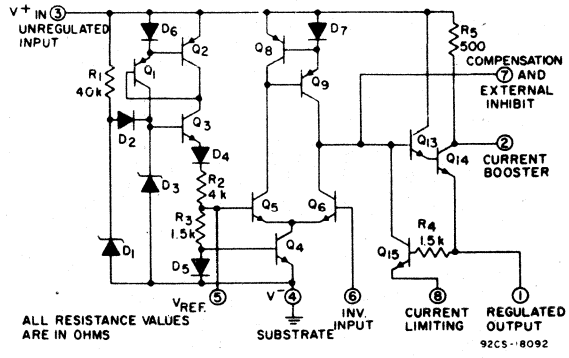


Fig.2—Schematic diagram of CA3085 Series.

CA3085, CA3085A, CA3085B Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: Test Circuit Fig. No.	TEST CONDITIONS: T_A = 25°C [Unless indicated otherwise]		CA3085 MIN.	CA3085 TYP.	CA3085 MAX.	CA3085A MIN.	CA3085A TYP.	CA3085A MAX.	CA3085B MIN.	CA3085B TYP.	CA3085B MAX.	UNITS
Reference Voltage	V_{REF}	4	V^+_{IN} = 15V		1.4	1.6	1.8	1.5	1.6	1.7	1.5	1.6	1.7	V
Quiescent Regulator Current	$I_{quiescent}$	4	V^+_{IN} = 30V		–	3.3	4.5	—	–	–	–	–	–	mA
			V^+_{IN} = 40V		–	–	–	–	3.65	5	–	–	–	
			V^+_{IN} = 50V		–	–	–	–	–	–	–	4.05	7	
Input Voltage Range	$V_{IN(range)}$	–	–		7.5	–	30	7.5	–	40	7.5	–	50	V
Maximum Output Voltage	$V_{O(max.)}$	4	V^+_{IN} = 30,40,50V#; R_L = 365 Ω; Term. No. 6 to Gnd.		26	27	–	36	37	–	46	47	–	V
Minimum Output Voltage	$V_{O(min.)}$	4	V^+_{IN} = 30V		–	1.6	1.8	–	1.6	1.7	–	1.6	1.7	V
Input-Output Voltage Differential	V_{IN}-V_{OUT}	–	–		4	–	28	4	–	38	3.5	–	48	V
Limiting Current	I_{LIM}	7	V^+_{IN} = 16V, V^+_{OUT} = 10V R_{SCP}* = 6 Ω		–	96	120	–	96	120	–	96	120	mA
Load Regulation●	–	–	I_L = 1 to 100mA, R_{SCP} = 0		–	–	–	–	0.025	0.15	–	0.025	0.15	%V_{OUT}
		–	I_L = 1 to 100mA, R_{SCP} = 0 T_A = 0°C to +70°C		–	–	–	–	0.035	0.6	–	0.035	0.6	
		–	I_L = 1 to 12mA, R_{SCP} = 0		–	0.003	0.1	–	–	–	–	–	–	
Line Regulation▲	–	–	I_L = 1 mA, R_{SCP} = 0		–	0.025	0.1	–	0.025	0.075	–	0.025	0.04	%/V
		–	I_L = 1mA, R_{SCP} = 0 T_A = 0°C to +70°C		–	0.04	0.15	–	0.04	0.1	–	0.04	0.08	
Equivalent Noise Output Voltage	V_{NOISE}	11	V^+_{IN} = 25V	C_{REF} = 0	–	0.5	–	–	0.5	–	–	0.5	–	mV p-p
				C_{REF} = 0.22μF	–	0.3	–	–	0.3	–	–	0.3	–	
Ripple Rejection	–	12	V^+_{IN} = 25V f = 1kHz	C_{REF} = 0	–	50	–	–	50	–	45	50	–	dB
				C_{REF} = 2μF	–	56	–	–	56	–	50	56	–	
Output Resistance	r_o	12	V^+_{IN} = 25V, f = 1kHz		–	0.075	1.1	–	0.075	0.3	–	0.075	0.3	Ω
Temperature Coefficient of Reference and Output Voltages	ΔV_{REF}, ΔV_o	–	I_L = 0, V_{REF} = 1.6V		–	0.0035	–	–	0.0035	–	–	0.0035	–	%/°C
Load Transient Recovery Time: Turn On	t_{ON}	16	V^+_{IN} = 25V, +50mA Step		–	1	–	–	1	–	–	1	–	μs
Turn Off	t_{OFF}		V^+_{IN} = 25V, −50mA Step		–	3	–	–	3	–	–	3	–	μs
Line Transient Recovery Time: Turn On	t_{ON}	–	V^+_{IN} = 25V, f = 1kHz, 2V Step		–	0.8	–	–	0.8	–	–	0.8	–	μs
Turn Off	t_{OFF}	–			–	0.4	–	–	0.4	–	–	0.4	–	μs

30V (CA3085), 40V(CA3085A), 50V(CA3085B)

* RSCP: Short-circuit protection resistance

● Load Regulation = $\frac{\Delta V_{OUT}}{V_{OUT(initial)}} \times 100\%$

▲ Line Regulation = $\frac{(\Delta V_{OUT})}{[V_{OUT(initial)}]\ (\Delta V_{IN})} \times 100\%$

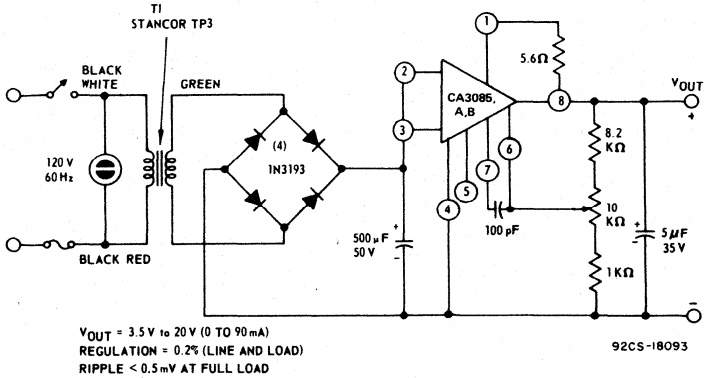
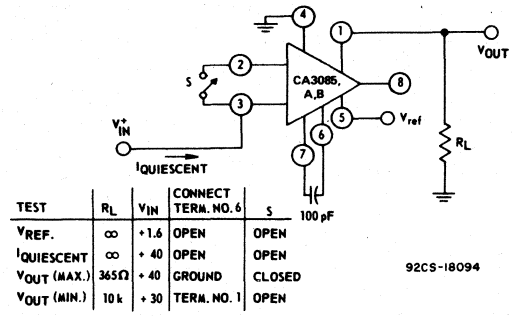


Fig.3—Application of the CA3085 Series in a typical power supply.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES



TEST	R_L	V_{IN}	CONNECT TERM. NO. 6	S
$V_{REF.}$	∞	+1.6	OPEN	OPEN
$I_{QUIESCENT}$	∞	+40	OPEN	OPEN
V_{OUT} (MAX.)	365Ω	+40	GROUND	CLOSED
V_{OUT} (MIN.)	10k	+30	TERM. NO. 1	OPEN

Fig.4—Test circuit for V_{REF}, $I_{quiescent}$, $V_{OUT(max.)}$, $V_{OUT(min.)}$.

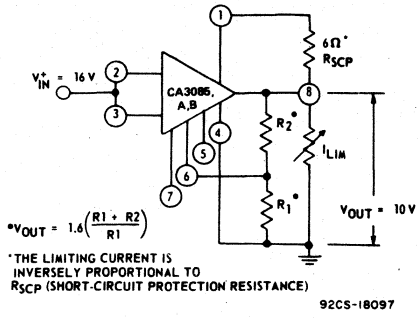


Fig.7—Test circuit for limiting current

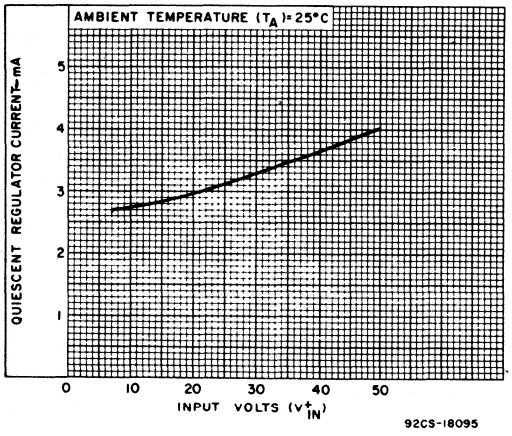


Fig.5—$I_{quiescent}$ vs. V^+_{IN}.

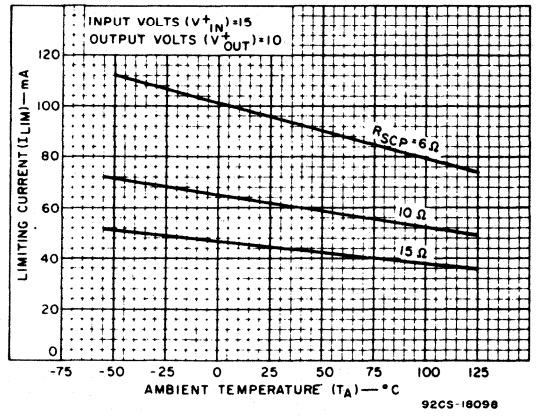


Fig.8—I_{LIM} vs. T_A.

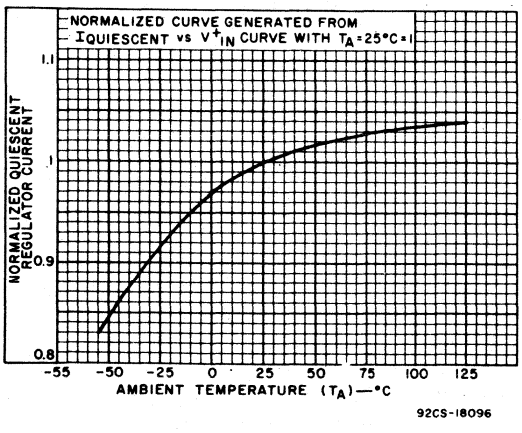


Fig.6—Normalized $I_{quiescent}$ vs. T_A.

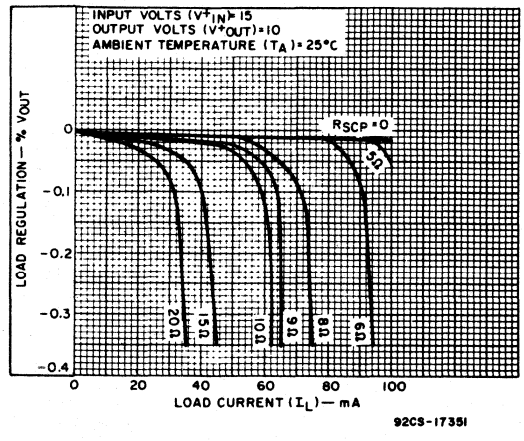


Fig.9—Load regulation characteristics.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES

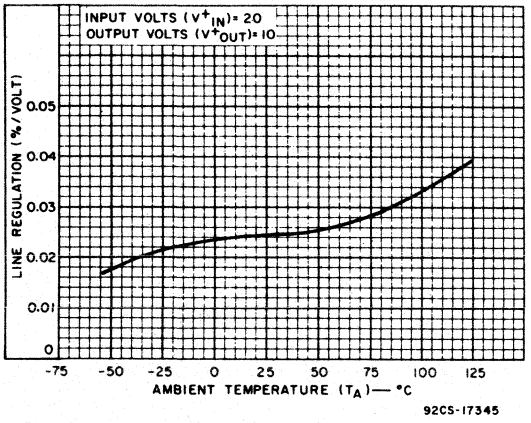


Fig.10—Line regulation temperature characteristics.

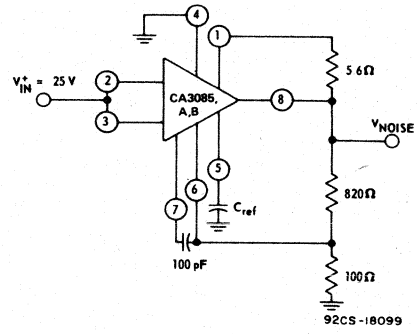


Fig.11—Test circuit for noise voltage.

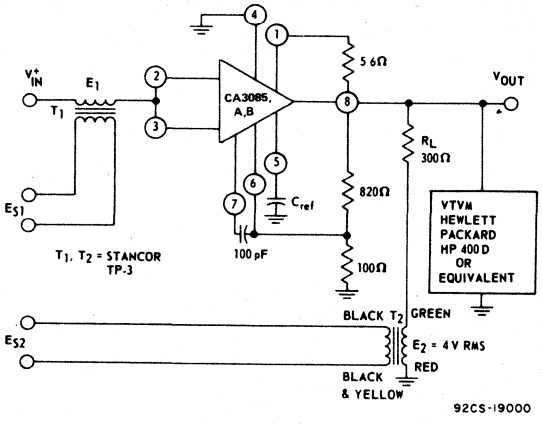


Fig.12—Test circuit for ripple rejection and output resistance.

TEST PROCEDURES FOR TEST CIRCUIT FOR RIPPLE REJECTION AND OUTPUT RESISTANCE

Output Resistance

Conditions:

1. V_{IN} = +25V, C_{REF} = 0, Short E_1
2. Set E_{S2} at 1 kHz so that E_2 = 4V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate R_{OUT} from $R_{OUT} = V_{OUT}(R_L/E_2)$

Ripple Rejection — I

Conditions:

1. V_{IN} = +25V, C_{REF} = 0, Short E_2
2. Set E_{S1} at 1 kHz so that E_1 = 3V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate Ripple Rejection from 20 log (E_1/V_{OUT})

Ripple Rejection — II

Conditions:

1. Repeat Ripple Rejection I with C_{REF} = 2 μF

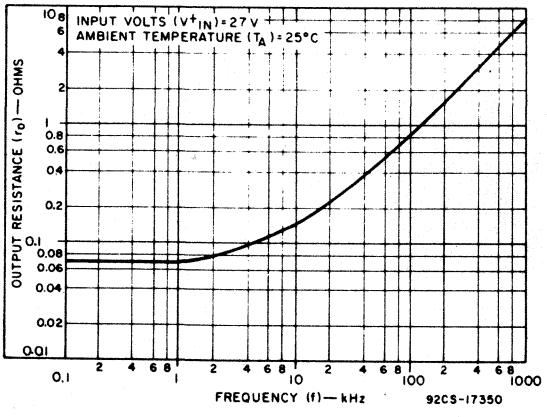


Fig.13—r_O vs. f.

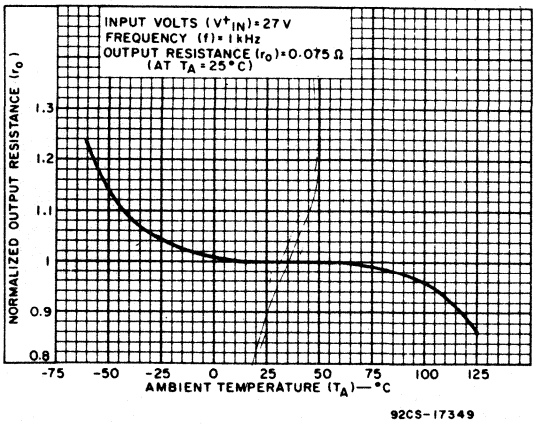


Fig.14—Normalized r_O vs. T_A.

CA3085, CA3085A, CA3085B Types

TEST CIRCUIT AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES

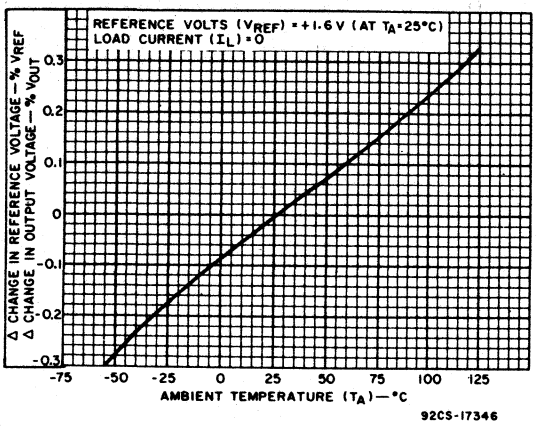


Fig.15—Temperature coefficient of V_{REF} and V_{OUT}.

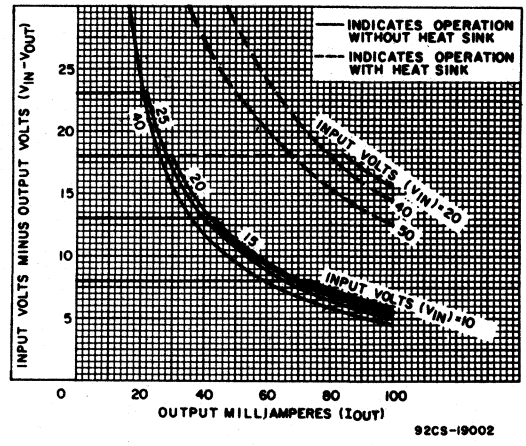
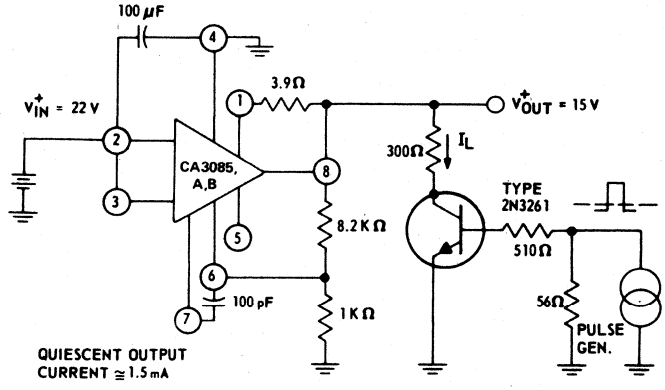


Fig.17—Dissipation limitation (V_{IN}—V_{OUT} vs. I_{OUT}).



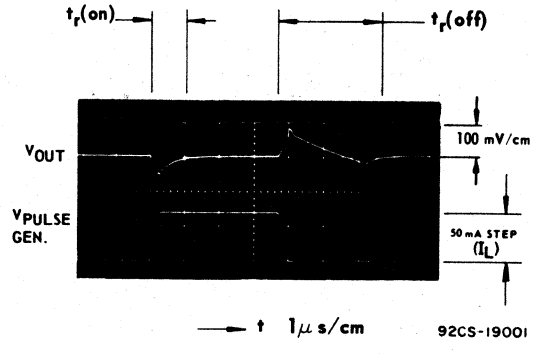


Fig.16—Turn-on and turn-off recovery time test circuit with associated waveforms.

TYPICAL REGULATOR CIRCUITS USING THE CA3085 SERIES

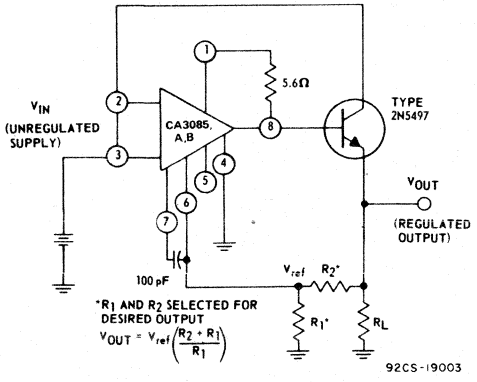


Fig.18—Typical high-current voltage regulator circuit.

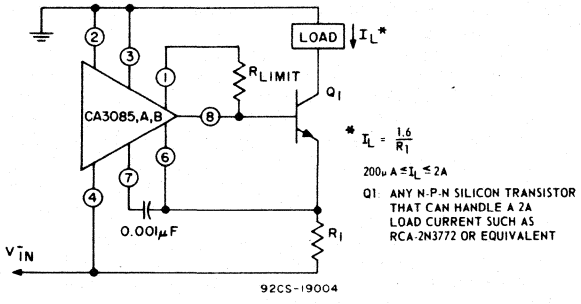
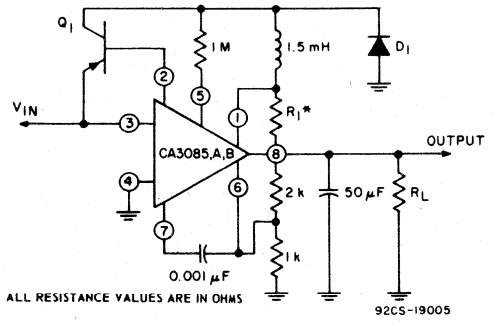
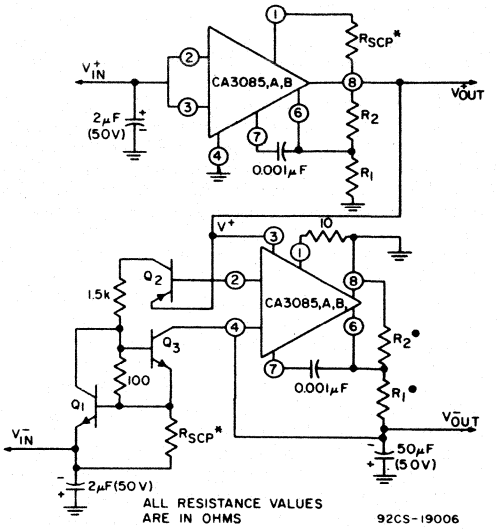


Fig.19—Typical current regulator circuit.



D1: RCA-1N1763A OR EQUIVALENT
Q1: RCA-2N5322 OR EQUIVALENT
*R1 = 0.7 I_L (MAX.)

Fig.20—Typical switching regulator circuit.



ALL RESISTANCE VALUES ARE IN OHMS

Q1: RCA-2N2102 OR EQUIVALENT
Q2: ANY P-N-P SILICON TRANSISTOR (RCA-2N5322 OR EQUIVALENT)
Q3: ANY N-P-N SILICON TRANSISTOR THAT CAN HANDLE THE DESIRED LOAD CURRENT (RCA-2N3772 OR EQUIVALENT)

*$V_{OUT} = \left(\frac{R_1 + R_2}{R_1}\right)$

*R_{SCP}: SHORT-CIRCUIT PROTECTION RESISTANCE

Fig.21—Combination positive and negative voltage regulator circuit.

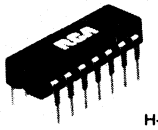
CA3058, CA3059, CA3079

CA3058

H-1553

14-Lead Dual-In-Line Ceramic Package

CA3059
CA3079



H-1517

14-Lead Dual-In-Line Plastic Package

Zero-Voltage Switches

For 50/60 and 400 Hz Thyristor Control Applications

Applications:

- *Relay control*
- *Valve control*
- *Synchronous switching of flashing lights*
- *On-off motor switching*
- *Differential comparator with self-contained power supply for industrial applications*
- *Photosensitive control*
- *Power one-shot control*
- *Heater control*
- *Lamp control*

The RCA-CA3058, CA3059, and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24 V, 120 V, 208/230 V, and 277 V at 50/60 and 400 Hz. Each of the zero-voltage switches incorporates 4 functional blocks (see Fig. 1) as follows:

1. Limiter-Power Supply — Permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier — Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.
3. Zero-Crossing Detector — Synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point; thereby eliminating radio-frequency interference (RFI) when used with resistive loads.
4. Triac Gating Circuit — Provides high-current pulses to the gate of the power controlling thrysistor.

In addition, the CA3058 and CA3059 provide the following important auxiliary functions (see Fig. 1):

1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

For an explanation of these functions see Operating Considerations, page 11. For detailed application information, see companion Application Note, ICAN-6182, "Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3058, CA3059, and CA3079)".

The CA3058 is supplied in a hermetic 14-lead dual-in-line ceramic package. Types CA3059 and CA3079 are supplied in 14-lead dual-in-line plastic packages. The CA3079 is also available in chip form (H suffix).

Features	CA3058	CA3059	CA3079
24V, 120V, 208/230V, 277V at 50 60, or 400 Hz operation	√	√	√
Differential Input	√	√	√
Low Balance Input Current (max.) -μA	1	1	2
Built-in Protection Circuit for opened or shorted sensor (Term. 14)	√	√	
Sensor Range (Rx) - kΩ	2 to 100	2 to 100	2 to 50
DC Mode (Term 12)	√	√	
External Trigger (Term 6)	√	√	
External Inhibit (Term 1)	√	√	
DC Supply Volts (max.)	14	14	10
Operating Temperature Range - °C		-55 to +125	

MAXIMUM RATINGS,
Absolute-Maximum Values at $T_A = 25^oC$

DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 7):
- CA3058, CA3059 ..... 14 V
- CA3079 ..... 10 V

DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 8):
- CA3058, CA3059 ..... 14 V
- CA3079 ..... 10 V

PEAK SUPPLY CURRENT (TERMS. 5 AND 7) ..... ±50 mA

OUTPUT PULSE CURRENT (TERM. 4) ..... 150 mA

POWER DISSIPATION:
- Up to T_A=75°C – CA3058 ..... 700 mW
- Up to T_A=55°C – CA3059,CA3079 ... 700 mW
- Above T_A=75°C – CA3058 ..... Derate Linearly 8 mW/°C
- Above T_A=55°C – CA3059,CA3079 ..... Derate linearly 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating ..... –55 to +125°C
- Storage ..... –65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
- At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL NO.	1 Note 3	2	3	4	5 Note 1	6 Note 3	7	8	9	10	11	12 Note 3	13	14 Note 2,3	MAXIMUM CURRENT RATINGS I_{IN} mA	I_{OUT} mA
1 Note 3		*	*	*	*	15 0	10 -2	*	*	*	*	*	*	*	10	0.1
2			0 -15	0 -15	2 -14	0 -14	0 -14▲	0 -14▲	0 -14	0 -14	0 -14	* .	0 -14	0 -14	150	10
3				0 -15	*	*	*	*	*	*	*	*	*	*	*	*
4					*	2 -10	*	*	*	*	*	*	*	*	0.1	150
5 Note 1						*	7 -7	*	*	*	*	*	*	*	50	10
6 Note 3							14 0	*	*	*	*	*	*	*	*	*
7								*	14 0	*	20 0	2.5 -2.5	14 0	6 -6	*	*
8									10 0	*	*	*	*	*	0.1	2
9										*	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12 Note 3													*	*	50	50
13														*	*	*
14 Note 3															2	2

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to –10 volts.

Note 1 – Resistance should be inserted between Terminal 5 and external supply or line voltage for limiting current into Terminal 5 to less than 50 mA.

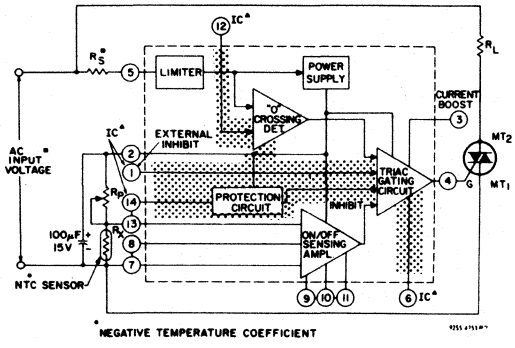
Note 2 – Resistance should be inserted between Terminal 14 and external supply for limiting current into Terminal 14 to less than 2 mA.

Note 3 – For the CA3079 indicated terminal is internally connected and, therefore, should not be used.

▲For CA3079 (0 to –10 V).

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

CA3058, CA3059, CA3079



AC Input Voltage (50/60 or 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE:

Circuitry, within shaded areas, not included in CA3079

■ See chart

▲ IC = Internal Connection - - DO NOT USE (Terminal Restriction applies only to CA3079).

Fig. 1–Functional block diagram of CA3058, CA3059, and CA3079.

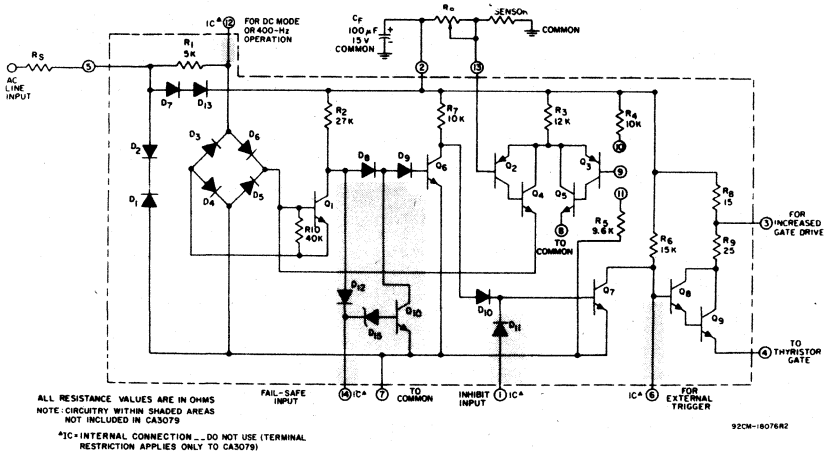


Fig. 2–Schematic diagram of CA3058, CA3059, and CA3079.

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise)

All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS T_A = 25°C (Unless Indicated Otherwise)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)●					
DC Supply Voltage, V_S					
Inhibit Mode					
At 50/60 Hz	R_S = 8 kΩ, I_L = 0	6.1	6.5	7	V
At 400 Hz	R_S = 10 kΩ, I_L = 0	–	6.8	–	V
At 50/60 Hz	R_S = 5 kΩ, I_L = 2 mA	–	6.4	–	V
Pulse Mode					
At 50/60 Hz	R_S = 8 kΩ, I_L = 0	6	6.4	7	V
At 400 Hz	R_S = 10 kΩ, I_L = 0	–	6.7	–	V
At 50/60 Hz	R_S = 5 kΩ, I_L = 2 mA	–	6.3	–	V
At 50/60 Hz (CA3058) *See Fig. 3*	R_S = 8 kΩ, I_L = 0; T_A = –55 to +125°C	5.5	–	7.5	V

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise) (Cont'd)
All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS T_A = 25°C (Unless Indicated Otherwise)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)●					
Gate Trigger Current, I_{GT}(4) *See Figs. 4, 5(a)*	Terms. 3 and 2 connected, V_{GT} = 1 V	–	105	–	mA
Peak Output Current (Pulsed), I_{OM}(4) With Internal Power Supply	Term. 3 open, Gate Trigger Voltage (V_{GT}) = 0	50	84	–	mA
	Terms. 3 and 2 connected, Gate Trigger Voltage (V_{GT})=0	90	124	–	mA
With External Power Supply	Term. 3 open, V^+=12 V, V_{GT}=0	–	170	–	mA
See Figs. 5, 6	Terms. 3 and 2 connected, V^+=12 V, V_{GT} = 0	–	240	–	mA
Inhibit Input Ratio, V_9/V_2 All Types	Voltage Ratio of Term. 9 to 2	0.465	0.485	0.520	–
CA3058 *See Fig. 7*	T_A = –55 to +125°C	0.450	–	0.520	–
Total Gate Pulse Duration:* For positive dv/dt, t_P 50-60 Hz	C_{EXT} = 0	70	100	140	μs
400 Hz	C_{EXT} = 0, R_{EXT} = ∞	–	12	–	μs
For negative dv/dt, t_N 50-60 Hz	C_{EXT} = 0	70	100	140	μs
400 Hz *See Fig. 8*	C_{EXT} = 0, R_{EXT} = ∞	–	10	–	μs
Pulse Duration After Zero Crossing (50-60 Hz): For positive dv/dt, t_{P1}	C_{EXT} = 0	–	50	–	μs
For negative dv/dt, t_{N1} *See Fig. 8*	R_{EXT} = ∞	–	60	–	μs
Output Leakage Current, I_4 Inhibit Mode: All Types		–	0.001	10	μA
CA3058 *See Fig. 9*	T_A = –55 to +125°C	–	–	20	μA
Input Bias Current, I_I CA3058, CA3059		–	220	1000	nA
CA3079 *See Fig. 10*		–	220	2000	nA
Common-Mode Input Voltage Range, V_{CMR}	Terms. 9 and 13 connected	–	1.5 to 5	–	V
Sensitivity, $\Delta V_{13}^{\neq}$ (Pulse Mode) *See Figs. 5(a), 12*	Term. 12 open	–	6	–	mV

≠Required voltage change at Term. 13 to either turn OFF the triac when ON or turn ON the triac when OFF.

*Pulse duration in 50 Hz applications is approximately 15% longer than shown in Fig. 8(b).

● The values given in the Electrical Characteristics Chart at 120 V also apply for operation at input voltages of 24 V, 208/230 V, and 277 V, except for Pulse Duration. However, the series resistor (R_S) must have the indicated value, shown in the chart in Fig. 1, for the specified input voltage.

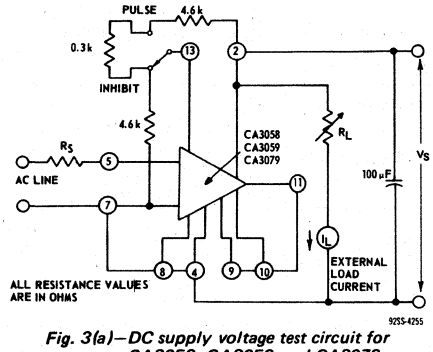


Fig. 3(a)—DC supply voltage test circuit for CA3058, CA3059, and CA3079.

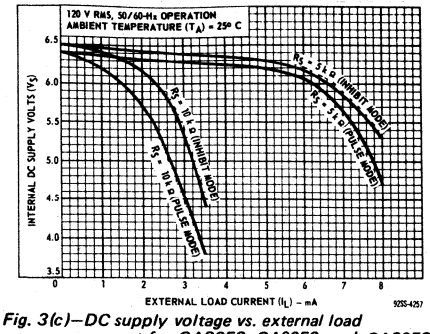


Fig. 3(c)—DC supply voltage vs. external load current for CA3058, CA3059, and CA3079.

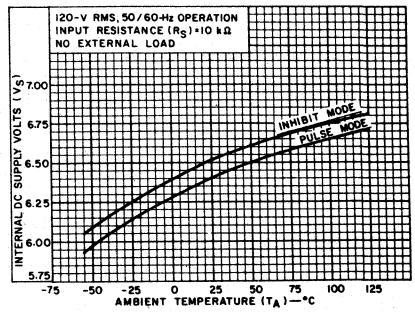


Fig. 3(b)—DC supply voltage vs. ambient temperature for CA3058, CA3059, and CA3079.

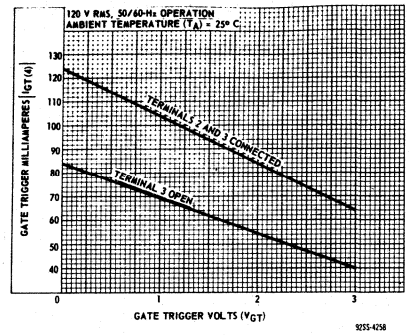


Fig. 4—Gate trigger current vs. gate trigger voltage for CA3058, CA3059, and CA3079.

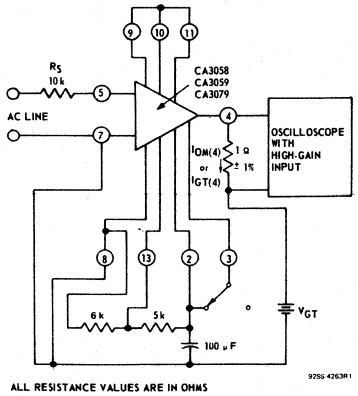


Fig. 5(a)—Peak output (pulsed) and gate trigger current with internal power supply test circuit for CA3058, CA3059, and CA3079.

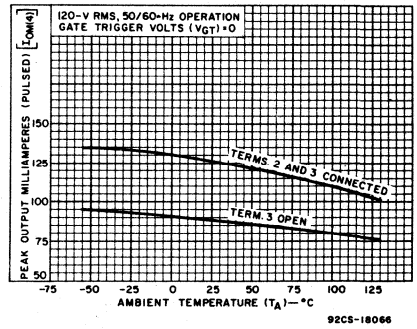


Fig. 5(b)—Peak output current (pulsed) vs. ambient temperature for CA3058, CA3059, and CA3079.

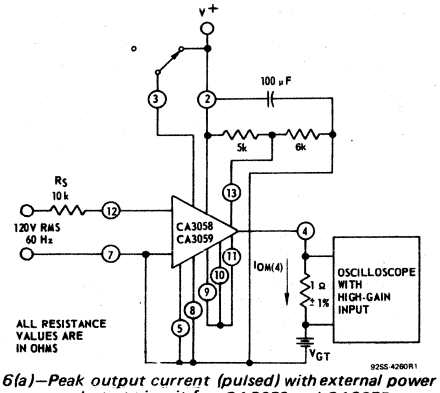


Fig. 6(a)—Peak output current (pulsed) with external power supply test circuit for CA3058 and CA3059.

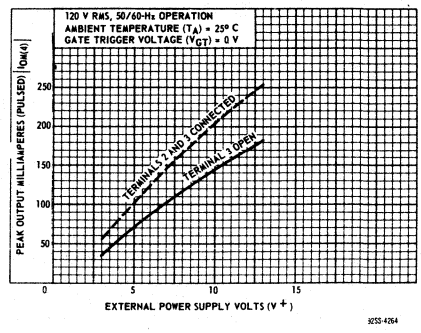


Fig. 6(b)—Peak output current (pulsed) vs. external power supply voltage for CA3058 and CA3059.

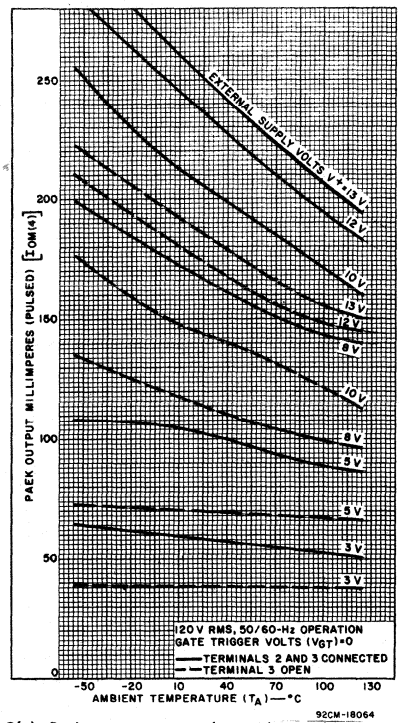


Fig. 6(c)—Peak output current (pulsed) vs. ambient temperature for CA3058 and CA3059.

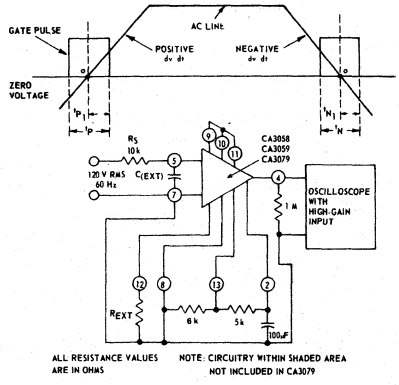


Fig. 8(a)—Gate pulse duration test circuit with associated waveform for CA3058, CA3059, and CA3079.

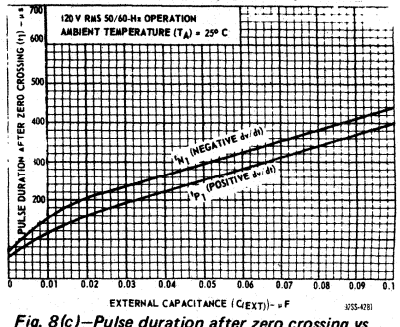


Fig. 8(c)—Pulse duration after zero crossing vs. external capacitance for CA3058, CA3059, and CA3079.

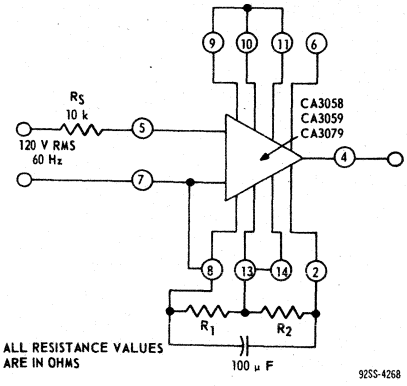


Fig. 7(a)—Input inhibit voltage ratio test circuit for CA3058, CA3059, and CA3079.

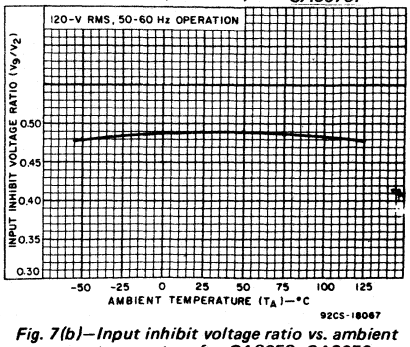


Fig. 7(b)—Input inhibit voltage ratio vs. ambient temperature for CA3058, CA3059, and CA3079.

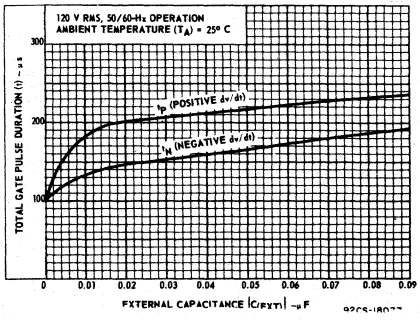


Fig. 8(b)—Total gate pulse duration vs. external capacitance for CA3058, CA3059, and CA3079.

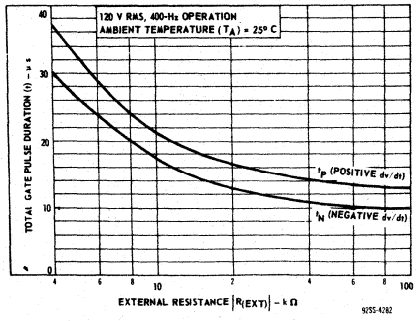


Fig. 8(d)—Total gate pulse duration vs. external resistance for CA3058 and CA3059.

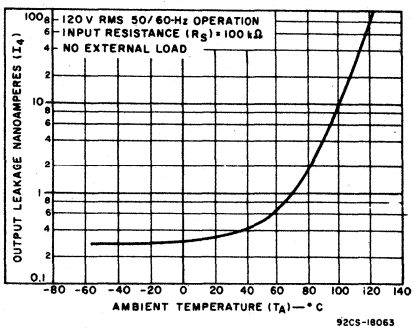


Fig. 9—Output leakage current (inhibit mode) vs. ambient temperature for CA3058, CA3059, and CA3079.

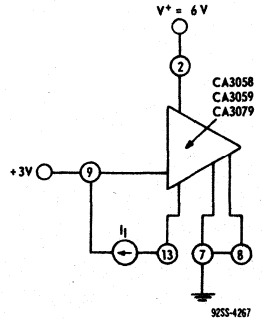
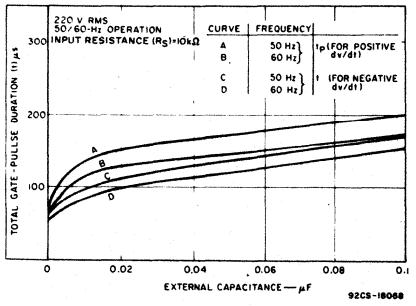
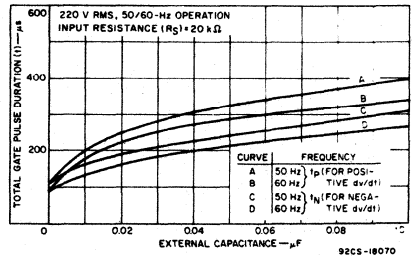


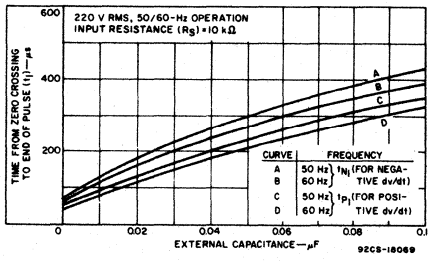
Fig. 10—Input bias current test circuit for CA3058, CA3059, and CA3079.



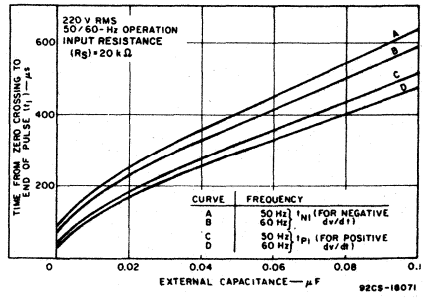
(a)



(b)



(c)



(d)

Fig. 11—Relative pulse width and location of zero crossing for 220-volt operation for CA3058, CA3059, and CA3079.

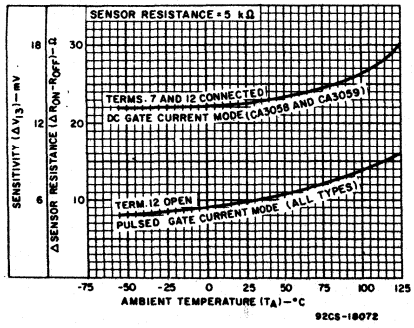


Fig. 12—Sensitivity vs. ambient temperature for CA3058, CA3059, and CA3079.

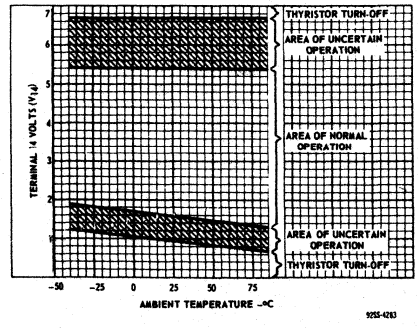


Fig. 13—Operating regions for built-in protection circuit for CA3058 and CA3059.

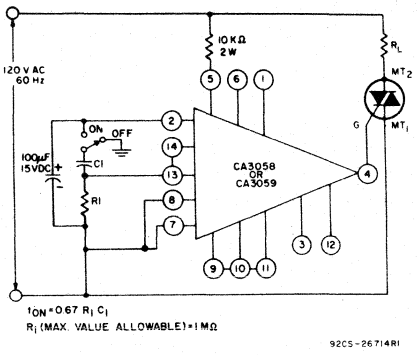


Fig. 14—Line-operated one-shot timer.

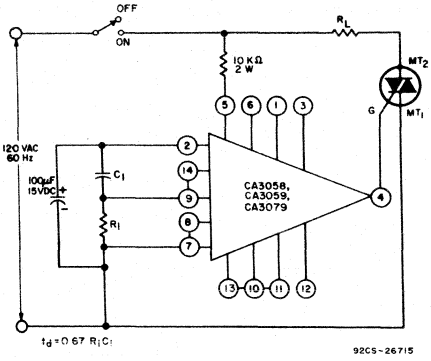


Fig. 15—Line-operated thyristor control time delay turn-on circuit.

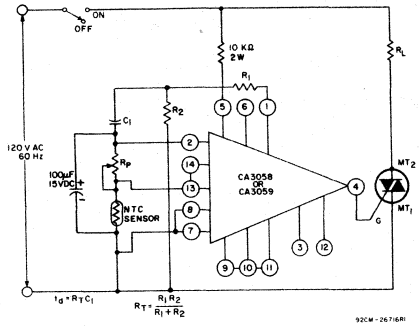


Fig. 16—On/off temperature control circuit with delayed turn-on.

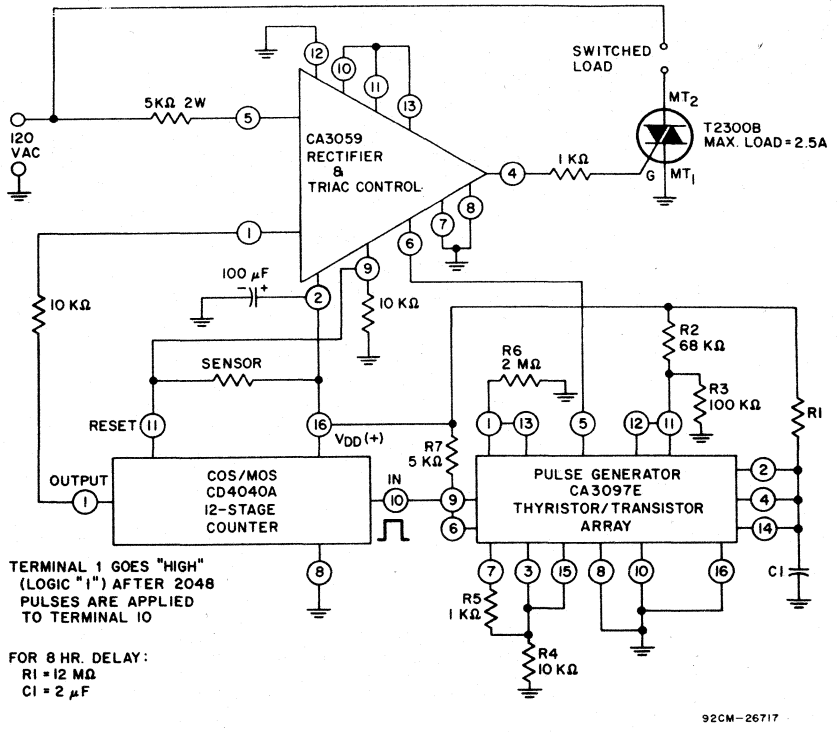


Fig. 17(a)—Line-operated IC timer for long time periods.

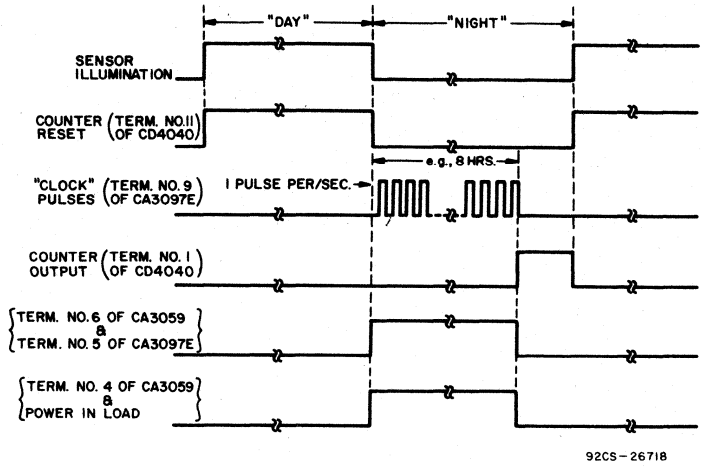


Fig. 17(b)—Timing diagram for Fig. 17(a).

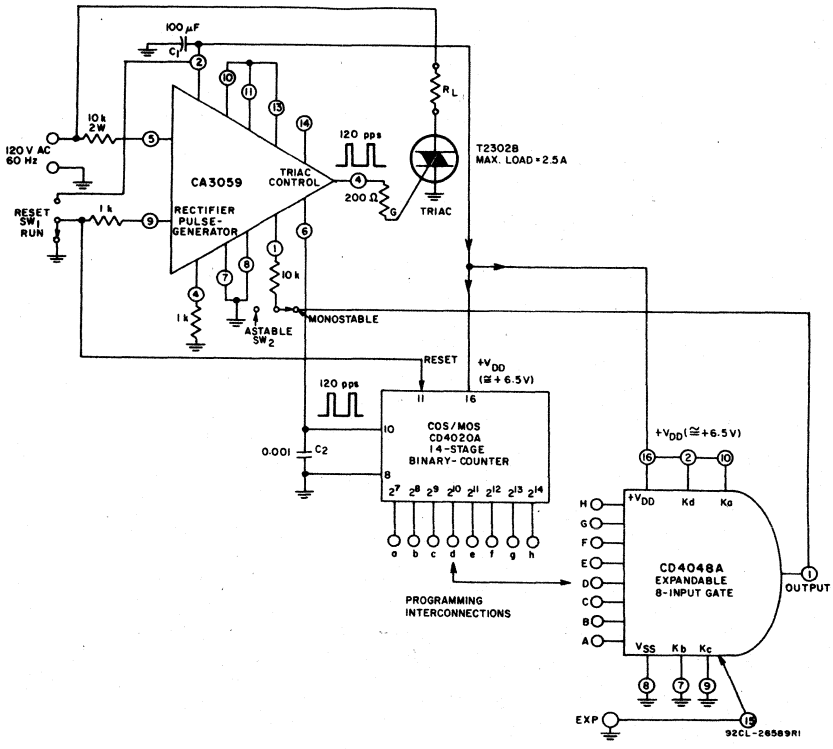


Fig. 18(a)—Programmable ultra-accurate line-operated timer. (Programmable over the range from 0.5333 seconds to 2 minutes, 16 seconds in 0.5333-second increments)

Time Periods (t = 0.5333 s)	1 t	2 t	4 t	8 t	16 t	32 t	64 t	128 t	t_o
Terminals									
CD4020A	a	b	c	d	e	f	g	h	
CD4048A	A	B	C	D	E	F	G	H	
	C	NC	NC	NC	NC	NC	NC	NC	1 t
	NC	C	NC	NC	NC	NC	NC	NC	2 t
	C	C	NC	NC	NC	NC	NC	NC	3 t
	NC	NC	C	NC	NC	NC	NC	NC	4 t
	C	NC	C	NC	NC	NC	NC	NC	5 t
	NC	C	C	NC	NC	NC	NC	NC	6 t
	C	C	C	NC	NC	NC	NC	NC	7 t
	NC	NC	NC	C	NC	NC	NC	NC	8 t
	C	NC	NC	C	NC	NC	NC	NC	9 t
	NC	C	NC	C	NC	NC	NC	NC	10 t
	C	C	NC	C	NC	NC	NC	NC	11 t
	NC	NC	C	C	NC	NC	NC	NC	12 t
	C	NC	C	C	NC	NC	NC	NC	13 t
	NC	C	C	C	NC	NC	NC	NC	14 t
	C	C	C	C	NC	NC	NC	NC	15 t
	C	C	C	C	NC	C	C	NC	111 t
	NC	NC	NC	NC	C	C	C	NC	112 t
	C	NC	NC	NC	C	C	C	NC	113 t
	C	C	C	C	C	C	C	C	255 t

Notes:

t_o = Total time delay = $n_1 t + n_2 t + \ldots n_n t$.

C = Connect. For example, interconnect terminal a of the CD4020A and terminal A of the CD4048A.

NC = No Connection. For example, terminal b of the CD4020A open and terminal B of the CD4048A connected to $+V_{DD}$ bus.

Fig. 18(b)—"Programming" table for Fig. 18(a).

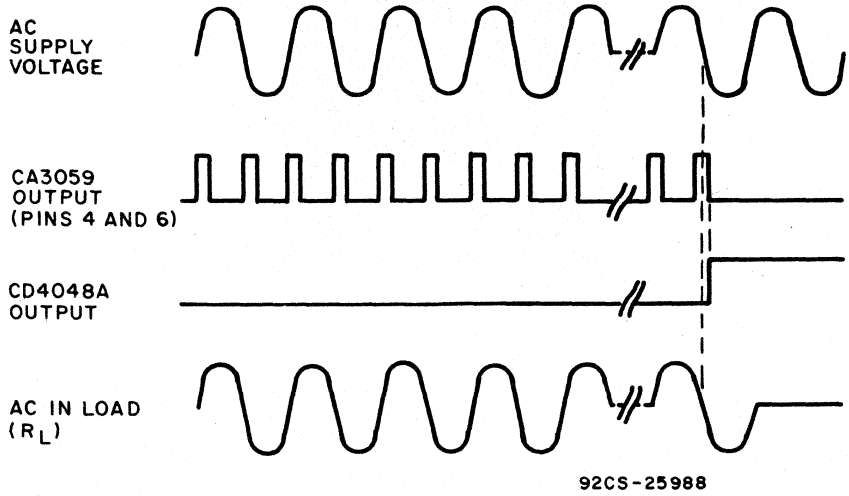


Fig. 18(c)—Timing diagram for Fig. 18(a).

OPERATING CONSIDERATIONS

Power Supply Considerations for CA3058, CA3059, and CA3079

The CA3058, CA3059, and CA3079 are intended for operation as self-powered circuits with the power supplied from an AC line through a dropping resistor. The internal supply is designed to allow for some current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figs. 3(b) and 3(c).

Power Supply Considerations for CA3058 and CA3059

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Fig. 5 for the peak output current characteristics). When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Fig. 5(a).

Operation of Built-in Protection for the CA3058, CA3059

A special feature of the CA3058 and CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in Fig. 1. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2 mA with a 5 kΩ dropping resistor.
2. Set the value of R_P and sensor resistance (R_X) between 2 kΩ and 100 kΩ.
3. The ratio of R_X to R_P, typically, should be greater than 0.33 and less than 3. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series or shunt resistor must be added to avoid undesired activation of the circuit.

If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Fig. 13.

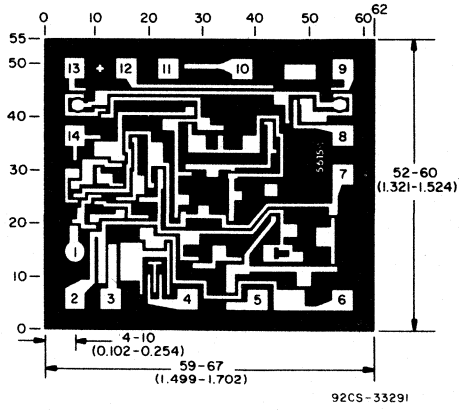
External Inhibit Function for the CA3058 and CA3059

A priority inhibit command may be applied to Terminal 1. The presence of at least +1.2 V at 10 μA will remove drive from the thyristor. This required level is compatible with DTL or T^2L logic. A logical 1 activates the inhibit function.

DC Gate Current Mode for the CA3058 and CA3059

Connecting Terminals 7 and 12 disables the zero-crossing detector and permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be exercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.

For a list of RCA thyristors, see RCA Thyristor Data Bulletin, File No. 406, dated 5-75.



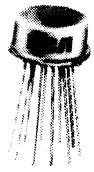
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid gradations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CA3059H.

Differential Amplifiers
Technical Data

CA3000



10-Lead TO-5

H-1384

DC Amplifier

Features:

- *Designed for use in Communication, Telemetry, Instrumentation, and Data-Processing Equipment*
- *Balanced differential-amplifier configuration with controlled constant-current source to provide outstanding versatility*
- *Built-in temperature stability for operation from −55°C to +125°C*
- *Companion Application Note, ICAN 5030 "Applications of RCA CA3000 Integrated Circuit DC Amplifier" covers characteristics of different operating modes, frequency considerations, 10 MHz narrow band tuned amplifier design, crystal oscillator design, and many other application aids*
- *Input impedance - 195 kΩ typ.*
- *Voltage gain - 37 dB typ.*
- *Common-mode rejection ratio - 98 dB typ.*
- *Input offset voltage - 1.4 mV typ.*
- *Push-pull input and output*
- *Frequency capability - DC to 30 MHz (with external C and R)*
- *Wide AGC range - 90 dB typ.*

Applications

- *Schmitt trigger*
- *RC-coupled feedback amplifier*
- *Mixer*
- *Comparator*
- *Modulator*
- *Crystal oscillator*
- *Sense amplifier*

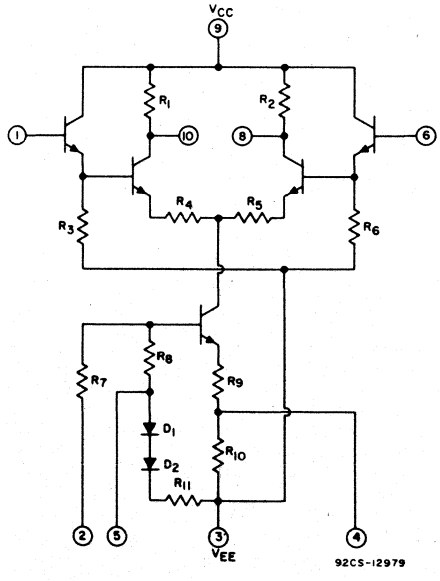


Fig. 1 — Schematic Diagram

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_A = 25°C

Indicated voltage limits for each terminal can be used under specified voltage conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2	+2	2	0
			3	-6
			6	0
			9	+6
2	-8	0	1	0
			3	-8
			6	0
			9	+6
3	-10	0	1	0
			2	0
			6	0
			9	+6
4	-8	0	1	0
			2	0
			6	0
			9	+6
5	-6	0	1	0
			2	0
			3	-6
			6	0
			9	+6

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
6	-2	+2	1	0
			2	0
			3	-6
			9	+6
7	NO CONNECTION			
8	0	+6	1	0
			2	0
			3	-6
			6	0
9	0	+10	1	0
			2	0
			3	-6
			6	0
10	0	+6	1	0
			2	0
			3	-6
			6	0
CASE	Internally Connected to Terminal No.3 (Substrate) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE	-55°C to +125°C
STORAGE-TEMPERATURE RANGE	-65°C to +150°C
LEAD TEMPERATURE (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	± 4 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	± 2 V
MAXIMUM DEVICE DISSIPATION:	
From -55°C to 85°C	450
Above 85°C	Derate 5 mW/°C

CA3000

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V_{CC} = +6V, V_{EE} = -6V, unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 & No.5 Not Connected Unless Specified		TEST CIRCUITS	LIMITS TYPE CA3000				TYPICAL CHARACTERISTICS CURVES
				Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS									
Input Offset Voltage	V_{IO}				-	1.4	5	mV	2
Input Offset Current	I_{IO}				-	1.2	10	μA	2
Input Bias Current	I_{IB}				-	23	36	μA	3
Quiescent Operating Voltage	V_8 or V_{IO}	TERMINALS 4	5						
		NC	NC		-	2.6	-	V	4
		NC	VEE		-	4.2	-	V	4
		VEE	NC		-	-1.5	-	V	4
		VEE	VEE		-	0.6	-	V	4
Device Dissipation	P_D	NC	NC		-	30	-	mW	NONE
DYNAMIC CHARACTERISTICS									
Differential Voltage Gain Single-Ended Input	A_{DIFF}	Single-Ended Output f = 1 kHz		9	28	32	-	dB	5
		Double-Ended Output f = 1 kHz		9	-	38	-	dB	5
Bandwidth at -3 dB Point	BW	V_I = 10 mV, R_S = 1 kΩ			-	650	-	kHz	7
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	f = 1 kHz		9	-	6.4	-	V(P-P)	NONE
Common-Mode Rejection Ratio	CMRR	f = 1 kHz		13	70	98	-	dB	8
Single-Ended Input Impedance	Z_{IN}	f = 1 kHz		15	70K	195K	-	Ω	10
Single-Ended Output Impedance	Z_{OUT}	f = 1 kHz		17	5.5K	8K	10.5K	Ω	12
Total Harmonic Distortion	THD	R_S=1kΩ f = 1 kHz V_O=42V_{p-p}			-	0.2	5	%	14
AGC Range (Maximum Voltage Gain to Complete Cutoff)	AGC	f = 1 kHz		20	80	90	-	dB	NONE

STATIC CHARACTERISTICS

INPUT OFFSET VOLTAGE AND CURRENT vs TEMPERATURE

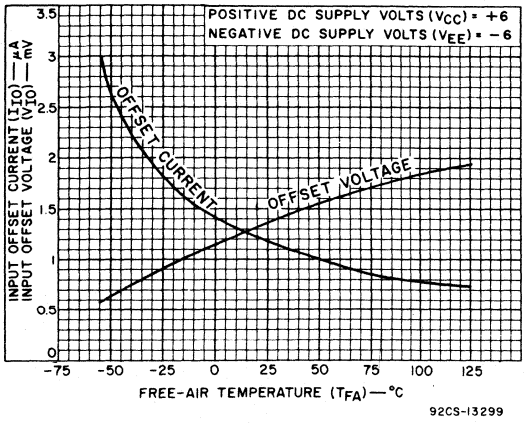


Fig.2

INPUT BIAS CURRENT vs TEMPERATURE

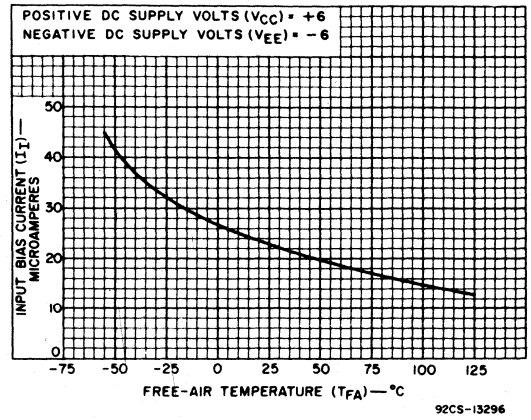


Fig.3

STATIC CHARACTERISTICS

QUIESCENT OPERATING VOLTAGE vs TEMPERATURE

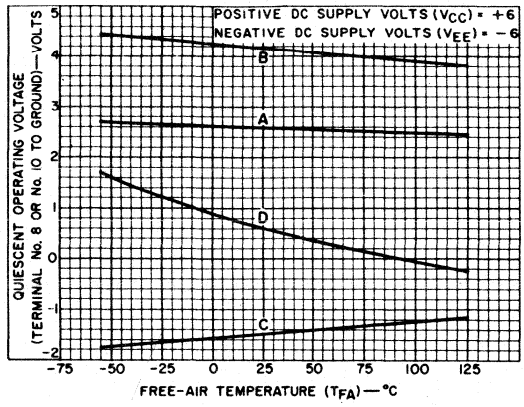


Fig. 4

DYNAMIC CHARACTERISTICS AND TEST CIRCUIT FOR TYPE CA3000

DIFFERENTIAL VOLTAGE GAIN vs TEMPERATURE

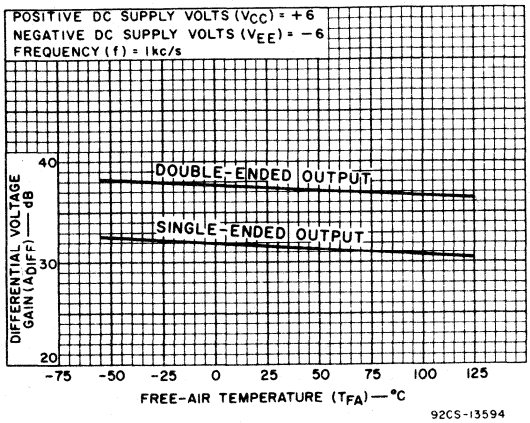


Fig. 5

DIFFERENTIAL VOLTAGE GAIN AND MAXIMUM OUTPUT VOLTAGE SWING TEST CIRCUIT

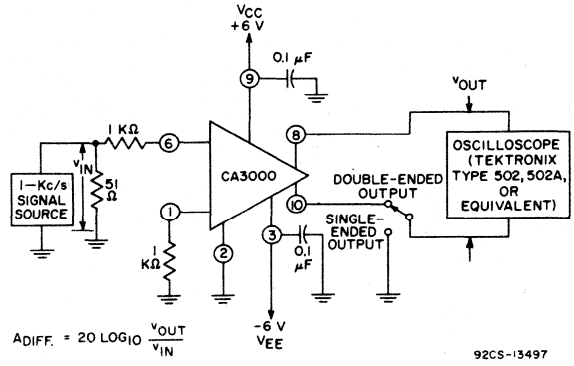


Fig. 6

DYNAMIC CHARACTERISTICS AND TEST CIRCUIT

BANDWIDTH AT -3 dB POINT vs TEMPERATURE

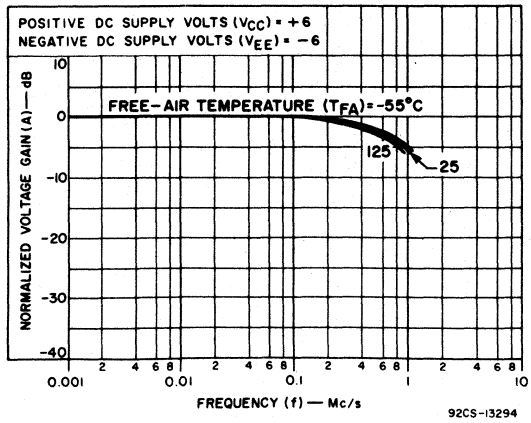


Fig. 7

COMMON-MODE REJECTION RATIO vs TEMPERATURE

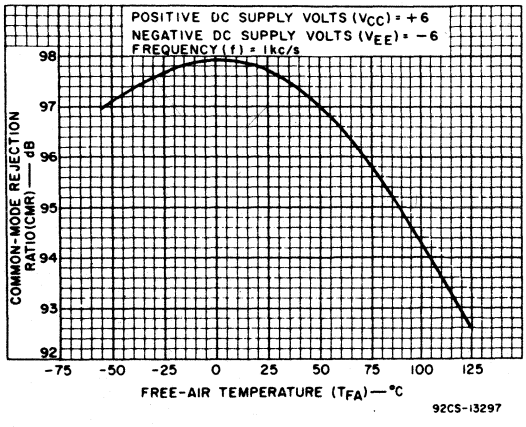
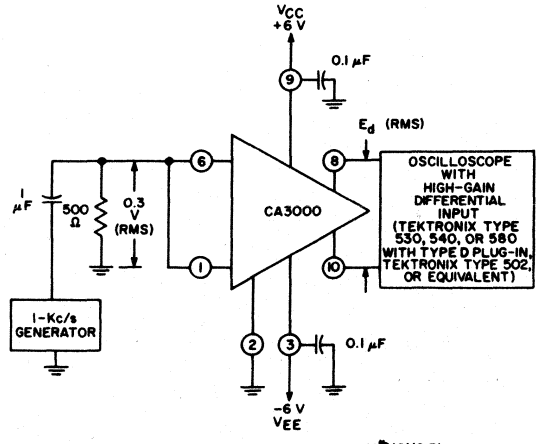


Fig. 8

COMMON-MODE REJECTION RATIO TEST CIRCUIT



COMMON-MODE REJECTION RATIO (CMR) = 20 log $\frac{(A^*)(2)(0.3)}{E_{d\,(RMS)}}$

*A = SINGLE-ENDED VOLTAGE GAIN

92CS-12983RI

Fig. 9

DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3000

SINGLE-ENDED INPUT IMPEDANCE vs TEMPERATURE

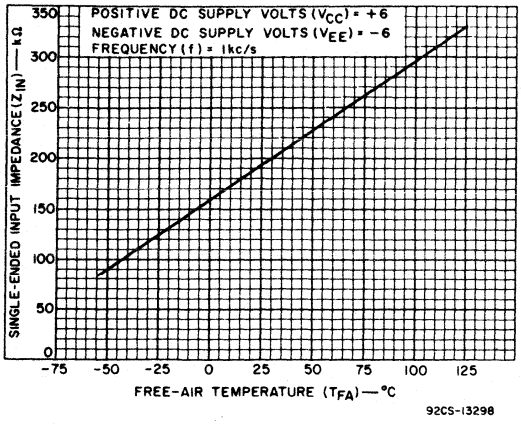


Fig. 10

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

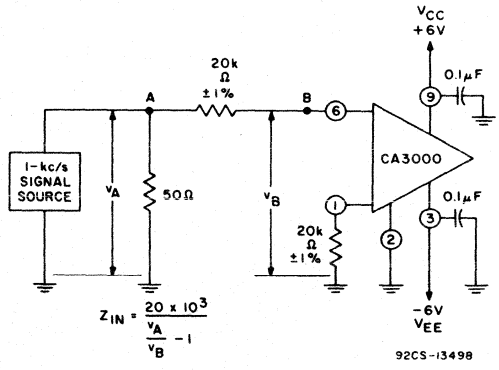


Fig. 11

SINGLE-ENDED OUTPUT IMPEDANCE vs TEMPERATURE

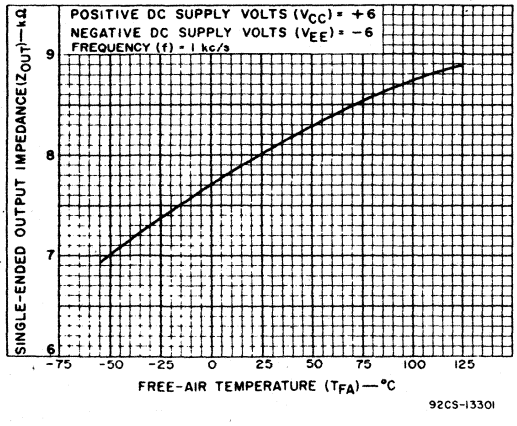
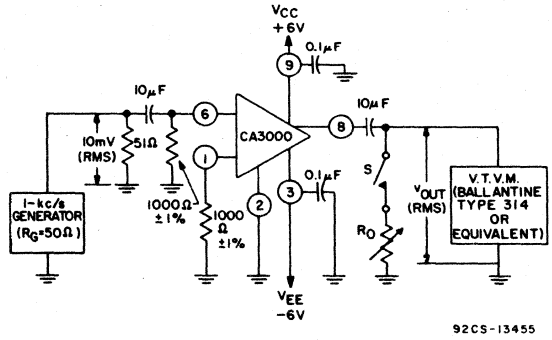


Fig. 12

SINGLE-ENDED OUTPUT IMPEDANCE TEST CIRCUIT



1. With Switch S open, record reference voltage V_{OUT}(rms).
2. Close Switch S, and adjust R_O until
   $V_{OUT} = \frac{\text{Reference Voltage}}{2}$
3. Record value of R_O as Z_{OUT}.

Fig. 13

DYNAMIC CHARACTERISTICS AND TEST CIRCUIT

TOTAL HARMONIC DISTORTION vs TEMPERATURE

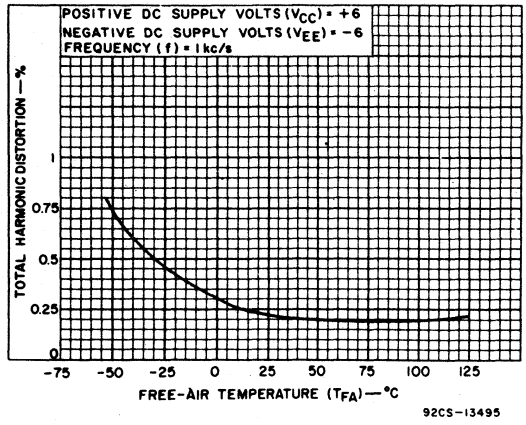
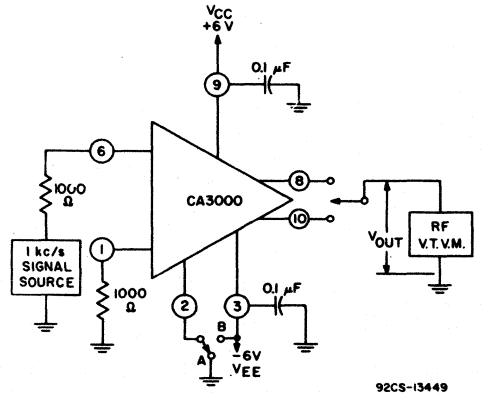


Fig. 14

AGC RANGE TEST CIRCUIT



$$\text{AGC Range} = 20 \log_{10} \frac{\text{A with S in Position A}}{\text{A with S in Position B}}$$

Fig. 15

12-Lead TO-5 Package

H-1463

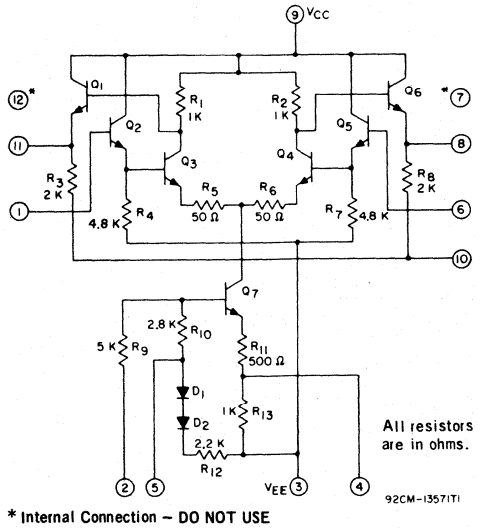
Video and Wide-band Amplifier

Features:

- *Designed for use in video systems and communication equipment*
- *Balanced differential amplifier configuration with controlled constant-current source provides outstanding versatility*
- *Built-in temperature stability for operation from −55° C to +125° C*
- *Emitter follower input & output*
- *Companion Application Note ICAN5038 "Application of the RCA-CA3001 Integrated-Circuit Video Amplifier", covers different operating modes, gain control, distortion, swing capability, 3 stage amplifier design, and a Schmitt trigger study.*
- *Push-pull input & output*
- *AGC range - 60 dB typ.*
- *Bandwidth - 29 MHz*
- *Input resistance - 150 kΩ typ.*
- *Output resistance - 45 Ω typ.*
- *Voltage gain - 19 dB typ.*
- *Input offset voltage - 1.5 mV typ.*

Applications

- *Schmitt trigger*
- *Mixer*
- *Modulator*
- *DC, IF & video amplifier*



* Internal Connection – DO NOT USE

Fig. 1 — Schematic Diagram.

CA3001

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS at T_A = 25°C

Indicated voltage or current limits for each terminal can be applied under the specified conditions for other terminals.
All Voltages are with respect to ground (common terminal of Positive and Negative DC Supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2, 6 3, 10 9	0 -6 +6
2	-8.5	0	1, 6 3, 10 9	0 -8.5 +6
3	-10	0	1, 2, 6 9 10	0 +6 -6
4	-8.5	0	1, 2, 6 9 10	0 +6 -6
5	-6	0	1, 2, 6 3, 10 9	0 -6 +6
6	-2.5	+2.5	1, 2 3, 10 9	0 -6 +6
7	INTERNAL CONNECTION DO NOT USE			

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.8 & No.10	0 -6 +6
9	0	+10	1, 2, 6, 10 3	0 -6
10	-10	0	1, 2, 6 3 9	0 -6 +6
11	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.10 & No.11	0 -6 +6
12	INTERNAL CONNECTION DO NOT USE			
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

OPERATING TEMPERATURE RANGE ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE ..... -65°C to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ±1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. ..... +265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE ..... ± 4 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE ..... ± 2.5 V
MAXIMUM DEVICE DISSIPATION:
-55 to 85°C ..... 450 mW
Above 85°C ..... Derate linearly 5 mW/°C

ELECTRICAL CHARACTERISTICS, AT T_A = 25°C, V_{CC} = +6V, V_{EE} = -6V

CHARACTERISTICS (See Page 2 for Definitions of Terms)	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 and No.5 Not Connected Unless Specified	TEST CIRCUITS	LIMITS TYPE CA3001				TYPICAL CHARACTERISTICS CURVES
			Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS:								
Input Offset Voltage	V_{IO}		4	-	1.5	-	mV	2
Input Offset Current	I_{IO}		5	-	1	10	μA	2
Input Bias Current	I_I		5	-	16	36	μA	3
Output Offset Voltage	V_{OO}	R_S = 1 kΩ		-	54	300	mV	6
Quiescent Operating Voltage	V_8 OR V_{11}	TERMINALS MODE A: 4 = NC, 5 = NC		3.8	4.4	5	V	7
		MODE B: 4 = NC, 5 = V_{EE}		-	4.8	-	V	7
		MODE C: 4 = V_{EE}, 5 = NC		-	2.7	-	V	7
		MODE D: 4 = V_{EE}, 5 = V_{EE}		-	4	-	V	7
Device Dissipation	P_D	A: 4 = NC, 5 = NC		60	78	120	mW	8
		B: 4 = NC, 5 = V_{EE}		-	71	-	mW	8
		C: 4 = V_{EE}, 5 = NC		-	110	-	mW	8
		D: 4 = V_{EE}, 5 = V_{EE}		-	86	-	mW	8
DYNAMIC CHARACTERISTICS:								
Differential Voltage Gain (Single-ended input and output)	A_{DIFF}	f = 1.75 MHz f = 20 MHz		16 10	19 14	- -	dB dB	9 A, 9 B 9 B
Bandwidth at -3 dB Point	BW	R_S = 50Ω		16	29	-	MHz	NONE
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	R_S = 50Ω f = 1.75 MHz		-	5	-	V_{P-P}	NONE
Noise Figure	NF	f = 1.75 MHz, R_S = 1 KΩ	14	-	5	8	dB	10
		f = 11.7 MHz, R_S = 1 KΩ	14	-	7.7	-	dB	10
Common-Mode Rejection Ratio	CMRR	f = 1 KHz	16	70	88	-	dB	12
Input Impedance Components:								
Parallel Input Resistance	R_{IN}	f = 1.75 MHz		50	140	-	KΩ	14
Parallel Input Capacitance	C_{IN}	f = 1.75 MHz		-	3.4	7	pF	14
Output Resistance	R_{OUT}	f = 1.75 MHz		-	45	70	Ω	NONE
AGC Range (Maximum voltage gain to complete cutoff)	AGC	f = 1.75 MHz	19	55	60	-	dB	NONE

TYPICAL STATIC CHARACTERISTICS

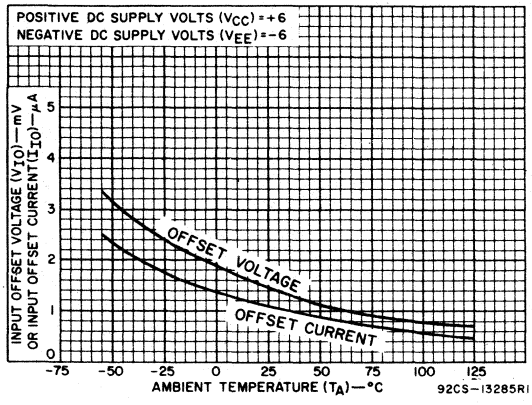


Fig.2 - Input offset voltage and current vs. temperature.

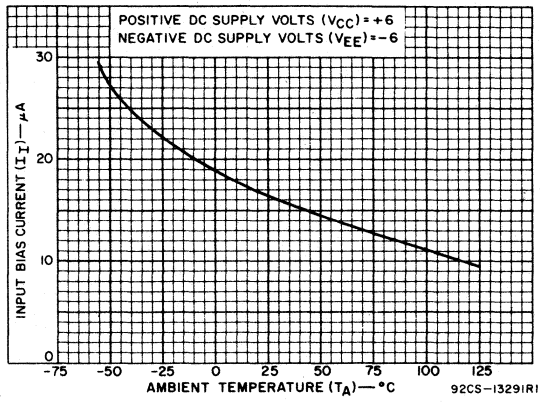
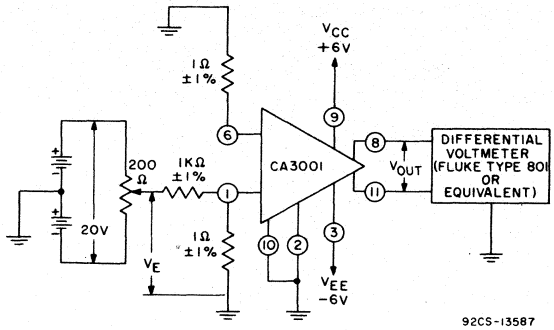


Fig.3 - Input bias current vs. temperature.

CA3001

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS



1. Adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ V 2. Measure V_E and record input offset voltage (V_{IO}) in mV as $V_{IO} = \frac{V_E}{1000}$

Fig.4 - Input offset voltage test circuit.

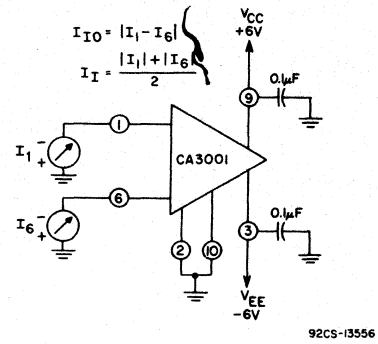


Fig.5 - Input offset current and input bias current test circuit.

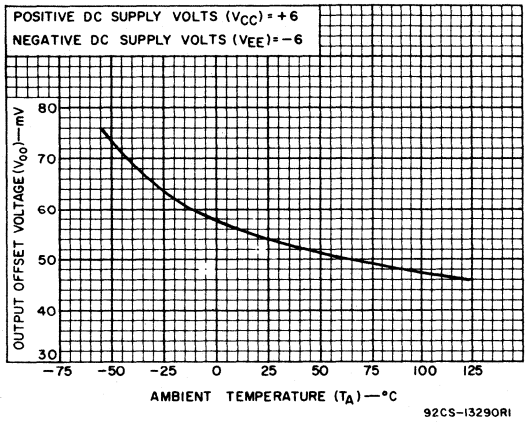


Fig.6 - Output offset voltage vs. temperature.

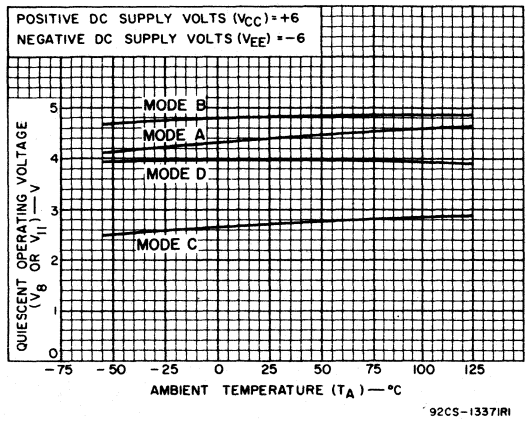


Fig.7 - Quiescent operating voltage vs. temperature.

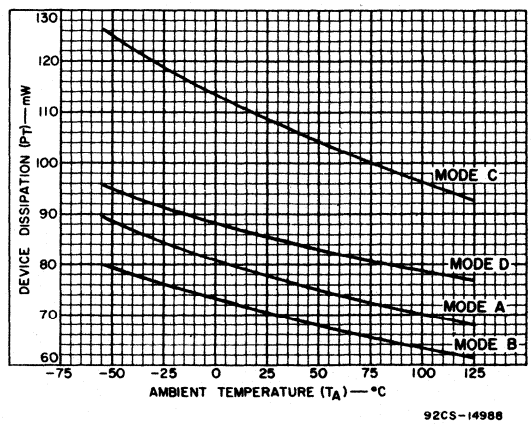


Fig.8 - Device dissipation vs. temperature.

TYPICAL DYNAMIC CHARACTERISTICS

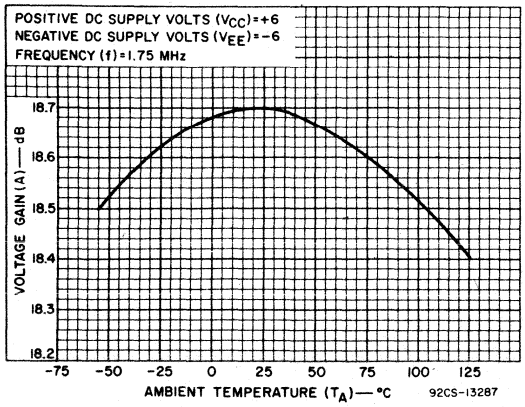


Fig.9a - Differential voltage gain vs. temperature.

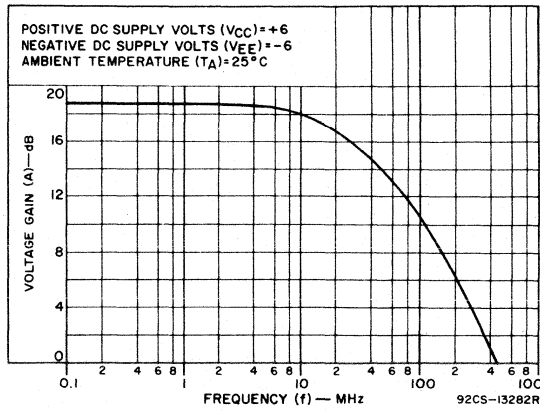


Fig.9 b - Differential voltage gain vs. frequency.

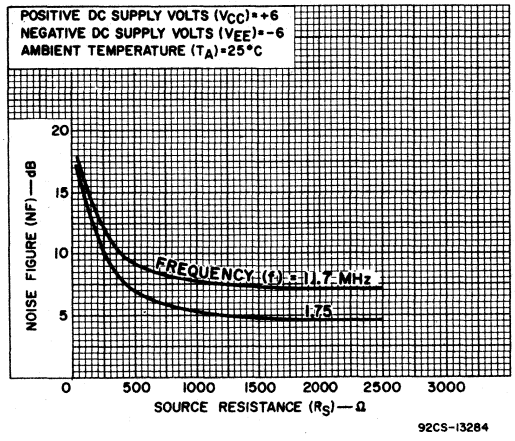
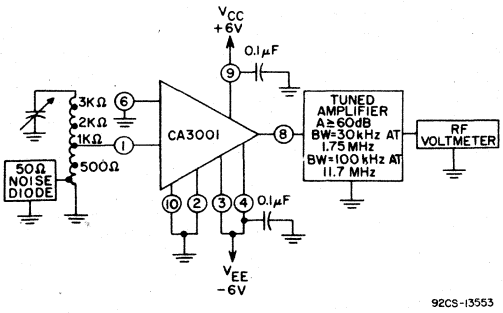


Fig.10 - Noise figure vs. source resistance and frequency.

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS



* Separate tuned input circuits are used for 1.75 MHz and 11.7 MHz. Source-resistance matching taps adjusted with circuit tuned to resonance and with 50-ohm resistor connected to simulate noise diode.

Fig.11 - Noise figure test circuit.

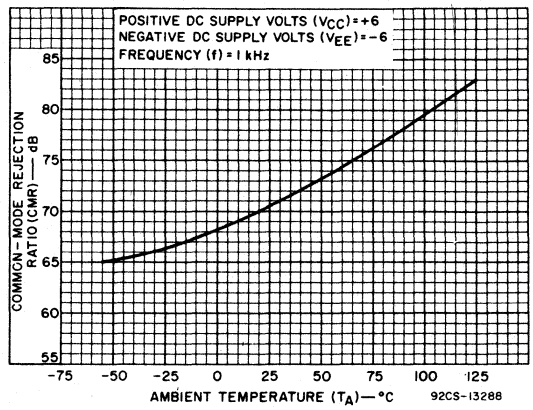
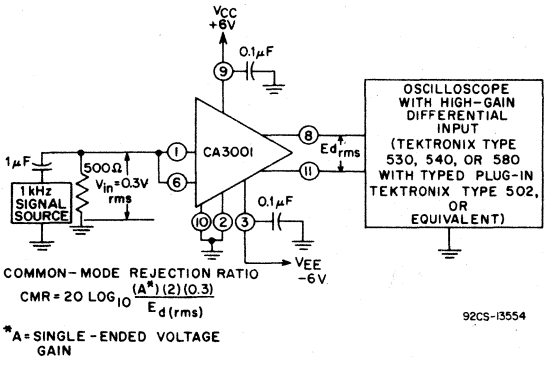


Fig.12 - Common-mode rejection ratio vs. temperature.



*A = SINGLE-ENDED VOLTAGE GAIN

Fig.13 - Common-mode rejection ratio test circuit.

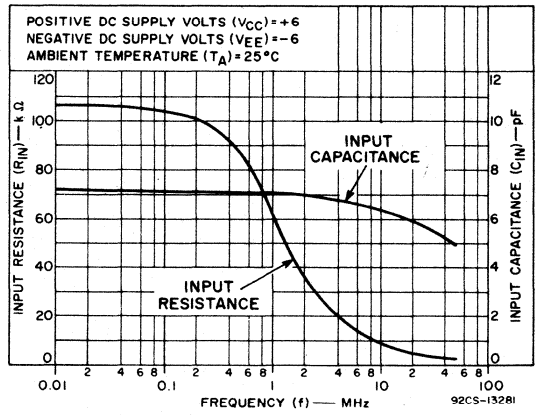


Fig.14 - Input impedance components vs. frequency.

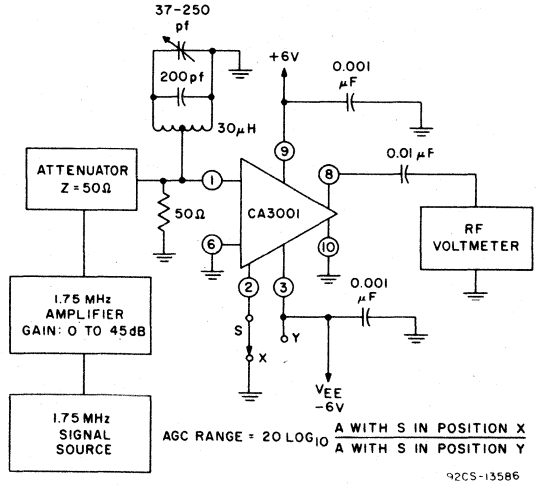


Fig.15 - AGC range test circuit.

12-Lead TO-5

H-1463

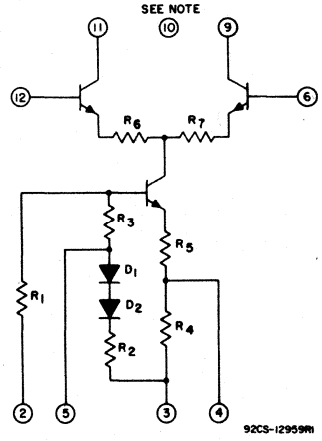
RF Amplifier

Features:

- *Designed for use in communications equipment*
- *Balanced differential-amplifier configuration with controlled constant-current source provides unexcelled versatility*
- *Built-in temperature stability for operation from −55° C to +125° C*
- *Similar to RCA CA3005 and CA3006, plus emitter-degeneration resistors to provide more linear transfer characteristic and increased input-signal handling capability*
- *Companion Application Note ICAN 5022 "Application of RCA CA3004, CA3005, and CA3006 Integrated Circuit RF Amplifiers", covers characteristics of different operating modes, noise performance, cross-modulation, mixer, AGC, limiter, detector, and amplifier design considerations.*

Applications:

- *Push-pull input and output*
- *Wide and narrow-band amplifier*
- *AGC*
- *Detector*
- *Operation from DC to 100 MHz*
- *Mixer*
- *Limiter*
- *Modulator*
- *RF, IF and video frequency capability*



NOTE: Connect Terminal No. 10 to most positive dc supply voltage used for circuit.

Fig. 1 — Schematic Diagram for CA3004

CA3004

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_{FA} = 25°C

Voltage limits shown for each terminal can be applied under the indicated circuit conditions for other terminals. All voltages are with respect to GROUND (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	NO CONNECTION			
2	-9.5	0	6	0
			12	0
			3	-9.5
			9	+6
			10	+6
			11	+6
3	-12	0	2	0
			6	0
			9	+6
			10	+6
			11	+6
			12	0
4	-12	0	2	0
			6	0
			9	+6
			10	+6
			11	+6
			12	0
5	-6	0	2,6,12	0
			3	-6
			9	+6
			10	+6
			11	+6
6	-3.5	+3.5	2	0
			3	-6
			9	+6
			10	+6
			11	+6
			12	0

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
7	NO CONNECTION			
8	NO CONNECTION			
9	0	+12	2	0
			3	-6
			6	0
			10	+6
			11	+6
			12	0
10	0	+12	2	0
			3	-6
			6	0
			9	+6
			11	+6
			12	0
11	0	+12	2	0
			3	-6
			6	0
			10	+6
			11	+6
			12	0
12	-3.5	+3.5	2	0
			3	-6
			6	0
			9	+6
			10	+6
			11	+6
CASE	INTERNALLY CONNECTED TO TERMINAL NO.3 (SUBSTRATE) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE . . . . . -55°C to +125°C

STORAGE-TEMPERATURE RANGE . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

MAXIMUM SINGLE-ENDED INPUT-
SIGNAL VOLTAGE . . . . . ±3.5 V

MAXIMUM COMMON-MODE INPUT-
SIGNAL VOLTAGE . . . . . -2.5 V, +3.5 V

MAXIMUM DEVICE DISSIPATION . . . . . 300 mW

ELECTRICAL CHARACTERISTICS, at T_{FA} = 25° C, V_{CC} = +6V, V_{EE} = -6 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 and No.5 Open Unless Otherwise Specified		TEST CIRCUIT	LIMITS TYPE CA3004				TYPICAL CHARACTERISTICS CURVES
				Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS									
Input Offset Voltage	V_{IO}			Fig.4	–	1.7	5	mV	Fig.2
Input Offset Current	I_{IO}			Fig.5	–	0.125	5	μA	Fig.2
Input Bias Current	I_I			Fig.5	–	21	40	μA	Fig.3
		TERMINALS							
		4	5						
Quiescent Operating Current	I_9 or I_{11}	NC	NC	Fig.8	–	1	–	mA	Fig.6
		V_{EE}	NC	Fig.8	–	2.7	–	mA	Fig.6
		NC	V_{EE}	Fig.8	–	0.45	–	mA	Fig.6
		V_{EE}	V_{EE}	Fig.8	–	1.25	–	mA	Fig.6
Quiescent Operating Current Ratio	I_9/I_{11}			Fig.8	–	1.1	–	–	Fig.7
Device Dissipation	P_T			Fig.8	–	26	–	mW	NONE
DYNAMIC CHARACTERISTICS									
Power Gain	G_P	f = 100 Mc/s		Fig.11	10	12	–	dB	Fig.9
Noise Figure	NF	f = 100 Mc/s		Fig.11	–	6.3	9	dB	Fig.10
Common Mode Rejection Ratio	CMR	f = 1 Kc/s		Fig.13	–	98	–	dB	Fig.12
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 Mc/s		Fig.14	-60	–	–	dB	NONE

DEFINITIONS OF TERMS

Input Offset Voltage

The difference in the dc voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

Input Offset Current

The difference in the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Bias Current

The average value (one-half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Quiescent Operating Current

The average (dc) value of the current in either output terminal.

Quiescent Operating Current Ratio

The ratio of the Quiescent operating currents in the two output terminals.

Device Dissipation

The total power drain of the device with no signal applied and no external load current.

Power Gain

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

Noise Figure

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

Common-Mode Rejection Ratio

The ratio of the full differential voltage gain to the common-mode voltage gain.

Common-Mode Voltage Gain

The ratio of the signal voltages developed between the two output terminals to the signal voltage applied to the two input terminals connected in parallel for ac.

Differential Voltage Gain

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at ac ground.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device.

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3004

INPUT OFFSET VOLTAGE AND CURRENT VS TEMPERATURE

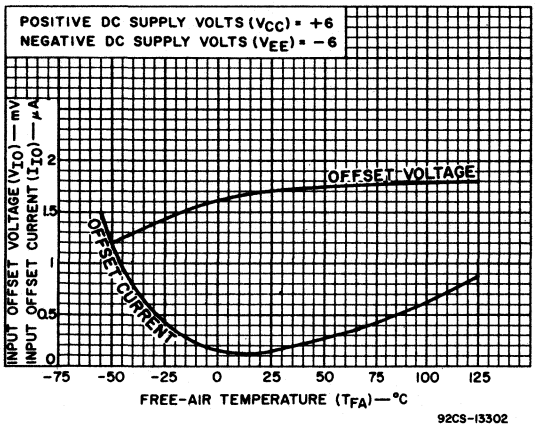


Fig.2

INPUT BIAS CURRENT VS TEMPERATURE

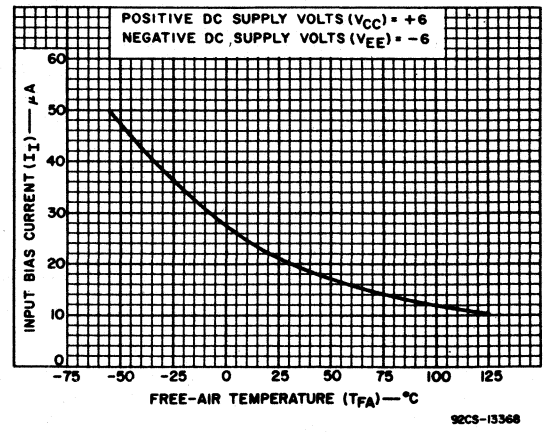


Fig.3

INPUT OFFSET VOLTAGE TEST CIRCUIT

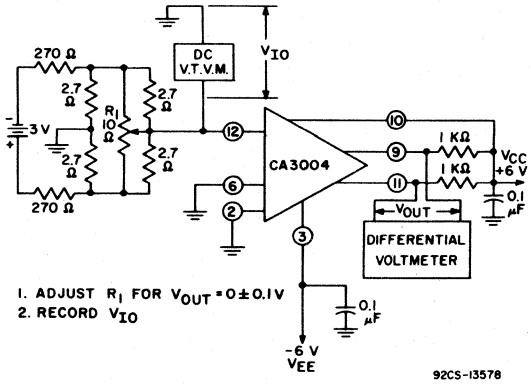


Fig.4

INPUT OFFSET CURRENT AND BIAS CURRENT TEST CIRCUIT

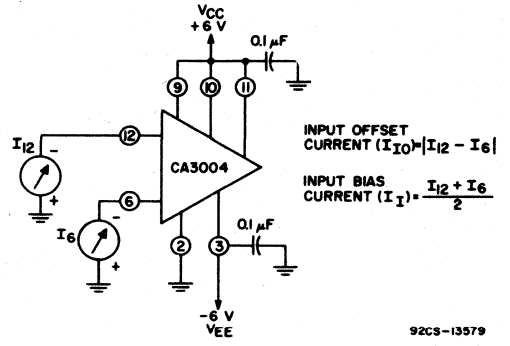


Fig.5

QUIESCENT OPERATING CURRENT VS TEMPERATURE

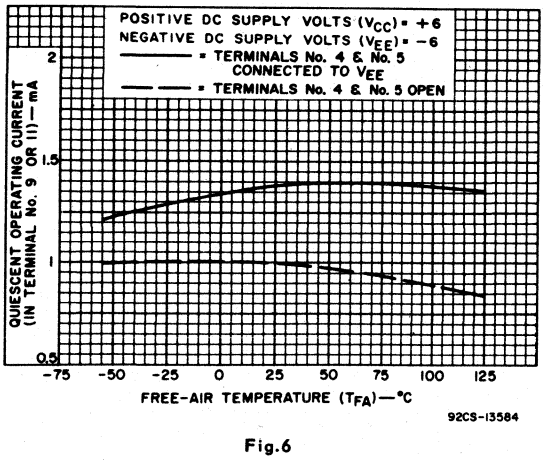


Fig.6

QUIESCENT OPERATING CURRENT RATIO VS TEMPERATURE

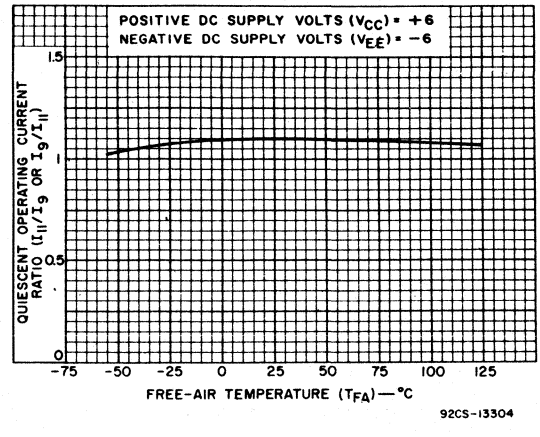
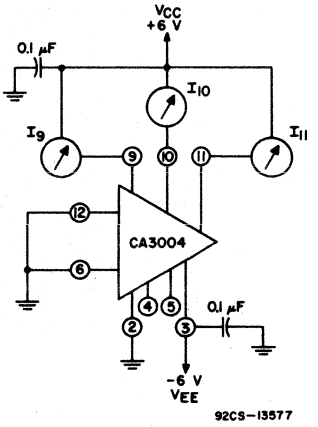


Fig.7

TEST CIRCUIT FOR TYPE CA3004

QUIESCENT OPERATING CURRENT, QUIESCENT OPERATING CURRENT RATIO, AND DEVICE DISSIPATION TEST CIRCUIT



$$P_T = V_{CC}(I_9 + I_{10} + I_{11}) + V_{EE} I_3$$

Fig.8

TYPICAL DYNAMIC CHARACTERISTICS FOR TYPE CA3004

POWER GAIN VS FREQUENCY

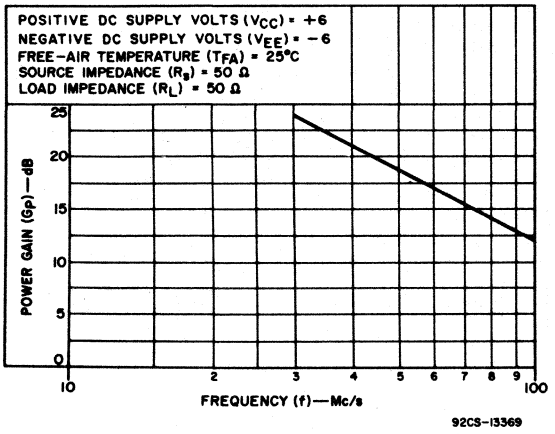


Fig.9

NOISE FIGURE VS FREQUENCY

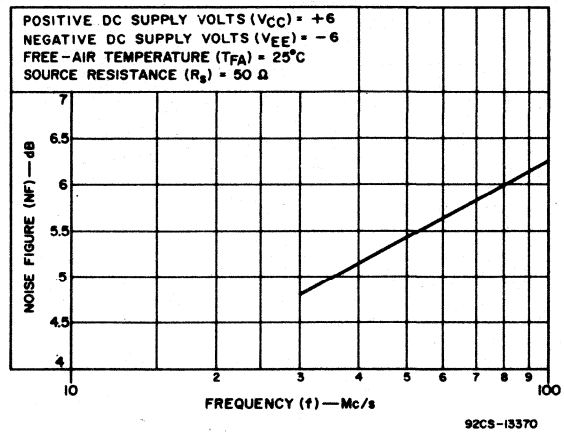


Fig. 10

CA3004

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3004

100 Mc/s POWER GAIN AND NOISE FIGURE TEST CIRCUIT

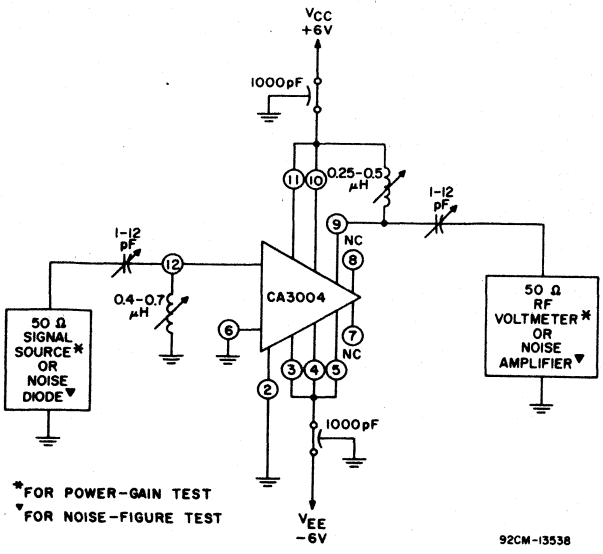


Fig. 11

COMMON-MODE REJECTION RATIO VS TEMPERATURE

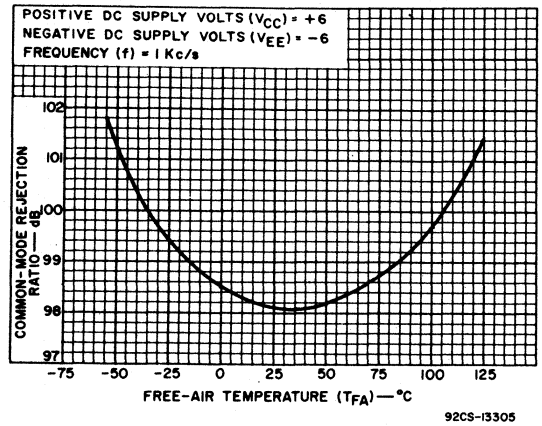


Fig. 12

COMMON-MODE REJECTION RATIO TEST CIRCUIT

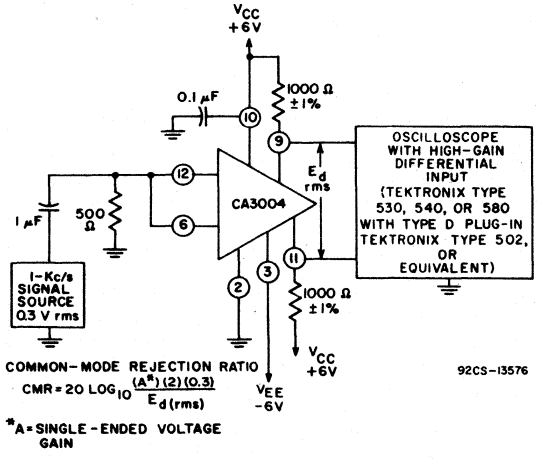


Fig. 13

AGC RANGE TEST CIRCUIT

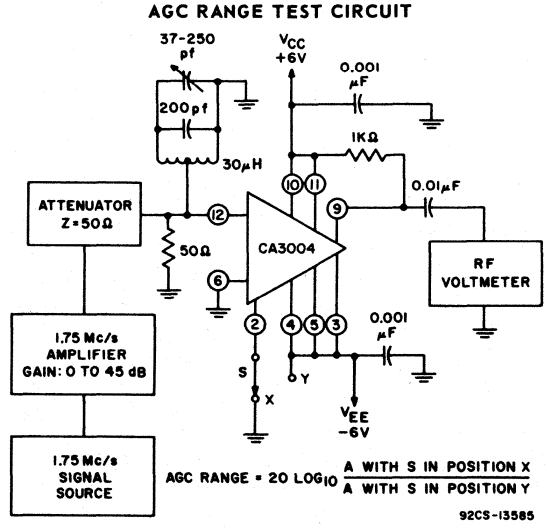


Fig. 14

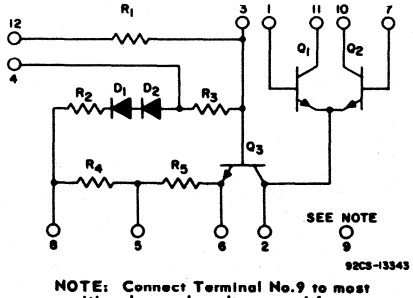
12-Lead TO-5

H-1463

RF Amplifiers

Features:

- *Designed for use in communications equipment*
- *Balanced differential amplifier configuration with controlled constant-current source to provide unexcelled versatility*
- *Built-in temperature stability for operation from −55° C to +125° C*
- *Companion Application Note, ICAN 5022 "Application of RCA CA3004, CA3005, and CA3006 Integrated Circuit RF Amplifiers", covers characteristics of different operating modes, noise performance, cross-modulation, mixer, AGC limiter, detector, and amplifier design considerations.*



NOTE: Connect Terminal No.9 to most positive dc supply voltage used for circuit.

Fig. 1 — Schematic Diagram for CA3005 and CA3006.

Applications:

- *Push-pull input and output*
- *Wide and narrow band amplifier*
- *AGC*
- *Detector*
- *RF, IF, and video frequency capability*
- *Operation from DC to 100 MHz*
- *Mixer*
- *Limiter*
- *Modulator*
- *Cascade Amplifier*

CA3005, CA3006

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_{FA} = 25°C

Voltage limits shown for each terminal can be applied under the indicated voltage conditions for other terminals.
All voltages are with respect to GROUND (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-3.5	+3.5	7 8 9 10 11 12	0 -6 +6 +6 +6 0
2	TEST POINT: DO NOT APPLY VOLTAGE FROM EXTERNAL SOURCE			
3	-9.5	0	1 7 8 9 10 11 12	0 0 -9.5 +6 +6 +6 0
4	-6	0	1 7 8 9 10 11 12	0 0 -6 +6 +6 +6 0
5	-12	0	1 7 9 10 11 12	0 0 +6 +6 +6 0
6	-6	0	1 7 9 10 11 12	0 0 +6 +6 +6 -6
7	-3.5	+3.5	1 8 9 10 11 12	0 -6 +6 +6 +6 0

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	-12	0	1 7 9 10 11 12	0 0 +6 +6 +6 0
9	0	+12	1 7 8 10 11 12	0 0 -6 +6 +6 0
10	0	+12	1 7 8 9 11 12	0 0 -6 +6 +6 0
11	0	+12	1 7 8 9 10 12	0 0 -6 +6 +6 0
12	-9.5	0	8 9 10 11	-9.5 +6 +6 +6
CASE	Internally connected to Terminal No.8 (substrate) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE . . . . . -55°C to +125°C

STORAGE-TEMPERATURE RANGE . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

MAXIMUM SINGLE-ENDED INPUT-
SIGNAL VOLTAGE . . . . . ±3.5 V

MAXIMUM COMMON-MODE INPUT-
SIGNAL VOLTAGE . . . . . -2.5 V, +3.5 V

MAXIMUM DEVICE DISSIPATION . . . . . 300 mW

ECTRICAL CHARACTERISTICS, at $T_A = 25^oC$, $V_{CC} = +6V$, $V_{EE} = -6V$

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.3,4,5, and 6 Not Connected Except Where Noted	TEST CIRCUITS	LIMITS							TYPICAL CHARAC-TERISTICS CURVES
				TYPE CA3005			TYPE CA3006				
			Fig.	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
ATIC CHARACTERISTICS											
ut Offset Voltage	V_{IO}		Fig.3	–	2.6	5	–	0.8	1	mV	Fig.2
ut Offset Current	I_{IO}		Fig.4	–	1.4	–	–	1.4	–	μA	Fig.2
ut Bias Current	I_{IB}		Fig.4	–	19	40	–	19	40	μA	Fig.5
escent erating rrent	I_{10} or I_{11}	TERMINALS 4 / 5: NC / NC	Fig.8	–	1	–	–	1	–	mA	Fig.6
		NC / -V_{EE}	Fig.8	–	2.7	–	–	2.7	–	mA	NONE
		-V_{EE} / NC	Fig.8	–	0.45	–	–	0.45	–	mA	NONE
		-V_{EE} / -V_{EE}	Fig.8	–	1.25	–	–	1.25	–	mA	Fig.6
escent Operating rrent Ratio	$\frac{I_{10}}{I_{11}}$		Fig.8	–	1.05	–	–	1.05	–	–	Fig.7
ice Dissipation	P_T		Fig.8	–	26	–	–	26	–	mW	NONE
NAMIC CHARACTERISTICS											
wer Gain	G_p	f = 100 MHz, Cascode Configuration	Fig.10	16	20	–	16	20	–	dB	Fig.9
		f = 100 MHz, Differential-Ampl. Configuration	Fig.12	14	16	–	14	16	–	dB	Fig.11
se Figure	NF	f = 100 MHz, Cascode Configuration	Fig.10	–	7.8	9	–	7.8	9	dB	Fig.13
		f = 100 MHz, Differential Ampl. Configuration	Fig.12	–	7.8	9	–	7.8	9	dB	Fig.14
mmon-Mode ejection Ratio	CMR	f = 1 kHz	Fig.16	–	101	–	–	101	–	dB	Fig.15
C Range (Max. Voltage ain to Complete Cutoff)	AGC	f = 1.75 MHz	Fig.17	-60	–	–	-60	–	–	dB	NONE

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPES CA3005 AND CA3006

INPUT OFFSET VOLTAGE AND CURRENT

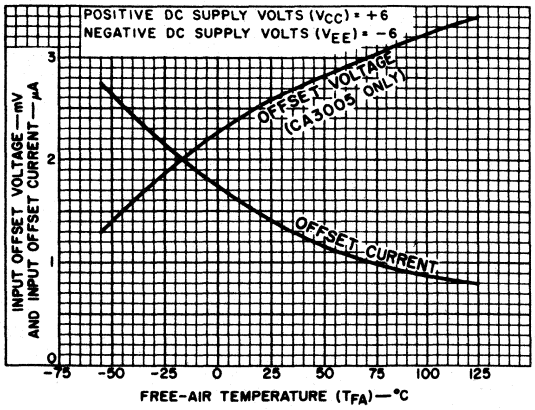


Fig.2

INPUT OFFSET VOLTAGE TEST CIRCUIT

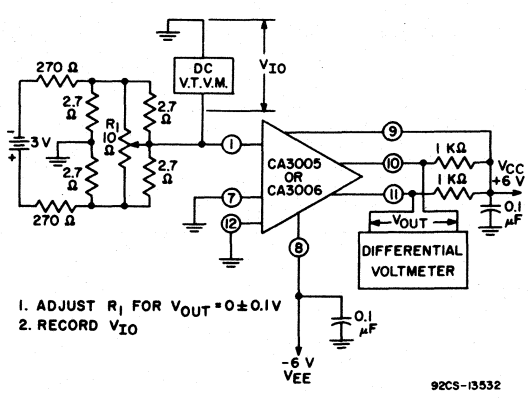


Fig.3

INPUT BIAS CURRENT

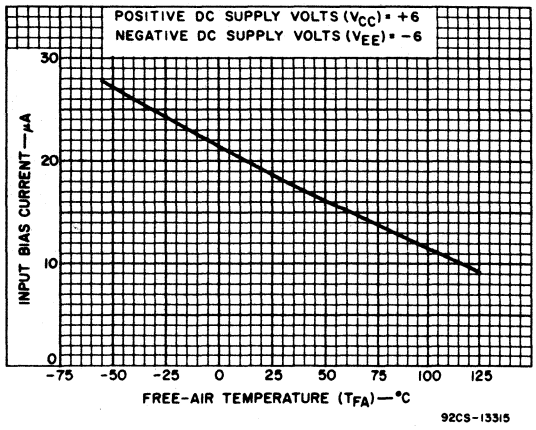


Fig. 4

QUIESCENT OPERATING CURRENT

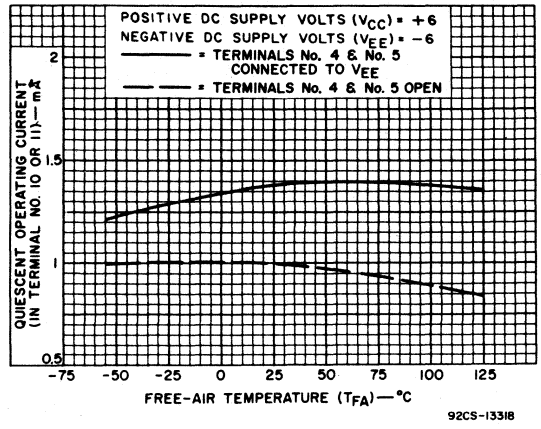


Fig.5

QUIESCENT OPERATING CURRENT RATIO

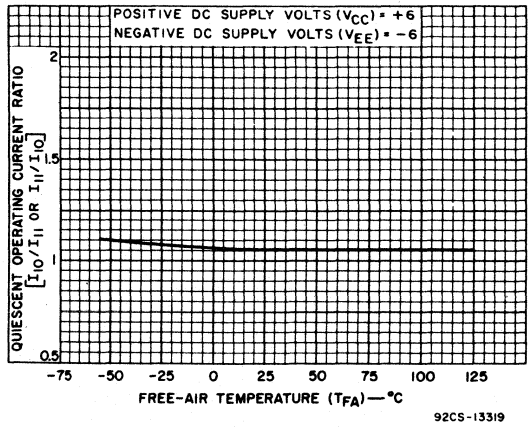


Fig.6

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPES CA3005 AND CA3006

POWER-GAIN (CASCODE CONFIGURATION)

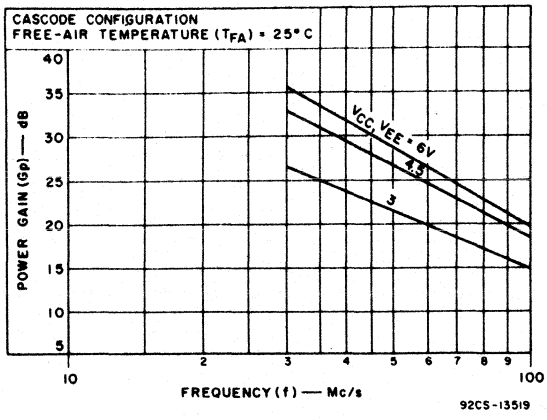


Fig.7

POWER-GAIN (DIFFERENTIAL-AMPLIFIER CONFIGURATION)

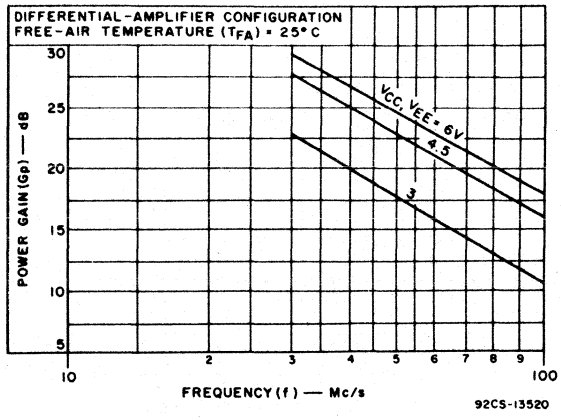
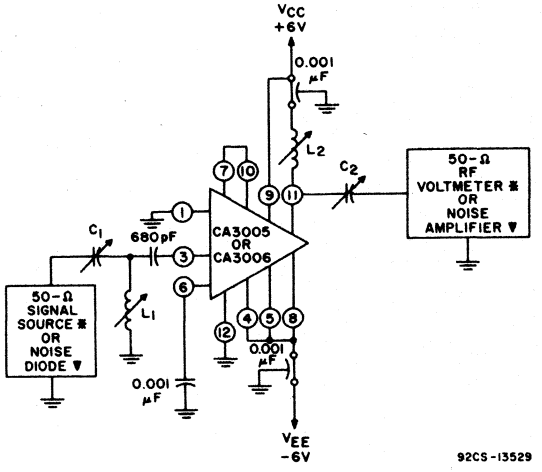


Fig.9

NOISE FIGURE AND POWER GAIN TEST CIRCUIT (CASCODE CONFIGURATION)



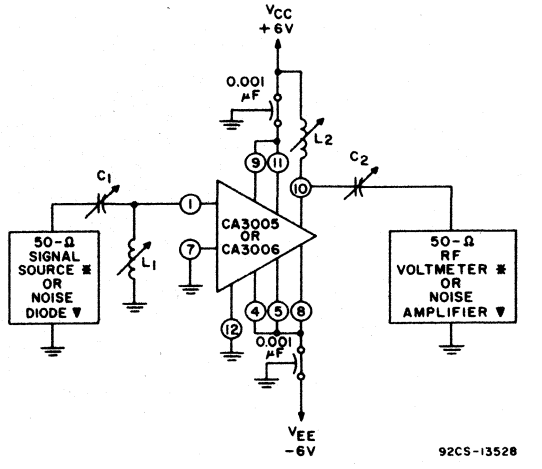
f Mc/s	C_1 pF	C_2 pF	L_1 μH	L_2 μH
30	14-150	5-40	0.3-0.6	0.8-1.4
100	5-40	5-40	0.07-0.12	0.15-0.3

* FOR POWER-GAIN TEST

▼ FOR NOISE-FIGURE TEST

Fig. 8

NOISE FIGURE AND POWER-GAIN TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION)



f Mc/s	C_1 pF	C_2 pF	L_1 μH	L_2 μH
30	5-40	1.5-20	1.2-2	1.2-2
100	1-12	1-12	0.4-0.7	0.25-0.5

* FOR POWER-GAIN TEST

▼ FOR NOISE-FIGURE TEST

Fig. 10

TYPICAL DYNAMIC CHARACTERISTICS FOR TYPES CA3005 AND CA3006

100-Mc/s NOISE FIGURE VS. V_{EE} (CASCODE CONFIGURATION)

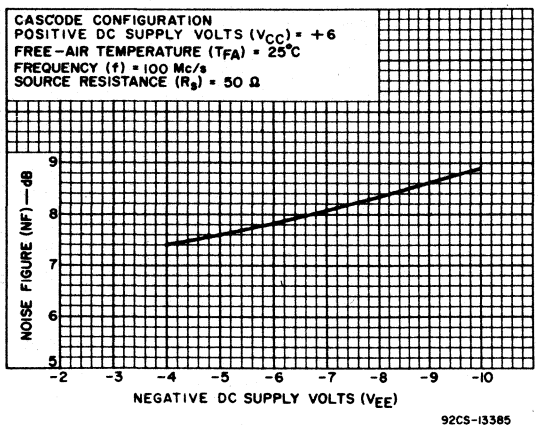


Fig. 11

100 Mc/s NOISE FIGURE VS. V_{EE} (DIFFERENTIAL AMPLIFIER CONFIGURATION)

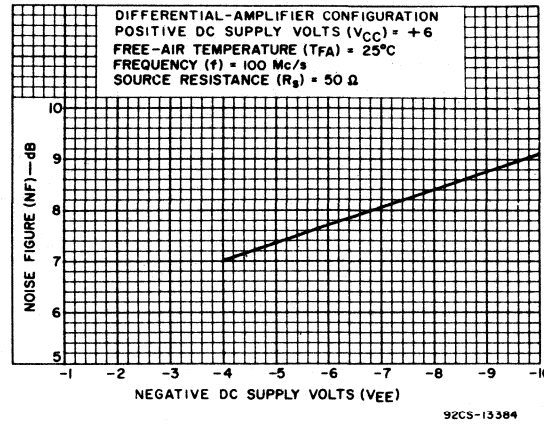


Fig. 12

COMMON-MODE-REJECTION RATIO

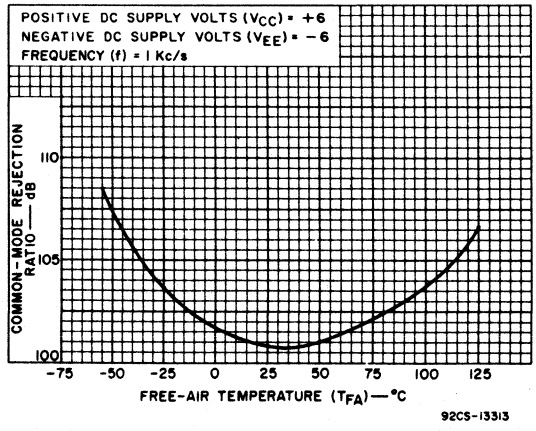


Fig. 13

TYPICAL DYNAMIC TEST CIRCUITS FOR TYPES CA3005 AND CA3006

COMMON-MODE REJECTION RATIO TEST CIRCUIT

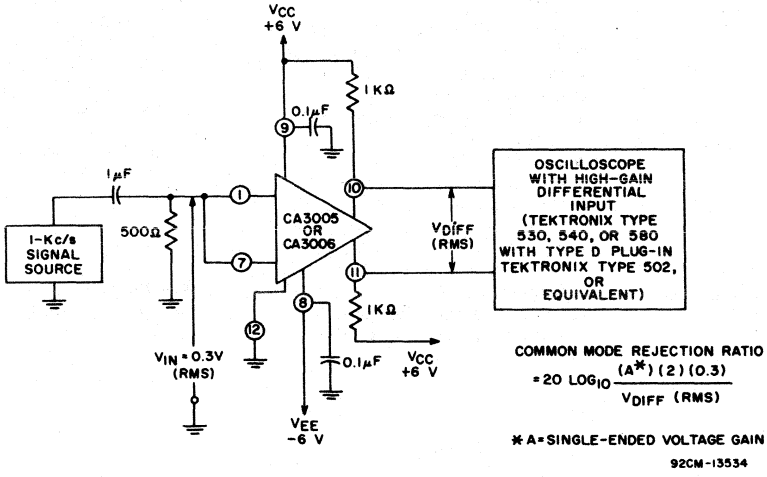


Fig. 14

AGC RANGE TEST CIRCUIT

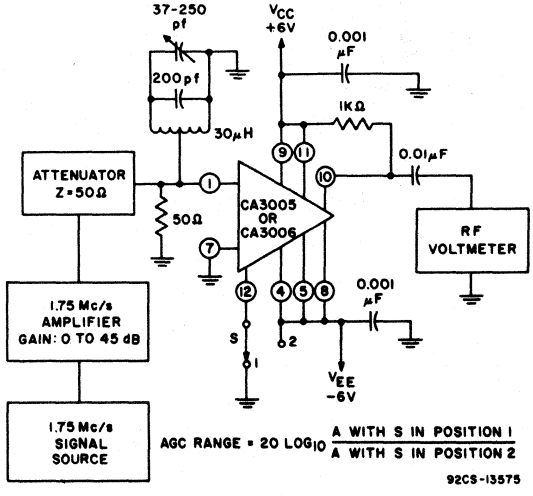


Fig. 15

CA3007

12-Lead TO-5

H-1463

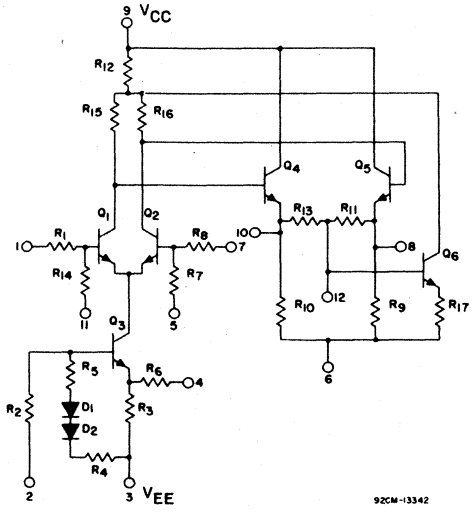
AF Amplifier

Features:

- *Input impedance - 4 kΩ typ.*
- *Output impedance - 60 Ω typ.*
- *Power gain - 22 dB typ.*
- *Push-pull input & output*
- *Direct coupling to class B audio output stage*
- *Designed for use in sound systems and communication equipment*
- *Balanced differential-amplifier configuration with controlled constant-current source provides for both audio amplification and phase inversion*
- *Built-in temperature stability for operation from −55° C to +125° C*
- *Eliminates need for audio driver transformer*
- *Companion Application Note, ICAN 5037 "Application of the RCA-CA3007 Integrated Circuit Audio Driver" covers design of a dual supply audio driver in a direct-coupled audio amplifier, and a single supply audio driver in a capacitor-coupled audio amplifier*

Applications

- *Audio amplifier*
- *Audio driver*



SCHEMATIC DIAGRAM

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_A = 25° C

Indicated voltage limits for each terminal can be applied under the specified operating conditions for other terminals. All voltages are with respect to ground (-V_{CC}, +V_{EE}, or common terminal of Positive and Negative DC supplies).

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
2	-8	0	3	-8
			6	0
			7	0
			9	+6
			11	0
3	-10	0	6	0
			7	0
			9	+6
			11	0
4	-8.5	0	6	0
			7	0
			9	+6
			11	0
5	-2.5	+2.5	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
6	-3	0	2	0
			3	-6
			7	0
			9	+6
			11	0
7	-2.5	+2.5	1	0
			2	0
			3	-6
			5	0
			6	0
			9	+6
8	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
9	0	+10	2	0
			3	-6
			6	0
			7	0
			11	0
10	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
11	-2.5	+2.5	1	0
			2	0
			3	-6
			6	0
			7	0
			9	+6
12	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE . . . . . -55°C to +125°C

STORAGE-TEMPERATURE RANGE . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

MAXIMUM SINGLE-ENDED INPUT-
SIGNAL VOLTAGE . . . . . ±2.5 V

MAXIMUM COMMON-MODE INPUT-
SIGNAL VOLTAGE . . . . . ±2.5 V

MAXIMUM DEVICE DISSIPATION . . . . . 300 mW

CA3007

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V_{CC} = +6 V, V_{EE} = -6 V,

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Pin 4 Not Connected Unless Otherwise Noted	TEST CIRCUITS	LIMITS TYPE CA3007				TYPICAL CHARACTERISTICS CURVES
			Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS								
Input Unbalance Voltage	V_{IU}		3	–	0.57	5	mV	2
Input Unbalance Current	I_{IU}		3	–	0.57	5	μA	2
Input Bias Current	I_I		3	–	11	34	μA	4
Quiescent Operating Voltage	V_8 or V_{10}		3	–	0.87	–	V	5
Device Dissipation	P_T		3	–	30	–	mW	NONE
DYNAMIC CHARACTERISTICS								
Power Gain	G_P	f = 1 kHz	6	20	22	–	dB	NONE
Total Harmonic Distortion	THD	f = 1 kHz	6	–	0.28	–	%	NONE
Input Impedance	Z_{IN}	f = 1 kHz	7	–	4K	–	Ω	NONE
Common-Mode Rejection Ratio	CMR	f = 1 kHz	9(A) 9(B)	–	77	–	dB	8

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUIT FOR CA3007

INPUT UNBALANCE VOLTAGE AND CURRENT vs TEMPERATURE

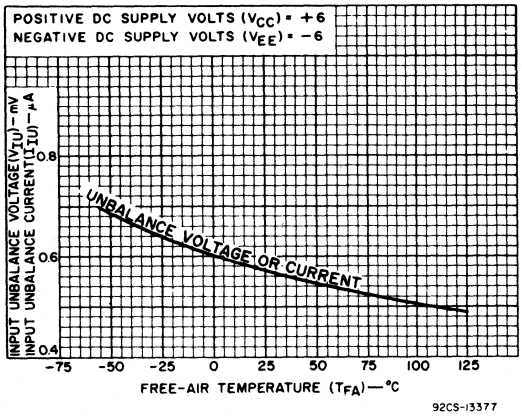
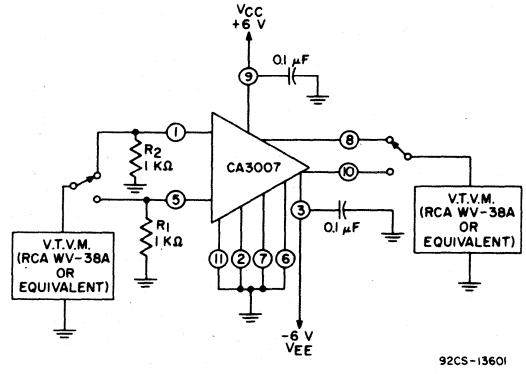


Fig.2

INPUT UNBALANCE VOLTAGE & CURRENT, INPUT BIAS CURRENT, QUIESCENT OPERATING VOLTAGE, AND DEVICE DISSIPATION TEST CIRCUIT



R_1 and R_2 matched to ± 1%.

$P_T = V_{CC}I_9 + V_{EE}I_3$

I_9 = Direct Current into Terminal No.9

I_3 = Direct Current out of Terminal No.3

Fig.3

INPUT BIAS CURRENT vs TEMPERATURE

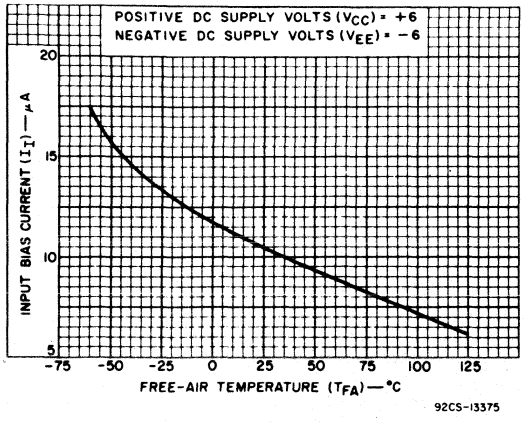


Fig.4

QUIESCENT OPERATING VOLTAGE vs TEMPERATURE

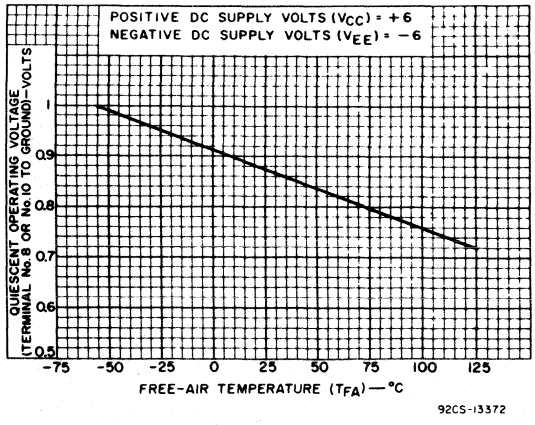
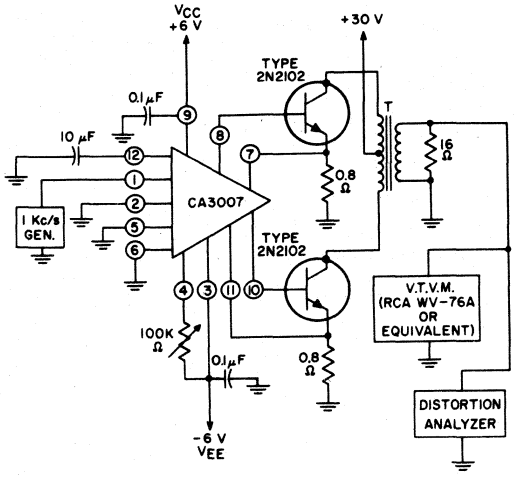


Fig.5

TYPICAL DYNAMIC TEST CIRCUITS FOR CA3007

POWER GAIN AND TOTAL HARMONIC DISTORTION TEST CIRCUIT



T (Output Transformer):
Primary Impedance = 2000 Ω C.T.
Secondary Impedance = 16 Ω
Efficiency = 45% approx.
(STANCOR TYPE TA-10 OR EQUIVALENT)

Fig.6

INPUT IMPEDANCE TEST CIRCUIT

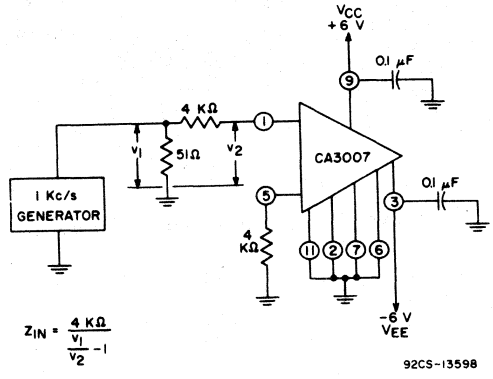


Fig.7

TYPICAL DYNAMIC CHARACTERISTIC AND TEST CIRCUITS FOR CA3007

COMMON-MODE REJECTION RATIO vs TEMPERATURE

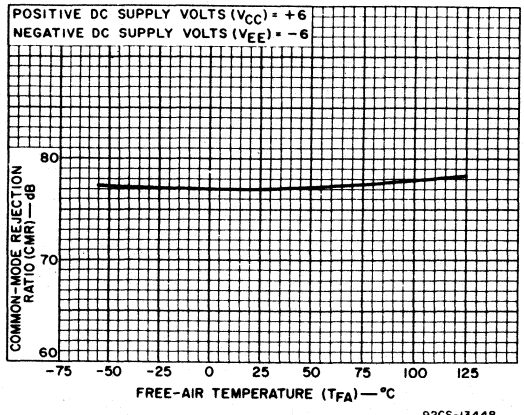
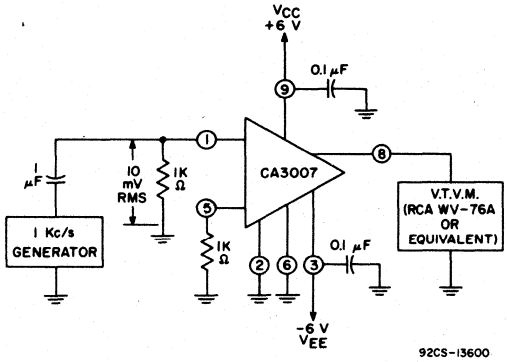


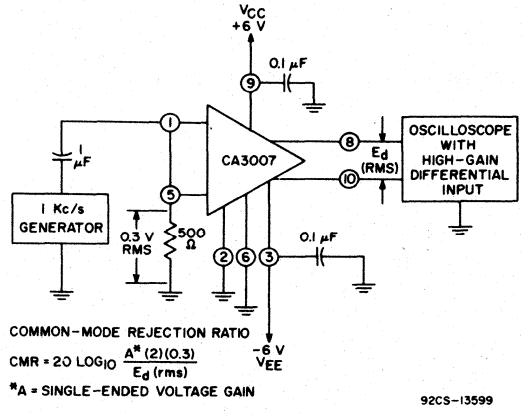
Fig.8

COMMON-MODE REJECTION-RATIO TEST CIRCUITS

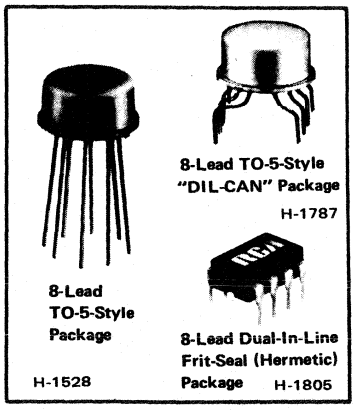


(A) Single-Ended Differential Voltage Gain

Fig.9



(B) Common-Mode Voltage Gain



DIFFERENTIAL/CASCODE AMPLIFIERS

For Communications and Industrial Equipment at Frequencies from DC to 120 MHz

FEATURES

- Controlled for Input Offset Voltage, Input Offset Current, and Input Bias Current (CA3028 Series only)
- Balanced Differential Amplifier Configuration with Controlled Constant-Current Source
- Single- and Dual-Ended Operation
- Operation from DC to 120 MHz
- Balanced-AGC Capability
- Wide Operating-Current Range

The CA3028A and CA3028B are differential/cascode amplifiers designed for use in communications and industrial equipment operating at frequencies from dc to 120 MHz.

The CA3028B is like the CA3028A but is capable of premium performance particularly in critical dc and differential amplifier applications requiring tight controls for input offset voltage, input offset current, and input bias current.

The CA3053 is similar to the CA3028A and CA3028B but is recommended for IF amplifier applications.

The CA3028A, CA3028B, and CA3053 are supplied in a hermetic 8-lead TO-5-style package. The "F" versions are supplied in a frit-seal TO-5 package, and the "S" versions in formed-lead (DIL-CAN) packages.

APPLICATIONS

- RF and IF Amplifiers (Differential or Cascode)
- DC, Audio, and Sense Amplifiers
- Converter in the Commercial FM Band
- Oscillator • Mixer • Limiter
- Companion Application Note, ICAN 5337 "Application of the RCA CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges." This note covers characteristics of different operating modes, noise performance, mixer, limiter, and amplifier design considerations.

The CA3028A, CA3028B, and CA3053 are available in the packages shown below. When ordering these devices, it is important to add the appropriate suffix letter to the device.

Package 8-Lead TO-5	Suffix Letter	CA3028A	CA3028B	CA3053
TO-5	T	√	√	√
With Dual-In-Line Formed Leads (DIL-CAN)	S	√	√	√
Frit-Seal Ceramic	F	√	√	√
Beam-Lead	L	√		
Chip	H	√		

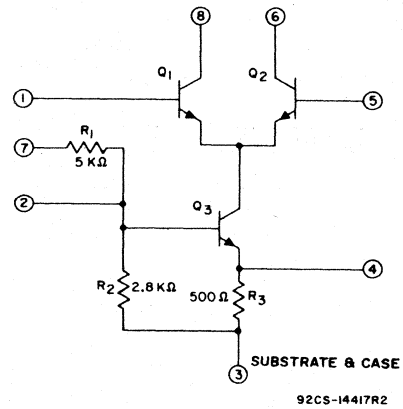


Fig.1 - Schematic diagram for CA3028A, CA3028B and CA3053.

CA3028A, CA3028B, CA3053 Types

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

DISSIPATION:

At T_A up to 55°C
(CA3028AF, CA3028BF, CA3053F) ..... 750 mW

At T_A > 55°C
(CA3028AF, CA3028BF, CA3053F) ..... Derate linearly 6.67 mW/°C

At T_A up to 85°C
(CA3028A, CA3028B, CA3053) ..... 450 mW

At T_A > 85°C
(CA3028A, CA3028B, CA3053) Derate linearly 5 mW/°C

AMBIENT-TEMPERATURE RANGE:

Operating ..... −55°C to +125°C

Storage ..... −65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL No.	1	2	3	4	5	6	7	8
1		0 to -15▲	0 to -15▲	0 to -15▲	+5 to -5	*	*	+20⊕ to 0
2			+5 to -11	+5 to -1	+15♦ to 0	*	+15♦ to 0	*
3‡				+10 to 0	+15♦ to 0	+30● to 0	+15♦ to 0	+30● to 0
4					+15♦ to 0	*	*	*
5						+20⊕ to 0	*	*
6							*	*
7								*
8								

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal terminal 4 with respect to terminal 2 is -1 to +5 volts.

‡ Terminal #3 is connected to the substrate and case.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.

▲ Limit is -12V for CA3053

⊕ Limit is +15V for CA3053

♦ Limit is +12V for CA3053

● Limit is +24V for CA3028A and +18V for CA3053

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CIRCUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A			LIMITS TYPE CA3028B			LIMITS TYPE CA3053			UNITS	TYPICAL CHARACTERISTICS CURVES Fig.
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
STATIC CHARACTERISTICS															
			$+V_{CC}$	$-V_{EE}$											
Input Offset Voltage	V_{IO}	2	6V 12V	6V 12V	- -	- -	- -	- -	0.98 0.89	5 5	- -	- -	- -	mV	4
Input Offset Current	I_{IO}	3a	6V 12V	6V 12V	- -	- -	- -	- -	0.56 1.06	5 6	- -	- -	- -	μA	4
Input Bias Current	I_I	3a	6V 12V	6V 12V	- -	16.6 36	70 106	- -	16.6 36	40 80	- -	- -	- -	μA	5a
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	29 36	85 125		5b
Quiescent Operating Current	I_6 or I_8	3a	6V 12V	6V 12V	0.8 2	1.25 3.3	2 5	1 2.5	1.25 3.3	1.5 4	- -	- -	- -	mA	6a 7
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	1.2 2.0	2.2 3.3	3.5 5.0		6b
AGC Bias Current (Into Constant-Current Source Terminal No.7)	I_7	8a	12V 12V	V_{AGC} =+9 V_{AGC} = +12	- -	1.28 1.65	- -	- -	1.28 1.65	- -	- -	- -	- -	mA	8b
		-	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	1.15 1.55	- -		-
Input Current (Terminal No.7)	I_7	-	6V 12V	6V 12V	0.5 1	0.85 1.65	1 2.1	0.5 1	0.85 1.65	1 2.1	- -	- -	- -	mA	-
Device Dissipation	P_T	3a	6V 12V	6V 12V	24 120	36 175	54 260	24 120	36 175	42 220	- -	- -	- -	mW	9
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	50 100	80 150		-

ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A Min.	Typ.	Max.	LIMITS TYPE CA3028B Min.	Typ.	Max.	LIMITS TYPE CA3053 Min.	Typ.	Max.	UNITS	TYPICAL CHARAC-TERISTICS CURVE Fig.
DYNAMIC CHARACTERISTICS															
Power Gain	G_P	10a	f = 100 MHz	Cascode	16	20	-	16	20	-	-	-	-	dB	10b
		11a,d	V_{CC} = +9V	Diff.-Ampl.	14	17	-	14	17	-	-	-	-		11b,e
		10a	f = 10.7 MHz	Cascode	35	39	-	35	39	-	35	39	-	dB	10b *
		11a	V_{CC} = +9V	Diff.-Ampl.	28	32	-	28	32	-	28	32	-		11b *
Noise Figure	NF	10a	f = 100 MHz	Cascode	-	7.2	9	-	7.2	9	-	-	-	dB	10c
		11a,d	V_{CC} = +9V	Diff.-Ampl.	-	6.7	9	-	6.7	9	-	-	-		11c,e
Input Admittance	Y_{11}	-	f = 10.7 MHz V_{CC} = +9V	Cascode				-	0.6 + j 1.6	-				mmho	12
		-		Diff.-Ampl.				-	0.5 + j 0.5	-					13
Reverse Transfer Admittance	Y_{12}	-		Cascode				-	0.0003 - j0	-				mmho	14
		-		Diff.-Ampl.				-	0.01 - j0.0002	-					15
Forward Transfer Admittance	Y_{21}	-		Cascode				-	99 - j18	-				mmho	16
		-		Diff.-Ampl.				-	-37 + j0.5	-					17
Output Admittance	Y_{22}	-		Cascode				-	0. + j0.08	-				mmho	18
		-		Diff.-Ampl.				-	0.04 + j0.23	-					19
Power Output (Untuned)	P_o	20a	f = 10.7 MHz	Diff.-Ampl. 50 Ω Input-Output	-	5.7	-	-	5.7	-	-	-	-	μW	20b
AGC Range (Max. Power Gain to Full Cutoff)	AGC	21a	V_{CC} = +9V	Diff.-Ampl.	-	62	-	-	62	-	-	-	-	dB	21b
Voltage Gain at f = 10.7 MHz	A	22a	f = 10.7 MHz	Cascode	-	40	-	-	40	-	-	40	-	dB	22b
		22c	V_{CC} = +0V R_L = 1 kΩ	Diff. Ampl.	-	30	-	-	30	-	-	30	-		22d
Voltage Gain Differential at f = 1 kHz		23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	35	38	42	-	-	-	dB	-
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	-	-	40	42.5	45	-	-	-		
Max. Peak-to-Peak Output Voltage at f = 1 kHz	V_o(P-P)	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	7	11.5	-	-	-	-	V_{P-P}	-
			V_{CC} = +12V, V_{EE} = -12V R_L = 1.6 kΩ		-	-	-	15	23	-	-	-	-		
Bandwidth at -3 dB point	BW	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	-	7.3	-	-	-	-	MHz	-
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	-	-	-	8	-	-	-	-		
Common-Mode Input-Voltage Range	V_{CMR}	24	V_{CC} = +6V, V_{EE} = -6V		-	-	-	-2.5	(-3.2 - 4.5)	4	-	-	-	V	-
			V_{CC} = +12V, V_{EE} = -12V		-	-	-	-5	(-7 - 9)	7	-	-	-		
Common-Mode Rejection Ratio	CMR	24	V_{CC} = +6V, V_{EE} = -6V		-	-	-	60	110	-	-	-	-	dB	-
			V_{CC} = +12V, V_{EE} = -12V		-	-	-	60	90	-	-	-	-		
Input Impedance at f = 1 kHz	Z_{IN}		V_{CC} = +6V, V_{EE} = -6V		-	-	-	-	5.5	-	-	-	-	kΩ	-
			V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	3	-	-	-	-		
Peak-to-Peak Output Current	I_{P-P}		V_{CC} = +9V	f = 10.7 MHz	2	4	7	2.5	4	6	2	4	7	mA	-
			V_{CC} = +12V	e_{in} = 400 mV Diff.-Ampl.	3.5	6	10	4.5	6	8	3.5	6	10		

* Does not apply to CA3053

CA3028A, CA3028B, CA3053 Types

DEFINITIONS OF TERMS

AGC Bias Current

The current drawn by the device from the AGC-voltage source, at maximum AGC voltage.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device.

Common-Mode Rejection Ratio

The ratio of the full differential voltage gain to the common-mode voltage gain.

Device Dissipation

The total power drain of the device with no signal applied and no external load current.

Input Bias Current

The average value (one-half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Offset Current

The difference in the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Offset Voltage

The difference in the dc voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

Noise Figure

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

Power Gain

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

Quiescent Operating Current

The average (dc) value of the current in either output terminal.

Voltage Gain

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at ac ground.

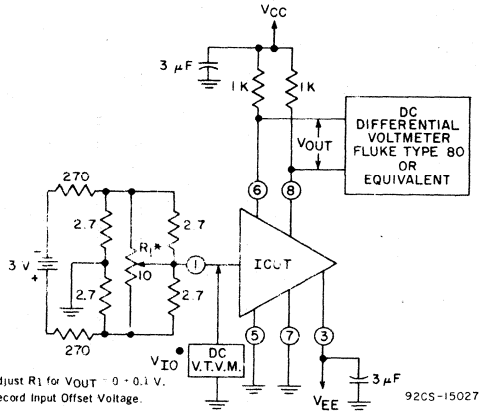


Fig.2 - Input offset voltage test circuit for CA3028B.

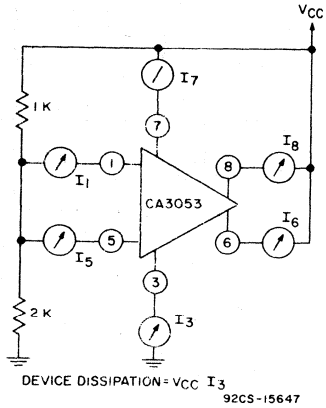


Fig.3b - Input bias current, device dissipation, and quiescent operating current test circuit for CA3053.

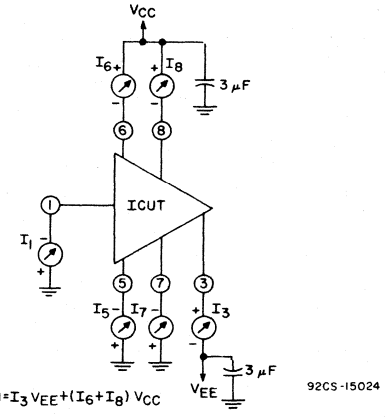


Fig.3a - Input offset current, input bias current, device dissipation, and quiescent operating current test circuit for CA3028A and CA3028B.

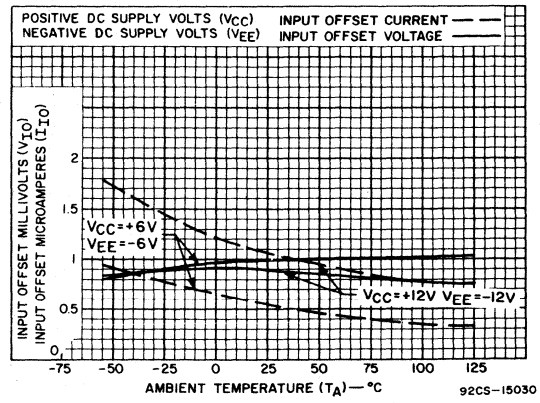


Fig.4 - Input offset voltage and input offset current for CA3028B.

TYPICAL CHARACTERISTICS

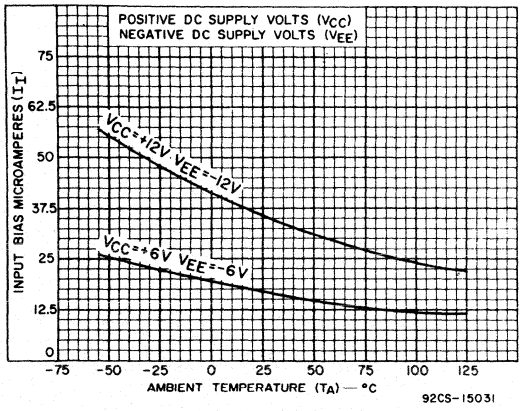


Fig.5a - Input bias current vs. ambient temperature for CA3028A and CA3028B.

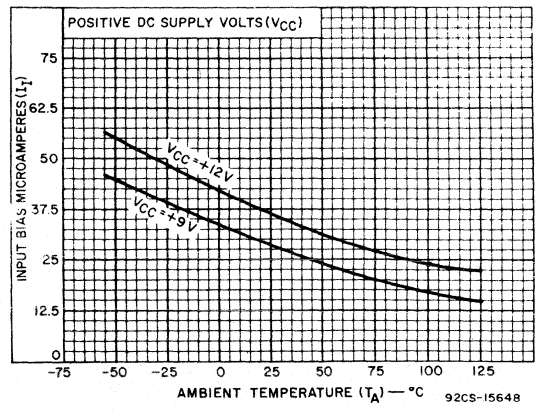


Fig.5b - Input bias current vs. ambient temperature for CA3053.

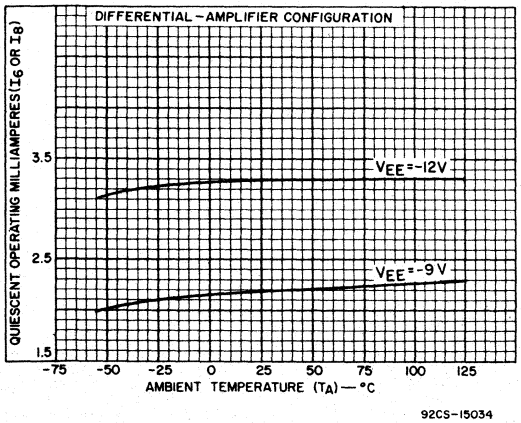


Fig.6a - Quiescent operating current vs. ambient temperature for CA3028A and CA3028B.

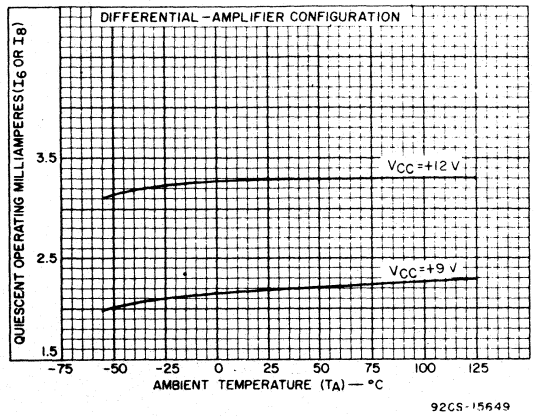


Fig.6b - Quiescent operating current vs. ambient temperature for CA3053.

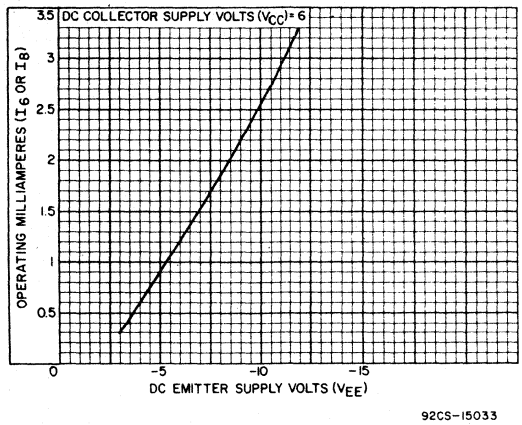


Fig.7 - Operating current vs. V_{EE} voltage for CA3028A and CA3028B.

TYPICAL CHARACTERISTICS AND TEST CIRCUITS

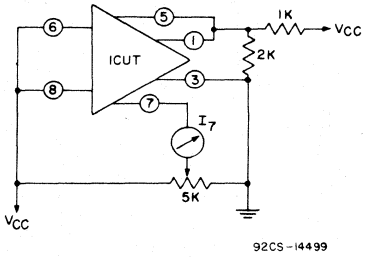


Fig.8a - AGC bias current test circuit (differential-amplifier configuration) for CA3028A and CA3028B.

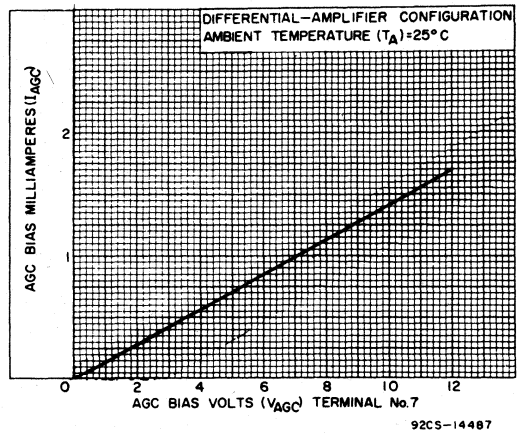


Fig.8b - AGC bias current vs. bias volts (terminal No.7) for CA3028A and CA3028B.

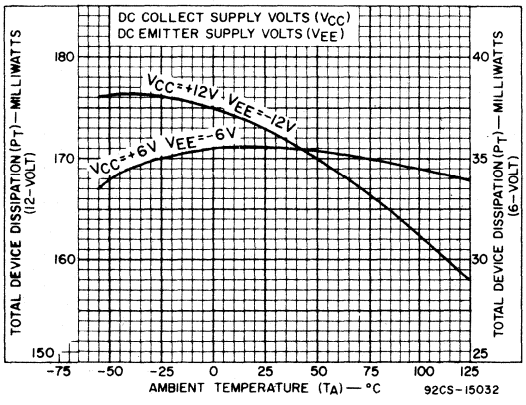
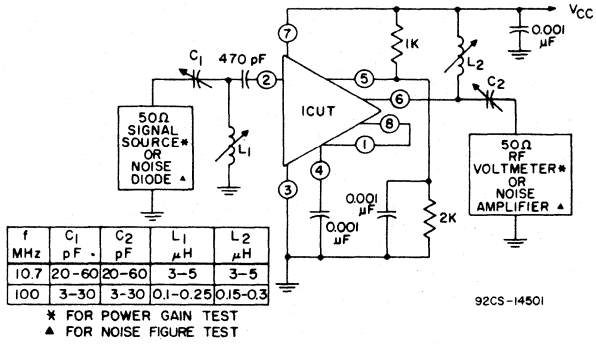


Fig.9 - Device dissipation vs. temperature for CA3028A and CA3028B.



f MHz	C1 pF	C2 pF	L1 µH	L2 µH
10.7	20-60	20-60	3-5	3-5
100	3-30	3-30	0.1-0.25	0.15-0.3

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig.10a - Power gain and noise figure test circuit (cascode configuration) for CA3028A, CA3028B and CA3053.*

* 10.7 MHz Power Gain Test Only.

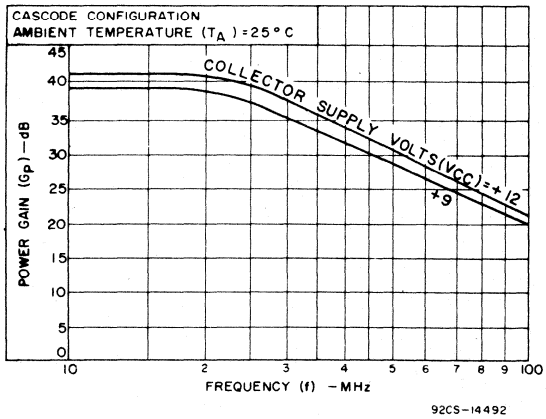


Fig.10b - Power gain vs. frequency (cascode configuration) for CA3028A and CA3028B.

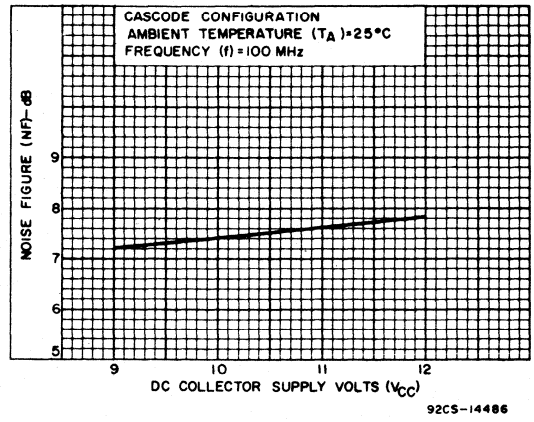
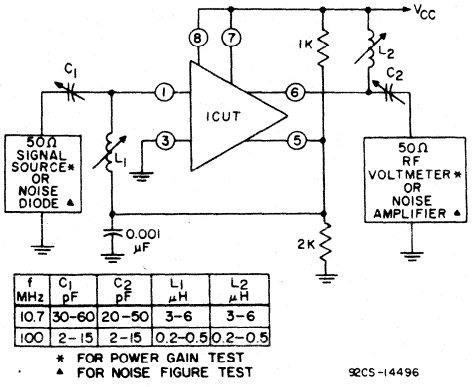


Fig.10c - 100 MHz noise figure vs. collector supply volts (cascode configuration) for CA3028A and CA3028B.

TYPICAL NOISE FIGURE AND POWER GAIN TEST CIRCUITS AND CHARACTERISTICS



f MHz	C_1 pF	C_2 pF	L_1 μH	L_2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

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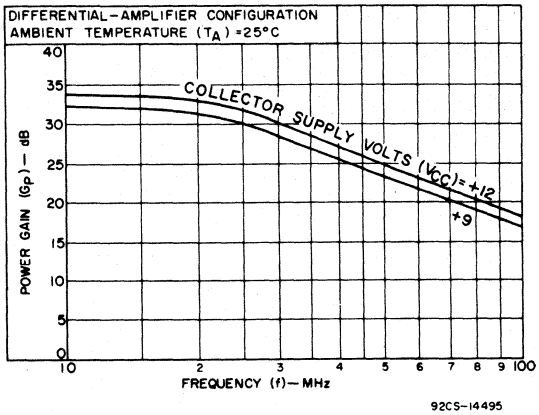
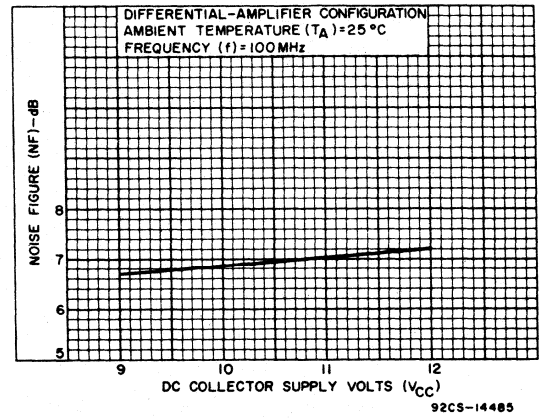
Fig.11a - Power gain and noise figure test circuit (differential-amplifier configuration and terminal No.7 connected to V_{CC}) for CA3028A, CA3028B and CA3053.*

* 10.7 MHz Power Gain Test Only.



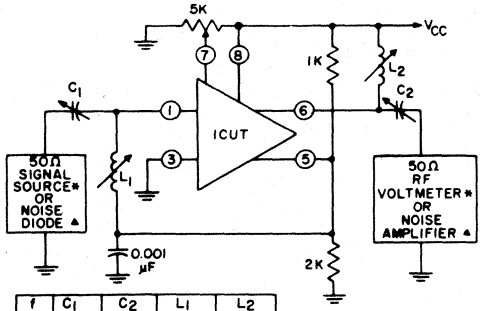
92CS-14495

Fig.11b - Power gain vs. frequency (differential-amplifier configuration) for CA3028A and CA3028B.



92CS-14485

Fig.11c - 100 MHz noise figure vs. collector supply voltage (differential-amplifier configuration) for CA3028A and CA3028B.

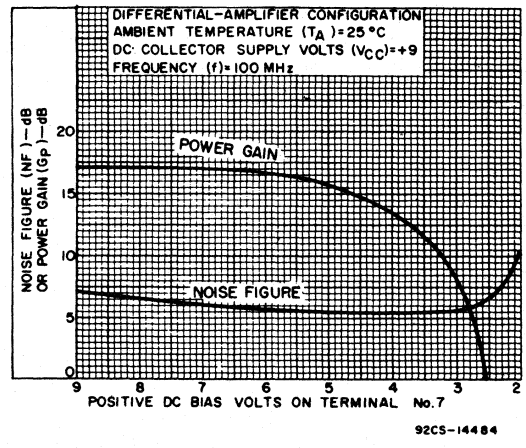


f MHz	C_1 pF	C_2 pF	L_1 μH	L_2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

92CS-14516

Fig.11d - Power gain and noise figure test circuit (differential-amplifier configuration for CA3028A and CA3028B.



92CS-14484

Fig.11e - 100 MHz noise figure and power gain vs. base-to-emitter bias (terminal No.7) for CA3028A and CA3028B.

TYPICAL ADMITTANCE PARAMETERS

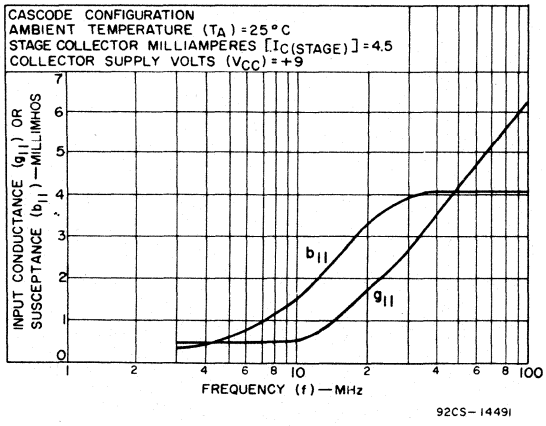


Fig.12 - Input admittance (Y_{11}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

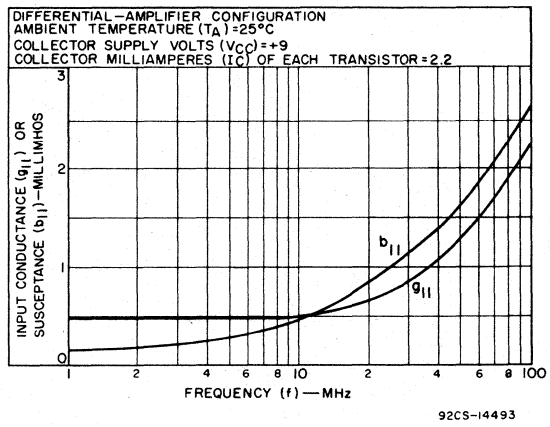


Fig.13 - Input admittance (Y_{11}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

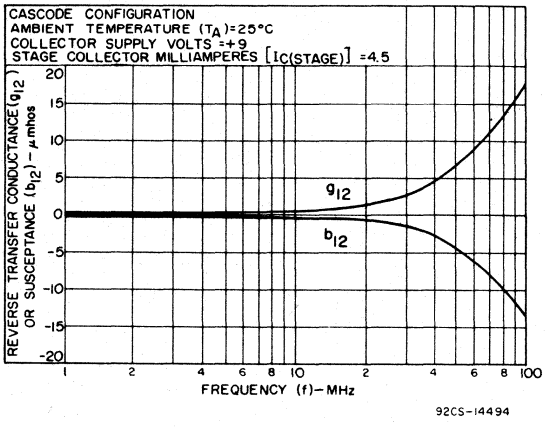


Fig.14 - Reverse transadmittance (Y_{12}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

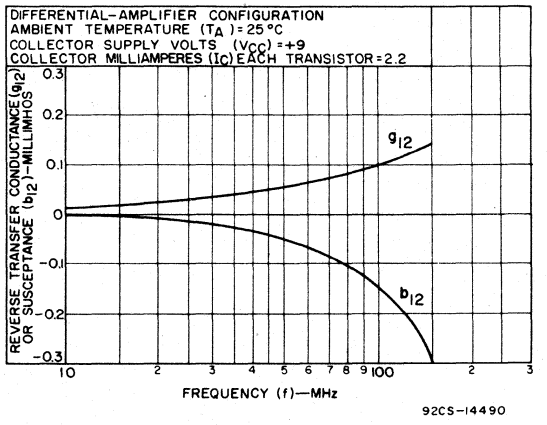


Fig.15 - Reverse transadmittance (Y_{12}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

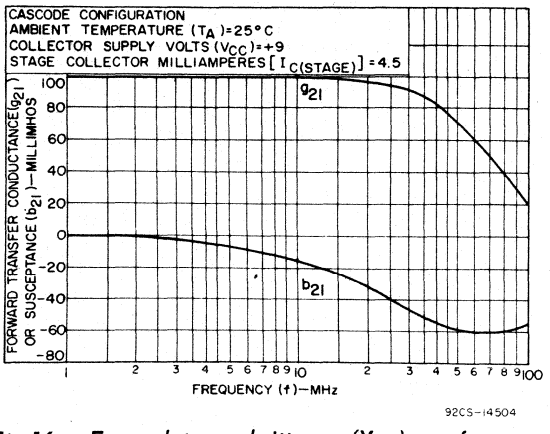


Fig.16 - Forward transadmittance (Y_{21}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

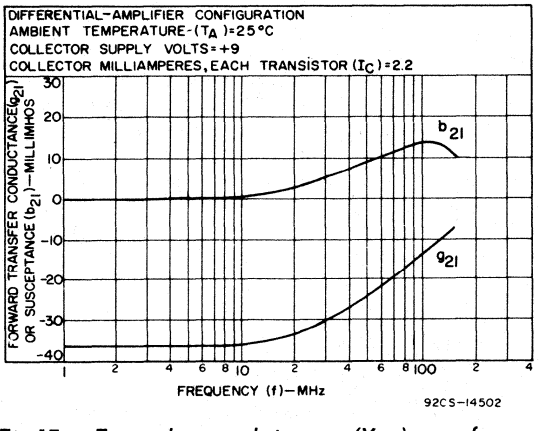


Fig.17 - Forward transadmittance (Y_{21}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

TYPICAL ADMITTANCE PARAMETERS

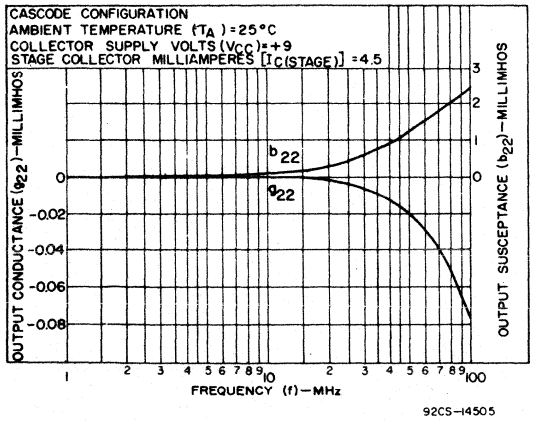


Fig.18 - Output admittance (Y_{22}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

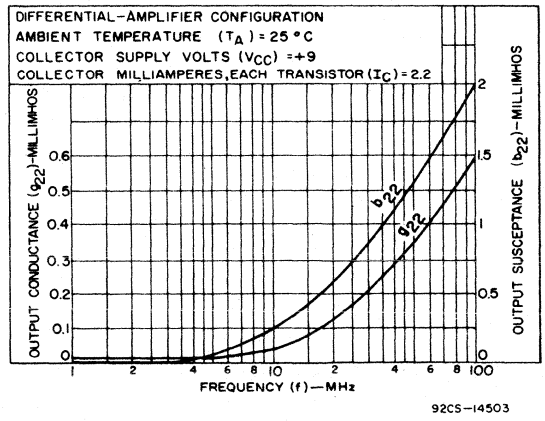


Fig.19 - Output admittance (Y_{22}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

TYPICAL TEST CIRCUITS AND CHARACTERISTICS

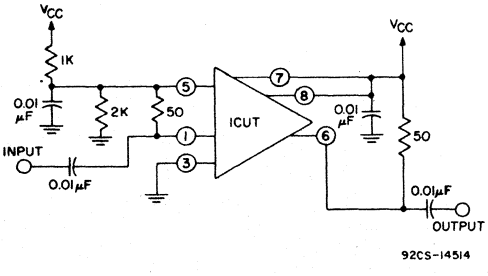


Fig.20a - Output power test circuit for CA3028A and CA3028B.

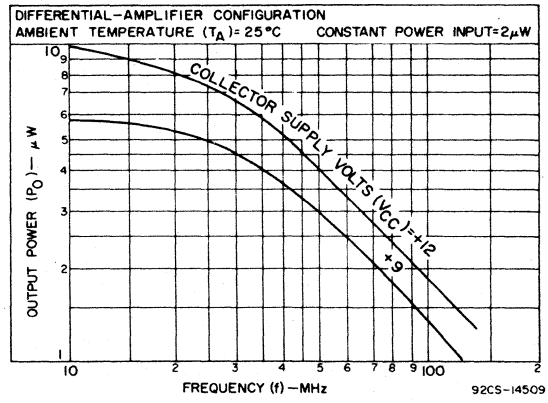
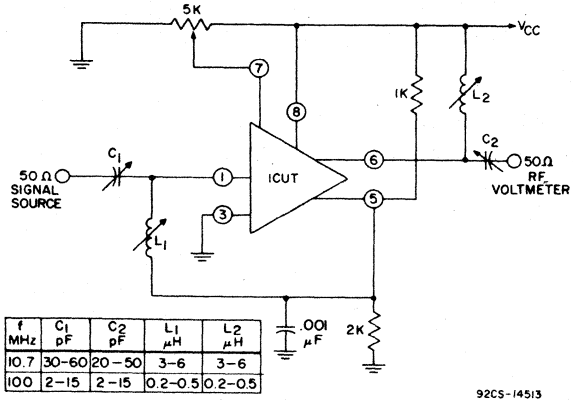


Fig.20b - Output power vs. frequency — 50 Ω input and 50 Ω output (differential-amplifier configuration) for CA3028A and CA3028B.



f MHz	C1 pF	C2 pF	L1 μH	L2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

Fig.21a - AGC range test circuit (differential amplifier) for CA3028A and CA3028B.

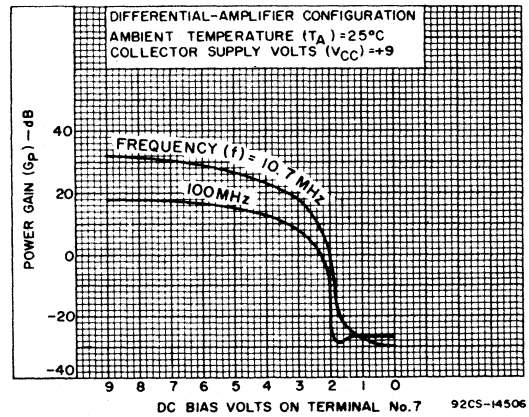


Fig.21b - AGC characteristics for CA3028A and CA3028B.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS

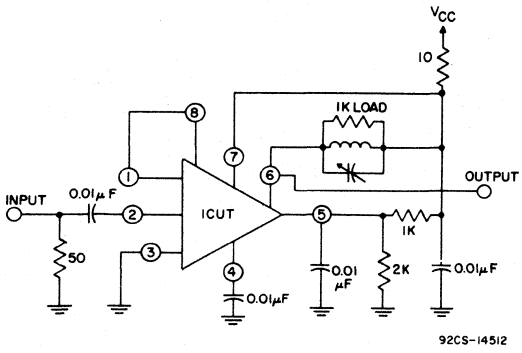


Fig.22a - Transfer characteristic (voltage gain) test circuit (10.7 MHz) cascode configuration for CA3028A, CA3028B and CA3053.

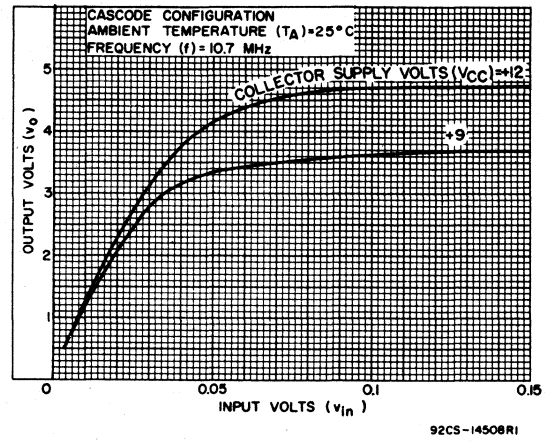


Fig.22b - Transfer characteristics (cascode configuration) for CA3028A, CA3028B and CA3053.

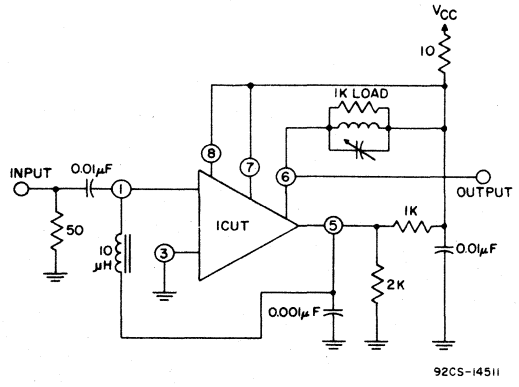


Fig.22c - Transfer characteristic (voltage gain) test circuit (10.7 MHz) differential-amplifier configuration for CA3028A, CA3028B and CA3053.

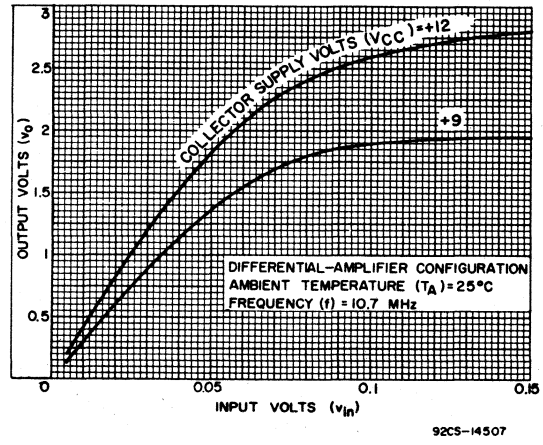
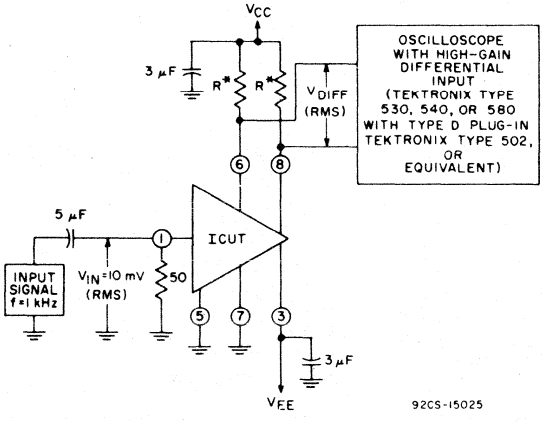
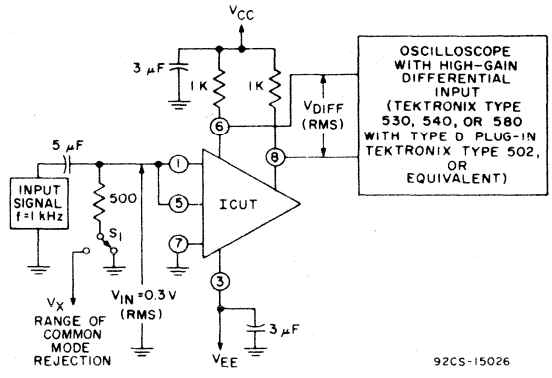


Fig.22d - Transfer characteristics (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.



* For R = 1.6 kΩ – (V_{CC} = 12V, V_{EE} = -12V)
For R = 2 kΩ – (V_{CC} = 6V, V_{EE} = -6V)

Fig.23 - Differential voltage gain, maximum peak-to-peak output voltage, and bandwidth test circuit for CA3028B.



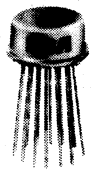
For CMR test: S_1 to ground
For input common-mode voltage range test: S_1 to V_X

Common mode rejection ratio = $20 \log_{10} \frac{(A^*)\ (2)\ (0.3)}{V_{DIFF}\ (RMS)}$

* A = Single-ended voltage gain.

Fig.24 - Common-mode rejection ratio and common-mode input-voltage range test circuit for CA3028B.

CA3040



12-Lead TO-5 Style

H-1463

Video and Wide-band Amplifier

For Industrial and Commercial Equipment at Frequencies up to 200 MHz

Features:

- *High differential push-pull voltage gain - 37 dB typ.*
- *Single-ended voltage gain - 31 dB typ.*
- *Wide [3dB] bandwidth - 55 MHz typ.*
- *Balanced input and output*
- *High input resistance - 150 kΩ typ.*
- *Low output resistance - 125 Ω typ.*
- *Bias options for temperature compensation:*
  Bias Mode A: "Constant" Voltage
  Bias Mode B: "Constant" Gain

Applications

- *Video amplifier*
- *Schmitt trigger*
- *Modulator*
- *IF Amplifier*
- *Mixer*
- *DC Amplifier*
- *Sense Amplifier*

The RCA CA3040 is a monolithic silicon integrated circuit designed to meet the requirements of a wide variety of applications requiring high gain and wide bandwidth. The cascode-connected differential amplifier achieves a double-ended gain of 37 dB with a typical 3 dB bandwidth of 55 MHz. Emitter-Follower input and output stages provide the desirable high input impedance and output impedance for coupling to other circuits.

The CA3040 includes two biasing options, allowing the user to optimize his design over the entire military temperature range of −55 to +125° C. **Bias Mode A** yields a substantially constant voltage at the output terminals for applications using DC coupling to succeeding stages or requiring maximum dynamic range over the temperature range. DC output voltage varies less than 0.1 volt (typically) over the entire temperature range while gain varies ± 2 dB. **Bias Mode B** provides extremely stable gain over the temperature range. Gain variation is 0 dB (typically) in this Bias Mode. DC variation is ± 0.8 volt.

Provisions are also made for stabilizing the operating point for either single or split power supplies.

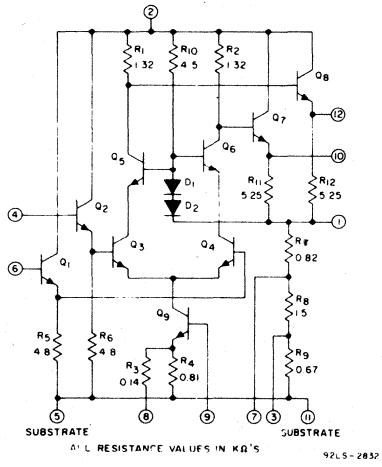


Fig. 1 — Schematic Diagram for CA3040.

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION * . . . . . 450 mW
Derating factor for T_A > 85°C . . . . . 5 mW/°C
TEMPERATURE RANGE:
Operating . . . . . -55°C to +125°C
Storage . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

* Limitation imposed by the thermal resistance of package.

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 2 with respect to terminal 11 is 0 to +14 volts.

TERMINAL No.	1	2	3	4	5▲	6	7	8	9	10	11▲	12
1		0 -14	*	*	+14 0	*	+10 -10	*	*	*	+14 0	*
2			*	+14 0	+14 0	+14 0	*	*	*	+14 0	+14 0	+14 0
3				*	+5 -3	*	*	*	*	*	+5 -3	*
4					*	+3 -3	*	*	*	*	*	*
5▲					▲	*	+10 -3	*	+3 -7	*	0 Note 1	*
6							*	*	*	*	*	*
7								*	*	*	+10 -3	*
8									+3 -3	*	*	*
9										*	+7 -3	*
10											*	*
11▲											▲	*
12												

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	5
2	-	-
3	5	5
4	1	0.1
5	-	-
6	1	0.1
7	5	5
8	5	5
9	1	0.1
10	-	10
11	-	-
12	-	10

▲ Reference Substrate

Note 1: External connection required for proper operation.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

CA3040

ELECTRICAL CHARACTERISTICS AT T_A = 25°C Unless Otherwise Specified

Characteristics	Symbols	Test Circuits	Special Test Conditions	Limits CA3040			Units	Typical Characteristics Curves
		Fig.		Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS	V_{CC} = +6V, V_{EE} = -6V							
Output Voltage	V_{10} or V_{12}	2(a) 2(b)	Bias Mode Switch A or B: Closed	1.4	2.7	3.7	V	9
Base Bias Voltage	V_9	2(a)	Bias Mode A Switch Closed	-	-1.7	-	V	-
		2(b)	Bias Mode B Switch Closed	-	-1.7	-	V	-
Input Bias Reference Voltage	V_1	2(a) 2(b)	Bias Mode Switch A or B: Open	-1	-	+1	V	9
Input Bias Current	I_4, I_6	2(a) 2(b)	Bias Mode Switch A or B: Closed	-	15	45	μA	-
Input Unbalance Current	$\lvert I_6-I_4 \rvert$	2(a) 2(b)	Bias Mode Switch A or B: Closed	-	-	6	μA	-
Power Supply Current Drain	I_2 or I_5+I_{11}	2(a)	Mode A Switch open or closed	4.7	8.5	15.5	mA	10
	I_2 or $I_5+I_8+I_{11}$	2(b)	Mode B Switch open or closed					
DYNAMIC CHARACTERISTICS	V_{CC} = +12V, V_{EE} = 0, Split Voltage Supply (Optional) = +6V							
Differential Voltage Gain								-
Single-Ended Input Differential Output	$A_{DIFF(DE)}$	3(a)	f = 1 MHz R_S = 50 Ω	34	37	-	dB	-
Single-Ended Input and Output	$A_{DIFF(SE)}$	3(a)	f = 1 MHz R_S = 50 Ω	28	31	-	dB	4,5
-3 dB Bandwidth	BW	3(a)	R_S = 50 Ω	40	55	-	MHz	4,7
Differential Voltage Gain Balance	$A_{DIFF(SE)10}$ $-A_{DIFF(SE)12}$	3(a)	f = 1 MHz	-1	0	+1	dB	-
Output Voltage Swing	V_8 or V_{10} RMS	3(a)	f = 1 MHz R_S = 50 Ω	-	0.5	-	V_{RMS}	7
Noise Figure	NF	3(a)	(Note 1) f = 30 MHz R_S = 400 Ω	-	7.5	9	dB	8
Parallel Input Resistance	R_I	3(a)	f = 1 MHz	-	150	-	kΩ	-
Parallel Input Capacitance	C_I	3(a)		-	2.2	-	pF	-
Output Resistance	R_O	3(a)		-	125	-	Ω	-
TEMPERATURE DEPENDENT CHARACTERISTICS Temperature coefficients for ambient temperature: -55°C ≤ T_A ≤ + 125°C								
Output Voltage	$\frac{\Delta V_{10} \text{ or } \Delta V_{12}}{°C}$	3(a)	Bias Mode A	-	0	-	mV/°C	9
		3(b)	Bias Mode B	-	6.4	-	mV/°C	
Power Supply Current Drain	$\Delta I_2/°C$	3(a)	Bias Mode A	-	5	-	μA/°C	11
Differential Voltage Gain	$A_{DIFF}/°C$	3(a)	Bias Mode A	-	0.0166	-	dB/°C	12
		3(b)	Bias Mode B	-	0	-		

Note 1: Replace 1-kΩ resistors between Term. 1 and 4 and Te .. 1 and 6 with suitable chokes so that reactance at 30 MH_z exceeds 5kΩ

STATIC CHARACTERISTICS TEST CIRCUITS FOR CA3040

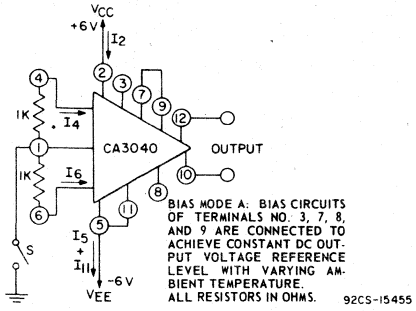


Fig.2(a) - Bias Mode A

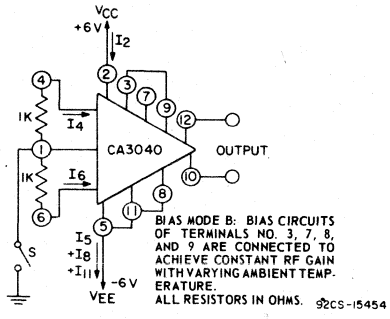
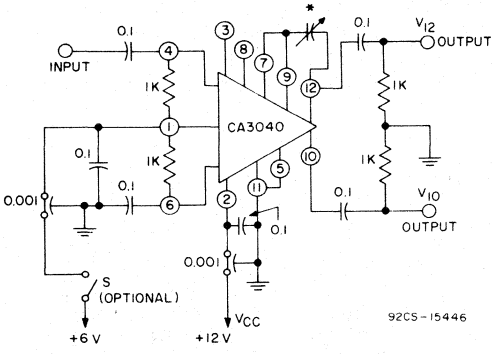


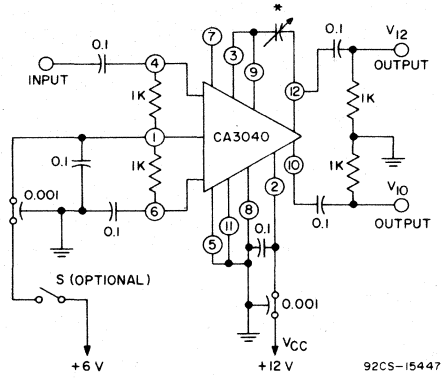
Fig.2(b) - Bias Mode B

DYNAMIC CHARACTERISTICS TEST CIRCUITS FOR CA3040



* VARIABLE CAPACITANCE (0.5 – 1.0 μF) ADJUSTMENT FOR EQUAL 3dB BANDWIDTH AT AMPLIFIER OUTPUTS, TERMINALS 10 AND 12.
ALL RESISTORS IN OHMS.
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED).
BIAS MODE A IS AS DEFINED IN FIG. 2(a)

Fig.3(a) - Bias Mode A



* SEE FIG 3(a)
BIAS MODE B IS AS DEFINED IN FIG 2(b)
ALL RESISTORS IN OHMS.
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED).

Fig.3(b) - Bias Mode B

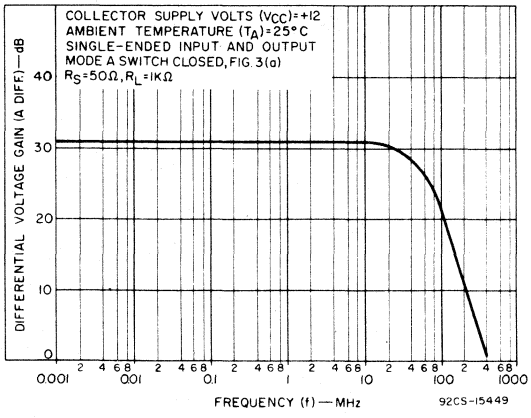


Fig.4 - Differential Voltage Gain vs Frequency

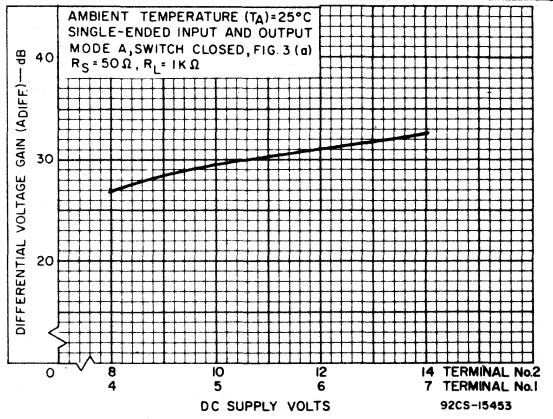


Fig.5 - Differential Voltage Gain vs DC Supply Voltages

CA3040

OPERATING CONSIDERATIONS

General

The CA3040 is designed to provide flexibility in the selection of power supply configurations and to provide the circuit designer the choice between two modes of temperature-compensated performance. Mode A, which provides constant DC output voltage, is recommended for most applications. The control of the operating point provided by this mode maintains the dynamic range of the device while gain variation over most of the range is less than ±1 dB. Mode B provides constant gain for applications where this consideration is critical, but will exhibit a reduction of dynamic range at the temperature extremes.

Power Supply Considerations

Figures 2 and 3 illustrate the use of the CA3040 with balanced dual supplies and single power supplies, respectively. Both figures demonstrate that the inputs may be directly referenced to the center point of the supply (ground in Fig.2) by closing the included switch. This is the natural connection in Fig.2. This connection is optional, however, and need not be made. Use of this connection in Fig.3 implies the presence of another DC supply or a "stiff" bleeder. If such a source is present its use is suggested in order to maintain maximum common mode range. Dynamic performance and dynamic range of the output circuit are unaffected by the choice of biasing scheme used so that in most cases direct connection of Terminal No.1 to the center point of the supply is not required. Where direct connection is not used, Terminals No.4 and No.6 must be biased from Terminal No.1 for proper operation.

High-Frequency Considerations

Stable high-frequency operation requires that proper high-frequency construction techniques be followed. The photograph of Fig.6 illustrates the precautions taken in the construction of the test circuit of Fig.3.

Extreme caution is required because of the extended gain bandwidth capability of the device. Oscillations have been observed in the 400-to-800 MHz range when precautions were not taken. In addition to normal considerations of shielding, parts layout, and isolation, the following specific suggestions are made:

1. Use sockets only when necessary. Sockets, when used, must provide shielding within the pin circle. The socket shown in the chassis of Fig.6 is a Barnes MG-1201, or equivalent, modified by drilling a 1/8" hole in the center and inserting a grounded brass pin.
2. Do not bypass Terminal No.9 in normal operation. Fig.3 shows the use of neutralization between Terminal No.9 and one output to balance the amplifier at high frequencies. Experience shows that stable operation, while possible, is difficult to achieve if Terminal No.9 is bypassed to ground.
3. In DC testing, 1 kΩ, 1/4 W carbon resistors should be soldered directly to the socket Terminals No.4 and No.6 to suppress parasitic oscillations. All current carrying connections are made at the other end of the resistors. Direct sensing of Terminal No.4 or No.6 voltage should not be attempted.

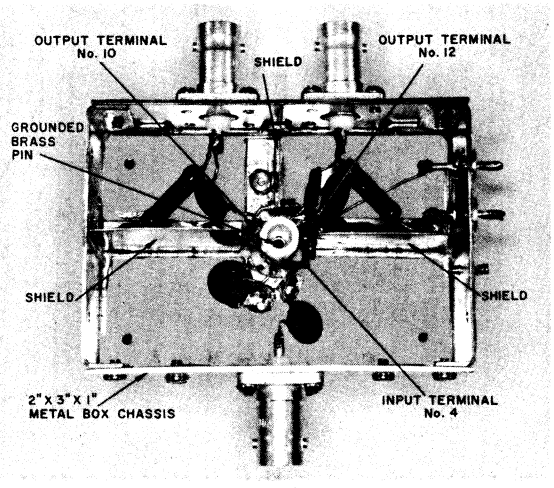


Fig.6 - Test Circuit Layout

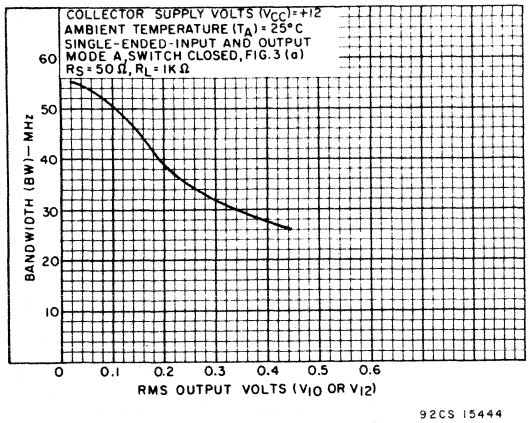


Fig.7 -3dB Bandwidth vs Single-Ended Output Voltage

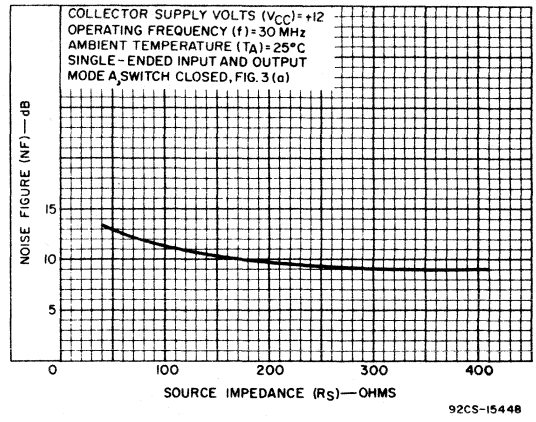


Fig.8 -Noise Figure (NF) vs Source Impedance

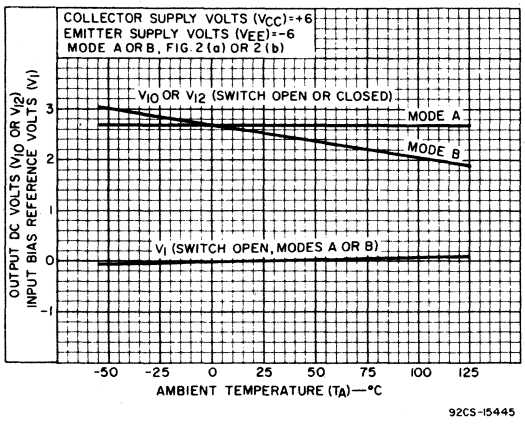


Fig.9 - Output Volts or Input Bias Reference Volts vs Ambient Temperature

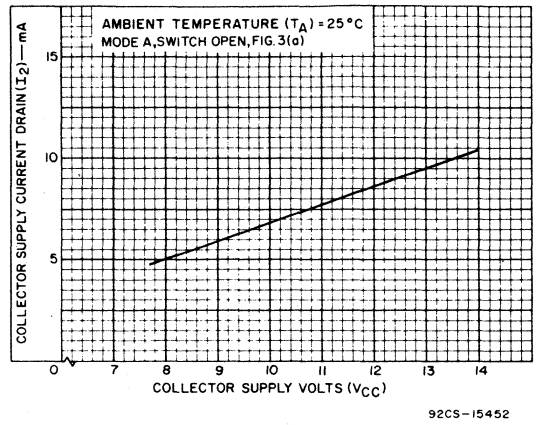


Fig.10 -Collector Supply Current Drain (I_2) vs Collector Supply Voltage (V_{CC})

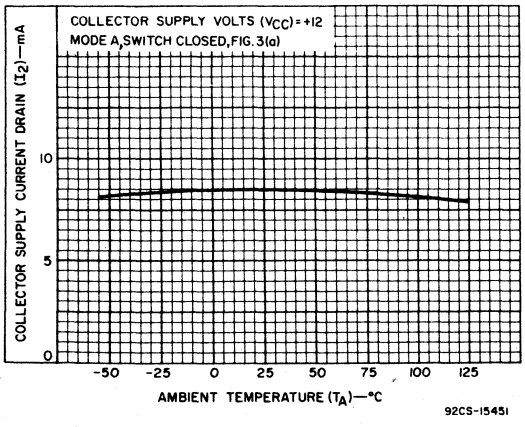


Fig.11 - Collector Supply Current Drain (I_2) vs Ambient Temperature

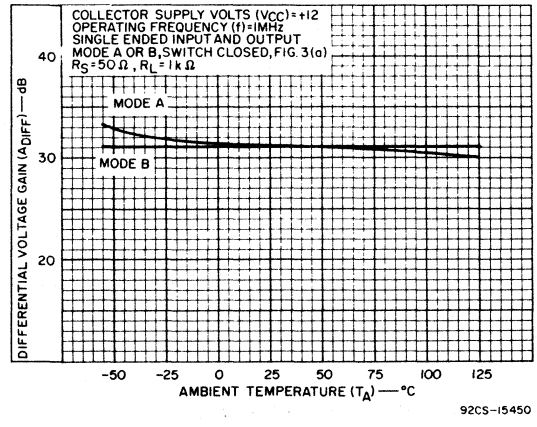


Fig.12 - Single-Ended Differential Voltage Gain vs Ambient Temperature

Special Function Circuits
Technical Data

Automotive Circuits

Broadband (Video) Amplifiers

Four Quadrant Multiplier

Prescalers

Single-Chip Detector Alarm Systems

Timer

*BIMOS types

CA3002

10-Lead TO-5

H-1384

IF Amplifier

For Use in Communication Equipment

Features:

- *Input resistance - 100 kΩ typ.*
- *Output resistance - 70 Ω typ.*
- *Voltage gain - 24 dB typ. @ 1.75 MHz*
- *Push-pull input, single-ended output*
- *-3 dB bandwidth - 11 MHz typ.*
- *AGC range - 80 dB typ.*
- *Useful frequency range DC to 15 MHz.*

Applications:

- *Product detector*
- *IF & video amplifier*
- *AM detector*
- *Schmitt trigger*

The RCA-CA3002 integrated-circuit IF amplifier is a balanced differential amplifier that can be used with either a single-ended or a push-pull input and can provide either a direct-coupled or a capacitance-coupled single-ended output. Its applications include RC-coupled IF amplifiers that use the internal silicon output-coupling capacitor, video amplifiers that use an external coupling capacitor, envelope detectors, product detectors, and various trigger circuits.

The CA3002 is supplied in the 10-lead hermetic TO-5 style package.

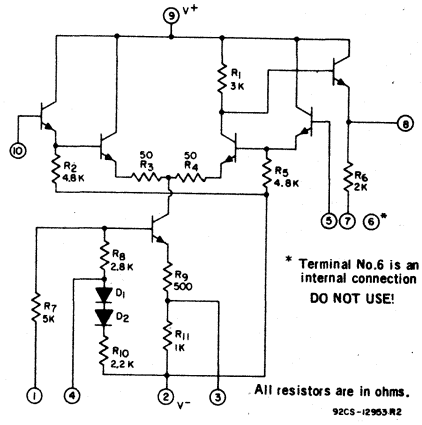


Fig. 1 — Schematic diagram.

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, *at* $T_A = 25°C$

COMMON-MODE INPUT SIGNAL VOLTAGE . . . . . ±2 V
MAXIMUM POWER SUPPLY VOLTAGE . . . . . 16 V or ±8 V
OPERATING-TEMPERATURE RANGE . . . . . −55°C to +125°C
STORAGE-TEMPERATURE RANGE . . . . . −65°C to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265°C
MAXIMUM INPUT-SIGNAL VOLTAGE . . . . . ±4 V
MAXIMUM DEVICE DISSIPATION:
−55 to 85°C . . . . . 450 mW
Above 85°C . . . . . Derate linearly 5 mW/°C

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$, $V_{CC} = +6$ V, $V_{EE} = -6$ V

CHARACTERISTICS	SPECIAL TEST CONDITIONS TERMINALS No. 3 & No.4 NOT CONNECTED UNLESS OTHERWISE NOTED	TEST CIRCUITS	LIMITS CA3002			UNITS
		Fig.	Min.	Typ.	Max.	
STATIC CHARACTERISTICS						
Input Unbalance Voltage V_{IU}		4	–	2.2	–	mV
Input Unbalance Current I_{IU}		5	–	2.2	10	μA
Input Bias Current I_I		5	–	20	36	μA
Quiescent Operating Voltage	MODE: TERMINAL 2 / TERMINAL 4					
	A: V_{EE} / NC	7a	–	2.8	–	V
	B: V_{EE} / V_{EE}	8b	–	3.9	–	V
Device Dissipation P_T		4	–	55	–	mW
DYNAMIC CHARACTERISTICS						
Differential Voltage Gain A_{DIF} (Single-Ended Input and Output)	f = 1.75 MHz	10	19	24	–	dB
Bandwith at −3 dB Point BW	–	10	–	11	–	MHz
Maximum Output Voltage Swing $V_{OUT(P-P)}$	–	10	–	5.5	–	V_{P-P}
Noise Figure NF	f = 1.75 MHz R_S = 1 kΩ	12	–	4	8	dB
Input Impedance Components: Parallel Input Resistance R_{IN}	f = 1.75 MHz	None	–	100k	–	Ω
Parallel Input Capacitance C_{IN}	f = 1.75 MHz	None	–	4	–	pF
Output Resistance R_{OUT}	f = 1.75 MHz	14	–	70	–	Ω
3rd Harmonic Intermodulation Distortion IMD	–	16	−30	−40	–	dB
AGC Range (Maximum Voltage Gain to Complete Cutoff AGC	f = 1.75 MHz	18	60	80	–	dB

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, *at* $T_A = 25°C$

Indicated voltage or current limits for each terminal can be applied under the specified operating conditions for other terminals.

All voltages are with respect to ground ($-V_{CC}$, $+V_{EE}$) or common terminal of Positive and Negative DC supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	−8 V	0 V	2, 7 5, 10 9	−8 0 +6
2	−10 V	0 V	1, 5, 10 9	0 +6
3	−8.5 V	0 V	1, 5, 10 7 9	0 −6 +6
4	−8 V	0 V	1, 5, 10 2, 7 9	0 −8 +6
5	−3.5 V	+3.5 V	1, 10 2, 7 9	0 −6 +6
6	INTERNAL CONNECTION DO NOT USE			
7	−12 V	0 V	1, 5, 10 2 9	0 −6 +6
8	20 mA		1, 5, 10 2 9 200 Ω Resistor Between Terminals 7 & 8	0 −6 +6
9	0 V	+10 V	1, 5, 10 2, 3, 7	0 −6
10	−3.5 V	+3.5 V	1, 5 2, 7 9	0 −6 +6
CASE	INTERNALLY CONNECTED TO TERMINAL No.2 (SUBSTRATE) DO NOT GROUND			

STATIC CHARACTERISTICS

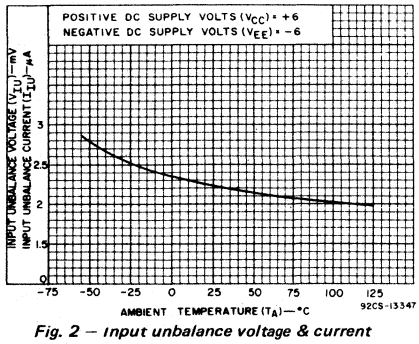


Fig. 2 — Input unbalance voltage & current vs temperature.

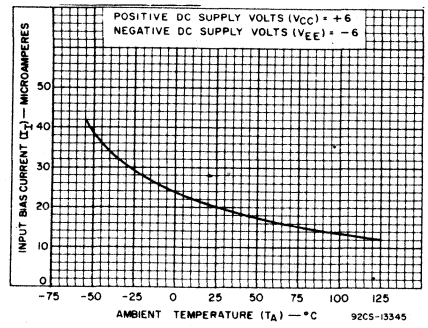


Fig. 3 — Input bias current vs temperature.

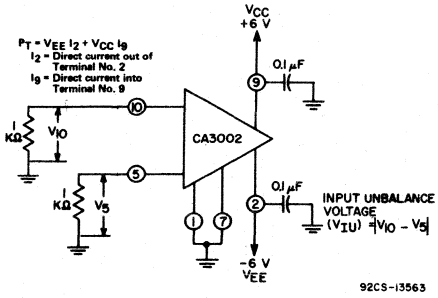


Fig. 4 – Input unbalance voltage and device dissipation test circuit.

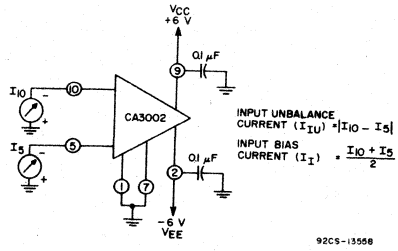


Fig. 5 – Input unbalance current & bias current test circuit.

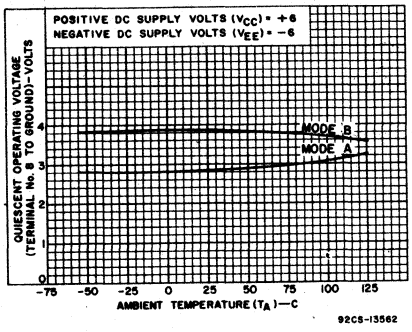


Fig. 6 – Quiescent operating voltage vs temperature.

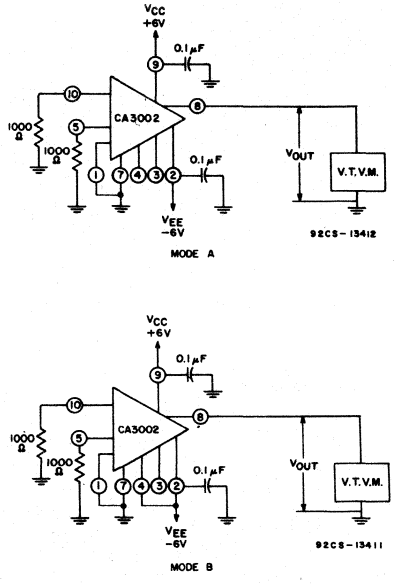


Fig. 7 – Quiescent operating voltage.

DYNAMIC CHARACTERISTICS

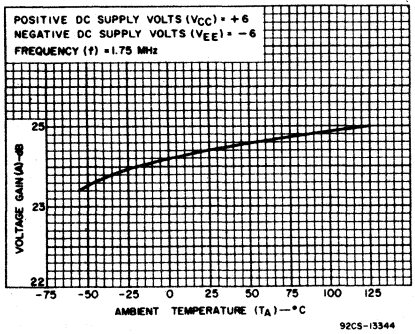


Fig. 8a – Differential voltage gain vs temperature.

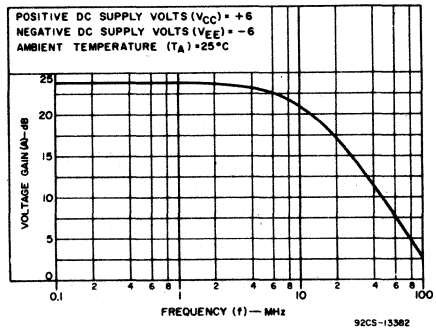


Fig. 8b – Differential voltage gain vs frequency.

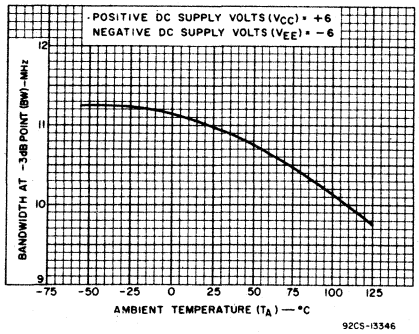


Fig. 9 — Bandwidth of −3 dB point vs temperature.

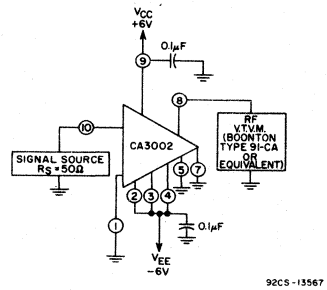


Fig. 10 — Differential voltage gain, −3 dB bandwidth, and maximum output voltage swing.

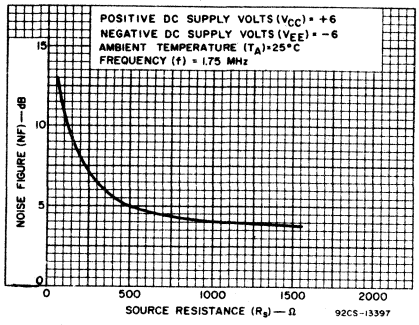
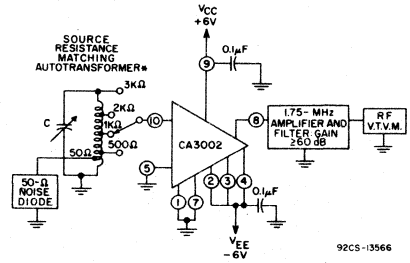


Fig. 11 — Noise figure vs source resistance.



* Taps are adjusted to provide indicated equivalent values of R_S with tank tuned to resonance at 1.75 MHz, and a 50-Ω resistor connected to simulate the noise diode.

Fig. 12 — Noise figure.

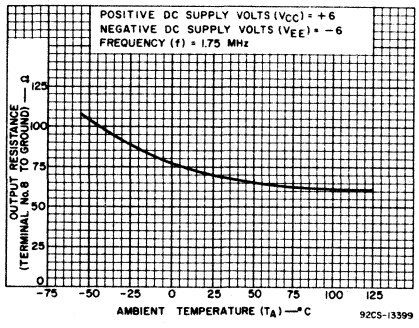


Fig. 13a — Output resistance vs temperature.

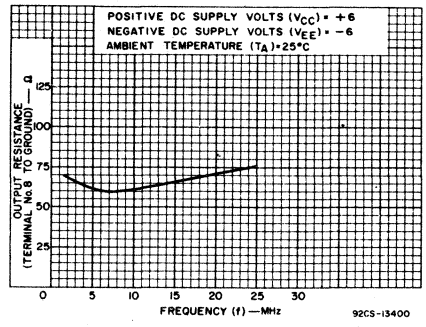


Fig. 13b — Output resistance vs frequency.

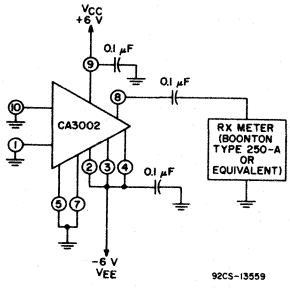


Fig. 14 — Output resistance.

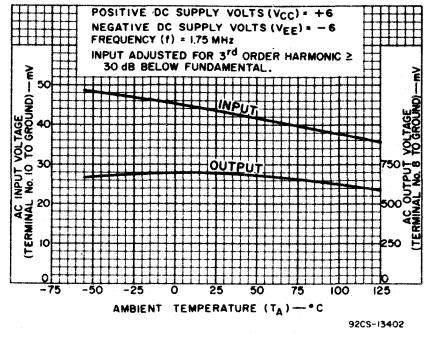
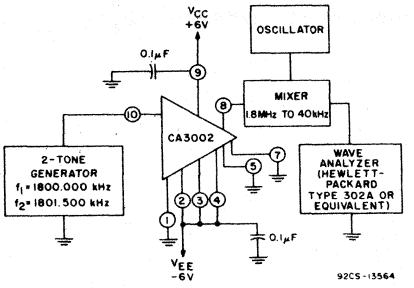


Fig. 15 — Input level for −30 dB intermodulation vs temperature.



1) Increase both input-signal tones until the $2f_2$-f1 and $2f_1$-f2 output-signal voltages are 30 dB below the f_1 and f_2 output-signal voltages.
2) Measure rms values of the input and output signal voltages.
3) The measured input signal voltage is that value when the 3rd-harmonic intermodulation products are 30 dB below the fundamental outputs.

Fig. 16 – Intermodulation circuit.

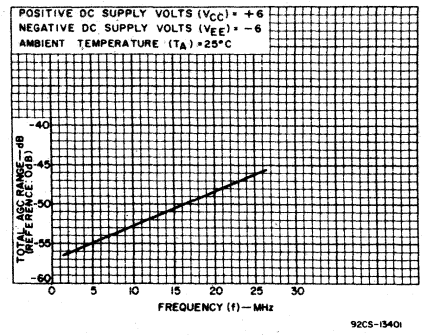
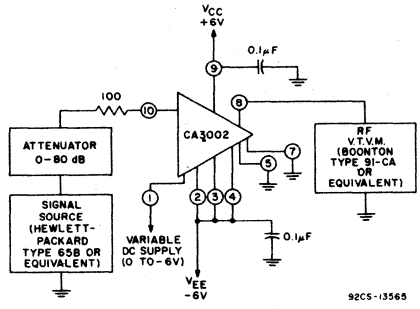


Fig. 17 – AGC range vs frequency.



1) Set attenuator at 80 dB attenuation.
2) Set variable dc supply voltage at 0 V.
3) Increase signal input voltage until RF V.T.V.M. indicates 5 mV output.
4) Set variable dc supply voltage at -6 V.
5) Adjust attenuator until RF V.T.V.M. again indicates 5 mV output.
6) Change in attenuator setting in dB is total AGC Range.

Fig. 18 – AGC range.

CA3091D

14-Lead Dual-In-Line Ceramic Package H-1553

Four-Quadrant Multiplier

Applications:

- **Multiplier** ■ **Divider** ■ **Squarer** ■ **Square Rooter**
- **Power-series approximator**
- **Full-wave rectifier**
- **Automatic level controller**
- **RMS converter**
- **Frequency discriminator**
- **Voltage-controlled filters and oscillators**

RCA-CA3091D*, a monolithic silicon integrated circuit, is a four-quadrant multiplier that provides an output voltage that is the product of two input (x and y) voltages.

This device functions as a multiplier, divider, squarer, square rooter, and power-series approximator. In addition, this device is useful in applications such as ideal full-wave rectifiers, automatic level controllers, RMS converters, frequency discriminators, and voltage-controlled filters and oscillators.

The CA3091D comprises five basic circuits (See Fig. 1), including: a multiplier block, two linearity compensators, a current converter, a current source for biasing, and a regulator (reference voltage). A brief description of the operation, functions and typical applications is given in the section "Operating Considerations". In addition there is a separate section on "Symbols, Terms, and Definitions" that defines the terms and symbols used throughout the data bulletin.

The CA3091D is supplied in 14-lead dual-in-line ceramic package and operates over the full military temperature range of -55°C to +125°C.

* Formerly Developmental Type TA5855A.

Features: ●

- **"Accuracy": ±4% (max.)**
- **"Linearity": 3.0% (max.)**
- **Feedthrough: 9 mV p-p (typ.)**
- **3-db bandwidth: 4.4 MHz**
- **Low power operation capability: ±6.0 V, 4 mW drain**
- **Low power-supply sensitivity: 36 mV/V typ.**
- **Smooth overload characteristics — no foldback if full-scale input signal is exceeded**
- **Negligible warm-up drift**
- **Broadband operation capability (flat to 1 MHz) — both inputs have similar characteristics for reduced high-frequency phase shift between the inputs**
- **Low-level linearity correction circuitry minimizes low-level feedthrough for improved small-signal accuracy**
- **All multiplication is performed with wideband circuitry — this permits two signals of frequencies much higher than the -3 db frequency of the multiplier to produce a difference frequency that is within the multiplier's bandwidth**
- **High immunity to parasitic oscillation**
- **Essentially free from excess peaking — provides improved frequency response**
- **Requires no level shifting at the output — current-source operation at the output permits output signal to be referenced to ground or other levels within the output voltage swing capabilities of the multiplier**
- **Internal bias regulator**

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DC Supply Voltages:		
Between Terms. 12 and 1	+18	V
Between Terms. 4 and 1	−18	V
DC Supply Currents:		
At Term. 12 with DC Supply Voltage = +15 V	4	mA
At Term. 4 with DC Supply Voltage = −15 V	16	mA
Bias Current (At Term. 3)	1	mA
* Input Current	±1	mA
Output Short-Circuit Duration	No limitation	
Voltage Reference Current	10	mA
Linearity Correction Currents:		
At Terminals 7 and 8	10	mA
Device Dissipation (Up to 125°C)	200	mW
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (during soldering):		
At distance not less than 1/32 inch (0.79 mm) from case for 10 seconds max.	+265	°C

* External resistance is required to limit the current to the indicated ±1 mA value.

ELECTRICAL CHARACTERISTICS, For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: T_A = 25°C, I_{IB} = 0.5 mA, V^+ = 15 V, V^- = -15 V	Circuit and/or Char. Curve	LIMITS: Min.	Typ.	Max.	UNITS
STATIC CHARACTERISTICS							
INPUT CIRCUIT							
Input Balance (Correction) Currents:							
At x Input	I_{IC}	x = 0	–	−20	−2.1	+20	μA
At y Input		y = 0	–	−20	−8.7	+20	μA
Feedthrough Linearity Balance (Correction) Current	I_{OC}		–	−34	−2.9	+34	μA
OUTPUT CIRCUIT							
Output Offset Current	I_{OO}	x & y = O,	–	−10	−0.23	+10	μA
Output Offset Voltage	V_{OO}	I_{OO} thru R_L = 33kΩ	–	−0.330	−0.0076	+0.330	V
Output Peak Current Swing	$\|I_O\|$	Thru R_L = 24kΩ	3	0.41	0.45	–	mA
Output Peak Voltage Swing	$\|V_O\|$	Across R_L = 33kΩ	4	12	12.9	–	V
DC SUPPLIES & BIASING							
Current Drain (Idling):							
At Term. 4		V^- = -15 V	–	–	2.9	4.5	mA
At Term. 12		V^+ = +15 V	–	–	2.0	3.0	mA
Reference Voltage	V_{ref}	Measured across Terms. 6 & 4 at I = 1mA	–	5.5	6.1	6.7	V
DYNAMIC CHARACTERISTICS							
Output Current	I_O	With I = 0.2mA at each input	–	–	0.21	0.32	mA
Normalized k Factor $\left(k_N = \frac{k}{k_r}\right)$			11	0.69	1.0	1.7	
Accuracy		Worst case at 25°C	–	–	2.6	4.0	% of 10 V
Linearity				–	1.7	3.0	
Feedthrough Voltage:							
At y = 20V p-p, x = O			–	–	9	20	mV p-p
At x = 20V p-p, y = O			–	–	9	20	

NOTE: See page 7 for "Symbols, Terms and Definitions".

ELECTRICAL CHARACTERISTICS, Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: T_A = 25°C, I_{IB} = 0.5 mA, V^+ = 15 V, V^- = −15 V	Circuit and/or Char. Curve	TYPICAL VALUES	UNITS
STATIC CHARACTERISTICS					
INPUT CIRCUIT					
Input Resistance:					
At x Input	R_I	$\lvert I_x \rvert \leq 0.2$ mA	5	1.3	kΩ
At y Input		$\lvert I_y \rvert \leq 0.2$ mA		0.5	kΩ
Input Capacitance:					
At x Input	C_I	at 1 MHz	–	5.8	pF
At y Input				5.8	pF
OUTPUT CIRCUIT					
Output Resistance	R_O		6	1.0	MΩ
Output Capacitance:	C_O	at 1 MHz		4.0	pF
DC Supply Voltage Sensitivity:					
At Term. 4	$\frac{\Delta V_O}{\Delta V^-}$		11	26	mV/V
At Term. 12	$\frac{\Delta V_O}{\Delta V^+}$			36	mV/V
DYNAMIC CHARACTERISTICS					
Bandwidth (At -3dB point):					
Through x Input	BW		8, 10	4.8	MHz
Through y Input			8, 9	4.4	MHz
3° Error Frequency:					
Through x Input			–	360	kHz
Through y Input				310	kHz
Maximum Slew Rate	SR	7pF in parallel with 10 MΩ load	7	27	V/μs
Temperature Coefficients:					
Output Offset Current	$\Delta I_{OO}/\Delta T$	x & y = 0	–	−0.021	μA/°C
x-Input Balance Current	$\Delta I_{IC}/\Delta T$	x = 0	–	−0.063	μA/°C
y-Input Balance Current		y = 0	–	−0.063	μA/°C
Normalized k Factor $\left(k_N = \frac{k}{k_r}\right)$	k_N		–	−0.76	%/%/°C
Accuracy			–	0.11	%/°C
Linearity			–	0.06	%/°C
Feedthrough:					
At x = 0			–	5.6	mV/°C
At y = 0				5.7	mV/°C

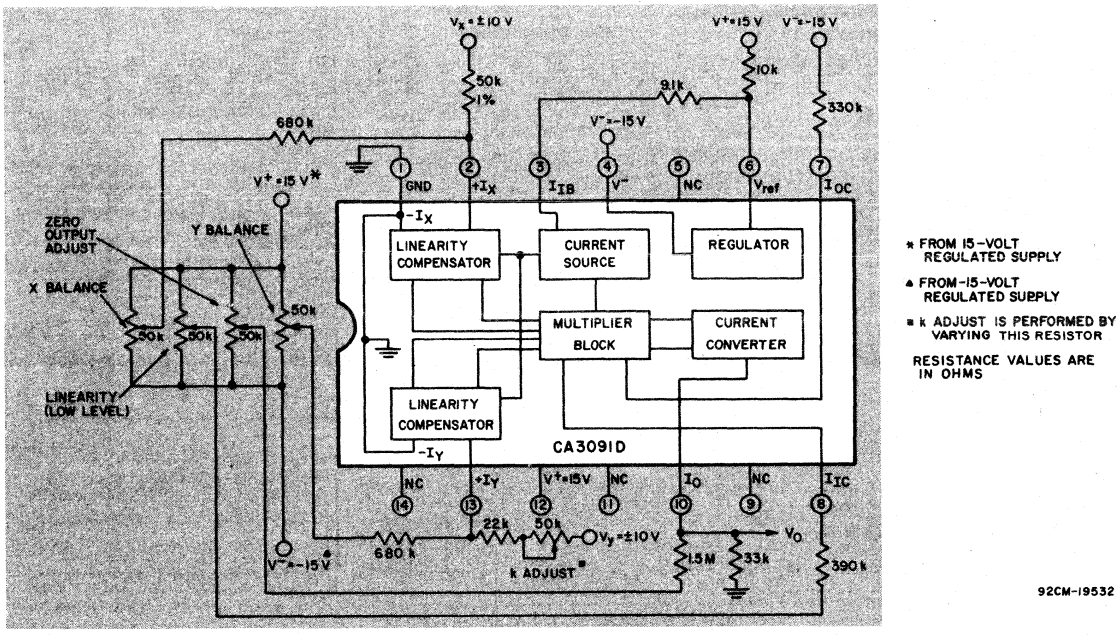


Fig.1—Functional block diagram of CA3091D with typical multiplier outboard (peripheral) circuitry.

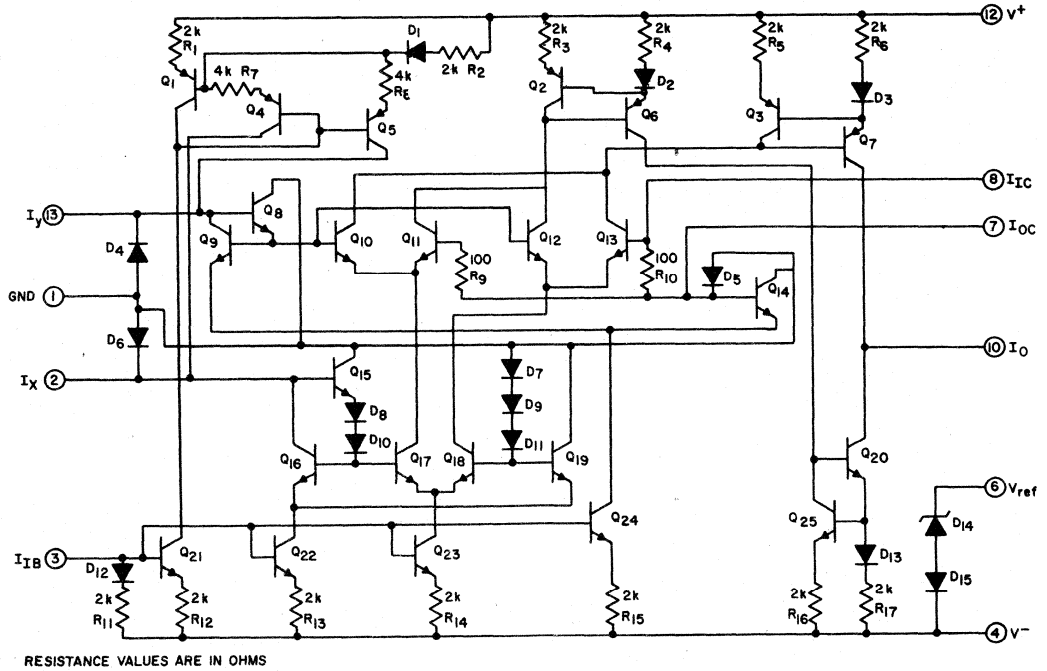


Fig.2—Schematic diagram of the CA3091D.

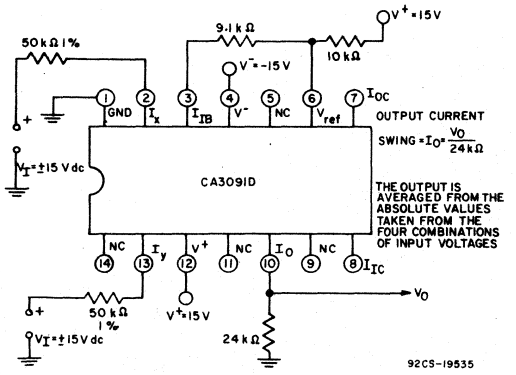


Fig.3—Test circuit for measurement of output current swing capability.

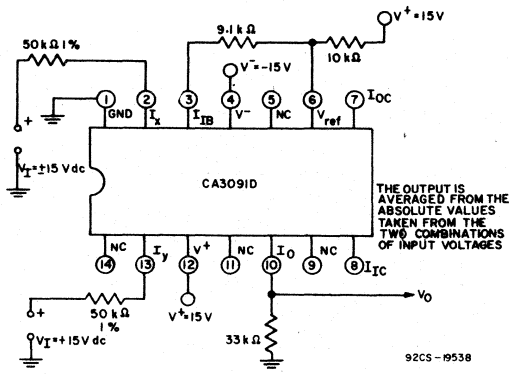


Fig.4—Test circuit for measurement of output voltage swing capability.

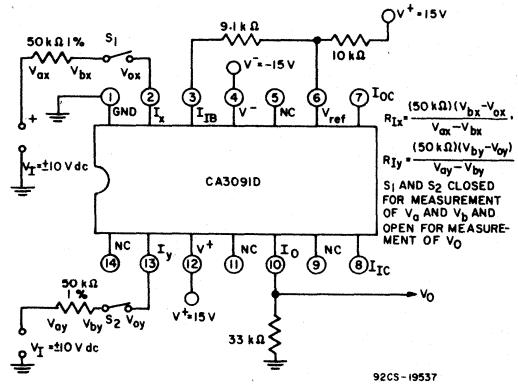


Fig.5—Test circuit for measurement of input resistance.

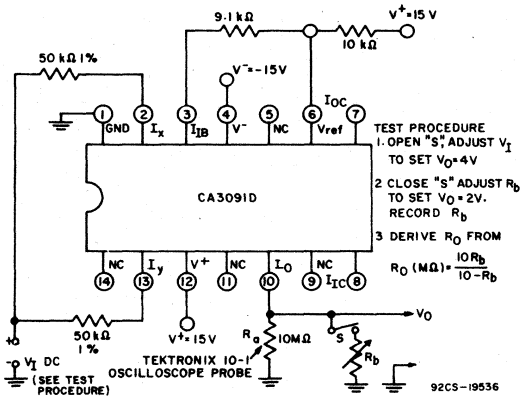


Fig.6—Test circuit for measurement of output resistance.

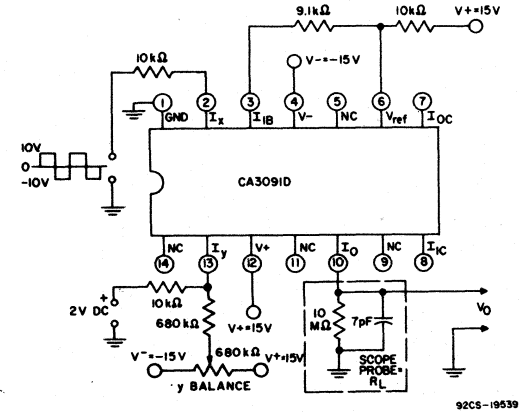


Fig.7—Test circuit for measurement of maximum slew rate.

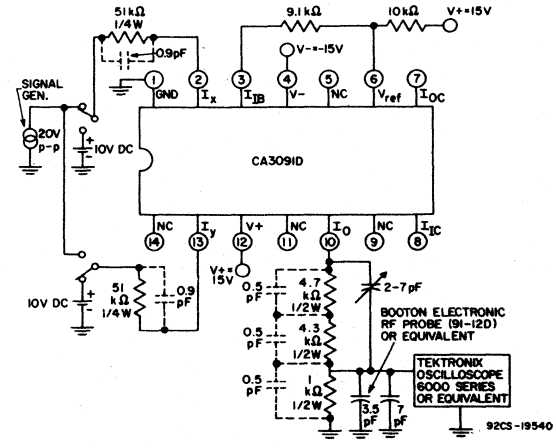


Fig.8—Test circuit for measurement of frequency response.

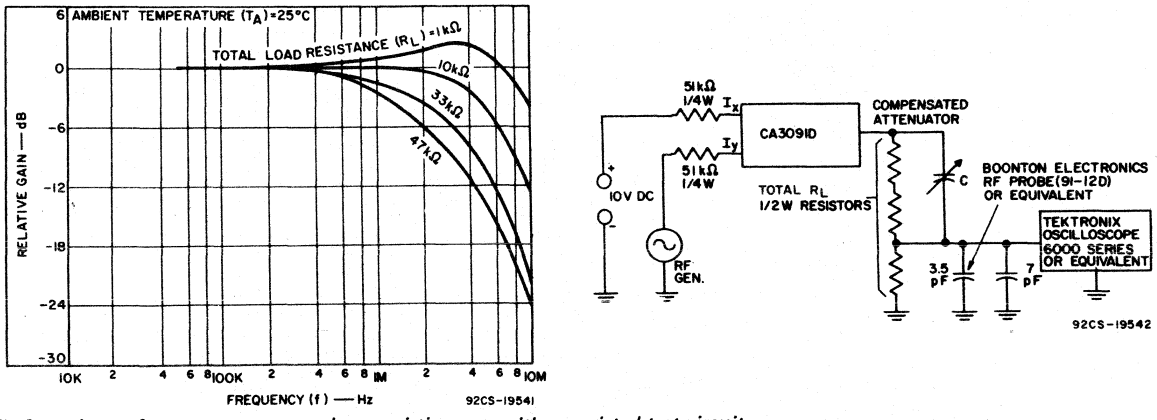


Fig.9- y—input frequency response characteristic curve with associated test circuit.

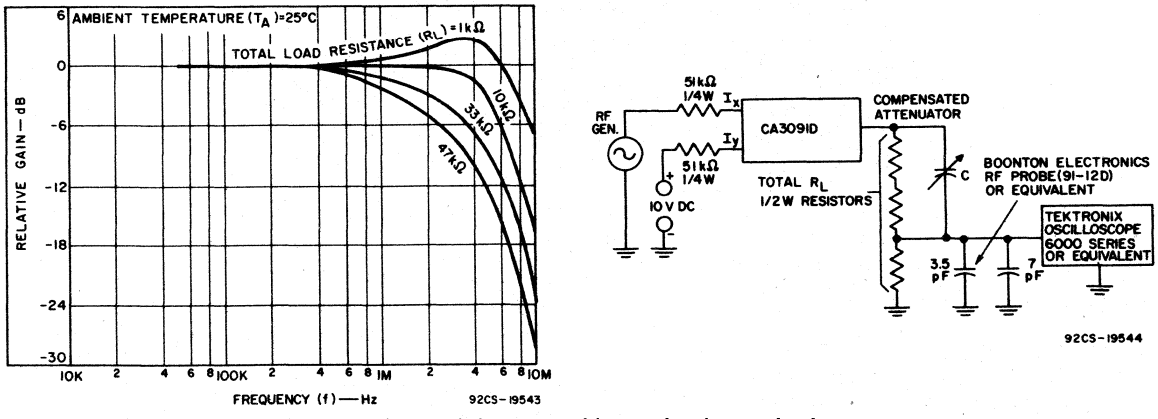


Fig.10- x—input frequency response characteristic curve with associated test circuit.

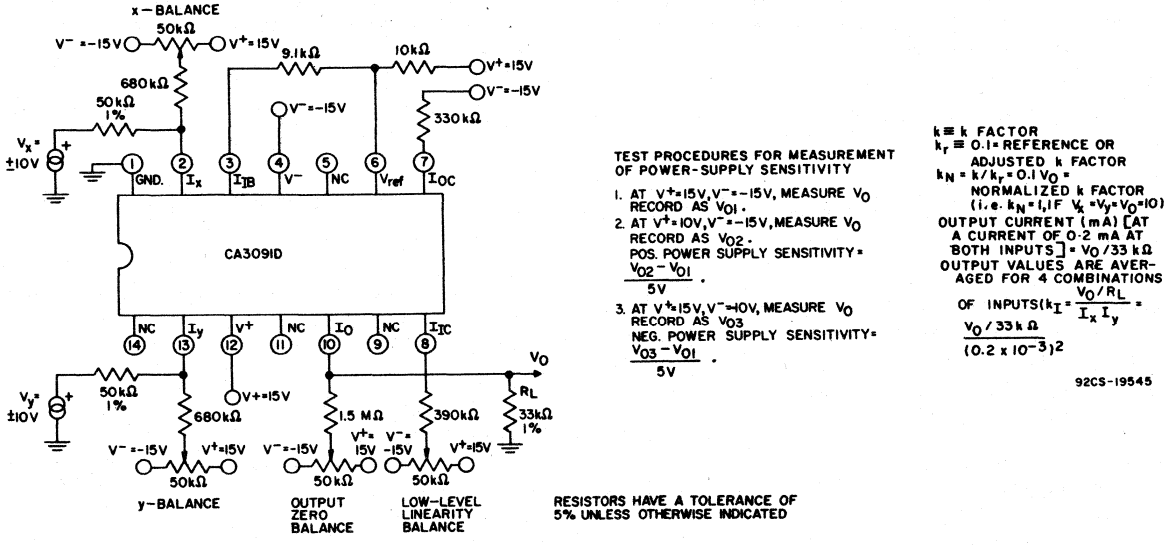
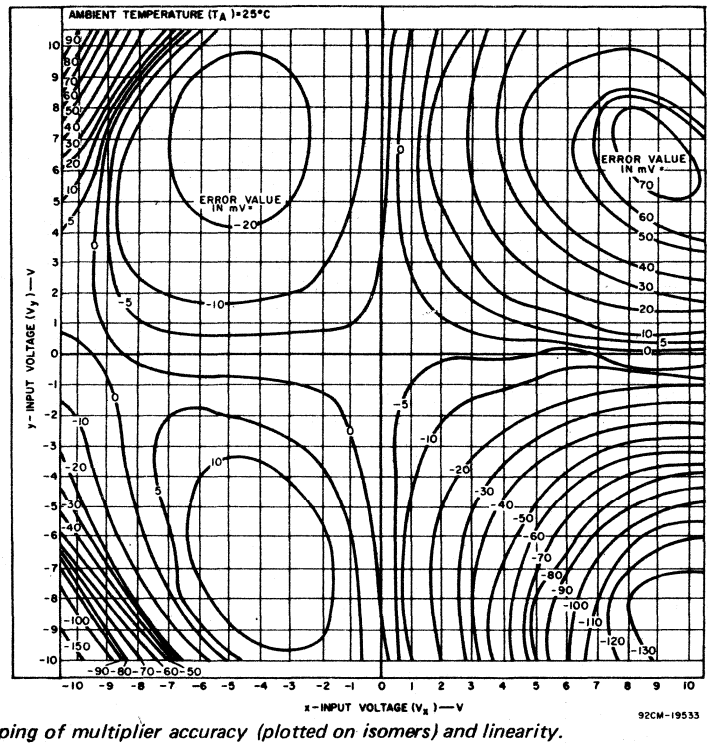


Fig.11—Test circuit for measurement of current gain and power-supply sensitivity.



Note: See "Contour Map" in "Symbols, Terms and Definitions" Section.

Fig.12—Contour mapping of multiplier accuracy (plotted on isomers) and linearity.

SYMBOLS, TERMS AND DEFINITIONS

Output Offset Current
The multiplier output current produced when both of the multiplier input signals are in the zero state.

Output Zero
Sets the output at the zero level when the x and y inputs are in the zero state. (It is implied that all other zeroing adjustments have been effected.)

R_I
Input Resistance — Converts the input voltage to an input current.

R_L
Output (Load) Resistance — Converts the output current to a voltage.

R_O
Output Resistance — See V_O and I_O for the equations associated with these properties.

Regulator Diode
A temperature compensated Zener diode, included in the multiplier circuit, to provide a stable I_{IB}.

Scale Factor or k factor (k)
Represents the basic gain of the multiplier as expressed in the equation $V_O = kV_XV_Y$

The equation indicates the ideal transfer function for the multiplier. The normalized k factor is expressed by $k_N = k/k_{ref}$ where k_{ref} is the ideal or reference k factor. The ideal factor, k_{ref} is the value at which the k factor is set when the k-factor adjust control is trimmed. Optimum operation of the CA3091D is achieved when the k-factor is 0.1.

V_{IM}
The maximum ac sine-wave voltage to be applied to the multiplier; a 20-volt p-p sine wave is the nominal maximum swing voltage recommended for use with 50-kilohm input resistors.

V_{MID}
An ac or dc voltage that approximately satisfies the equation

$$V_{MID} = V_{IM}/\sqrt{2.}$$

V_O
The output product voltage derived from the expression

$$(kV_XV_Y = V_O)$$

$V_{ref.}$
Temperature compensated zener connected to the −15 volt supply to provide a reference voltage as an aid in setting up a stable I_{IB}.

V_X, V_Y
The input voltages to be multiplied.

x-Balance Circuit
Sets the output to the zero level when the x-input is in the zero state.

y-Balance Circuit
Sets the output to the zero level when the y-input is in the zero state.

SYMBOLS, TERMS AND DEFINITIONS — continued

Accuracy
Accuracy defines the degree of error encountered in the operation of the multiplier. It is portrayed on a contour map by isomers (contour lines). Isomers with the highest values indicate "less-accurate" operation of the multiplier. (See illustrative Contour Map in Fig. 12.)

Contour Map
The contour map, shown in Fig. 12, is a graphical portrayal of the multiplier errors in the x, y input plane. Each contour line, termed "isomer", connects those points whose error values (in millivolts) are equal in magnitude. For example, a −20 mV contour line with points at $V_X = 5V$ and $V_Y = -3V$ indicates that the output voltage is 20 mV less than the theoretical output product (kV_XV_Y). This error voltage, presented in percent of full-scale input (±10 V), defines the "accuracy" of the device. Thus, a 20-mV error voltage represents an "accuracy" of 0.2% as derived from the equation:

$$\text{Accuracy} = 20\,\text{mV}/10 \times 100\% = 0.2\%.$$

A contour map provides a true indication of multiplier performance in each of the four quadrants. Each CA3091D is comprehensively tested and must provide the specified accuracy in the four quadrants.

Current Converter
This portion of the IC combines the multiplier's differential-amplifier output currents and converts them to a single-ended output current.

Current Sources
These circuits provide the biasing currents for the various circuits in the IC. The I_{IB} terminal provides the control current for the current-source circuit.

Feedthrough
Feedthrough occurs when an output signal is produced even though one of the input signals is zero. Consequently, feedthrough signal characteristics constitute a source of error in the operation of a multiplier. In the CA3091D, for example, the feedthrough signal output is specified to be less than 20 mV p-p when either terminal is set at 20 V p-p and the other terminal is set to zero.

I_{IB}
Circuit biasing control current.

I_{IC}
See I_{OC}.

I_O
Output product current ($k_I I_X I_Y = I_O$), where $k_I = kR_I^2 / R_L$

I_{OC}, I_{IC}
Compensatory input and output currents required to correct unlinearity along the x axis. (Optional for low-level signal use.)

I_X, I_Y
Input currents to be multiplied.

k
Voltage Scale Factor (determines the gain of the multiplier).

k_I
Current Scale Factor (k_I) = $(R_I^2 / R_L)k$.

k adjust
Scale-Factor Adjustment.

Linearity
"Linearity" indicates the degree of multiplier error (i.e. deviation from "straight-line" characteristics) along each of the four boundaries of the input x, y field. These boundaries are formed when one input is held at one of the two maximum values (10 volts or −10 volts) and the other input is swept through the voltage range. (See Contour Map for additional information.)

Linearity Adjust
An external circuit to provide vernier adjustment for optimum linearity. This control should be adjusted before adjusting the y-balance control.

Linearity Balance Circuit (Low-Level)
This circuit makes the multiplier's transfer function linear for low-level x-input signals.

Linearity Compensator
Internal circuitry that converts input current into a non-linear voltage, a requisite for producing a linear output in the differential amplifiers of the multiplier circuit.

Multiplier Circuitry
Provides the product of the two input voltages.

Multiplier Transfer Function
This function mathematically describes the interaction of the two inputs and the resulting output signal. The basic transfer function for a multiplier is

$$k(V_X + V_{Xe})(V_Y + V_{Ye}) = V_O + V_{Oe}$$

where: k = k factor and represents the basic gain of the multiplier

V_X, V_Y = the external inputs to be multiplied

V_O = the desired value of the product output signal

V_{Xe}, V_{Ye} = the "effective" errors that occur at the inputs of the multiplier and cause an output signal when either input is in a zero state.

V_{Oe} = the error voltage that develops at the output of the multiplier

DC correction factors are added to the multiplier inputs and output to compensate for the errors and offset variations. A complex linearity error term appears in the transfer function; however, this term is not included in the above equation for the purpose of clarity.

OPERATING CONSIDERATIONS

Operation of a Multiplier

A multiplier is, essentially, a gain-controlled amplifier (See Fig. 13) that multiplies the input signal (V_X) with the external gain controlling signal (V_Y) to produce the resultant output (V_O). The gain is externally adjustable by a coefficient (k). Stated simply, a multiplier produces an output voltage that is the linear product of two input voltages.

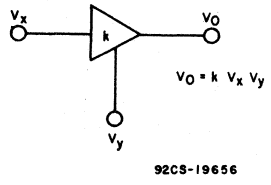
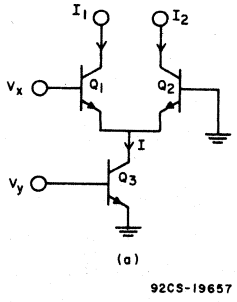
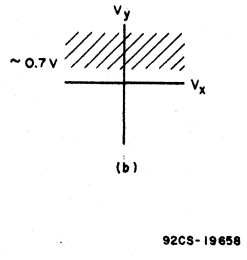


Fig.13—Gain-controlled amplifier.

The basic multiplier, shown in Fig. 14a, is a two-quadrant multiplier. The input signal (V_X) may have either a positive or negative polarity whereas, the external gain-controlling signal (V_Y) must be positive and greater than the base-to-emitter voltage (Fig. 14b). The output current ($I_1 - I_2$) of the differential amplifier, comprised of transistors Q1 and Q2, is related to both the input signal (V_X) and the current source (I). Since the current source (I) is related to the gain controlling signal (V_Y) the output current ($I_1 - I_2$), therefore, is related to both V_X and V_Y.





a) Basic circuit.

b) Multiplier functional only in shaded region.

Fig.14—Two-quadrant multiplier.

This relationship is essentially non-linear; thus an appropriate linearization circuit must be provided in the input stage to achieve the following linear relationship:

$$I_1 - I_2 = k' V_X V_Y \qquad \text{(Eq. 1)}$$

where k' is a constant

Figure 15 shows a typical arrangement of three differential amplifiers to form a four-quadrant multiplier. This arrangement incorporates the operating principles of the two-quadrant multiplier, but, in addition, it permits both of the input signals (V_X and V_Y) to have positive or negative polarities (or zero). When either input is zero, the output current ($I_1 - I_2$) must, theoretically, be zero as is shown by the following:

1. Assume $V_X = 0$,
   then $i_1 = i_2$ and $i_3 = i_4$
   therefore $i_1 + i_4 = i_2 + i_3$.
   Since $I_1 = i_1 + i_4$ and $I_2 = i_2 + i_3$,
   then $I_1 = I_2$.
   This equality is independent of V_Y
2. Now assume $V_Y = 0$,
   then $i_5 = i_6$.
   Sine $i_5 = i_1 + i_2$ and $i_6 = i_3 + i_4$,
   then $i_1 + i_2 = i_3 + i_4$.
   Since $i_1 = i_3$ and $i_2 = i_4$
   then $i_1 + i_4 = i_3 + i_2$.
   Therefore $I_1 = I_2$.
   This equality is independent of V_X.

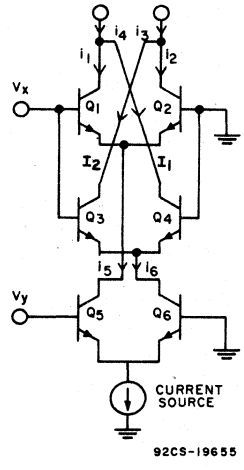


Fig.15—Basic four-quadrant multiplier.

The multiplying operation discussed in the previous section applies when neither V_X nor V_Y is zero. The output current ($I_1 - I_2$) then satisfies Equation 1,

$$I_1 - I_2 = k' V_X V_Y.$$

The multiplying action of the four-quadrant multiplier is dependent on current unbalance in the three differential amplifiers. Ideally, the multiplying operation should not occur if either V_X or V_Y is O. However, in practical applications slight current unbalances do exist. It is necessary, therefore, to null out such unbalances with external potentiometers prior to operation.

TYPICAL OPERATING CONSIDERATIONS

The RCA-CA3091D, shown in Fig. 2, is a four-quadrant multiplier that incorporates the basic multiplier principle, previously discussed in "Operation of a Multiplier". Because the design of this multiplier is based on the multiplication of two input currents to produce an output current it is necessary to convert the input voltages to input currents and the output current to an output voltage by inserting resistors at both input and output terminals. Fig. 1 shows the four-quadrant multiplier with its peripheral circuitry for nulling current unbalances.

The Bias Current (I_{IB}) at Term. 3 sets the operating current level for the entire multiplier circuit by means of a current-source circuit. Therefore, it is essential that this bias current level remain constant under all operating conditions. To maintain this steady state, a temperature compensated zener diode is provided on the chip and connected to the Reference Voltage (Term.6).

Linearity of the differential amplifier transconductance function is accomplished by linearity compensators as shown in Fig. 1. To correct low-level signal unbalances that may occur between Differential Amplifiers A and B, an external potentiometer is connected to Terminals 7 and 8 (See Fig. 1). The Current Converter circuit, which consists of a set of current mirrors, supplies the output current ($I_1 - I_2$). It is important that circuit unbalances be corrected prior to operation. Table I describes the alignment procedures for correcting these unbalances.

A multifunctional circuit board (Figs. 16 and 17) is available for performing the four basic applications, such as, multiplying, dividing, squaring and taking the square root.

When the CA3091D is used as a multiplier (Fig. 18) or as a squarer (Fig. 18) only the basic pheripheral circuitry on the multifunctional circuit board is utilized and the general-purpose operational amplifier (CA3741T) is disabled from operation. Follow the ac alignment procedures for these two applications before operating the circuit.

When the CA3091D is used as a divider (Fig. 20), the operational amplifier is required in order to provide the proper negative feedback. The limitations for operation as a divider are that $O < V_Y \leqslant 10V$ and $-10V \leqslant V_Z \leqslant 10V$. Note, the range of V_Y is limited to the positive polarity; if V_Y was permitted to go negative, the feedback loop would go positive and, thereby, create an unstable operating condition.

Alignment of the divider (Fig. 19) differs from multiplier and squarer alignment because of the additional variances introduced by the operational amplifier. A coupling capacitor is

Table I

AC Alignment Procedures For CA3091D, Four-Quadrant Multiplier

(Refer to Fig. 16, for circuit pertaining to following alignment procedures.)

Step No.	Voltage Setting		Control Adjust	Test Equipment Used	Measure	Notes
	V_X	V_Y				
1	–	–	–	–	–	Set all potentiometers to center of range.
2	O	V_{IM}	x Balance	AC VM	V_O	Adjust for a minimum reading.
3	O	V_{IM}	Linearity	AC VM	V_O	Adjust for a minimum reading.
4	–	–	–	–	–	Repeat Steps 1 and 2 until no further improvement is noted.
5	V_{IM}	O	y Balance	AC VM	V_O	Adjust for a minimum reading.
6	O	O	Zero Output	DC VM	V_O	Adjust for zero output.
7	V_{MID}	V_{MID}	R_k	AC/DC VM	V_O	Adjust for $V^2_{MID}/10$ at the output.
8	–	–	–	–	–	Check multiplier for alignment in all four quadrants.

V_{IM} – Is the maximum AC swing of the sine wave that will be applied to the multiplier. A 20-volt p-p value is the nominal maximum swing of the AC sine wave with input resistors of 50 kilohms.

V_{MID} – An AC or DC voltage that approximately satisfies the equation $V_{MID} = V_{IM}/\sqrt{2}$. For example, if a 50-kilohm resistor is used with a 7-volt input, then R_k should be adjusted for a 4.9-volt output.

provided at the output of the divider alignment circuit in order to separate the ac signal from the dc signal and, thus, avoid interaction between the calibrating potentiometers.

The alignment procedure for the square-rooter function (Fig. 21) is identical to the alignment procedure for the divider function. The input voltage range is limited to $0 < V_I \leqslant 10V$. This limitation is necessary in order to prevent the output voltage (V_O) from latching to the negative output saturation voltage of the operational amplifier. Table II describes the divider alignment procedure.

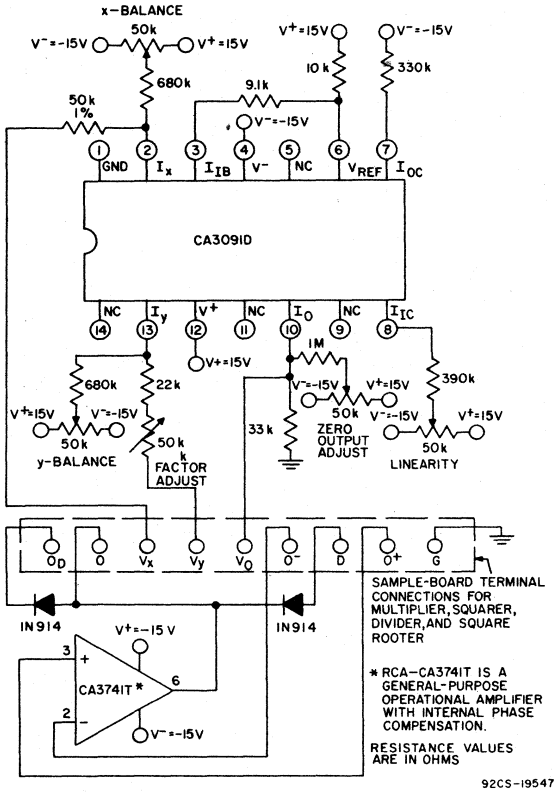
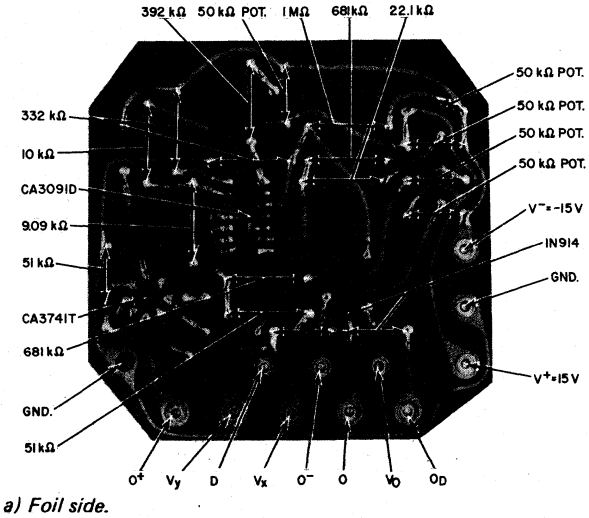
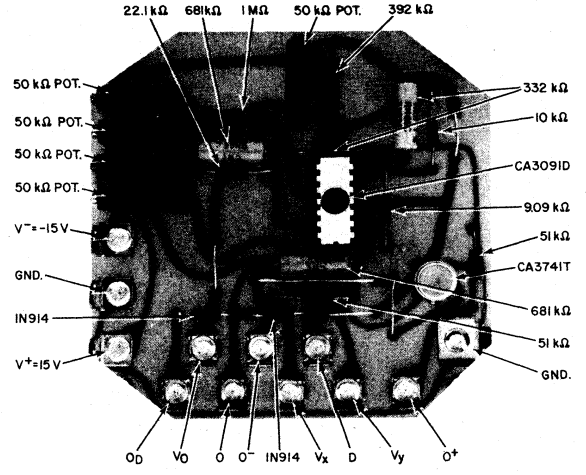


Fig.16—Typical multifunction circuit arrangement utilizing the CA3091D and CA3741T.



a) Foil side.

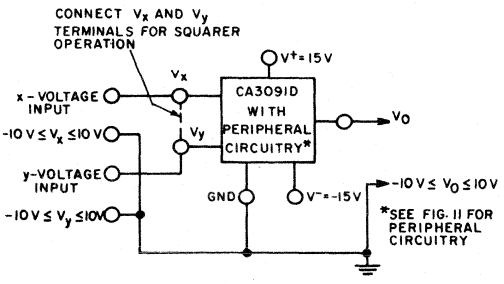


b) Component side.

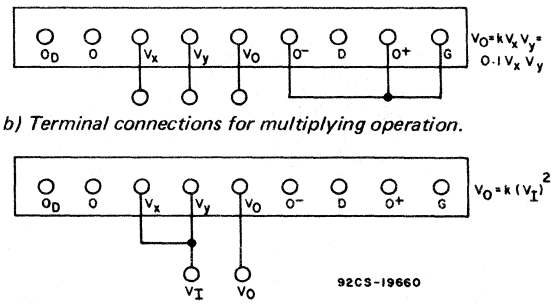
Fig.17—Photographs of a printed-circuit board for multifunction applications (multiplier, squarer, divider, square rooter) utilizing the CA3091D and CA3741T.

Table II — Divider Alignment Procedure

Step No.	Set V_z V	Set V_y V	Measure	Output Coupling	Test Equipment Used	Adjust	Notes
1	—	—	—	—	—	—	Set all potentiometers to center of range.
2	0	V_S	V_O	ac	ac — VM	O_{zero}	Adjust for minimum reading.
3	0	10V dc	V_O	dc	dc — VM	$x_{balance}$	Adjust for OV dc output.
4	V_S	V_S	V_O	ac	ac — VM	$y_{balance}$	Adjust for minimum reading.
5	5V dc	5V dc	V_O	dc	dc — VM	k_{adjust}	Adjust for 10V dc output.



a) Circuit arrangement for multiplier or squarer operation.



b) Terminal connections for multiplying operation.

c) Terminal connections for squarer operation.

Fig.18—Multifunction circuit-board arrangement with terminal connections for multiplier and squarer operation.

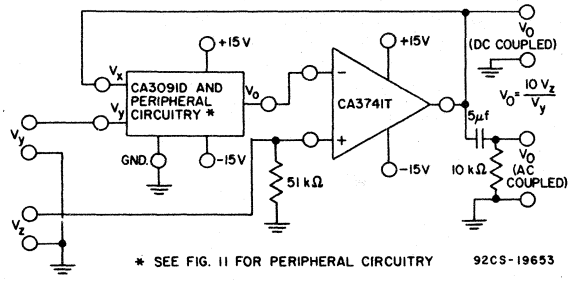


Fig.19—(a) Divider alignment circuit.

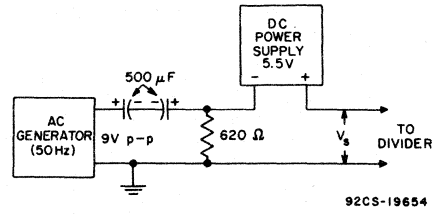
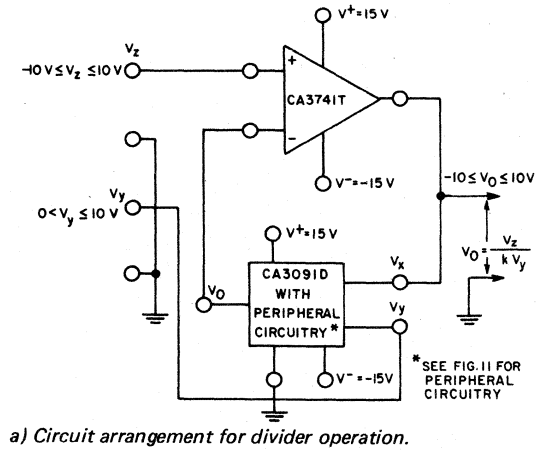
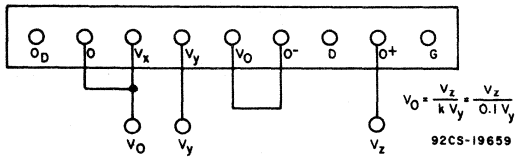


Fig.19—(b) Circuit to provide offset ac signal for use in divider alignment procedure.

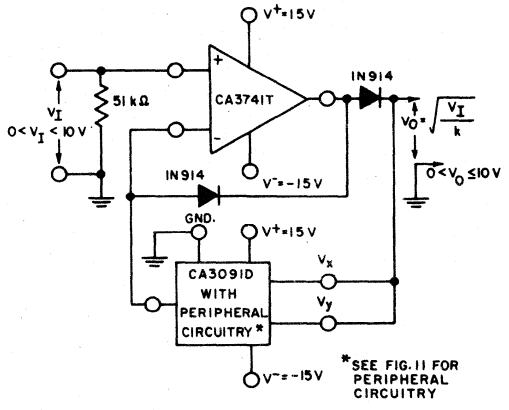


a) Circuit arrangement for divider operation.

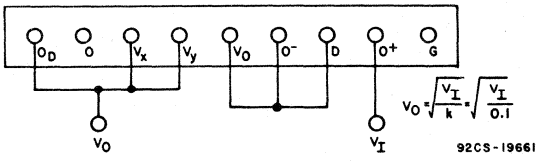


b) Terminal connections for divider operation.

Fig.20—Multifunction circuit-board arrangement with terminal connections for divider operation.



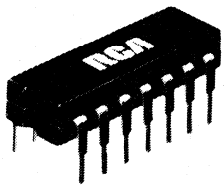
a) Circuit arrangement for square-rooter operation.



b) Terminal connections for square-rooter operation.

Fig.21—Multifunction circuit-board arrangement with terminal connections for square-rooter operation.

CA3179E



14-Lead Dual-In-Line
Plastic Package
"E"-Suffix Type H-1517

1.25 GHz Prescaler

For Industrial Applications

FEATURES:
- *Broadband operation - DC to 1.25 GHz*
- *High sensitivity*
- *Standard T^2L or ECL power supply*
- *Dual mode operation - VHF/UHF (÷ 64/ ÷ 256)*
- *Complementary ECL outputs*
- *Independent VHF and UHF input terminals*

The RCA-CA3179E is an integrated-circuit prescaler intended for use in communications and instrumentation systems. It performs division by 256 in the uhf mode and division by 64 in the vhf mode.

The mode of operation is selected by means of the bandswitch and the separate uhf and vhf input terminals provided. Either single- or double-ended inputs can be applied. These inputs are normally ac coupled, but dc coupling can be used if the specified bias levels are maintained. The output is a complementary emitter-coupled stage capable of driving a 33-pF or equivalent load. The harmonic output is reduced above 40 MHz by limiting output-signal rise and fall times and by maintaining a balanced load.

In the uhf mode, which is activated by applying a high level (logical 1) to the bandswitch input terminal, all eight divider stages are operative, resulting in division by 256. In the vhf mode, activated by a low level (logical 0) at the vhf input terminal, two divider stages are bypassed, resulting in division by 64. An internal amplifier/multiplexer provides this control while isolating both inputs, amplifying the input signal, and improving sensitivity.

The CA3179E is supplied in the 14-lead dual-in-line plastic package.

Applications:
- *Digital frequency synthesizers for:*
  - *VHF/UHF receivers*
  - *Satellite communications*
  - *Instrumentation*
- *High-frequency divider for:*
  - *UHF frequency counters*
  - *UHF timers*
  - *High-speed computers*
  - *Frequency standards*
  - *SHF second IF local-oscillator injection*
  - *PCM communications*
  - *Satellite communications*
  - *Radar ranging systems*
- *High-frequency up-converters*

Table of Absolute-Maximum Ratings

Term. No.	Min. Volts	Max. Volts	Max. I_{IN} (mA)	Max. I_{OUT} (mA)
1 & 2*	0	5.5	110	0
3	−0.3	20	1	1
4 & 5	—	—	0.1	10
9, 10, 13, 14▲	—	4	0.1	1

*Terms. 1 & 2 tied together.
▲Maximum rf drive = 500 mVRMS.
Terms. 7 & 8 are system ground and tied together.
Terms. 6, 11, 12 = no connection.

CA3179E

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE ..... 5.5 V
DC BANDSWITCH VOLTAGE ..... 20 V
RMS INPUT VOLTAGE ..... 0.5 V
DEVICE DISSIPATION:
  UP TO T_A = 70 °C ..... 700 mW
  ABOVE T_A = 70 °C ..... derate linearly at 11.1 mW/ °C
AMBIENT TEMPERATURE RANGE:
  OPERATING ..... 0 to 85 °C
  STORAGE ..... −55 to +150 °C
LEAD TEMPERATURE (DURING SOLDERING):
  AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)
  FROM CASE FOR 10 SECONDS MAX. ..... +265 °C

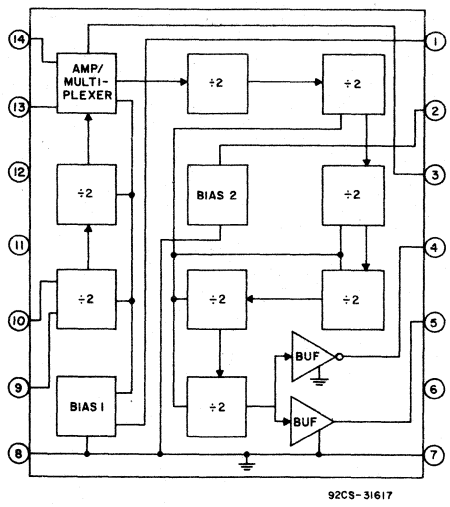


Fig. 1 - CA3179G block diagram.

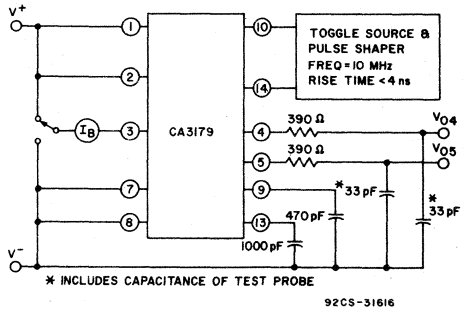


Fig. 2 - DC characteristics test circuit.

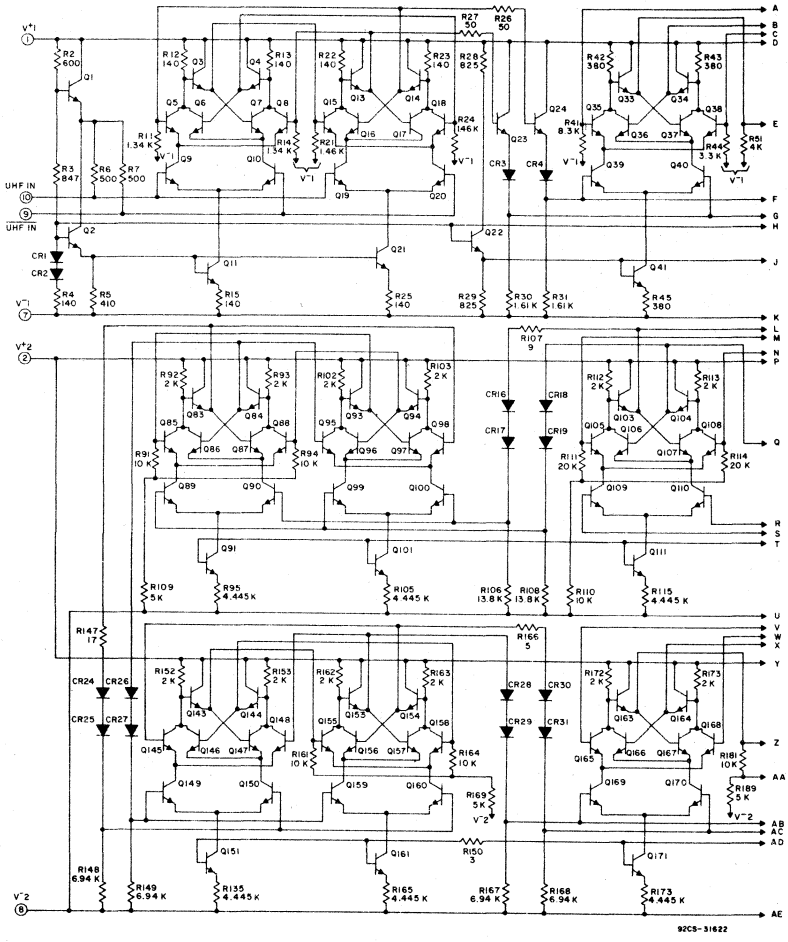


Fig. 3 - Schematic diagram (cont'd on next page).

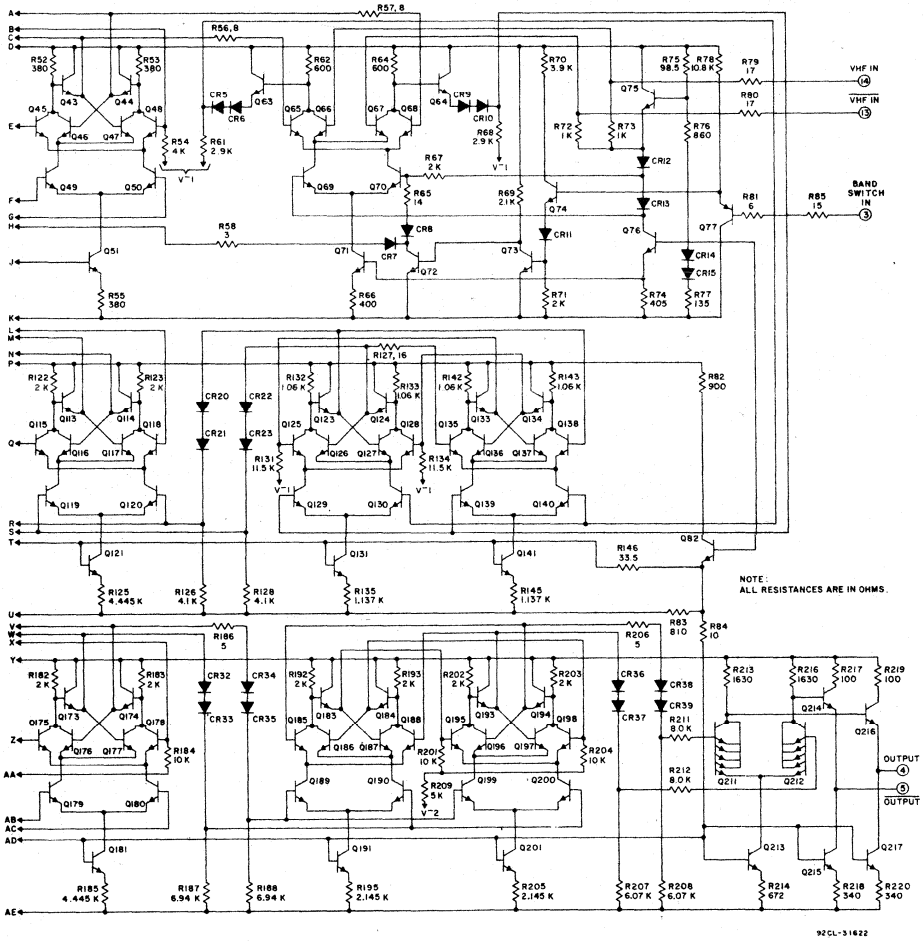


Fig. 3 - Schematic diagram (cont'd from previous page).

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V+ = 5 V, V− = 0 V

CHARACTERISTIC	TEST CONDITIONS	LIMITS Min.	Typ.	Max.	UNITS
Static (See Fig. 2)					
Supply Current, I+	Terms. 1 & 2	30	65	100	mA
Bandswitch Voltage: Low, V_{BL}	Term. 3	2.4	—	—	V
Bandswitch Voltage: High, V_{BH}	Term. 3	—	—	0.8	V
Bandswitch Current: Low, I_{BL}	V3 = 0 V	−1	—	—	mA
Bandswitch Current: High, I_{BH}	V3 = 20 V	—	—	0.5	mA
Dynamic (See Fig. 4)					
Sine Wave Sensitivity (Single-ended)	f_{IN} = 450 to 950 MHz, V3 = 5 V	0	30	80	mVRMS
Sine Wave Sensitivity (Single-ended)	f_{IN} = 80 to 450 MHz, V3 = 5 V	—	50	160	mVRMS
Sine Wave Sensitivity (Single-ended)	f_{IN} = 90 to 275 MHz, V3 = 0 V	—	5	40	mVRMS
Output Voltage: High, V_{OH}	Term. 4 or 5	—	4.2	—	V
Output Voltage: Low, V_{OL}	Term. 4 or 5	—	3	—	V
Output Voltage: Peak-to-Peak, V_{OP-P}	Term. 4 or 5	0.65	1.1	1.6	V
Output Rise or Fall Time, t_r,t_f		40	70	110	ns
Internal Bias	Term. 13 or 14	(V_{DD} − 1)			V
Internal Bias	Term. 9 or 10	(V_{DD} − 2.7)			V
DC Input Resistance, R_I	Term. 13 to 14	2000			Ω
DC Input Resistance, R_I	Term. 9 to 10	1000			Ω
Complex Input Impedance	Term.9 to 10, V_{IN} = 100 mV, f_{IN} = 950 MHz	20			Ω
Complex Input Impedance	Term.9 to 10, V_{IN} = 100 mV, f_{IN} = 450 MHz	30 - j80			Ω
Complex Input Impedance	Term.13 to 14, V_{IN} = 100mV, f_{IN} = 275 MHz	35 - j100			Ω

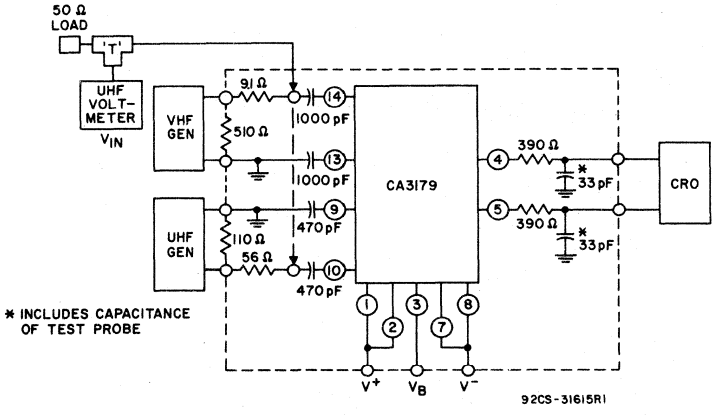


Fig. 4 - AC characteristics test circuit.

CA3179E

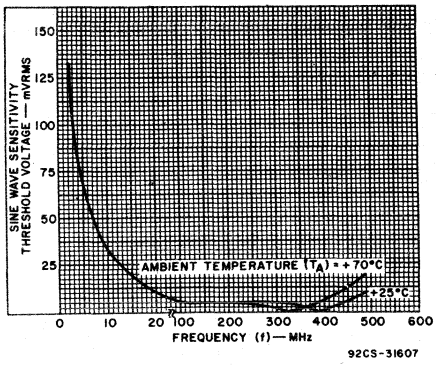


Fig. 5 - Typical threshold sensitivity in the ÷64 VHF mode.

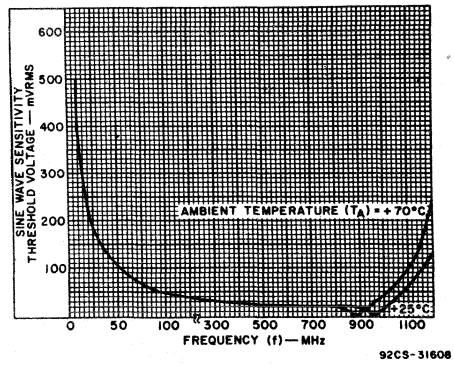


Fig. 6 - Typical threshold sensitivity in the ÷256 UHF mode.

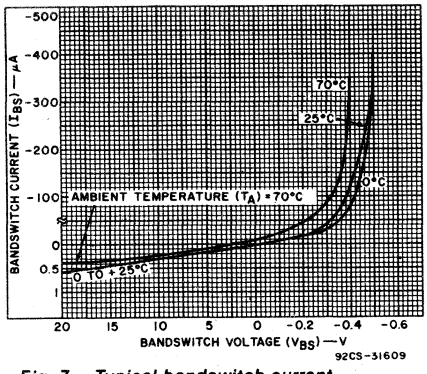


Fig. 7 - Typical bandswitch current as a function of bandswitch voltage and ambient temperature.

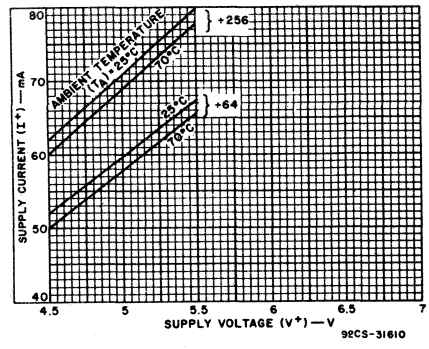


Fig. 8 - Supply current as a function of supply voltage and ambient temperature.

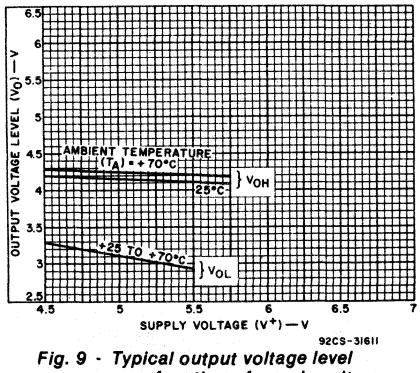


Fig. 9 - Typical output voltage level as a function of supply voltage and ambient temperature.

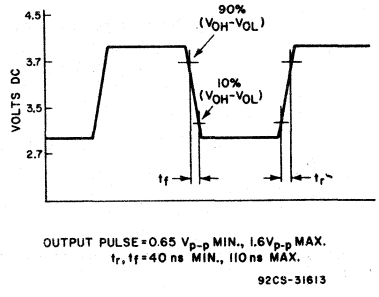


Fig. 10 - Output pulse characteristics.

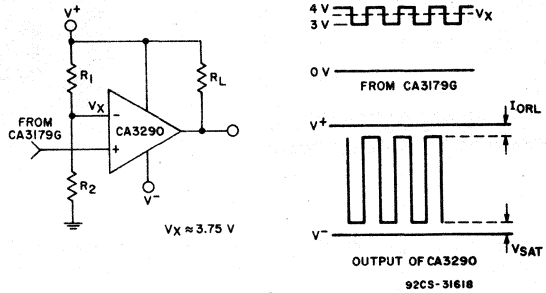


Fig. 11 - Typical bipolar interface circuit.

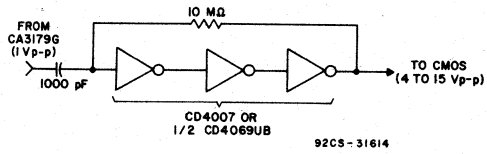
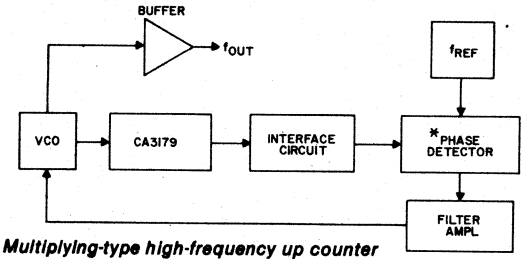
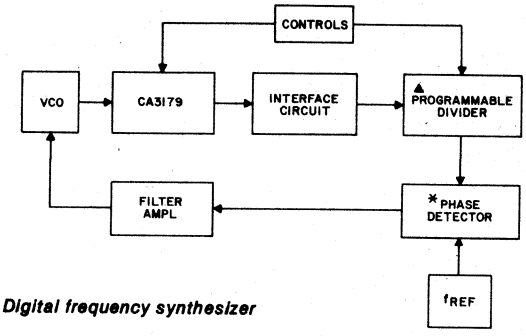


Fig. 12 - Typical CMOS interface circuit.



a) Multiplying-type high-frequency up counter



b) Digital frequency synthesizer

Fig. 13 - Typical system configuration.

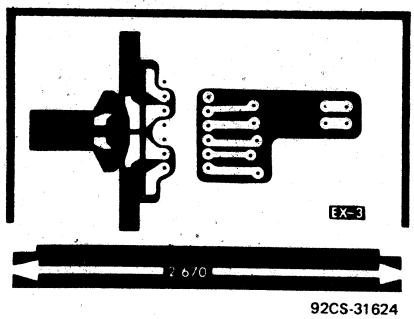


Fig. 14 - Printed-circuit board for the dynamic test circuit.

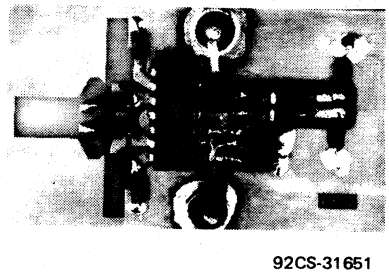
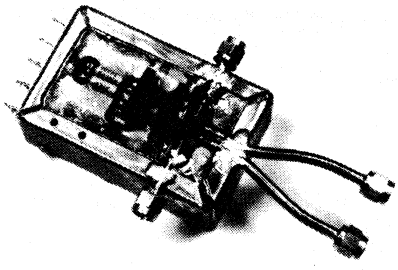


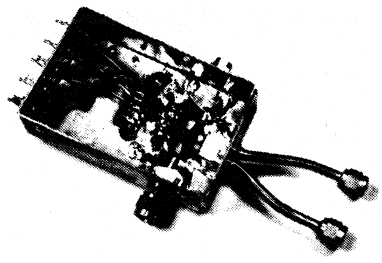
Fig. 15 - Printed-circuit board for the dynamic test circuit with components.

CA3179E



TOP VIEW

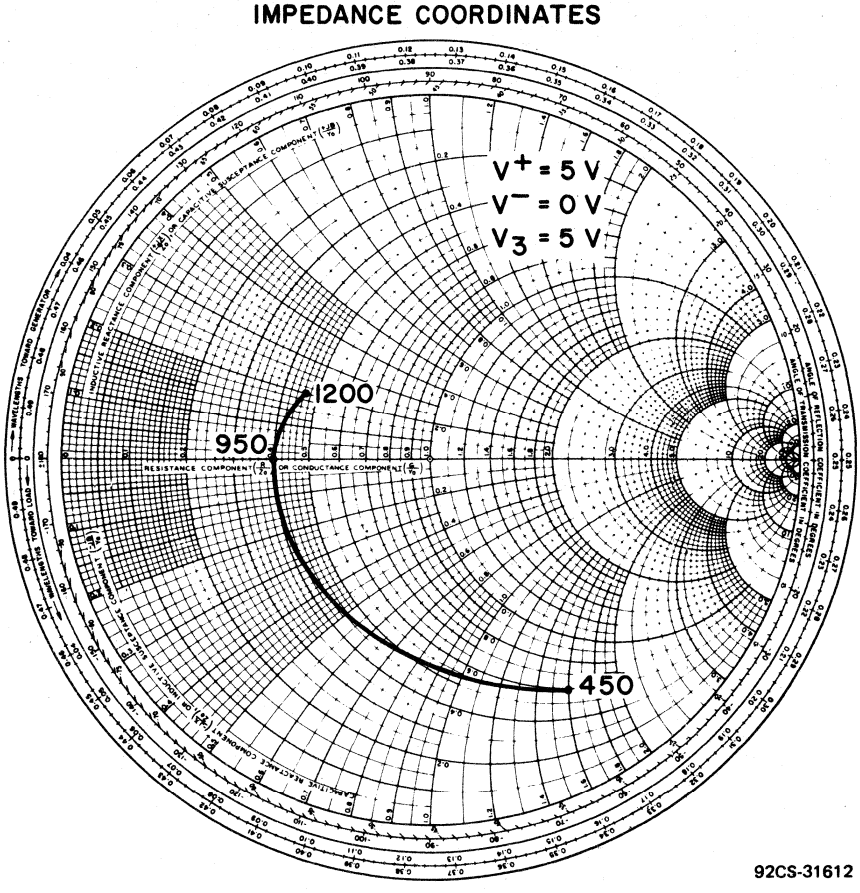
92CS-31652



BOTTOM VIEW

92CS-31653

Fig. 16 - Dynamic test circuit fixture.



92CS-31612

Fig. 17 - Impedance as a function of frequency.

High-frequency construction and design techniques must be followed if the operation of the CA3179G test circuit is to be stable and if the results of repeated tests are to be consistent. The dynamic test circuit is shown in Fig. 4, and a photo of the test fixture that houses it is shown in Fig. 16. Listed below are some precautionary construction considerations for the circuit and test fixture.

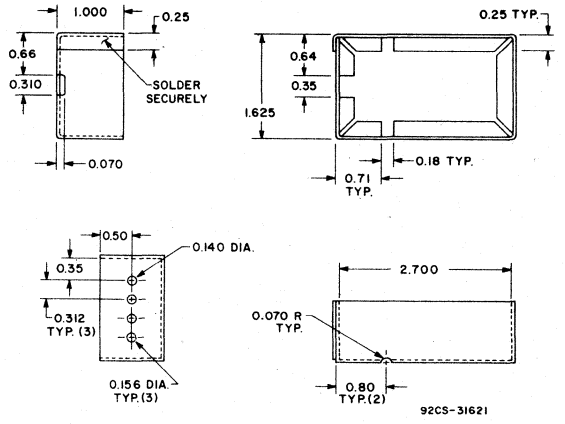
1. Supply the ground plane with frequent ground connections.
2. Use 50-Ω coaxial cable for input connections
3. Use a "dead bug" type socket to minimize lead lengths and reduce series inductances
4. Use input pads that reduce impedance mismatch at the generator-test and meter-test input interfaces
5. Use leadless ceramic disc capacitors wherever possible
5. Provide capacitor by-passing near active terminals where ac grounds are required

Specific applications may require changes in the procedures listed above. The socket, for instance, can be eliminated by soldering the device directly to the p.c. board or by using individual board-mounted socket pins. Input and output interface connections and circuitry will also vary according to specific circuit requirements.

Partial Parts List for the Dynamic Test Circuit and Fixture:

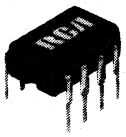
4 Pasternac PE3493-6 SMA cable connectors and semi-rigid coaxial cable
1 Chassis
1 P.C. board
1 14-lead socket
2 1000-pF capacitors, Stettner Trush Inc. No. TEFIC-7
3 470-pF disc capacitors
3 1000-pF disc capacitors
2 33-pF feedthrough capacitors
3 1000-pF feedthrough capacitors
3 Ferrite beads, 0.375 x 0.187 x 0.250
2 Resistors, 390-Ω, ¼-W, 2%
1 Resistor, 56-Ω, 1/8-W, 5%
1 Resistor, 110-Ω, 1/8-W, 5%
1 Resistor, 9.1-Ω, 1/8-W, 5%
1 Resistor, 510-Ω, 1/8-W, 5%

Dimensions of Test Fixture



CA3199E

VHF/UHF ÷ 4 Prescaler



8-Lead Dual-In-Line Plastic (Mini-DIP)

H-1817

Features:

- *Broadband operation - DC to 1.3 GHz*
- *High sensitivity*
- *Standard T^2L or ECL power supply of 5 V ± 0.5 V*
- *Complementary ECL outputs*

Applications:

- *Digital frequency synthesizers for:*
  VHF/UHF receivers
  Satellite communications
  Instrumentation
- *High-frequency divider for:*
  UHF frequency counters
  UHF timers
  High-speed computers
  Frequency standards
  SHF second IF local-oscillator injection
  PCM communications
  Satellite communications
  Radar ranging systems
- *High-frequency up-converters*

The CA3199E* is a bipolar integrated fixed-ratio (divide-by-four) counter which operates over the VHF/UHF frequency band (DC to 1.3 GHz). It accepts either single or double-ended ac-coupled input signals and provides complementary emitter follower outputs at standard ECL logic levels.

The CA3199E is supplied in an 8-lead dual-in-line plastic (Mini-DIP) package, and operates over an ambient temperature range of 0 to +85°C.

*Formerly RCA Dev. Type No. TA10853.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE ..... 5.5 V

RMS INPUT VOLTAGE ..... 0.5 V

DEVICE DISSIPATION:

UP TO T_A = 70°C ..... 630 mW

ABOVE T_A = 70°C ..... derate linearly at 7.7 mW/°C

AMBIENT TEMPERATURE RANGE:

OPERATING ..... 0 to 85°C

STORAGE ..... −55 to −150°C

LEAD TEMPERATURE (DURING SOLDERING):

AT DISTANCE 1/16 ± 1/32 IN. (1.59 ± 0.79 mm) FROM CASE FOR 10 SECONDS MAX. ..... −265°C

CA3199E

STATIC CHARACTERISTICS (T_A=25° C, V_{CC}=+5.0 V, V_5=Ground)

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
"1" Output Voltage, V_{OH}	Outputs Unloaded	—	4.2	—	V
"0" Output Voltage, V_{OL}	Outputs Unloaded	—	3.4	—	V
Internal Bias Voltage, V_{BIAS}	Pin #4 Left Floating	—	2.4	—	V
Power Supply Current Drain, I_D		35	60	85	mA

DYNAMIC CHARACTERISTICS (T_A=25° C, V_{CC}=+5.0 V, V_5=Ground)

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Input Frequency Range (sinusoidal), V_{IN}	Single-Ended Input, 1000 MHz	—	—	400	mVpp
Output Voltage Swing, V_6, V_7		0.6	0.8	—	Vpp
"1" Transition Time, t_{-+}	Output Unloaded	—	0.6	—	ns
"0" Transition Time, t_{+-}	Output Unloaded	—	0.6	—	ns
Input Capacitance, C_{IN}		—	2.5	—	pF
Input Resistance, R_{IN}		—	400	—	Ω

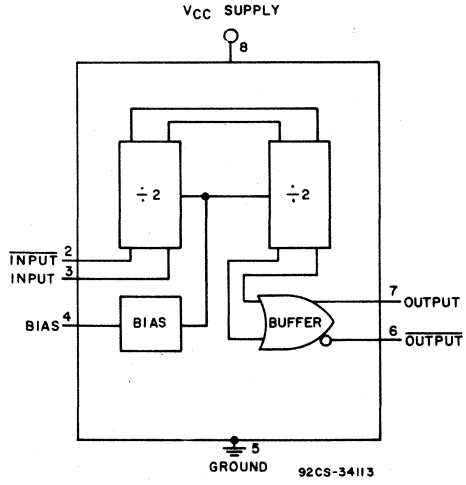


Fig. 1 - Logic diagram for divide-by-four counter.

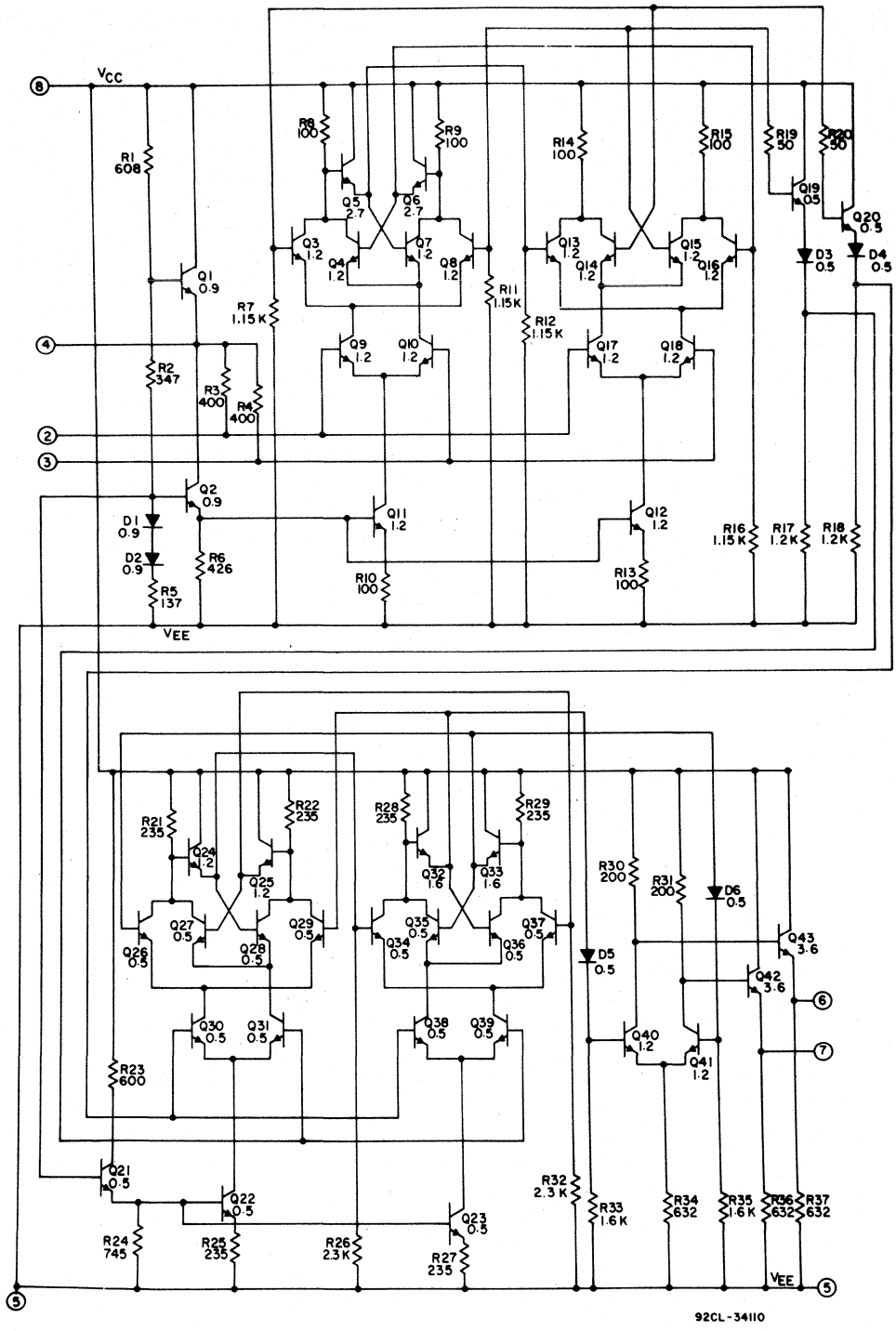


Fig. 6 - Schematic diagram for CA3199E.

CA3199E

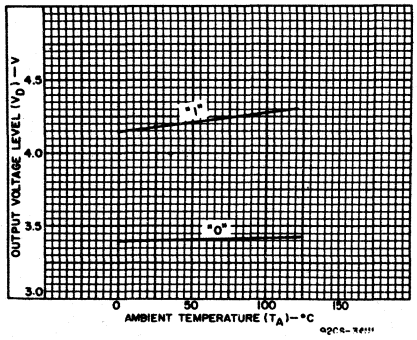


Fig. 2 - Typical output levels as a function of ambient temperature.

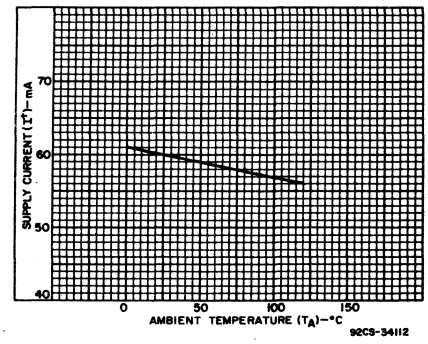


Fig. 3 - Typical power-supply current as a function of ambient temperature.

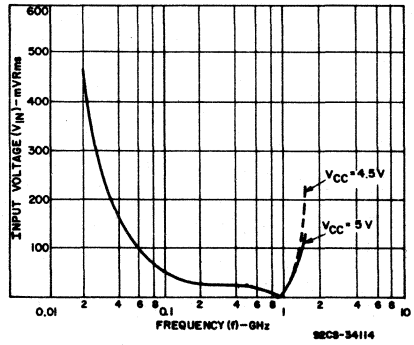


Fig. 4 - Sinusoidal input sensitivity.

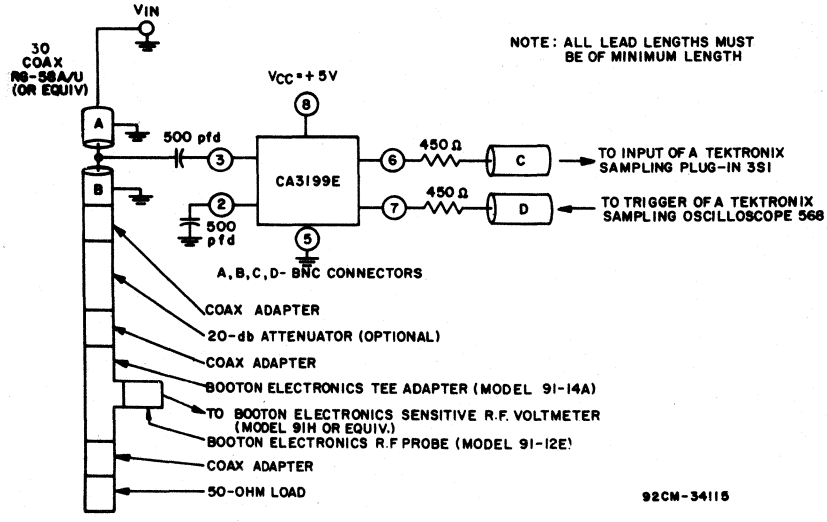
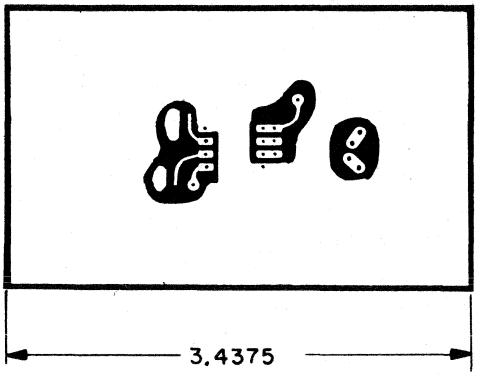


Fig. 5 - Test circuit for CA3199E.



92CS-34146

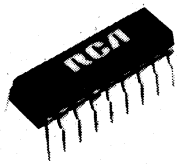
Fig. 7 - Printed-circuit board for the test circuit.

Application and Test Notes

1. Both complementary inputs and outputs are provided. When driven single-ended, normally at pin 3, the unused input (pin 2) should be ac by-passed (500 pF) to ground for best performance.
2. Internal bias monitor, pin 4, is normally left floating or ac by-passed to ground.
3. Device inputs should be ac coupled to the signal source. 500-pF coupling capacitors are adequate above 50 MHz.
4. Input signal voltage (sinusoidal) required is 100 mV RMS (typical) over the frequency range of 100-1000 MHz
5. When the input signal voltage is a square wave, a rise time of ≤5 ns is required. The signal should be 400-800 mV peak-to-peak over the frequency range from dc-1000 MHz. This corresponds to an input slew rate minimum of 62.5 V/μs.
6. All test data are for the 8-pin dual-in-line packaged circuit as mounted in a standard IC socket. Somewhat improved higher frequency performance can be obtained by attaching directly to a suitable PC board.
7. High-frequency construction and design techniques must be followed if the operation of the test circuit is to be stable and if the results of repeated tests are to be consistent. Listed below are some precautionary construction considerations for the circuit and test fixture.
    1. Supply the ground plane with frequent ground connections.
    2. Use 50-Ω coaxial cable for input connections.
    3. Use a "dead bug" type socket to minimize lead lengths and reduce series inductances.
    4. Use input pads that reduce impedance mismatch at the generator-test and meter-test input interfaces.
    5. Use leadless ceramic disc capacitors wherever possible.
    6. Provide capacitor by-passing near active terminals where ac grounds are required.

Specific applications may require changes in the procedures listed above. The socket, for instance, can be eliminated by soldering the device directly to the PC board or by using individual board-mounted socket pins. Input and output interface connections and circuitry will also vary according to specific circuit requirements.

CA3211E



H-1899

18-Lead Dual-In-Line Plastic Package E Suffix

VHF/UHF Prescaler

Features

- *Divide by 256*
- *Input frequency to 1 GHz*
- *Dual input ports electrically selectable*
- *Input sensitivity*
  < 10 μW typical
  (Generator available power into a 50-Ω load)
- *5-V power supply*
- *Balanced output ports*

The RCA-CA3211E* is an integrated-circuit prescaler intended for use in TV frequency synthesis tuning systems over an input frequency range of 90 to 1000 MHz. It performs division by 256 in the UHF and VHF mode.

The mode of operation can be selected by means of the bandswitch and the separate UHF and VHF input terminals provided. The output is a complementary emitter-coupled stage with controlled slew rate for harmonic suppression.

The CA3211E is supplied in a 18-lead dual-in-line plastic package.

*Formerly RCA Developmental No. TA11355.

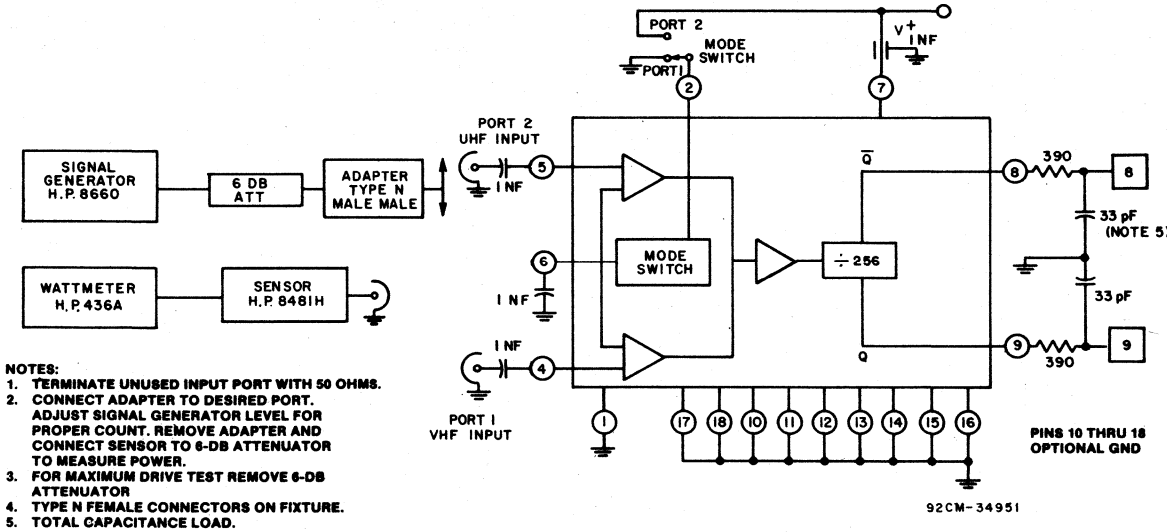


Fig. 1 - Block diagram and test circuit of the CA3211E.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE ..... 6 V
DC BANDSWITCH VOLTAGE ..... 20 V
RMS INPUT VOLTAGE ..... 0.5 V
DEVICE DISSIPATION:
To 70°C ..... 890 mW
Above 70°C ..... Derate linearly at 11.1 mW/°C
AMBIENT TEMPERATURE:
Operating ..... −40 to +85°C
Storage ..... −65 to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 in. (1.59 mm ± 0.79 mm) from case for 10 s max. ..... 265°C

ELECTRICAL CHARACTERISTICS, T_A=25° C, V+=5.0 V

CHARACTERISTIC	LIMITS			UNITS
	Min.	Typ.	Max.	
Supply Current, Terminal 7	30	65	110	mA
Band Change Voltage:				
Port 1 Select (VHF)	−0.5	0	0.6	V
Port 2 Select (UHF)	3	5	18	
Band Change Current, Terminal 2:				
At 0 Volts	—	—	−1	mA
At 18 Volts	—	—	2	
Divide Ratio, $f_{IN} \div f_{OUT}$:				
Port 1, f_{IN} 80-500 MHz	—	256	—	Ratio
Port 2, f_{IN} 80-1000 MHz	—	256	—	
Input Sensitivity, f_{IN}:				
40 MHz	—	15	—	mV rms
80 MHz	—	10	35	
150-800 MHz	—	10	20	
900 MHz	—	10	35	
1000 MHz	—	15	45	
Maximum Drive Level:				
80-1000 MHz	500	—	—	mV rms
Output at Terminal 9 or 8:				
Mean Value	—	3.5	—	V dc
Peak-Peak Swing	0.75	1	—	V_{p-p}
Rise or Fall Time	—	70	—	ns
Internal Bias at Terminal 6	—	2	—	V dc
Internal Bias, Terminal 2=5 V:				
At Terminal 4	—	0.07	—	V dc
At Terminal 5	—	2	—	

CA3211E

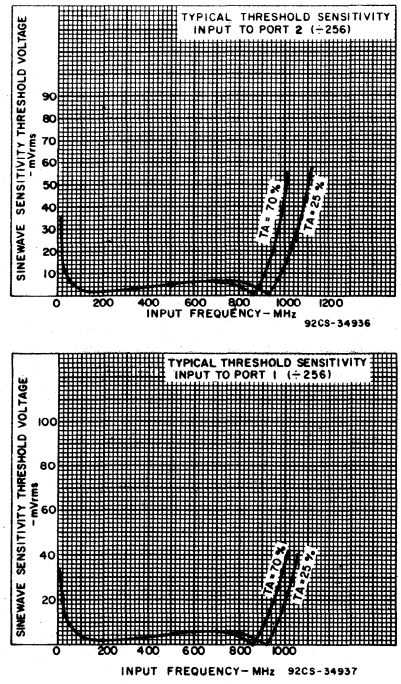
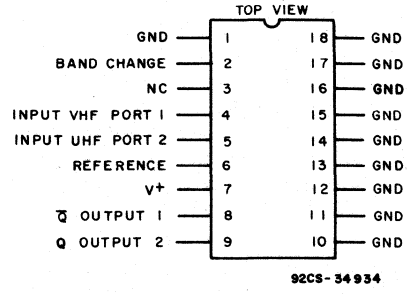
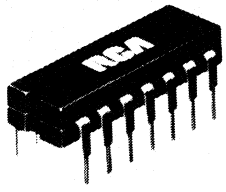


Fig. 2 - Sinewave sensitivity threshold voltage as a function of input frequency.



TERMINAL DIAGRAM



14-Lead Dual-In-Line Plastic Package H-1517

BiMOS Single-Chip Detector/Alarm System

With Integral Drivers for Mechanical and Piezoelectric Horn Alarms

Features:

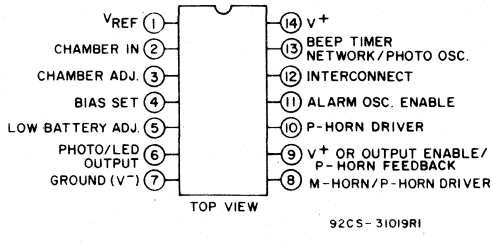
- *Interfaces directly with high Z sensors — no external buffer FET required*
- *Low input current: 1 pA max.*
- *Gate-protected input terminals*
- *On-chip beep oscillator for low battery indication*
- *Self-contained low-battery-voltage detection circuit*
  - *(a) Fixed or adjustable trip point available*
  - *(b) Dynamic battery test when filter capacitor = 2 μF*

The RCA-CA3164E is a monolithic BiMOS integrated circuit designed to meet the stringent system requirements of a battery- or line-operated alarm circuit. When used with an ionization chamber and electromechanical or piezoelectric horn, it provides a one-chip approach to smoke detection. No external active devices are required to interface with either the chamber input or horn output terminals. The CA3164E can also be used with photoelectric chambers by the addition of several external components.

The CA3164E is supplied in the 14-lead dual-in-line plastic package.

- *Chamber trigger voltage independent of battery supply voltage (less than 150 mV over temperature and supply variations)*
- *Reference source current available = 5 μA (typ.)*
- *Low standby battery current = 8 μA (typ.)*
- *Can be used with photoelectric sensors by using a minimum of external passive components in combination with the RCA-CA3078 micropower op-amp*
- *Multiple-unit interconnect terminal controls a common annunciator circuit*
  - *(a) A fault to ground doesn't prevent local operation*
  - *(b) The low battery alarm signal triggers only the local unit*
- *LED output indicates status of smoke-detector circuit*
- *Operates from 11 V (max.) supply (either battery or line)*
- *Battery reversal protection feature*

TERMINAL ASSIGNMENT



92CS-31019RI

CA3164E

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE, V+ ..... +11 V
DEVICE DISSIPATION, P_D:
Up to $T_A = 25°C$ ..... 600 mW
Above $T_A = 25°C$ derate linearly at ..... 6.7 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating ..... 0 to +50°C
Storage ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, V+ = 9 V

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Operating Voltage		7	9	11	V
Common-Mode Input Voltage Range, V_{ICR}	(V+ − 2 V) = 7 V	0	—	7	V
Low-Battery Trigger Voltage	External adjust (increase only)	7.3	7.7	7.9	V
Horn Driver V_{CE}(sat)	Term. 8 = 100 mA	—	—	0.5	V
	Term. 8 = 300 mA	—	—	1.1	
Reference Voltage	Term. 1	6.1	6.5	6.9	V
Input Leakage Current, I_L	Term. 2	—	—	1	pA
	Term. 2 at 50°C	—	—	2.5	
	Term. 3	—	—	50	
Standby Current (10 MΩ from Term. 4 to gnd)	No LED connected	—	8*	14	μA
	LED connected - 20 mA for 30 ms every 60 s	—	18	—	
	Photoelectric operation - LED photocurrent = 0.6 A (5-second rate)	—	13	—	
Reference Source Current		5	—	—	μA
LED Driver Sink Current	Term. 6	20	50	—	mA
Output Sink Current — Term. 8	Term. 8 = 1.1 V	200	300	—	mA
Output Sink Current — Term. 8	Term. 8 = 0.5 V	100	150	—	
Output Sink Current — Term. 10	Term. 10 = 2 V	20	25	—	
Output Source Current — Term. 8	Term. 8 = V+ − 2 V	20	25	—	mA
Output Source Current — Term. 10	Term. 10 = V+ − 2 V	20	25	—	
Interconnect Current Source	$V_O = 0$ V	1.5	3.5	6	mA
Interconnect Current Sink	$V_O = 9$ V	—	45	65	μA
Remote Fan-Out		20	—	—	
Low-Battery Adjust, Term.5 Input Current		50	70	225	nA
Timing Current	Term. 13	10	—	62	nA
LED Blink Period	Adjustable	—	—	1	PPM
LED Pulse Width	Fixed	—	30	—	ms
Alarm Pulse Duty Cycle (4.7 MΩ from Term. 11 to gnd)	On-time	—	95	—	%
	On-time = 95%	—	0.5	—	sec.
	Off-time = 5%	—	0.026	—	

*Adjustable to 5 μA.

OPERATING MODE TRUTH TABLE

CONDITION	BATTERY	LED TERM. 6	ALARM HORN TERMS. 8, 9, 10	SYSTEM REMOTE OUTPUT TERM. 12	REMOTE UNIT ALARM STATUS
No Smoke In Chamber	NORMAL	BLINK[1]	OFF	LOW	OFF
No Smoke In Chamber	LOW	BLINK[1]	BEEP[1]	LOW	OFF
Smoke In Chamber	X	ON	ON[2]	HIGH	ON
Remote Alarm On, No Smoke In Local Chamber	X	BLINK[1]	ON[2]	HIGH[3]	ON

X = Don't Care

1. 30-ms pulse every 50 seconds (typ.).
2. Alarm horn may be programmed for continuous sound by connecting terminal 11 to V+. The alarm may be pulsed by connecting terminal 11 to ground through a resistor (from 3.9 to 10 MΩ). The typical duty cycle is 95% ON, and is determined by the size of the resistor.
3. Signal received from activated remote alarm.

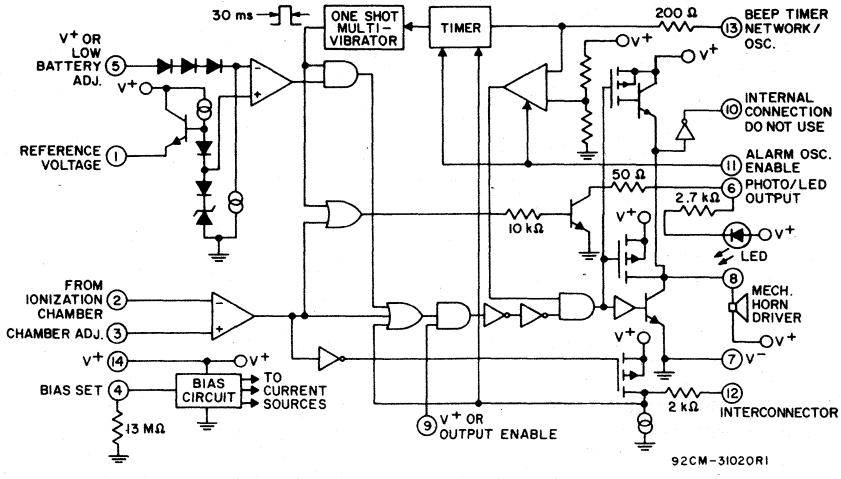


Fig. 1 - Simplified functional diagram for CA3164E.

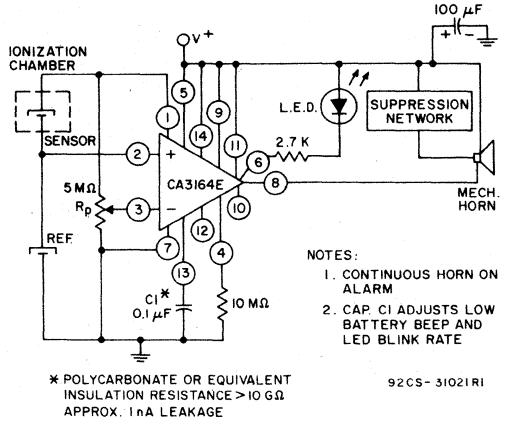


Fig. 2 - Basic ionization detector with electromechanical horn.

CA3164E

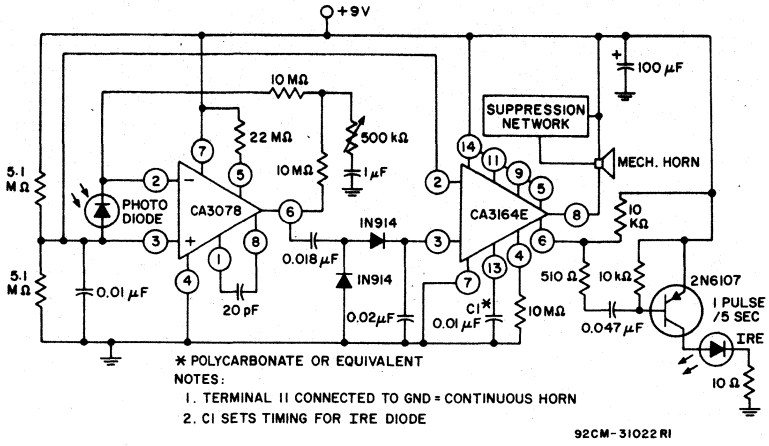


Fig. 3 - Typical photoelectric system using CA3164E.

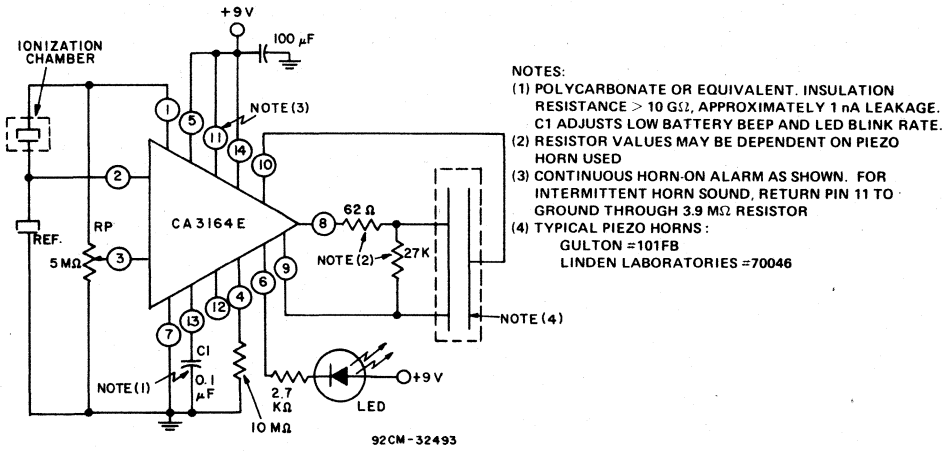
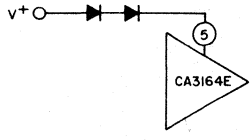


Fig. 4 - Basic ionization detector with piezoelectric horn.

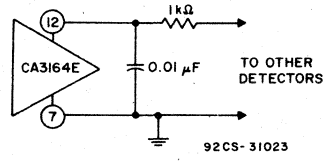
Connections for Optional Functions

1. **Low Battery Adjustment - Terminal 5**
   Add diodes as shown below to increase the low-battery trigger point.



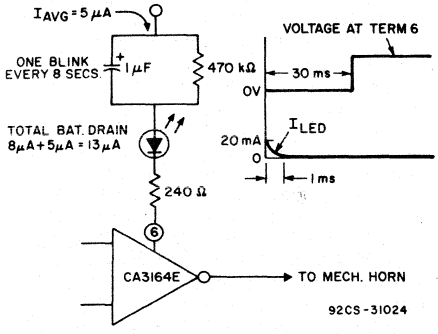
2. **Sounder Operating Mode**
   Continuous sound on alarm - connect terminal 11 to V+.
   Pulsed sound on alarm - connect a 3.9-MΩ resistor between terminal 11 and ground.

3. **Remote (Interconnect)**
   Connect terminal 12 to same terminal on all other units (fan out = 20 units). When interconnecting units for the remote-alarm function, the extremely low currents involved make it extremely important that a provision be made for limiting externally induced transients into the remote terminal. For example, inadvertent contact with external power sources or electrical storm activity may cause triggering of the remote alarm function. The circuit below will reduce the possibility of such occurrences.



4. LED On-Time Adjustment

The CA3164E is designed to provide a fixed LED on-time of approximately 30 ms. For applications requiring a reduction in on-time, the following circuit is recommended:



This circuit reduces the LED on-time but does not affect the horn on-time of 30 ms. When using this configuration during the continuous-alarm mode (smoke in chamber), the LED will be off instead of on, as shown in the truth table. If the horn is pulsed during the alarm mode, the LED will blink at the pulse rate.

Cleaning Procedure

To insure leakage currents of less than 1 pA, the following procedure is recommended:

(a) degrease in trichlorethylene
(b) rinse in de-ionized water

Circuit Description

Basic Functions - The CA3164E is designed to interface directly with an ionization-chamber type of smoke detector. Upon being triggered by a decreasing voltage at the ionization-chamber output, the IC operates a mechanical transducer. In addition to this basic smoke-detector function, another circuit monitors and compares the battery voltage to an internal reference-voltage source. Once the battery voltage drops below a defined level, a short 30-ms beep sound is produced in synchronism with an LED indicator every 50 seconds. This rate is determined by a programming resistor connected between terminal 4 and ground and an external 0.1-μF capacitor connected between terminal 13 and ground.

A buffered output voltage is available from the reference supply that may be used to operate the ionization chamber. This voltage helps maintain constant sensitivity with decreasing supply voltage.

There are two alarm modes and two conditions that will sound the alarm. The first alarm condition is the normal smoke in the ionization chamber; the other condition is a high level to the remote input/output terminal of the IC.

The first alarm mode is the customary continuous sound. The second alarm mode is an interrupted or pulsed sound.

Operation - The CA3164E is current programmable by placing a resistor from terminal 4 to ground. This resistor establishes the operating current levels for all the current sources within the IC including the timing circuits.

An operational amplifier configuration is used for the ionization chamber input. P-channel MOS field-effect transistors are used on this input in the bootstrap configuration shown in Fig. 5 to drive the protection diodes and maintain the sub-picoampere input current.

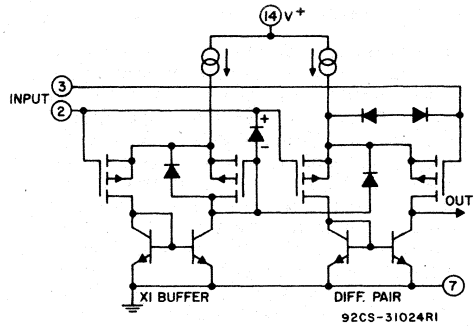


Fig. 5 - Schematic of ionization-chamber amplifier.

A conventional bipolar amplifier is used for the battery monitor circuit. The zener diode is biased at about 3 μA. This zener voltage is raised one V_{AK} and then applied to the base of an emitter-follower transistor to buffer and reflect the zener voltage to the outside reference terminal. By providing an additional input terminal (terminal 5), where three level-shifting diodes are available, an additional external means is provided to raise the voltage level at which the CA3164E goes into the low-voltage alarm mode.

An integrating type of timer is used to generate the one-minute LED power-monitor and battery-function indicator pulse. Fig. 6 shows the system. A constant-current source charges the external 0.1-μF timing capacitor C_T, which subsequently triggers the 30-ms one-shot multivibrator composed of n-channel MOS transistor N_3 and n-p-n transistor Q1.

N_3 is then cut off and its drain climbs to the supply rail, linearly charging capacitor C_{PULSE}. When the drain of N_3 reaches the supply rail, the charging current ceases, cutting off the base current of Q1 and discharging the capacitor.

A open-collector n-p-n transistor is used to drive the optional external LED power monitor and battery-condition indicator (Fig. 1).

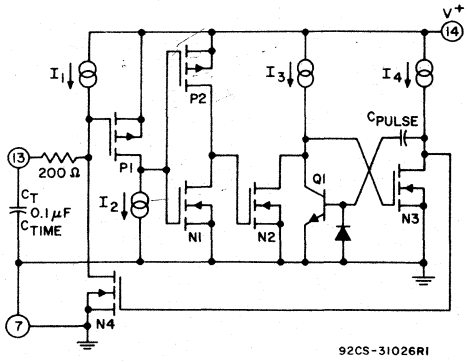


Fig. 6 - Schematic of timer and one-shot multivibrator.

The schematic diagram of the drive circuit for a mechanical horn (M-horn) and a piezoelectric horn (P-horn) is shown in Fig. 7. For M-horn operation, the output of the driver at terminal 8 is used. A large n-p-n transistor Q3 with an active pull-up transistor Q2 provide over 300 mA of drive current. In the M-horn mode, terminal 9 must be returned directly to V+. P-horn operation requires the output from a second inverting amplifier at terminal 10, as well as the output from terminal 8. For P-horn operation, terminal 9 is connected to the feedback terminal of the horn.

The horn output, on alarm, can be continuous or pulsed. The mode is determined by the connection of terminal 11. When this terminal is connected to V+, the alarm sound is continuous, and when it is connected to ground through a programming resistor, as shown in Fig. 7, the alarm is pulsed. The pulse rate is determined by the sum of the current through the programming resistor connected to terminal 11 and the current from the basic timer-current source. Thus, when the detector goes into the alarm mode, the nominal 50-second time period is decreased to a nominal 0.5-second period. This 0.5-second period is set by the external 3.9-MΩ resistor. PMOS transistor P4 and bipolar transistor Q6 provide the on-off switching of NMOS transistor N4 in the driver circuit to provide the pulsed output from the horn.

Terminal 12, the interconnect terminal, is both an input and output for the circuit. When connected by two wires to other units, alarm in any one unit will activate the other units. A small sinking current of only 10 μA keeps the line impedance down while a sourcing current of over 2 mA is available in the alarm mode. This current is more than sufficient to trigger over 20 additional units.

Other Applications of the CA3164E

Although the primary function of the CA3164E is smoke detection, it may also be used in many other circuits that require high front-end sensitivity and the very high input resistance of MOS transistors. The internal circuitry of the CA3164E requires a minimum of external components, and the low battery drain eliminates the need for ac power in most circuits.

A few of the possible uses are: humidity sensor, where two metal electrodes replace the ionization chamber; intrusion alarm; P-horn driver; controller for a dc-to-dc converter such as might be used in an electronic photoflash unit; or with a photodiode as an automatic switch for turning on night lights.

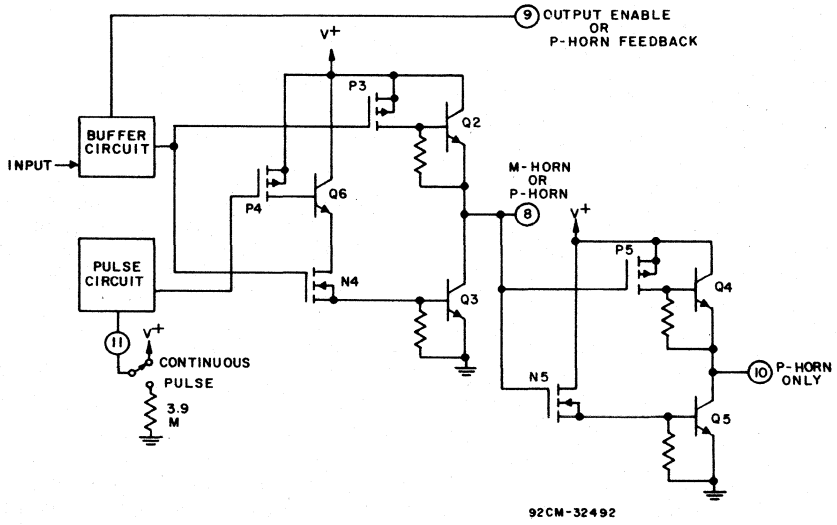
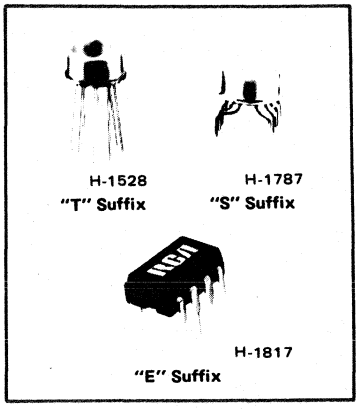


Fig. 7 - Schematic of mechanical and piezoelectric horn drivers.



Timers

For Timing Delays & Oscillator Applications in Commercial, Industrial, and Military Equipment

CA555T, CA555CT:	Standard 8-Lead TO-5 Style Package
CA555S, CA555CS:	Standard 8-Lead TO-5 Style Package With Formed Leads (DIL-CAN)
CA555E, CA555CE:	8-Lead Dual-In-Line Plastic Package (MINI-DIP)

Features:

- *Accurate timing from microseconds through hours*
- *Astable and monostable operation*
- *Adjustable duty cycle*
- *Output capable of sourcing or sinking up to 200 mA*
- *Output capable of driving TTL devices*
- *Normally ON and OFF outputs*
- *High-temperature stability - 0.005%/°C*
- *Directly interchangeable with SE555, NE555, MC1555, and MC1455*

Applications

- *Precision timing*
- *Sequential timing*
- *Time-delay generation*
- *Pulse generation*
- *Pulse-width and position modulation*
- *Pulse detector*

The RCA-CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours. These devices are also useful for astable oscillator operation and can maintain an accurately controlled free-running frequency and duty cycle with only two external resistors and one capacitor.

The circuits of the CA555 and CA555C may be triggered by the falling edge of the wave-form signal, and the output of these circuits can source or sink up to a 200-milliampere current or drive TTL circuits.

The CA555 and CA555C are supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead TO-5 style packages with dual-in-line formed leads (DIL-CAN, S suffix), 8-lead dual-in-line plastic packages (MINI-DIP, E suffix), and in chip form (H suffix). These types are direct replacement for industry types in packages with similar terminal arrangements e.g. SE555 and NE555, MC1555 and MC1455, respectively. The CA555 type circuits are intended for applications requiring premium electrical performance. The CA555C type circuits are intended for applications requiring less stringent electrical characteristics.

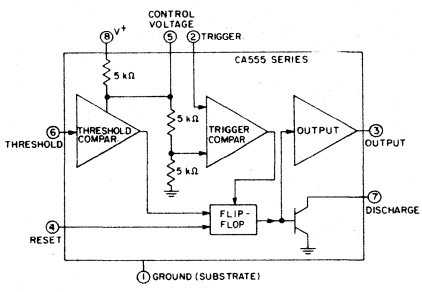


Fig. 1 — Functional diagram of the CA555 series.

CA555, CA555C Types

ELECTRICAL CHARACTERISTICS, *At $T_A = 25^oC$, $V^+ = 5$ to 15 V unless otherwise specified*

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA555			CA555C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
DC Supply Voltage, V^+		4.5	–	18	4.5	–	16	V
DC Supply Current (Low State)*, I^+	$V^+ = 5$ V, $R_L = \infty$	–	3	5	–	3	6	mA
	$V^+ = 15$ V, $R_L = \infty$	–	10	12	–	10	15	mA
Threshold Voltage, V_{TH}		–	(2/3)V^+	–	–	(2/3)V^+	–	V
Trigger Voltage	$V^+ = 5$ V	1.45	1.67	1.9	–	1.67	–	V
	$V^+ = 15$ V	4.8	5	5.2	–	5	–	
Trigger Current		–	0.5	–	–	0.5	–	μA
Threshold Current▲, I_{TH}		–	0.1	0.25	–	0.1	0.25	μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current		–	0.1	–	–	0.1	–	mA
Control Voltage Level	$V^+ = 5$ V	2.9	3.33	3.8	2.6	3.33	4	V
	$V^+ = 15$ V	9.6	10	10.4	9	10	11	V
Output Voltage Drop: Low State, V_{OL}	$V^+ = 5$ V, $I_{SINK} = 5$ mA	–	–	–	–	0.25	0.35	V
	$I_{SINK} = 8$ mA	–	0.1	0.25	–	–	–	
	$V^+ = 15$ V, $I_{SINK} = 10$ mA	–	0.1	0.15	–	0.1	0.25	V
	$I_{SINK} = 50$ mA	–	0.4	0.5	–	0.4	0.75	
	$I_{SINK} = 100$ mA	–	2.0	2.2	–	2.0	2.5	
	$I_{SINK} = 200$ mA	–	2.5	–	–	2.5	–	
High State, V_{OH}	$V^+ = 5$ V, $I_{SOURCE} = 100$ mA	3.0	3.3	–	2.75	3.3	–	V
	$V^+ = 15$ V, $I_{SOURCE} = 100$ mA	13.0	13.3	–	12.75	13.3	–	
	$I_{SOURCE} = 200$ mA	–	12.5	–	–	12.5	–	
Timing Error (Monostable): Initial Accuracy	R_1, R_2 = 1 to 100 kΩ, C = 0.1 μF, Tested at $V^+ = 5$ V, $V^+ = 15$ V	–	0.5	2	–	1	–	%
Frequency Drift with Temperature		–	30	100	–	50	–	p/m/^oC
Drift with Supply Voltage		–	0.05	0.2	–	0.1	–	%/V
Output Rise Time, t_r		–	100	–	–	100	–	ns
Output Fall Time, t_f		–	100	–	–	100	–	ns

* When the output is in a high state, the dc supply current is typically 1 mA less than the low-state value.

▲ The threshold current will determine the sum of the values of R_1 and R_2 to be used in Fig. 16 (astable operation): the maximum total $R_1 + R_2 = 20$ MΩ.

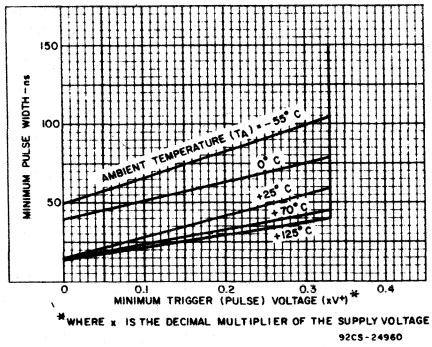


Fig.2 – Minimum pulse width vs. minimum trigger voltage.

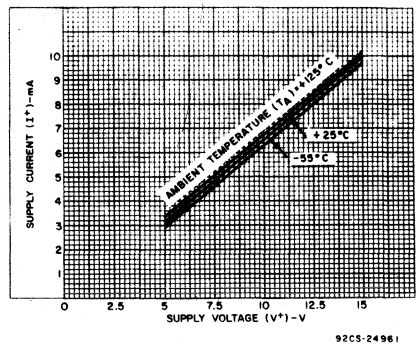


Fig.3 – Supply current vs. supply voltage.

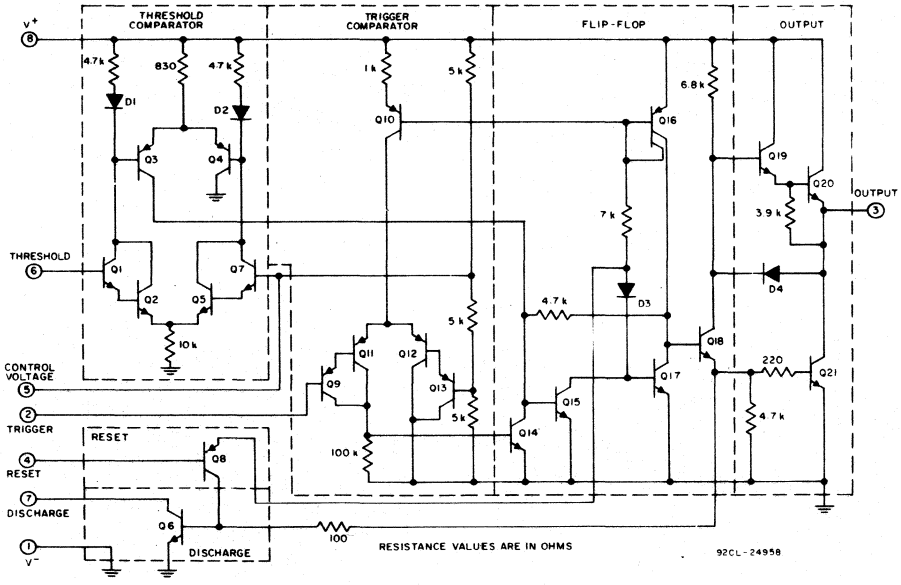
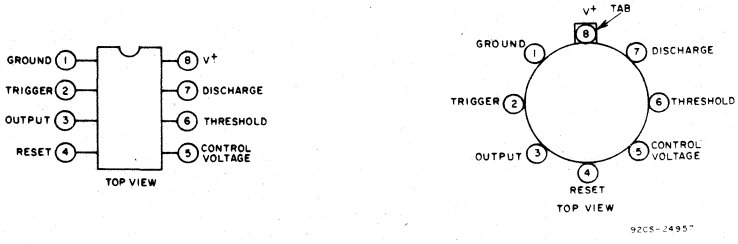


Fig.4 – Schematic diagram of the CA555 and CA555C.



a. MINI-DIP plastic package
TO-5 style package with formed leads

b. TO-5 style package

Fig.5 – Terminal assignment diagrams.

CA555, CA555C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE . . .	18	V
DEVICE DISSIPATION:		
Up to T_A = 55°C	600	mW
Above T_A = 55°C Derate linearly	5	mW/°C
AMBIENT TEMPERATURE RANGE (All Types):		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. . . .	+265	°C

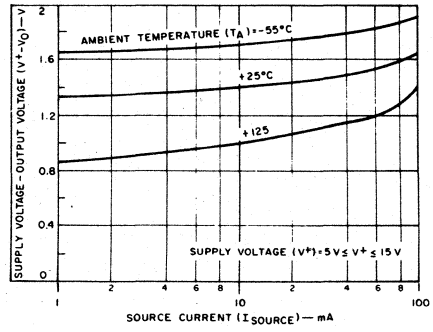


Fig.6 — Output voltage drop (high state) vs. source current.

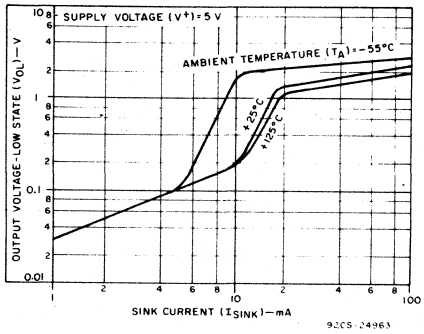


Fig.7 — Output voltage-low state vs. sink current at V^+ = 5 V.

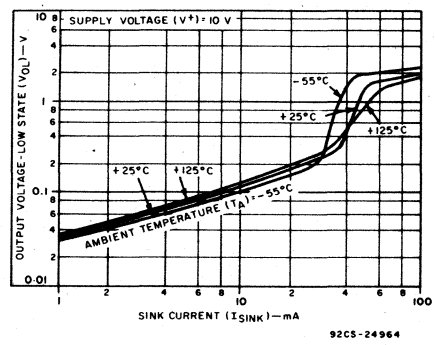


Fig.8 — Output voltage-low state vs. sink current at V^+ = 10 V.

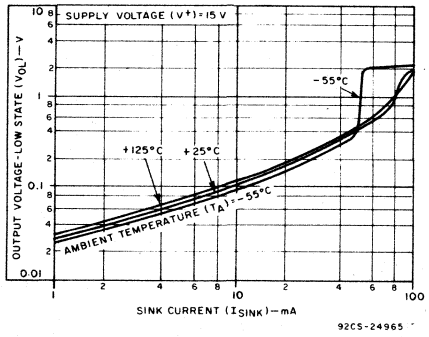


Fig.9 — Output voltage-low state vs. sink current at V^+ = 15 V.

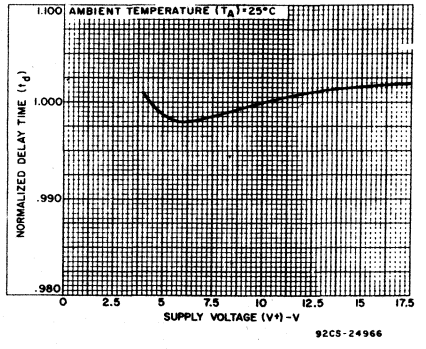


Fig.10 — Delay time vs. supply voltage.

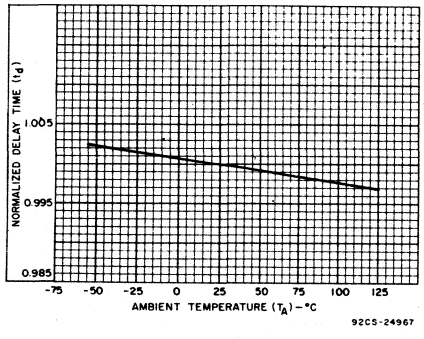


Fig.11 — Delay time vs. temperature.

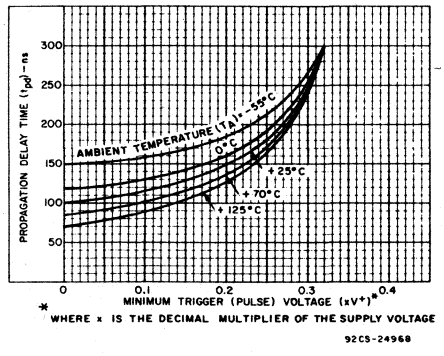


Fig.12 — Propagation delay time vs. trigger voltage.

TYPICAL APPLICATIONS

Reset Timer (Monostable Operation)

Fig.13 shows the CA555 connected as a reset timer. In this mode of operation capacitor C_T is initially held discharged by a transistor on the integrated circuit. Upon closing the "start" switch, or applying a negative trigger pulse to terminal 2, the integral timer flip-flop is "set" and releases the short circuit across C_T which drives the output voltage "high" (relay energized). The action allows the voltage across the capacitor to increase exponentially with the time constant $t = R_1C_T$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state.

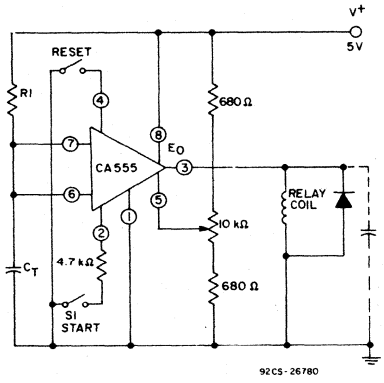


Fig.13 – Reset timer (monostable operation).

Since the charge rate and threshold level of the comparator are both directly proportional to V^+, the timing interval is relatively independent of supply voltage variations. Typically, the timing varies only 0.05% for a 1 volt change in V^+.

Applying a negative pulse simultaneously to the reset terminal (4) and the trigger terminal (2) during the timing cycle discharges C_T and causes the timing cycle to restart. Momentarily closing only the reset switch during the timing interval discharges C_T, but the timing cycle does not restart.

Fig.14 shows the typical waveforms generated during this mode of operation, and Fig.15 gives the family of time delay curves with variations in R_1 and C_T.

Repeat Cycle Timer (Astable Operation)

Fig.16 shows the CA555 connected as a repeat cycle timer. In this mode of operation, the total period is a function of both R_1 and R_2;

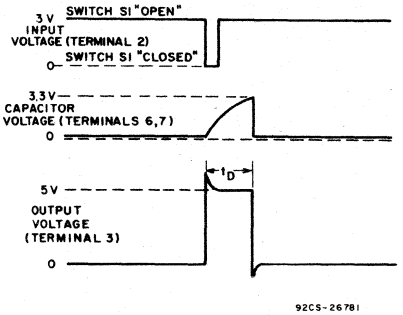


Fig.14 – Typical waveforms for reset timer.

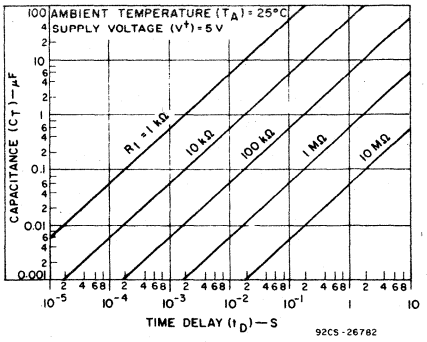


Fig.15 – Time delay vs. resistance and capacitance.

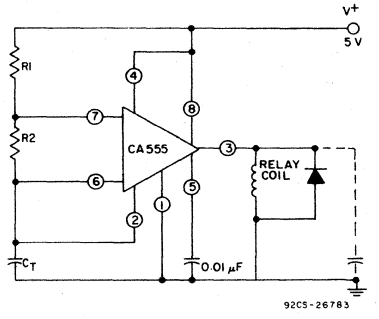


Fig.16 – Repeat cycle timer (astable operation).

$$T = 0.693(R_1 + 2R_2)C_T = t_1 + t_2$$

where $t_1 = 0.693(R_1 + R_2)\,C_T$

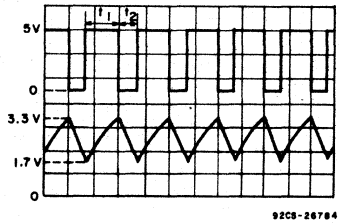
and $t_2 = 0.693(R_2)C_T$

The duty cycle is:

$$\frac{t_2}{t_1 + t_2} = \frac{R_2}{R_1 + 2R_2}$$

Typical waveforms generated during this mode of operation are shown in Fig. 17. Fig. 18 gives the family of curves of free running frequency with variations in the value of $(R_1 + 2R_2)$ and C_T.

CA555, CA555C Types



Top Trace: Output voltage (2V/div. and 0.5 ms/div.)
Bottom Trace: Capacitor voltage (1 V/div. and 0.5 ms/div.)

Fig.17 – Typical waveforms for repeat cycle timer.

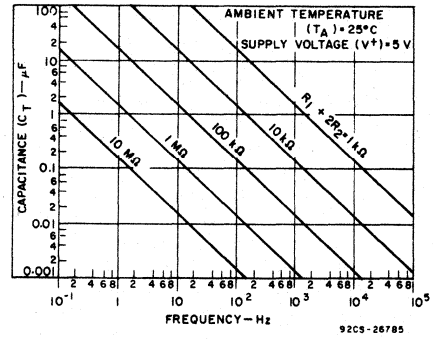
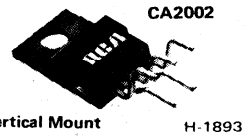


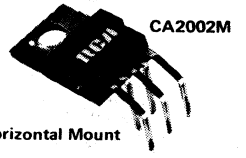
Fig.18 – Free running frequency of repeat cycle timer with variation in capacitance and resistance.

Audio Circuits
Technical Data

CA2002, CA2002M



Vertical Mount H-1893



Horizontal Mount

VERSA-V TO-220-Style Plastic Packages H-1894

8-Watt Audio Power Amplifier

Especially suited for automobile and other mobile applications

FEATURES:

- *Output short-circuit and thermal overload protection*
- *Drives load impedance as low as 1.6Ω*
- *Load dump voltage surge protection*
- *Output current capability of up to 3.5A*
- *Few external components*
- *Versa-V power transistor package-requires no electrical insulation*

The RCA-CA2002 is a monolithic silicon class B audio power amplifier designed for driving loads as low as 1.6Ω. It provides a high output current capability (up to 3.5A), very low harmonic and cross-over distortion, and load-dump voltage-surge protection.

The maximum operating supply-voltage of the CA2002 is 18 V, and internal protection is provided for peaks of up to 40 V, as shown in Fig. 18. Supply-voltage peaks of more than 40 V will require an LC network between the supply and terminal 5. An LC network, such as the one shown in Fig. 18, provides protection against supply-voltage surges of up to 120 V for 2 ms. This type of protection is ON when the supply voltage (pulsed or dc exceeds 18 V).

Thermal shut-down occurs if the output overloads (temporary or permanent), the ambient temperature is excessive, or the junction temperature is excessive. None of these conditions results in device damage. They merely cause a temporary automatic reduction of output power and drain current, as shown in Figs. 16 and 17.

A heater fan motor run-down hysteresis circuit is included for automotive applications. Typical starting voltage is 10 volts; typical drop-out voltage is 6.5 volts.

The CA2002 is supplied in a 5-lead plastic TO-220-style VERSA-V package. All leads (except term. 3) are electrically insulated from the mounting flange, eliminating the need for insulating hardware. The VERSA-V package is available with two lead configurations. The CA2002 has a vertical-mount lead form, and the CA2002M has a horizontal-mount lead form.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

PEAK SUPPLY VOLTAGE (50 ms)	40 V
DC SUPPLY VOLTAGE	28 V
OPERATING SUPPLY VOLTAGE	18 V
OUTPUT PEAK CURRENT:	
REPETITIVE	3.5 A
NON-REPETITIVE	4.5 A
POWER DISSIPATION, P_D at $T_A = 90°C$	15 W
THERMAL RESISTANCE, JUNCTION TO CASE	4° C/W
AMBIENT-TEMPERATURE RANGE:	
OPERATING	**See Figures 16 & 17**
STORAGE	-40 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 12 s max.	260° C

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 14.4 V
Unless otherwise specified (See Figure 2)

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
			Min.	Typ.	Max.	
Supply Voltage, V^+			11	–	18	V
Quiescent Output Voltage, V_O	Measure at Term. 4		6.4	7.2	8	V
Quiescent Drain Current, I_D	Measure at Term. 5		–	45	80	mA
Output Power, P_O	THD = 10%, A = 40 dB, f = 1 KHz					
	V^+ = 14.4V	R_L = 4 Ω	4.8	5.2	–	W
		R_L = 2 Ω	7	8	–	
	V^+ = 16 V	R_L = 4 Ω	–	6.5	–	
		R_L = 2 Ω	–	10	–	
Input Saturation Voltage, $V_{I(RMS)}$			400	–	–	mV
Input Sensitivity, e_I	A = 40 dB, f = 1 KHz					
		P_O = 0.5 W, R_L = 4 Ω	–	15	–	mV
		P_O = 0.5 W, R_L = 2 Ω	–	11	–	
		P_O = 5.2 W, R_L = 4 Ω	–	55	–	
		P_O = 8 W, R_L = 2 Ω	–	50	–	
Frequency Response (−3 dB)	R_L = 4 Ω (See Fig. 19)			25000		Hz
Input Resistance, R_I (Term. 1)	f = 1 KHz		70	150	–	KΩ
Open-Loop Voltage Gain, A_{OL}	R_L = 4 Ω, f = 1 KHz		–	80	–	dB
Closed-Loop Voltage Gain, A	R_L = 4Ω, f = 1 KHz		39.5	40	40.5	dB
Input Noise Voltage, e_N	Freq. Resp. = 40 to 15,000 Hz (−3 dB)		400	4	–	μV
Input Noise Current, i_N	Freq. Resp. = 40 to 15,000 Hz (−3 dB)		–	60	–	pA
Efficiency, η	A = 40 dB, f = 1 KHz					
		P_O = 5.2 W, R_L = 4 Ω	–	68	–	%
		P_O = 8 W, R_L = 2 Ω	–	58	–	
Power Supply Rejection Ratio, PSRR	R_L = 4 Ω, A = 40 dB, Rg = 10 KΩ, f_{ripple} = 100 Hz, V_{ripple} = 0.5 V		30	35	–	dB

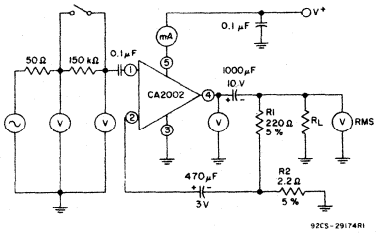


Fig. 1 – Test circuit.

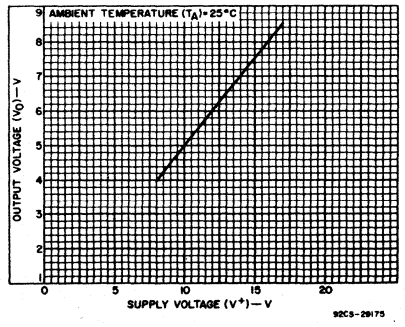


Fig. 2 – Typical quiescent output voltage as a function of supply voltage.

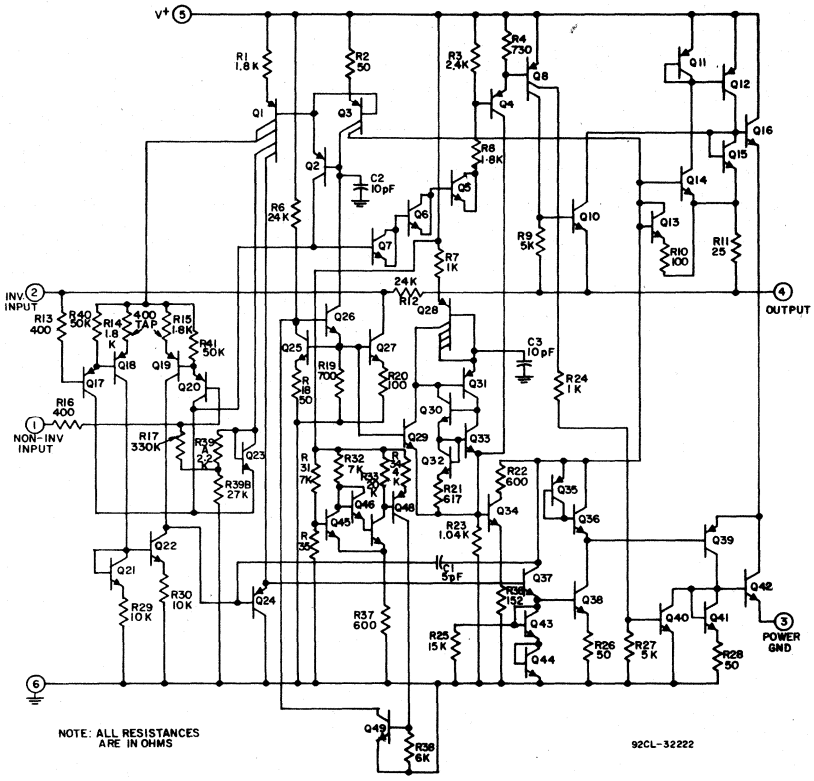


Fig. 3 – Schematic diagram.

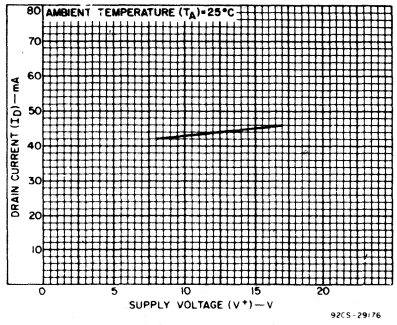


Fig. 4 – Typical quiescent drain current as a function of supply voltage.

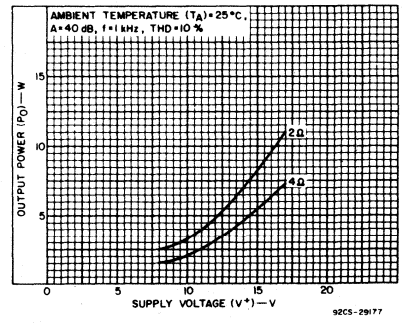


Fig. 5 – Typical output power as a function of supply voltage.

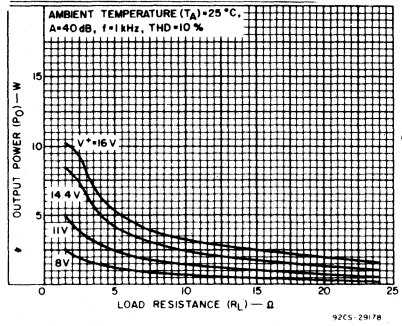


Fig. 6 – Typical output power as a function of load resistance.

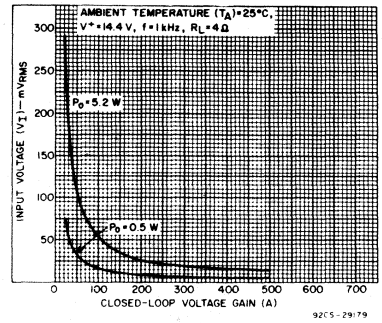


Fig. 7 – Typical input voltage as a function of closed-loop voltage gain.

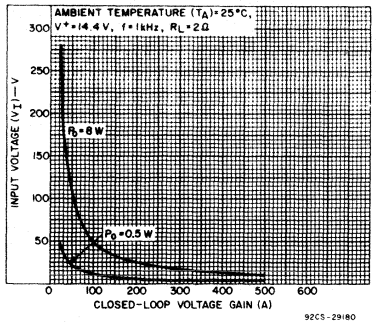


Fig. 8 — Typical input voltage as a function of closed-loop voltage gain.

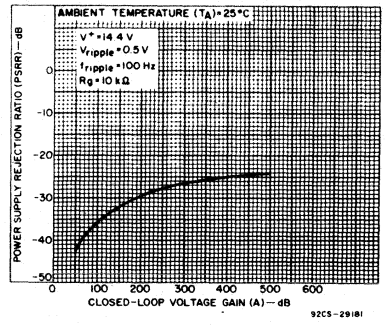


Fig. 9 — Typical power supply rejection ratio as a function of closed-loop voltage gain.

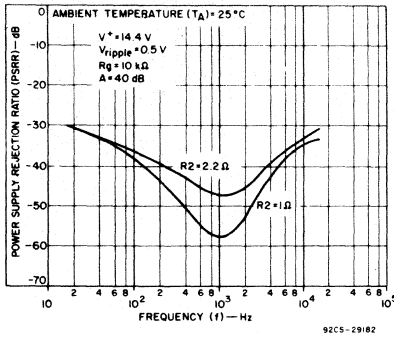


Fig. 10 — Typical power supply rejection ratio as a function of frequency.

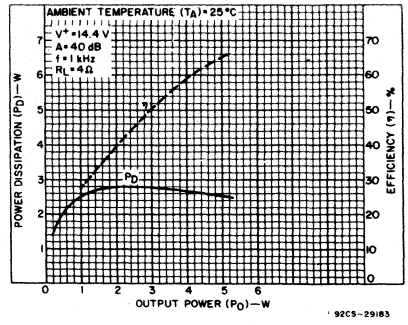


Fig. 11 — Typical power dissipation and efficiency as a function of output power.

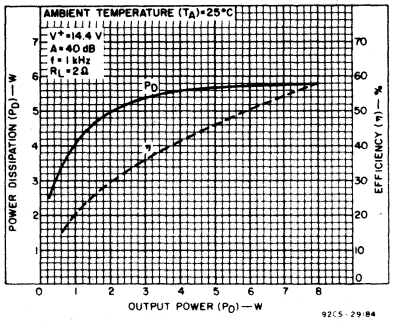


Fig. 12 — Typical power dissipation and efficiency as a function of output power.

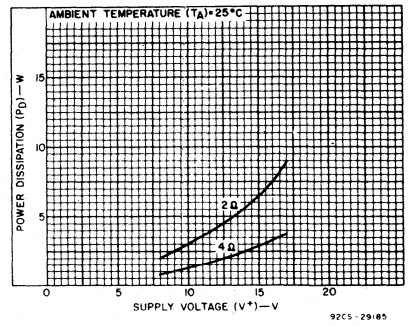


Fig. 13 — Maximum power dissipation as a function of supply voltage (sine-wave operation).

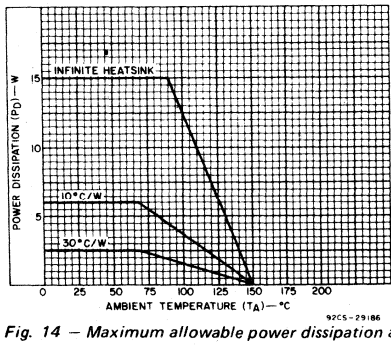


Fig. 14 — Maximum allowable power dissipation as a function of ambient temperature.

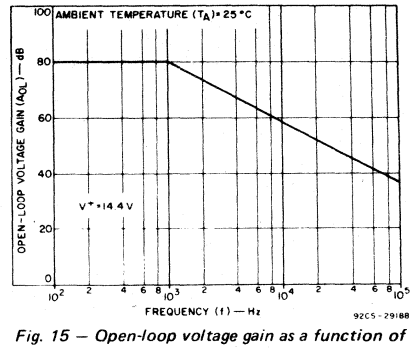


Fig. 15 — Open-loop voltage gain as a function of frequency.

Load-Dump Voltage-Surge Protection

The maximum operating supply-voltage of the CA2002 is 18 V, and internal protection is provided for peaks of up to 40 V, as shown in Fig. 18. Supply-voltage peaks of more than 40 V will require an LC network between the supply and terminal 5. An LC network, such as the one shown in Fig. 18, provides protection against supply-voltage surges of up to 120 V for 2 ms. This type of protection is ON when the supply voltage (pulsed or dc) exceeds 18 V.

Thermal Shut-Down

Thermal shut-down occurs if the output overloads (temporary or permanent), the ambient temperature is excessive, or the junction temperature is excessive. None of these conditions results in device damage. They merely cause a temporary automatic reduction of output power and drain current, as shown in Figs. 16 and 17.

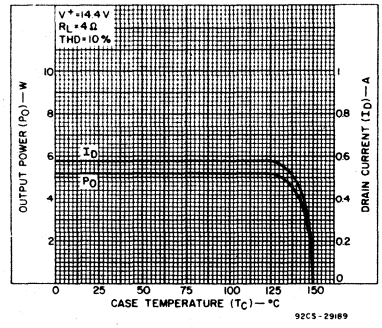


Fig. 16 – Output power and drain current as a function of case temperature.

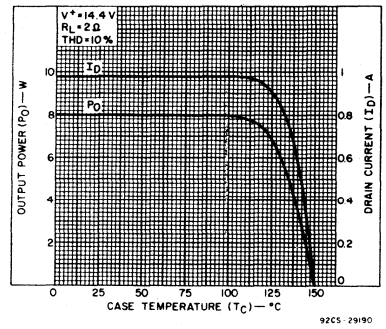


Fig. 17 – Output power and drain current as a function of case temperature.

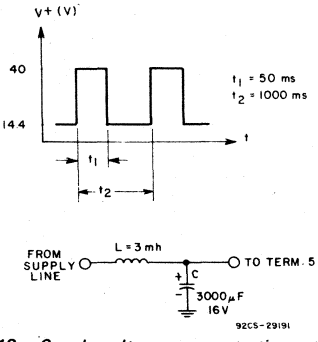


Fig. 18 – Supply-voltage surge protection network and timing diagram.

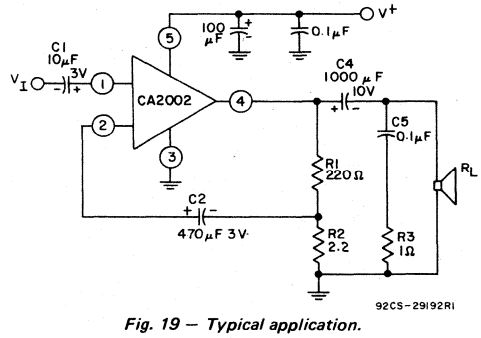


Fig. 19 – Typical application.

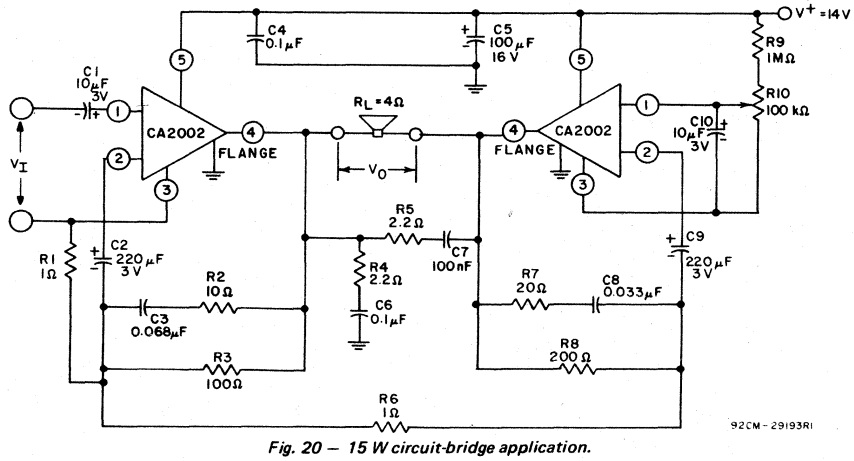
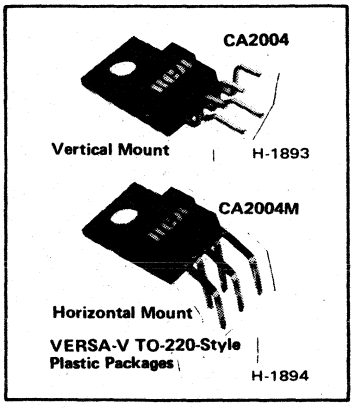


Fig. 20 – 15 W circuit-bridge application.

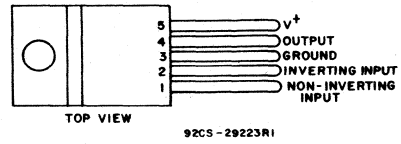


12-Watt Audio Power Amplifier

FEATURES:
- *VERSA-V 5-lead plastic TO-220-style package (insulation not required)*
- *Thermal overload protection*
- *Drives load impedance as low as 3.2Ω*
- *Deflection amplifier capability*
- *Output current capability of up to 3.5 A*
- *Few external components*

The RCA-CA2004 is a monolithic silicon class B audio power amplifier designed for driving loads as low as 3.2Ω. It provides a high output current capability (up to 3.5A), and very low harmonic and cross-over distortion.

The CA2004 is supplied in a 5-lead plastic TO-220-style VERSA-V package. All leads (except term. 3) are electrically insulated from the mounting flange, eliminating the need for insulating hardware. The VERSA-V package is available with two lead configurations. The CA2004 has a vertical-mount lead form, and the CA2004M has a horizontal-mount lead form.



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE	28 V
OPERATING SUPPLY VOLTAGE	26 V
OUTPUT PEAK CURRENT:	
REPETITIVE	3.5 A
NON-REPETITIVE	4.5 A
POWER DISSIPATION, P_D at T_A = 90°C	15 W
THERMAL RESISTANCE, JUNCTION TO CASE	4°C/W
AMBIENT-TEMPERATURE RANGE:	
OPERATING	0 to +125°C
STORAGE	-40 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 12 s max.	260°C

CA2004, CA2004M

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 24 V
Unless otherwise specified (See Figure 1)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Voltage, V^+		8	–	26	V
Quiescent Output Voltage, V_O	Measure at Term. 4	11	12	13	V
Quiescent Drain Current, I_D	Measure at Term. 5	–	40	100	mA
Output Power, P_O	THD = 10%, A = 40 dB, f = 1 KHz, R_L = 4 Ω	10	12	–	W
	THD = 10%, A = 40 dB, f = 1 KHz, R_L = 8 Ω	–	8	–	W
Input Saturation Voltage, $V_{I(RMS)}$		400	–	–	mV
Input Resistance, R_I (Term.1)	f = 1 KHz	70	150	–	KΩ
Open-Loop Voltage Gain, A_{OL}	R_L = 8 Ω, f = 1 KHz	–	80	–	dB
Closed-Loop Voltage Gain, A	R_L = 8 Ω, f = 1 KHz	39.5	40	40.5	dB
Input Noise Voltage, e_N	Freq. Resp. = 40 to 15,000 Hz (–3 dB)	–	4	–	μV
Power Supply Rejection Ratio, PSRR	R_L = 4 Ω, A = 40 dB, Rg = 10 KΩ, f_{ripple} = 100 Hz, V_{ripple} = 0.5 V	30	35	–	dB

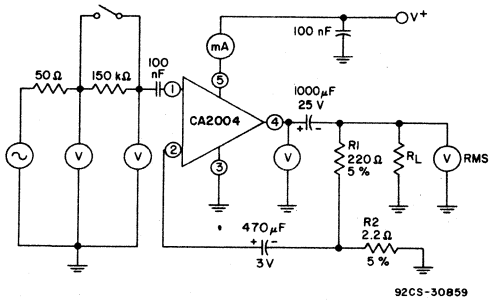


Fig. 1 – Test circuit.

Thermal Shut-Down

Thermal shut-down occurs if the output overloads (temporary or permanent), the ambient temperature is excessive, or the junction temperature is excessive. None of these conditions results in device damage. They merely cause a temporary automatic reduction of output power and drain current.

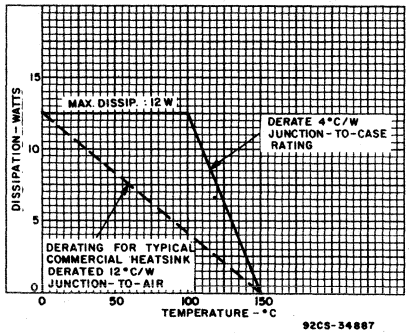


Fig. 2 —Derating curve

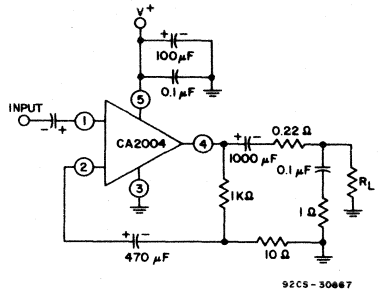


Fig. 3 — Typical application.

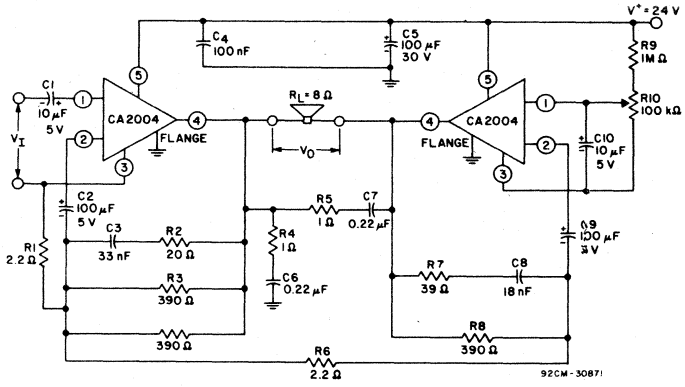


Fig. 4 — 25 W circuit-bridge application.

Radio Circuits
Technical Data

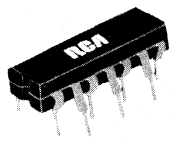
AM/FM Communications Circuits

FM IF Circuits

Gain Blocks

Subsystems

CA3075



14-lead dual-in-line plastic package, leads in quad-formed arrangement.

FM IF Amplifier - Limiter, Detector, and Audio Preamplifier

For FM IF Amplifier Applications Up To 20 MHz In Communications Receivers And High-Fidelity Receivers

Features:

- Good sensitivity: Input limiting voltage (knee) = 250 μV typ. at 10.7 MHz
- Excellent AM rejection: 55 dB typ. at 10.7 MHz
- Internal Zener diode regulation for the IF amplifier section
- Low harmonic distortion
- Differential peak detection: Permits simplified single-coil tuning
- Audio preamplifier voltage gain: 21 dB typ.
- Minimum number of external parts required

RCA CA3075 is an integrated circuit which provides, in a single monolithic chip, an FM IF subsystem for Communications and High-Fidelity Receivers. This device, shown in the schematic diagram (Fig. 2), consists of a multistage IF amplifier-limiter section with a Zener regulated power supply, an FM detector stage, and an AF preamplifier section. A typical application of the CA3075, in FM receiver circuits, is shown in the block diagram (Fig. 1).

The three-stage, emitter-follower-coupled IF amplifier section provides a 60-dB typ. voltage gain at an operating frequency of 10.7 MHz and features, because of its transistor constant-current sink, an output stage with exceptionally good limiting characteristics.

The FM detector section, which utilizes a differential-peak-detection circuit, requires only a single coil in the associated outboard detector circuit; hence, tuning the detector circuit is a simple procedure.

The audio preamplifier circuit provides a 21-dB voltage gain with low impedance output for driving subsequent audio amplifier stages.

The CA3075 utilizes a 14-lead dual-in-line plastic package with leads in a special quad-formed arrangement.

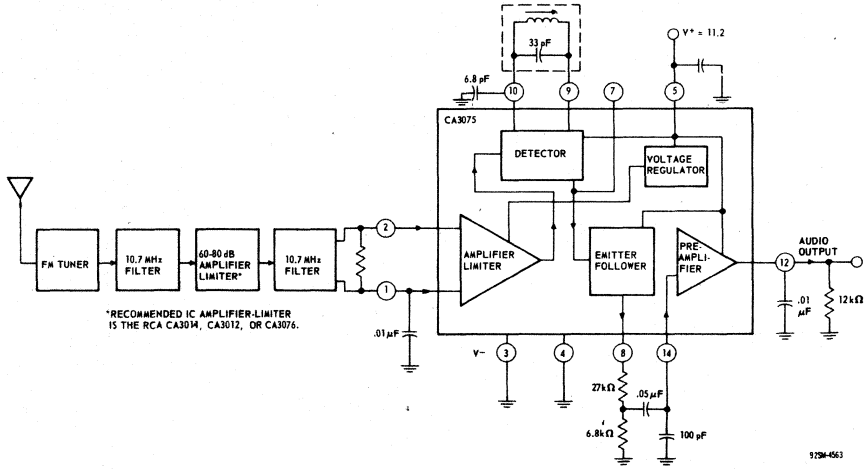


Fig. 1 - Block diagram of typical FM receiver utilizing the CA3075

MAXIMUM RATINGS, *Absolute-Maximum Values at* T_A = 25°C

DC Supply Voltage [between Terminals 5 (V^+) and 3 (V^-)]	12.5	V
DC Current (into Terminal 5)	30	mA
Device Dissipation:		
Up to T_A = 50°C	760	mW
Above T_A = 50°C	derate linearly 7.6	mW/°C
Ambient Temperature Range:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
Lead Temperature (During soldering for 10 s max.)	+260	°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CIRCUIT FIG. NO.
Static Characteristics							
DC Voltage:							
At Terminal 7	V_7	V^+ = 11.2 V	–	6.1	–	V	6
At Terminal 8	V_8		–	5.4	–	V	
At Terminal 12	V_{12}		–	5.2	–	V	
DC Current (into Terminal 5):							
At V^+ = 8.5 V	I_5	–	8.5	15	–	mA	6
At V^+ = 11.2 V			–	17.5	–	mA	
At V^+ = 12.5 V			–	19	29	mA	
Dynamic Characteristics at V^+ = 11.2							
IF AMPLIFIER Input Limiting Voltage (knee, − 3 dB point)	V_I(lim)	f_0 = 10.7 MHz f(Modulation) = 400 Hz Deviation = ±75 kHz	–	250	600	μV	3
AM Rejection	AMR	f_0 = 10.7 MHz f(Modulation) = 400 Hz FM: Deviation = ±75 kHz AM: Modulation = 30%	–	55	–	dB	5
Input Impedance Components:							–
Parallel Resistance	R_I	f_0 = 10.7 MHz	–	4.5	–	kΩ	
Parallel Capacitance	C_I	V_{IN} = 10 mV RMS	–	4.5	–	pF	
DETECTOR							3
Recovered AF Voltage (at Terminal 12)	V_O(AF)	f_0 = 10.7 MHz f(Modulation) = 400 Hz	–	1.5	–	V	
Total Harmonic Distortion	THD	Deviation = ± 75 kHz	–	1	2	%	
AUDIO PREAMPLIFIER							
Voltage Gain	A(AF)	V_{IN} = 100 mV, f_0 = 400 Hz	–	21	–	dB	4
Total Harmonic Distortion	THD	V_{OUT} = 2 V, f_0 = 400 Hz	–	1.5	5	%	4

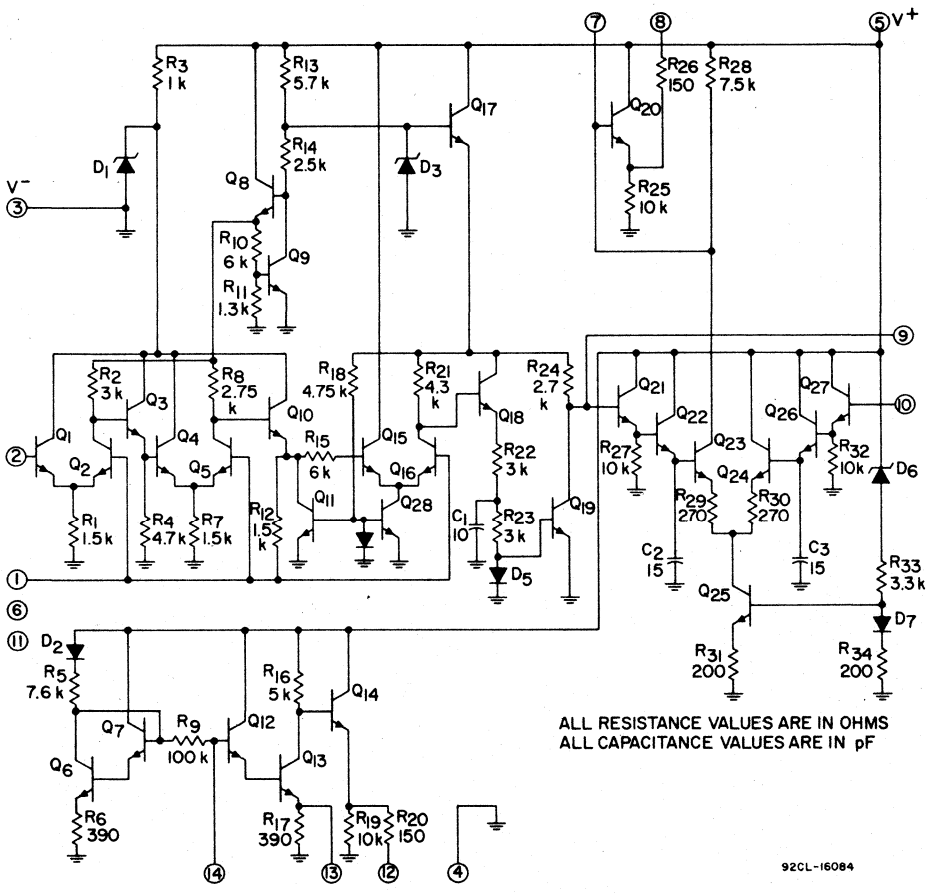


Fig. 2 - Schematic diagram of CA3075

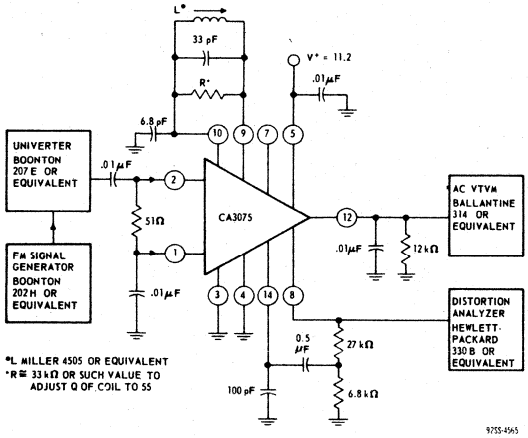


Fig. 3 - Test circuit for input limiting voltage, recovered AF voltage, and total harmonic distortion

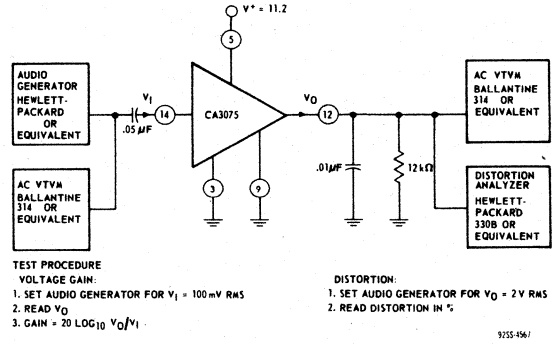


Fig. 4 - Test circuit for audio preamplifier voltage gain and total harmonic distortion

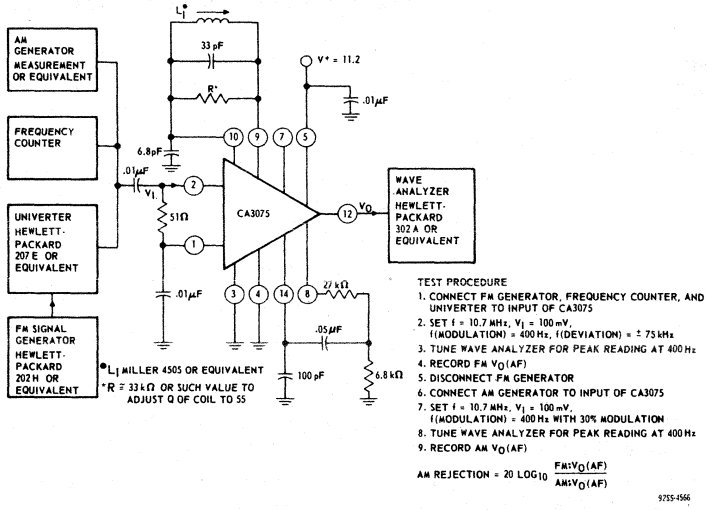


Fig. 5 - Test circuit for AM rejection

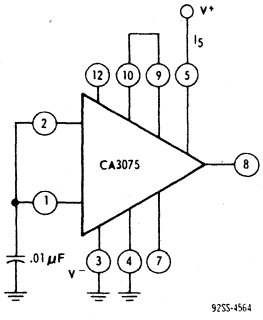
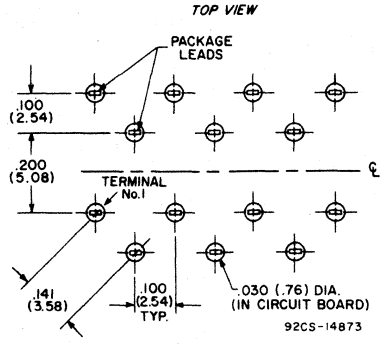


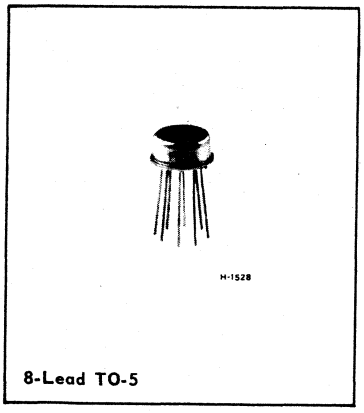
Fig. 6 - Test circuit for static characteristics

Recommended Mounting-Hole Dimensions and Spacings.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.

CA3076



High-Gain Wide-Band IF Amplifier-Limiter

For FM IF Amplifier Applications in Communications Receivers

Features:

- exceptionally good sensitivity: input limiting voltage (knee) = 50 μV typ. at 10.7 MHz
- high gain: 80 dB with 2-kilohm load
- internal voltage supply regulator
- wide frequency capability: > 20 MHz

RCA CA3076, monolithic integrated circuit, is a high-gain wide-band amplifier-limiter for use in the IF sections of Communications and High-Fidelity FM Receivers. The CA3076, shown in the schematic diagram (Fig. 2), consists of a four stage IF amplifier-limiter section with a voltage regulator section. A typical application of the CA3076 in FM receiver circuits is shown in the block diagram (Fig. 1).

The four-stage emitter-follower-coupled IF amplifier section provides an 80-dB voltage gain with a 2-kilohm load at a frequency of 10.7 MHz. The output stage has exceptionally good limiting characteristics because of its transistor constant-current sink. The voltage regulator section provides zener-regulated, decoupled voltages for the IF amplifier.

The CA3076 utilizes an hermetically-sealed 8-lead TO- package.

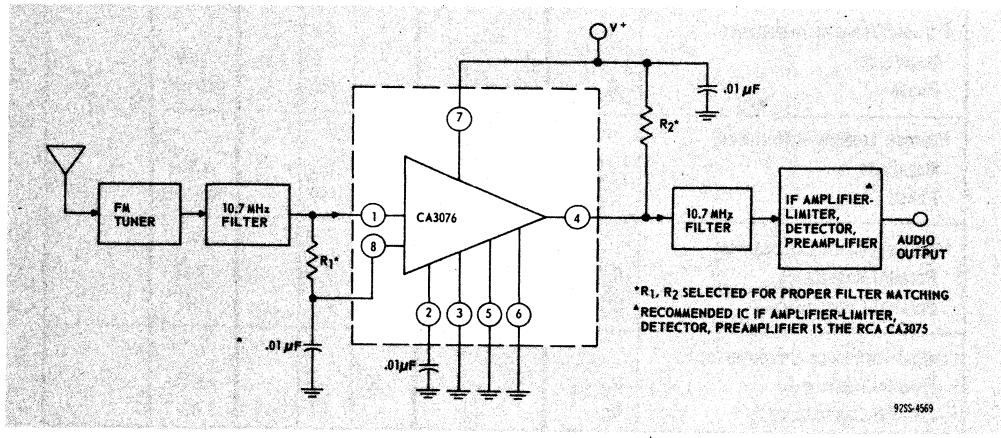


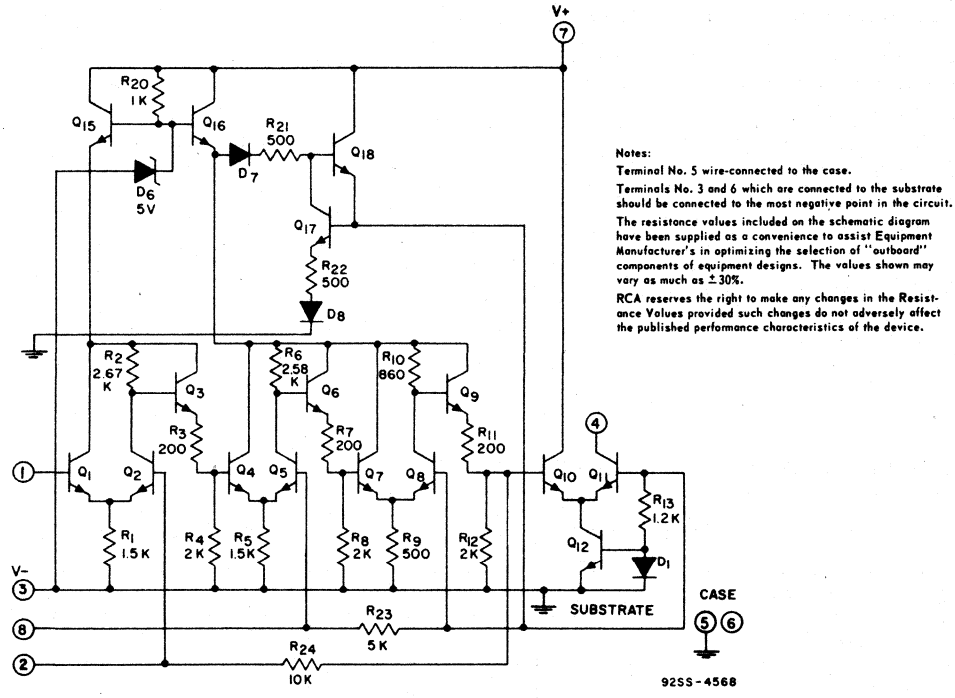
Fig. 1 - Block diagram of typical FM receiver utilizing the CA3076.

MAXIMUM RATINGS, *Absolute Maximum-Values at* T_A = 25°C

DC Supply Voltage [between Terminals 7 (V^+) and 3 (V^-)]	15	V
DC Current (into Terminal 7)	35	mA
Device Dissipation:		
Up to T_A = 50°C	500	mW
Above T_A = 50°C	derate linearly 5	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/32 in (3.17 mm) from seating plane for 10 s max	+260	°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	TEST CIRCUIT FIG. NO.
			MIN.	TYP.	MAX.		
Static Characteristics – V^+ = 8.5 V							
DC Current (into Term. 7)	I_7	–	10	15	24	mA	3
Quiescent Operating Current (into Term. 4)	I_4	–	–	0.65	–	mA	3
Dynamic Characteristics – V^+ = 8.5 V, f_O = 10.7 MHz							
Input Limiting Voltage (knee, −3 dB point)	V_I (lim.)	–	–	50	200	μV	–
Output Voltage	V_O	V_I = 20 μV	4	12	–	mV	5
Output Noise Voltage	V_N	V_I = 0	–	1	–	mV	5
Forward Transfer Admittance:							
Magnitude	$\lvert Y_{21} \rvert$	V_I =	–	6	–	mho	4
Phase	θ_{21}	10 μV	–	80	–	degrees	
Reverse Transfer Admittance:							
Magnitude	$\lvert Y_{12} \rvert$	–	–	0.1	–	μmho	–
Phase	θ_{12}		–	−90	–	degrees	
Input-Impedance Components:							
Parallel Resistance	R_I	–	–	7.5	–	kΩ	–
Parallel Capacitance	C_I		–	4	–	pF	
Output-Impedance Components:							
Parallel Resistance	R_O	–	50	–	–	kΩ	–
Parallel Capacitance	C_O		–	1.7	–	pF	



Notes:

Terminal No. 5 wire-connected to the case.

Terminals No. 3 and 6 which are connected to the substrate should be connected to the most negative point in the circuit.

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturer's in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

Fig. 2 - Schematic diagram of CA3076.

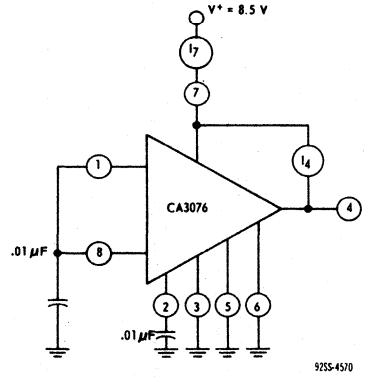


Fig. 3 - Test circuit for DC current (Terminal 7) and operating current (Terminal 4).

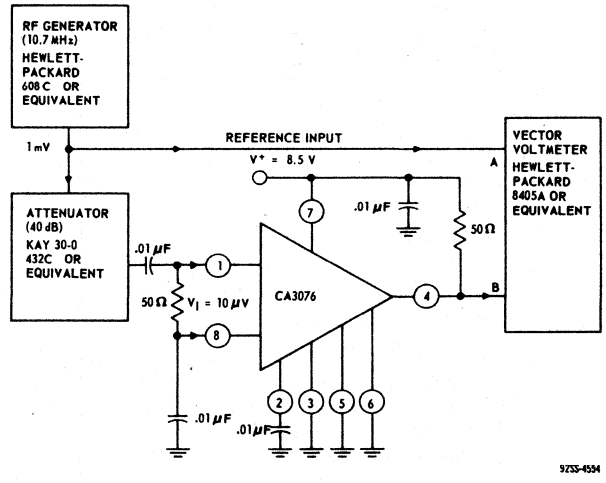
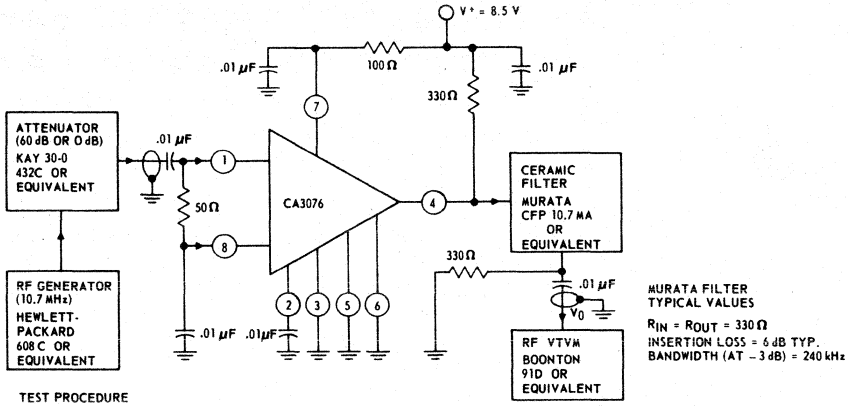


Fig. 4 - Forward transfer admittance (Y_{21}) test circuit



TEST PROCEDURE

OUTPUT VOLTAGE:

1. SET ATTENUATOR TO 0 dB
2. SET RF GENERATOR TO 20 μV CW
3. READ V_0 IN mV

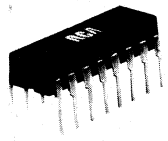
OUTPUT NOISE VOLTAGE:

1. SET ATTENUATOR TO 60 dB
2. READ V_0 IN mV

92SS-4571

Fig. 5 - 10.7 MHz voltage gain and noise test circuit

CA3088E



H-1622

16-Lead Dual-In-Line Plastic Package

AM Receiver Subsystem and General-Purpose Amplifier Array

Includes: AM Converter, IF Amplifiers, Detector and Audio Preamplifier

For Applications in a Variety of AM Broadcast and Communications Receivers and Applications Requiring an Array of Amplifiers

Features:

- **Excellent overload characteristics**
- **AGC for IF amplifier**
- **Buffered output signal for tuning meter**
- **Low harmonic distortion (THD)**
- **Delayed AGC for RF amplifier**
- **Terminals for optional inclusion of tone control**
- **Internal Zener diode provides voltage regulation**
- **Two IF amplifier stages**
- **Low-noise converter and first IF amplifier**
- **Operates from wide range of power supplies: V^+ = 6 to 16 volts**
- **Optional AC and/or DC feedback on wide-band amplifier**
- **Array of amplifiers for general-purpose applications**
- **Suitable for use with optional external RF stage, either MOS or bipolar**

RCA-CA3088E*, a monolithic integrated circuit, is an AM subsystem that provides the converter, IF amplifier, detector, and audio preamplifier stages for an AM receiver.

The CA3088E also provides internal AGC for the first IF amplifier stage, delayed AGC for an optional external RF amplifier, a buffer stage to drive a tuning meter, and terminals facilitating the optional use of a tone control.

Fig. 2 is a functional diagram of the CA3088E. The signal from the low-noise converter is applied to the first IF amplifier and is then coupled to the second IF amplifier. This IF signal is then detected and externally filtered. The resultant audio signal is applied to an audio preamplifier. Optionally, a tone control circuit may be connected at the junction of the detector circuit and the audio preamplifier. The gain of the first IF amplifier stage is controlled by an internal AGC circuit. The CA3088E supplies a delayed AGC signal output for use with an external RF amplifier. A buffered output signal is also available for driving a tuning meter. A DC voltage, internally regulated by a Zener diode, supplies the second IF amplifier, the AGC and tuning meter circuits and may also be used with any other stage.

The CA3088E features four independent transistor amplifiers, each incorporating internal biasing for temperature tracking. These amplifiers are particularly useful in general-purpose amplifier, oscillator, and detector applications in a wide variety of equipment designs.

The CA3088E utilizes a 16-lead dual-in-line plastic package and operates over an ambient temperature range of −40°C to +85°C.

*Formerly Developmental Type TA5842.

MAXIMUM RATINGS, *Absolute Maximum Values, at T_A = 25°C*

DC SUPPLY VOLTAGE:		
Across Term. 5 and Terms. 3, 6, 13, 16, respectively	16	V
DC CURRENT:		
At Terms. 3, 6, 13, 16, respectively	10	mA
At Term. 10	30	mA
DEVICE DISSIPATION:		
Up to T_A = 50°C	760	mW
Above T_A = 50°C	derate linearly 7.6	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V^+ = 12 V.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
			TEST CIRCUIT FIG. NO.		
Static (DC) Characteristics					
DC Voltages:					
Terms. 1, 4, 9, 11	$V_{1, 4, 9, 11}$		1	0.7	V
Terms. 2, 7, 8	$V_{2, 7, 8}$			1.4	V
Term. 10	V_{10}			5.6	V
Term. 12	V_{12}			0	V
Term. 15	V_{15}			3.5	V
DC Current:					
Term. 3	I_3		1	0.35	mA
Term. 6	I_6			1.0	mA
Term. 10	I_{10}			20	mA
Term. 13	I_{13}			0	mA
Term. 16	I_{16}			1.2	mA
Dynamic Characteristics					
Detector Output		30% Modulation	4	75	mV RMS
Audio Amplifier Gain	A_{AF}	f = 1 kHz	4	30	dB
Audio Distortion		V_{OUT} = 100 mV	4	0.2	%
Sensitivity:		f_{IN} = 1 MHz			
At Converter Stage Input		Signal-to-Noise Ratio (S/N) = 20 dB	2	200	μV/m
At RF Stage Input			4	100	μV/m
Total Harmonic Distortion	THD	30% Modulation	4	1.0	%
Input Resistance:	R_{IN}				
At Transistor Q1				3500	Ω
At Transistor Q5		No AGC,		2000	Ω
Input Capacitance:	C_{IN}				
At Transistor Q1		Input signal frequency		17	pF
At Transistor Q5		(f_{IN}) = 1 MHz		12	pF
Feedback Capacitance:	C_{FB}				
At Transistor Q1				1.5	pF
At Transistor Q5				1.5	pF

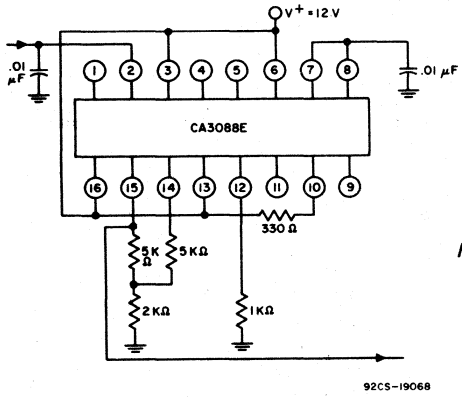


Fig.1—Test circuit for DC characteristics.

CA3088E

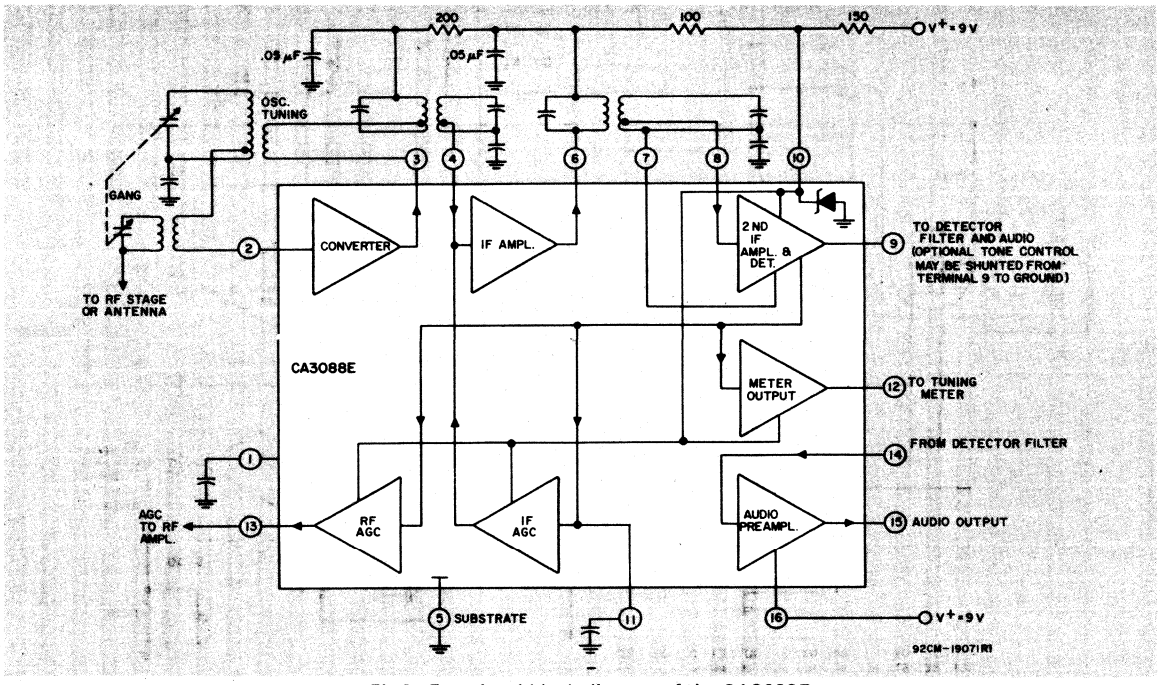


Fig.2—Functional block diagram of the CA3088E.

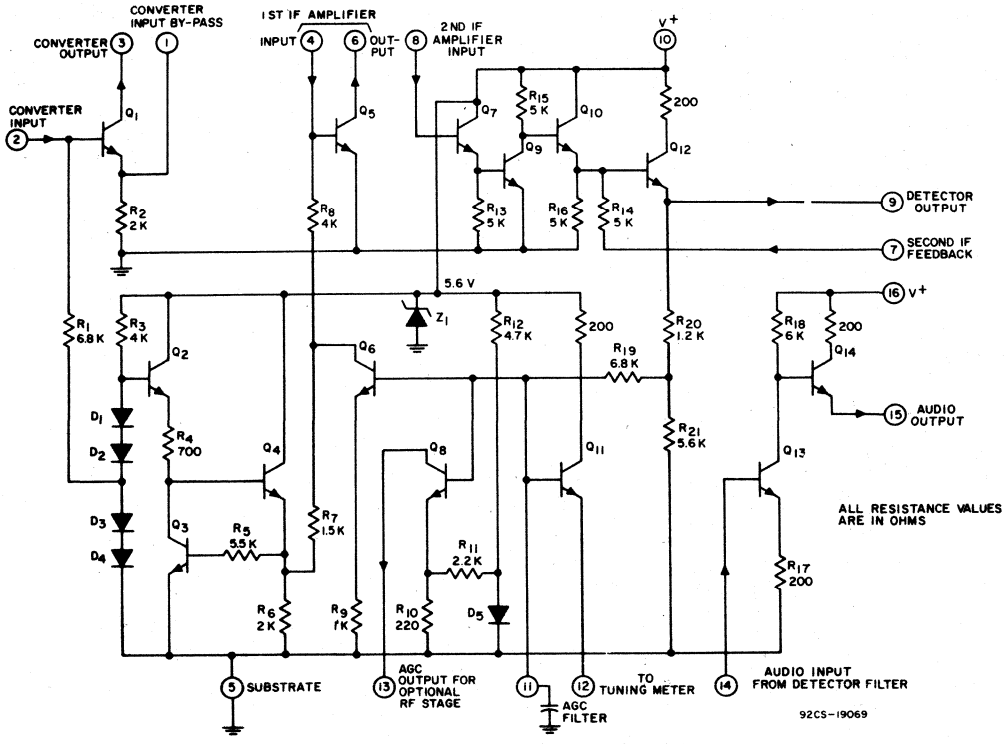


Fig.3—Schematic diagram of the CA3088E.

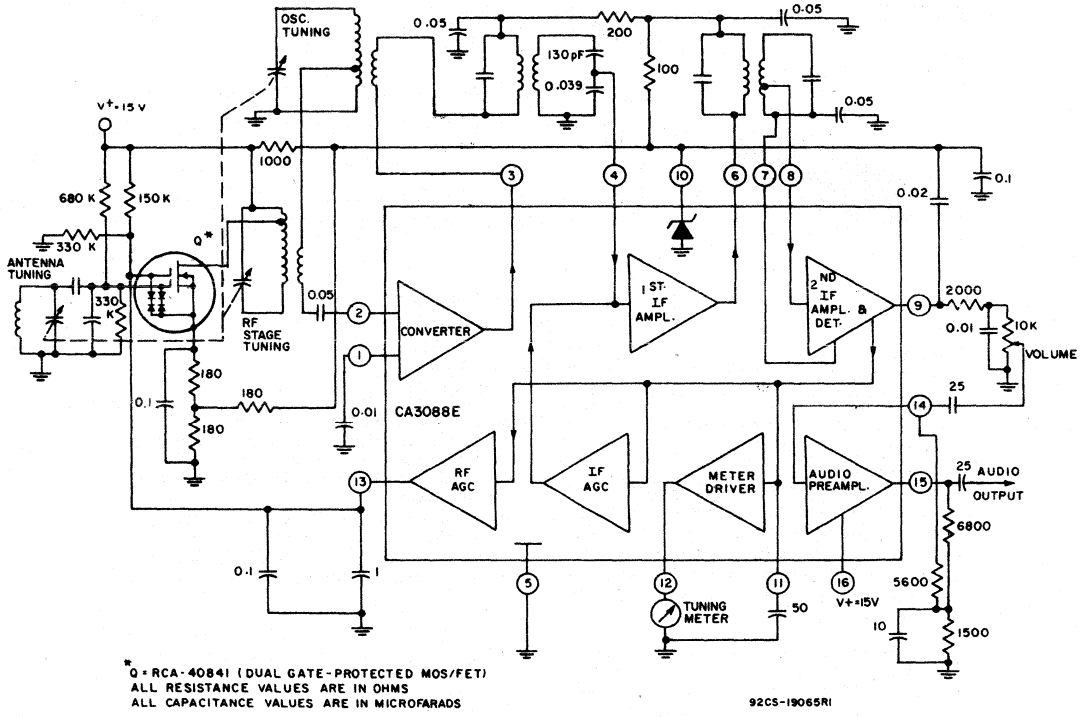
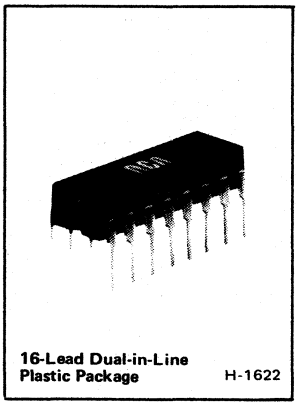


Fig.4—Typical AM broadcast receiver using the CA3088E with optional RF amplifier stage.

CA3089E



16-Lead Dual-in-Line Plastic Package H-1622

FM IF System

For FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers

Includes———IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Muting (Squelch), and Tuning Meter

Features:

- **Exceptional limiting sensitivity: 12 μV typ. at −3 dB point**
- **Low distortion: 0.1% typ. (with double-tuned coil)**
- **Single-coil tuning capability**
- **High recovered audio: 400 mV typ.**
- **Provides specific signal for control of inter-channel muting (squelch)**
- **Provides specific signal for direct drive of a tuning meter**
- **Provides delayed AGC voltage for RF amplifier**
- **Provides a specific circuit for flexible AFC**
- **Internal supply-voltage regulators**

RCA-CA3089E is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Fig. 1 is a block diagram showing the CA3089E features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as delayed AGC for the RF tuner, and AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5 to +16 volts.

The CA3089E is ideal for high-fidelity operation. Distortion in a CA3089E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089E utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of −40°C to +85°C.

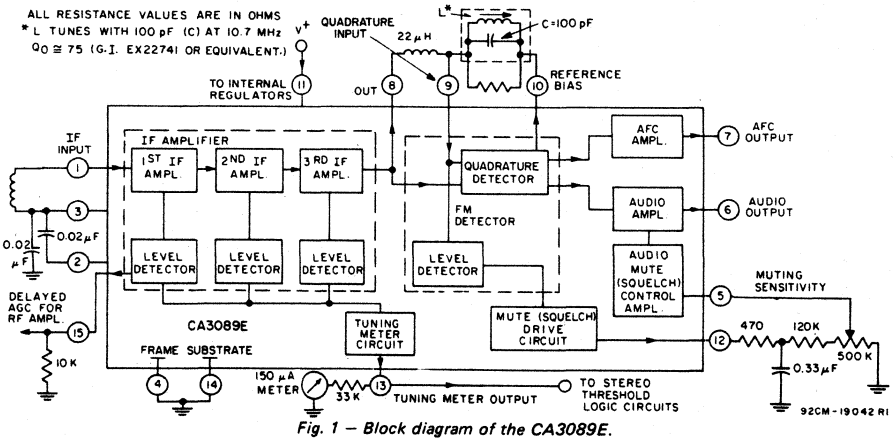


Fig. 1 – Block diagram of the CA3089E.

MAXIMUM RATINGS, *Absolute Maximum Values*

DC Supply Voltage:			
Between Terminals 11 and 4		16	V
Between Terminals 11 and 14		16	V
DC Current (out of Terminal 15)		2	mA
Device Dissipation:			
Up to $T_A = 60^\circ C$		600	mW
Above $T_A = 60^\circ C$	derate linearly	6.7	mW/°C
Ambient Temperature Range:			
Operating		−40 to + 85	°C
Storage		−65 to +150	°C
Lead Temperature (During Soldering):			
At distance not less than 1/32" (0.79mm) from case for 10 seconds max.		+265	°C

ELECTRICAL CHARACTERISTICS, at $T_A = 25^\circ C$, V+ = 12 Volts (See Figs. 5 and 6)

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
			Min.	Typ.	Max.	
Static (DC) Characteristics						
Quiescent Circuit Current	No signal input, Non muted		16	23	30	mA
DC Voltages:						
Terminal 1 (IF Input)			1.2	1.9	2.4	V
Terminal 2 (AC Return to Input)			1.2	1.9	2.4	V
Terminal 3 (DC Bias to Input)			1.2	1.9	2.4	V
Terminal 6 (Audio Output)			5.0	5.6	6.0	V
Terminal 10 (DC Reference)			5.0	5.6	6.0	V
Dynamic Characteristics						
Input Limiting Voltage (−3 dB point), V_1 (lim)	–	f_O = 10.7 MHz, $f_{mod.}$ = 400 Hz, Deviation = ±75 kHz	–	12	25	μV
AM Rejection (Term. 6), AMR	V_{IN} = 0.1V, AM Mod. = 30%		45	55	–	dB
Recovered AF Voltage (Term. 6) V_O (AF)	V_{IN} = 0.1 V		300	400	500	mV
Total Harmonic Distortion, THD:*						
Single Tuned (Term. 6)			–	0.5	1.0	%
Double Tuned (Term. 6)			–	0.1	–	%
Signal plus Noise to Noise Ratio (Term. 6)			60	67	–	dB

*THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8,9, and 10.

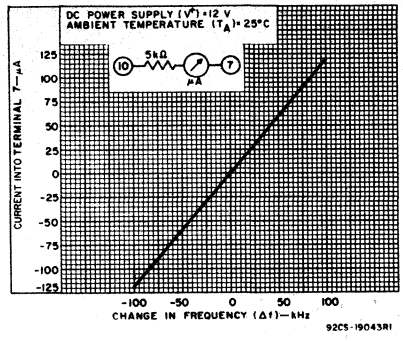


Fig. 2 — AFC characteristics (current at Term.7) as a function of change in frequency. (See test circuit Fig. 5.)

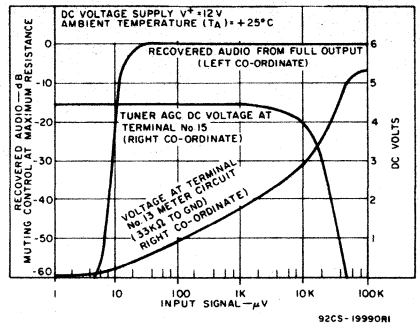


Fig. 3 — Muting action, tuner AGC, and tuning meter output as a function of input signal voltage. (See test circuit Fig.5.)

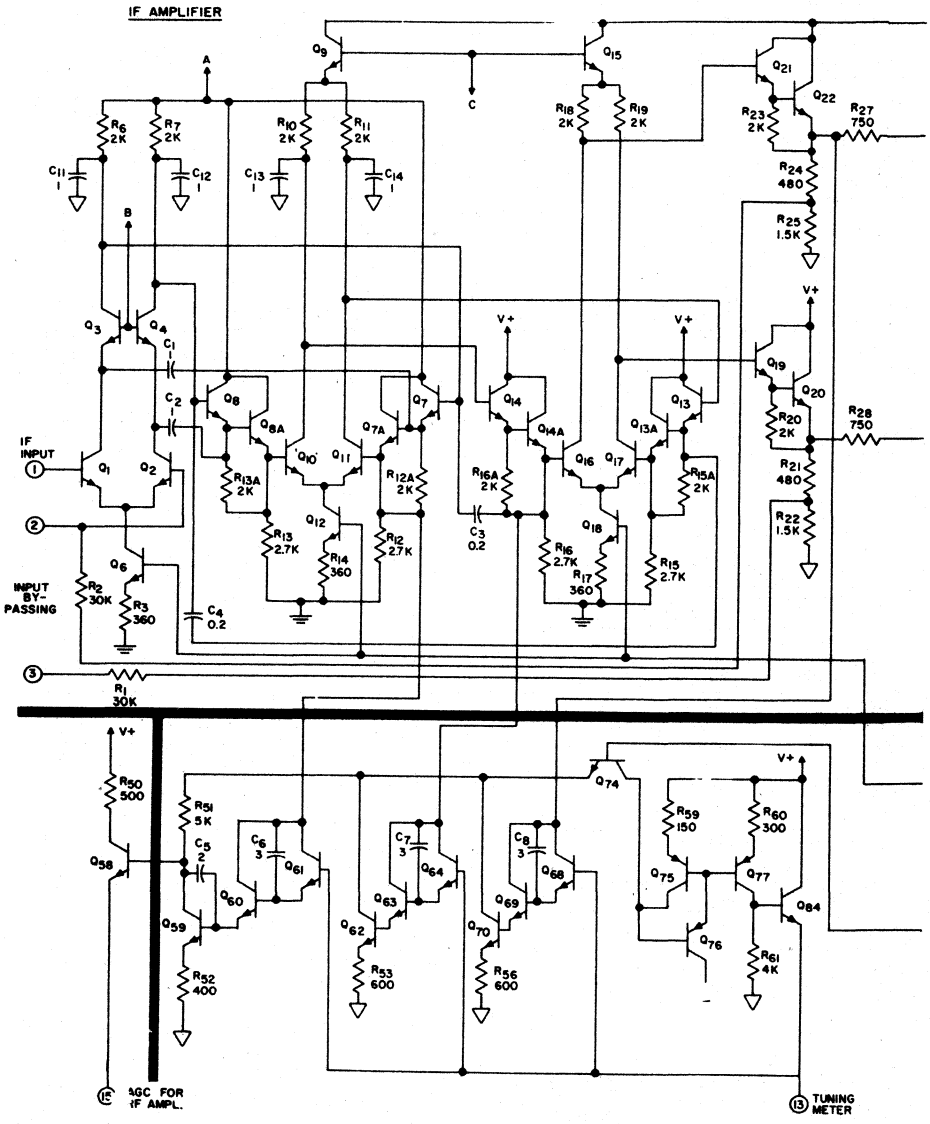


Fig. 4 – Schematic diagram of the CA3089E (cont'd on next page).

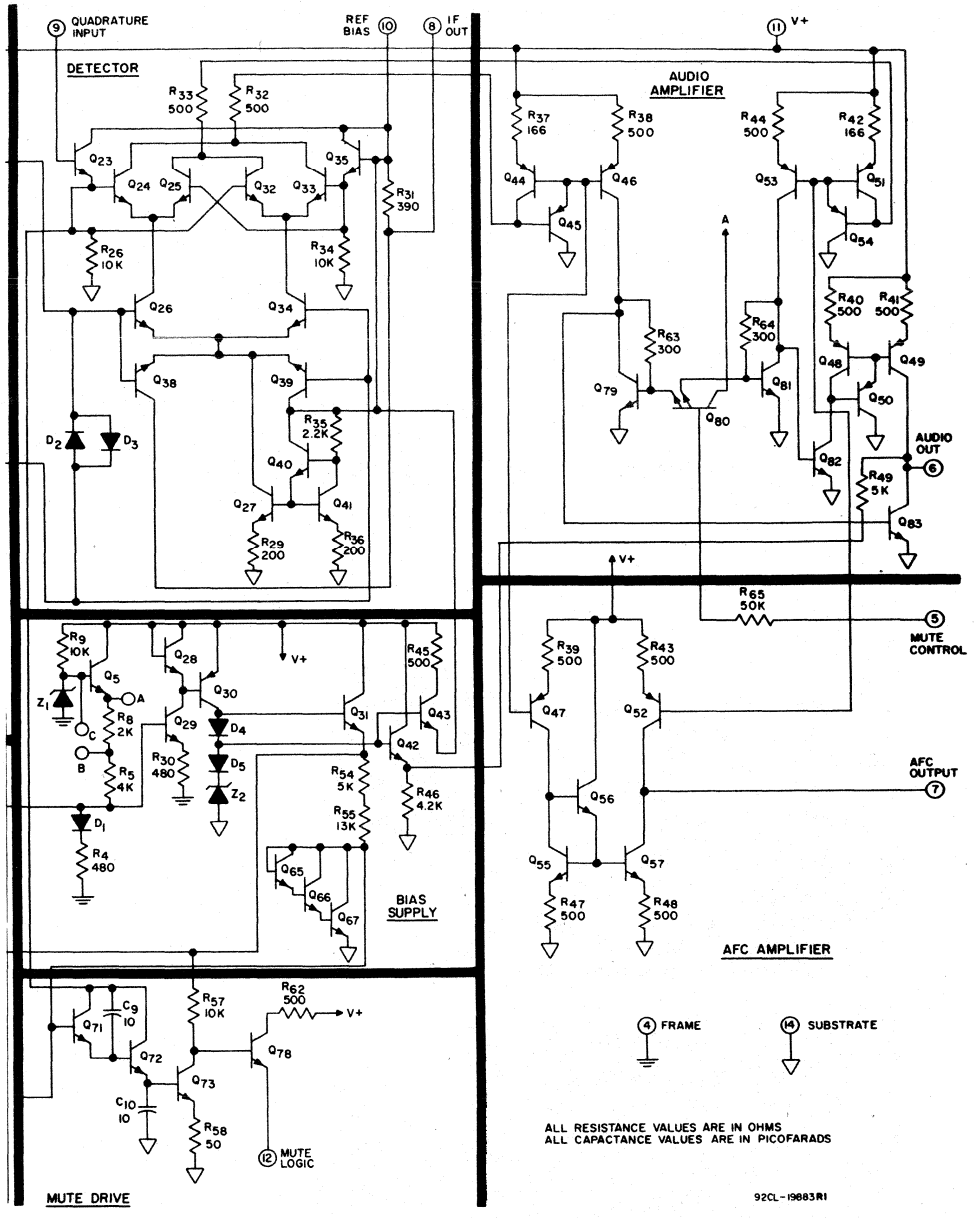
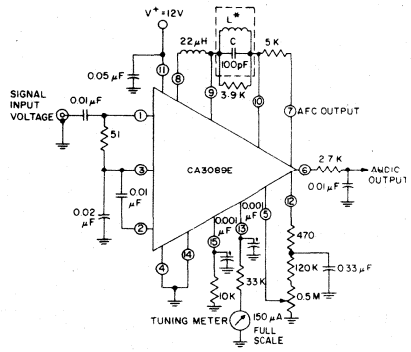


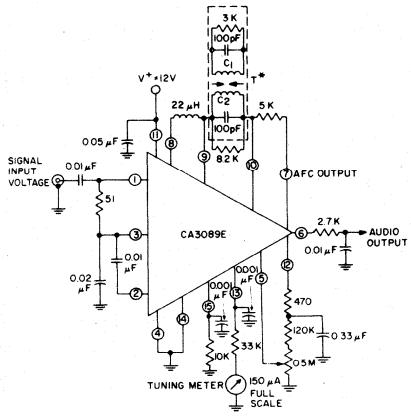
Fig. 4 - Schematic diagram of the CA3089E (cont'd from previous page).



ALL RESISTANCE VALUES ARE IN OHMS
*L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_0(UNLOADED) ≅ 75 (G.I. AUTOMATIC MFG. DIV. EX22741 OR EQUIVALENT)

92CM-19043-1

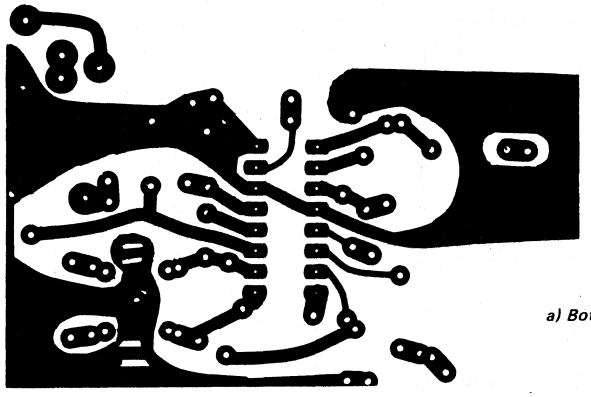
Fig. 5 — Test circuit for CA3089E using a single-tuned detector coil.



ALL RESISTANCE VALUES ARE IN OHMS
* T PRI. - Q_0(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C1) 20 t OF 34e ON 7/32" DIA FORM
SEC. - Q_0(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C2) 20 t OF 34e ON 7/32" DIA FORM
kQ (PER CENT OF CRITICAL COUPLING) ≅ 70%
(ADJUSTED FOR COIL VOLTAGE V_C) = 150 mV
ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT
"E" TYPE SLUGS, SPACING 4 mm

92CM-19044-1

Fig. 6 — Test circuit for CA3089E using a double-tuned detector coil.

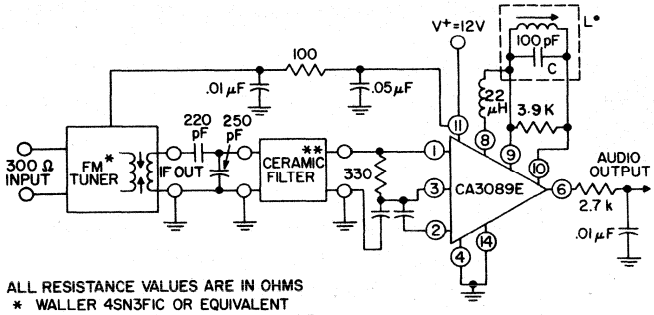


a) Bottom view of printed-circuit board.

b) Component side — top view.

92CS-30376

Fig. 7 - Actual size photographs of the CA3089E and outboard components mounted on a printed-circuit board.



ALL RESISTANCE VALUES ARE IN OHMS
* WALLER 4SN3FIC OR EQUIVALENT
** MURATA SFG 10.7 MA OR EQUIVALENT
• L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_O UNLOADED ≠75 (G.I EX22741 OR EQUIVALENT)

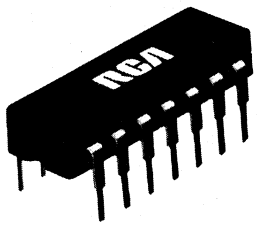
92CS-19045

Performance data at f_o = 98 MHz, f_{MOD} = 400 Hz, Deviation = ±75 kHz:

-3dB Limiting Sensitivity	2μV (Antenna Level)
20dB Quieting Sensitivity	1μV (Antenna Level)
30dB Quieting Sensitivity	1.5μV (Antenna Level)

Fig. 8 – Typical FM tuner using the CA3089E with a single-tuned detector coil.

CA3123E



14-Lead Dual-in-Line Plastic Package

H-1517

AM Radio Receiver Subsystem

Includes RF Amplifier, IF Amplifier, Mixer, Oscillator, AGC Detector, and Voltage Regulator

Features:

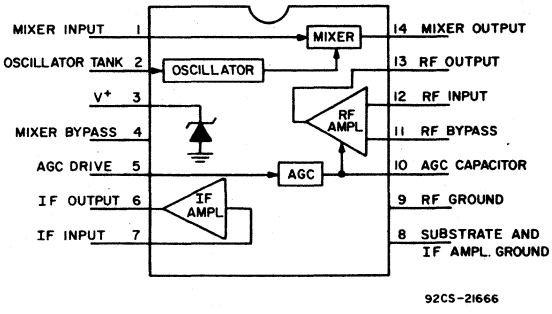
- **Low-noise, low-R_b' rf stage in cascode connection — eliminates Miller-Effect regeneration and allows controlled power rise by the choice of external components**
- **Mixer-oscillator stage with internal feedback — eliminates need for tapped or multi-winding oscillator coils**
- **Cascode if amplifier with controlled output impedance and negligible Miller Effect — eliminates regeneration and selectivity skewing**
- **Frequency-counter AGC circuit — allows control of AGC response by selection of the coupling capacitor**
- **Integral regulation with built-in surge protection**
- **Separately accessible amplifiers**

The CA3123E* is a monolithic silicon integrated circuit that provides an rf amplifier, if amplifier, mixer, oscillator, AGC detector, and voltage regulator on a single chip. It is intended for use in super-heterodyne AM radio receiver applications particularly in automobiles. The CA3123E is supplied in a 14-lead dual-in-line plastic package and operates over the temperature range of −55° to 125°C.

* Formerly RCA Dev. No. TA6155

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:	
At Terminal No. 3 (V^+)	9 V
At Terminal No. 6 (IF Output)	40 V
At Terminal No. 13 (RF Output)	20 V
At Terminal No. 14 (Mixer Output)	20 V
DC CURRENT:	
Into Terminal No. 3 (V^+)	35 mA
DEVICE DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16" ± 1/3" (1.59 mm ± 0.79 mm) from case for 10 s max.	265°C



Terminal assignment diagram.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Static Characteristics In Circuit of Fig. 3						
DC Voltage:						
At Terminals 1, 4	V_1, V_4			4.7		V
At Terminals 2, 3, 14	V_2, V_3, V_{14}			6.8		V
At Terminal 5	V_5			0.25		V
At Terminal 6	V_6			12		V
At Terminal 7	V_7			0.76		V
At Terminals 8, 9	V_8, V_9			0		V
At Terminals 10, 11	V_{10}, V_{11}			0.71		V
At Terminal 12	V_{12}			0.71		V
At Terminal 13	V_{13}			4.0		V
DC Current:						
Into Terminals 1, 4, 5, 7 8, 9, 10, 11, 12	$I_1, I_4, I_5, I_7, I_8, I_9, I_{10}, I_{11}, I_{12}$			0		mA
Into Terminal 2	I_2			1.2		mA
Into Terminal 3	I_3			15		mA
Into Terminal 6	I_6			4.3		mA
Into Terminal 13	I_{13}			4.5		mA
Into Terminal 14	I_{14}			0.170		mA
Performance Characteristics In Circuit of Fig. 3						
Sensitivity		Input Signal to Dummy Antenna at f_{IN}=1 MHz, 30% AM Modulation at f_{MOD}=400 Hz, for 11 mV output at V_O	–	2.3	5	μV
Signal-to-Noise Ratio	S/N	Ratio of Output at V_O with Modulation ON and then OFF, Input Signal=100 μV, 30% AM Modulation at f_{MOD}=400 Hz	34	43	–	dB
Overload Distortion		Input Signal set at 1 MHz, 90% AM Modulation, Distortion at V_O must be $\leq$ 10%	160000	400000	–	μV

Dynamic Characteristics For Indicated Stages In Circuit of Fig. 3

Stage	Parallel Capacitance		Parallel Resistance		Transconductance
	Input pF	Output pF	Input Ω	Output Ω	μmhos
RF Amplifier	80	6	750	2 x 10^6 min.	140000
IF Amplifier	35	3.5	950	10^4	80000
Mixer	6	2	2000	2 x 10^6 min.	2500 (Mixer) 3000 (Amplifier)

CA3123E

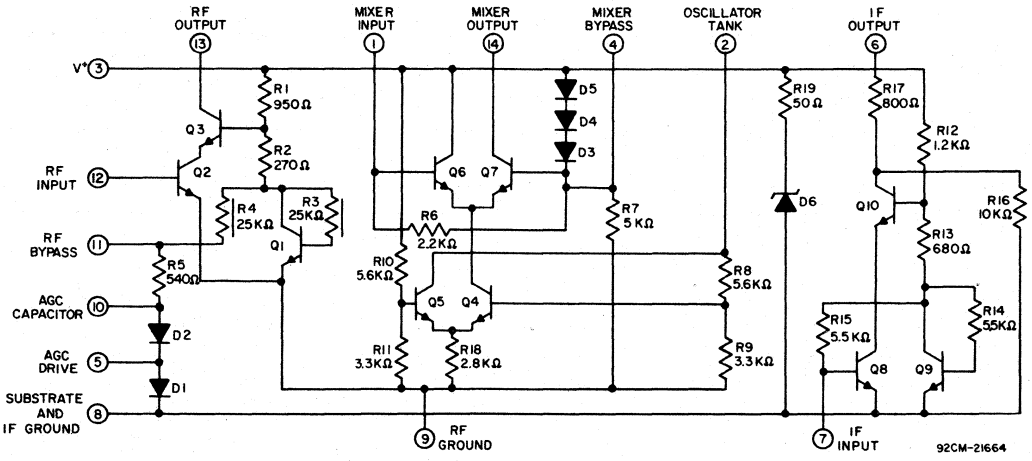
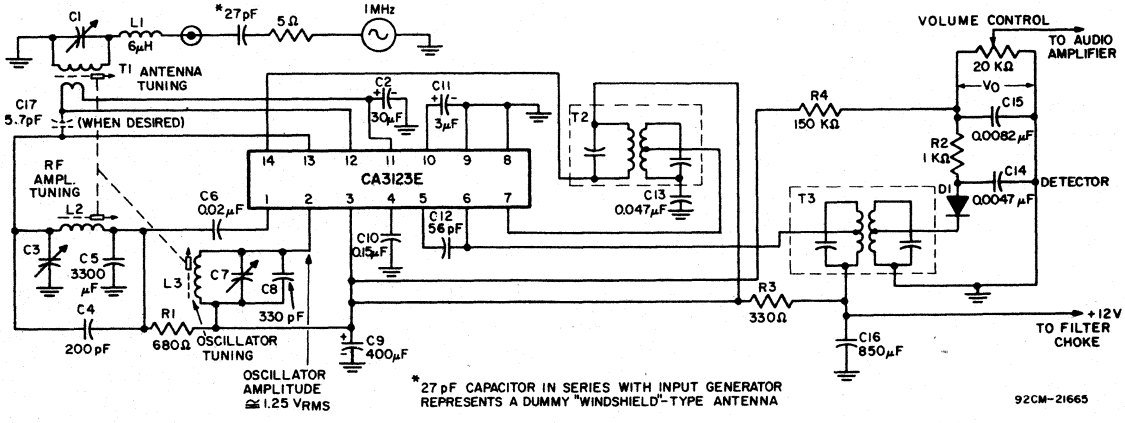


Fig. 2– Schematic diagram of CA3123E.



Transformer	Symbol	Frequency	Inductance μh (≈)	Capacitance pF (≈)	Q (≈)	Total Turns To Tap Turns Ratio	Coupling
First IF: Primary	T_2	262 kHz	2840	130	60	none	critical ≈0.017 ≈1/Q
Secondary			2840	130	60	or 30:1 31:1	
Second IF: Primary	T_3	262 kHz	2840	130	60	8.5:1	– critical ≈0.017 ≈1/Q
Secondary			2840	130	60	8.5:1	
Antenna: Primary	T_1	1 MHz	195	$(C_1)-130$	65		
Secondary		Adjusted to an impedance of 75 Ω with primary resonant at 1 MHz. Coupling should be as tight as practical. Wire should be would around end of coil away from tuning core.					
Coils	L_1	7.9 MHz	6		50		
	L_2	1 MHz	55		50		
	L_3	1.262 MHz	41		40		

Fig. 3– Schematic diagram of AM radio receiver using CA3123E.

TYPICAL CHARACTERISTICS

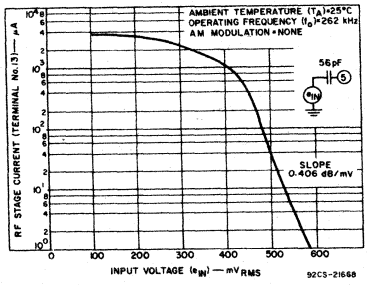


Fig. 4— Control of RF stage by signal into Terminal No. 5.

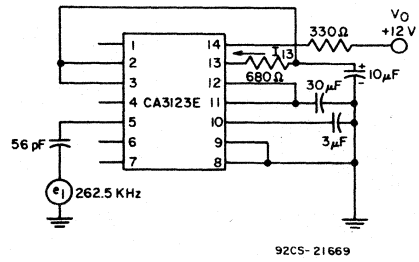


Fig. 5— Test circuit for Fig. 4.

PERFORMANCE CHARACTERISTICS IN CIRCUIT OF FIG. 3

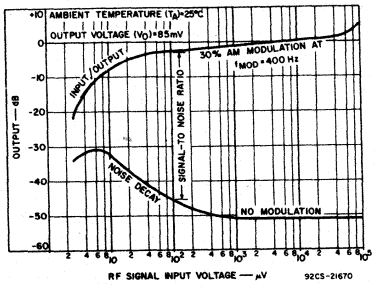


Fig. 6— Signal-to-noise performance.

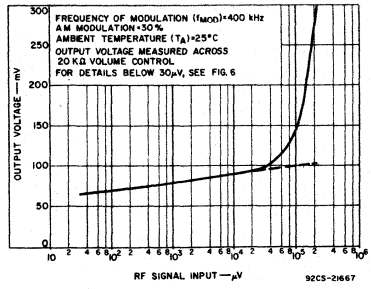


Fig. 7— AGC curve showing voltage rise (controlled by external capacitance of 5.7 pF: C_{17}, Fig. 3).

Change in slope in the vicinity of 40000 μV signal input voltage is the result of the use of C_{17} (5.7 pF) in Fig. 3. The dotted curve indicates expected performance if C_{17} = 0.

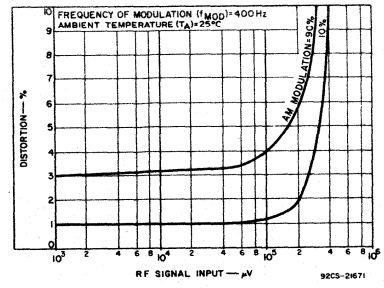
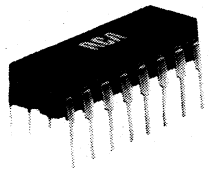


Fig. 8— Overload response.

CA3189E



16-Lead Dual-In-Line Plastic Package (E)

H-1622

FM IF System

Includes IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Tuning Meter, Deviation-Noise Muting, and ON Channel Detector

For FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers

Features:

- *Exceptional limiting sensitivity: 12μV typ. at −3 dB point*
- *Low distortion: 0.1% typ. (with double-tuned coil)*
- *Single-coil tuning capability*
- *Improved S + N/N Ratio*
- *Externally programmable recovered audio level*
- *Provides specific signal for control of interchannel muting (squelch)*
- *Provides specific signal for direct drive of a tuning meter*
- *On channel step for search control*
- *Provides programmable AGC voltage for RF amplifier*
- *Provides a specific circuit for flexible audio output*
- *Internal supply-voltage regulators*
- *Externally programmable "on" channel step width, and deviation at which muting occurs*

The RCA-CA3189E* is a monolithic intergrated circuit that provides all the functions of a comprehensive FM-IF system. Fig. 1 shows a block diagram of the CA3189E, which includes a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as programmable delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power-supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5 to +16 volts.

The CA3189E is ideal for high-fidelity operation. Distortion in a CA3189E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3189E has all the features of the CA3089E plus additions. See CA3189E features compared to the CA3089E in Table I.

The CA3189E utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of −40° C to +85° C.

*Formerly Developmental Type No. TA10038.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C:*

DC SUPPLY VOLTAGE (between Terms. 11 and 4) ..... 16 V

(between Terms. 11 and 14) ..... 16 V

DC CURRENT (Out of Term. 15) ..... 2 mA

DEVICE DISSIPATION:

Up to T_A = 85° C ..... 640 mW

Above T_A = 85° C ..... derate linearly at 9.9 mW/° C

AMBIENT TEMPERATURE RANGE:

Operating ..... −40 to +85° C

Storage ..... −65 to +150° C

LEAD TEMPERATURE (During soldering):

At distance not less than 1/32 inch (0.79 mm) from case for 10s max. ..... +265° C

ELECTRICAL CHARACTERISTICS, at $T_A = 25^oC$, $V^+ = 12$ Volts

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS			UNITS
				Circuit or Fig. No.	Min.	Typ.	Max.	
Static (DC) Characteristics								
Quiescent Circuit Current	I_{11}	No signal input, Non muted		3,4	20	31	40	mA
DC Voltages: Terminal 1 (IF Input)	V_1				1.2	1.9	2.4	V
Terminal 2 (AC Return to Input)	V_2				1.2	1.9	2.4	V
Terminal 3 (DC Bias to Input)	V_3				1.2	1.9	2.4	V
Terminal 15 (RF AGC)	V_{15}				7.5	9.5	11	V
Terminal 10 (DC Reference)	V_{10}				5	5.6	6	V
Dynamic Characteristics								
Input Limiting Voltage (−3 dB point)	V_I(lim)				–	12	25	μV
AM Rejection (Term. 6)	AMR	V_{IN} = 0.1 V, AM Mod. = 30%	f_O = 10.7 MHz,	3,4	45	55	–	dB
Recovered AF Voltage (Term. 6)	V_O(AF)				325	500	650	mV
Total Harmonic Distortion:* Single Tuned (Term. 6)	THD	V_{IN} = 0.1 V	$f_{mod.}$ = 400 Hz,	3	–	0.5	1	%
Double Tuned (Term. 6)	THD		Deviation ±75 kHz	4	–	0.1	–	%
Signal plus Noise to Noise Ratio (Term. 6)	S + N/N			3,4	65	72	–	dB
Deviation Mute Frequency	$f_{DEV.}$		$f_{mod.}$ = 0	3,6,7	–	±40	–	kHz
RF AGC Threshold	V_{16}			3,4	–	1.25	–	V
On Channel Step	V_{12}	V_{IN} = 0.1 V	$f_{DEV.}$ < ±40 kHz	3	–	0	–	V
			$f_{DEV.}$ > ±40 kHz		–	5.6	–	

*THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.

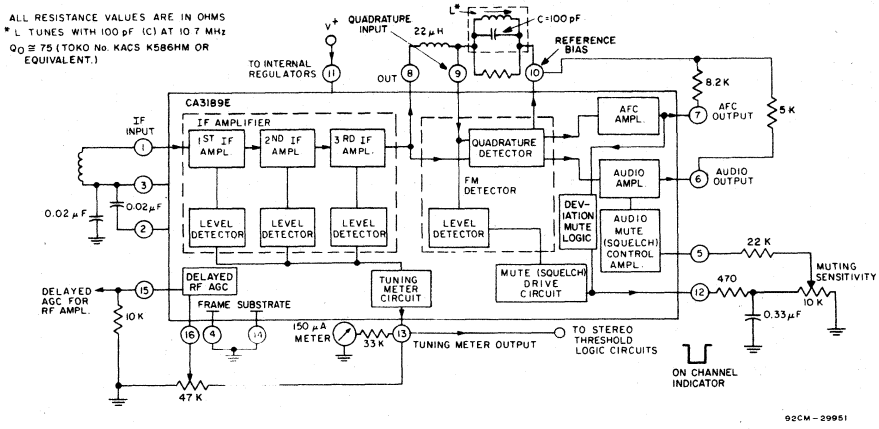


Fig. 1 – Block diagram of the CA3189E.

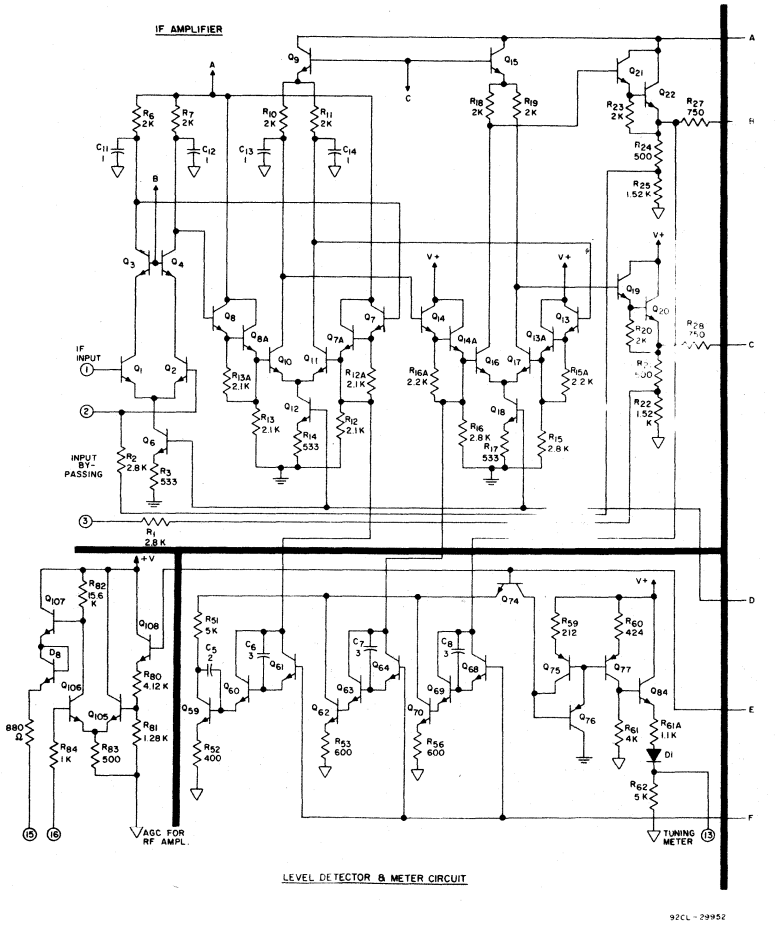


Fig. 2 – Schematic diagram of the CA3189E (cont'd on next page).

TABLE I – CA3189E Features Compared to CA3089E

FEATURES	CA3189E	CA3089E
Low Limiting Sensitivity (12 μV typ.)	Yes	Yes
Low Distortion	Yes	Yes
Single-coil Tuning Capability	Yes	Yes
Programmable Audio Level	Yes	No
S/N Mute	Yes	Yes
Deviation Mute	Yes	No
Flexible AFC	Yes	Yes
Programmable AGC Threshold and Voltage	Yes	No
Typical S + N/N > 70 dB	Yes	No
Meter Drive Voltage Depressed at Very-Low Signal Levels	Yes	No
On-Channel Step Control Voltage	Yes	No

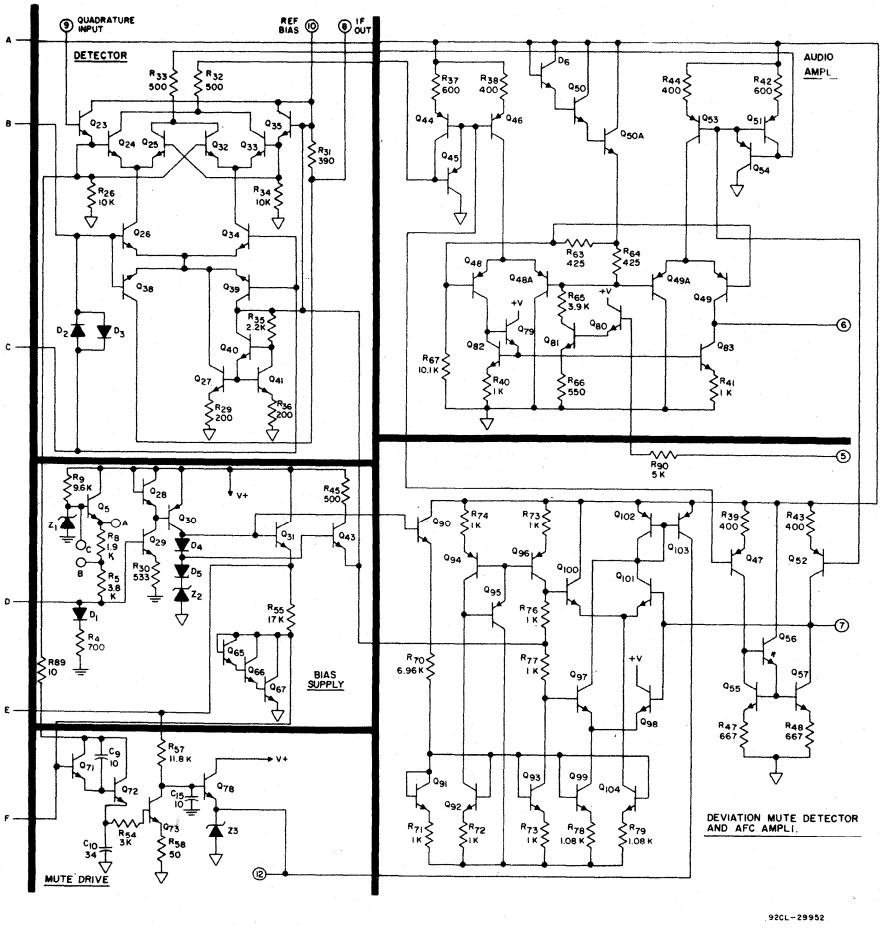
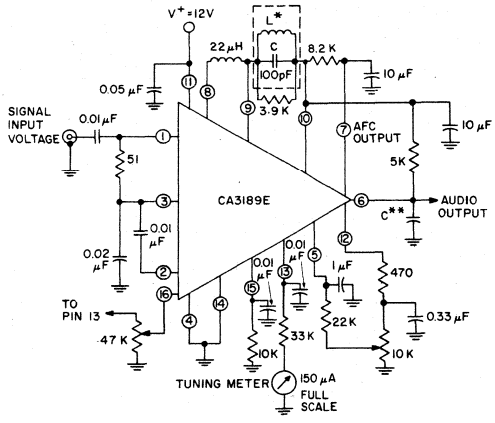


Fig. 2 - Schematic diagram of the CA3189E (cont'd from previous page).

CA3189E



ALL RESISTANCE VALUES ARE IN OHMS
*L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_0(UNLOADED)≅75 (TOKO No. KACS K586HM OR EQUIVALENT)
**C=0.01 μF FOR 50 μs DEEMPHASIS (EUROPE)
=0.015 μF FOR 75 μs DEEMPHASIS (USA)

92CM-29953

Fig. 3 – Test circuit for CA3189E using a single-tuned detector coil.

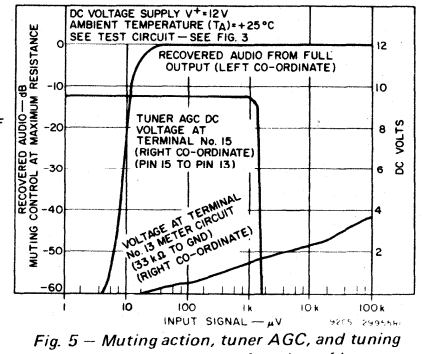


Fig. 5 – Muting action, tuner AGC, and tuning meter output as a function of input signal voltage.

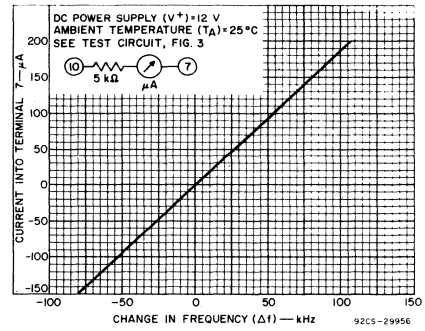
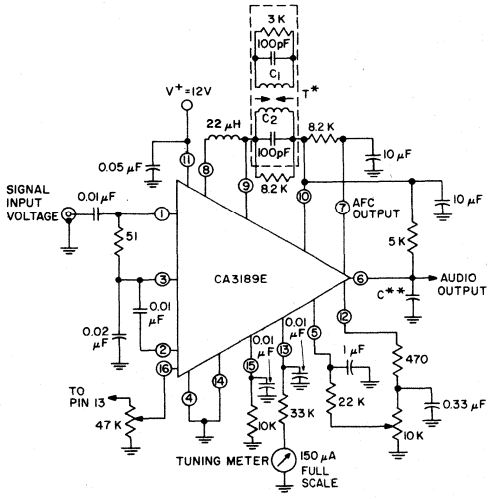


Fig. 6 – AFC characteristics (current at Term. 7 as a function of change in frequency).



ALL RESISTANCE VALUES ARE IN OHMS
*T: PRI.–Q_0(UNLOADED)≅75 (TUNES WITH 100 pF (C1) 20t OF 34e ON 7/32" DIA. FORM
SEC.–Q_0(UNLOADED)≅75 (TUNES WITH 100 pF (C2) 20t OF 34e ON 7/32" DIA. FORM
kQ (PER CENT OF CRITICAL COUPLING)≅70%
(ADJUSTED FOR COIL VOLTAGE V_C)=150 mV
ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT
"E" TYPE SLUGS, SPACING 4 mm
**C=0.01 μF FOR 50 μs DEEMPHASIS (EUROPE)
=0.015 μF FOR 75 μs DEEMPHASIS (USA)

Fig. 4 – Test circuit for CA3189E using a double-tuned detector coil.

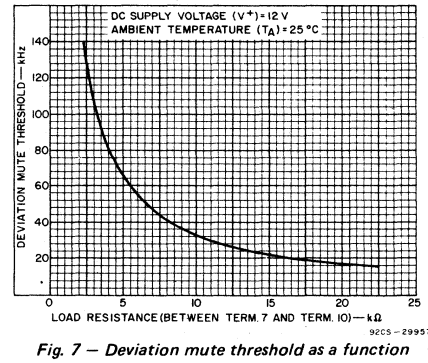


Fig. 7 – Deviation mute threshold as a function of load resistance (between Term. 7 and Term. 10).

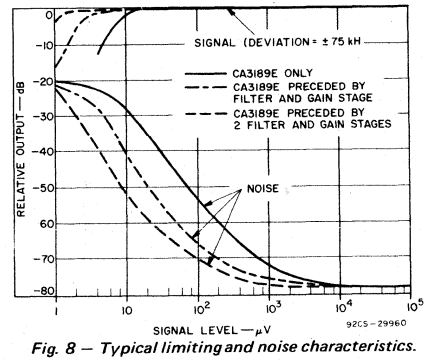


Fig. 8 – Typical limiting and noise characteristics.

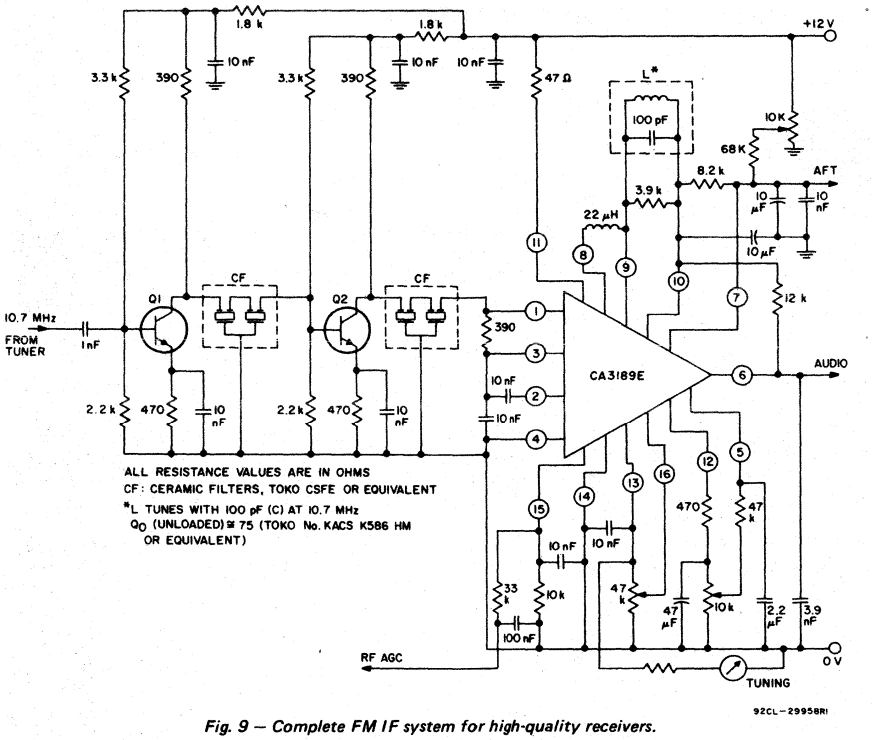
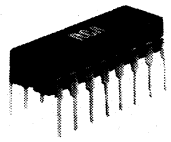


Fig. 9 — Complete FM IF system for high-quality receivers.

CA3209E



16-Lead Dual-In-Line Plastic Package

H-1622

FM-IF System

For Search and Scan

Features:

- *Exceptional limiting sensitivity: 12 μV typ. at -3 dB point*
- *Exceptional temperature stability of tuning and stop-pulse window*
- *Single-coil tuning capability*
- *Externally programmable stop-pulse window width*
- *Programmable level for AGC action*
- *Forward AGC for pin-diode or bipolar rf amplifier*
- *Required input level to generate a stop-pulse is programmable*

The RCA CA3209E• is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. It is intended for use in FM—IF amplifier applications in high-fidelity, automotive, and communications receivers where the synthesizer counter can be controlled by a stop-pulse for scan and search operation.

•Formerly Developmental Type No. TA10493B

Fig. 1 shows the CA3209E features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier.

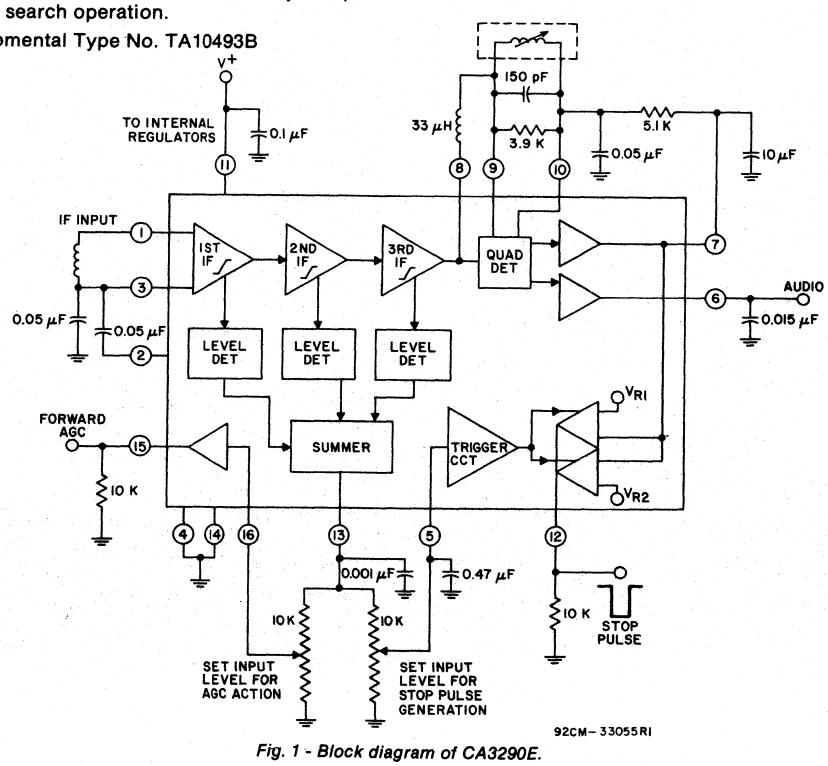


Fig. 1 - Block diagram of CA3290E.

CA3209E

The advanced circuit design of the if system includes desirable deluxe features such as delayed AGC for the rf tuner, and an output signal to drive a tuning meter and/or provide stereo switching logic control of stop pulse and AGC thyristors. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5 to +16 volts.

The CA3209E is ideal for high-fidelity operation. Distortion in a CA3209E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3209E utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of -40° C to +85° C.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
- Between terminals 11 and 4 ..... 16 V
- Between terminals 11 and 14 ..... 16 V

DC CURRENT (Out of Terminal 15) ..... 2 mA

DEVICE DISSIPATION:
- Up to T_A = 85° C ..... 735 mW
- Above T_A = 85° C ..... Derate linearly 11.4 mW/° C

AMBIENT TEMPERATURE RANGE:
- Operating ..... -40 to +85° C
- Storage ..... -65 to +150° C

LEAD TEMPERATURE (During Soldering):
- At distance not less than 1/32" (0.79 mm) from case for 10 seconds max. ..... +265° C

ELECTRICAL CHARACTERISTICS at T_A = 25° C, V+ = 12 Volts
(See Fig. 3 for Test Circuit)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Static (DC) Characteristics					
Quiescent Circuit Current		20	31	44	mA
DC Voltages:					
V_1, V_2, V_3		1.2	1.9	2.4	V
V_{10}		4.9	5.6	6.1	V
V_{15}	V_{16} = 0 V	—	0.005	0.4	V
V_{15}	V_{16} = 1.4 V	4.1	5.1	5.6	V
V_{16}	V_{15} = 1-2 V	—	1.22	—	V
V_{12}	$V_5 \leqq$ 0.24 V	4.3	5.7	6.6	V
V_{12}	$V_5 \geqq$ 0.53 V	—	0.06	0.4	V
V_5 to cause transition of trigger (V_{12}) high to low		—	0.45	—	V
V_5 to cause transition of trigger (V_{12}) low to high		—	0.40	—	V
Dynamic Characteristics					
Input Limiting Voltage (-3 dB point)		—	12	25	μV
Recovered Audio Voltage	400 Hz Input ≧ 1 mV ±75 kHz Deviation	350	520	700	mV
Frequency Window of Stop Pulse V_5 = 0.6 V Input = 100 μV	R_7 -10 = 5.1 K	70	120	200	kHz
	R_7 -10 = 8.2 K	45	75	125	
Total Harmonic Distortion, THD: *			0.50	1.0	%
AM Rejection	30% AM 100 mV Input	50	65	—	dB
	100 μV Input	35	42	—	
S/N Ratio **	100 mV Input	70	80	—	dB
	100 μV Input	55	65	—	
V_{13}	No Signal	0	0.2	0.8	V
	100 μV Input	1.4	2.2	3.2	
	100 mV Input	4.9	6.5	8.5	

* THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.

** Measured with a 30-kHz low-pass filter (-3 dB at 30 kHz, 18 dB/octave).

CA3209E

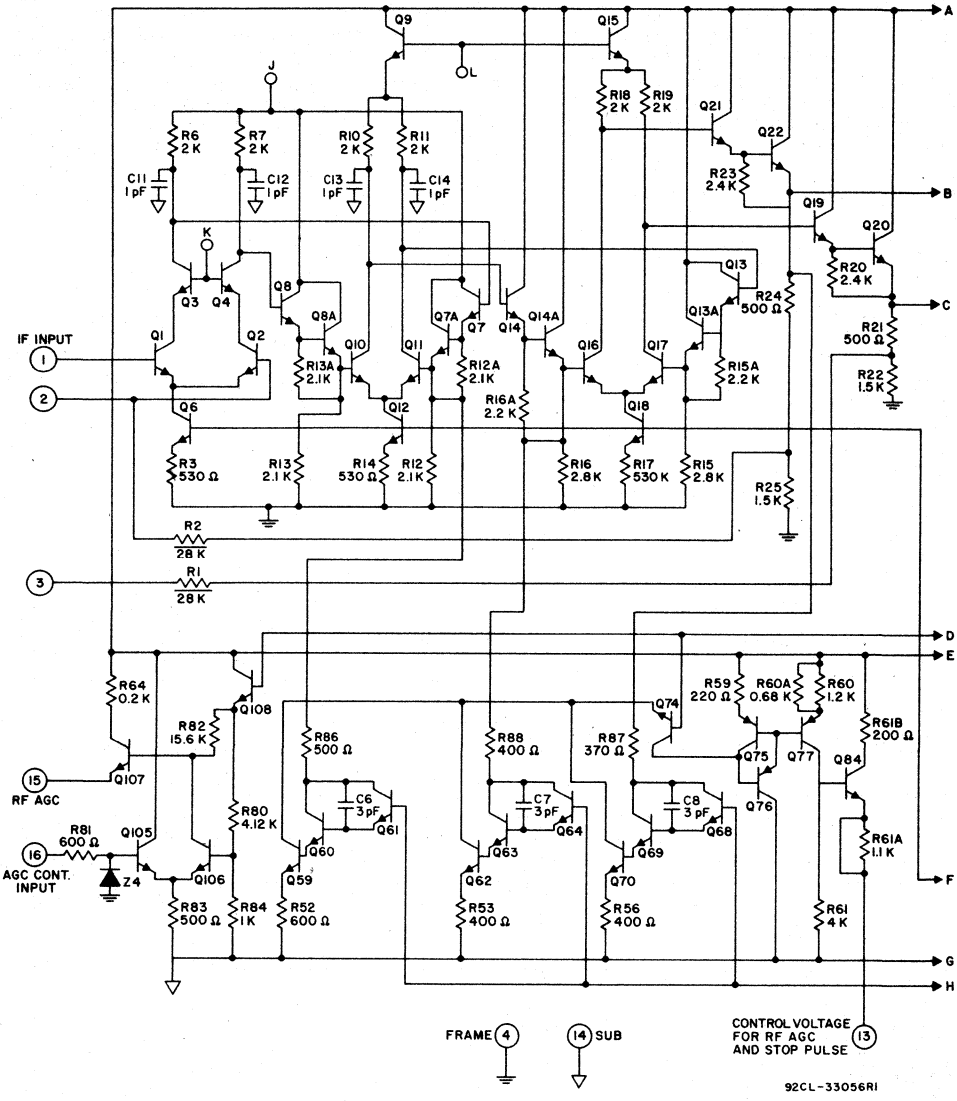


Fig. 2 - Schematic diagram of CA3209E
(continued on next page).

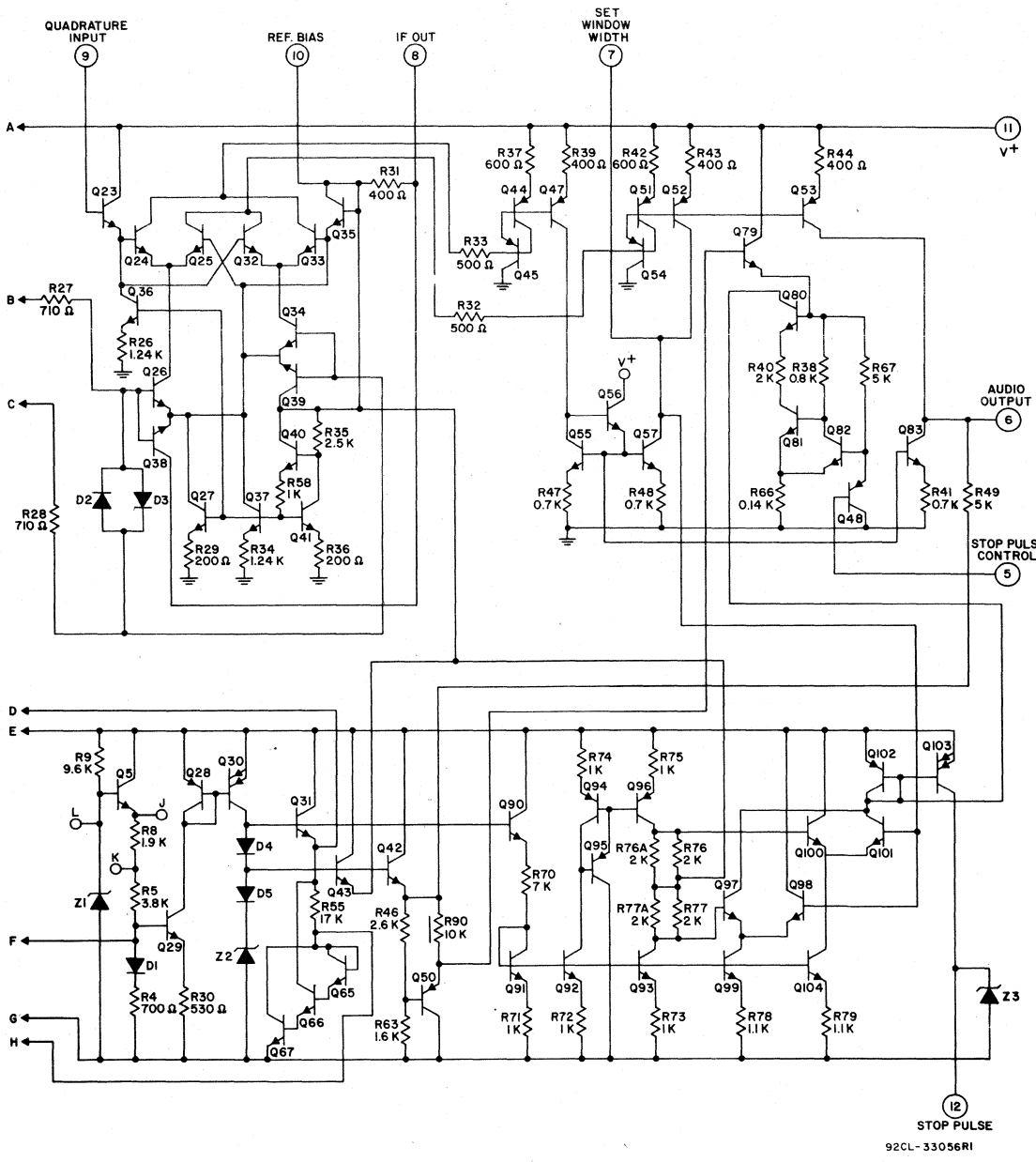


Fig. 2 - Schematic diagram of CA3209E (continued from previous page).

CA3209E

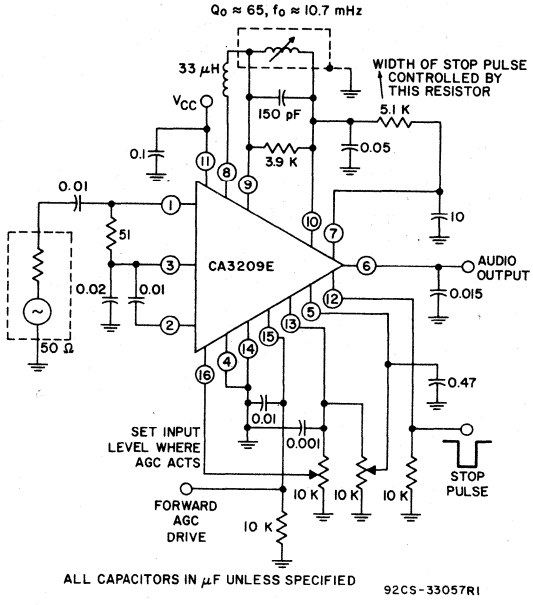


Fig. 3 - Test circuit.

MOS/FET Devices
Technical Data

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFET Story

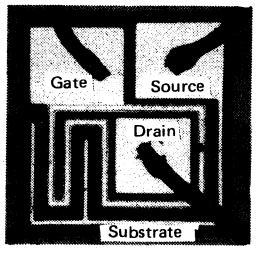
RCA MOS insulated-gate field-effect transistors are N-channel, depletion-type silicon devices, and are available in both single-gate and dual-gate types. Both types offer the advantages of extremely high input resistance, low input capacitance, very low feedback capacitance, high forward transconductance, and low noise at very high frequencies. Because of their insulated-gate construction, these devices have extremely low leakage currents which are relatively insensitive to temperature variations. In addition, their drain currents have a negative temperature coefficient which makes "thermal runaway" virtually impossible.

The extremely high input resistance of RCA MOS transistors permits the use of simple biasing techniques. It also makes these devices capable of handling relatively large positive and negative input-signal excursions without degradation of input impedance due to diode-current loading. Because of this capability, MOS transistors have considerably greater dynamic ranges than junction-type field-effect transistors and bipolar transistors of comparable ratings, and can provide superior performance in amplifier circuits utilizing automatic gain control. Furthermore, the extremely high input resistances of these devices impose virtually no loading on AGC voltage sources.

In addition to the features described above, RCA MOS transistors are notably superior to other solid-state devices in cross-modulation characteristics, and in their relative freedom from spurious responses. These transistors are also characterized by zero offset voltage—a feature which makes them especially desirable for chopper applications.

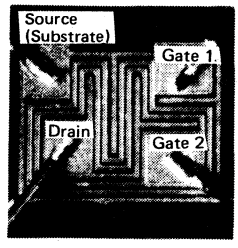
Applications

RCA Single-Gate MOS Transistors provide outstanding performance in applications requiring extremely high input impedance. They are also capable of providing high power gains at frequencies up to approximately 250 MHz. Typical applications for these devices include



rf-amplifier, mixer, and oscillator service in mobile and fixed communications equipment and in home entertainment equipment, and as audio and wide-band amplifiers, variable attentuators, choppers, and current limiters in industrial instrumentation and control equipment. *RCA single-gate MOS transistors also feature a separate terminal permitting connection to the bulk (substrate).*

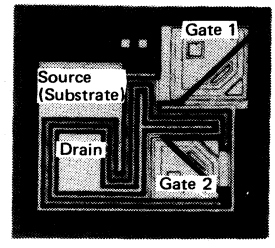
RCA Dual-Gate MOS Transistors feature a series arrangement of two separate channels, each channel having an independent control gate. This arrangement results in substantially lower feedback capacitance, greater gain, remote AGC capability in rf-amplifier applications, substantially better cross-modulation characteristics and lower spurious response than are provided by single-gate types. The availability of two independent control gates also offers unique advantages for chopper, clipper, and gated-amplifier service, and for applications involving the combination of two or



more signals, such as mixers, product detectors, color demodulators, and balanced modulators.

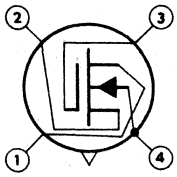
RCA Dual-Gate-Protected RF MOS Transistors incorporate back-to-back diodes for each gate within the same silicon MOSFET pellet. The major technical challenge in the development of these new MOSFETs was that gate protection must not significantly degrade the RF performance. Special back-to-back diodes were developed as the answer to this objective.

The back-to-back diodes are diffused directly into the MOS pellet and are electronically connected between each insulated gate and the FET's source; this arrangement permits the device to handle a wide dynamic signal swing and still provide excellent RF performance. The low junction capacitance of the diodes adds little to the total capacitance shunting the gate. Furthermore, the resistive components of these diodes are such that they do not materially affect the overall noise performance of the unit.

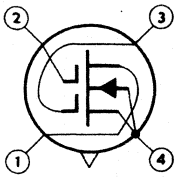


The net result is a MOSFET which protects against static discharge during handling operations without the need for external shorting mechanisms, protects against in-circuit transients, and is more rugged than any other solid-state amplifier providing comparable performance.

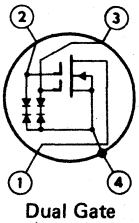
RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)



Single Gate



Dual Gate



Dual Gate
with gate protection

RCA Single-gate and dual-gate MOSFETs offer these features and benefits to the designer:

- Extremely high input resistance — imposes virtually no loading on AGC voltage source
- Very low feedback capacitance
- High forward transconductance
- Wide dynamic range — handle positive and negative input-signal excursions without diode-current loading
- Wide AGC range
- Virtually no AGC power required
- Very low gate leakage current — relatively insensitive to temperature variations
- Negative temperature coefficient of drain current — makes "thermal runaway" virtually impossible
- Zero offset voltage — especially desirable for chopper applications
- Bulk (substrate) terminal available on all single-gate types
- Substantially better cross-modulation characteristics and lower spurious response than junction-type FET's and bipolar transistors
- Operating-temperature range, all types: −65 to +175°C

RCA Dual-gate MOSFETs offer these additional features

- Extremely low feedback capacitance
- Reduced oscillator feedthrough
- Higher frequency capabilities
- Exceptionally high forward transconductance
- Higher vhf power gain
- No neutralization required
- Increased gain reduction with AGC
- Cross-modulation characteristics actually improve as device approaches cutoff
- Unique advantages for mixer, product-detector, remote gain control, color-demodulator, balanced-modulator, chopper, clipper, and gated-amplifier applications
- Can function as a triode equivalent device when the two gates are connected to a single terminal

Quick-Selection Guide

Application	Industrial Types													Consumer Types																	
	Single-Gate								Dual-Gate			Dual-Gate Protected		Single-Gate			Dual-Gate					Dual-Gate Protected									
	3N128	3N138	3N139	3N142	3N143	3N152	3N153	3N154	3N140	3N141	3N159	3N187	3N200	40819	40467A	40468A	40559A	40600	40601	40602	40603	40604	3N204	3N205	3N206	40673	3N211	3N212	3N213	40820	40821	40822	40823	40841
RF Amplifier, Mixer	■			■	■	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
Chopper		■					■																										■
General-Purpose Amplifier			■	■																■													■
Oscillator	■		■	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
Low-Noise						■					■	■	■										■	■			■	■						
Low-Leakage		■					■		■	■	■							■	■	■	■	■												
High-Gain						■			■		■	■	■										■	■	■		■	■	■					
Gain-Controlled									■	■	■	■	■	■				■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
Premium-Performance						■					■	■	■																				

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application and for instrumentation, chopper, and control application in industrial and military equipment

Description and Application				Absolute Maximum Ratings# At T_A = 25°C					
RCA Type	Description	Usable Frequency Range MHz	Circuits and End-Use Equipment	Drain-to-Source Volts V_{DS}		Gate 1-to-Source Volts V_{G1S}		Gate 2-to-Source Volts V_{G2S}	
				Neg.	Pos.	DC	Peak AC	DC	Peak AC
SINGLE-GATE DEVICES■									
For RF Applications									
3N128	High-Gain, Low-Noise RF Amplifier, IF Amplifier, Oscillator	to 250	High-Impedance Timing Circuits, Detectors, Frequency Multipliers, Phase Splitters, Pulse Stretchers, Voltage-Controlled Attenuators Electrometer Amplifiers, High-Impedance Differential Amplifiers in VHF Fixed and Mobile Communications Equipment and for Instrumentation and Navigation	0	+20	+1 to −8	±15	–	–
3N139	High-Gain RF Amplifier, Video Amplifier, IF Amplifier For Use With High Drain Supply Voltage (+35 V max.)	to 250		0	+35	±10	±14	–	–
3N142	High-Gain Low-Noise RF Amplifier and Oscillator	to 175		0	+20	+1 to −8	±15	–	–
3N143	Mixer and Oscillator	to 250		0	+20	+1 to −8	±15	–	–
3N152	Low-Noise, Premium-Performance RF Amplifier	to 250		0	+20	+1 to −8	±15	–	–
3N154	Low-Leakage Premium-Performance RF Amplifier	to 250		0	+20	+1 to −8	±15	–	–
For Chopper, Instrumentation, and Control Applications									
3N128	High-Gain DC Amplifier	to 250	Servo Amplifiers, Telemetry Amplifiers, Computer Operational Amplifiers, Sampling Circuits, Electrometer Amplifiers in Communications, Navigation, and Instrumentation Equipment and Control Circuits	0	+20	+1 to −8	±15	–	–
3N138	For Chopper and Multiplex Service to 60 MHz DC Amplifier	to 250		0	+35	±10	±14	–	–
3N139	DC Amplifier, Video Amplifier, RF Amplifier with High Drain Voltage Capability (+35 V max.)	to 250		0	+35	±10	±14	–	–
3N142	DC Amplifier	to 175		0	+20	+1 to −8	±15	–	–
3N153	For Chopper and Multiplex Service to 60 MHz DC Amplifier	to 250		0	+20	+6 to −8	±14	–	–
DUAL-GATE DEVICES WITH INTEGRAL GATE PROTECTION									
For RF Applications									
3N140	High-Gain, Low-Noise Gain-Controlled RF Amplifier, IF Amplifier	to 300	Communications Equipment	0	+20	+1 to −8	+20 to −8	−8 to 40% of V_{DS}	−8 to +20

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application and for instrumentation, chopper, and control application in industrial and military equipment

Electrical Characteristics at T_A = 25°C												
Typical Gate-Leakage (Input) Resistance r_{GS} Ohms	Offset Voltage V_O● Volts	Typical "ON" Resistance $r_{DS}(on)$ Ohms	Typical Power Gain G_{PS} dB	Typical Noise Figure NF dB	Noise Figure and Power Gain Test Frequency MHz	Typical Forward Transconductance g_{fs} umho	Max. Gate Leakage Current I_{GSS} nA	Typ. Input Capacitance C_{iss} pF	Typical Gate-to-Source Cutoff Volts V_{GS}	Typical Reverse Transfer Capacitance (Feedback) C_{rss} pF	Application Note and Data Sheet File No.	RCA Type
												SINGLE-GATE DEVICES■
												For RF Applications
–	–	–	16*	3.5	200	7500	5	5.5	–3	0.25	AN3193 AN3341 309	3N128
–	–	–	–	–	–	6000	1 0.1 nA Typ.	3	–6 max.	0.2	ST3703 284	3N139
–	–	–	16*	2.5	100	7500	1 0.1 pA Typ.	5.5	–3	0.22	ST3703 286	3N142
–	–	–	13.5 (conv.)	–	f_{IN}=200 f_{OUT}=30	7500	200	5.5	–3	0.25	AN3193 AN3341 309	3N143
–	–	–	16*	2.5	200	7500	1 0.1 pA Typ.	5.5	–3	0.25	ST3703 314	3N152
Closely Controlled Zero-Bias Drain Current (I_{DSS}), 10 to 25 mA			16*	3.5	200	7500	5 0.1 pA Typ.	5.5	–3	0.25	– 335	3N154
												For Chopper, Instrumentation, and Control Applications
10^{14}	0	200	16*	3.5	200	7500	5	5.5	–3	0.25	AN3193 AN3341 309	3N128
10^{14}	0	180#	–	–	–	6000	10 pA	3	–10 max.	0.2	AN3452 283	3N138
10^{14}	0	200	–	–	–	6000	1	3	–6 max.	0.2	ST3703 284	3N139
10^{12}	0	200	16*	2.5	100	7500	1 0.1 pA Typ.	5.5	–3	0.22	ST3703 286	3N142
10^{10}	0	200##	–	–	–	10000	50 pA	6	–2	0.34	– 320	3N153
												DUAL-GATE DEVICES WITH INTEGRAL GATE PROTECTION
												For RF Applications
–	–	–	–	3.5	18	10000	1▲	5.5	–2▲	0.02	– 285	3N140

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application and for instrumentation, chopper, and control application in industrial and military equipment—cont'd.

Description and Application				Absolute Maximum Ratings# At T_A = 25°C					
RCA Type	Description	Usable Frequency Range MHz	Circuits and End-Use Equipment	Drain-to-Source Volts V_{DS}		Gate 1-to-Source Volts V_{G1S}		Gate 2-to-Source Volts V_{G2S}	
				Neg.	Pos.	DC	Peak AC	DC	Peak AC
3N141	Mixer, Product Detector, Modulator	to 300	Aircraft and Marine Vehicular Receivers	0	+20	+1 to −8	+20 to −8	−8 to 40% VDS	−8 to +20
3N159	High-Gain, Very Low-Noise, Gain-Controlled RF Amplifier	to 300		0	+20	+1 to −8	+20 to −8	−8 to 40% V_{DS}	−8 to +20
3N187	RF Amplifier, Mixer, and IF Amplifier	to 300	CATV and MATV Equipment	−0.2	+20	+3 to −6	±6	−6 to 30% V_{DS}	±6
3N200	High-Gain RF Amplifier, Mixer, and IF Amplifier	to 500	Telemetry and Multiplex Equipment	−0.2	+20	+3 to −6	±6	−6 to 30% V_{DS}	±6
40819	RF Amplifier, Mixer, and IF Amplifier	to 300		−0.2	+25	+3 to −6	±6	−6 to 40% V_{DS}	±6
For Chopper, Instrumentation, and Control Applications									
3N140	DC Amplifier	to 300	See Choppers Instrumentation, and Control Applications on Page 4	0	+20	+1 to −8	+20 to −8	−8 to 40% V_{DS}	−8 to +20
3N141	DC Amplifier	to 300		0	+20	+1 to −8	+20 to −8	−8 to 40% V_{DS}	−8 to +20
40841	General-Purpose	to 500				−4.5 to +3		−4.5 to 40% V_{DS}	

For a Maximum Drain Current (I_D) = 50 mA, Device Dissipation (P_T) = 330 mW

■ Bulk (Substrate) is brought out as a separate terminal lead (connected to case internally).

RCA MOSFETs for RF application in consumer equipment

Description and Application				Absolute Maximum Ratings # at T_A = 25°C					
RCA Type	Description	Usable Frequency Range MHz	End-Use Equipment	Drain-to-Source Volts V_{DS}		Gate 1-to-Source Volts V_{G1S}		Gate 2-to-Source Volts V_{G2S}	
				Neg.	Pos.	DC	Peak AC	DC	Peak AC
SINGLE-GATE DEVICES■									
40467A	200-MHz General-Purpose RF Amplifier and Oscillator	to 220	VHF Amplifier Applications in Commercial and Industrial Electronic Equipment	0	+20	+1 to −8	±15	–	–

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application and for instrumentation, chopper, and control application in industrial and military equipment—cont'd.

Electrical Characteristics at T_A = 25°C												
Typical Gate-Leakage (Input) Resistance r_{GS} Ohms	Offset Voltage V_O● Volts	Typical "ON" Resistance $r_{DS(on)}$ Ohms	Typical Power Gain G_{PS} dB	Typical Noise Figure NF dB	Noise Figure and Power Gain Test Frequency MHz	Typical Forward Transconductance g_{fs} umho	Max. Gate Leakage Current I_{GSS} nA	Typ. Input Capacitance C_{iss} pF	Typical Gate-to-Source Cutoff Volts V_{GS}	Typ. Rev. Transfer Capacitance (Fdbk) C_{rss} pF	Application Note and Data Sheet File No.	RCA Type
–	–	–	17 (conv.)	–	f_{IN}= 200 f_{OUT}=30	10000	1▲	5.5	−2▲	0.02	– 285	3N141
–	–	–	16 min.	2.5	200	10000	1▲	5.5	−2▲	0.02	– 326	3N159
–	–	–	18	3.5	200	12000	50▲	6	−2▲	0.02	ST3703 AN4018 436	3N187
–	–	–	12.5	3.9	400	15000	50▲	6	−1▲	0.02	ST3703 AN4018 437 AN4431	3N200
–	–	–	18	3.5	200	12000	50▲	6	−2▲	0.02	ST3703 AN4018 463	40819
For Chopper, Instrumentation, and Control Applications												
10^{12}	0	–	–	–	–	10000	1▲	5.5	−2▲	0.02	– 285	3N140
10^{12}	0	–	–	–	–	10000	1▲	5.5	−2▲	0.02	– 285	3N141
–	–	–	32 24 (conv.)	0.46†	Gps at 44 MHz	12000	60▲	6.5	−2▲	0.20	– 498	40841

* Fixed Neutralization
#Typical "OFF" resistance $[r_{DS(off)}] = 10^{11}\ \Omega$
##Typical "OFF" resistance $[r_{DS(off)}] = 10^{10}\Omega$

●In measurements of Offset Voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings of 1 microvolt or more. These errors may be minimized by the use of solder having a low thermal e.m.f., such as Leeds & Northrup No. 107-1.0.1, or equivalent.

■Bulk (Substrate) is brought out as a separate terminal lead connected to case internally.

▲Value applies to each gate

†Audio spot at 1 kHz.

RCA MOSFETs for RF application in consumer equipment

Electrical Characteristics at T_A = 25°C										
Typical Power Gain G_{PS} dB	Typical Noise Figure NF dB	Noise Figure and Power Gain Test Frequency MHz	Typical Forward Transconductance g_{fs} umho	Max. Gate Leakage Current I_{GSS} mA	Typ. Input Capacitance C_{iss} pF	Typical Gate-to-Source Cutoff Volts		Typical Reverse Transfer Capacitance (Feedback) C_{rss} pF	Application Note and Data Sheet File No.	RCA Type
						Gate 1 V_{G1S}	Gate 2 V_{G2S}			
SINGLE-GATE DEVICES■										
16	3.5	200	7500	1	5.5	−8 max.	–	0.16	ST-2990A 324	40467A

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application in consumer equipment - cont'd.

Description and Application				Absolute Maximum Ratings # at T_A = 25°C					
RCA Type	Description	Usable Frequency Range MHz	End-Use Equipment	Drain-to-Source Volts V_{DS}		Gate 1-to-Source Volts V_{G1S}		Gate 2-to-Source Volts V_{G2S}	
				Neg.	Pos.	DC	Peak AC	DC	Peak AC
40468A	100-MHz RF Amplifier	to 125	FM and AM/FM Receivers	0	+20	+1 to −8	±15	–	–
40559A	100-MHz Oscillator or Mixer	to 125		0	+20	+1 to −8	±15	–	–
DUAL-GATE DEVICES									
40600	200-MHz Gain-Controlled RF Amplifier	to 250	VHF TV Tuners	0	+20	+1 to −8	+20 to −8	−8 to 40% to V_{DS}	−8 to +20
40601	200-MHz Mixer	to 250		0	+20	+1 to −8	+20 to −8	−8 to 40% of V_{DS}	−8 to +20
40602	44-MHz Gain-Controlled IF Amplifier	to 75	TV Receivers	0	+20	+1 to −8	+20 to −8	−8 to 40% of V_{DS}	−8 to +20
40603	100-MHz Gain-Controlled IF Amplifier	to 150	FM Receivers	0	+20	+1 to −8	+20 to −8	−8 to 40% of V_{DS}	−8 to +20
40604	100-MHz Mixer	to 150		0	+20	+1 to −8	+20 to −8	−8 to 40% of V_{DS}	−8 to +20
DUAL-GATE DEVICES WITH INTEGRAL GATE-PROTECTION									
3N204	Low-Noise	RF Amplifier	to 220	VHF TV Receivers	0	+25	P_T = 360 mW		
3N205		Mixer	to 220		0	+25	P_T = 360 mW		
3N206		IF Amplifier	to 220		0	+25	P_T = 360 mW		
3N211		RF Amplifier	to 220		0	+27	P_T = 360 mW		
3N212		Mixer	to 220		0	+27	P_T = 360 mW		
3N213		IF Amplifier	to 220		0	+35	P_T = 360 mW		

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application in consumer equipment - cont'd.

Electrical Characteristics at T_A = 25°C										
Typical Power Gain G_{PS} dB	Typical Noise Figure NF dB	Noise Figure and Power Gain Test Frequency MHz	Typical Forward Transconductance g_{fs} uMho	Max. Gate Leakage Current I_{GSS} mA	Typ. Input Capacitance C_{iss} pF	Typical Gate-to-Source Cutoff Volts: Gate 1 V_{G1S}	Typical Gate-to-Source Cutoff Volts: Gate 2 V_{G2S}	Typical Reverse Transfer Capacitance (Feedback) C_{rss} pF	Application Note and Data Sheet File No.	RCA Type
17	3.5	100	7500	1	5.5	−8 max.	–	0.16	AN-3453 323 AN-3535	40468A
22 (conv.)	–	f_{IN} = 100 f_{OUT}=10.7	2800 (conv.)	1	5.5	−8 max.	–	0.17	AN-3535 323	40559A
DUAL-GATE DEVICES										
20	3.5	200	10000	1	5.5	−3	−3	0.02	ST-3703 333	40600
14 (conv.)	–	200	2800 (conv.)	1	5.5	−3	−3	0.02	ST-3703 333	40601
28	–	44	10000	1	5.5	−3	−3	0.02	ST-3703 333	40602
24	3	100	10000	1	5.5	−3	−3	0.02	ST-3703 334	40603
23 (conv.)	–	f_{IN} = 100 f_{OUT}=10.7	2800 (conv.)	1	5.5	−3	−3	0.02	ST-3703 334	40604
DUAL-GATE DEVICES WITH INTEGRAL GATE-PROTECTION										
24 (Insertion)	2.5	200	14	10▲	5	−4 max.	−4 max.	0.03 max.	– 959	3N20[illegible]
23 (conv.)	–	200	14	10▲	5	−4 max.	−4 max.	0.03 max.	– 959	3N205
30 (Insertion)	3	45	12	10▲	5	−4 max.	−4 max.	0.03 max.	– 959	3N206
30 (Insertion)	2.5	–	30	10▲	7	−5.5 max.	−2.5 max.	0.05 max.	– 875	3N211
25 (conv.)	–	200	30	10▲	7	−4 max.	−4 max.	0.05 max.	– 875	3N212
31 (Insertion)	3	45	25	10▲	7	−5.5 max.	−4 max.	0.05 max.	– 875	3N213

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application in consumer equipment - cont'd.

Description and Application				Absolute Maximum Ratings # at T_A = 25°C					
RCA Type	Description	Usable Frequency Range MHz	End-Use Equipment	Drain-to-Source Volts V_{DS}		Gate 1-to-Source Volts V_{G1S}		Gate 2-to-Source Volts V_{G2S}	
				Neg.	Pos.	DC	Peak AC	DC	Peak AC
40673	200 MHz RF Amplifier, Mixer, and IF Amplifier	to 400	Aircraft and Marine Receivers CATV and MATV Equipment	−0.2	+20	+1 to −6	±6	−6 to 30% of V_{DS}	±6
40820	RF Amplifier	to 250	VHF TV Tuners	−0.2	+20	+3 to −6	±6	−6 to 40% of V_{DS}	±6
40821	RF Mixer	to 250		−0.2	+20	+3 to −4.5	±6	−4.5 to 40% of V_{DS}	±6
40822	RF Amplifier	to 250	FM Tuners	−0.2	+18	+3 to −6	±6	−6 to 40% of V_{DS}	±6
40823	RF Mixer	to 150		−0.2	+18	+3 to −4.5	±6	−4.5 to 40% of V_{DS}	±6

For a Maximum Drain Current (I_D) = 50 mA,
Device Dissipation (P_T) = 330 mW
Operating Temperature Range (T_A) = −65°C to +121°C

■ Bulk (Substrate) is brought out as a separate terminal lead (connected to case internally)

Handling of MOSFETs which do not include gate-protection circuits

Insulated-Gate Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in a MOSFET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

In some MOSFETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms.

MOSFETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

*Trademark: Emerson and Cumming, Inc.

RCA MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

RCA MOSFETs for RF application in consumer equipment - cont'd.

Electrical Characteristics at T_A = 25°C										
Typical Power Gain G_{PS} dB	Typical Noise Figure NF dB	Noise Figure and Power Gain Test Frequency MHz	Typical Forward Transcond-uctance g_{fs} umho	Max. Gate Leakage Current I_{GSS} mA	Typ. Input Capac-itance C_{iss} pF	Typical Gate-to-Source Cutoff Volts		Typical Reverse Transfer Capacitance (Feedback) C_{rss} pF	Application Note and Data Sheet File No.	RCA Type
						Gate 1 V_{G1S}	Gate 2 V_{G2S}			
18	3.5	200	12000	50	6	−2	−2	0.02	ST-3703 381 AN-4018	40673
17	4.5	200	12000	50	6	−1	−1	0.02	ST-3703 464 AN4018	40820
11 (conv.)	–	f_{IN}=200 f_{OUT}=44	12000	50	6	−1	−1	0.02	ST-3703 464 AN-4018	40821
24	3.5	100	12000	50	6.5	−2	−2	0.02	ST-3703 465 AN-4018	40822
18 (conv.)	–	f_{IN} = 100 f_{OUT}=10.7	12000	50	6.5	−2	−2	0.02	ST-3703 465 AN4018	40823

■ Bulk (Substrate is brought out as a separete terminal lead (connected to case internally.

▲ Value applies to each gate

APPLICATION NOTES

No.	Title
AN3193	"Application Considerations for the RCA-3N128 VHF MOS Field-Effect Transistor"
AN3341	"VHF Mixer Design Using the RCA-3N128 MOS Transistor"
AN3435	"Cross-Modulation Effects in Single-Gate and Dual-Gate MOS FET Transistors"
AN3452	"Chopper Circuits Using RCA MOS Field-Effect Transistors"
AN3453	"An FM Tuner Using an RCA-40468 MOS-Transistor RF Amplifier"
AN3535	"An FM Tuner Using Single-Gate MOS Field-Effect Transistors as RF Amplifier and Mixer"
AN4018	"Design of Gate-Protected MOS Field-Effect Transistors"
AN4125	"MOS FET Biasing Techniques"
AN4431	"RF Applications of the Dual-Gate MOS FET up to 500 MHz"
AN4590	"Using MOS FET IC's in Linear Circuit Applications"
ST3486	"Application of Dual-Gate MOS Field-Effect Transistors in Practical Radio Receivers"
ST3520	"Insulated-Gate Field-Effect Transistors in Oscillator Circuits"

A copy of a Technical Bulletin for any of the MOSFET types or a copy of the Application Notes shown above, is available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876. To expedite receipt of the requested data, please refer to the Technical Bulletin File No. shown on the Characteristics Charts, or to the Application Note No.

Supplementary Information

RCA High-Reliability Bipolar IC's

RCA MIL-STD-883 Slash-Series Linear IC's

The RCA CA3000 slash-series of high-reliability linear integrated circuits includes a broad range of types for use in satellites and other aerospace, military, and critical industrial applications in which maintenance is extremely difficult. These integrated circuits are processed and screened in accordance with MIL-STD-883, Method 5004 format.

The RCA CA3000 slash-series types are supplied to three screening levels (/1, /3, and /3W) that meet the electrical, mechanical, and environmental test methods and procedures established for microelectronics in MIL-STD-883.

RCA CA3000-series IC products listed below are commercial products that can be supplied to standard RCA screening levels or to specialized customer requirements on a custom basis.

CA3000-Series Linear IC's and MOS/FET's

Type No.	Description	No. of Leads
CA101A	Operational Amplifiers	8
CA723	Voltage Regulators	10
CA741	Operational Amplifiers	8
CA747	Dual Operational Amplifiers	10
CA748	Operational Amplifiers	8
CA1558	Dual Operational Amplifiers	8
CA3000	Differential Amplifiers	10
CA3001	Differential Amplifiers	12
CA3002	Differential Amplifiers	10
CA3004	Differential Amplifiers (RF)	12
CA3006	Differential Amplifiers (RF)	12
CA3015A	Operational Amplifiers	12
CA3018A	Transistor Arrays	12
CA3019	Diode Arrays	10
CA3020A	Wide-Band Power Amplifiers	12
CA3026	Dual Differential Amplifier Arrays	12
CA3028B	Differential Amplifiers (RF)	8
CA3039	Diode Arrays	12
CA3045	Transistor Arrays	14
CA3049	Dual Differential Amplifier Arrays	12
CA3058	Zero-Voltage Switches	14
CA3078	Micropower Operational Amplifiers	8
CA3080	Variable Operational Amplifiers	8
CA3081	Transistor Arrays	16
CA3082	Transistor Arrays	16
CA3085	Voltage Regulators	8
CA3085A	Voltage Regulators	8
CA3085B	Voltage Regulators	8
CA3094	Programmable Power Switch/ Amplifier	8
CA3094A	Programmable Power Switch/ Amplifier	8
CA3094B	Programmable Power Switch/ Amplifier	8
CA3100	BiMOS Operational Amplifiers	8
CA3118	Transistor Arrays	12
CA3118A	Transistor Arrays	12
CA3130	BiMOS Operational Amplifiers	8
CA3130A	BiMOS Operational Amplifiers	8
CA3140	BiMOS Operational Amplifiers	8
CA3140A	BiMOS Operational Amplifiers	8
CA3160	BiMOS Operational Amplifiers	8
CA3160A	BiMOS Operational Amplifiers	8
CA3260T	BiMOS Operational Amplifier	8
CA3260AT	BiMOS Operational Amplifier	8
CA3290	BiMOS Dual Voltage Comparators	8

MOS/FET's

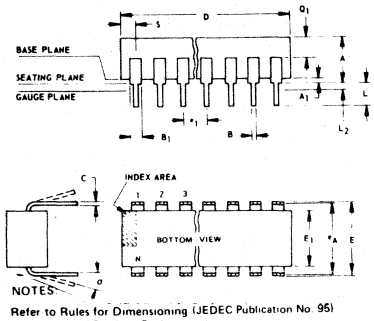
HR3N187	Dual-Gate MOS Field-Effect Transistor	4
HR3N200	Dual-Gate MOS Field-Effect Transistor	4

Note:
High-reliability versions of most commercially available CA3000-series linear IC's not listed above can also be supplied on a custom basis.

Screening Levels for RCA MIL-STD-883 Slash-Series Linear Integrated Circuits

RCA Levels	Screening Levels: MIL-STD-883, Method 5004 Format	Application	Description
For Packaged Devices (D, F, K, S, T, or V1 Suffix)			
/1	Class S with Condition B Precap Visual Inspection	Aerospace and Missiles	For devices intended for use where maintenance and replacement are impossible and reliability is imperative
/3	Class B	Military and Industrial For example, in Airborne Electronics	For devices intended for use where maintenance and replacement can be performed but are difficult and expensive
/3W	Class B with High- and Low-Temperature DC Testing omitted		
For Chips (H Suffix)			
/M	Condition B Precap Visual Inspection with Traceability and Certificate of Compliance Required	Military and Industrial	For general applications

CERAMIC DUAL-IN-LINE PACKAGES



NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(D) Suffix (JEDEC MO-001-AD) 14-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.065	0.090		1.66	2.28

92SS-4411R2

(D) Suffix (JEDEC MO-001-AE) 16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

92SS-4286R5

DUAL-IN-LINE PLASTIC, (E) SUFFIX AND FRIT-SEAL CERAMIC, (F) SUFFIX PACKAGES

(E) Suffix 8-Lead Plastic (Mini-DIP)

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.889	1.65
C	0.008	0.012	1	0.203	0.304
D	0.370	0.400		9.40	10.16
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.762
α	0	15	4	0	15
N	8		5	8	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.381	1.52

92CS-24026R1

(E) and (F) Suffixes (JEDEC MO-001-AB) 14-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

92SS-4296R3

(F) Suffix (JEDEC MO-001-AC) 16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-15967R4

(E) Suffix 18-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.845	0.885		21.47	22.47
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2,3	7.62 TP	
L	0.125	0.150		3.18	3.81
α	0°	15°	4	0°	15°
N	18		5	18	
N_1	0		6	0	
S	0.015	0.060		0.39	1.52

92CS-30630

(E) Suffix 22-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.015	0.020		0.381	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D		1.120			28.44
E	0.390	0.420		9.91	10.66
E_1	0.345	0.355		8.77	9.01
e_1	0.100 TP		2	2.54 TP	
e_A	0.400 TP		2, 3	10.16 TP	
L	0.125	0.150		3.18	3.81
L_2	0	0.030		0	0.762
α	2°	15°	4	2°	15°
N	22		5	22	
N_1	0		6	0	
Q_1	0.055	0.085		1.40	2.15
S	0.015	0.060		0.381	1.27

92CS-30830

(E) Suffix (JEDEC MO-015-AA) 24-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A_1	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B_1	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	1.20	1.29		30.48	32.76
E	0.600	0.625		15.24	15.87
E_1	0.515	0.580		13.09	14.73
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.200		2.54	5.00
L_2	0.000	0.030		0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.040	0.100		1.02	2.54

92CS26938R3

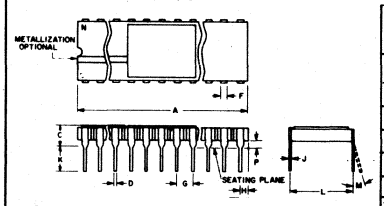
Dimensional Outlines

DUAL-IN-LINE PLASTIC PACKAGE (Cont'd)
(E) Suffix
28-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A_1	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B_1	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	1.400	1.490		35.56	37.85
E_1	0.515	0.580		13.09	14.73
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.200		2.54	5.00
L_2	0.000	0.030		0.00	0.76
α	0°	15°	4	0°	15°
N	28		5	28	
N_1	0		6	0	
Q_1	0.045	0.080		1.14	2.03
S	0.040	0.100		1.02	2.54

92CS-31862

DUAL-IN-LINE SIDE-BRAZED CERAMIC PACKAGE
(D) Suffix
18-Lead

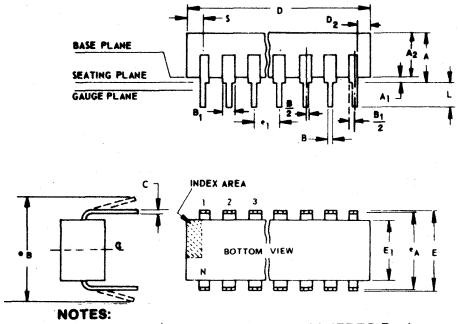


NOTES:
1. Leads within 0.005" (0.13 mm)-radius of True Position at maximum material condition.
2. Dimension "L" to center of leads when formed parallel.
3. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.890	0.915		22.606	23.241
C	—	0.200		—	5.080
D	0.015	0.021		0.381	0.533
F	0.054 REF.		1	1.371 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.035	0.065		0.889	1.651
J	0.008	0.012	3	0.203	0.304
K	0.125	0.150		3.175	3.810
L	0.290	0.310	2	7.366	7.874
M	0°	15°		0°	15°
P	0.025	0.045		0.635	1.143
N	18			18	

92CS-27231R1

(E) Suffix (JEDEC MS-001)
16-Lead Dual-In-Line Plastic Package

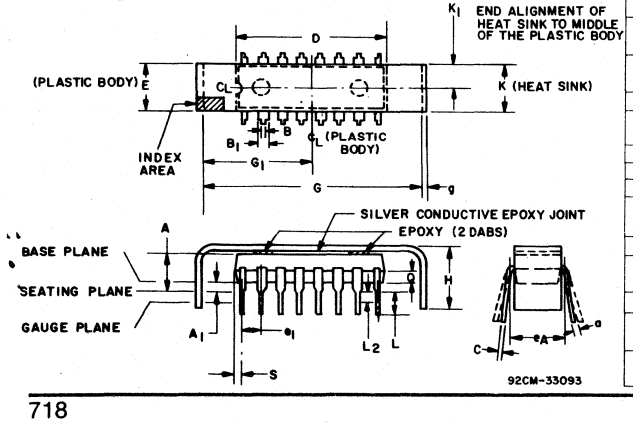


NOTES:
1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines.
2. Protrusions (flash) on the base plane surface shall not exceed .25 mm (.010 in.).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions 1, N, $\frac{N}{2}$, $\frac{N}{2}$ +1.
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed .25 mm (.010 in.).
5. This dimension is controlling when a particular combination of body length, lead width and lead spacing dimensions would allow lead material to overhang the ends of the package.
6. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
7. Dimension E_1 does not include mold flash or protrusions.
8. Package body and leads shall be symmetrical around center line shown in end view within .25 mm (.010 in.).
9. Lead spacing e_1 shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
10. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within .25 mm (.010 in.) diameter for dimension e_A.
11. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
12. N is the maximum number of lead positions.
13. Dimension S at the left end of the package must equal dimension S at the right end of the package within .76 mm (.030 in.).

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	—	0.210	10	—	5.33
A_1	0.015	—	10	0.39	—
A_2	0.115	0.195		2.93	4.95
B	0.014	0.022		0.356	0.558
B_1	0.045	0.070	3	1.15	1.77
C	0.008	0.015		0.204	0.381
D	0.745	0.840	4	18.93	21.33
D_2	0.005	—	5	0.13	—
E	0.300	0.325	6	7.62	8.25
E_1	0.240	0.280	7, 8	6.10	7.11
e_1	0.090	0.110	9	2.29	2.79
e_A	0.300 TP		10	7.62 TP	
e_B	—	0.410	11	—	10.41
L	0.115	0.150	10	2.93	3.81
N	16		12	16	
S	—	—	13	—	—

92CM-34834R1

(EM) Suffix
16-Lead Modified Dual-In-Line Plastic Package with "Power Slab"



92CM-33093

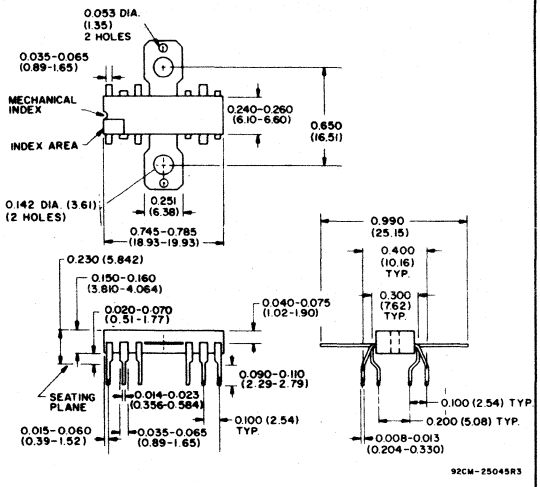
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2,3	7.62 TP	
G_1	0.537	0.587		13.64	14.91
G	1.125			28.58	
g	0.030	0.036		0.76	0.91
H	0.350			8.89	
K	0.250		7	6.35	
K_1	0.093	0.157		2.36	3.99
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.
7. Bulging to 0.280" (7.11 mm) permissible at points of debossing.

Dimensional Outlines

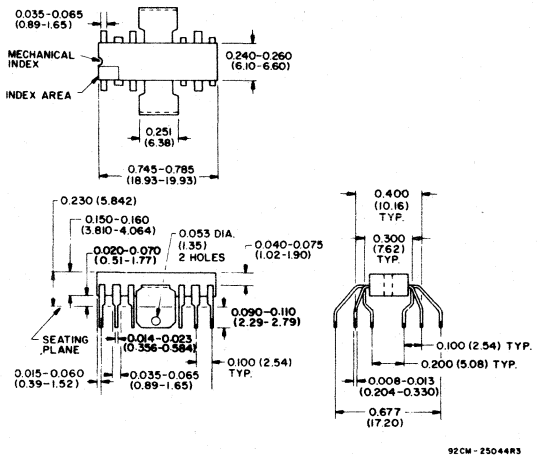
QUAD-IN-LINE PLASTIC PACKAGES

(QM) Suffix
Modified 16-Lead with Integral Flat Wing-Tab Heat Sink

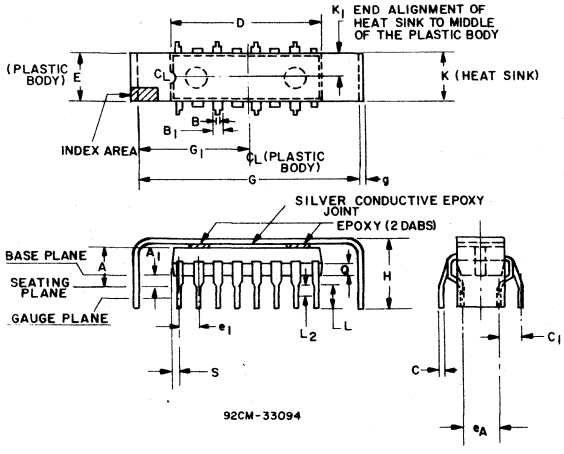


DIMENSIONS IN PARENTHESES ARE MILLIMETER EQUIVALENTS OF THE BASIC INCH DIMENSIONS

(Q) Suffix
Modified 16-Lead with Integral Bent Down Wing-Tab Heat Sink



(QM) Suffix, 16-Lead Quad-In-Line Plastic with "Power Slab"



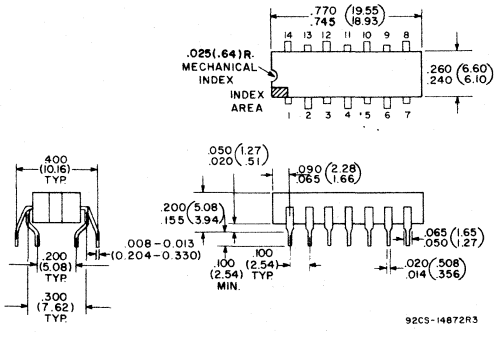
SYMBOL	INCHES MIN.	INCHES MAX.	NOTE	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
C_1	0.095	0.105		2.41	2.67
D	0.745	0.785		18.93	19.93
E	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.200 TP		2,3	7.62 TP	
G	1.125 TP			2.858	
G_1	0.537	0.587		13.64	14.91
g	0.030	0.036		0.76	0.91
H	0.350			8.89	
K	0.250		7	6.35	
K_1	0.093	0.157		2.36	3.99
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for *Axial Lead Product Outlines*.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.
7. Bulging to 0.280" (7.11 mm) permissible at points of debossing.

QUAD-IN-LINE PLASTIC PACKAGES

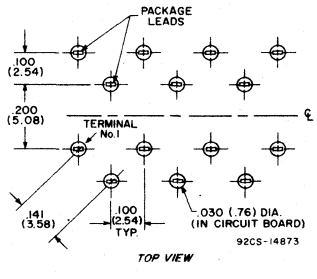
(W) Suffix, 14-Lead Staggered



NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

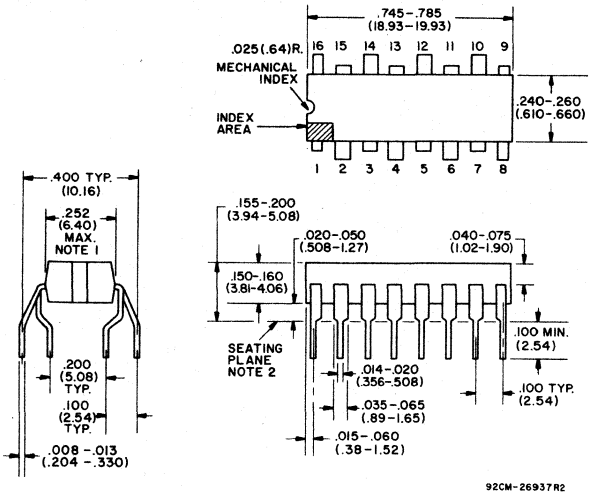
Recommended Mounting Hole Dimensions and Spacing



Dimensional Outlines

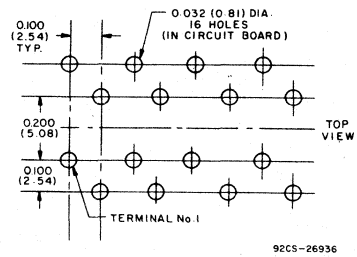
QUAD-IN-LINE PLASTIC PACKAGES

(W) Suffix, 16-Lead Staggered



92CM-26937R2

Recommended Mounting Hole Dimensions and Spacing

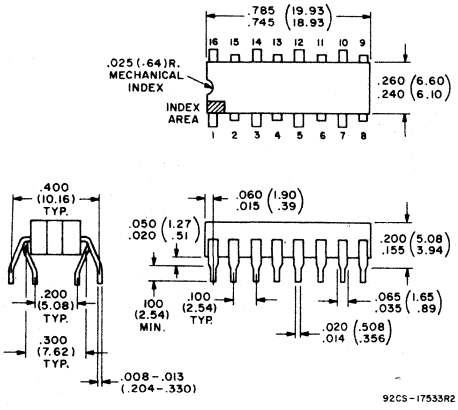


92CS-26936

NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

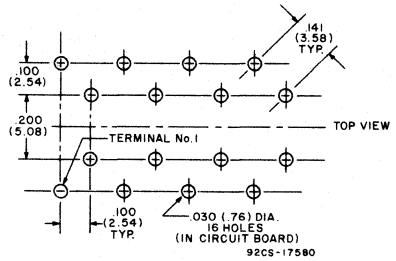
Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

(Q) Suffix, 16-Lead



92CS-17533R2

Recommended Mounting Hole Dimensions and Spacing

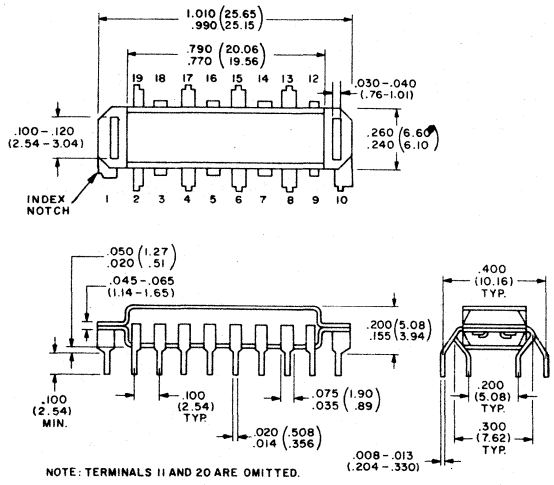


92CS-17580

NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

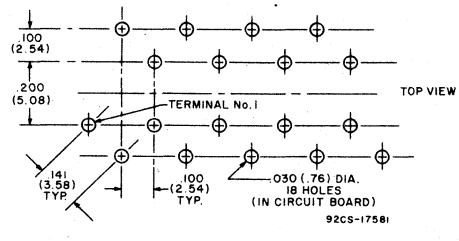
20-Lead Shielded Plastic Package



NOTE: TERMINALS 11 AND 20 ARE OMITTED.

92CS-17587R1

Recommended Mounting Hole Dimensions and Spacing



92CS-17581

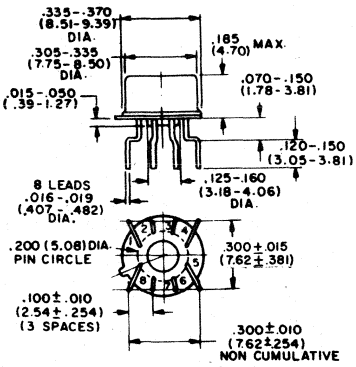
NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

Dimensional Outlines

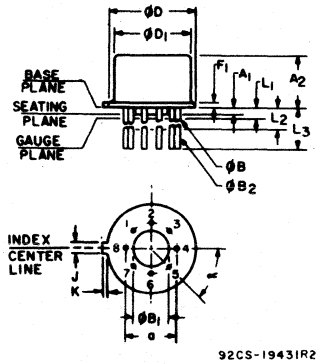
TO-5 STYLE PACKAGES

(S) Suffix, 8-Lead TO-5 Style with Dual-In-Line Formed Leads (DIL-CAN)



92CS-20296R3

(T) Suffix (JEDEC MO-002-AL), 8-Lead TO-5 Style



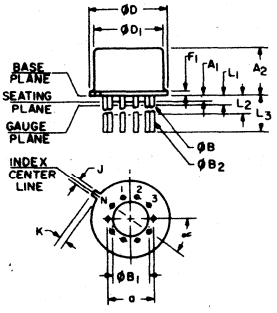
92CS-19431R2

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.200 TP		2	5.88 TP	
A_1	0.010	0.050		0.26	1.27
A_2	0.165	0.185		4.20	4.69
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0.125	0.160		3.18	4.06
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	45° TP			45° TP	
N	8		6	8	
N_1	3		5	3	

NOTES

1. Refer to JEDEC Publication No 95 for Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radium of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2 øB2 applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

(T) Suffix (JEDEC MO-006-AF), 10-Lead TO-5 Style

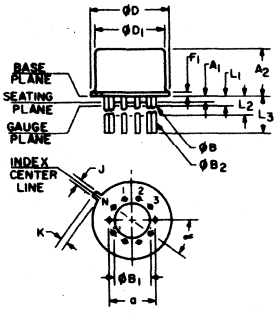


SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230 TP		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0	0		0	0
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	36° TP			36° TP	
N	10		6	10	
N_1	1		5	1	

NOTES:
1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2. $øB_2$ applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

92CS-15835

(T) Suffix (JEDEC MO-006-AG), 12-Lead TO-5 Style



92CS-19774

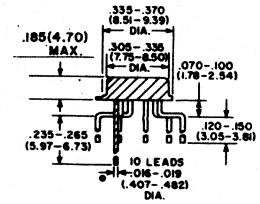
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0	0		0	0
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	30° TP			30 TP	
N	12		6	12	
N_1	1		5	1	

NOTES:
1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2. $øB_2$ applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

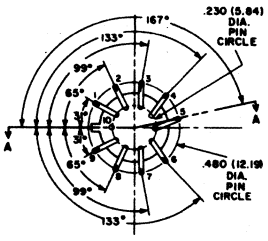
Dimensional Outlines

TO-5 STYLE PACKAGE (Cont'd)

(V) Suffix
10 Formed Leads Radially Arranged TO-5 Type (Available in 8 and 12-lead versions)

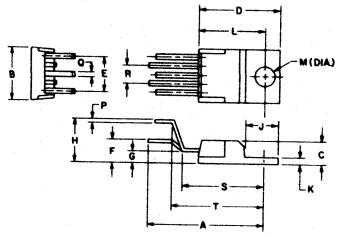


92CS-14638R2



TO-220 STYLE (VERSA-V) PLASTIC PACKAGE

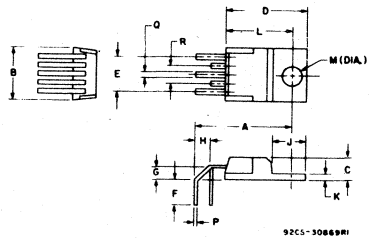
VERTICAL MOUNT



92CS-30868RI

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.876	0.896	22.25	22.75
B	0.396	0.408	10.06	10.36
C	0.173	0.182	4.395	4.622
D	0.604	0.619	15.35	15.72
E	0.263	0.273	6.681	6.934
F	0.168	0.188	4.268	4.775
G	0.100	0.104	2.540	2.641
H	0.320	0.340	8.128	8.638
J	0.246	0.254	6.249	6.451
K	0.046	0.054	1.169	1.371
L	0.496	0.508	12.60	12.90
M	0.140	0.150	3.556	3.810
N	5		5	
P	0.015	0.020	0.381	0.406
Q	0.033	0.040	0.839	1.016
R	0.129	0.139	3.277	3.530
S	0.600	0.630	15.24	16.00
T	0.680	0.710	17.27	18.03

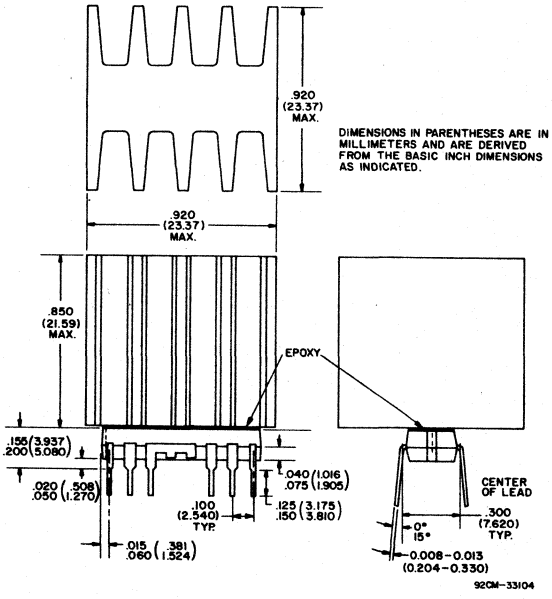
HORIZONTAL MOUNT (M Suffix)



92CS-30869RI

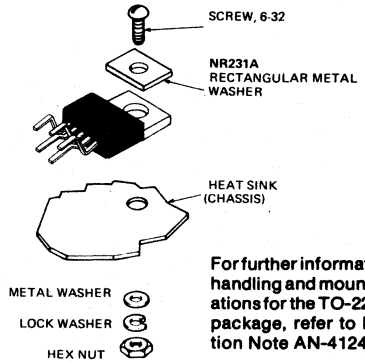
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.726	0.746	18.44	18.94
B	0.396	0.408	10.06	10.36
C	0.173	0.182	4.395	4.622
D	0.604	0.619	15.35	15.72
E	0.263	0.273	6.681	6.934
F	0.221	0.251	5.614	6.375
G	0.100	0.104	2.540	2.641
H	0.143	0.163	3.633	4.140
J	0.246	0.254	6.249	6.451
K	0.046	0.054	1.169	1.371
L	0.496	0.508	12.60	12.90
M	0.140	0.150	3.556	3.810
N	5		5	
P	0.015	0.020	0.381	0.406
Q	0.033	0.040	0.839	1.016
R	0.129	0.139	3.277	3.530

(EM) Suffix (Dual-In-Line)
Modified 16-Lead with Integral Heat Sink



92CM-33104

Suggested Hardware and Mounting Arrangement



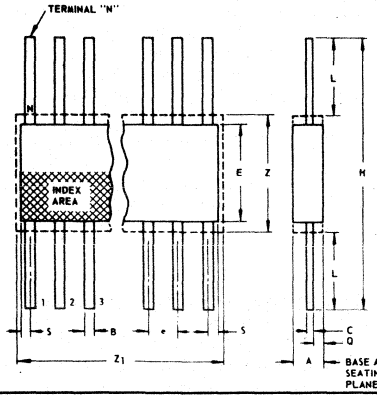
For further information regarding handling and mounting considerations for the TO-220 style plastic package, refer to RCA Application Note AN-4124.

NOTE: MAXIMUM TORQUE APPLIED TO MOUNTING FLANGE IS 8-in.-lb. (0.09 kgf-m)

92CS-29194RI

CERAMIC FLAT PACKS

(K) Suffix (JEDEC MO-004-AF), 14-Lead

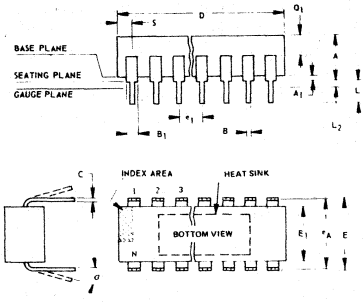


NOTES:
1. Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
2. Leads within .005" (.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92SS-4300R3

(P) Suffix
16-Lead "Power Slab" Dual-In-Line Plastic Package

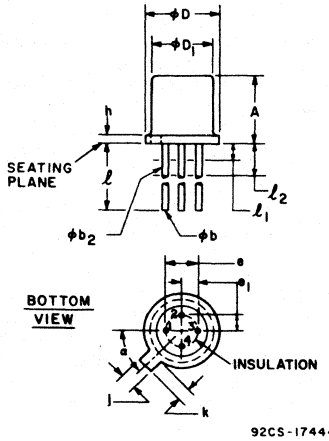


NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-32023

JEDEC TO-72 Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX	MIN	MAX	
A	0.170	0.210	4.32	5.33	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		4
e_1	0.050 T.P.		1.27 T.P.		4
h		0.030		0.762	
l	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
l	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
α	45° T.P.		45° T.P.		4, 6

Note 1 (Four leads) Maximum number leads omitted in this outline, "none" (0). The number and position of leads actually present are indicated in the product registration. Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads.

Note 2 (All leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and .500" (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond .500" (12.70 mm) from seating plane.

Note 3 Measured from maximum diameter of the product.

Note 4 Leads having maximum diameter .019" (.483 mm) measured in gaging plane .054" (1.37 mm) + .001" (.025 mm) - .000" (.000 mm) below the seating plane of the product shall be within .007" (.178 mm) of their true position relative to a maximum width tab.

Note 5 The product may be measured by direct methods or by gage.

Note 6 Tab centerline.

92CS-17444R1

Abstracts of Application Notes

AN-3193 ..... 9 pages
Application Considerations for the RCA-3N128 VHF MOS Field-Effect Transistor

This Note describes applications and vhf circuit considerations for a high-frequency n-channel MOS field-effect transistor, the RCA 3N128. Biasing requirements and basic circuit configurations are discussed, and selection of the optimum operating point and methods of automatic gain control are explained. The cross-modulation and intermodulation distortion characteristics of the 3N128 MOS transistor are compared to those of bipolar transistors, and procedures are given for the design of a practical vhf amplifier that uses the 3N128.

AN-3341 ..... 3 pages
VHF Mixer Design Using the RCA-3N128 MOS Transistor

The 3N128 is a vhf MOS field-effect transistor suitable for use throughout the vhf band (30 to 300 MHz) as an amplifier, mixer, or oscillator. This Note discusses some of the design criteria pertinent to the construction of MOS mixers, and presents an example of a complete vhf MOS converter.

AN-3452 ..... 7 pages
Chopper Circuits Using RCA MOS Field-Effect Transistors

Although electromechanical relays have long been used to convert low-level dc signals into ac signals or for multiplex purposes, relays are seriously limited with respect to life, speed, and size. Conventional (bipolar) transistors overcome the inherent limitations of relays, but introduce new problems of offset voltage and leakage currents. This Note describes the use of MOS field-effect transistors in solid-state chopper and multiplex designs that have the long life, fast speed, and small size of bipolar-transistor choppers, but that eliminate their inherent offset-voltage and leakage-current problems.

AN-3453 ..... 6 pages
An FM Tuner Using an RCA-40468 MOS-Transistor RF Amplifier

This Note describes an FM tuner that incorporates an MOS field-effect transistor as the rf amplifier, and shows how the MOS transistor is instrumental in minimizing the spurious responses normally found in FM receivers.

AN-3535 ..... 6 pages
An FM Tuner Using Single-Gate MOS Field-Effect Transistors as RF Amplifier and Mixer

Selection of the transistors for use in FM-tuner stages involves consideration of such device characteristics as spurious response, dynamic range, noise immunity, gain, and feedthrough capacitance. MOS field-effect transistors are especially suitable for use in FM rf-amplifier and mixer stages because of their inherent superiority for spurious-response rejection and signal-handling capability. This Note describes an FM tuner that uses an RCA-40468 MOS transistor as the rf amplifier and an RCA-40559 MOS transistor as the mixer.

AN-4018 ..... 5 pages
Design of Gate-Protected MOS Field-Effect Transistors

MOS (metal-oxide-semiconductor) field-effect transistors are in demand for rf-amplifier applications because their transfer characteristics make possible significantly better performance than that experienced with other solid-state devices. Unless equipped with gate protection, however, MOS transistors require careful handling to prevent static discharges from rupturing the dielectric material that separates the gate from the channel. This Note describes the design of dual-gate MOS field-effect transistors that use a built-in signal-limiting diode structure to provide an effective short circuit to static discharge and limit high potential buildup across the gate insulation.

AN-4125 ..... 7 pages
MOS/FET Biasing Techniques

Field-effect transistors are applied in rf amplifiers, and mixers, if and audio amplifiers, electrometer and memory circuits, attenuators, and switching circuits. The dual-gate MOS/FET appears to be particularly useful in rf stages because of low feedback capacitance, high transconductance, and superior cross modulation with automatic-gain-control capability. The rules for biasing FET's vary slightly depending on type. However, most possibilities are covered in this Note through examination of the biasing of a single-gate, a junction-gate, and a dual-gate transistor. Substrate biasing and biasing to compensate for temperature variations are also discussed.

AN-4431 ..... 8 pages
RF Applications of the Dual-Gate MOS/FET Up to 500 MHz

The dual-gate protected, metal-oxide silicon, field-effect transistor (MOS FET) is especially useful for high-frequency applications in rf amplifier circuits. The dual-gate feature permits the design of simple AGC circuitry requiring very low power. The integrated diodes protect the gates against damage due to static discharge that may develop during handling and usage. This Note describes the use of the RCA-3N200 dual-gate MOS FET in rf applications. The 3N200 has good power gain and a low noise factor at frequencies up to 500 MHz, offers especially good cross-modulation performance, and has a wide dynamic range; its low-feedback capacitance provides stable performance without neutralization.

AN-4590 ..... 16 pages
Using MOS/FET Integrated Circuits in Linear Circuit Applications

A brief review of MOS/FET IC device theory is given, and some linear circuit applications are surveyed. Theory discussed includes gate protection and electrical requirements. Applications include choppers, attenuators, constant-current sources, general-purpose amplifier circuits, and rf amplifiers, oscillators, and mixers.

ICAN-4072 ..... 8 pages
Applications of the RCA-CA3048 Integrated-Circuit Amplifier Array

The RCA-CA3048 integrated circuit, an array of four identical amplifiers, each with independent inputs and outputs, all on a single monolithic silicon chip, has an operating and storage temperature range of -25°C to +85°C. Each amplifier in the low-noise array has a typical open-loop gain of 58 dB and input impedance of 90,000 ohms. The gain-frequency response, stability, output swing versus supply voltage, and noise of the device are discussed. Circuit applications include Hartley and Colpitts Oscillators, astable multivibrators, a 4-channel linear mixer, a driver for a 600-ohm balanced line, and a gain-controlled amplifier.

ICAN-5015 ..... 15 pages
Application of the RCA-CA3008 and CA3010 Integrated-Circuit Operational Amplifiers

This Note describes the circuit arrangement, lists the performance characteristics, explains the major design considerations, and discusses typical applications of the CA3008 and CA3010 operational amplifiers. These amplifiers are silicon monolithic integrated circuits designed to operate from two symmetrical low- or medium-level dc power supplies (at supply voltages in the range from +3 volts to +6 volts).

Abstracts of Application Notes (Cont'd)

ICAN-5022 ..... 26 pages
Application of the RCA-CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers

The CA3004, CA3005, and CA3006 rf amplifiers are discussed. These silicon-epitaxial monolithic integrated circuits are designed to operate from low or medium levels of dc supply voltage, over a range of ambient temperatures from -55°C to +125°C, and at frequencies from dc to 100 MHz. They may be used with external tuned-circuit, transformer, or resistive load impedances to provide wide- or narrow-band amplification, mixing, limiting, product detection, frequency generation, and generation of pulse or digital waveforms.

ICAN-5030 ..... 11 pages
Application of the RCA-CA3000 Integrated-Circuit DC Amplifier

This Note describes the RCA-CA3000 dc amplifier, a stabilized and compensated differential amplifier that has push-pull outputs, high-impedance (0.1-megohm) inputs, and gain of approximately 30 dB at frequencies up to one MHz. Its useful frequency response can be increased to several tens of megahertz by the use of external resistors or coils. The CA3000 can be used as a single switch (with pedestal), a squelchable audio amplifier (with suppressed switching transient), a modulator, a mixer or a product detector. When suitable external components are added, it can also be used as an oscillator, a one-shot multivibrator, or a trigger with controllable hysteresis.

ICAN-5036 ..... 9 pages
Application of the RCA-CA3002 Integrated-Circuit IF Amplifier

The RCA-CA3002 integrated-circuit if amplifier described in this Note is a balanced differential amplifier that can be used with either a single-ended or a push-pull input and can provide either a direct-coupled or a capacitance-coupled single-ended output. Its applications include RC-coupled if amplifiers that use the internal silicon output-coupling capacitor, video amplifiers that use an external coupling capacitor, envelope detectors, product detectors, and various trigger circuits.

ICAN-5037 ..... 4 pages
Application of the RCA-CA3007 Integrated-Circuit Audio Amplifier

This Application Note describes the RCA-CA3007 audio driver, a balanced differential configuration with either a single-ended or a differential input and two push-pull emitter-follower outputs. The circuit features all-monolithic silicon epitaxial construction, and is intended for use as a direct-coupled driver in a class B audio amplifier which exhibits both gain and operating-point stability over the temperature range from -55 to +125°C.

ICAN-5038 ..... 8 pages
Application of the RCA-CA3001 Integrated-Circuit Video Amplifier

The CA3001 silicon monolithic integrated circuit is designed for use in intermediate-frequency or video amplifiers at frequencies up to 20 MHz and in Schmitt-trigger applications. This integrated circuit can be gated, and gain control can be applied. The CA3001 incorporates all-monolithic silicon epitaxial construction designed for operation at ambient temperatures from -55 to +125°C, balanced differential-amplifier configuration with low-impedance double-ended input, and a built-in temperature-compensating network for gain or dc operating-point stability over the temperature range from -55 to +125°C.

ICAN-5213 ..... 6 pages
Application of the RCA CA3015 and CA3016 Integrated-Circuit Operational Amplifiers

The integrated-circuit operational amplifiers CA3015 and CA3016 are identical in circuit configuration to the CA3008 and CA3010, but have an improved device breakdown voltage that permits operation from +12-volt supplies as well as from +6-volt or +3-volt supplies. This Note describes the operating characteristics of the CA3015 and CA3016 at +12 volts, and discusses applications that take advantage of the higher gain-bandwidth product and increased output signal swing obtained at the higher voltages: a 50-dB amplifier; a 10-dB, 42-MHz amplifier; a twin-T bandpass amplifier; and a voltage-follower.

ICAN-5269 ..... 7 pages
Integrated Circuits for FM Broadcast Receivers

This Note describes several approaches to FM receiver design using silicon monolithic integrated circuits. The tuner section is described first, and then the if-amplifier and detector sections. Performance characteristics are described where applicable. The FM receivers discussed are designed for use from a +9-volt supply. The key to design simplicity is the use of the RCA multifunction integrated circuits CA3005, CA3012, and CA3014. The CA3005 may be used as a cascode rf amplifier, a differential rf amplifier, a mixer-oscillator, and an if amplifier; the CA3012 and CA3014 perform if amplification, limiting, detection, and preamplification.

ICAN-5296 ..... 5 pages
Application of the RCA-CA3018 Integrated-Circuit Transistor Array

The CA3018 integrated circuit consists of four silicon epitaxial transistors produced by a monolithic process on a single chip mounted in a 12-lead TO-5 package. The four active devices, two isolated transistors plus two transistors with an emitter-base common connection, are especially suitable for applications in which closely matched device characteristics are required, or in which a number of active devices must be interconnected with non-integrable components such as tuned circuits, large-value resistors, variable resistors, and microfarad bypass capacitors. Such areas of application include if, rf (through 100 MHz), video, agc, audio, and dc amplifiers.

ICAN-5299 ..... 6 pages
Application of the RCA-CA3019 Integrated-Circuit Diode Array

The CA3019 integrated-circuit diode array provides four diodes internally connected in a diode-quad arrangement plus two individual diodes. Its applications include gating, mixing, modulating, and detecting circuits. Because all the diodes are fabricated simultaneously on a single silicon chip, they have nearly identical characteristics, and their parameters track each other with temperature variations. Consequently, the CA3019 is particularly useful in circuit configurations that require either a balanced diode bridge or identical diodes.

ICAN-5337 ..... 10 pages
Application of the RCA-CA3028A and CA3028B Integrated-Circuit RD Amplifiers in the HF and VHF Ranges

The CA3028A and CA3028B monolithic-silicon integrated circuits are single-stage differential amplifiers intended for service in communications systems operating at frequencies up to 100 MHz with single power supplies. This Note provides technical data and recommended circuits for use of the CA3028A and CA3028B in rf amplifiers, autodyne converters, if amplifiers, and limiters. The CA3028A and CA3028B are suitable for use in a wide range of applications in dc, audio, and pulse amplifier service; they have been used as sense amplifiers, preamplifiers for low-level transducers, and dc differential amplifiers.

Abstracts of Application Notes (Cont'd)

ICAN-5338 ..... 14 pages
Application of the RCA-CA3021, CA3022, and CA3023 Integrated-Circuit, Wideband Amplifiers

The CA3021, CA3022, and CA3023 integrated circuits are multipurpose high-gain amplifiers designed for use in video and AM or FM if stages in single-power-supply systems. Specifically, they can be used in video amplifiers operating at frequencies through 30 MHz. AM and FM if amplifiers, and buffer amplifiers in which an isolation capability greater than 60 dB at 1 MHz is desired.

ICAN-5380 ..... 7 pages
Integrated-Circuit Frequency-Modulation IF Amplifiers

The discussion in this Note shows that the simplest approach to the use of the CA3012 and CA3028 integrated circuits in FM if-amplifier strips is to replace each stage in present discrete-transistor if strips with a differential amplifier. This integrated-circuit approach requires a minimum of re-engineering because a cascade of individually tuned if stages is used. From a performance point of view, this approach results in better AM rejection than that obtained with discrete circuits because of the inherent limiting achieved with the differential-amplifier configuration.

ICAN-5766 ..... 8 pages
Application of the RCA-CA3020 and CA3020A Integrated-Circuit Multipurpose Wideband Power Amplifiers

The CA3020 and CA3020A integrated circuits are multipurpose, multifunction power amplifiers designed for use as power-output amplifiers and driver stages in portable and fixed communications equipment and in ac servo-control systems. The flexibility of these circuits and the high-frequency capabilities of the circuit components make these types suitable for a wide variety of applications such as broadband amplifiers, video emplifiers, and video line drivers. Voltage gains of 60 dB or more are available, with a 3-dB bandwidth of 8 MHz. Applications covered include audio, wideband, and driver amplifiers.

ICAN-5841 ..... 4 pages
Feedback-Type Volume-Control Circuits for RCA-CA3041 and CA3042 Integrated Circuits

This Note describes feedback-type volume controls for use with RCA-CA3041 and CA3042 integrated circuits in television receivers. In television sets using these integrated circuits, the volume control is often located remote from the amplifier. The long leads required in such a configuration sometimes pick up undesirable signals that, in turn, cause the system to exhibit hum and noise at low volume levels. The proposed feedback-type volume control reduces hum and noise pick-up by reducing the gain of the system rather than the signal level, and thus eliminates the cost of shielding the leads.

ICAN-6048 ..... 12 pages
Some Applications of a Programmable Power Switch/Amplifier

The CA3094 monolithic programmable power switch/amplifier IC consists of a high-gain preamplifier driving a power-output amplifier stage. It can deliver average power of 3 watts or peak power of 10 watts to an external load, and can be operated from either a single or dual power supply. This Note briefly describes the characteristics of the CA3094, and illustrates its use in applications such as class A instrumentations and power amplifiers, class A driver-amplifiers for complementary power transistors, wide-frequency-range power multivibrators, current- or voltage-controlled oscillators, comparators (threshold detectors), voltage regulators, analog timers (long time delays), alarm systems, motor-speed controllers, thyristor-firing circuits, battery-charge regulator circuits, and ground-fault-interrupter circuits.

ICAN-6077 ..... 12 pages
An IC Operational-Transconductance-Amplifier (OTA) with Power Capability

This Note defines the OTA and describes two circuits of this type, the CA3080 and the CA3094. The single, highly linear operational-transconductance-amplifier, the CA3080, because of its extremely linear transconductance characteristics with respect to amplifier bias current, has gained wide acceptance as a gain-control block. The CA3094 improved on the performance of the CA3080 through the addition of a pair of transistors; these transistors extended the current-carrying capability to 300 milliamperes, peak. The CA3094, is useful in an extremely broad range of circuits in consumer and industrial applications; this Note describes only a few of the many consumer applications.

ICAN-6157 ..... 12 pages
Applications of the CA3085-Series Monolithic IC Voltage Regulators

This Note describes the basic circuit of the CA3085-series devices and some typical applications that include a high-current regulator, constant-current regulators, a switching regulator, a negative-voltage regulator, a dual-tracking regulator, high-voltage regulators, and various methods of providing current limiting. A circuit in which the CA3085 is used as a general-purpose amplifier is also shown.

ICAN-6182 ..... 32 pages
Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3058, CA3059, and CA3079)

CA3058, CA3059, and CA3079 zero-voltage switches are monolithic integrated circuits designed primarily for use as trigger circuits for thyristors in many highly diverse ac power-control and power-switching applications. This Note discusses the operation and application of these circuits.

ICAN-6247 ..... 8 pages
Application of the CA3126Q Chroma-Processing IC Using Sample-and-Hold Circuit Techniques

This Note describes the CA3126Q monolithic integrated circuit intended for use in processing the chrominance signal in a color television receiver. In performing the functions of color subcarrier regeneration and chroma control, emphasis has been placed on utilizing all the information available in the signal so as to approach ultimate system performance capability, while at the same time substantially reducing the number of external components and adjustments.

ICAN-6257 ..... 8 pages
Application of the CA3089E FM-IF Subsystem

The CA3089E, is an FM-IF subsystem intended for use in FM receiver applications. In addition to the amplifier-limiter and quadrature detector sections, the CA3089E provides such auxiliary functions as mute, AFC output, tuning-meter output, and delayed rf-AGC. This Note briefly describes each circuit section and discusses practical aspects of designing with this device.

ICAN-6259 ..... 10 pages
Integrated-Circuit Stereo Decoder Using the CA3090AQ Stereo Multiplex Demodulator

The CA3090AQ integrated circuit provides features heretofore unavailable to the receiver designer. This device needs only a single tuning adjustment, which reduces to a minimum the manual effort during assembly; the phase-locked loop maintains performance under conditions of temperature variations, humidity, and aging. The compactness of the CA3090AQ and of the required external components, added to the other attributes, makes this stereo decoder a significant advancement in the state of the art of stereo decoder designs.

Abstracts of Application Notes (Cont'd)

ICAN-6302 ..... 9 pages
Description and Application of the RCA-CA3120E Integrated-Circuit TV-Signal Processor

The CA3120E is a 16-pin, dual-in-line monolithic-silicon integrated circuit that processes a video signal and provides the following outputs: non-inverted video output; noise-processed, inverted video output; dual-polarity, composite synchronization signals; and automatic gain-control signals (agc). The IC, which can be used in color or monochrome TV receivers, requires a single-polarity power supply (positive) and includes impulse-noise inversion and delay circuits that reduce the deleterious effects of impulse noise in the receiver agc and synchronization (sync) circuits. Standard agc strobing techniques are also used. The agc and impulse-noise thresholds are automatically set and require no controls. The if maximum-gain bias and the tuner agc delay may be adjusted for optimum TV-receiver performance; the time constant for the sync-separator input can also be optimized by the set designer.

ICAN-6303 ..... 16 pages
A Single IC for the Complete PIX-IF-System in TV Receivers

The CA3068 linear integrated circuit is a PIX-IF-sybsystem in a shielded, quad-formed, dual-in-line, 20-lead, plastic package. This package contains all the active devices and most of the passive elements necessary for a high performance, PIX-IF-system for a TV receiver. This Note describes the receiver functions performed by the CA3068, and its application to color and monochrome TV receivers.

ICAN-6668 ..... 16 pages
Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers

The CA3080 and CA3080A are similar in generic form to conventional operational amplifiers, but differ sufficiently to justify an explanation of their characteristics. This class of operational amplifier includes not only the usual differential input terminals, but an additional control terminal that enhances the device's flexibility. This Note describes the operation of the OTA and features various circuits using it. For example, communications and industrial applications, including modulators, multiplexers, sample-and-hold circuits, gain control circuits and micropower comparators, are shown and discussed. These circuits show the operation of the OTA in conjunction with CMOS devices as post-amplifiers.

ICAN-6728 ..... 8 pages
Application of the CA3134E Sound IF and Output Subsystems in Television Receivers

In the CA3134, the sound IF and audio output subsystems for color or black-and-white television receivers are combined in a single monolithic integrated circuit. The consolidation of these functions into an integrated circuit minimizes the number of components needed and reduces the area of the printed-circuit board necessary for this portion of a television receiver. This consolidation also permits a reduction in manufacturers' component inventories and simplifies field servicing. Circuit characteristics, functions, and applications are discussed.

ICAN-6732 ..... 8 pages
Measurement of Burst ("Popcorn") Noise in Linear Integrated Circuits

The advent in recent years of very high-gain operational amplifiers operating in the 1/f noise-frequency spectrum has placed emphasis on the need for very low-noise devices. This need is particularly true for operational amplifiers which have either low-offset characteristics and/or offset-null capability.

The traditional methods used to select very-low-noise devices for operational amplifiers involve the measurement of either spot or wideband (≈10 kHz) noise figures in the 1/f frequency range (10 Hz to 10 kHz) at various source resistances. This type of measurement, however, only provides an indication of the average noise power at the measurement frequency and does not reveal the burst ("popcorn") noise characteristics of the Device Under Test (DUT). This Note describes in detail a test that will detect burst noise.

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ECS Hilmar Frehsdorf GmbH Electronic Components Service
Carl-Zeiss Strasse 3
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Churchill Roosevelt Highway
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